

ADC12D1600RF

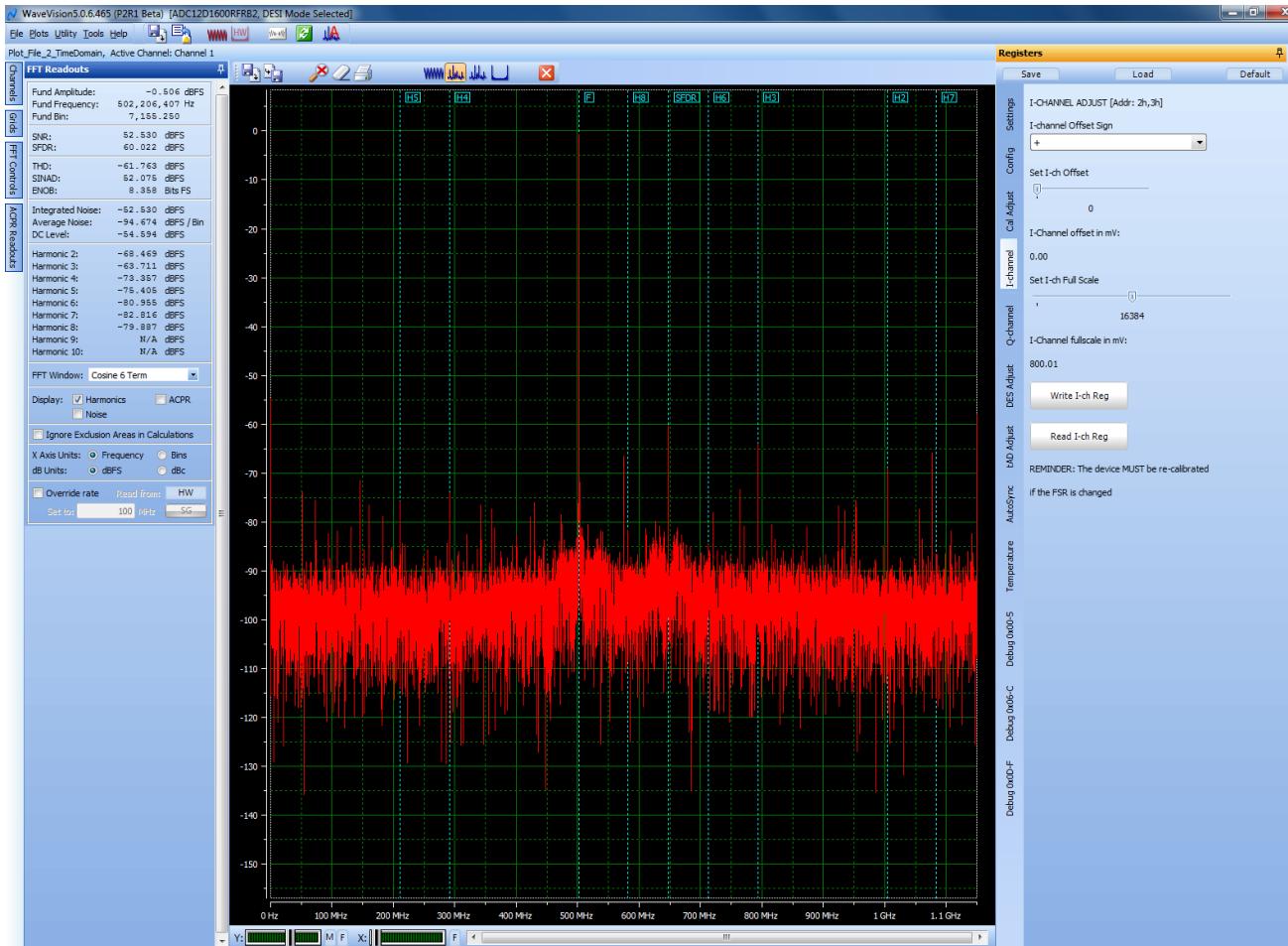
DESxx Interleave Spur Evaluation

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Setup

- ADC12D1600RFRB with ext clock
- Fclk = 1150 MHz @ 4.2dBm via tunable BPF
- DES mode so Fs = 2300 MSPS
- Fin = 1797.77MHz via tunable BFP
- DESI using Hyperlabs balun
- DESIQ using ADC-DESIQ-BB
- Fin folds to $1150 - (1797.77 - 1150) = 502.23\text{MHz}$
- $F_s/2 - \text{Fin}$ is at $1150 - 1797.77 = -647.77\text{MHz}$ which folds to 647.77MHz

DESI after DES-TA



DESIQ after DES-TA

