User options for analog input:
1. S/E input, AC-coupled:
   a. Default populate option
   b. Balun is {400MHz, 3GHz}
2. Differential DC-coupled:
   a. Remove C45, C69.
   b. Populate C33 = C70 = 0 ohm.
3. Differential AC-coupled:
   a. Remove C45, C69.
   b. Populate C33 = C70 = 100 pF.

Let C1 and C3 share a pad on the common net. Route from VIN_DIFF+ to VIN_P net as 50 ohm S/E.

Let C5 and C6 share a pad on the common net. Route from VIN_DIFF- to VIN_N net as 50 ohm S/E.

Let C32 and C30 share a pad on the common net. Let C33 and C36 share a pad on the common net.

Let R18 and R19 share a pad on the common net. Let R20 and R21 share a pad on the common net.

Locate VIN_SE, TMST+, TMST- at edge opposite FMC connector

Priorities for placement:
1. Decoupling caps close to IC.
2. J_VA12, J_VA19, J_VD12 close to IC.

The IC pad is the only ground connection for this IC. Ensure good connection through multiple vias to the PCB ground planes.

Locate close to U2A output pins to minimize stubs

Designed for: Internal Use Only	Mod. Date: 8/1/2013
Project Title: ADC12J4000 / LM15851 EVAL BOARD	
Number: SV600847 Rev: E3	Sheet Title:
SVN Rev: Not in version control	Assembly Variant: 002 Sheet: 1 of 7
Drawn By:	File: SV600847E3_1_ADC_IO.SchDoc Size: B
Engineer: Marjorie Plisch	Contact: http://www.ti.com/support

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The D<7:0> connections polarity have
been swapped from the TI standard
FMC ADC guidelines to ease routing.
This is accounted for in the FPGA code.

FMC_RX1A

DP1_M2C_P / DP1_M2C_N — D1_N / D1_P
DP2_M2C_P / DP2_M2C_N — D2_N / D2_P
DP3_M2C_P / DP3_M2C_N — D3_N / D3_P
DP4_M2C_P / DP4_M2C_N — D4_N / D4_P
DP5_M2C_P / DP5_M2C_N — D5_N / D5_P
D7_N / D7_P — DP7_M2C_P / DP7_M2C_N
D6_N / D6_P — DP6_M2C_P / DP6_M2C_N

ASP-134488-01

PG_RX1

VADJ_RX — RR6 4.99k

PG_C2M_RX — PG_M2C_RX

FMC_RX1B

DP0_M2C_P / DP0_M2C_N — D0_N / D0_P

GBTCLK0_M2C_P — DEVCLKARX_P
GBTCLK0_M2C_N — DEVCLKARX_N

LM15851_OR_T1

FMC_SCL
FMC_SDA
KC705_JTAG
3P3VAUX

12P0V_RX — EE_ADDR0_RX
EE_ADDR1_RX

3P3V_RX — 3P3RX — R132 0

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FMC_RX1C

NCO_0
NCO_1
NCO_2

VADJ_RX

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FMC_RX1D

LA00_P_CC / LA00_N_CC — DEVCLKBRX_P / DEVCLKBRX_N
LA03_P / LA03_N — SYSREFRX_P / SYSREFRX_N
LA08_P / LA08_N — SYNC_P / SYNC_N

LMX2581_CE
LMX2581_BUFEN

LM15851_OR_T0

FMC_SPI_CLK
FMC_SPI_SCSb1
FMC_SPI_SCSb2
FMC_ADC_SDI
FMC_ADC_SDO

SYNC_SE
FMC_SPI_SDIO
FMC_ADC_CLK
FMC_ADC_SCSb0

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PRSNT_M2C_L_RX

FMC_RX1E

LMK04828_SYNC
LMK04828_RESET

VIO_B_M2C_RX — RR7 0

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3P3VAUX

U16
C143 1µF

FMC_SDA
FMC_SCL

VSS VCC SDA SCL A2 A1 A0 NC
EE_ADDR1_RX
EE_ADDR0_RX

24C65T/SM

J1
TSW-104-07-G-S

3P3VAUX

Designed for: Internal Use Only	Mod. Date: 7/23/2013
Project Title: ADC12J4000 / LM15851 EVAL BOARD	
Number: SV600847 Rev: E3	Sheet Title:
SVN Rev: Not in version control	Assembly Variant: 002
Drawn By:	Sheet: 2 of 7
Engineer: Marjorie Plisch	File: SV600847E3_2_FMC.SchDoc Size: C
	Contact: http://www.ti.com/support

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Connect decoupling caps according to the following:
1. VccCP (Pin 6) - GND (Pin 8)
2. VccPLL (Pin 10) - GND (Pin 9)
3. VccDIG (Pin 28) - GND (Pin 27)
4. VccFRAC (Pin 32) - GND (Pin 31)
5. Very important - ensure a solid trace connects Pin 18 to caps on Pins 19, 22, 23, and 24.

VIO_3P3V_LMX
L1
120 ohm
C94 100pF
C213 100pF
C91 100pF
C75 100pF
C78 100pF
C76 100pF
C77 100pF
C89 100pF
C88 100pF
C95 100pF
C84 2.2µF
C82 10µF
C83 22µF
C80 10µF
C81 22µF
C85 0.01µF
C87 0.1µF
C101 100pF
LMX_OutA-
LMX_OutA_N
Place close to IC
R37 51
C99 100pF
R38 51
C93 100pF
R46 1.3k
LMX_OutA+
LMX_OutA_P
C96 100pF
C97 100pF
LMX2581_BUFEN
LMX_OutB+
LMX_OutB_P
LMX_OutB-
LMX_OutB_N
C100 100pF
R35 51
C98 100pF
R36 51
C79 0.1µF
U4
LMX2581SQ/NOPB
VCCCP
VCCPL
VCCBUF
VCCVCO
VCCDIG
VCCFRAC
Fin
RFoutA+
RFoutA-
BUFEN
RFoutB+
RFoutB-
OSCin
GND
PAD
VrefVCO
VbiasCOMP
VregVCO
VbiasVCO
Vtune
FLout
CPout
LD
MUXout
DATA
CLK
LE
CE
RFoutA_P
RFoutA_N
RFoutB_P
RFoutB_N
LMK_LMX_DATA
LMK_LMX_CLK
LMX2581_LE
Vtune
FLout
R34 DNP 430
C90 0.022µF
R33 430
C86 1500pF
C92 680pF
Loop Filter
MUX
TP_LD
R142 0
R143 0 DNP
FTDI_LMX_R2
FTDI_LMX_R1
R99 270 DNP
R100 270
MUXout Green
LD Green
VIO_3P3V_LMX
R117 1.3k
LMX2581_CE
R133 1.00k
R26 9.09k DNP
C74 0.1µF DNP
GND_OSC
Y1
CWX813-100.0M
100MHz
R24 0
C73 1µF
R30 0
R27 56
R29 18
R28 68
R25 0 DNP
OSCin
SASF546-P26-X1

Designed for: Internal Use Only	Mod. Date: 7/31/2013
Project: ADC12J4000 / LM15851 EVAL BOARD	
Sheet Title: LMX2581	Sheet: 3 of 7
Size: B	Schematic: 870PRJ_BasePN Rev: E3
Assembly Variant: 002	
File: SV600847E3_3_LMX2581.SchDoc	
Contact: http://www.ti.com/support	

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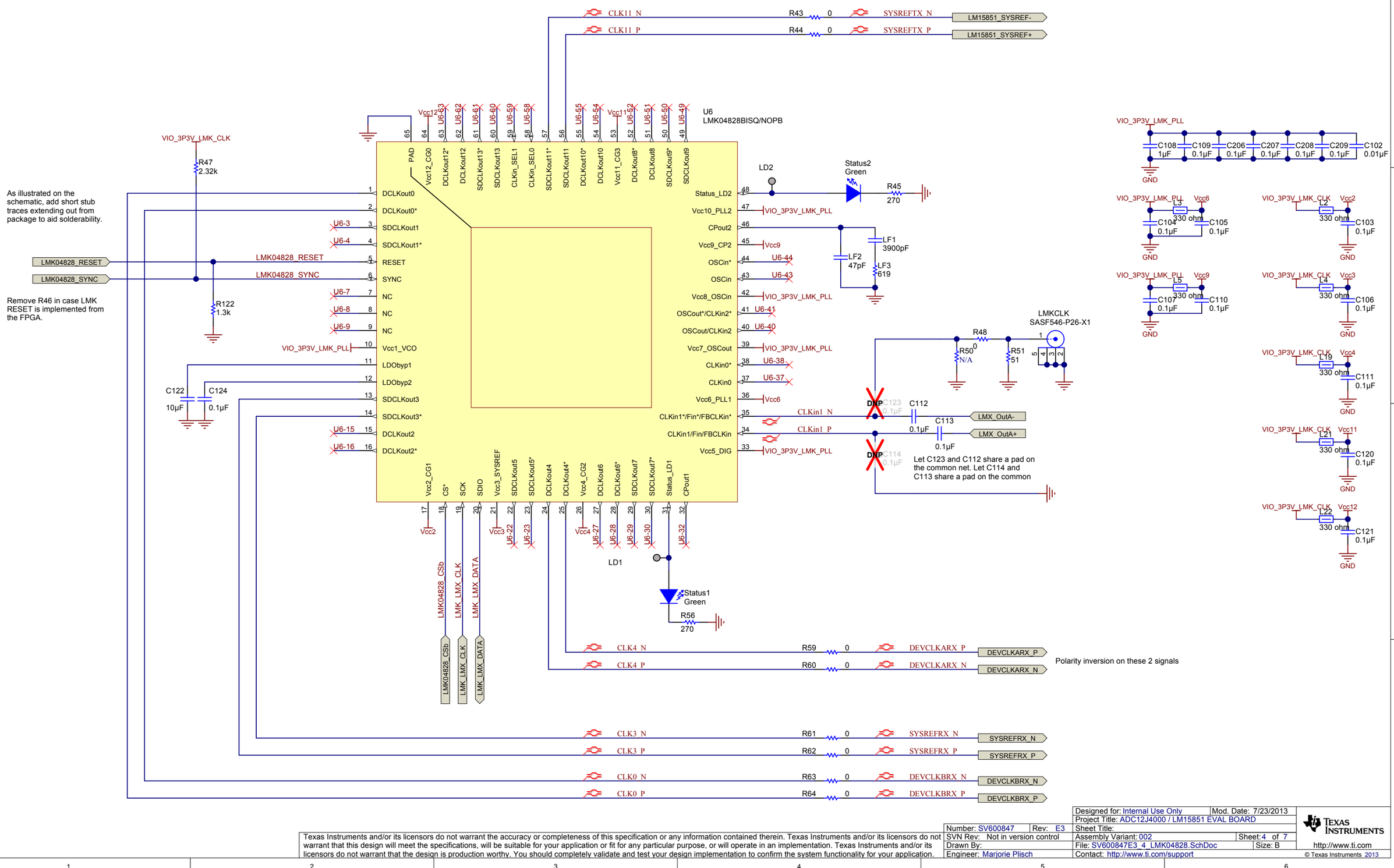

Designed for: Internal Use Only		Mod. Date: 7/23/2013	
Project Title: ADC12J4000 / LM15851 EVAL BOARD			
Number: SV600847	Rev: E3	Sheet Title:	
SVN Rev: Not in version control		Assembly Variant: 002	Sheet: 4 of 7
Drawn By:		File: SV600847E3_4_LMK04828.SchDoc	Size: B
Engineer: Marjorie Plisch		Contact: http://www.ti.com/support	

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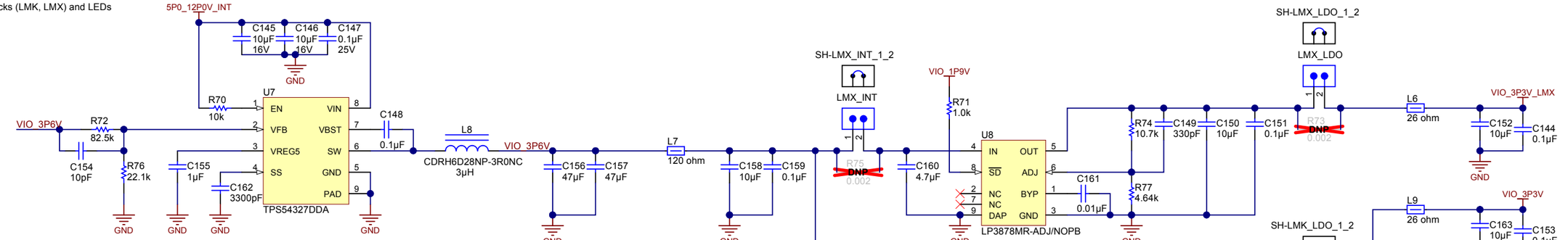
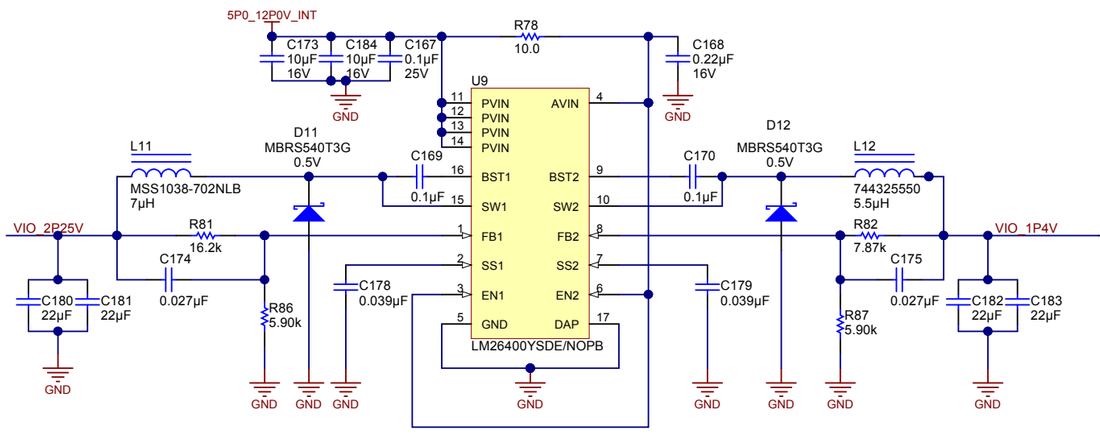
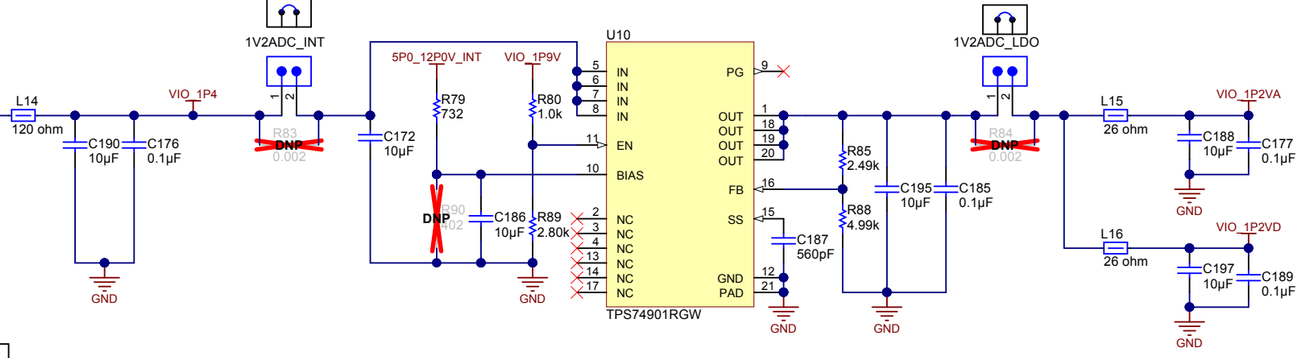
3.3V supply to clocks (LMK, LMX) and LEDs



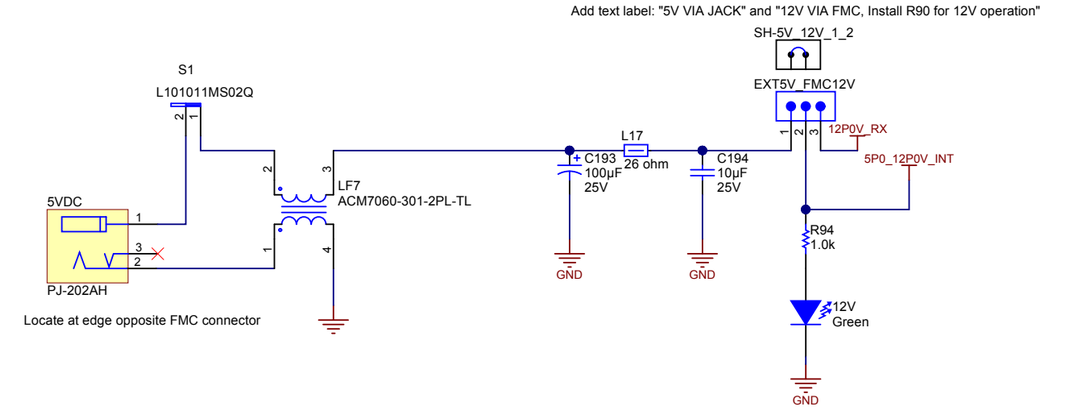
1.9V and 1.2V supply to LM15851 / ADC12X3500RF

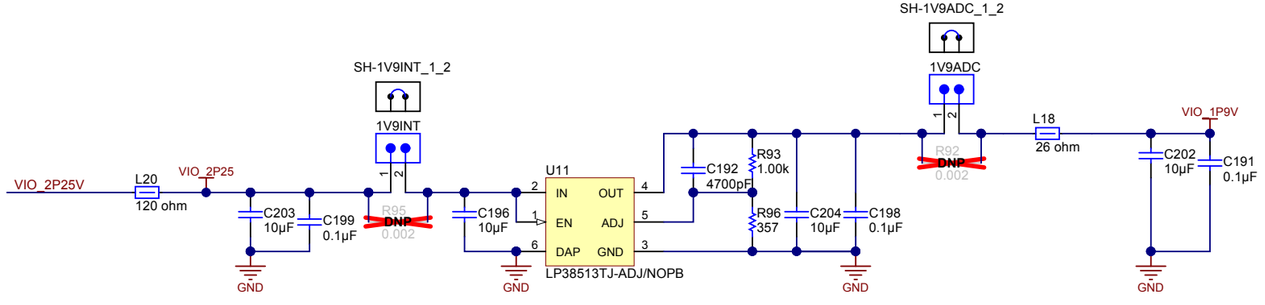




12V main supply, from jack or via FMC connector to regulators

Add text label: "5V VIA JACK" and "12V VIA FMC, Install R90 for 12V operation"





Number: SV600847	Rev: E3	Designed for: Internal Use Only	Mod. Date: 11/26/2013
SVN Rev: Not in version control		Project Title: ADC12J4000 / LM15851 EVAL BOARD	
Drawn By:		Sheet Title:	
Engineer: Marjorie Plisch		Assembly Variant: 002	Sheet: 5 of 7
		File: SV600847E3_5_Power.SchDoc	Size: B
		Contact: http://www.ti.com/support	

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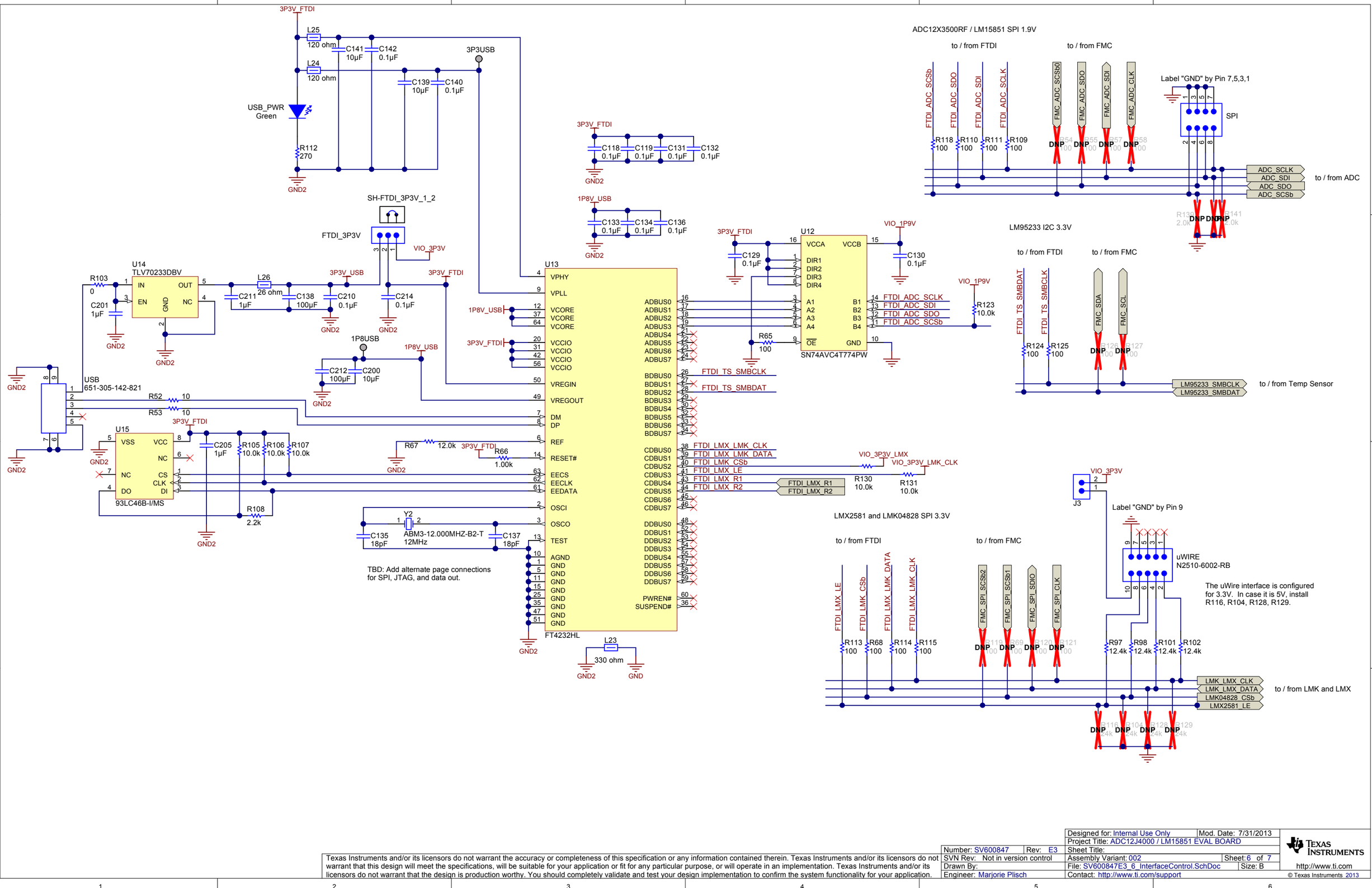

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Number: SV600847	Rev: E3	Designed for: Internal Use Only	Mod. Date: 7/31/2013
SVN Rev: Not in version control		Project Title: ADC12J4000 / LM15851 EVAL BOARD	
Drawn By:		Sheet Title:	
Engineer: Marjorie Plisch		Assembly Variant: 002	Sheet: 6 of 7
		File: SV600847E3_6_InterfaceControl.SchDoc	Size: B
		Contact: http://www.ti.com/support	

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FID1

PCB Number: SV600847
PCB Rev: E3

PCB
ESD LOGO
ESD Susceptible

PCB
LOGO
Texas Instruments

H6
H4
1902A
NY PMS 440 0025 PH

H5
H3
1902A
NY PMS 440 0025 PH

FID2

FID3

H9
MECH
FMC - FMC Screw
PMSSS 256 0075 PH

H10
MECH
FMC - FMC Nut

H11
MECH
FMC - FMC Screw
PMSSS 256 0075 PH

H12
MECH
FMC - FMC Nut

GND GND1 GND2 GND3

Place at least two of the GND test points in the power section.

LBL1
PCB Label
Size: 0.65" x 0.20 "

ZZ1
Label Assembly Note
This Assembly Note is for PCB labels only

ZZ2
Assembly Note
These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ3
Assembly Note
These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4
Assembly Note
These assemblies must comply with workmanship standards IPC-A-610 Class 2., unless otherwise specified.

VIO_3P3V C215 0.1µF GND
VIO_3P3V C216 0.1µF VIO_3P3V_LMX
VIO_3P3V C217 0.1µF VIO_3P3V_LMX
VIO_3P3V C218 0.1µF GND
VIO_1P4 C219 0.1µF VIO_3P3V
VIO_3P3V C220 0.1µF 5P0_12P0V_INT
VIO_1P4 C221 0.1µF 5P0_12P0V_INT

VIO_2P25 C222 0.1µF 5P0_12P0V_INT
VIO_2P25 C223 0.1µF 5P0_12P0V_INT
VIO_1P4 C224 0.1µF VIO_3P3V
VIO_1P4 C225 0.1µF 5P0_12P0V_INT
VIO_2P25 C226 0.1µF 5P0_12P0V_INT
VIO_2P25 C227 0.1µF 5P0_12P0V_INT

Designed for: Internal Use Only		Mod. Date: 11/25/2013	
Project Title: ADC12J4000 / LM15851 EVAL BOARD			
Number: SV600847	Rev: E3	Sheet Title:	
SVN Rev: Not in version control		Assembly Variant: 002	Sheet: 7 of 7
Drawn By:		File: SV600847E3_7_Hardware.SchDoc	Size: B
Engineer: Marjorie Plisch		Contact: http://www.ti.com/support	

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