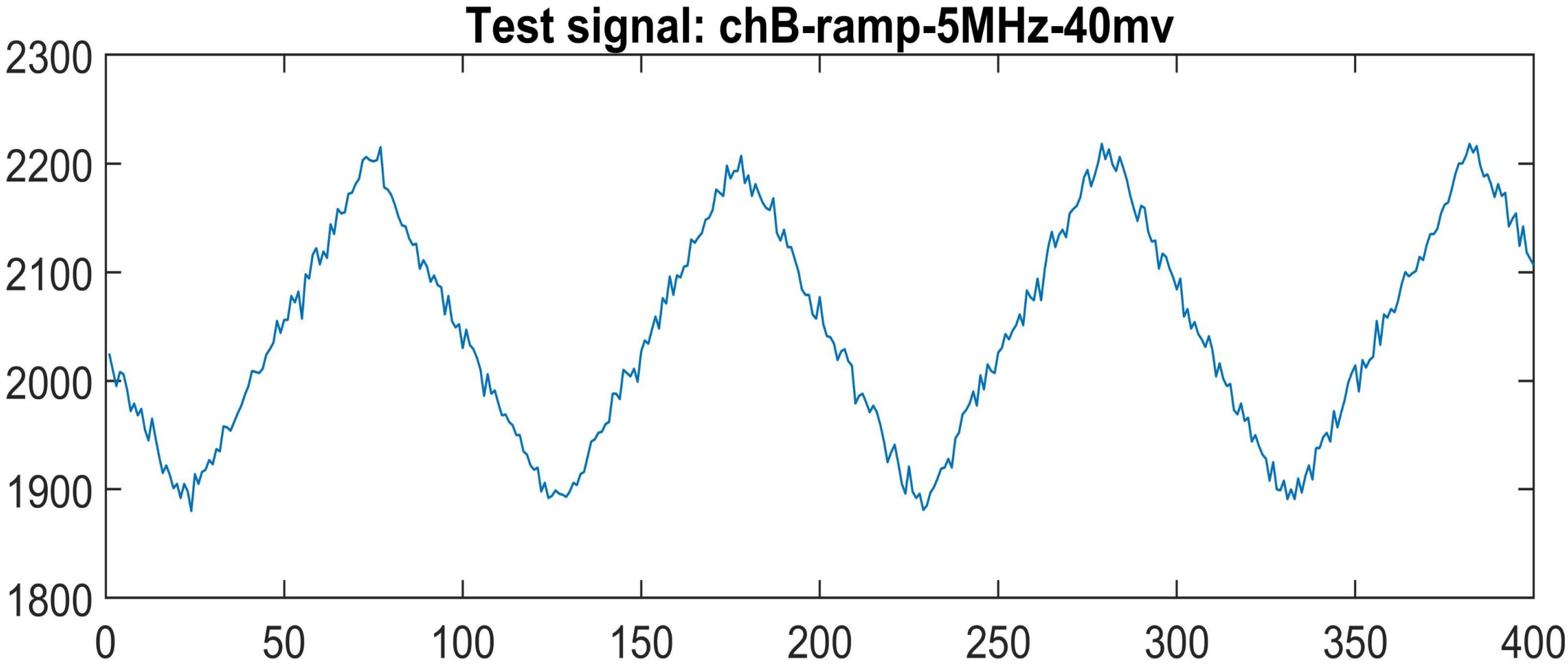
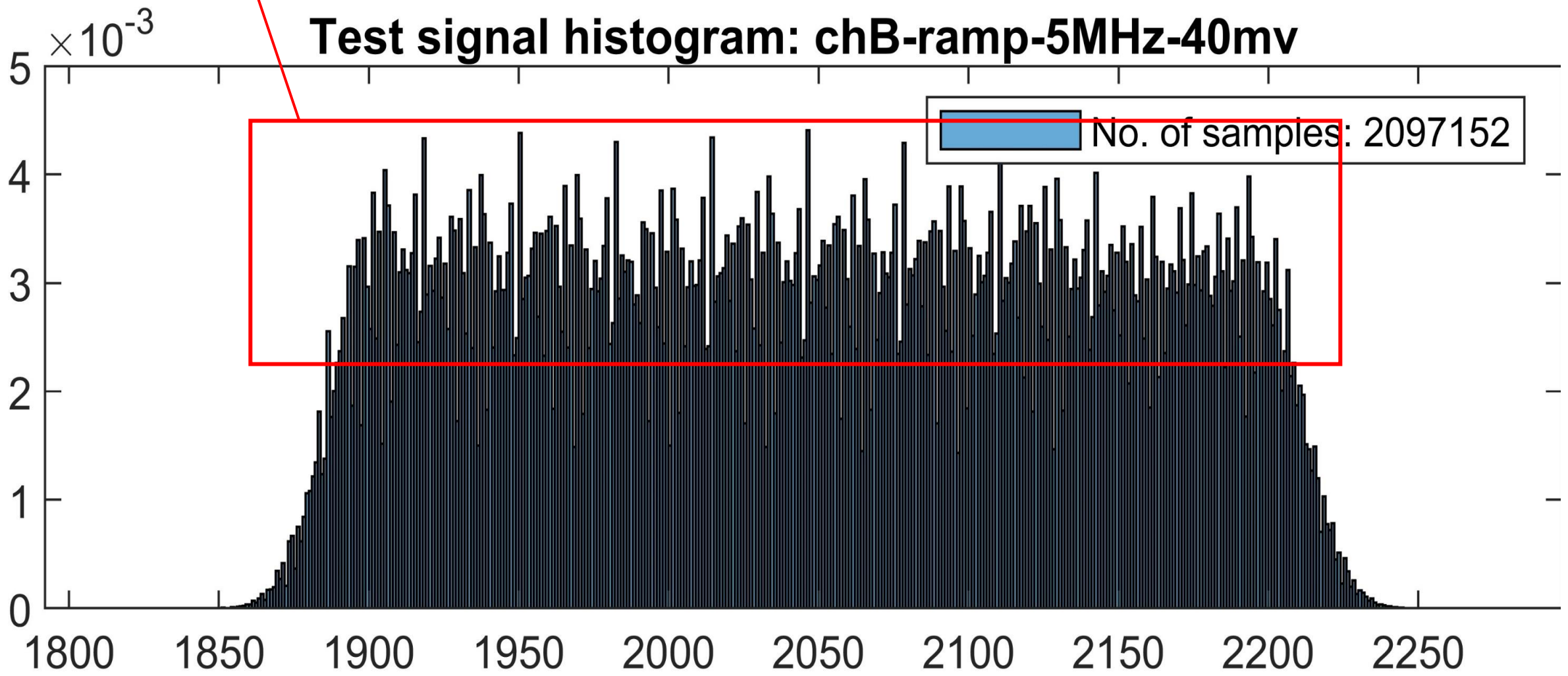
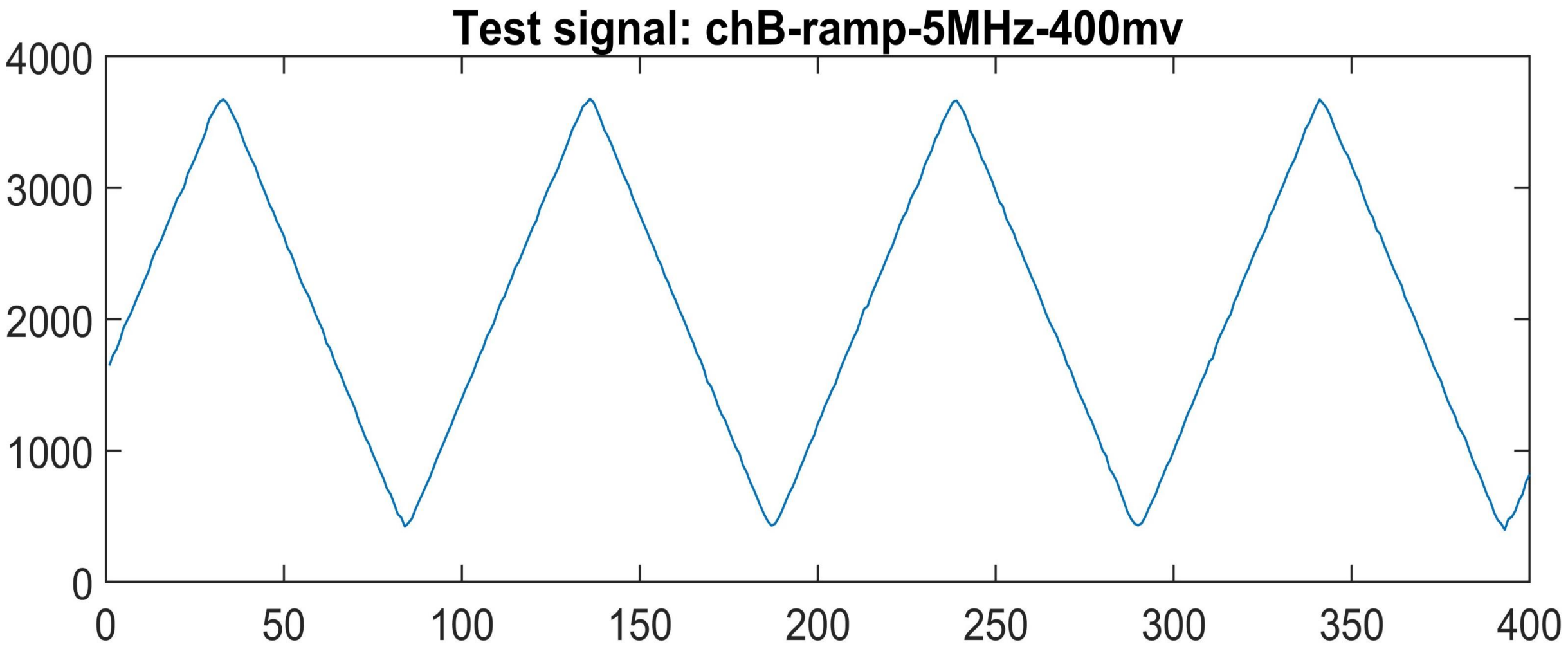
SECTION A: EXPERIMENTS DONE (1. RAMP SIGNAL AS INPUT with 40mV)

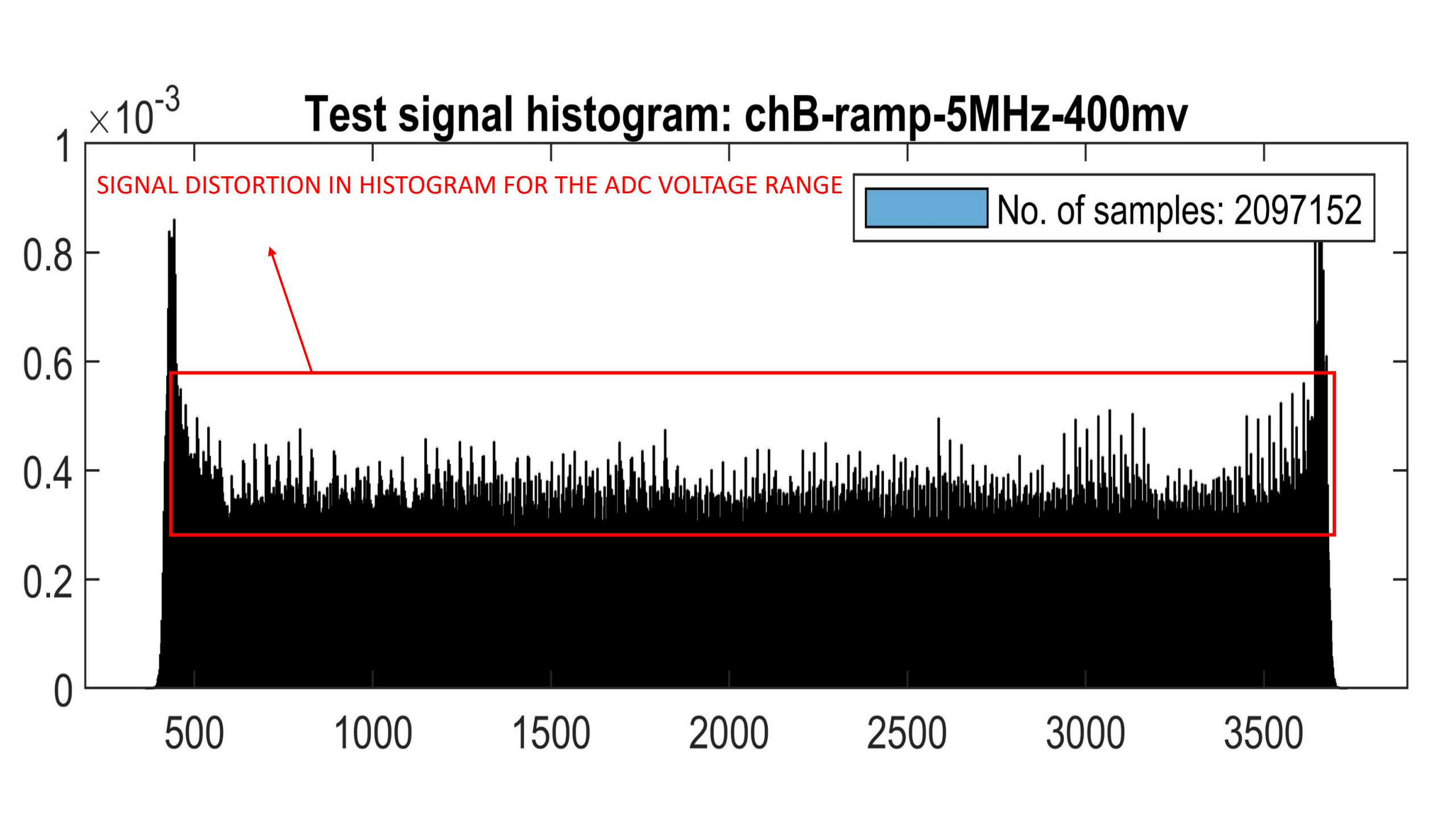


SIGNAL DISTORTION IN HISTOGRAM FOR THE ADC VOLTAGE RANGE

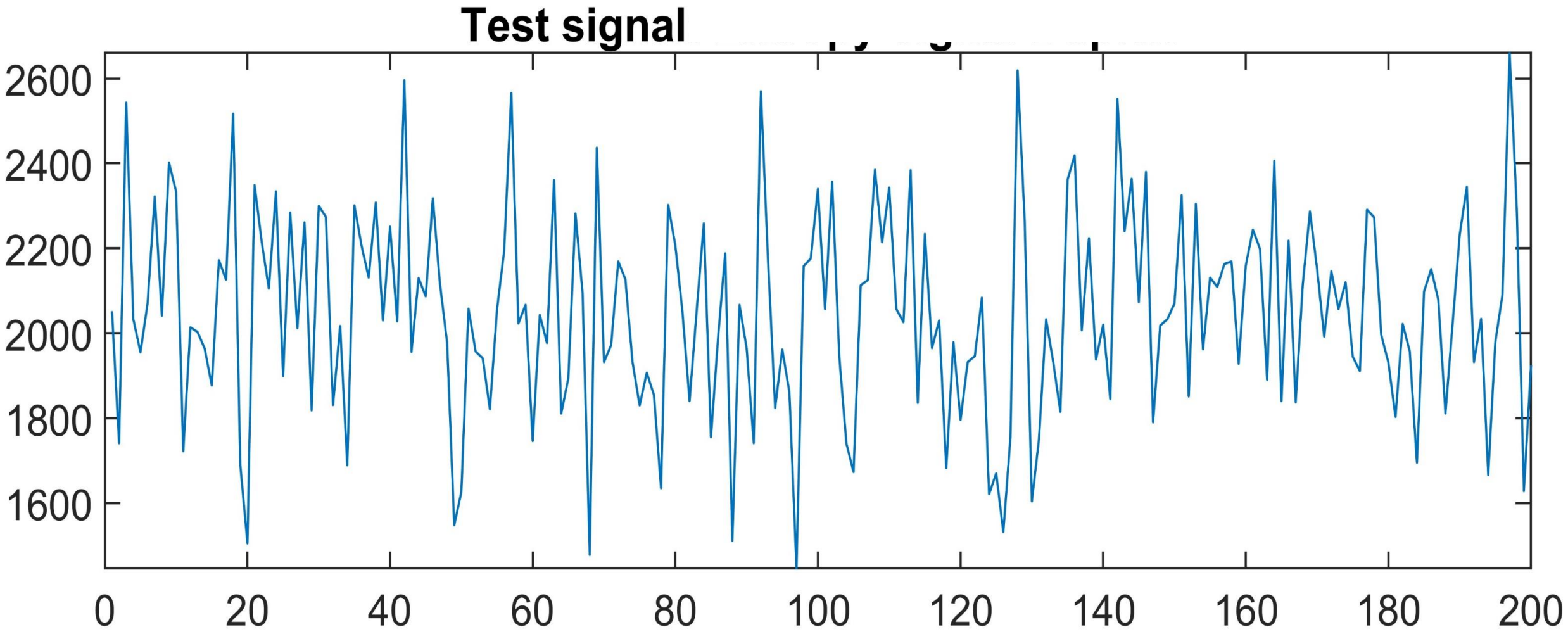


SECTION A: EXPERIMENTS DONE (2. RAMP SIGNAL AS INPUT with 400mV)

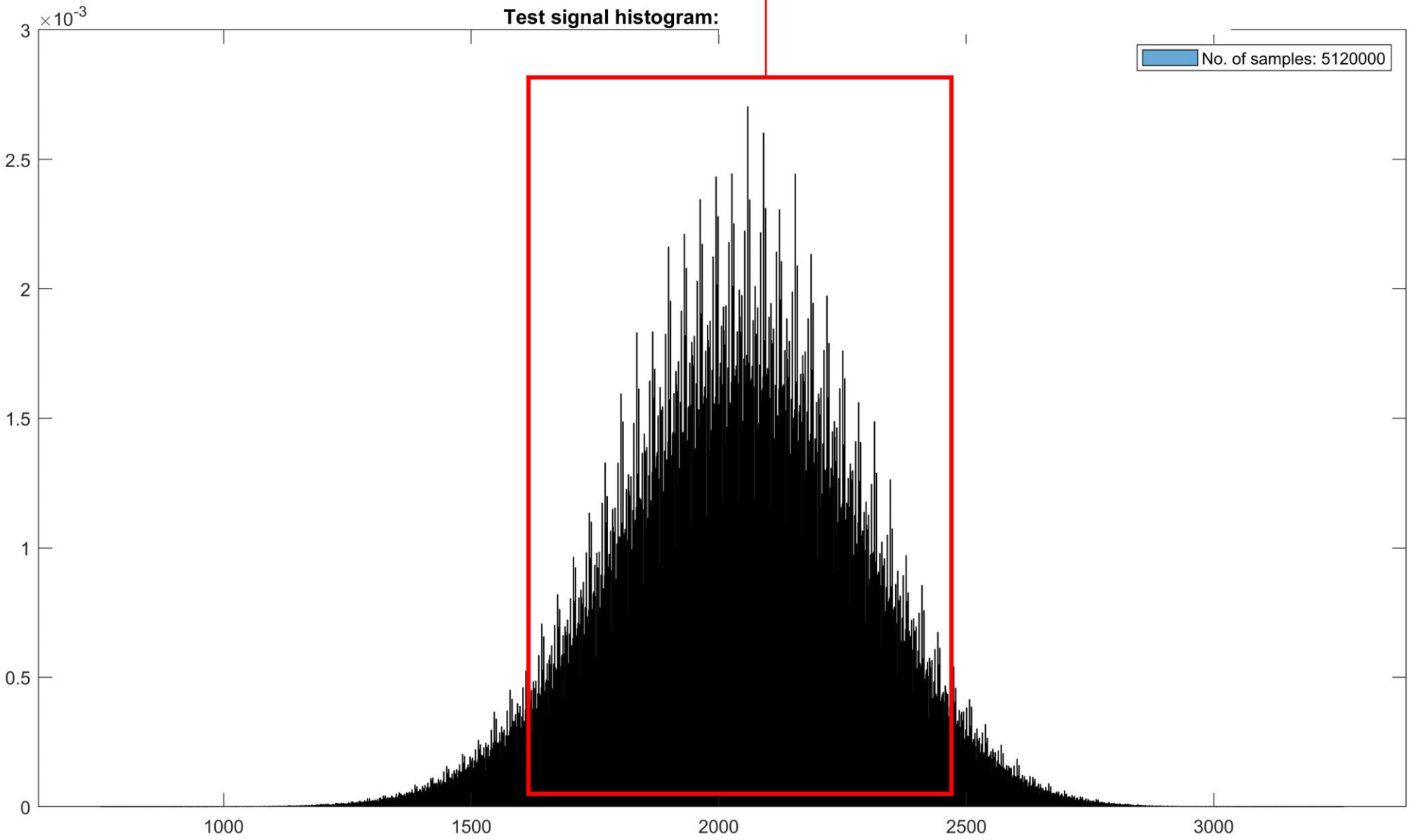



Test signal histogram: chB-ramp-5MHz-400mv
×10-3
1
0.8
0.6
0.4
0.2
0
SIGNAL DISTORTION IN HISTOGRAM FOR THE ADC VOLTAGE RANGE
No. of samples: 2097152
500
1000
1500
2000
2500
3000
3500

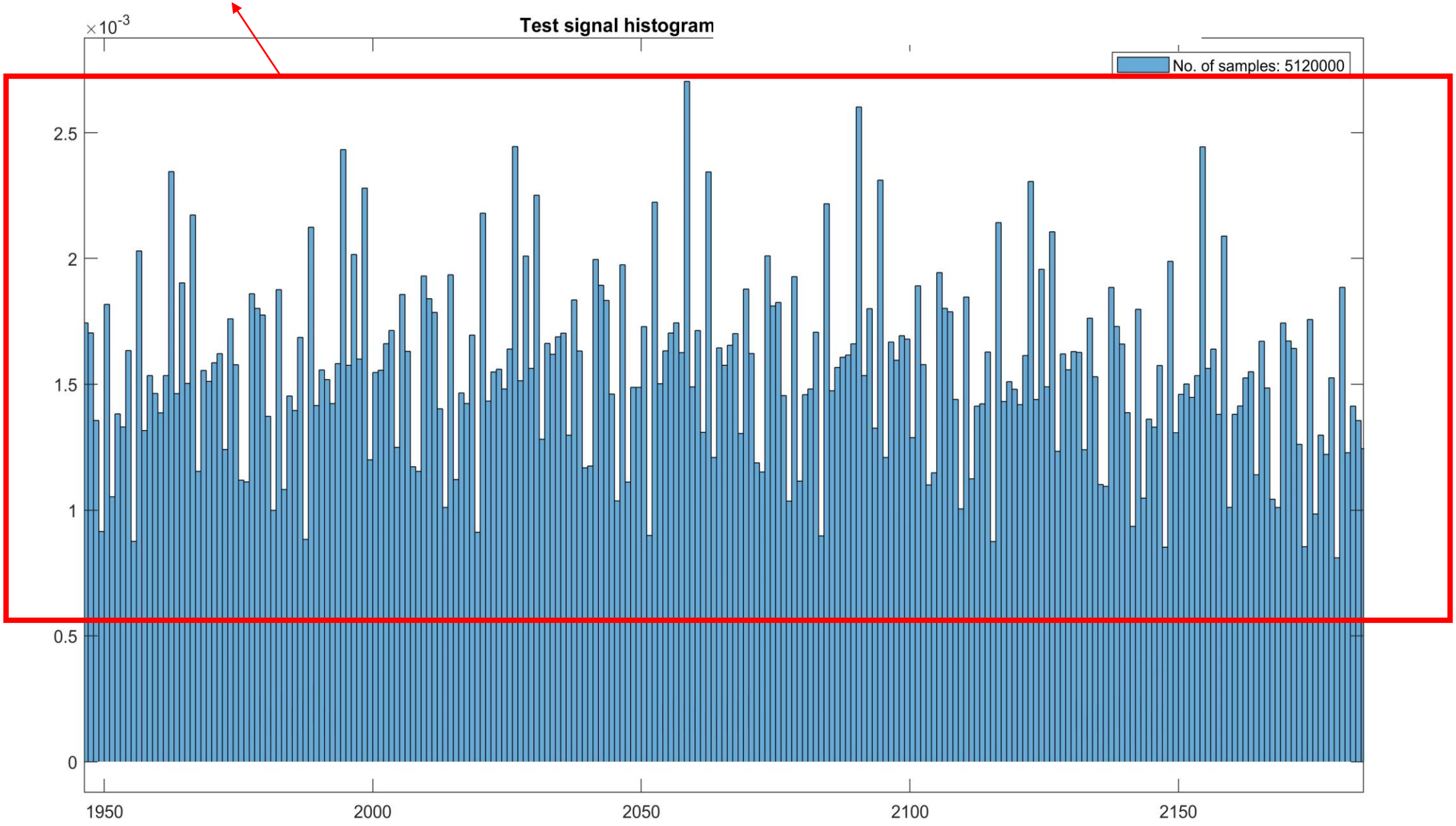
SECTION A: EXPERIMENTS DONE (3. WHITE NOISE SIGNAL AS INPUT)



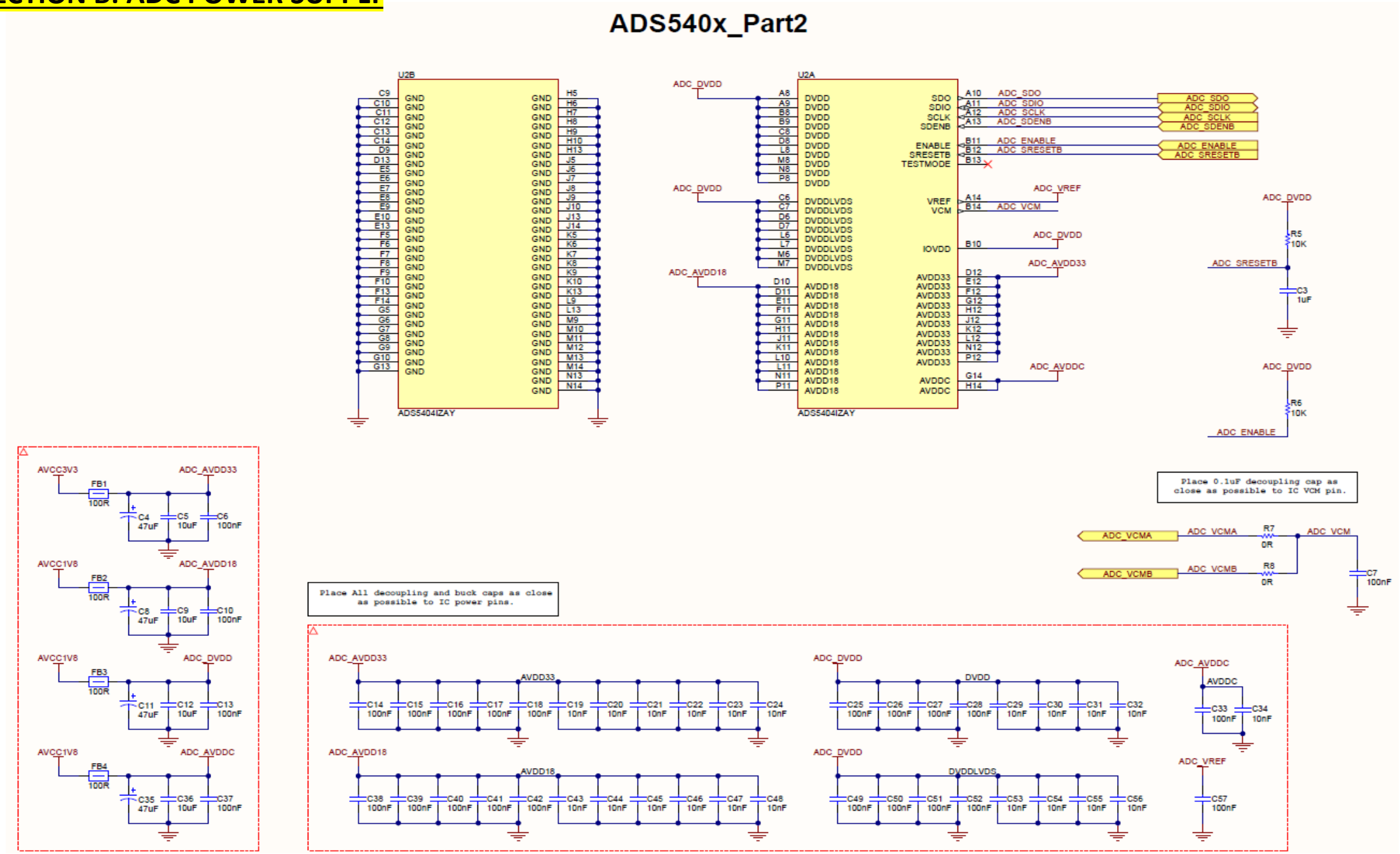
SIGNAL DISTORTION IN HISTOGRAM FOR THE ADC VOLTAGE RANGE



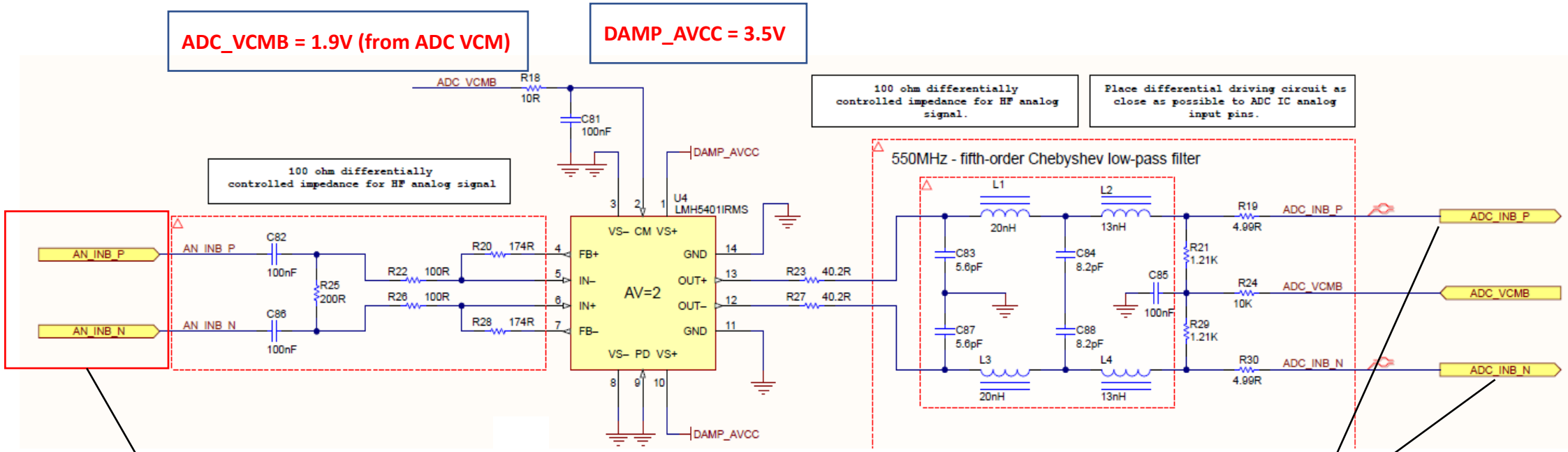
Zoomed-in picture of the distortion observed



SECTION B: ADC POWER SUPPLY



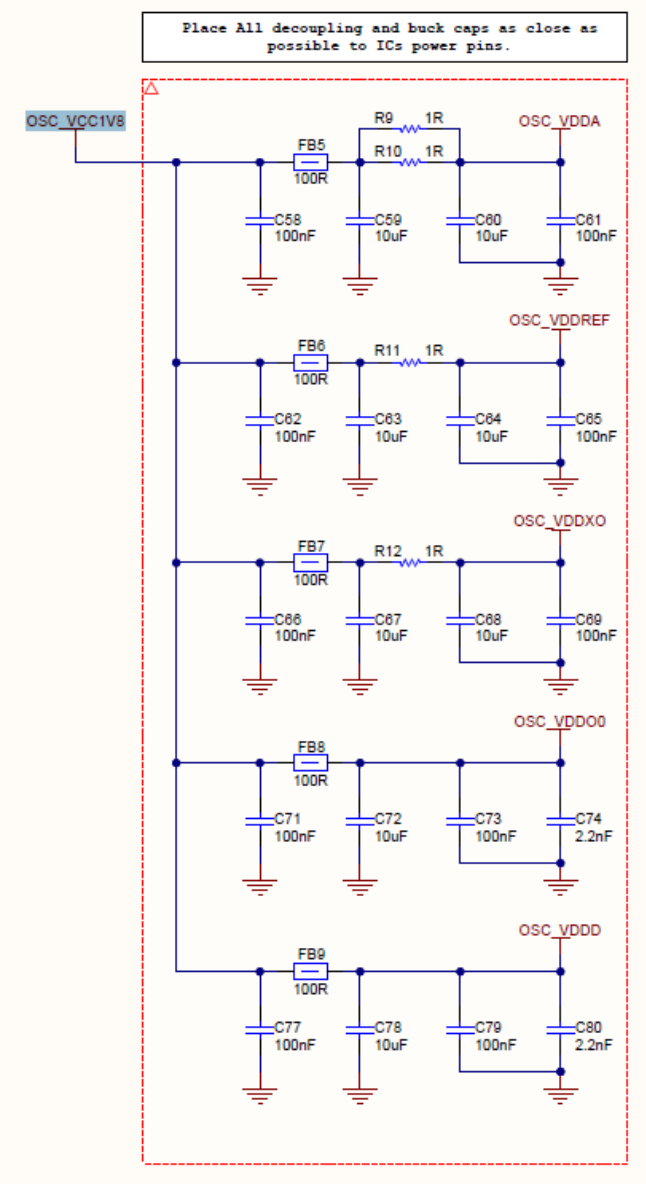
SECTION C: ADC INPUT DIFFERENTIAL DRIVER CIRCUIT



Differential Input from external system

Differential Input into ADC Channel B

SECTION D: ADC CLOCK GENERATOR CIRCUIT



OSC_VCC1V8 is generated from a separate high PSRR LDO and not shared with ADC. However, shares a common ground with the ADC.