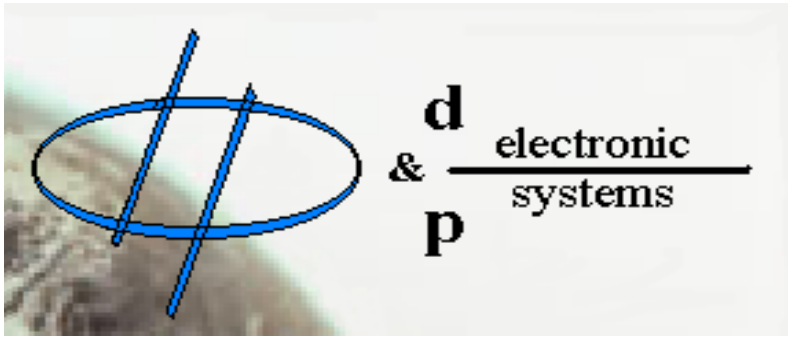


ADC 3U VPX board:
ADC Synchronization

Written by: *D. Sassaroli*

Doc.: *ADC_CONF_V10.pdf*

Data: *22/03/2019*

Index

In the next slides, there are:

- Front end block diagram of the board with internal and external clock network;
- Sys_ref buffer section of the Electrical Drawing;
- ADC Clock buffer section of the Electrical Drawing;
- Syncronization Test Set up with internal clock generation.

Synchronization activity

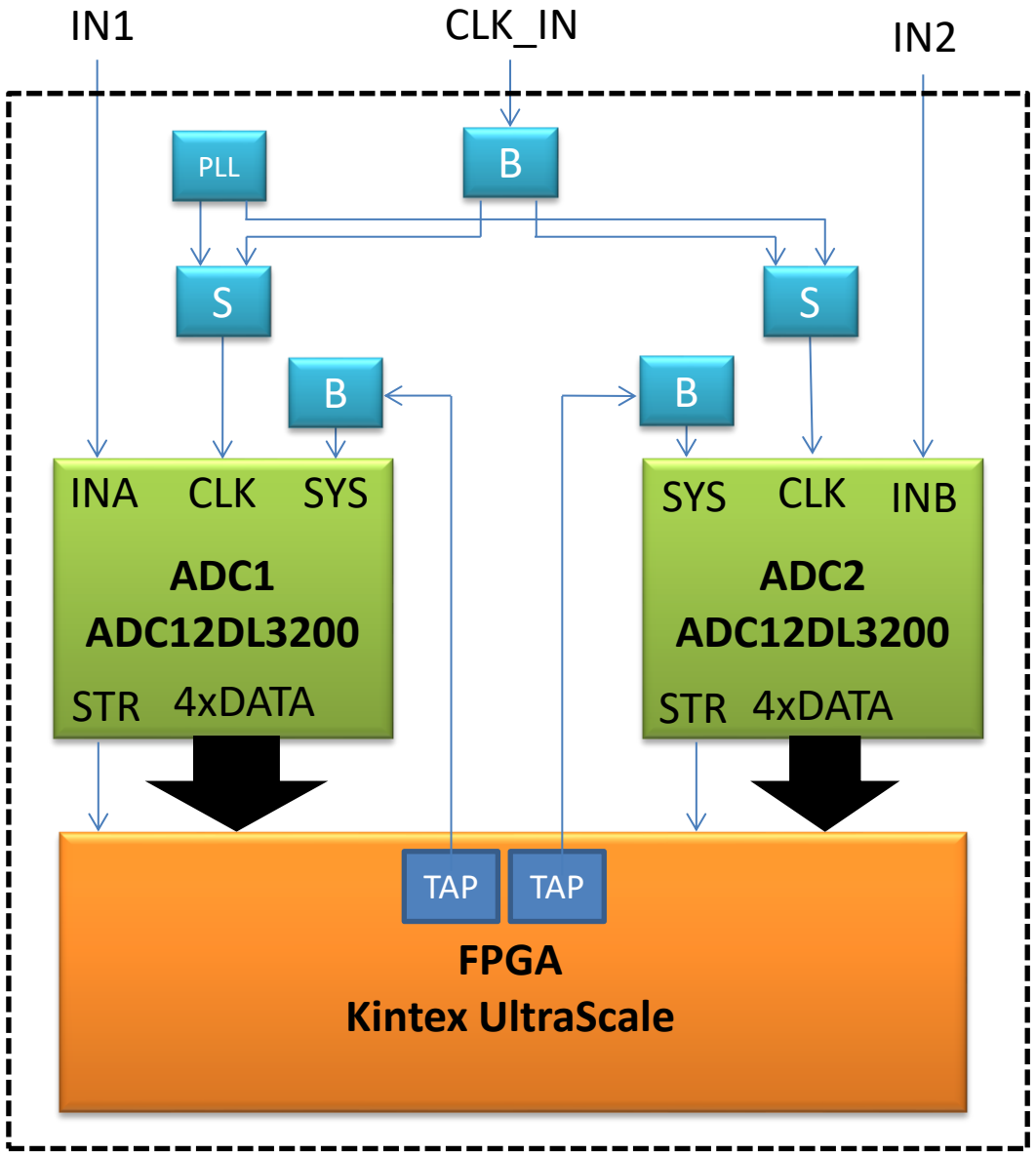
When I power on the board, I exectute these following operations:

- Power on the ADC1 and ADC 2;
- Configure the PLL at 2GHz and drive the input clock of the ADCs;
- Run the comands in the **CONF_SINGLE_ADC.txt** file (see the attached file);
- Send a SYS_REF signal and Verify the SYS_REF eye in the ADC registers;
- Set the SYS_REF position;
- Acquire the data from the two ADC using the STROBE signals such as trigger, in the FPGA;
- Measure the delta phase between the two ADCs (processing the sample downloaded);
- If the delta phase = <0>, stop.
  If the delta phase is not ok:
  1. Increment or decrement the SYS_REF delay of one ADC (inc/dec the TAP in the FPGA);
  2. Send a SYS_REF signal and Verify the SYS_REF eye;
  3. Set the SYS_REF position;
  4. Acquire the data from the ADCs, using the STROBE signal;
  5. Measure the delta phase between the two ADCs;
  6. If not ok repeat the steps from 1. Otherwise stop.

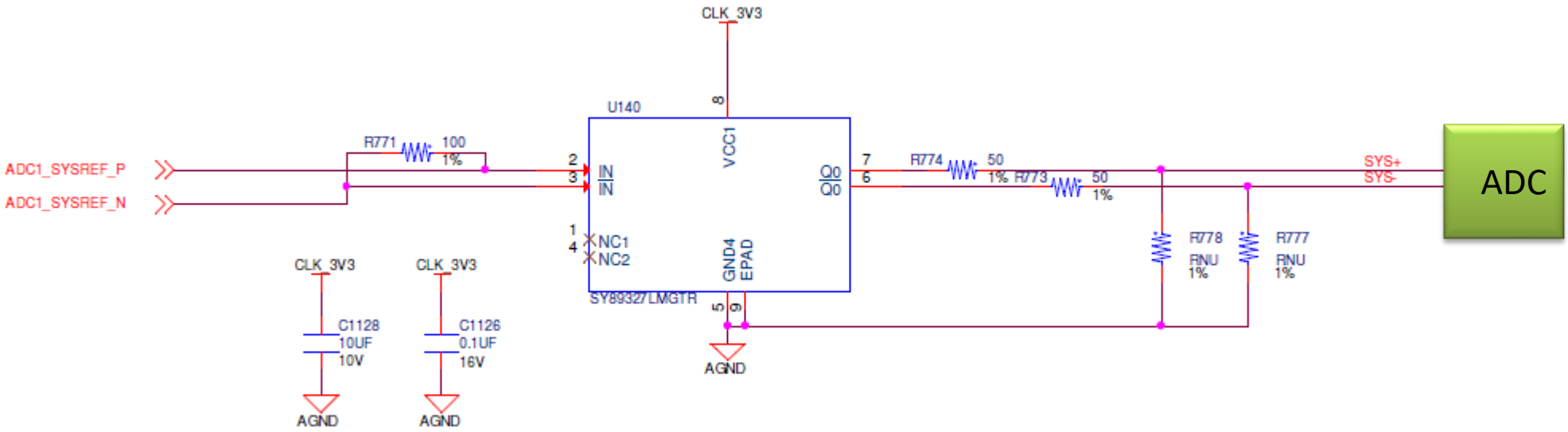
I've expected that if I move the SYS_REFs between them, I could alligned the STROBE signals of the two ADCs: the FPGA uses STROBE signals to trigger the data sample acquisition. Measuring the delta phase of the data acquired I can measure the effective allignmentAutomatic SYSREF Timing Calibration .

In this procedure I don't use the <Automatic SYSREF Timing Calibration> because this operation could move the ADC Clock phase.

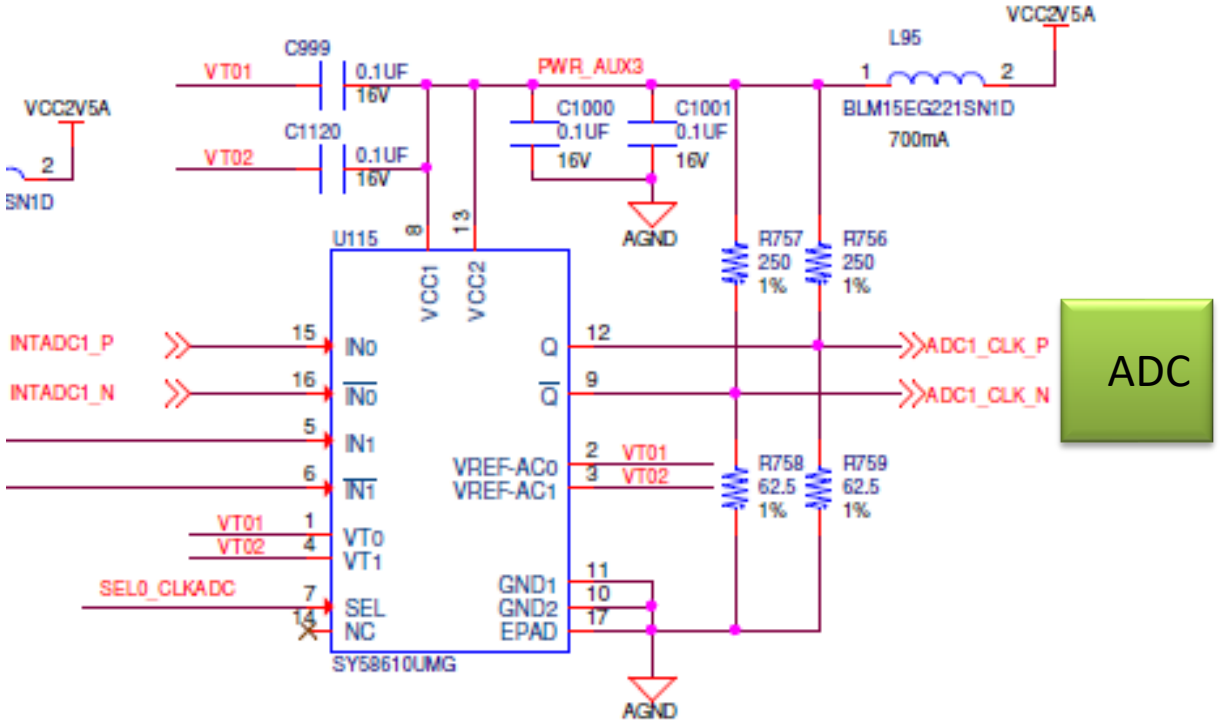
ADCs block diagram



SYSREF Buffer

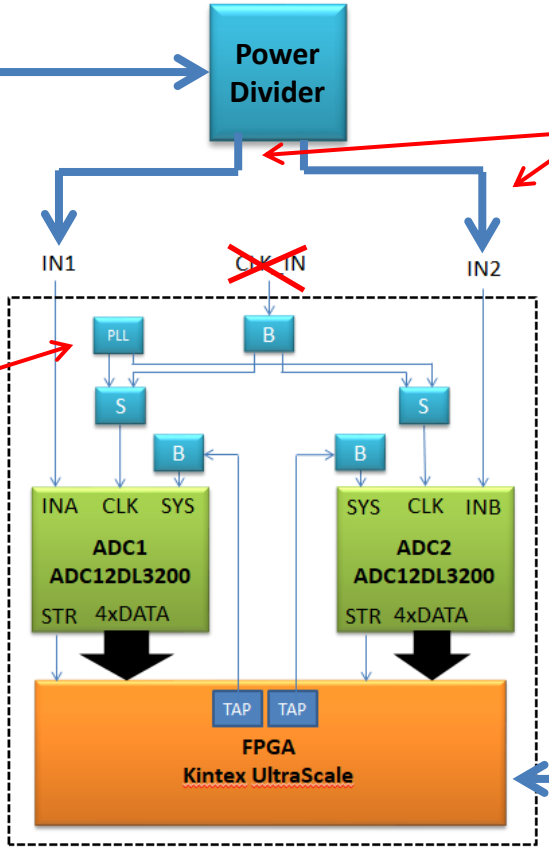


Clock Buffer



Phase data Test Set up

RF Generator



Matched RF cables

The ADC clock is generated internaly throught the PLL and it has 2 GHz frequency.

Notebook