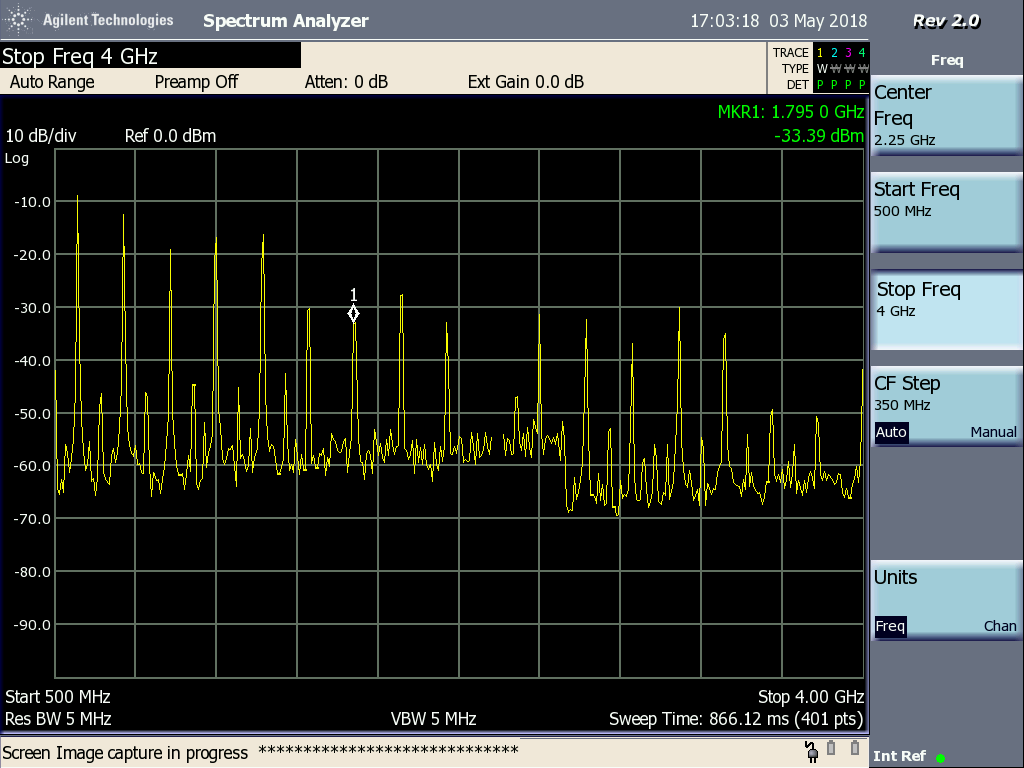
**ADC, JESD-data spectral measurement:**

Measured at JESD-Data-Lane (single-ended).

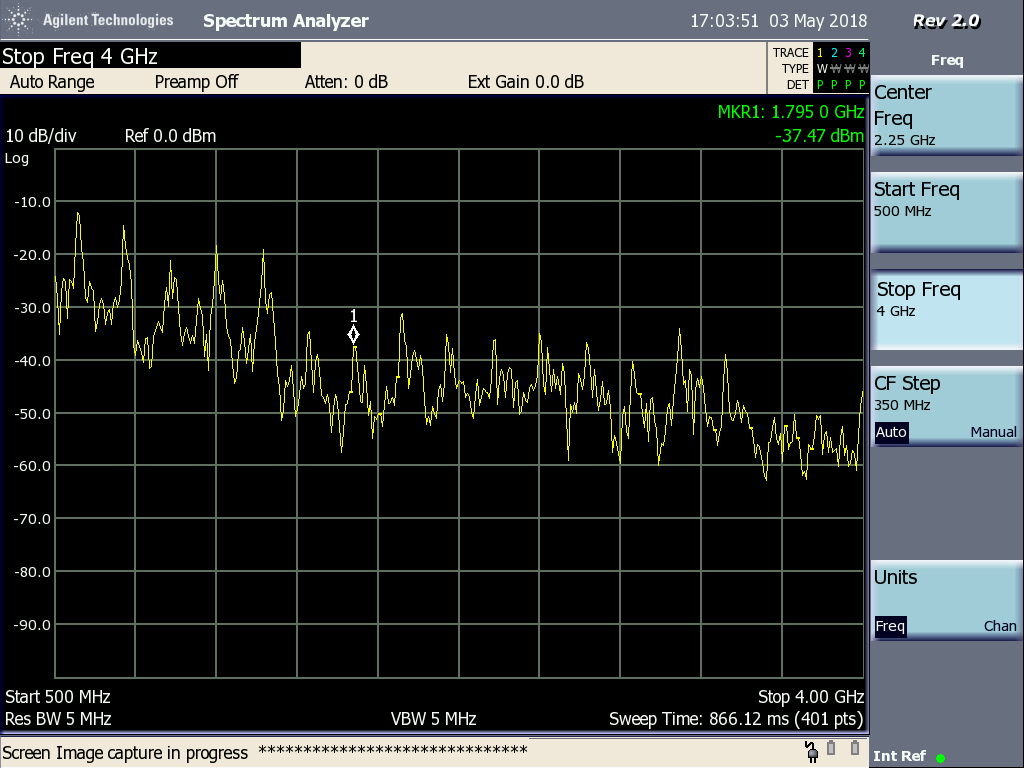
ADC operates in test-mode with the test pattern “all 0” because the JESD-Data spectrum has sharp peaks at dedicated frequencies and different sample rates can be easily compared.

The followed pictures are showing the spectrum of the JESD data lane at different ADC-sample rates and different clock divider settings: d32r

**ADC input clk: 100 MHz, div =1 🡪100 MSps**



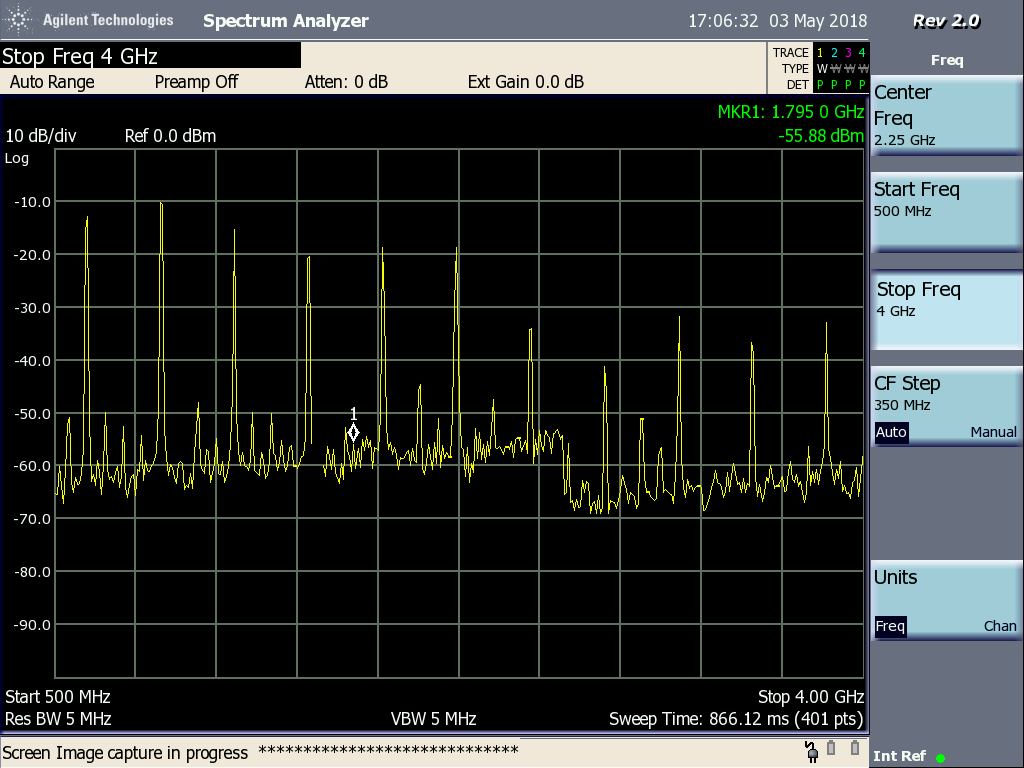
**ADC input clk: 200 MHz , div =2 🡪100 MSps**



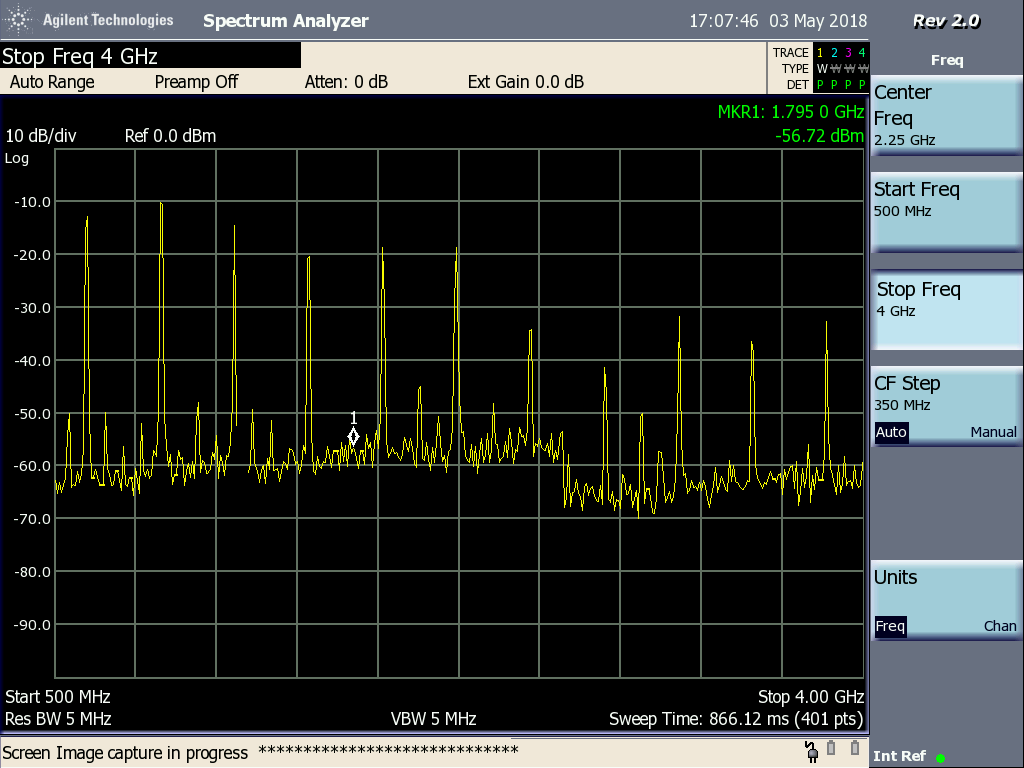
The same spectrum as above was expected but there seems to be a lot of noise in the signal.

Same measurement with 160 MSps

**ADC input clk: 160 MHz , div =1 🡪 160 MSps**



**ADCinput clk: 320 MHz , div =2 🡪 160 MSps**



Spectrum looks exactly the same, as it is expected.

Just one measurement with 160 MHz input clock and clock divider = 2 🡪 80 MSps

