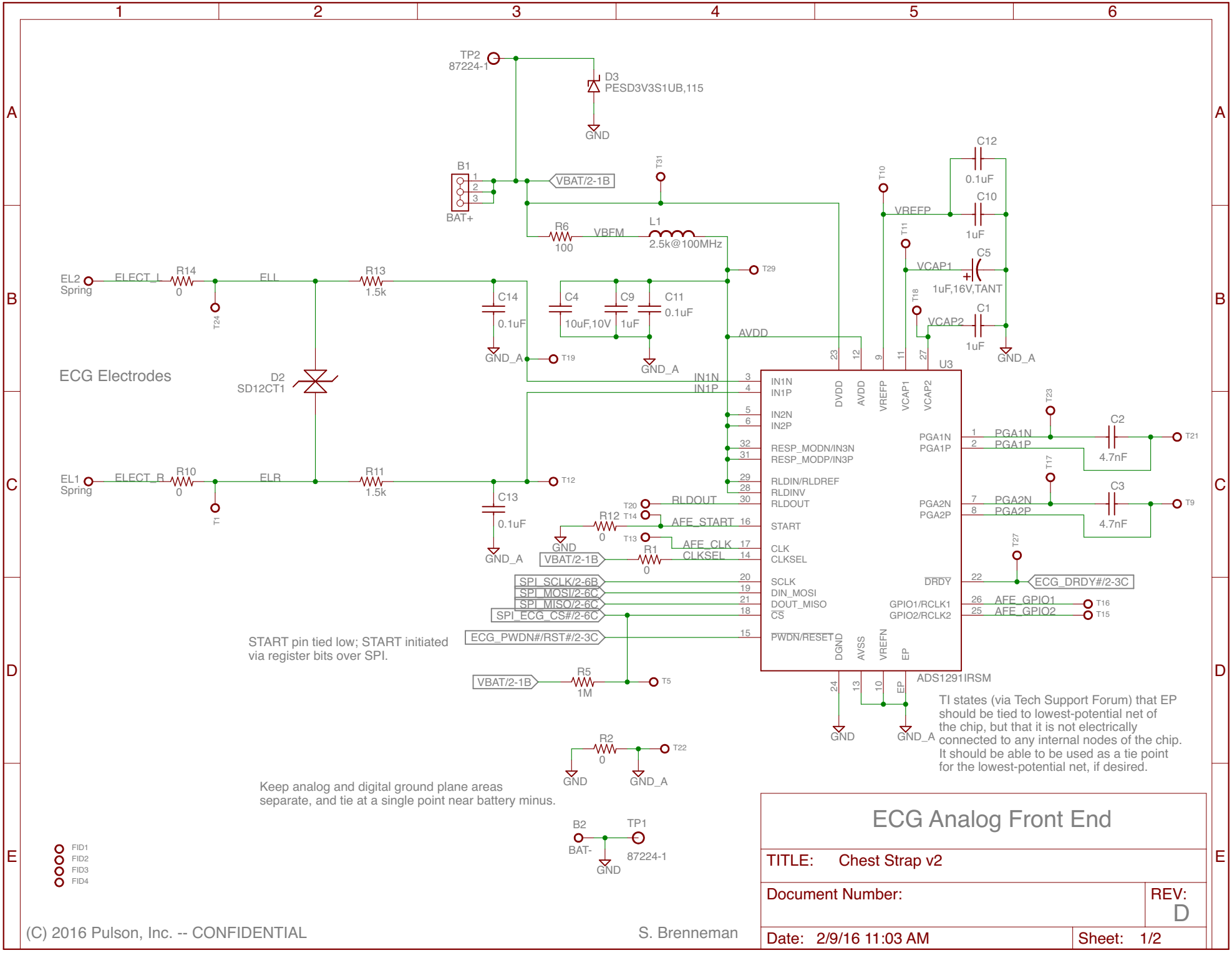
TP2
87224-1
D3
PESD3V3S1UB,115
GND
B1
BAT+
VBAT/2-1B
T31
R6
100
VBFM
L1
2.5k@100MHz
T29
EL2
Spring
ELECT_L
R14
0
T24
ELL
R13
1.5k
C14
0.1uF
GND_A
T19
C4
10uF,10V
C9
1uF
C11
0.1uF
GND_A
AVDD
ECG Electrodes
D2
SD12CT1
EL1
Spring
ELECT_R
R10
0
T1
ELR
R11
1.5k
T12
C13
0.1uF
GND_A
IN1N
IN1P
IN2N
IN2P
RESP_MODN/IN3N
RESP_MODP/IN3P
RLDIN/RLDREF
RLDINV
RLDOUT
START
CLK
CLKSEL
SCLK
DIN_MOSI
DOUT_MISO
CS
PWDN/RESET
DVDD
AVDD
VREFP
VCAP1
VCAP2
PGA1N
PGA1P
PGA2N
PGA2P
DRDY
GPIO1/RCLK1
GPIO2/RCLK2
DGND
AVSS
VREFN
EP
U3
ADS1291IRSM
T20
RLDOUT
T14
R12
0
AFE_START
T13
AFE_CLK
R1
0
CLKSEL
GND
VBAT/2-1B
SPI_SCLK/2-6B
SPI_MOSI/2-6C
SPI_MISO/2-6C
SPI_ECG_CS#/2-6C
ECG_PWDN#/RST#/2-3C
START pin tied low; START initiated via register bits over SPI.
VBAT/2-1B
R5
1M
T5
T10
VREFP
C12
0.1uF
C10
1uF
T11
VCAP1
C5
1uF,16V,TANT
T18
VCAP2
C1
1uF
GND_A
T23
PGA1N
PGA1P
C2
4.7nF
T21
T17
PGA2N
PGA2P
C3
4.7nF
T9
T27
ECG_DRDY#/2-3C
AFE_GPIO1
AFE_GPIO2
T16
T15
GND
GND_A
TI states (via Tech Support Forum) that EP should be tied to lowest-potential net of the chip, but that it is not electrically connected to any internal nodes of the chip. It should be able to be used as a tie point for the lowest-potential net, if desired.
R2
0
T22
GND
GND_A
Keep analog and digital ground plane areas separate, and tie at a single point near battery minus.
B2
BAT-
TP1
87224-1
GND
FID1
FID2
FID3
FID4
ECG Analog Front End
TITLE: Chest Strap v2
Document Number:
REV: D
Date: 2/9/16 11:03 AM
Sheet: 1/2
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S. Brenneman