ADS131B2x-Q1

Conversion Synchronization

Conversion control

- Conversions of the current measurement ADCs (ADC1A, ADC1B) are started using the STARTA and STARTB bits.
- The STARTy bits are written through SPI using the WREG command.
- Below diagram shows the WREG command structure.

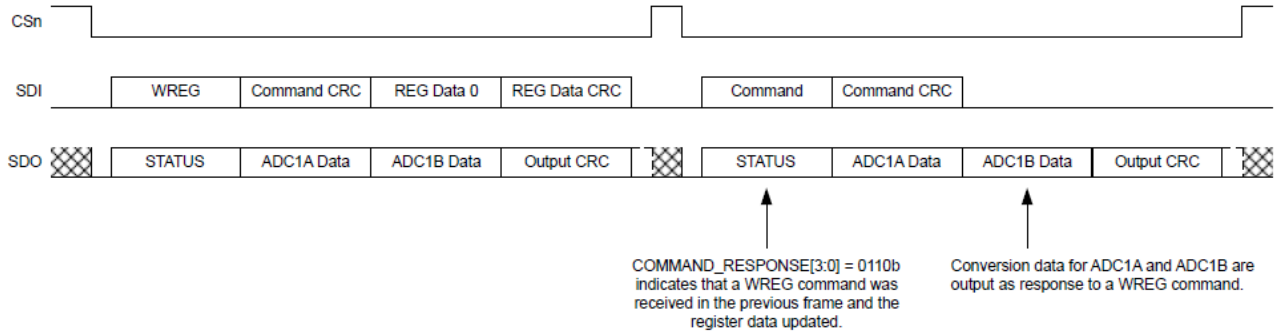

Figure 7-35. WREG Command Frame (Single Register)

- Each “box” in the diagram represents a 24-bit word
  (assuming the 24-bit word size is selected, which is the default setting)
- The STARTy bit is latched by the SPI at the 24th SCLK falling edge of the “REG Data CRC” word.

Timing considerations

- The internal digital logic latches the data at the next modulator clock rising edge.
  - The external clock is internally divided by 2x to generate the modulator clock ($f_{MOD} = f_{CLK}/2$).
  - f_{MOD} is toggling at the f_{CLK} rising edges.
  - The SCLK falling edges should stay away from the modulator clock rising edges to avoid any uncertainty in when the information is latched in the digital logic.
  - In case the same clock is used for SCLK and the external clock, then there is no issue.

Conversion latency after start of conversion

- The first conversion after setting the STARTy bit is available after t_{SETTLE} as described below.

ADC1y and ADC3y use a sinc3 digital filter that requires three conversion periods to settle. When conversions are started or restarted using the STARTy bits, the device hides the first two unsettled conversions and only provides a settled conversion result after the third conversion period. Use Equation 19 to calculate the time until the first conversion after a conversion start is available. All subsequent conversions have a conversion period, as shown in Figure 7-17, of $t_{DATA} = 1 / f_{DATA} = OSR / f_{MOD}$.

$$t_{SETTLE} = (3 \times OSR + 44) \times t_{MOD} \quad (19)$$

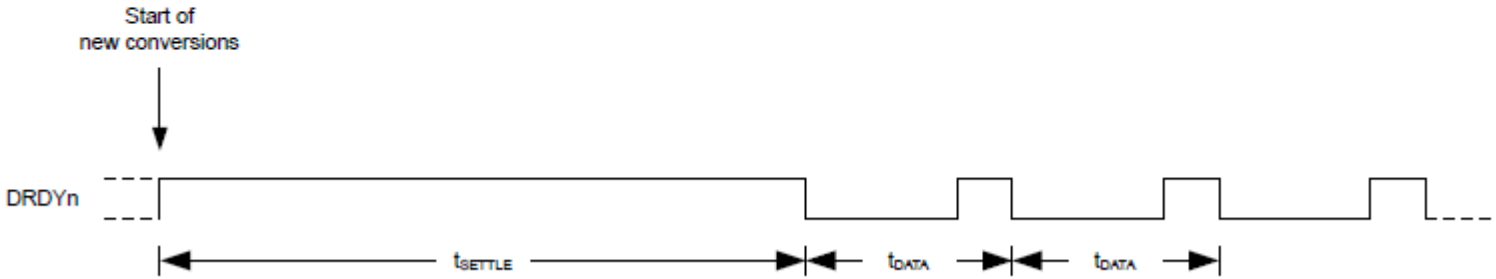

Figure 7-17. Sinc3 Filter Settling Time and Conversion Period