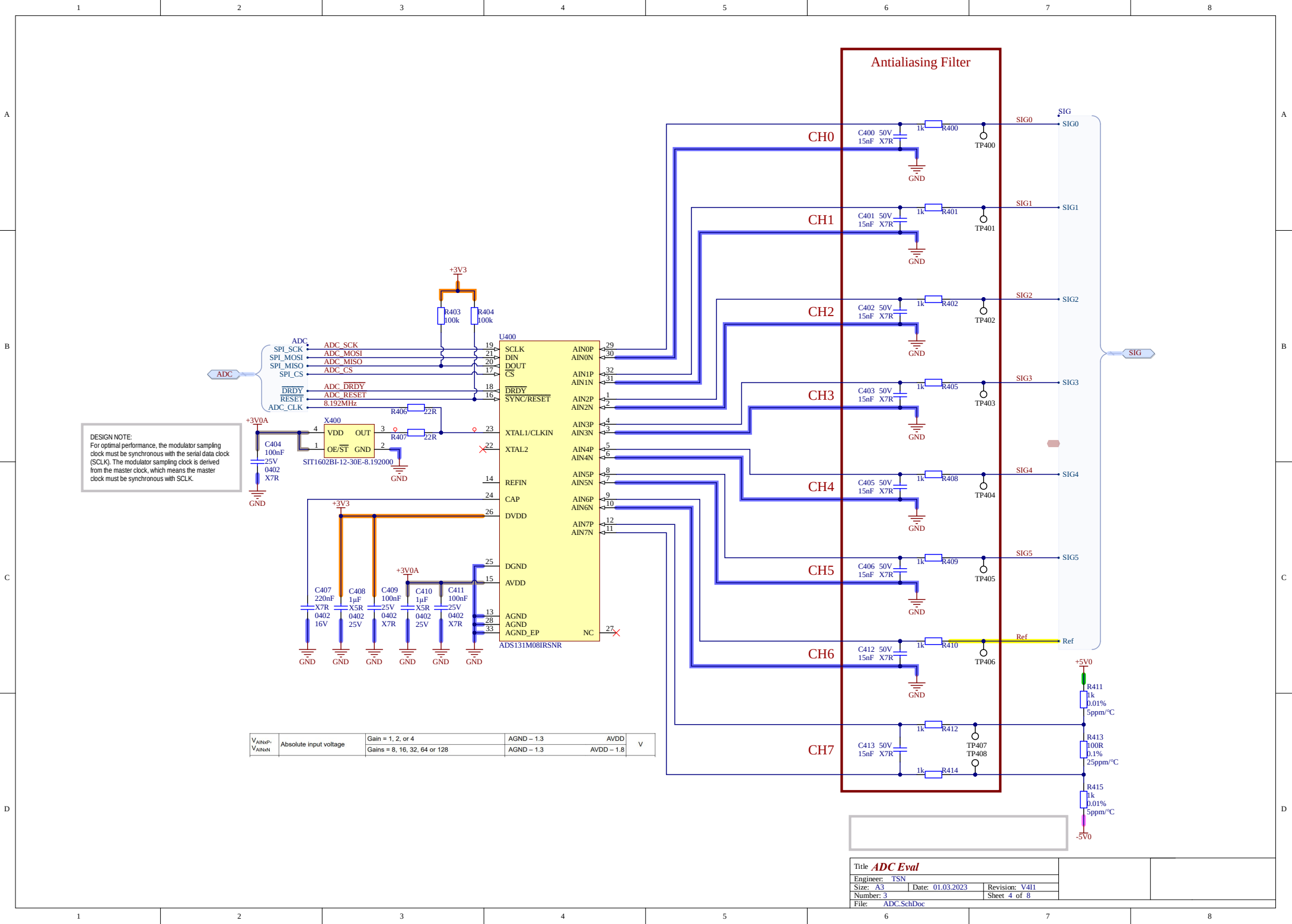




DESIGN NOTE:
For optimal performance, the modulator sampling clock must be synchronous with the serial data clock (SCLK). The modulator sampling clock is derived from the master clock, which means the master clock must be synchronous with SCLK.

VAINP+ VAINN	Absolute input voltage	Gain = 1, 2, or 4 Gains = 8, 16, 32, 64 or 128	AGND - 1.3 AGND - 1.3	AVDD AVDD - 1.8	V
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Title ADC Eval	
Engineer: TSN	
Size: A3	Date: 01.03.2023
Number: 3	Revision: V411
File: ADC.SchDoc	
Sheet 4 of 8	