what is the maximum delay between the CLKOUTABM/P and CLKOUTCDM/P?  
i thought it was 300ps but i can find out the information. See below

Skew, from CD clock rise to AB clock rise (ns), measured at 250MSPS, is shown in table below.

|  |  |  |  |
| --- | --- | --- | --- |
|  | Temp, C | | |
| Dvdd,V | -40 | 25 | 85 |
| 1.816 | 0.25 | 0.213 | 0.077056 |
| 1.916 | 0.239 | 0.202 | 0.065736 |
| 2.016 | 0.2996 | 0.203 | 0.045172 |

Other supplies (AVDD3V and AVDD) were kept at 3.3V and 1.9V respectively.

if i want to use ads4449 pattern generator (especially ramp generator) for all channels, is there a way to guarantee that all ramp patterns will start at the same time? My concern is synchronize AB and CD flows inside a fpga. No. The outputs are not synchronized between channels.

I have already asked an equivalent question but it seems the answer was only about custom pattern  
  
More generally, is there a way to have a same pattern (with different words) emitted synchronously on all channels with a delay between AB and CD channels which is the same as delay in normal operation? No.