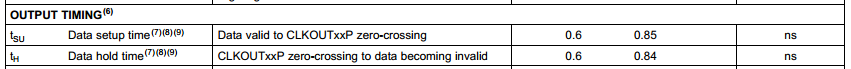
Data valid window doesn’t change when programmable output clock delay is applied. These SPI register bits simply move the output clock edge w.r.t output data so that the available setup or hold time can be changed as per FPGA’s requirements (data valid window is sum of setup and hold time, remains unchanged).

Mean value of data valid window remains similar for both channels. However, what is important for the latching (Rx) device is ‘from the active edge of the output clock of ADC, how much setup and hold time is available to latch ADC’s output data’. Datasheet gives this information in time characteristics table (for 250MSPS output clock).



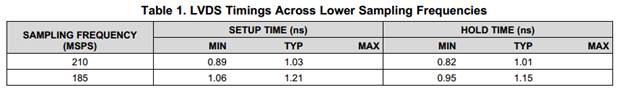
cid:image004.png@01D3DC9C.DD755720

Dedicated output clocks are available for a pair of channel (channel AB, and Channel CD). These clocks must be used to capture corresponding channel’s data in FPGA.

The setup and hold time values specified in datasheet are applicable to all four channels with respect to their corresponding output clock.

Customer should use min values of setup and hold time while making timing budget in FPGA.

For output timing at 192MSPS, refer to table 1 of datasheet (applies same register settings to delay the output clock for table above).



Using this information, the approximate values of setup and hold time (min and typ) are given below:

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  |  | setup,ns | | hold,ns | |
| fs,MSPS | ts, ns | min\_su | typ\_su | min\_su | typ\_ho |
| 250 | 4 | 0.6 | 0.85 | 0.6 | 0.84 |
| 210 | 4.761904762 | 0.89 | 1.03 | 0.82 | 1.01 |
| **192** | **5.208333333** | **1** | **1.15** | **0.91** | **1.1** |
| 185 | 5.405405405 | 1.06 | 1.21 | 0.95 | 1.15 |