**TEXAS INSTRUMENTS**

*User's Guide*
SLAU632−June 2015

# ADS52J90 8/16/32-Channel, Analog-to-Digital Converter Evaluation Module

This user's guide gives an overview of the evaluation module (EVM) and provides a general description of the features and functions to be considered while using this module. This manual is applicable to the ADS52J90 analog-to-digital converters (ADC). The ADS52J90 EVM provides a platform for evaluating the ADC under various signal, clock, reference, and ADC output formats. In addition, the EVM supports the testing of both an LVDS interface as well as a JESD204B interface.

> **NOTE:** A different capture card EVM is required for each.

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The ADS52J90 EVM can be tested using an LVDS data interface or a JESD204B data interface.

## 1.1    *LVDS Interface (ADS52J90 EVM + TSW1400)*

As shown in Figure 1, mating the ADS52J90 EVM with a TSW1400 EVM allows testing using an LVDS data interface.



**Figure 1. LVDS Evaluation Setup**

**FPGA EVM:** The TSW1400 high-speed LVDS de-serializer EVM is required for capturing data from the ADS52J90EVM. Analysis of the captured data is possible using its graphical user interface (GUI) which is called High Speed Data Converter Pro.

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**NOTE:**   The same GUI is used to control the TSW14J56 capture card for supporting a JESD204B data interface.

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For more information pertaining to be TSW1400EVM, see: http://focus.ti.com/docs/toolsw/folders/print/tsw1400evm.html.

**Equipment:** Signal generators (with low-phase noise) must be used as source of input signal and clock in order to get the desired performance. Additionally, a band-pass filter (BPF) is required on the analog input signal to attenuate the harmonics and noise from the generators.

**Power Supply:** A single +5-V supply powers the ADS52J90EVM through connectors located at **J47** and **J48** or through an AC adaptor (not provided) at **J46**. The supply for the ADS52J90 device is derived from this +5-V supply. The power supply must be able to source up to 1.5 A. The TSW1400 EVM is powered through an AC adaptor provided with its EVM kit.

**USB Interface to PC:** The USB connections from the ADS52J90EVM and TSW1400EVM to the computer are used for communication from the GUIs to the boards. Section 2 explains the *High Speed Data Converter Pro* and ADS52J90 GUI installation procedures.

## 1.2 JESD204B Interface (ADS52J90 EVM + TSW14J56)

As shown in Figure 2, mating the ADS52J90 EVM with a TSW14J56 EVM allows testing using a JESD204B data interface.
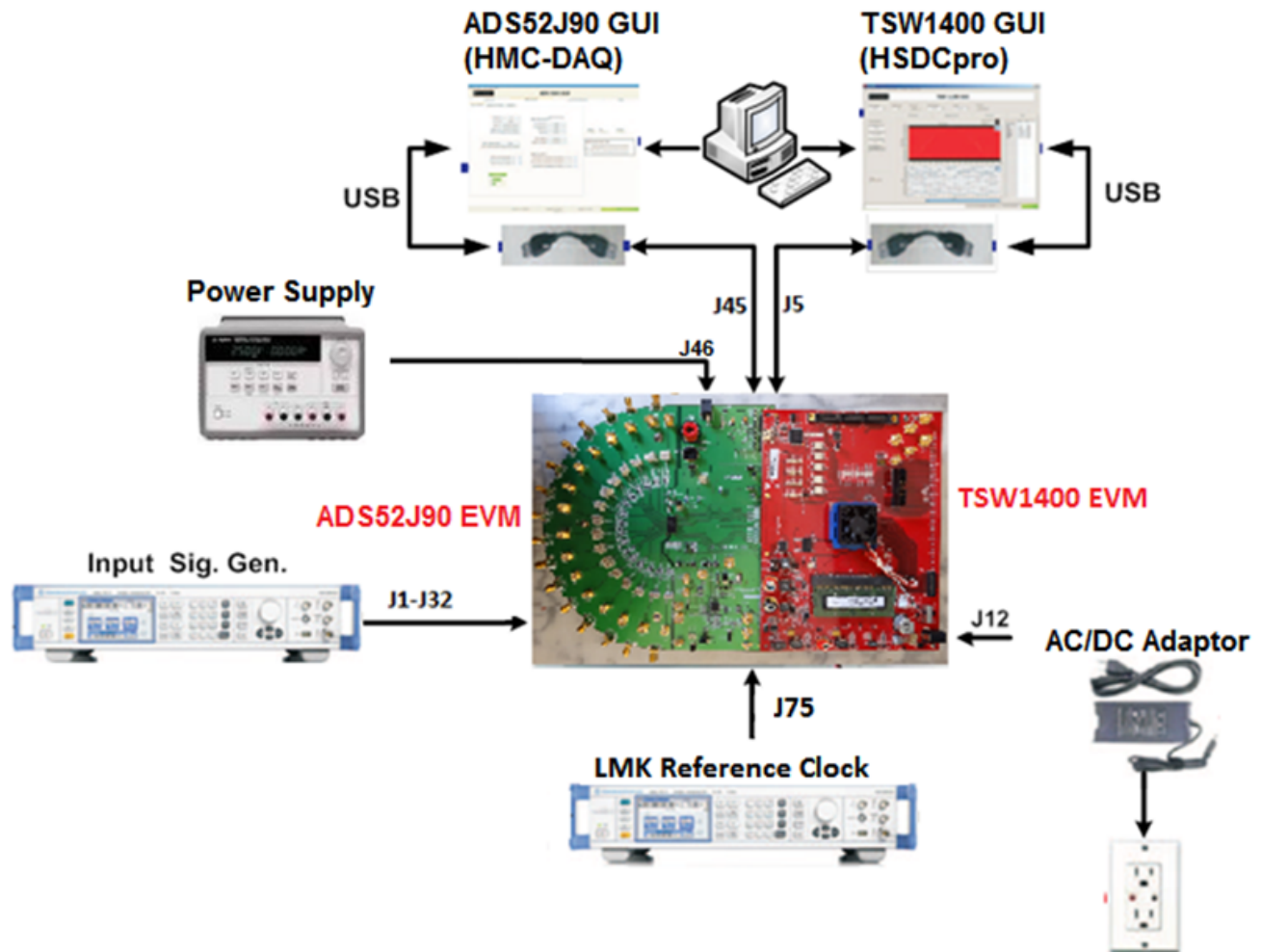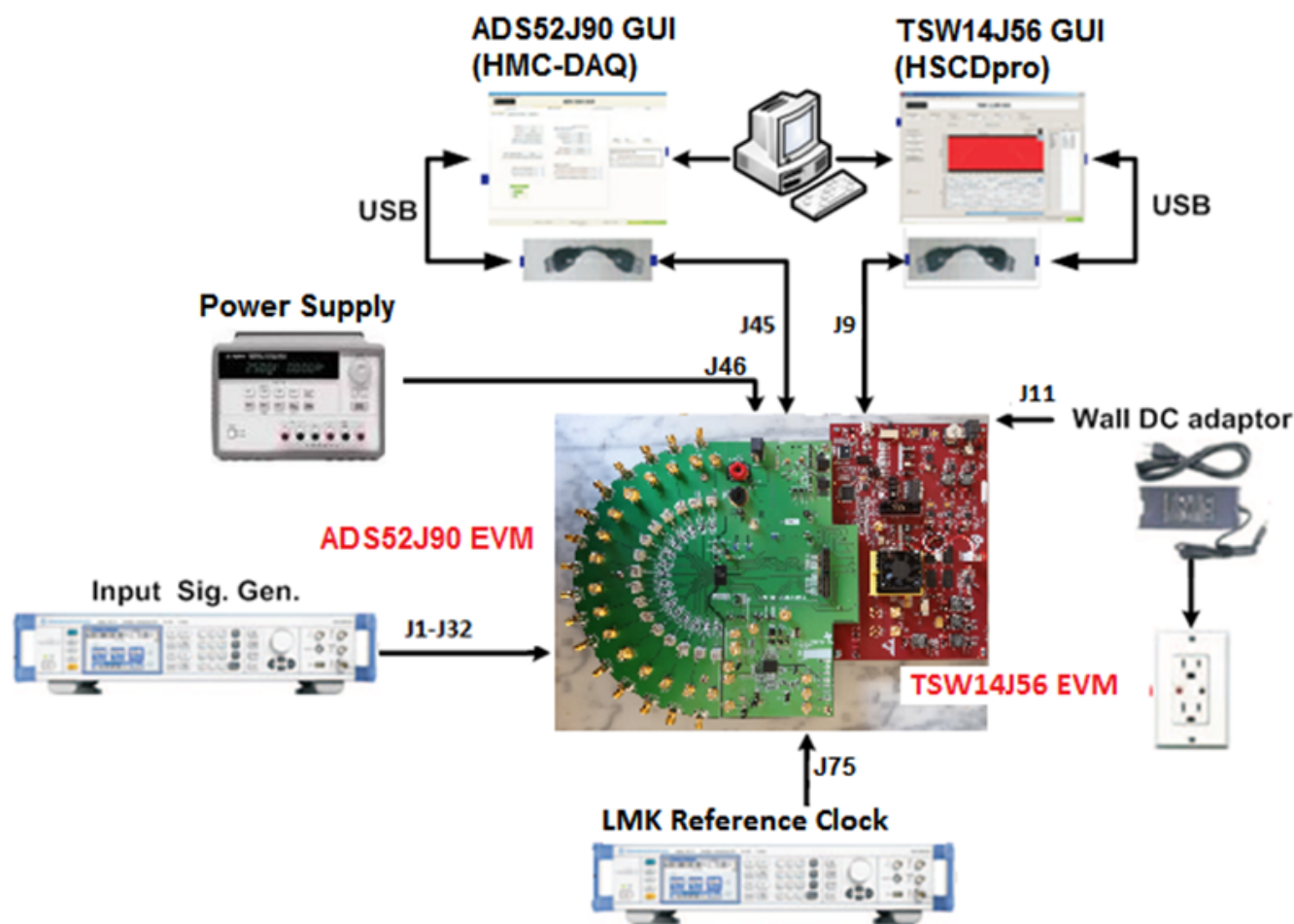


**Figure 2. JESD204B Evaluation Setup**

**FPGA EVM:** The TSW14J56 high-speed JESD204B de-serializer board is required for capturing data from the ADS52J90EVM. Analysis of the captured data is possible using its graphical user interface (GUI) which is called High Speed Data Converter Pro (*note: the same GUI is used to control the TSW1400 capture card for supporting an LVDS data interface*).

For more information pertaining to be TSW14J56EVM, see: http://www.ti.com/tool/tsw14j56evm

**Equipment:** Signal generators (with low-phase noise) must be used as source of input signal and clock in order to get the desired performance. Additionally, a band-pass filter (BPF) is required on the analog input signal to attenuate the harmonics and noise from the generator.

**Power Supply:** A single +5-V supply powers the ADS52J90EVM through connectors located at **J47** and **J48** or through an AC adaptor (not provided) at **J46**. The supply for the ADS52J90 device is derived from this +5-V supply. The power supply must be able to source up to 1.5 A. The TSW14J56 EVM is powered through an AC adaptor provided with its EVM kit.

**USB Interface to PC:** The USB connections from the ADS52J90EVM and TSW14J56EVM to the computer are used for communication from the GUIs to the boards. Section 2 explains the *High Speed Data Converter Pro* and ADS52J90 GUI installation procedures.

## 2    GUI Software Installation

The ADS52J90 EVM and the de-serializing capture card EVM both require software installations. The following two sections explain where to find and how to install the software properly. Ensure that no USB connections are made to the EVMs until after the installations are complete.

### 2.1    High Speed Data Converter Pro (HSDCpro) GUI Installation

Download the High Speed Data Converter Pro GUI Installer (SLWC107) from the Texas Instruments website (www.ti.com) and install per the instructions in its user's guide (SLWU087).

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NOTE:    Version 3.1 or higher of HSDC Pro is required to test the ADS52J0. If an earlier version of HSDC Pro is installed, please uninstall before installing the latest version.

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TI recommends installing HSDC Pro before installing the ADS52J90 GUI and installing it in the default location provided during installation.

### 2.2    ADS52J90 GUI Installation (HMC-DAQ)

The GUI used to control the ADS52J90 EVM is a suite that supports a family of devices. The GUI is called *Healthtech Multi-Channel Data Acquisition GUI*, or, *HMC-DAQ*. Download and save the file *HMC-DAQ_GUI_INSTALLER_SLOC326.zip* to a temporary location on the local PC hard drive. Once saved, unzip the file and run the executable as administrator by right clicking on the file. Follow the instructions provided during installation. TI recommends installing after HSDCpro has been installed and in the default location provided during installation.

## 3 ADS52J90 EVM Headers/Test Points and Clock Configuration

This section describes the functions of the headers on the EVM. It also provides a list of test points on the EVM that are useful for debug and general-use purposes. Finally, several options for providing clocks to the EVM are described.

### 3.1 ADS52J90 EVM Header Configuration

The ADS52J90 EVM is flexible in its configurability through the use of 2- and 3-pin headers. Table 1 describes the purpose of all headers on the EVM and the default positions. With this configuration, all required clocks for testing the LVDS or JESD204B interface are derived from a single reference clock provided to SMA J75 to the LMK04826 clocking device installed at designator **U2** on the EVM. The LMK04826 is configured for Clock Distribution Mode (CDM) with the provided scripts.

**Table 1. ADS52J90 Default Header Configuration**

| Jumper Description | Jumper# | Jumper Name | Default Config | Circuit | Description |
|---|---|---|---|---|---|
| Power Supply | JP9 | +3.3VCLK | Short pins 1-2 | Clocks | Power supply XTAL1, XTAL2, OSC1, LMK04826 |
| | JP10 | IOVDD_+3.3V | Short pins 1-2 | SPI BUFFERS | Power supply for SPI level shifters and isolators |
| | JP11 | DVDD_+1.2V | Short pins 1-2 | ADS52JD90 | +1.2-V digital power supply for ADS52JD90 |
| | JP12 | AVDD_+1.8V | Short pins 1-2 | ADS52JD90 | +1.8-V analog power supply for ADS52JD90 |
| | JP13 | LVDD_+1.8V | Short pins 1-2 | ADS52JD90 | +1.8-V digital power supply for ADS52JD90 |
| | JP15 | DISABLE | DNI | Regulator | Not used |
| | JP16 | 5VIN | DNI | Regulator | Not used |
| ADS52J90 SYNC Options | JP33 | n/a | Short pins 1-2 | ADS52JD90 SYNC pin | Selects SYNC signal source to ADS52JD90: (1) Auxiliary signal determined by JP28 or (3) GUI via FTDI device |
| | JP28 | n/a | Short pins 1-2 | ADS52JD90 SYNC pin | Selects auxiliary SYNC signal source to ADS52JD90: (1) SMA J50 or (3) FPGA via pin 105 of connector J44B |
| LMK04826 Options | JP2 | SYNC | Short pins 1-2 | LMK SYNC | Selects the source of SYNC signal into LMK042x clock device: (1) signal from SMA J39, LMK_SYNC or (3) signal from FPGA at pin K22 of connector J43C |
| | JP3 | LMK_RB | Short pins 2-3 | LMK Readback/Reset | Selects LMK RESET pin signal source: (1) LMK_DATA_OUT out to FDTI (3) LMK_RESET in from FTDI |
| ADC_CLKP/M SEL | JP39 | ADC_CLK_AUX | Short pins 1-2 | ADS52J90 CLKP/M & SYSREFP/M Source | Selects auxiliary CLKP/M signal source to ADS52JD90: (1) SMA J55, ADC_CLK or (3) one of two on-board XTAL oscillators determined by JP8 |
| | JP40 | ADC_CLK | Short pins 2-3 | | Selects signal source to CLKP/M of ADS52J90: (1) Auxiliary source from JP39 or (3) LMK04826 output |
| | JP41 | ADC_SYSREF | Short pins 1-2 | | Selects signal source to CLKP/M of ADS52J90: (1) Auxiliary source from JP39 or (3) LMK04826 output |
| XTAL Power Supply Options | JP4 | OSC1_VDD | Open | XTAL/OSC Power | Powers 100-MHz OSC1 |
| | JP5 | XTAL1_VDD | Open | | Powers 10-MHz XTAL1 |
| | JP6 | XTAL2_VDD | Open | | Powers 40-MHz XTAL2 |
| XTAL SEL | JP7 | LMK_CLKIN1 | Short pins 1-2 | LMK CLKIN1 | Selects signal source to CLKIN1 of LMK04826: (1) SMA J75, LMK_CLKIN1 or (3) XTAL determined by JP8 |
| | JP8 | XTAL_SEL | Open | XTAL Oscillators | Selects XTAL source to JP7 and JP39: (1) 10MHz XTAL1 or (3) 40MHz XTAL2 |
| Analog Inputs 8ch mode | JP700_7 | n/a | Short pins 2-3 | Analog Inputs 8ch mode | Selects between (1) 5-V power supply and (2) and GND for amplifier on channels 7,8 for 8ch mode |
| | JP800_8 | n/a | Short pins 2-3 | | |

Jumpers **JP11, JP12, JP13** can be removed and individual power supplies given to these headers in order to monitor the DC current consumed by the ADS52J90.

## 3.2 ADS52J90 EVM Test points

Table 2 lists all test points on the ADS52J90 EVM and their purposes.

**Table 2. ADS52J90 EVM Test Points**

| Test Point | Silkscreen | Circuit | Description |
|---|---|---|---|
| TP13 | +5.0V_IN | Power supply | Main +5-V power supply to EVM |
| TP15 | GND | Power supply | Ground reference for EVM |
| TP14 | IOVDD3.3V | Power supply | Power supply for VCM generation |
| TP12 | +3.3VCLK | Power supply | Power supply for LMK0482x and oscillators |
| TP16 | 4V | Power supply | Input supply to regulator at designator U11 |
| TP17 | AVDD_+1.8V | Power supply | Power supply to ADS52J90 |
| TP18 | LVDD_+1.8V | Power supply | Power supply to ADS52J90 |
| TP19 | FORCE_VCM | Analog inputs | Can provide external VCM to analog inputs by installing R108 and uninstalling R110 |
| TP20 | FORCE_VREF | Analog inputs | Can provide external VREF to ADS52J90 by installing R109 |
| TP1 | VCM | Analog inputs | ADS52J90 output providing VCM to analog inputs |
| TP4 | GTX_CLKP | LMK0428x output | GTX clock to FPGA on capture card |
| TP5 | GTX_CLKM | LMK0428x output | GTX clock to FPGA on capture card |
| TP21 | CLK_LAO_0P | LMK0428x output | Global clock to FPGA on capture card (typ. equals Fs) |
| TP22 | CLK_LAO_0M | LMK0428x output | Global clock to FPGA on capture card (typ. equals Fs) |
| TP6 | SYSREF_P | LMK0428x output | SYSREF clock to FPGA on capture card |
| TP7 | SYSREF_M | LMK0428x output | SYSREF clock to FPGA on capture card |
| TP8 | CLKP | LMK0428x output | Device clock (Fs) to DUT from LMK0482x |
| TP10 | CLKM | LMK0428x output | Device clock (Fs) to DUT from LMK0482x |
| TP9 | SYSREFP | LMK0428x output | SYSREF clock to DUT from LMK0482x |
| TP11 | SYSREFM | LMK0428x output | SYSREF clock to DUT from LMK0482x |
| TP37 | CLK_P | DET LAT EVM | Device clock (Fs) to DUT when Deterministic Latency EVM is used |
| TP38 | CLK_M | DET LAT EVM | Device clock (Fs) to DUT when Deterministic Latency EVM is used |
| TP35 | SYSREF_P | DET LAT EVM | SYSREF clock to DUT when Deterministic Latency EVM is used |
| TP36 | SYSREF_M | DET LAT EVM | SYSREF clock to DUT when Deterministic Latency EVM is used |
| TP23 | GND | GND | Ground reference for EVM |
| TP2 | SYNCP_SERDES | JESD SYNC | Input JESD SYNC~ to ADS52J90 from FPGA |
| TP3 | SYNCM_SERDES | JESD SYNC | Input JESD SYNC~ to ADS52J90 from FPGA |
| TPA0 | SCLK | ADS52J90 SPI PIN | SPI clock input to ADS52J90 |
| TPA1 | SDATA | ADS52J90 SPI PIN | SPI data input to ADS52J90 |
| TPA2 | SEN | ADS52J90 SPI PIN | SPI enable input to ADS52J90 |
| TPA3 | SDOUT | ADS52J90 SPI PIN | SPI read back output from ADS52J90 |
| TPA4 | RESET | ADS52J90 PIN | RESET pin to ADS52J90 |
| TPA5 | PDN_GBL | ADS52J90 PIN | PDN_GBL pin of ADS52J90 |
| TPA6 | PDN_FAST | ADS52J90 PIN | PDN_FAST pin of ADS52J90 |
| TPA7 | SYNC_LVDS_FTDI | ADS52J90 PIN | SYNC pin to ADS52J90 allowing for synchronized LVDS outputs |
| TPB0 | LMK_CLK | LMK SPI PIN | SPI clock input to LMK0482x |
| TPB1 | LMK_DATA_OUT | LMK SPI PIN | SPI read back output from LMK0482x |
| TPB2 | LMK_DATA | LMK SPI PIN | SPI data input to LMK0482x |
| TPB3 | LMK_SPI_EN | LMK SPI PIN | SPI enable input to LMK0482x |
| TPB4 | LMK_RESET | LMK PIN | RESET pin to LMK0482x |
| TPB5 | RSV_DIG | n/a | Reserved |
| TP24 | GND | GND | Ground Reference for EVM |

## 3.3 EVM Clock Configuration

The EVM should be shipped with jumpers setting the LMK04826 clocking device (U2) in clock distribution mode. In this configuration shown in Figure 3, the LMK04826 acts as a clock buffer/divider on the external input clock to SMA **J75**, **LMK_CLKIN1**. For LVDS mode, this input clock should be set to the desired system clock required by the ADS52J90. To support the JESD204B interface, this input clock should be set to 1/40 the SerDes line rate when the line rate is above 1Gbps and 1/10 the SerDes line rate when the line rate is below 1Gbps. Put another way, the SerDes lane rate will be 10x the reference clock when the calculated lane rate is below 1Gbps and will be 40x the reference clock when the calculated lane rate is above 1Gbps. The HSDCpro GUI will report both the calculated lane rate and the required reference clock each time the user changes the *Output Data Rate* value in the GUI. Figure 4 and Figure 5 show examples of the message when lane rate is 40x the reference clock and when the lane rate is 10x the reference clock, respectively. Configuration scripts for both 10x rate and 40x rate are provided in folders with the appropriate suffix appended to the folder names.
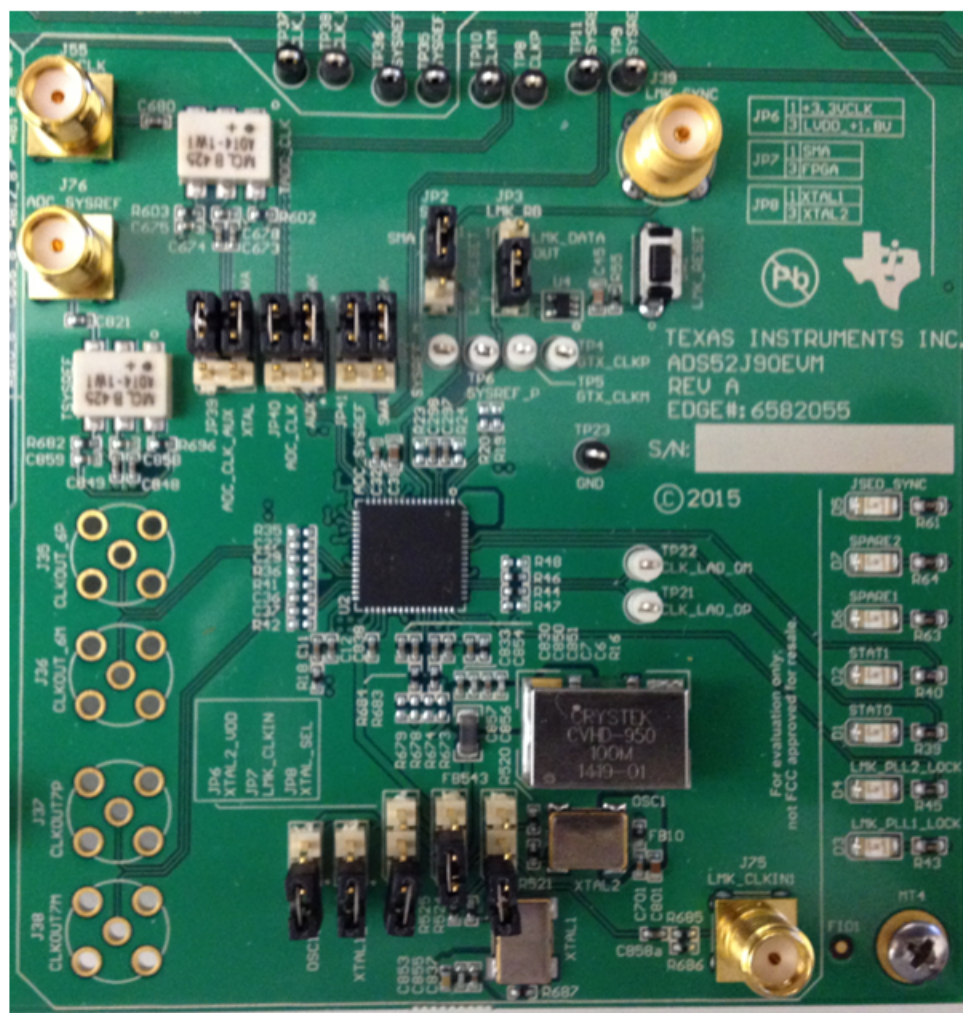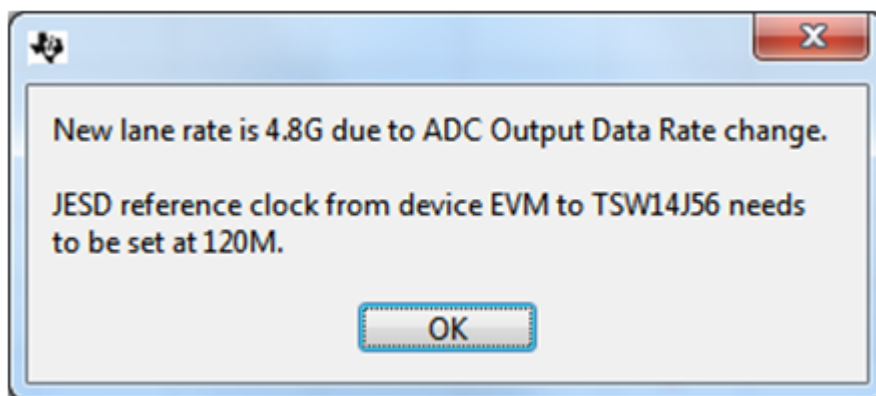


**Figure 3. Clock Config: LMK CDM Mode**

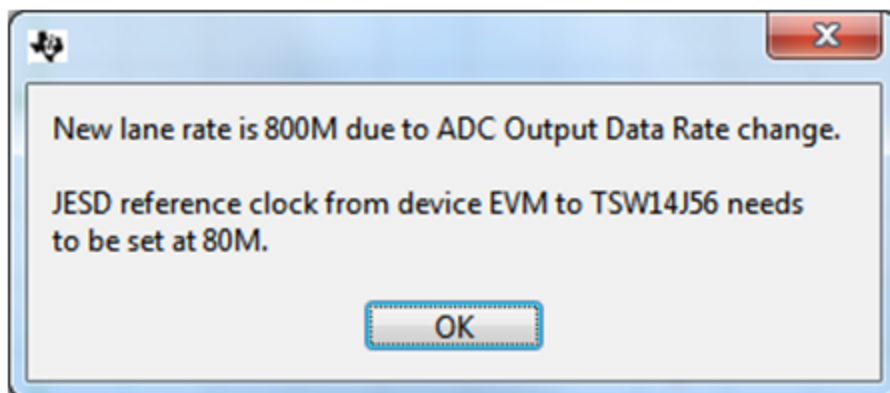**Figure 4. HSDCpro 40x Lane Rate Message**



**Figure 5. HSDCpro 10x Lane Rate Message**

## 4    Quick Test LVDS Interface

This section outlines the following:
- EVM Layout and Hardware Setup
- How to capture a RAMP and Sinusoidal Inputs for 16ch mode
- How to use scripts to measure all LVDS modes supported by the device

### *4.1  EVM Layout and Hardware Setup*

The ADS52J90 supports 3 modes of operation with respect to the analog inputs: (1) 32-channel mode, (2) 16-channel mode, (3) 8-channel mode. Figure 6 shows the breakdown of the analog channels on the EVM. Testing 32-channel mode is done using all Channels 1-24 on the EVM. Testing 16-channel mode is done using the odd channels of 1-23 on the EVM. These are the vertically-mounted SMAs. Testing 8-channel mode is done using Channels 7 and 8. Channel 7 is configured to accept a differential input to **SMA_CH7A** and **SMA_CH7** whereas Channel 8 is configured to convert a signal ended input to **SMA_CH8** into a differential signal via an amplifier.
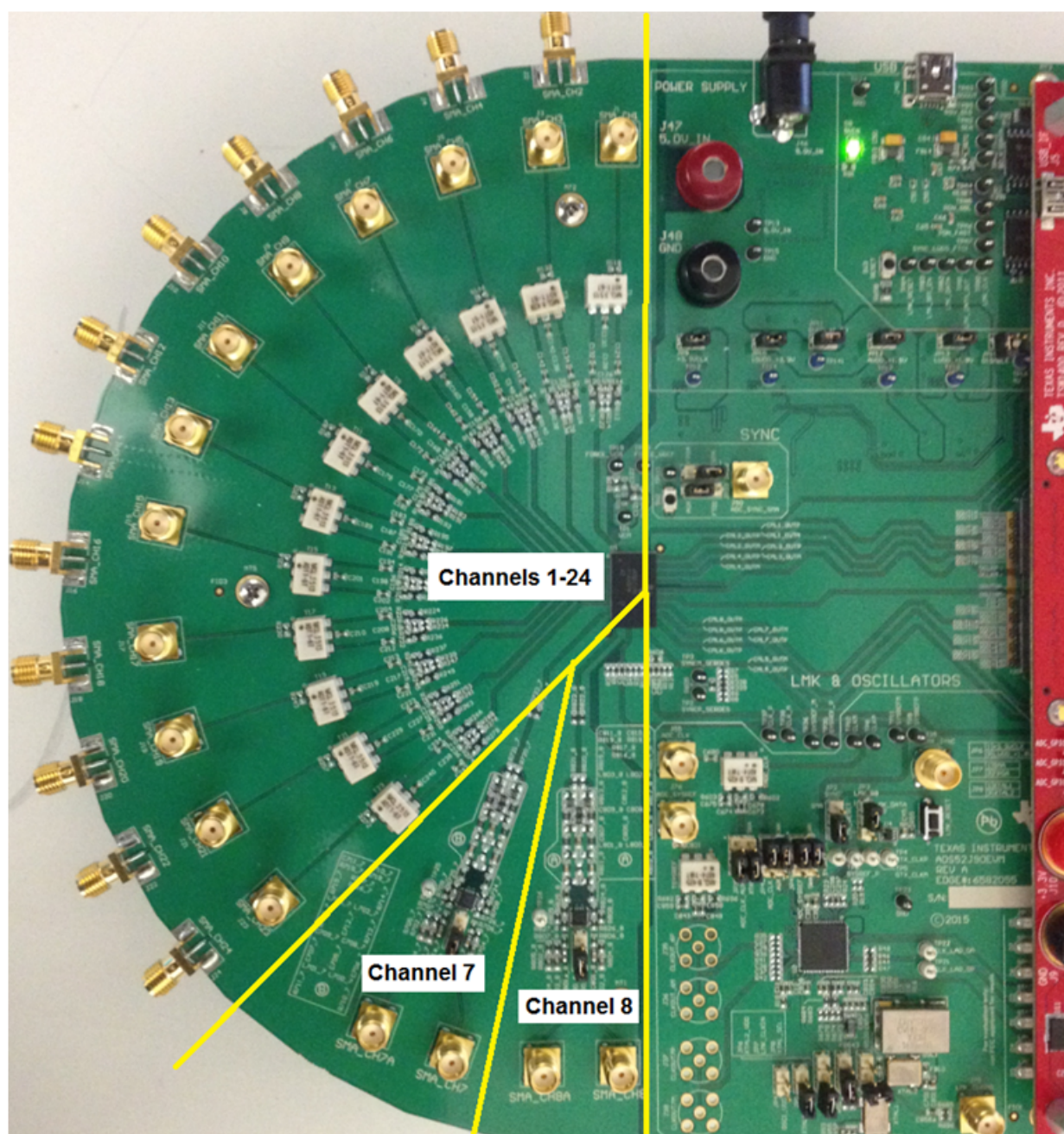
**Figure 6. ADS52J90 EVM Analog Channels**

The connections shown in Figure 7 should be made for proper hardware setup.

> **NOTE:** Testing the LVDS interface between the ADS52J90 EVM and the TSW1400 EVM can be performed using a RAMP test pattern generated within the ADS52J90 device in lieu of the signal source listed in item 7, in the following steps.
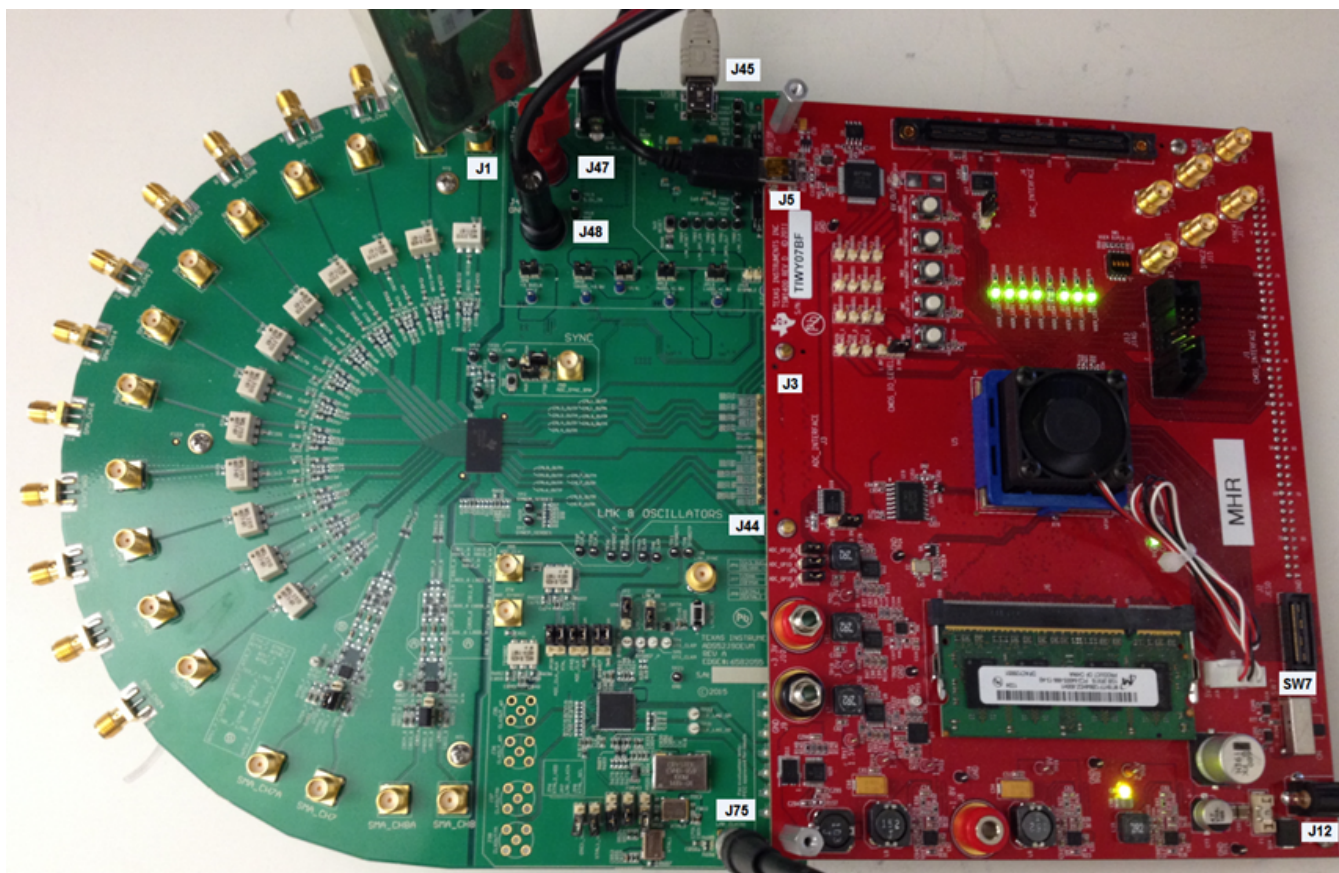
**Figure 7. TSW1400 and ADS52J90 Setup**

1. Mate the TSW1400 EVM at connector J3 to the ADS52J90 EVM at connector **J44** through the high speed ADC interface connector.

   **NOTE:** The two standoffs closest to J3 on the TSW1400 must be removed. Also, the EVM kit provides two supplementary standoffs that should be added to the remaining two standoffs so that the two EVMs are properly aligned.

2. Connect a DC +5-V power supply output of the provided AC-to-DC power supply to **J12 (+5V_IN)** of the TSW1400 EVM and the input of the power supply cable to a 110–230 VAC source.

3. Ensure that **SW7** is set to ON position on TSW1400.

4. Connect a DC +5-V power supply across banana jacks **J47** and **J48** on the ADS52J90 EVM. Alternatively, test points **TP13** and **TP15** can be used if alligator clip leads are available.

5. Connect the USB cable from the PC to **J45 (USB)** of the ADS52J90 EVM.

6. Connect the USB cable from the PC to **J5 (USB_IF)** of the TSW1400 EVM.

   **NOTE:**  TI recommends that the PC USB port be able to support USB2.0. If unsure, always chose the USB ports at the back of the PC chassis over ones located on the front or sides.

7.  Supply an analog input signal to SMA **J1 (SMA_CH1)** of the ADS52J90 EVM (such as +16 dBm, 5.0 MHz).

> **NOTE:** A low phase noise signal source (such as R&S SMA100A) with a band pass filter is needed in order to measure SNR values reported in the datasheet. Also, the instrument should have a 10-MHz back panel reference port allowing for coherent sampling when phase locked with the sampling clock signal.

8.  Supply a reference clock to SMA **J75 (LMK_CLKIN1)** of the ADS52J90 EVM that is equal to the desired system clock frequency. In the following examples 65 MHz is used as it supports all channel modes of the device.

> **NOTE:** A low phase noise, highly linear, signal source (such as RS SMA100A) is needed in order to measure SNR values reported in the datasheet. Also, the instrument should have a 10-MHz back panel reference port allowing for coherent sampling when phase locked with the analog input clock signal

## 4.2 *Capturing Ramp Test Pattern and Sinusoidal Input*

1.  With the hardware setup shown in Figure 7 established, launch the *High Speed Data Converter Pro GUI*. The GUI should automatically detect the serial number of the TSW1400 EVM connected as shown in Figure 8. Click on OK.
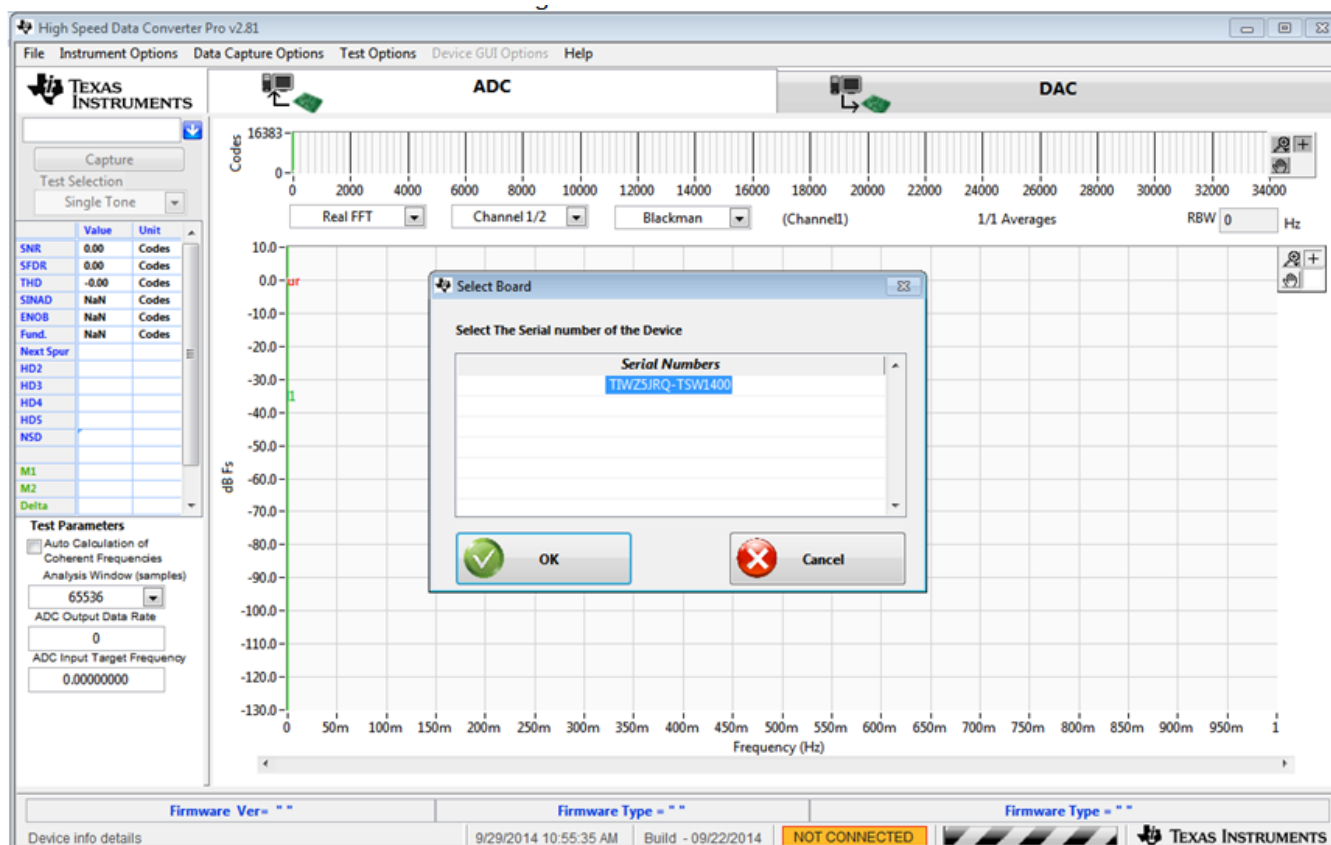


**Figure 8. TSW1400 GUI Setup (a)**
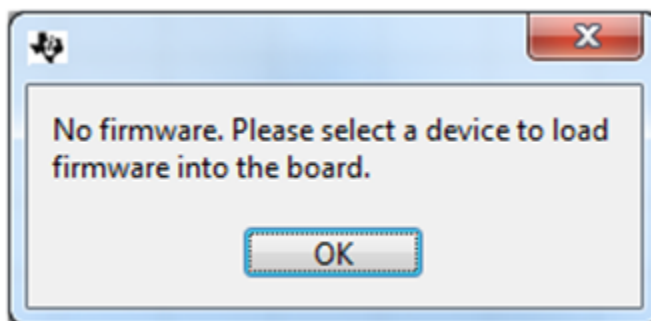
The message shown in Figure 9 will appear. Click OK.



**Figure 9. TSW1400 GUI Setup (b)**

If instead, the message shown in Figure 10 appears, it indicates that the USB connection to the TSW1400 EVM is not present. Click *OK*, then establish a USB connection and repeat step 1.
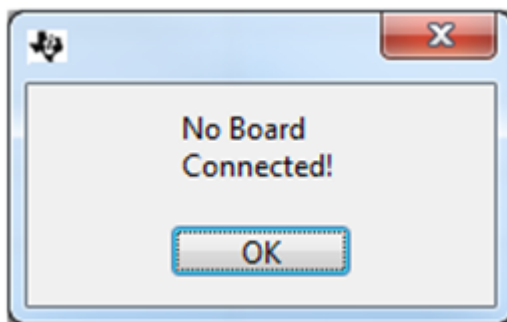


**Figure 10. TSW1400 GUI Setup (c)**

2. Select a device firmware to load in the FPGA by clicking on the blue arrow in the upper left corner of the *HSDCpro* GUI. Scroll down and select *ADS52J90* as shown in Figure 11.
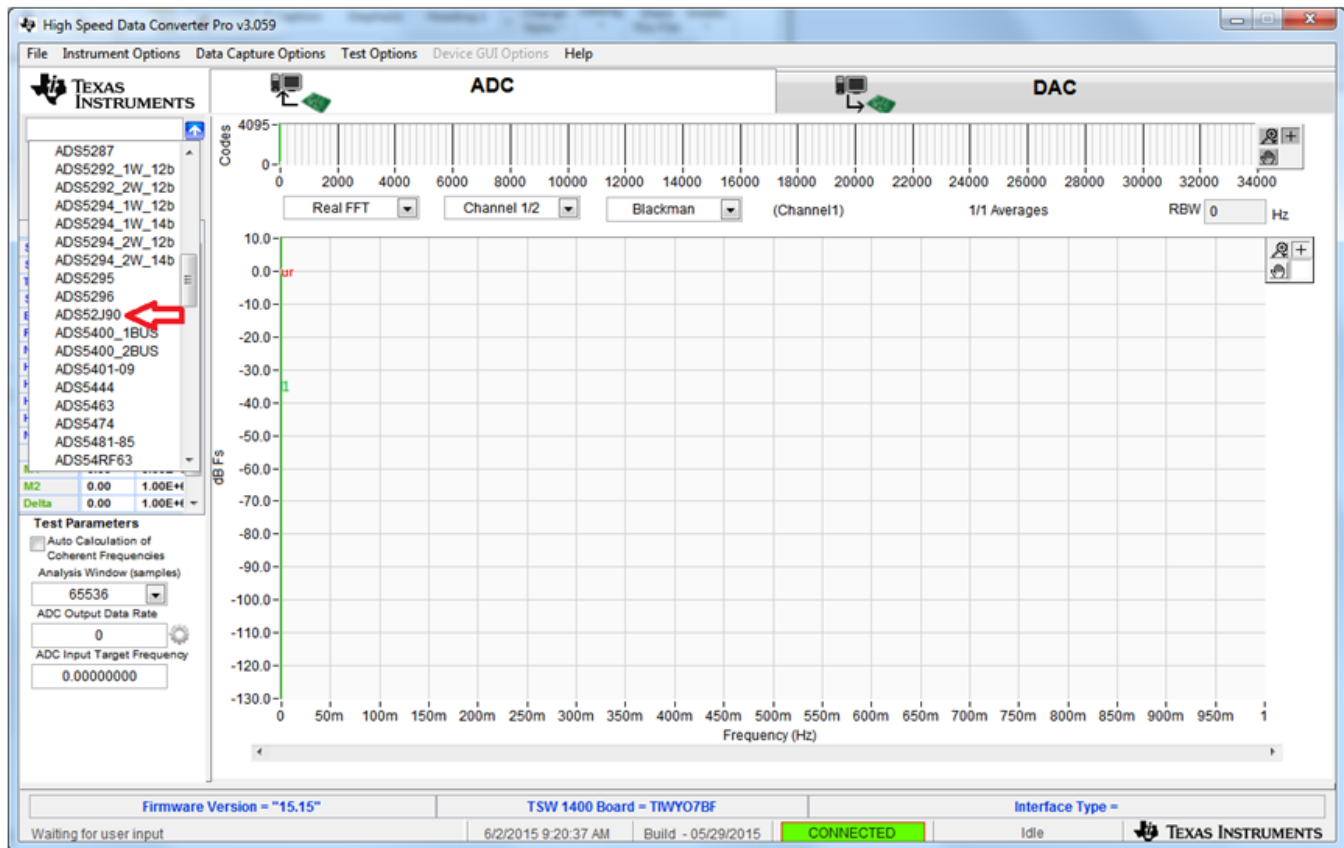


**Figure 11. TSW1400 GUI Setup (d)**

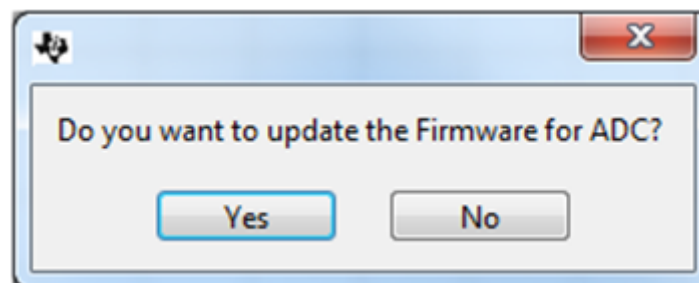Click the Yes button to update the ADC firmware on the TSW1400 FPGA as depicted in Figure 12.



**Figure 12. TSW1400 GUI Setup (e)**

While the firmware is being loaded into the TSW1400 FPGA, the graphic shown in Figure 13 will appear after which the device GUI (*HMC-DAQ*) will launch as shown in Figure 14.
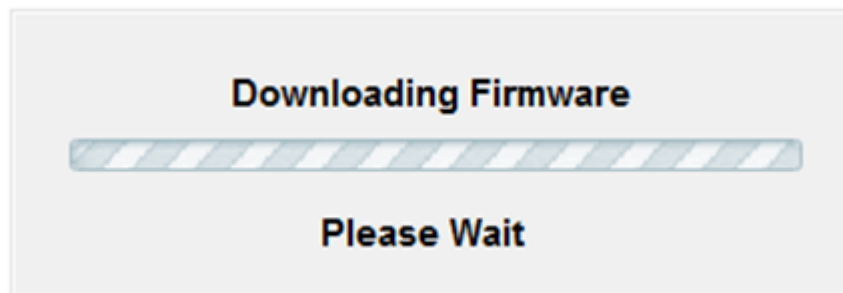


**Figure 13. TSW1400 GUI Setup (f)**
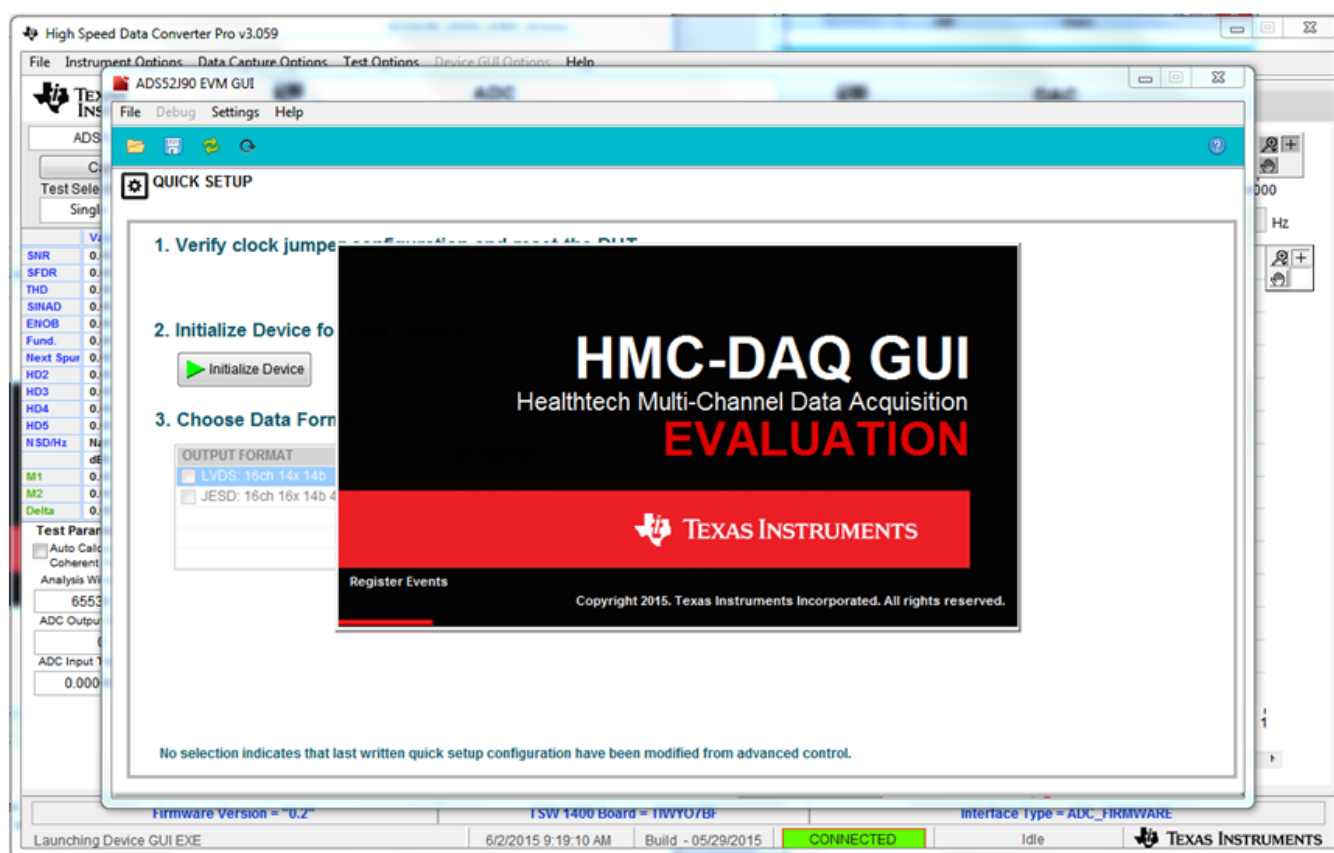


**Figure 14. HMC-DAQ GUI Setup (a)**

If the GUI recognizes that hardware is connected, HMC-DAQ will show HW CONNECTED in green in the border of the GUI as shown in Figure 15.
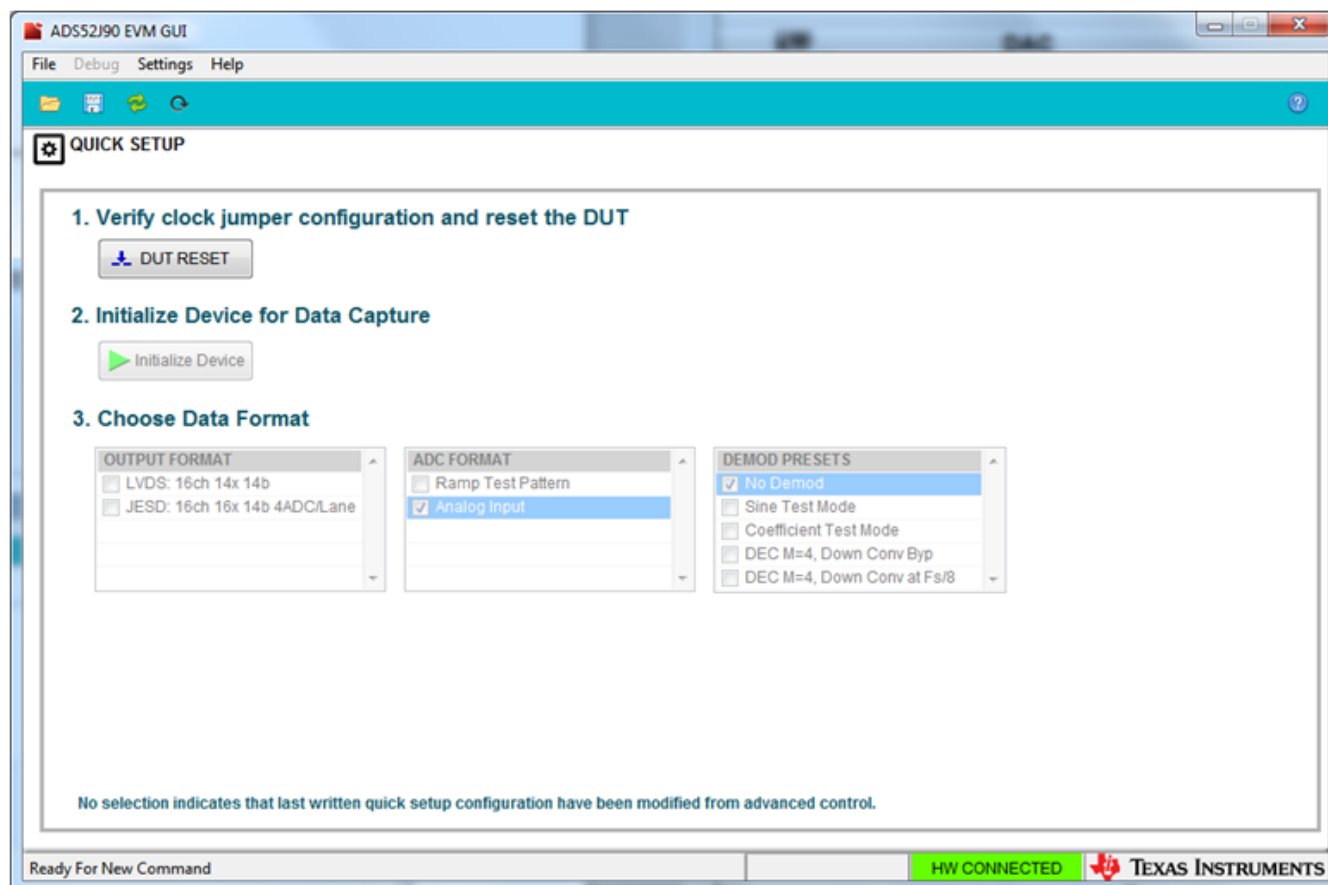


**Figure 15. HMC-DAQ GUI Setup (b)**

If instead, the message shown in Figure 16 appears, it indicates a USB connection issues between the PC and the ADS52J90 EVM. Close HSDCpro, establish USB connections and restart from procedure 1.
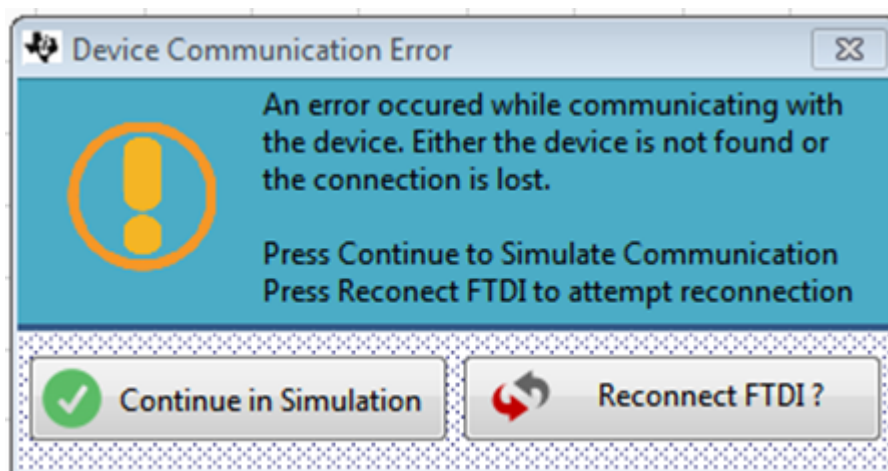


**Figure 16. HMC-DAQ GUI Setup (c)**

3. At this point there should be two GUI's running and connected, HSDCpro and HMC-DAQ which are communicating behind the scenes. Anytime the ADS52J90 device configuration is updated, HSDCpro is informed and the appropriate firmware updates are done automatically. To capture a RAMP test pattern in LVDS, 16-channel, 14 bit, 14x serialization configuration, do the following as shown in Figure 17:

(a) Press **DUT RESET** button

(b) Press **Initialize Device** button

(c) Check the box next to **LVDS 16ch 14x 14b**

(d) Check the box next to **Ramp Test Pattern**
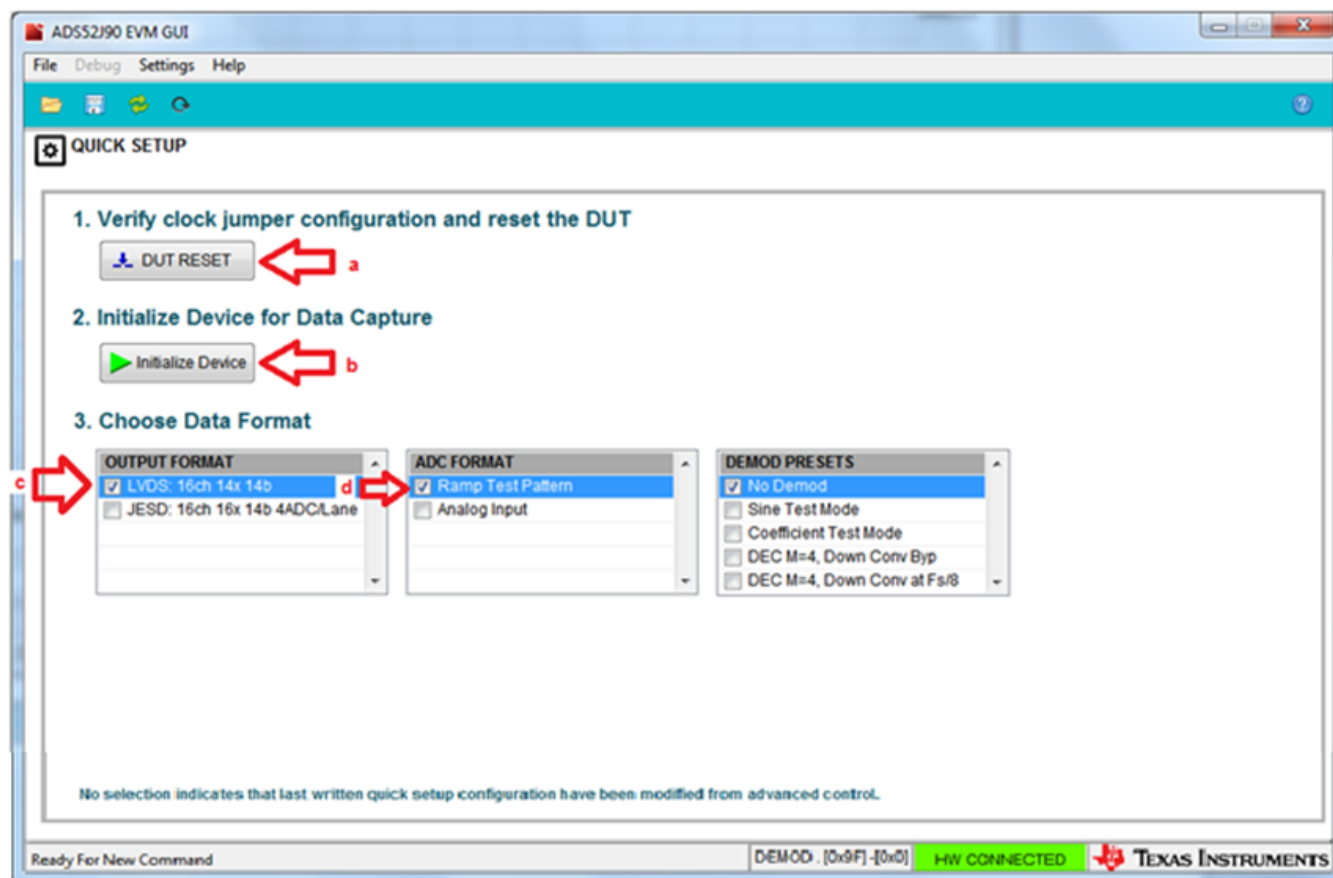


**Figure 17. HMC-DAQ GUI Setup (d)**

4. Return to HSDCpro GUI and perform the following steps as shown in Figure 18 .

(a) Change the plot type from *Real FFT to Codes*

(b) Enter 65M in the field labeled *ADC Output Data Rate*

(c) Press the *Capture* button.
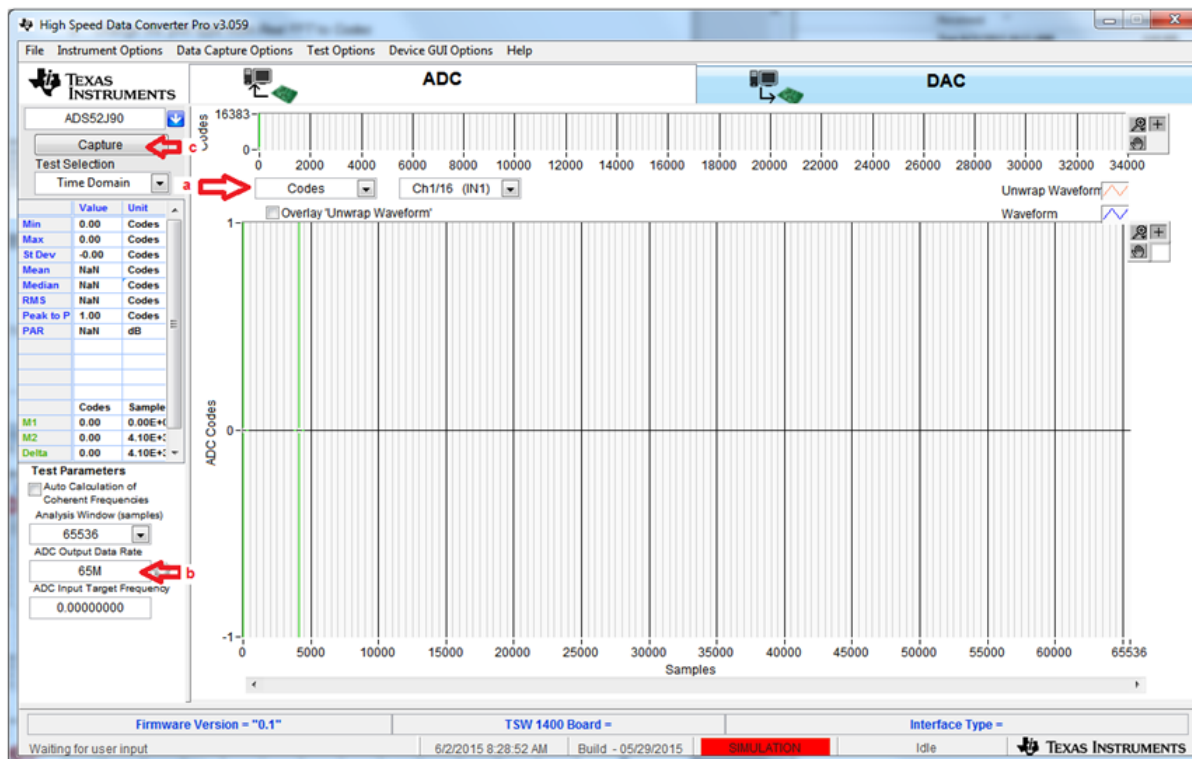


**Figure 18. ADS52J90 16-Channel RAMP Capture (a)**

A RAMP capture should appear as shown in Figure 19.
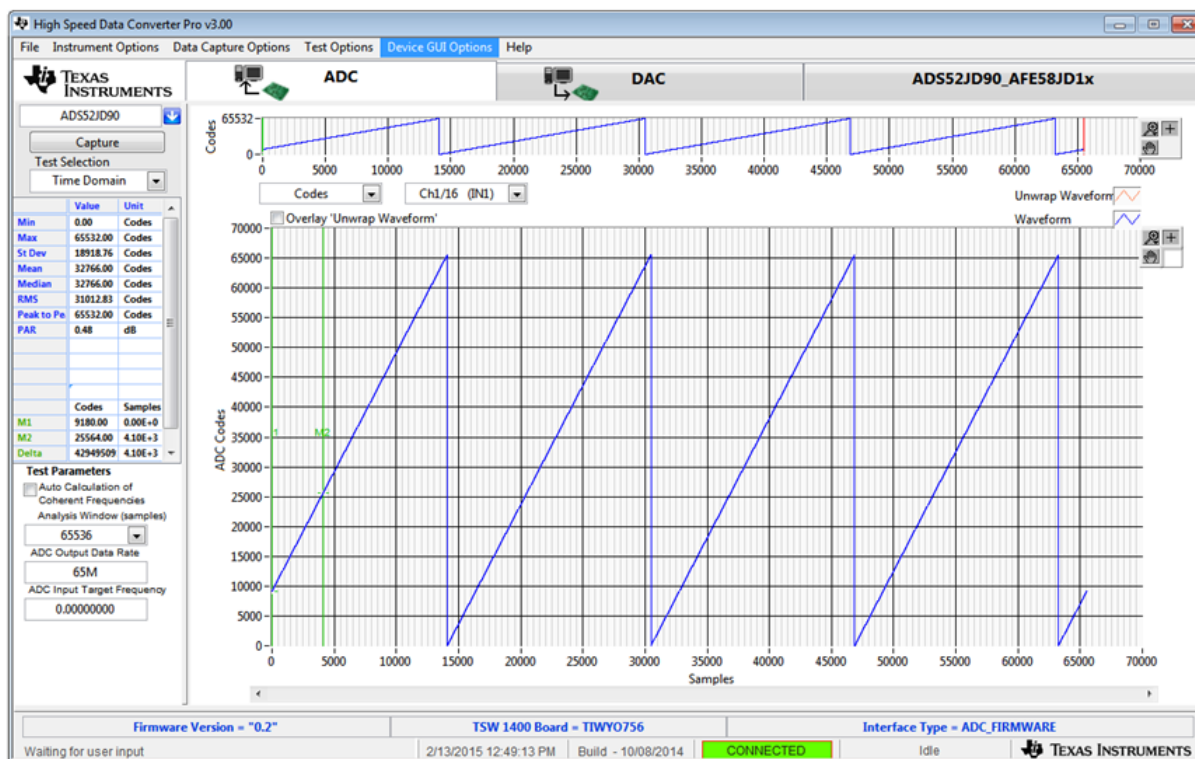


**Figure 19. ADS52J90 16-Channel RAMP Capture (b)**

By default, *Ch1 (16CH)* is the first channel displayed. Use the drop-down menu shown in Figure 20 to view any one 16 channels.
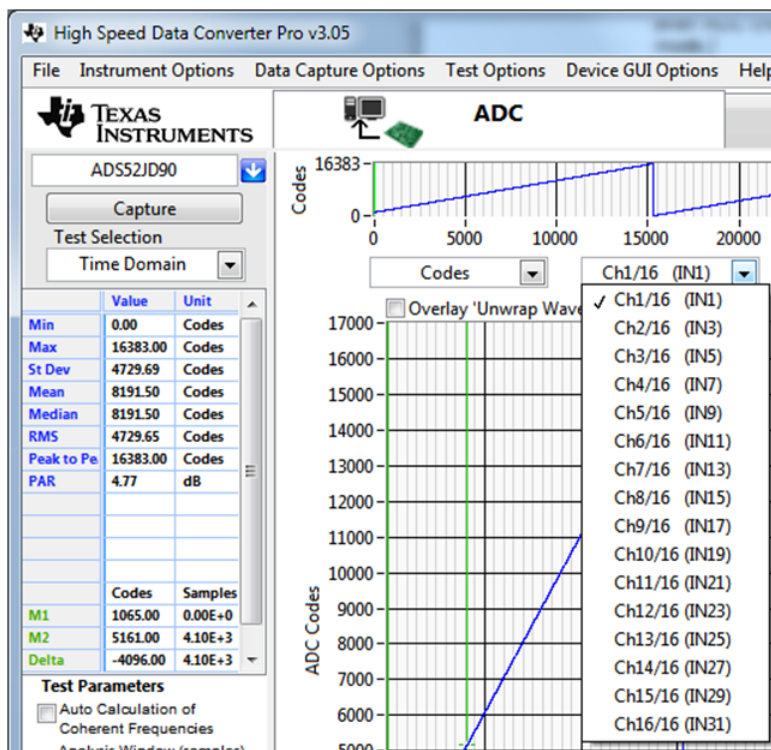


**Figure 20. ADS52J90 16-Channel RAMP Capture (c)**

Zooming into the waveform and changing the plot graphic (using the buttons to the upper right of graph), as shown in Figure 21, is recommended to confirm that the RAMP waveform is correct with each subsequent sample incremented 1 ADC code until max code of $(2^N) - 1$ is reached, where N is ADC resolution.
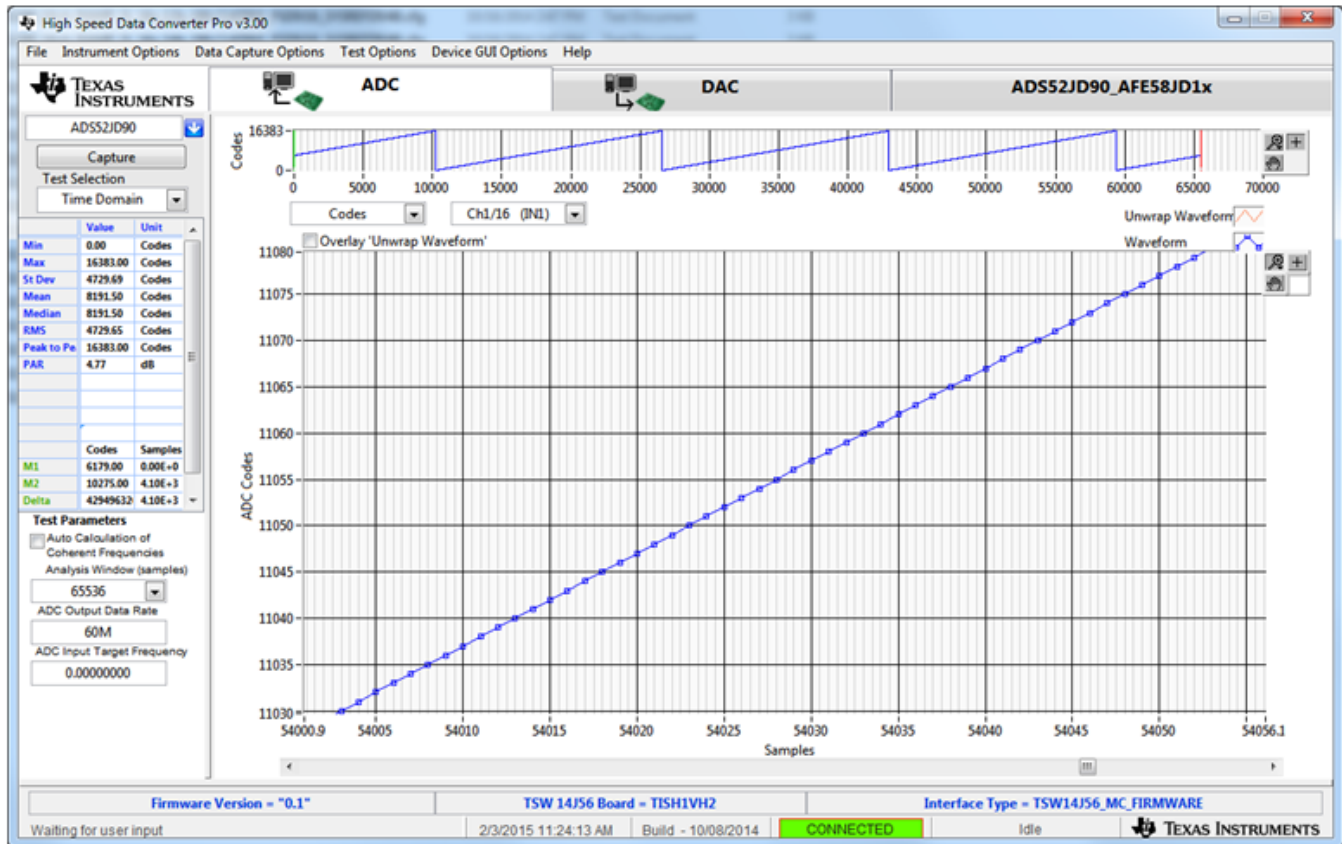


**Figure 21. ADS52J90 16-Channel RAMP Capture (d)**

5.  To capture a sinusoidal input, return to the HMC-DAQ GUI and press the check box next to **Analog Input** as shown in Figure 22.
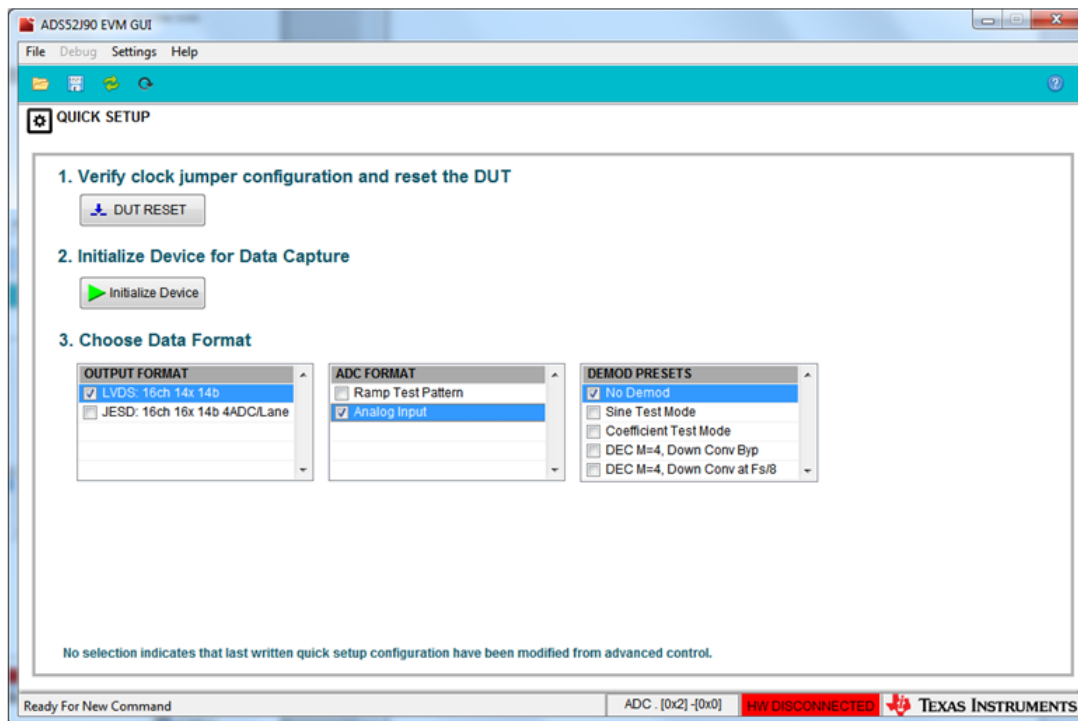


**Figure 22. ADS52J90 16-Channel SINE Capture (a)**

6. Return to HSDCpro GUI and perform the following (as illustrated in Figure 23):

   (a) Change the plot type from *Codes* to *Real FFT*

   (b) Enter *65M* in the field labeled *ADC Output Data Rate*

   (c) Enter *5.0M* in the field labeled *ADC Input Target Frequency* (or set to the desired input that is being provided to SMA **J1, SMA_CH1**, as described in ( Section 4.1).

   (d) Press the *Capture* button.
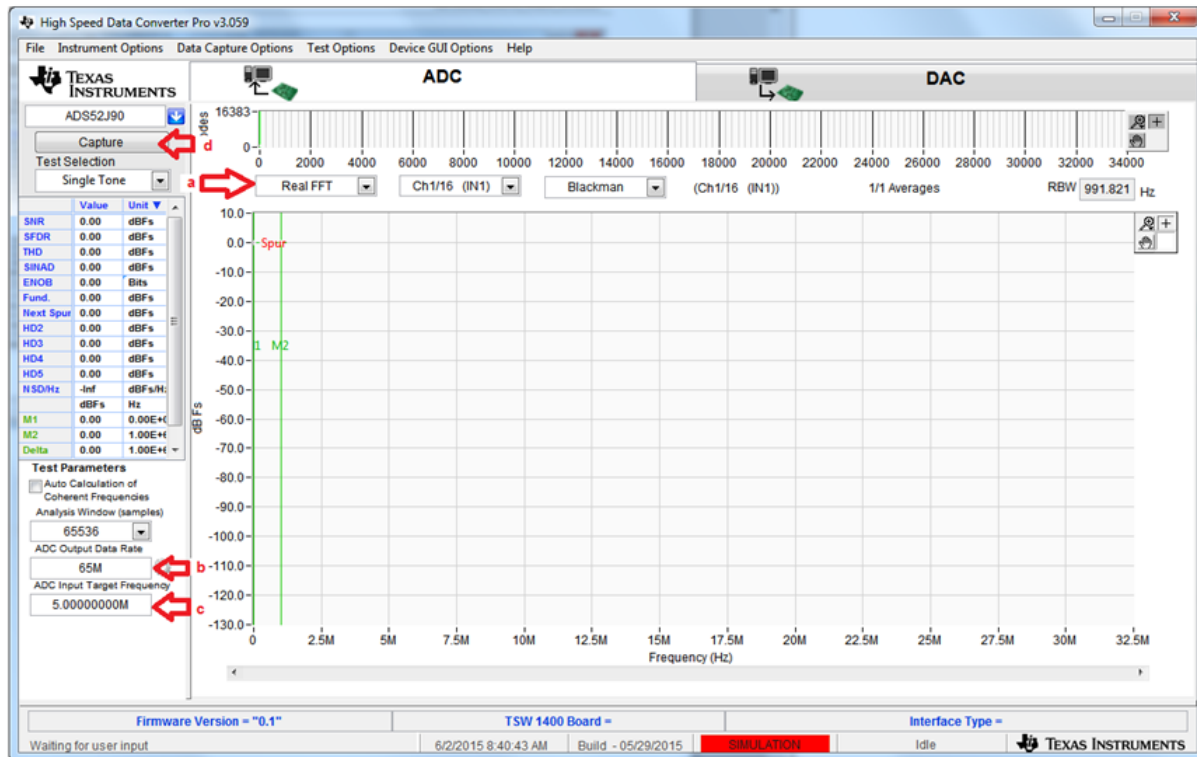


**Figure 23. ADS52J90 16-Channel SINE Capture (b)**

A capture similar to that shown in Figure 24 should appear.

NOTE: The analog input level was adjusted and a recapture done iteratively until the **Fund.** value was approximately –1 dBFs.
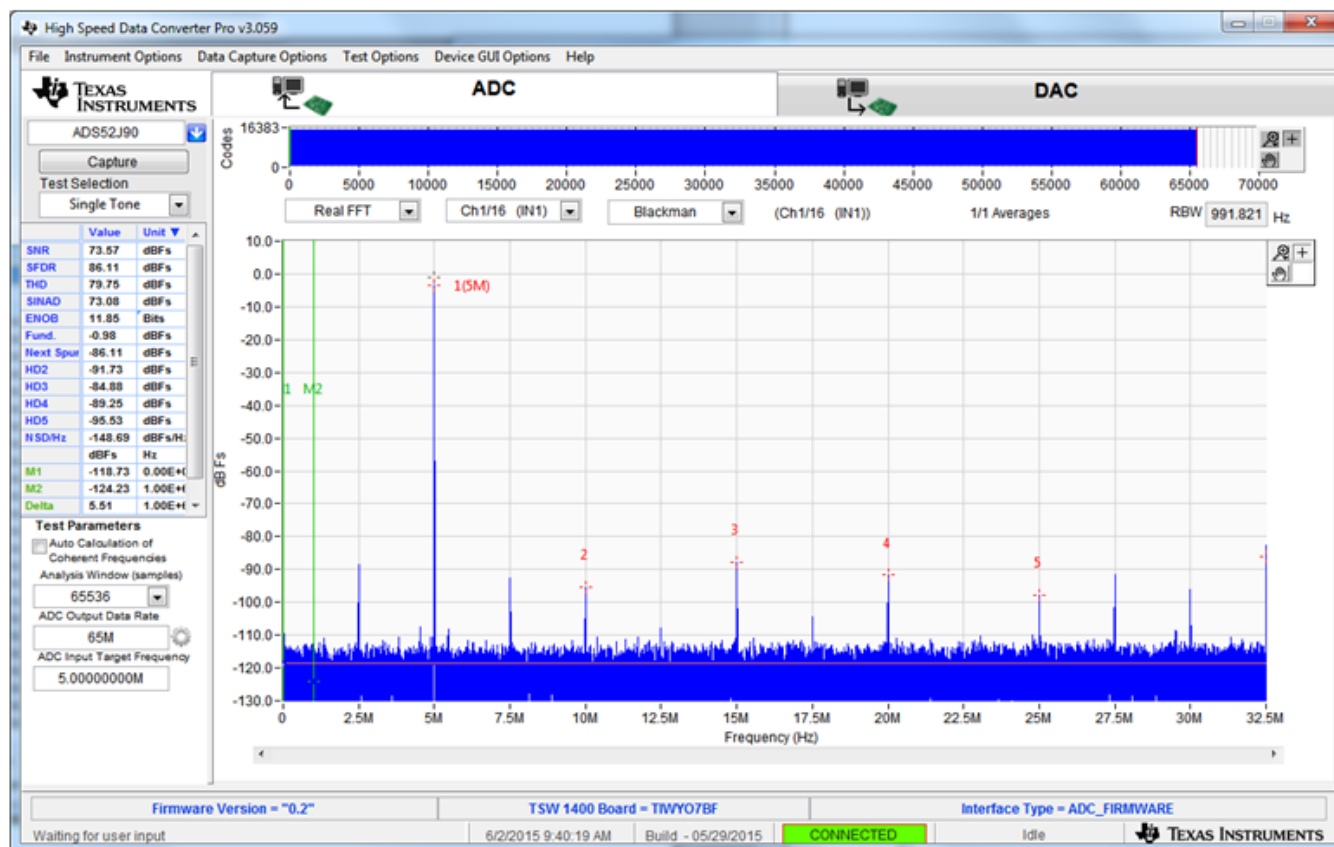


**Figure 24. ADS52J90 16-Channel SINE Capture (c)**

By default, *Ch1 (16CH)* is the first channel displayed. Use the drop-down menu to view any one 16 channels.

NOTE: The vertically-mounted SMAs on the EVM are the analog inputs to the odd ADC channels while the side-mounted SMAs are the analog inputs to the even ADC channels. Per the datasheet, only odd channels are being sampled when in 16-channel mode.

### 4.3    Testing All Modes of the Device

In addition to the quick start buttons provided on the **QUICK SETUP** tab of HMC-DAQ GUI, there are scripts to configure the device for all supported modes. To access the scripts, click on the folder icon in the upper left corner of the HMC-DAQ GUI, as shown in Figure 25.
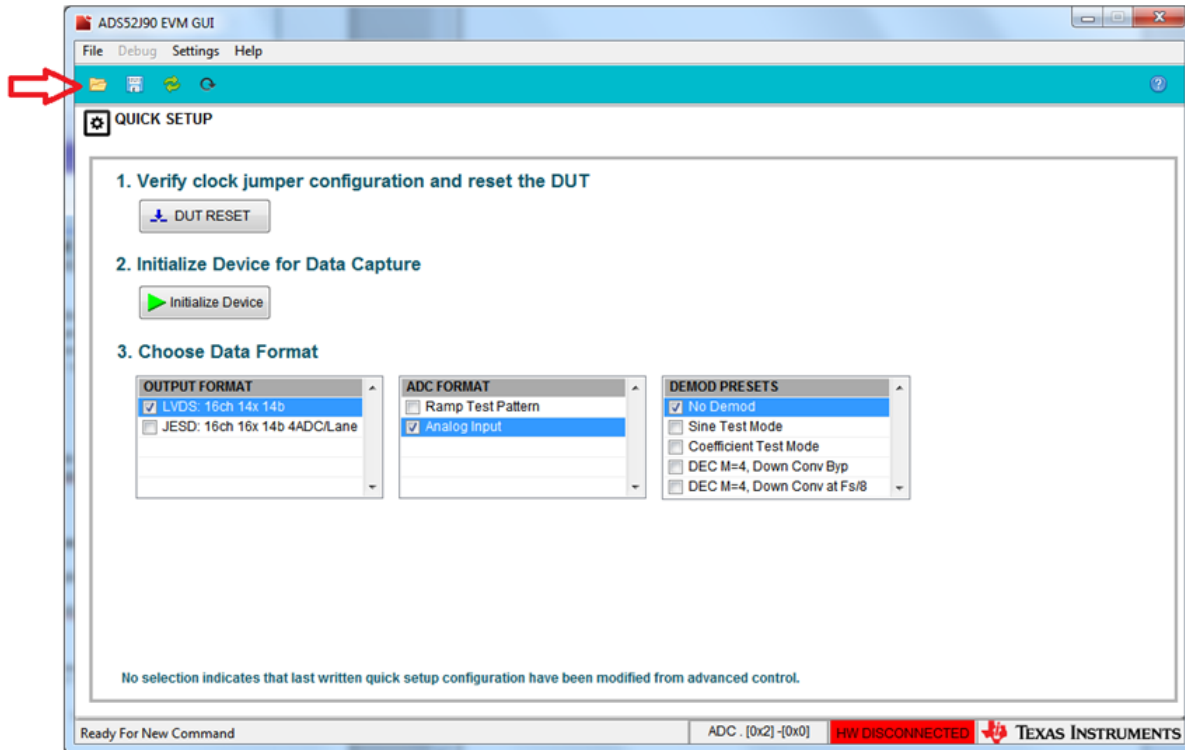


**Figure 25. ADS52J90 All Supported Configs**

Navigate to the folder …../*Scripts/ADS52J90/LVDS/LMK_CDM_MODE* as shown in Figure 26.
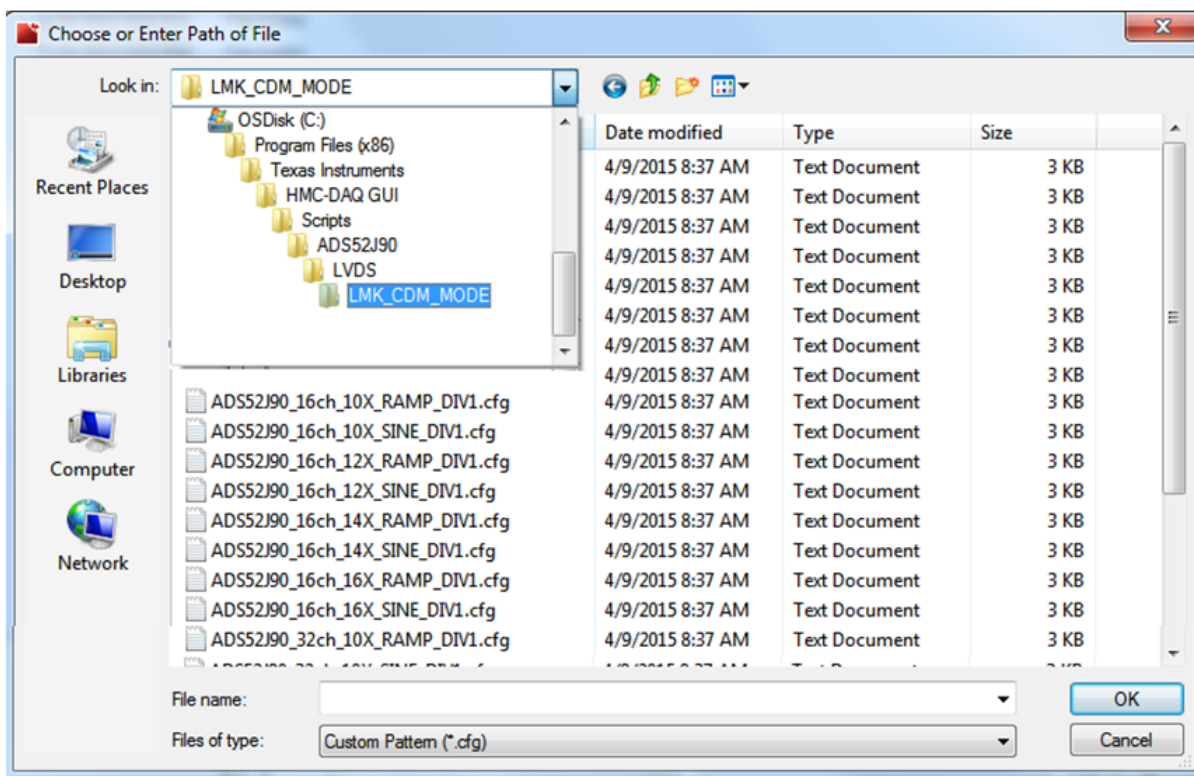


**Figure 26. ADS52J90 All Supported Configs (b)**

Select anyone of 24 configurations provided and then press *Capture* in HSDCpro. When testing 32-channel mode, ensure that the **ADC Output Data Rate** in HSDCpro is set to half the system clock being provided to the device. For example, if 65 MHz is supplied to **J75** then this value should be set to 32.5 MHz. When testing 8-channel or 16-channel modes, the **ADC Output Data Rate** should be set to the value of the system clock provided to the DUT.
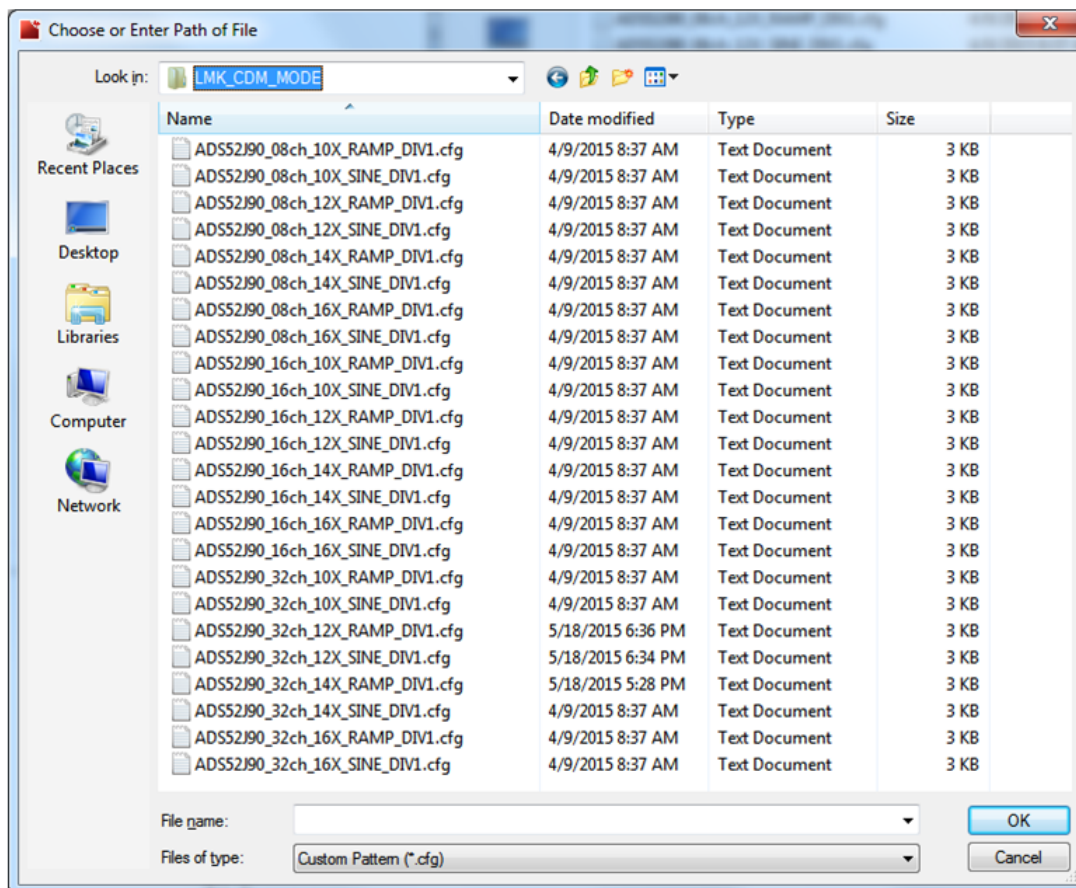


**Figure 27. ADS52J90 All Supported Configs (c)**

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    3.1.1 *Notice applicable to EVMs not FCC-Approved:*

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    3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

    **CAUTION**

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    Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

    **FCC Interference Statement for Class A EVM devices**

    *NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.*

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- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2  *Canada*

  3.2.1  *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210*

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**Concernant les EVMs avec antennes détachables**

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3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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