ADS54J60 – External DC offset correction

- ADS54J60 is a dual channel device. It can operate in 4 lane mode(default) or two lane mode per channel
- Each channel has four ADC cores @ Fs/4(Fs is the final sampling rate after interleaving).
- Sampling frequency of each ADC core = 250Mhz (Fs/4) and channel sampling rate @ 1Gsps
- Input clkp/m needs to be 1Ghz. Internal clock divide by four (default) sets the ADC core to 1GHz/4 = 250Mhz.
- Device operates in **subclass 1 mode** by default (LMFC reset using sysref signal)

The device has a DC corrector engine to correct the ADC core offsets. This removes the Fs/4 and Fs/2 spur in the FFT spectrum.

The following options are provided for the DC engine:

- The offset correction values (11 bit, signed (-1024 to1023)) estimated by the engine can be read out from the device.
- The DC offset values (11 bit) can be estimated externally and applied to the device via SPI writes.

The register map for DC OFFSET READ, FREEZE AND EXTERNAL CONFIGURATION is as below.

Register Address	Register Data							
A7-A0 in hex	D7	D6	D5	D4	D3	D2	D1	D0
offset_READ PAGE address: (0x61000000)								
0x68	TM_FREEZE_CORR	0	0	0	0	0	1	0
0x69	0	0	0	0	0	0	0	DC_EXTERNAL_FORCE_EN
0x74	ADC0_offset_read_back<7:0>							
0x75	0	0	0	0	0	ADC0_offset_read_back<10:8>		
0x76	ADC1_offset_read_back<7:0>							
0x77	0	0	0	0	0	ADC1_offset_read_back<10:8>		

0x78	ADC2_offset_read_back<7:0>					
0x79	0	0	0	0	0	ADC2_offset_read_back<10:8>
0x7A	ADC3_offset_read_back<7:0>					
0x7B	0	0	0	0	0	ADC3_offset_read_back<10:8>
offset_EXTERNAL_WRITE_PAGE address: (0x61000500)						
0x01	ADC0_offset_write_external<7:0>					
0x02	0	0	0	0	0	ADC0_offset_write_external<10:8>
0x04	ADC1_offset_write_external<7:0>					
0x05	0	0	0	0	0	ADC1_offset_write_external<10:8>
0x08	ADC2_offset_write_external<7:0>					
0x09	0	0	0	0	0	ADC2_offset_write_external<10:8>
0x0C	ADC3_offset_write_external<7:0>					
0x0D	0	0	0	0	0	ADC3_offset_write_external<10:8>

Example Writes for Channel A.

Format (16 bit address, 8 bit data)

// Read back the engine estimated DC corrector values for all the four cores of channel A

set_reg(0x4005,0x01) // Enable single channel writes
set_reg(0x4004,0x61) // Set page to 0x61000000
set_reg(0x4003,0x00)
set_reg(0x4002,0x00)
set_reg(0x4001,0x00)

// To read ADC0 offset corrector value (11 bit value, signed format)

$a=read_reg(0xE074,xx) , For read MSB bit needs to be '1', so 0x6000|0x8000 = 0xE000
$b=read_reg(0xE075,xx)
$DC_0 = (($b& 0x07)<<8)|$a;

$a=read_reg(0xE076,xx)
$b=read_reg(0xE077,xx)
$DC_1 = (($b& 0x07)<<8)|$a;

$a=read_reg(0xE078,xx)
$b=read_reg(0xE079,xx)
$DC_2 = (($b& 0x07)<<8)|$a;

$a=read_reg(0xE07A,xx)
$b=read_reg(0xE07B,xx)
$DC_3 = (($b& 0x07)<<8)|$a;

// To enable external offset correction

set_reg(0x6069,0x01)

// To write offset correction externally. Please note that these values do not get reflected in the read registers of the DC engine.

set_reg(0x4004,0x61) // Set page to 0x61000500
set_reg(0x4003,0x00)
set_reg(0x4002,0x05)
set_reg(0x4001,0x00)

set_reg(0x6000,DC_cor0<7:0>) // Write LSB 8 bit
set_reg(0x6001,"5'b00000 & DC_cor0<10:8>") // write MSB 3 bits

set_reg(0x6004,DC_cor1<7:0>) // Write LSB 8 bit
set_reg(0x6005,"5'b00000 & DC_cor1<10:8>") // write MSB 3 bits

set_reg(0x6008,DC_cor2<7:0>) // Write LSB 8 bit
set_reg(0x6009,"5'b00000 & DC_cor2<10:8>") // write MSB 3 bits

set_reg(0x600C,DC_cor3<7:0>) // Write LSB 8 bit
set_reg(0x600D,"5'b00000 & DC_cor3<10:8>") // write MSB 3 bits

For channel B:

Use 0x7000 for write + offset address
Use 0xF000 for write + offset address

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