

# 4. LMK04828

## ADS54Jxx GUI v1.8

Select the device

ADS54Jxx LMK04828 Low Level View

USB Status Reconnect FTDI ?

PLL1 Configuration | PLL2 Configuration | SYSREF and SYNC | **Clock Outputs**

**CLKout 0 and 1**  
*FPGA Clock & SYSREF*

**CLKout 2 and 3**  
*ADC Clock & SYSREF*

**CLKout 4 and 5**  
*Not Used*

**CLKout 6 and 7**  
*Not Used*

**CLKout 8 and 9**  
*Not Used*

**CLKout 10 and 11**  
*Not Used*

**CLKout 12 and 13**  
*Extra FMC Clocks*


CLKout 0 and 1 <i>FPGA Clock &amp; SYSREF</i>	CLKout 2 and 3 <i>ADC Clock &amp; SYSREF</i>	CLKout 4 and 5 <i>Not Used</i>	CLKout 6 and 7 <i>Not Used</i>	CLKout 8 and 9 <i>Not Used</i>	CLKout 10 and 11 <i>Not Used</i>	CLKout 12 and 13 <i>Extra FMC Clocks</i>
Group Powerdown <input type="checkbox"/>	Group Powerdown <input type="checkbox"/>	Group Powerdown <input checked="" type="checkbox"/>	Group Powerdown <input checked="" type="checkbox"/>	Group Powerdown <input checked="" type="checkbox"/>	Group Powerdown <input checked="" type="checkbox"/>	Group Powerdown <input type="checkbox"/>
Output Drive Level <input type="checkbox"/>	Output Drive Level <input checked="" type="checkbox"/>	Output Drive Level <input type="checkbox"/>	Output Drive Level <input type="checkbox"/>	Output Drive Level <input type="checkbox"/>	Output Drive Level <input type="checkbox"/>	Output Drive Level <input type="checkbox"/>
Input Drive Level <input type="checkbox"/>	Input Drive Level <input checked="" type="checkbox"/>	Input Drive Level <input type="checkbox"/>	Input Drive Level <input type="checkbox"/>	Input Drive Level <input type="checkbox"/>	Input Drive Level <input type="checkbox"/>	Input Drive Level <input type="checkbox"/>
DCLK Divider 30	DCLK Divider 3	DCLK Divider 8	DCLK Divider 8	DCLK Divider 8	DCLK Divider 8	DCLK Divider 30
DCLK Source Divider	DCLK Source Divider	DCLK Source Divider	DCLK Source Divider	DCLK Source Divider	DCLK Source Divider	DCLK Source Divider
DCLK Type Invert <input type="checkbox"/>	DCLK Type Invert <input type="checkbox"/>	DCLK Type Invert <input type="checkbox"/>	DCLK Type Invert <input type="checkbox"/>	DCLK Type Invert <input type="checkbox"/>	DCLK Type Invert <input type="checkbox"/>	DCLK Type Invert <input type="checkbox"/>
DCLK Type LVDS	DCLK Type LVPECL 2000 mV	DCLK Type LVDS	DCLK Type LVDS	DCLK Type LVDS	DCLK Type LVDS	DCLK Type LVDS
SDCLK Source SYSREF	SDCLK Source SYSREF	SDCLK Source Device Clock	SDCLK Source Device Clock	SDCLK Source Device Clock	SDCLK Source Device Clock	SDCLK Source Device Clock
SDCLK Type Invert <input type="checkbox"/>	SDCLK Type Invert <input type="checkbox"/>	SDCLK Type Invert <input type="checkbox"/>	SDCLK Type Invert <input type="checkbox"/>	SDCLK Type Invert <input type="checkbox"/>	SDCLK Type Invert <input type="checkbox"/>	SDCLK Type Invert <input type="checkbox"/>
SDCLK Type LVDS	SDCLK Type Powerdown	SDCLK Type Powerdown	SDCLK Type Powerdown	SDCLK Type Powerdown	SDCLK Type Powerdown	SDCLK Type Powerdown
SDCLK EN/DIS State Active/Active	SDCLK EN/DIS State Active/Active	SDCLK EN/DIS State Active/Active	SDCLK EN/DIS State Active/Active	SDCLK EN/DIS State Active/Active	SDCLK EN/DIS State Active/Active	SDCLK EN/DIS State Active/Active
SDCLKout_PD <input type="checkbox"/>	SDCLKout_PD <input type="checkbox"/>	SDCLKout_PD <input checked="" type="checkbox"/>	SDCLKout_PD <input checked="" type="checkbox"/>	SDCLKout_PD <input checked="" type="checkbox"/>	SDCLKout_PD <input checked="" type="checkbox"/>	SDCLKout_PD <input type="checkbox"/>
DCLKout_DDLY_PD <input checked="" type="checkbox"/>	DCLKout_DDLY_PD <input checked="" type="checkbox"/>	DCLKout_DDLY_PD <input type="checkbox"/>	DCLKout_DDLY_PD <input type="checkbox"/>	DCLKout_DDLY_PD <input type="checkbox"/>	DCLKout_DDLY_PD <input type="checkbox"/>	DCLKout_DDLY_PD <input type="checkbox"/>
DCLKout_HSg_PD <input checked="" type="checkbox"/>	DCLKout_HSg_PD <input checked="" type="checkbox"/>	DCLKout_HSg_PD <input checked="" type="checkbox"/>	DCLKout_HSg_PD <input checked="" type="checkbox"/>	DCLKout_HSg_PD <input checked="" type="checkbox"/>	DCLKout_HSg_PD <input checked="" type="checkbox"/>	DCLKout_HSg_PD <input checked="" type="checkbox"/>
DCLKout_ADLYg_PD <input checked="" type="checkbox"/>	DCLKout_ADLYg_PD <input checked="" type="checkbox"/>	DCLKout_ADLYg_PD <input checked="" type="checkbox"/>	DCLKout_ADLYg_PD <input checked="" type="checkbox"/>	DCLKout_ADLYg_PD <input checked="" type="checkbox"/>	DCLKout_ADLYg_PD <input checked="" type="checkbox"/>	DCLKout_ADLYg_PD <input checked="" type="checkbox"/>
DCLKout_ADLY_PD <input checked="" type="checkbox"/>	DCLKout_ADLY_PD <input checked="" type="checkbox"/>	DCLKout_ADLY_PD <input checked="" type="checkbox"/>	DCLKout_ADLY_PD <input checked="" type="checkbox"/>	DCLKout_ADLY_PD <input checked="" type="checkbox"/>	DCLKout_ADLY_PD <input checked="" type="checkbox"/>	DCLKout_ADLY_PD <input checked="" type="checkbox"/>

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## ADS54Jxx GUI v1.8

Select the device

ADS54Jxx LMK04828 Low Level View

USB Status  Reconnect FTDI ?

PLL1 Configuration PLL2 Configuration **SYSREF and SYNC** Clock Outputs

### SYSREF Configuration

SYSREF Source

SYSREF Divider

SYSREF Block PD

SYSREF PD

SYSREF DDLY PD

SYSREF Pulser PD

Pulse Count

### Global DDLY

DDLY Step Count

SYSREF DDLY

SYSREF DDLY EN

### SYNC Configuration

SYNC Mode

SYSREF SYNC Disable

DCLKout0 SYNC Disable

DCLKout2 SYNC Disable

DCLKout4 SYNC Disable

**Pulsed SYSREF must be configured before triggering will work.**

**Trigger SYSREF**

DCLKout6 SYNC Disable

DCLKout8 SYNC Disable

DCLKout10 SYNC Disable

DCLKout12 SYNC Disable

SYNC Pin Polarity

SYNC Enable

SYNC until PLL2 DLD

SYNC until PLL1 DLD

### CLKout Delays

#### CLKout 0 and 1 FPGA Clock & SYSREF

DCLK Delay

Dynamic DDLY EN

DCLK Continuous?

HS  # High  # Low

ADLY Input

ADLY (ps)

SDCLK Delay

HS  ADLY EN

DDLY  ADLY (ps)

#### CLKout 2 and 3 ADC Clock & SYSREF

DCLK Delay

Dynamic DDLY EN

DCLK Continuous?

HS  # High  # Low

ADLY Input

ADLY (ps)

SDCLK Delay

HS  ADLY EN

DDLY  ADLY (ps)

#### CLKout 4 and 5 Not Used

DCLK Delay

Dynamic DDLY EN

DCLK Continuous?

HS  # High  # Low

ADLY Input

ADLY (ps)

SDCLK Delay

HS  ADLY EN

DDLY  ADLY (ps)

#### CLKout 6 and 7 Not Used

DCLK Delay

Dynamic DDLY EN

DCLK Continuous?

HS  # High  # Low

ADLY Input

ADLY (ps)

SDCLK Delay

HS  ADLY EN

DDLY  ADLY (ps)

#### CLKout 8 and 9 Not Used

DCLK Delay

Dynamic DDLY EN

DCLK Continuous?

HS  # High  # Low

ADLY Input

ADLY (ps)

SDCLK Delay

HS  ADLY EN

DDLY  ADLY (ps)

#### CLKout 10 and 11 Not Used

DCLK Delay

Dynamic DDLY EN

DCLK Continuous?

HS  # High  # Low

ADLY Input

ADLY (ps)

SDCLK Delay

HS  ADLY EN

DDLY  ADLY (ps)

#### CLKout 12 and 13 Extra FMC Clocks

DCLK Delay

Dynamic DDLY EN

DCLK Continuous?

HS  # High  # Low

ADLY Input

ADLY (ps)

SDCLK Delay

HS  ADLY EN

DDLY  ADLY (ps)

# 4. LMK04828

## ADS54Jxx GUI v1.8

Select the device

ADS54Jxx LMK04828 Low Level View

USB Status ● Reconnect FTDI ?

PLL1 Configuration PLL2 Configuration **SYSREF and SYNC** Clock Outputs

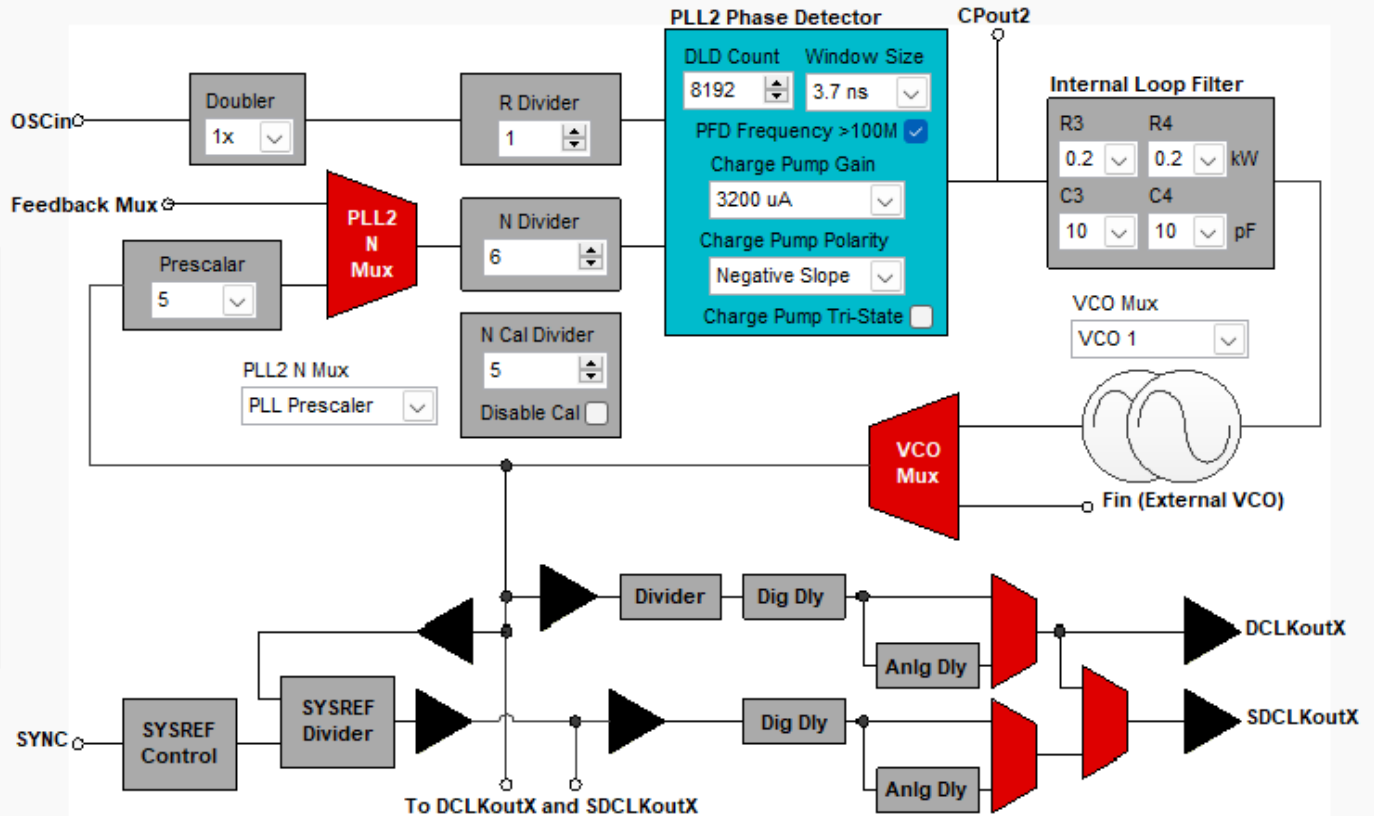
### OSCIin Configuration

OSCIin PD  PLL2 XTAL Enable

OSCIin Frequency

### Inputs and Indicators

Status LD1 Mux <input type="text" value="PLL1 DLD"/>	Status LD1 Type <input <="" td="" type="text" value="Output (push-)"/>
Status LD2 Mux <input type="text" value="PLL2 DLD"/>	Status LD2 Type <input <="" td="" type="text" value="Output (push-)"/>
CLKin SEL0 Mux <input type="text" value="Logic Low"/>	CLKin SEL0 Type <input <="" td="" type="text" value="Input w/ pull-"/>
CLKin SEL1 Mux <input type="text" value="Logic Low"/>	CLKin SEL1 Type <input <="" td="" type="text" value="Input w/ pull-"/>
RESET Mux <input type="text" value="SPI Readback"/>	RESET Type <input <="" td="" type="text" value="Output (push-)"/>



To DCLKoutX and SDCLKoutX

# 4. LMK04828

ADS54Jxx LMK04828 Low Level View

USB Status ● Reconnect FTDI ?

PLL1 Configuration **PLL2 Configuration** SYSREF and SYNC Clock Outputs

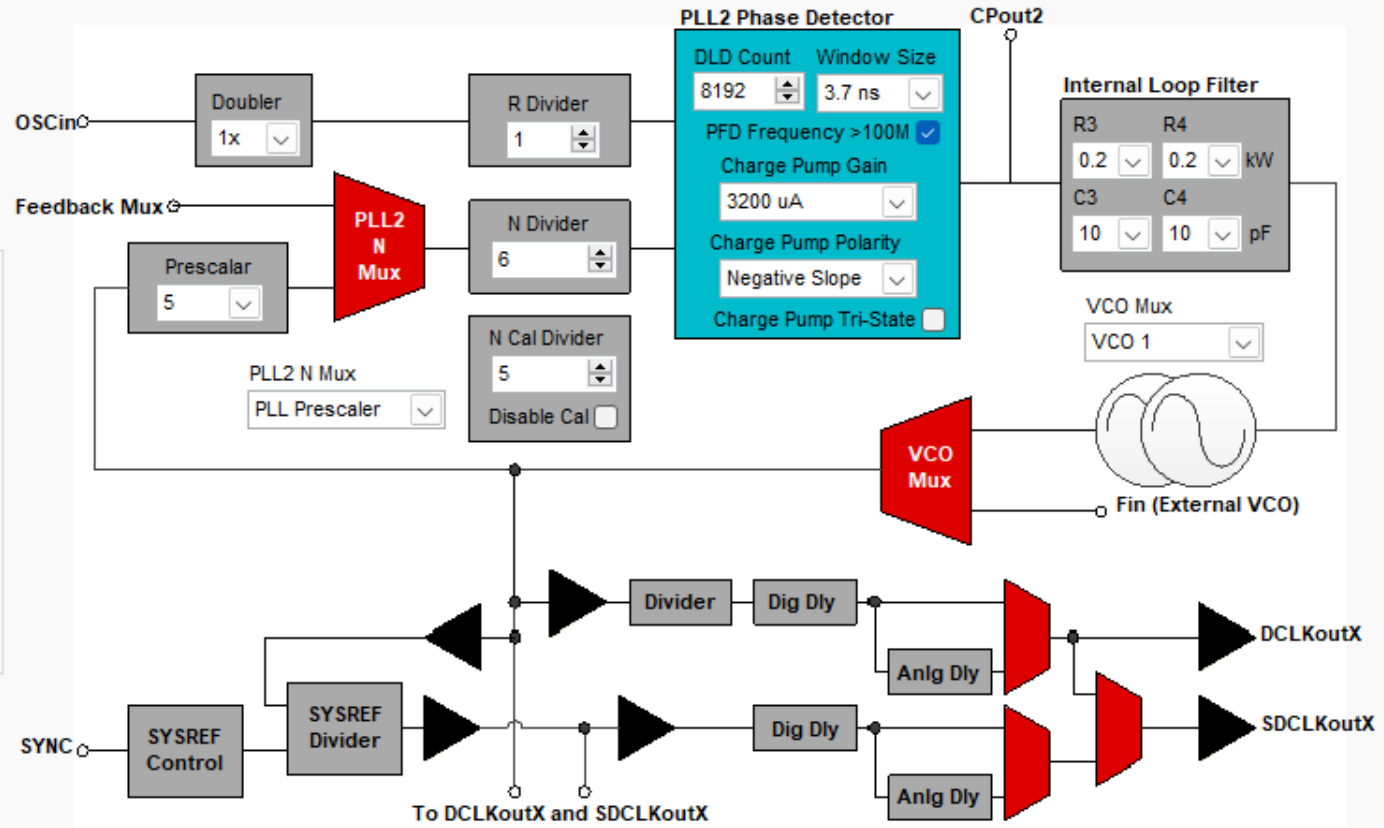
**OSCI<sub>in</sub> Configuration**

OSCI<sub>in</sub> PD  PLL2 XTAL Enable

OSCI<sub>in</sub> Frequency

**Inputs and Indicators**

Status LD1 Mux <input type="text" value="PLL1 DLD"/>	Status LD1 Type <input <="" td="" type="text" value="Output (push-)"/>
Status LD2 Mux <input type="text" value="PLL2 DLD"/>	Status LD2 Type <input <="" td="" type="text" value="Output (push-)"/>
CLKin SEL0 Mux <input type="text" value="Logic Low"/>	CLKin SEL0 Type <input <="" td="" type="text" value="Input w/ pull-"/>
CLKin SEL1 Mux <input type="text" value="Logic Low"/>	CLKin SEL1 Type <input <="" td="" type="text" value="Input w/ pull-"/>
RESET Mux <input type="text" value="SPI Readback"/>	RESET Type <input <="" td="" type="text" value="Output (push-)"/>



To DCLKoutX and SDCLKoutX

# 4. ADJ54J69

ADS54Jxx

LMK04828

Low Level View

USB Status



Reconnect FTDI ?

## RESET, Miscellaneous

- Analog Core Reset
- Digital Core Reset (Not self-clearing)
- Flip ADC Data
- Ignore SYSREF

## JESD Test Patterns

- EN Long Transport Layer Test Pattern
- Link Layer Testmode  
Testmode Disabled
- Change RPAT Disparity

## LMFC Control

- LMFC Resetting Disabled
- Use Different LMFC Counter Starting Value
- LMFC Counter Starting Value  
0

## EVM Startup Sequence

1. Load appropriate clock configuration using the "Load Config" button on the "Low Level View" tab. Choose the file based on the sample rate if the onboard clock is used or choose the external clock file to use an external clock. Note that for the ADS54J69 decimation modes, the sampling rate should be chosen as 2 or 4 times larger than the final data rate. For instance, if the final data rate is 256 Msps after 4x decimation, then 1024 Msps should be chosen as the sampling rate. In this case, the "ADC Output Data Rate" in HSDCPro should be set to "256M".
2. Press the "ADC RESET" button (SW1) on the EVM to provide a hardware reset to the ADC.
3. Load the ADC configuration file using the "Load Config" button on the "Low Level View" tab.

## JESD204B Core Setup

- JESD Mode  
LMFS 8224
- JESD PLL Mode  
20x mode, 4 Lanes/ADC
- EN Programming of K  
Frames per Multi-Frame (K)  
16
- Enable /A/ Character Replacement for Lane Alignment Monitoring
- Enable /F/ Character Replacement for Frame Alignment Monitoring
- Scrambling EN
- JESD204B Subclass  
Subclass 0

## Powerdown

- Global PDN
- Override PDN Pin

## Manual SYNC Control

- Enable Software SYNC
- Software SYNC  
Sync Deasserted

## ILA Sequence

- Disable ILA Sequence
- ILA Sequence Delay  
No Delay

# 5. Measure LMK04828 by 1Gbps Oscilloscope

1. DCLKOUT0(FPGA\_JESD\_CLK) : 100MHz/0.2V
2. SDCLKOUT1(FPGA\_JESD\_SYSREF) : 3.9MHz/
3. DCLKOUT2(CLK) : not measured
4. SDCLKOUT3(SYSREF) : not measured
5. DCLKOUT12(CLK\_LAO) : 100MHz/0.2V