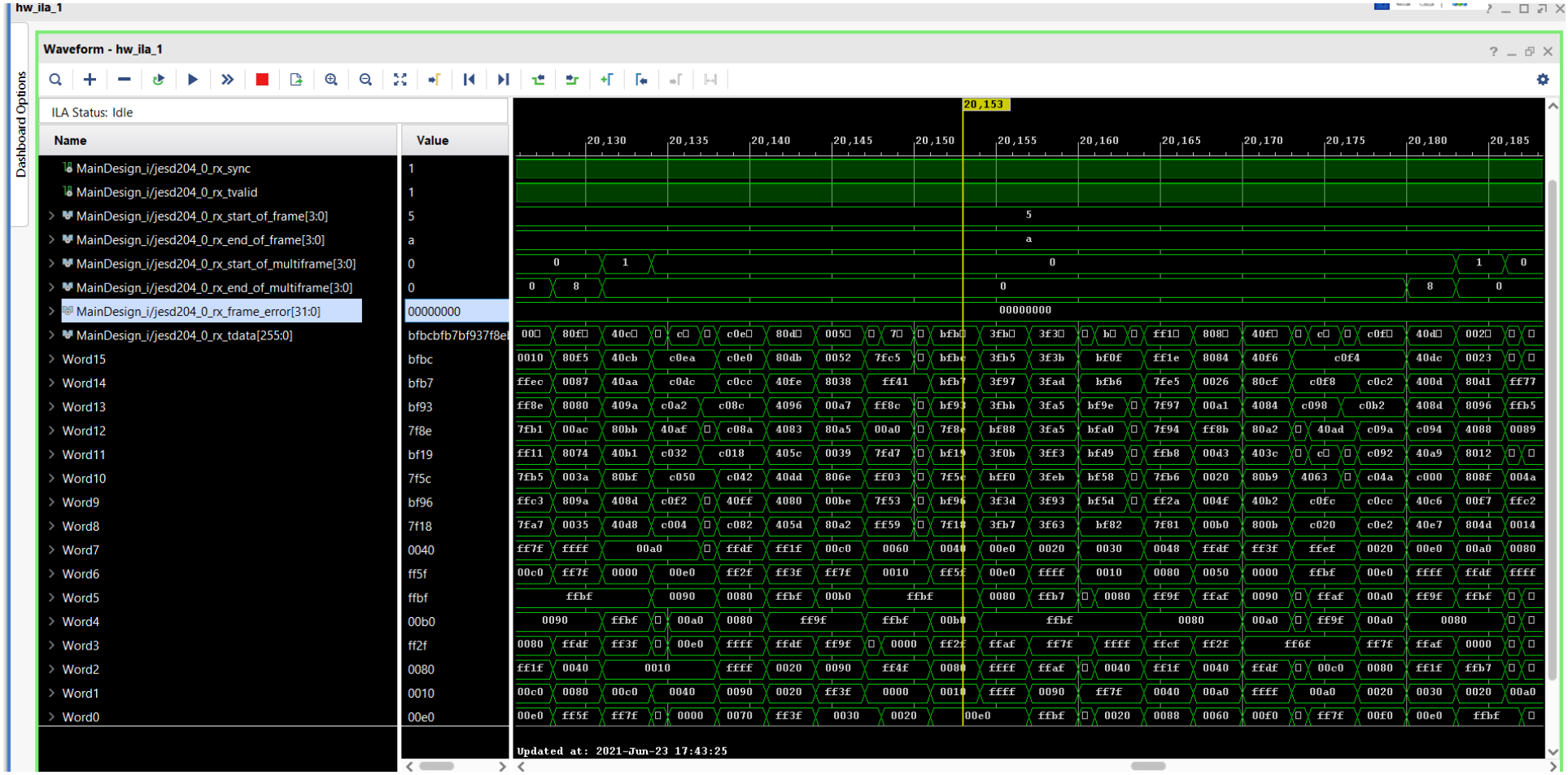
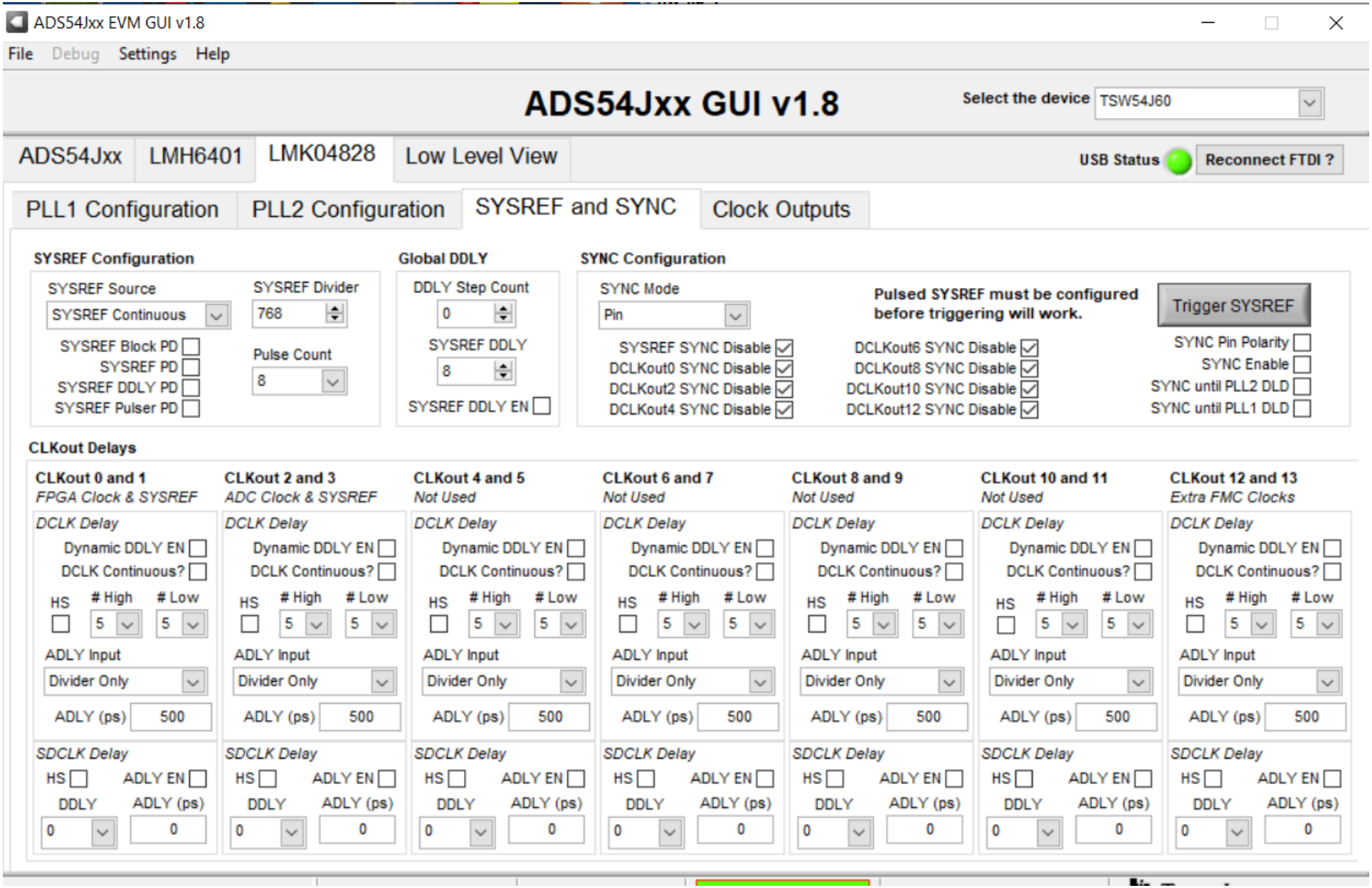
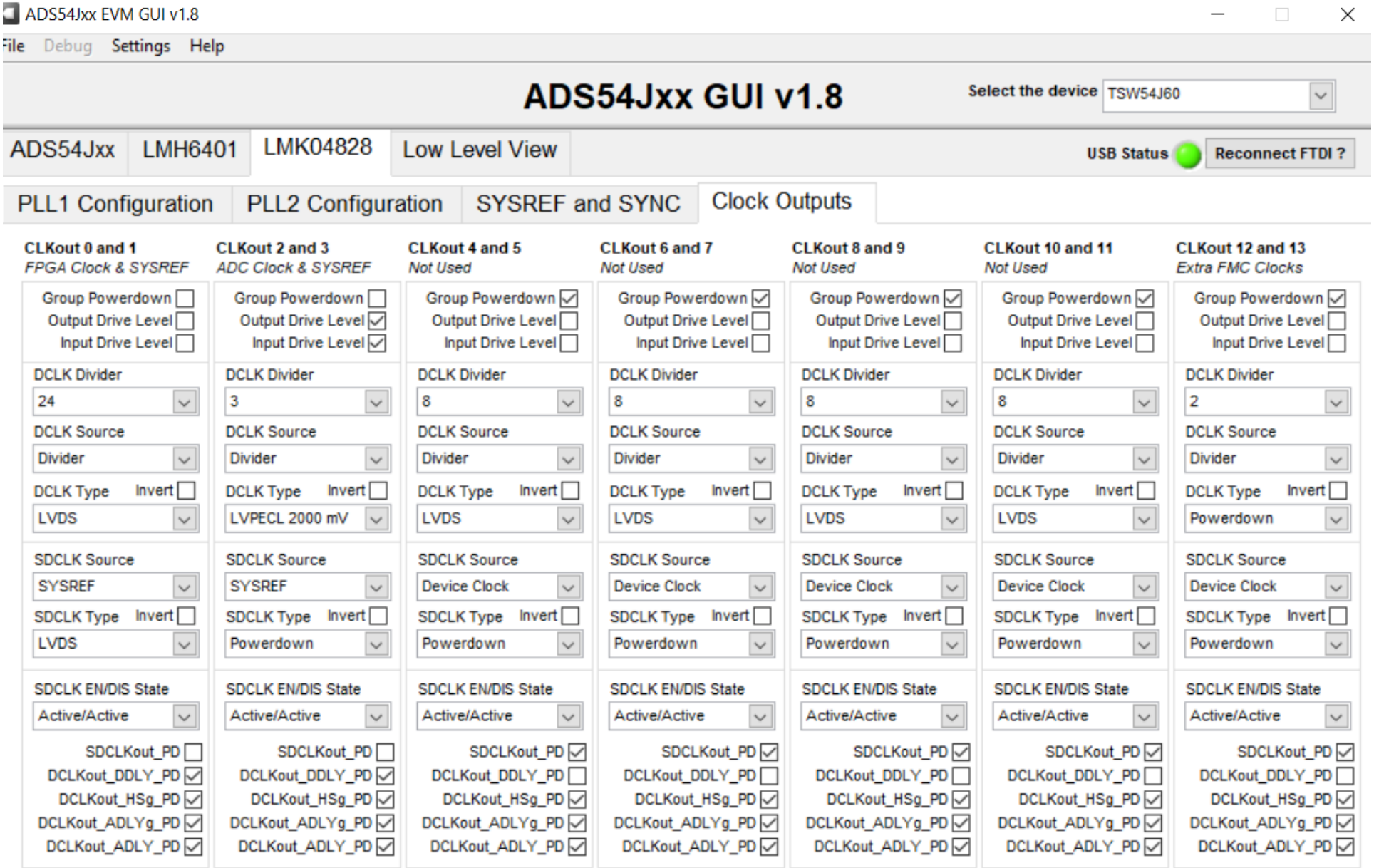
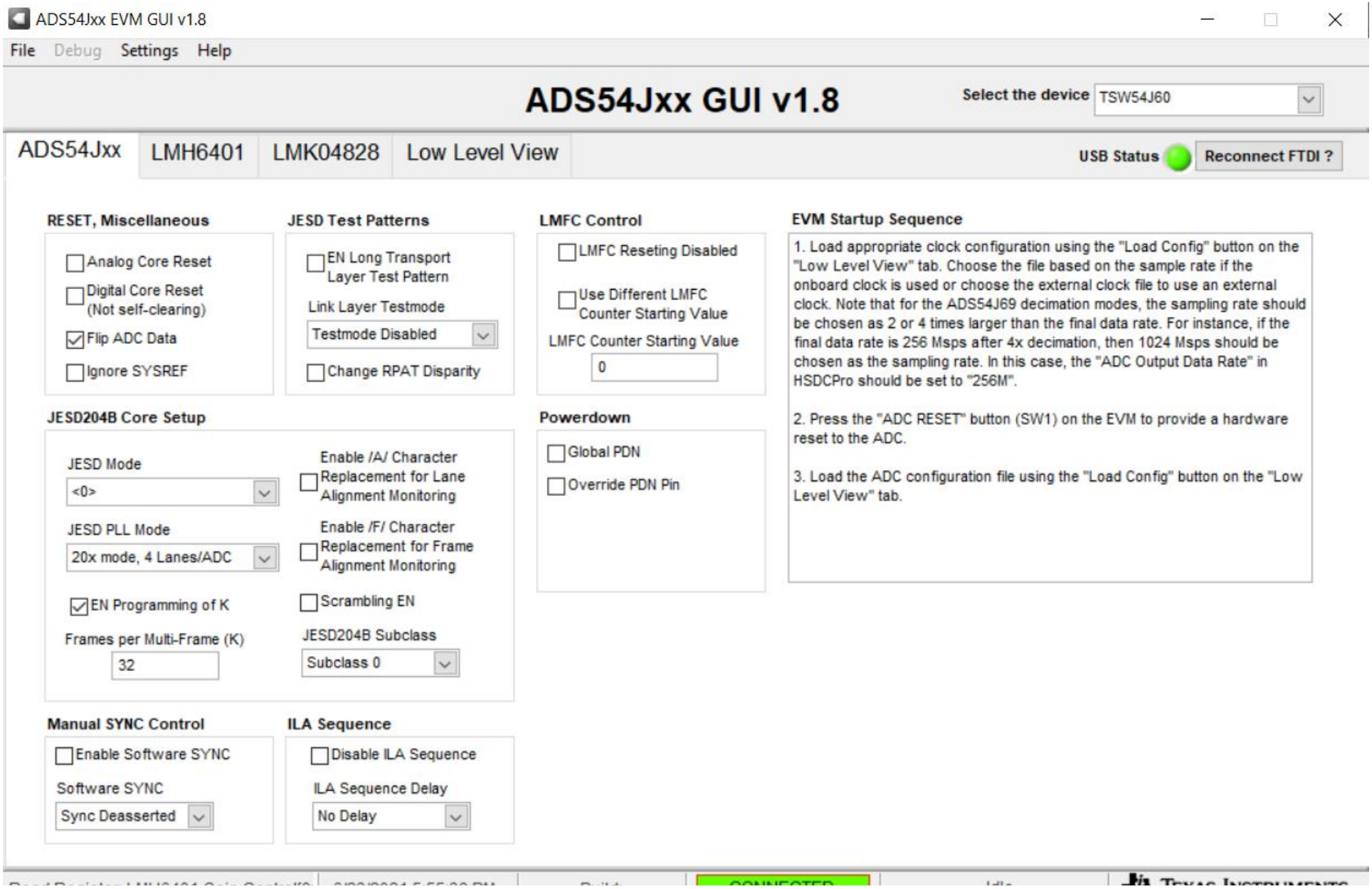
1. ILA data capture



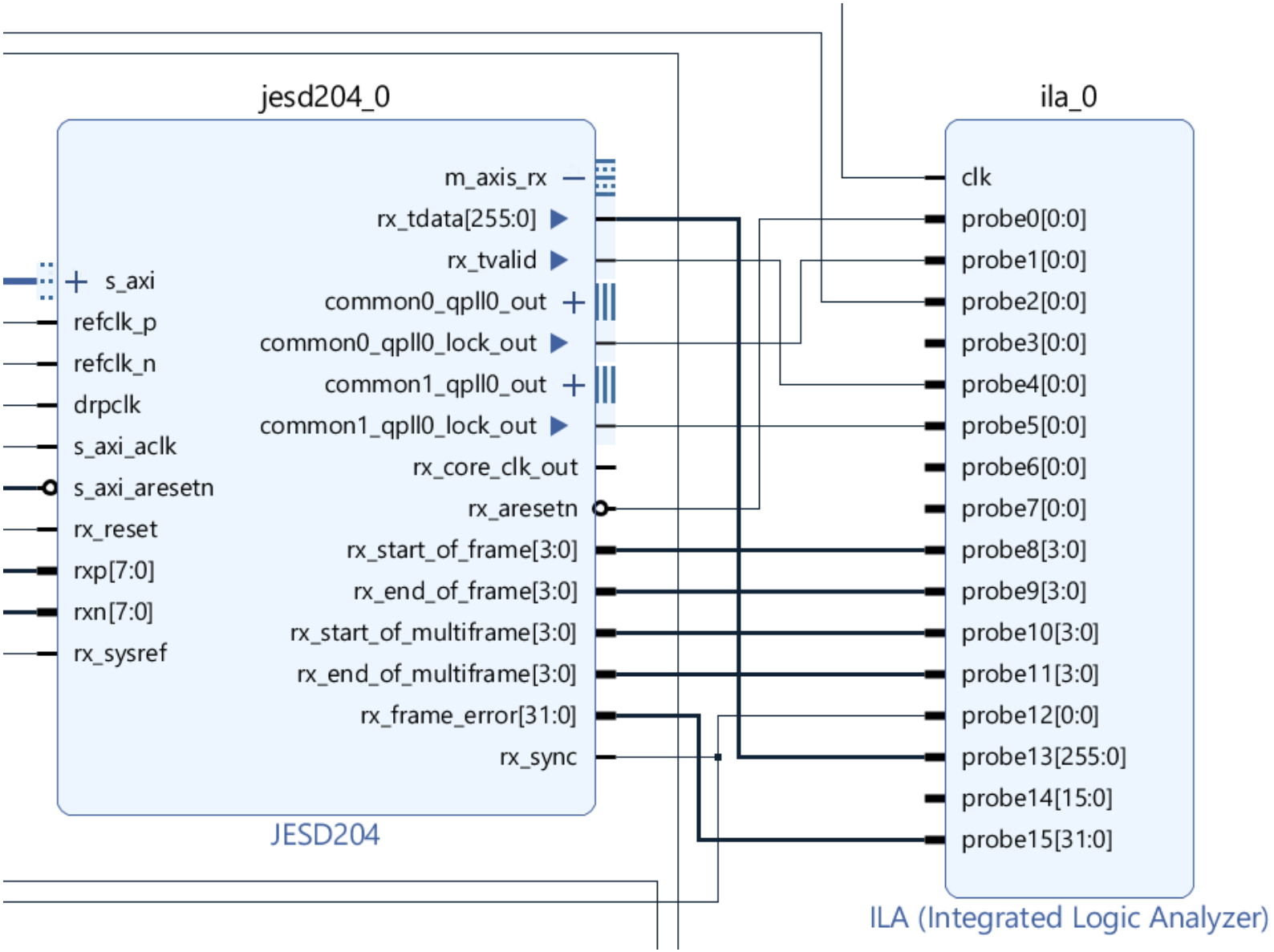
2. ADC and PLL settings

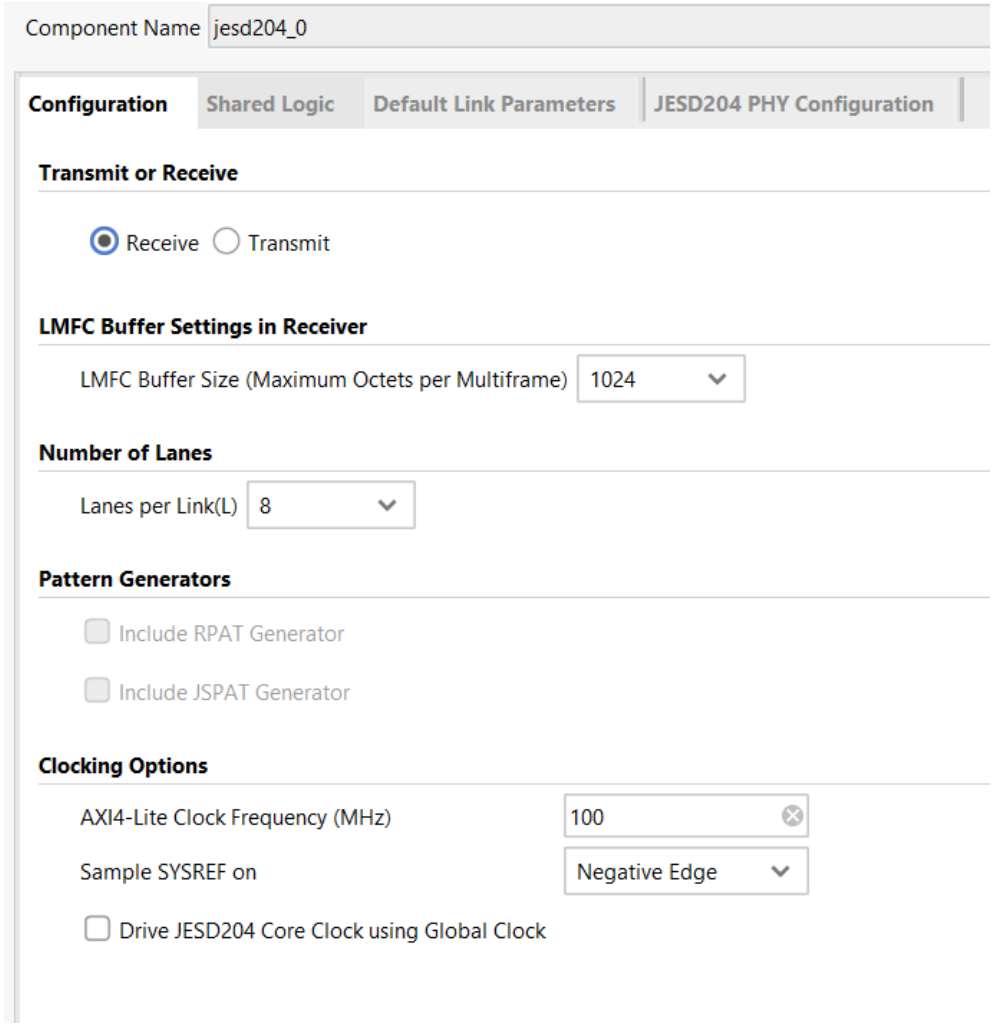


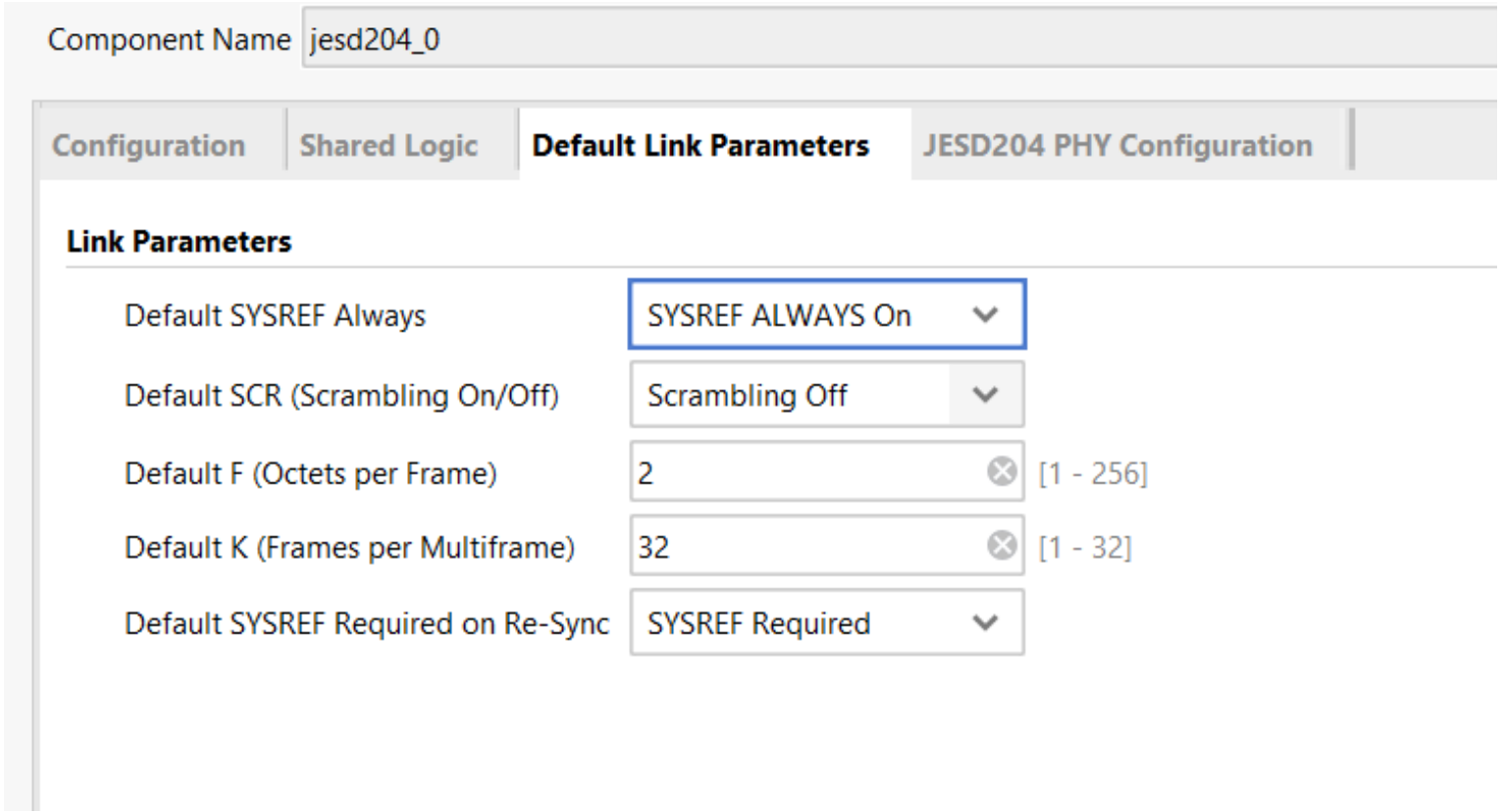

ADS54Jxx EVM GUI v1.8
File Debug Settings Help
ADS54Jxx GUI v1.8
Select the device TSW54J60
ADS54Jxx LMH6401 LMK04828 Low Level View
USB Status Reconnect FTDI ?
PLL1 Configuration PLL2 Configuration SYSREF and SYNC Clock Outputs
CLKout 0 and 1
FPGA Clock & SYSREF
CLKout 2 and 3
ADC Clock & SYSREF
CLKout 4 and 5
Not Used
CLKout 6 and 7
Not Used
CLKout 8 and 9
Not Used
CLKout 10 and 11
Not Used
CLKout 12 and 13
Extra FMC Clocks
Group Powerdown
Output Drive Level
Input Drive Level
DCLK Divider
24
3
8
8
8
8
2
DCLK Source
Divider
DCLK Type
Invert
LVDS
LVPECL 2000 mV
LVDS
LVDS
LVDS
LVDS
Powerdown
SDCLK Source
SYSREF
SYSREF
Device Clock
Device Clock
Device Clock
Device Clock
Device Clock
SDCLK Type
Invert
LVDS
Powerdown
Powerdown
Powerdown
Powerdown
Powerdown
Powerdown
SDCLK EN/DIS State
Active/Active
SDCLKout_PD
DCLKout_DDLY_PD
DCLKout_HSg_PD
DCLKout_ADLYg_PD
DCLKout_ADLY_PD

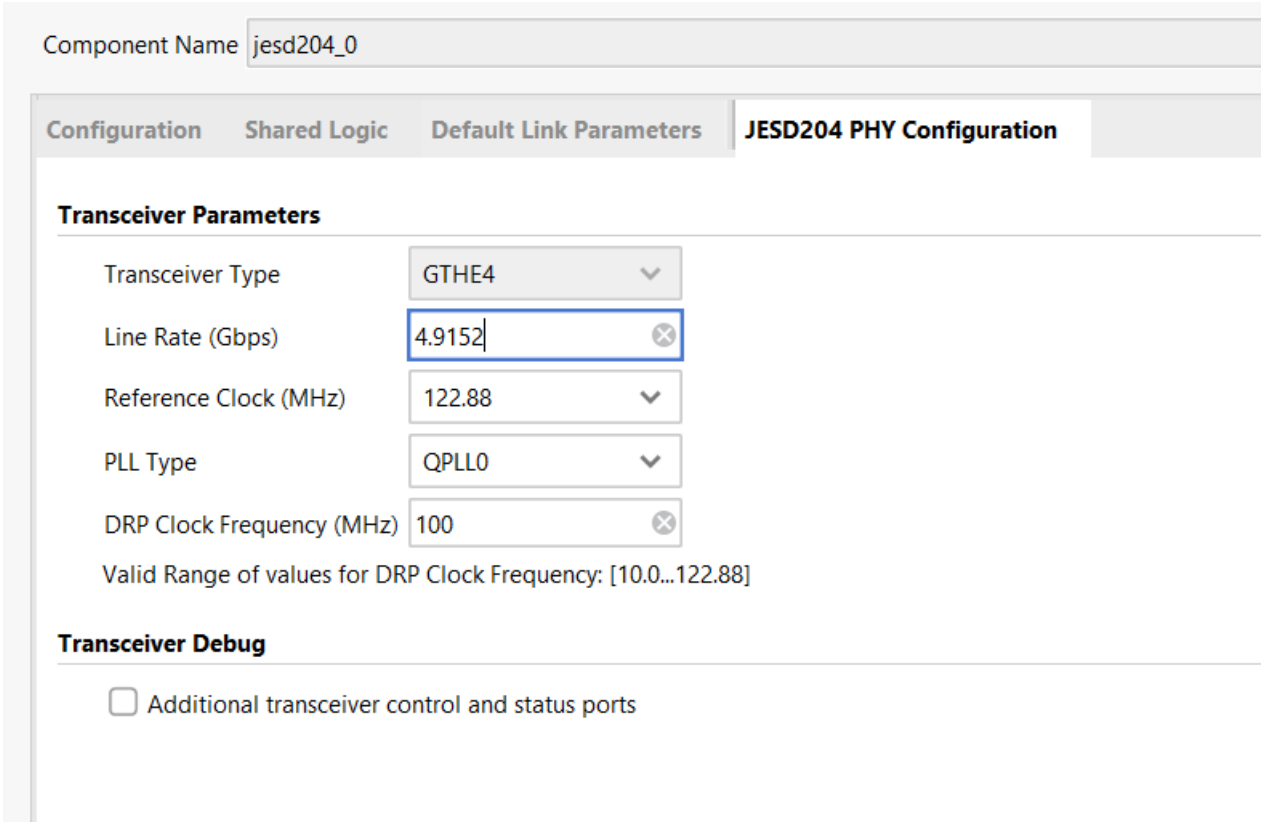

ADS54Jxx EVM GUI v1.8
File
Debug
Settings
Help
ADS54Jxx GUI v1.8
Select the device
TSW54J60
ADS54Jxx
LMH6401
LMK04828
Low Level View
USB Status
Reconnect FTDI ?
RESET, Miscellaneous
Analog Core Reset
Digital Core Reset (Not self-clearing)
Flip ADC Data
Ignore SYSREF
JESD Test Patterns
EN Long Transport Layer Test Pattern
Link Layer Testmode
Testmode Disabled
Change RPAT Disparity
LMFC Control
LMFC Reseting Disabled
Use Different LMFC Counter Starting Value
LMFC Counter Starting Value
0
EVM Startup Sequence
1. Load appropriate clock configuration using the "Load Config" button on the "Low Level View" tab. Choose the file based on the sample rate if the onboard clock is used or choose the external clock file to use an external clock. Note that for the ADS54J69 decimation modes, the sampling rate should be chosen as 2 or 4 times larger than the final data rate. For instance, if the final data rate is 256 Msps after 4x decimation, then 1024 Msps should be chosen as the sampling rate. In this case, the "ADC Output Data Rate" in HSDCPro should be set to "256M".
2. Press the "ADC RESET" button (SW1) on the EVM to provide a hardware reset to the ADC.
3. Load the ADC configuration file using the "Load Config" button on the "Low Level View" tab.
JESD204B Core Setup
JESD Mode
<0>
JESD PLL Mode
20x mode, 4 Lanes/ADC
EN Programming of K
Frames per Multi-Frame (K)
32
Enable /A/ Character Replacement for Lane Alignment Monitoring
Enable /F/ Character Replacement for Frame Alignment Monitoring
Scrambling EN
JESD204B Subclass
Subclass 0
Powerdown
Global PDN
Override PDN Pin
Manual SYNC Control
Enable Software SYNC
Software SYNC
Sync Deasserted
ILA Sequence
Disable ILA Sequence
ILA Sequence Delay
No Delay

3. JESD204 core and its setting on the FPGA




Component Name
jesd204_0
Configuration
Shared Logic
Default Link Parameters
JESD204 PHY Configuration
Transmit or Receive
Receive
Transmit
LMFC Buffer Settings in Receiver
LMFC Buffer Size (Maximum Octets per Multiframe)
1024
Number of Lanes
Lanes per Link(L)
8
Pattern Generators
Include RPAT Generator
Include JSPAT Generator
Clocking Options
AXI4-Lite Clock Frequency (MHz)
100
Sample SYSREF on
Negative Edge
Drive JESD204 Core Clock using Global Clock


Component Name
jesd204_0
Configuration
Shared Logic
Default Link Parameters
JESD204 PHY Configuration
Link Parameters
Default SYSREF Always
SYSREF ALWAYS On
Default SCR (Scrambling On/Off)
Scrambling Off
Default F (Octets per Frame)
2
[1 - 256]
Default K (Frames per Multiframe)
32
[1 - 32]
Default SYSREF Required on Re-Sync
SYSREF Required


Component Name
jesd204_0
Configuration
Shared Logic
Default Link Parameters
JESD204 PHY Configuration
Transceiver Parameters
Transceiver Type
GTHE4
Line Rate (Gbps)
4.9152
Reference Clock (MHz)
122.88
PLL Type
QPLL0
DRP Clock Frequency (MHz)
100
Valid Range of values for DRP Clock Frequency: [10.0...122.88]
Transceiver Debug
Additional transceiver control and status ports