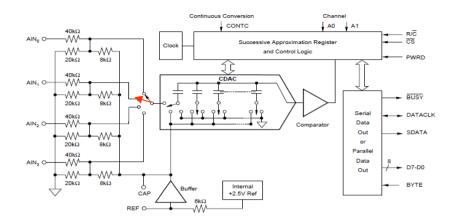


Test Result, Here is 1.79V to 62mV in case (E) Continuous Conversion Channel CONTC A0 | A1 40kΩ R/C AIN_n O-CS Successive Approximation Register Clock and Control Logic PWRD 20kΩ 8kΩ CDAC Q3) After the BUSY go up and R/C goes 20kΩ high to low (★), customer changes Serial AIN, O-Data Comparato Ain0 to Ain1.....In this time, Out $20k\Omega$ 8kΩ how is the state of previous channel(Ain0)? Parallel SW₁ SW1 Just Oepn? (If so, it should be 1.79V), but Out Test result is 62mV. 20kΩ 8kΩ CAP +2.5V Ref REF O D) Do you have any criteria (max limit) for tX? Even though t1 is within spec(max 12us), tX it may be long in the customer's case R/C Conversion Currently in Progress: BUSY n + 1 n + 2 n + 3 Channel Address for Conversion: A0, A1 n + 3n + 5n + 1 n + 2 n + 4(Input) Results from Conversion: D7-D0 n + 2 n-3n-2n-1n + 3n + 4 n n + 1

FIGURE 8. Channel Addressing in Normal Conversion Mode (CONTC and CS LOW).



Problem:

After conversion of Ain1, and then there are delay to next Ain2 channel conversion due to MCU setting. (i.e. next R/C rise/fall is delay)

