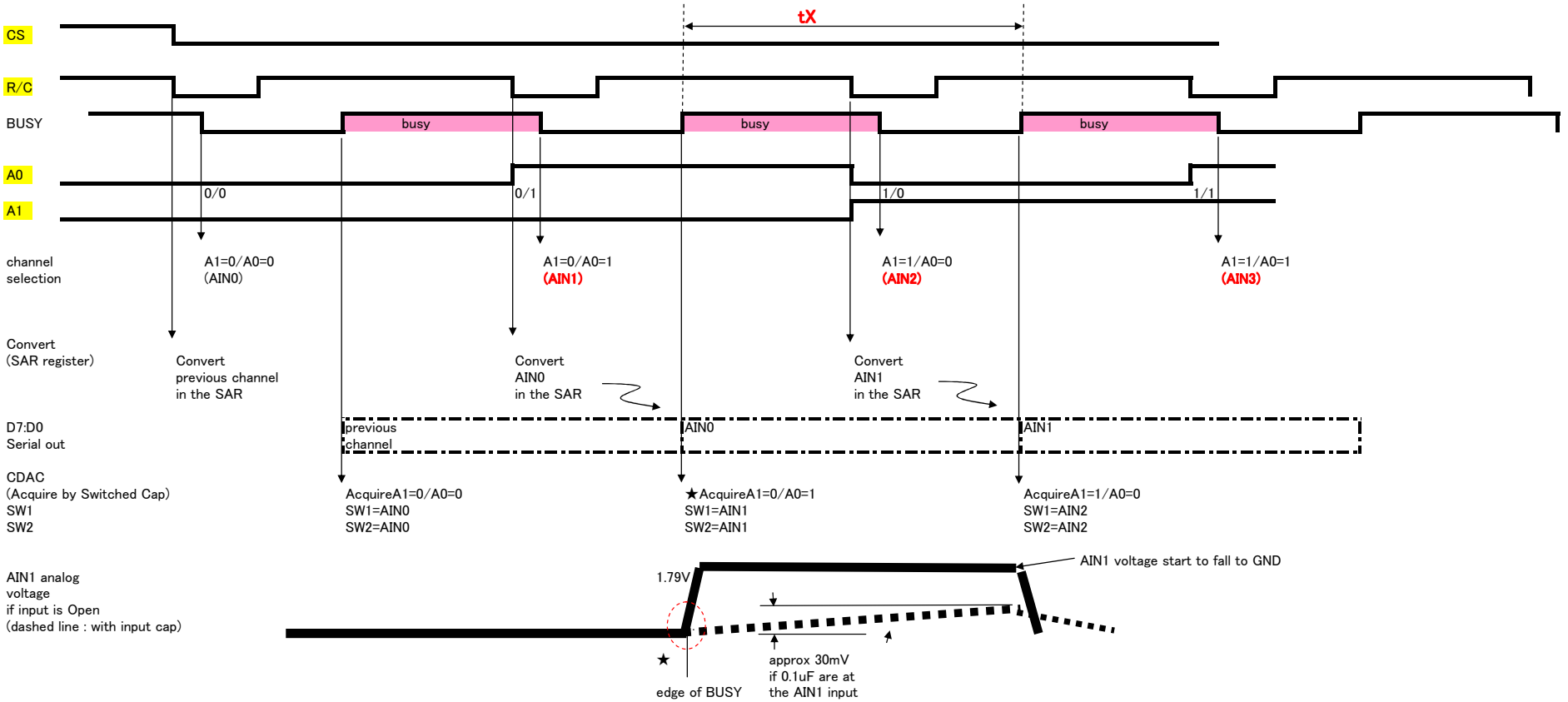
Jan22 2015/ K Shibatani



Question1

Is the timing diagram above correct? (Thank you for your answer to seishin)

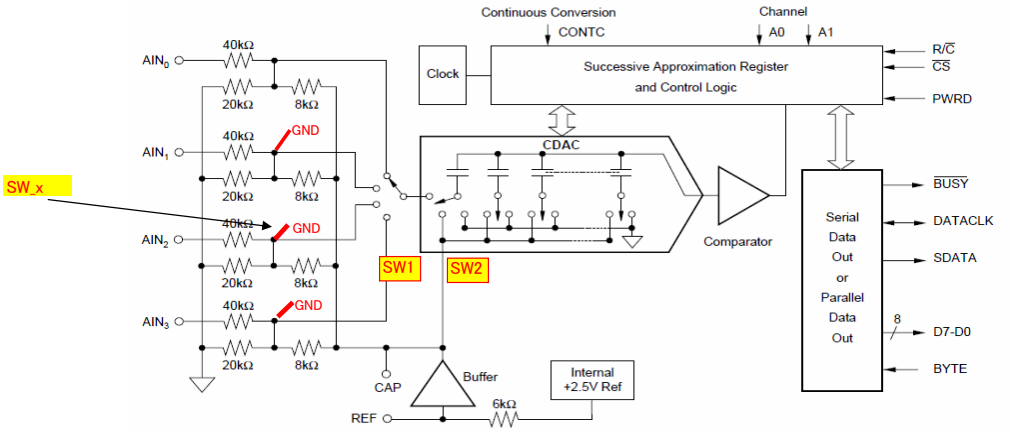
Question2

My understanding is CDAC acquire the analog voltage of AIN1 when SW1=SW2=AIN1.
In this time, customer's concern is voltage rise depend on input cap..
Does ADS7825 acquire the voltage just at the edge of BUSY goes UP? (No concern about the A/D conversion result even though we can see the rise of analog voltage…Is it correct?)

Qestion3

From Customer's test result, AIN1 analog voltage start to fall to 62mV (seishin's thread) when they had selct AIN2.
In this time, SW1/SW2 swtitches from AIN1 to AIN2…. Here is the question,,
Don't you have any additional switch (SW_x) who discharges the parastinc cap to ground in front of the SW1 ,, do you ?

Question4 If the mechanism above were corret, analog voltage on AIN_x pin goes up unless there are big (uF order) cap, Or, Opeamp which has sink current ability and also the time Tx (above) is short… how do you think ?


Continuous Conversion
CONTC
Channel
A0
A1
Clock
Successive Approximation Register
and Control Logic
R/C
CS
PWRD
CDAC
Comparator
BUSY
DATACLK
SDATA
Serial
Data
Out
or
Parallel
Data
Out
8
D7-D0
BYTE
AIN0
AIN1
AIN2
AIN3
40kΩ
20kΩ
8kΩ
GND
SW_x
SW1
SW2
CAP
REF
Buffer
6kΩ
Internal
+2.5V Ref