 **TEXAS INSTRUMENTS**

Title

SCH, TSW1418EVM

Size

B

Document Number

DC0??

Rev

E2

Date:

Thursday, July 12, 2018

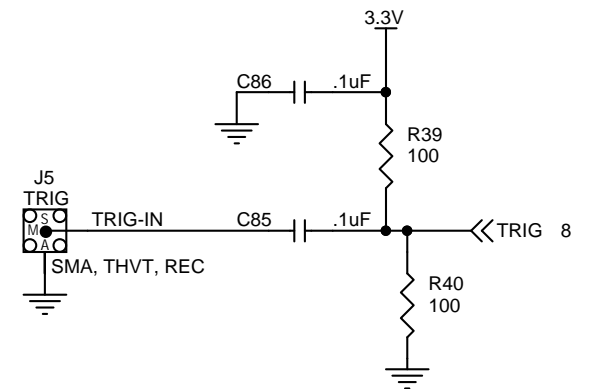
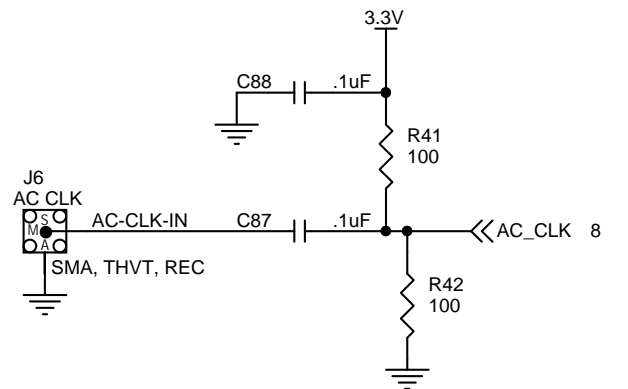
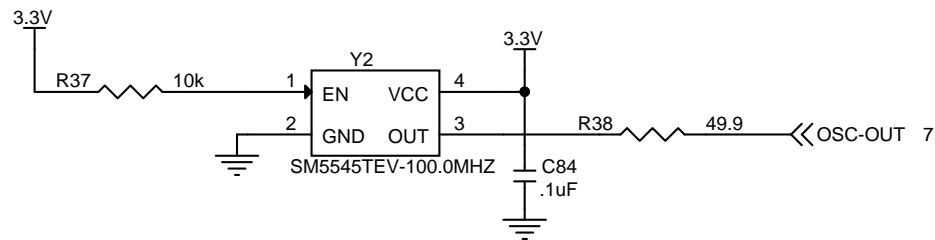
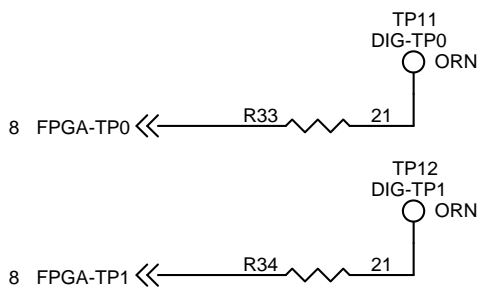
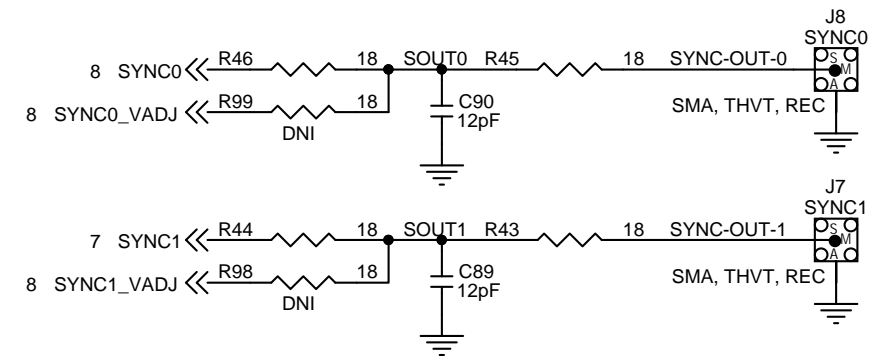
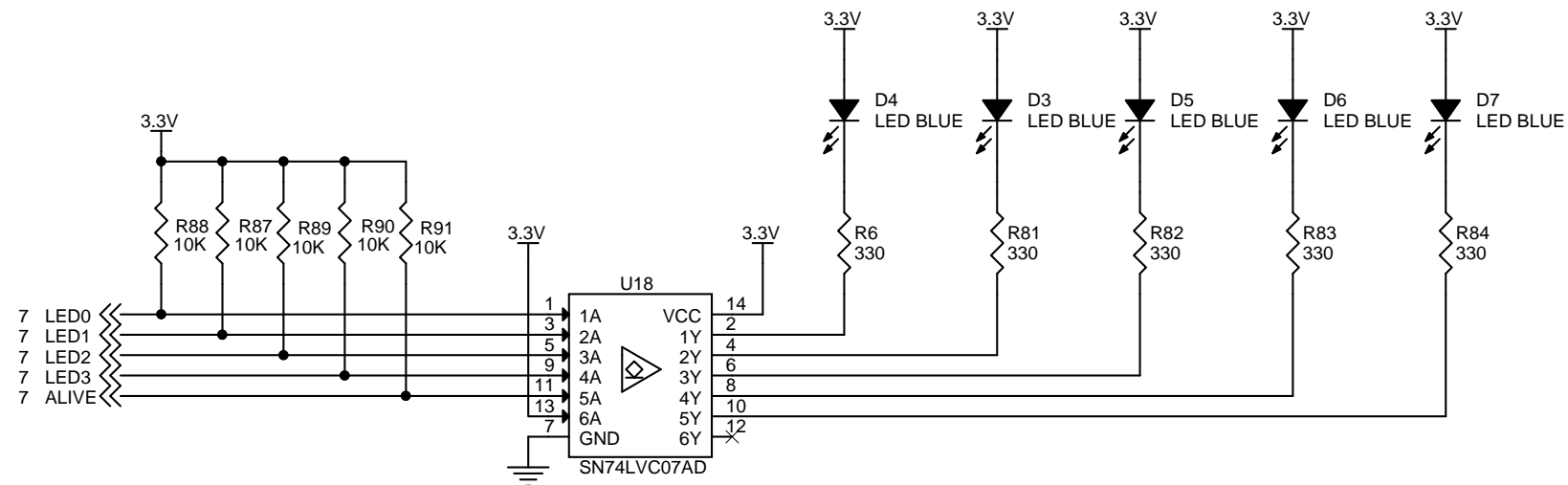
Sheet

1

of

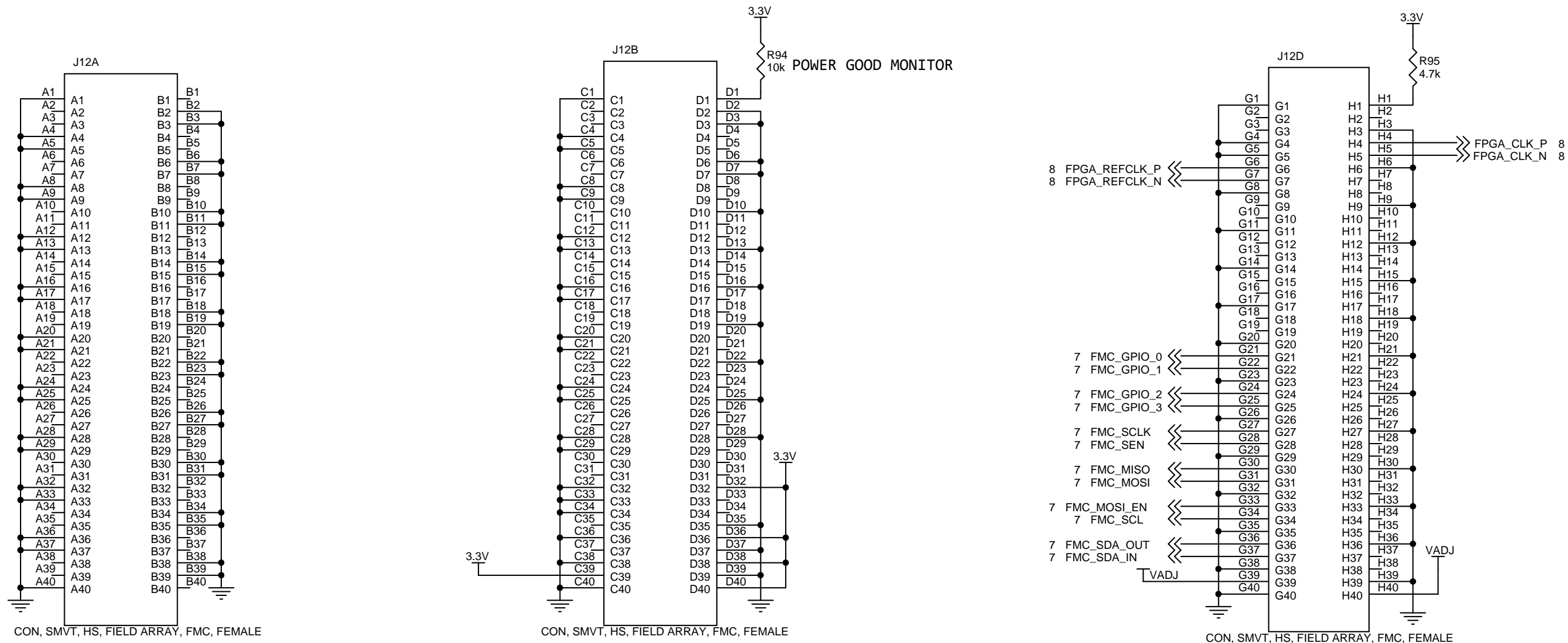
11

Drawn:	JV SMITH	02/2018
Engineer:	B. KINCAID	02/2018



5 BS_ENA << R92 0 >> JTAG_BS_EN 5
CLOSED = USE FTDI
OPEN = USE EXT JTAG

ADC Interface



3.3V available on FMC

VADJ available on FMC

All routed I/O is based on VADJ

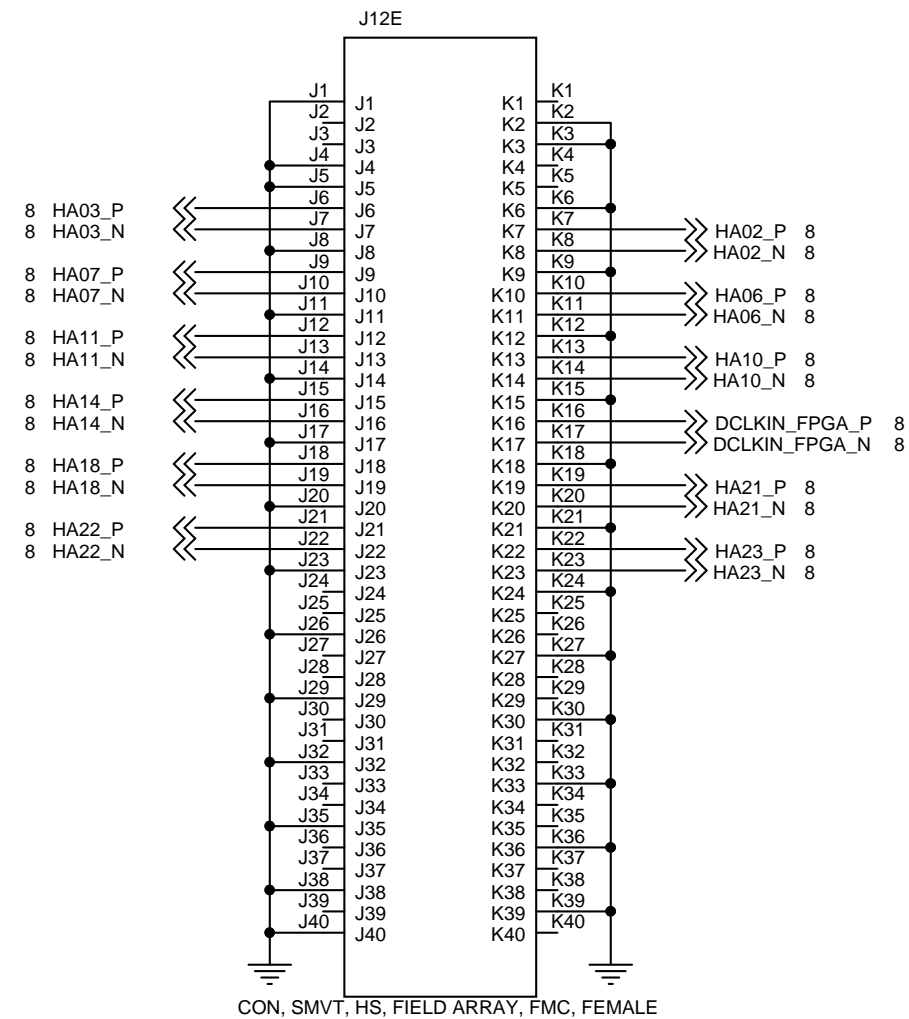
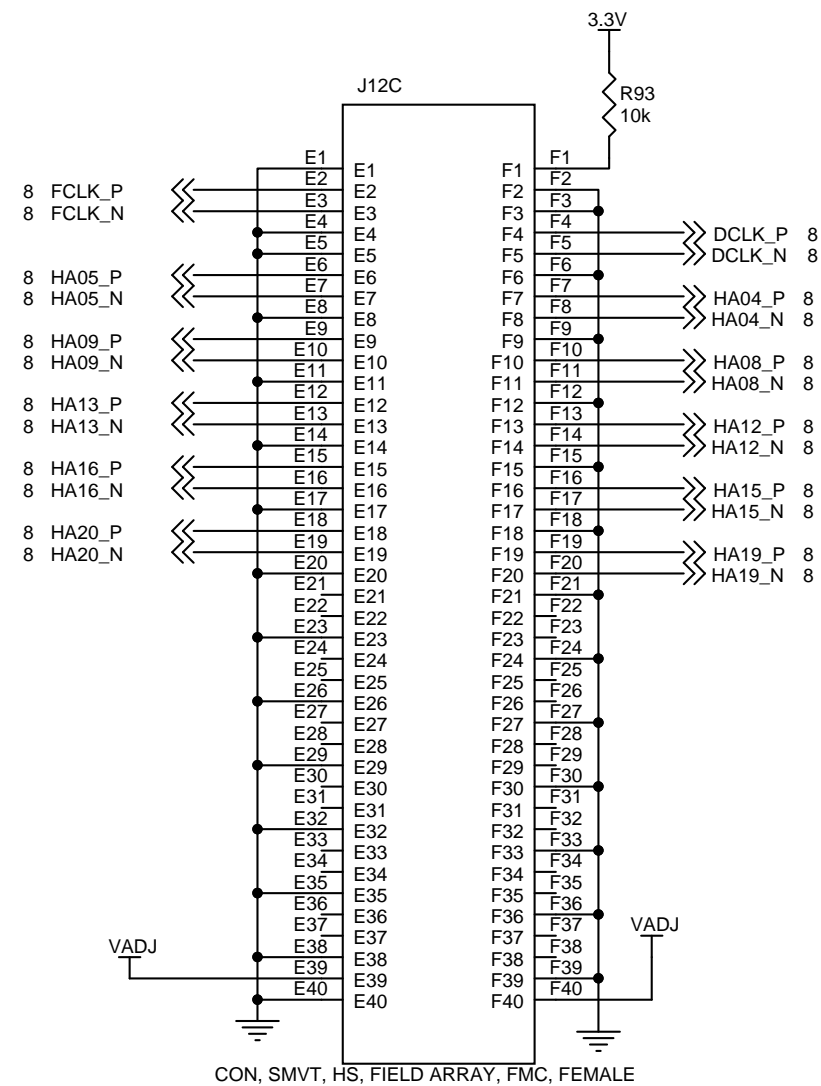
12V not available on FMC

Mates to male bottom side FMC on the ADC35* EVMs.



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ADC Interface

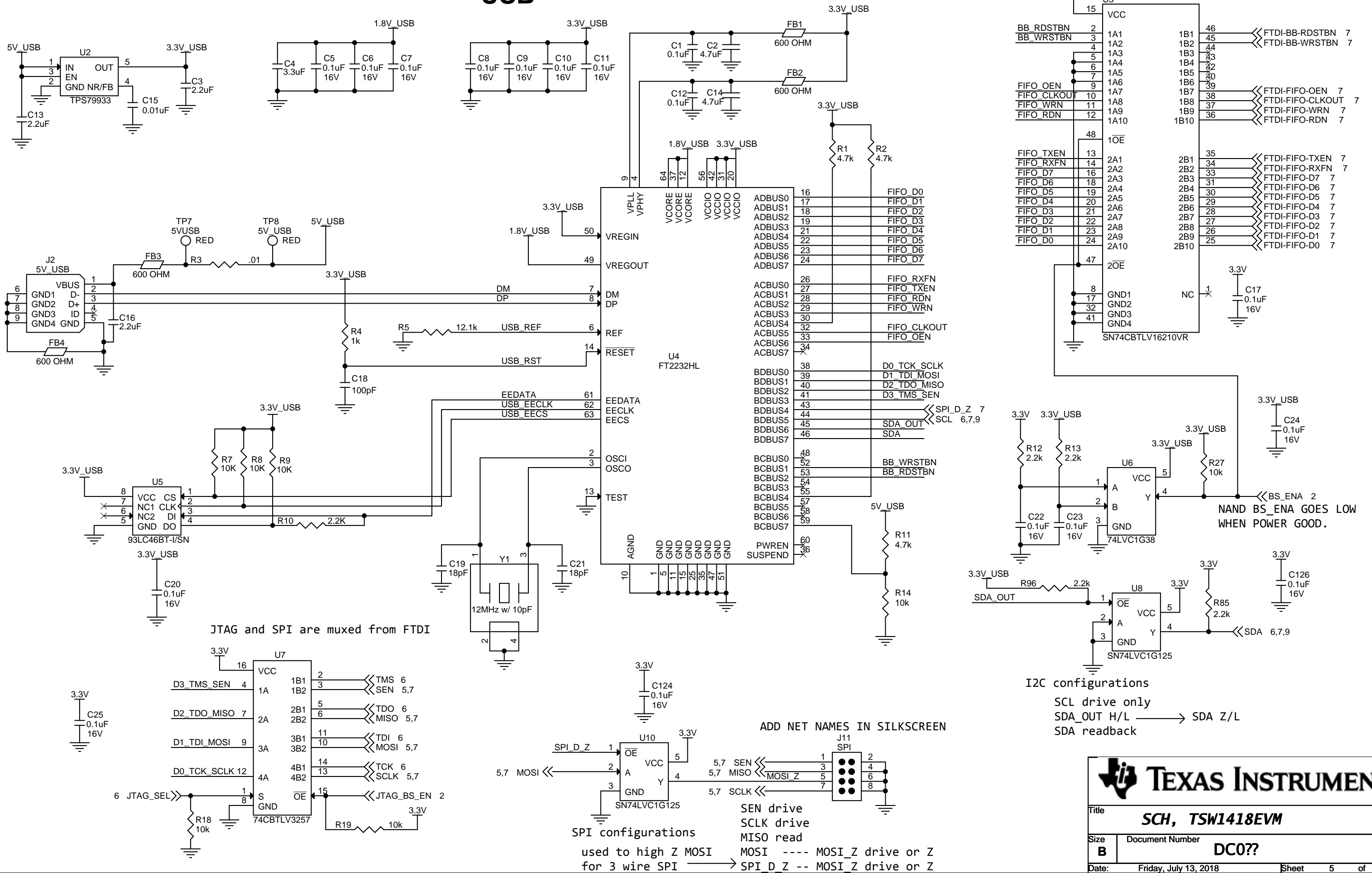


Mates to male bottom side FMC on the ADC35* EVMs.

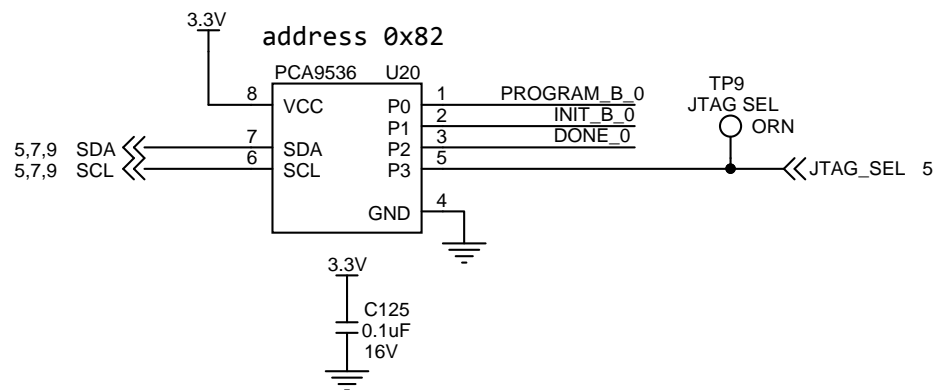
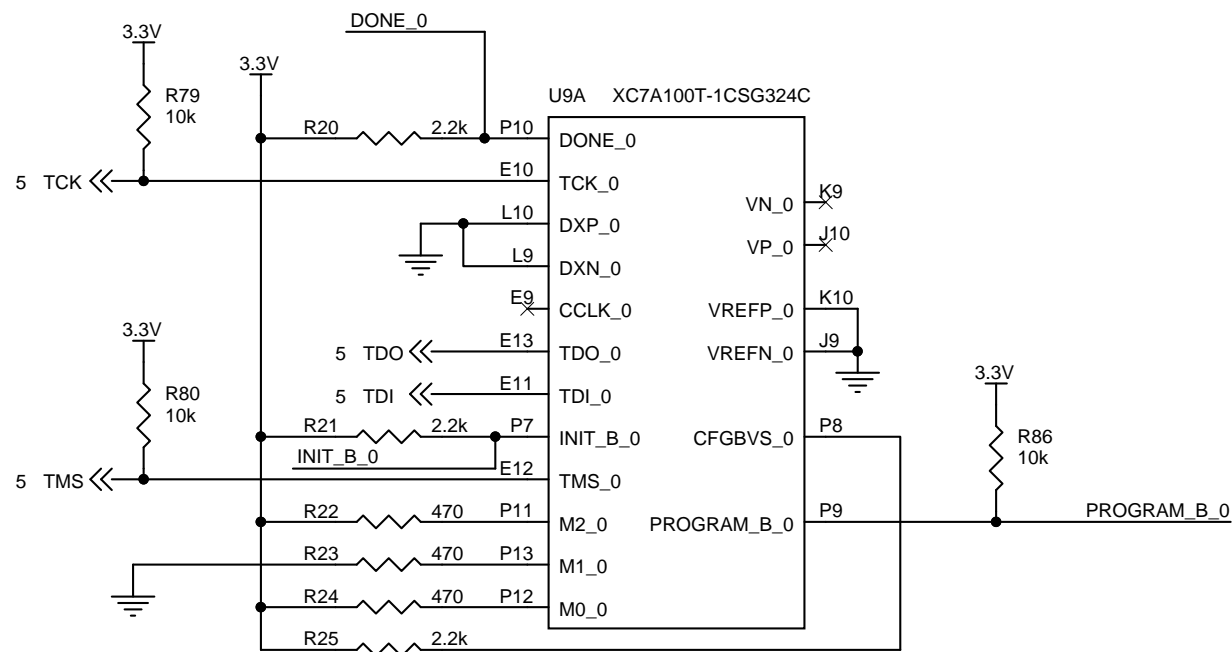
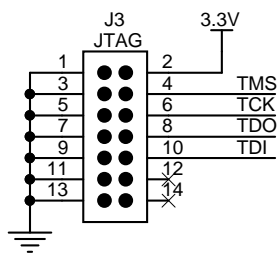


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USB



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FPGA JTAG CONFIG

CFGBVS= 1(VCC_0=3.3V)

M[2:0]= 101

TCK, TMS, TDI, TDO = from FTDI device through MUX

PROGRAM_B=I2C expander P0, write, pulse low to enable configuration mode

INIT_B= I2C expander P1, read only

DONE= I2C expander P2, read only

CCLK= no connect

PUDC_B= 3.3V

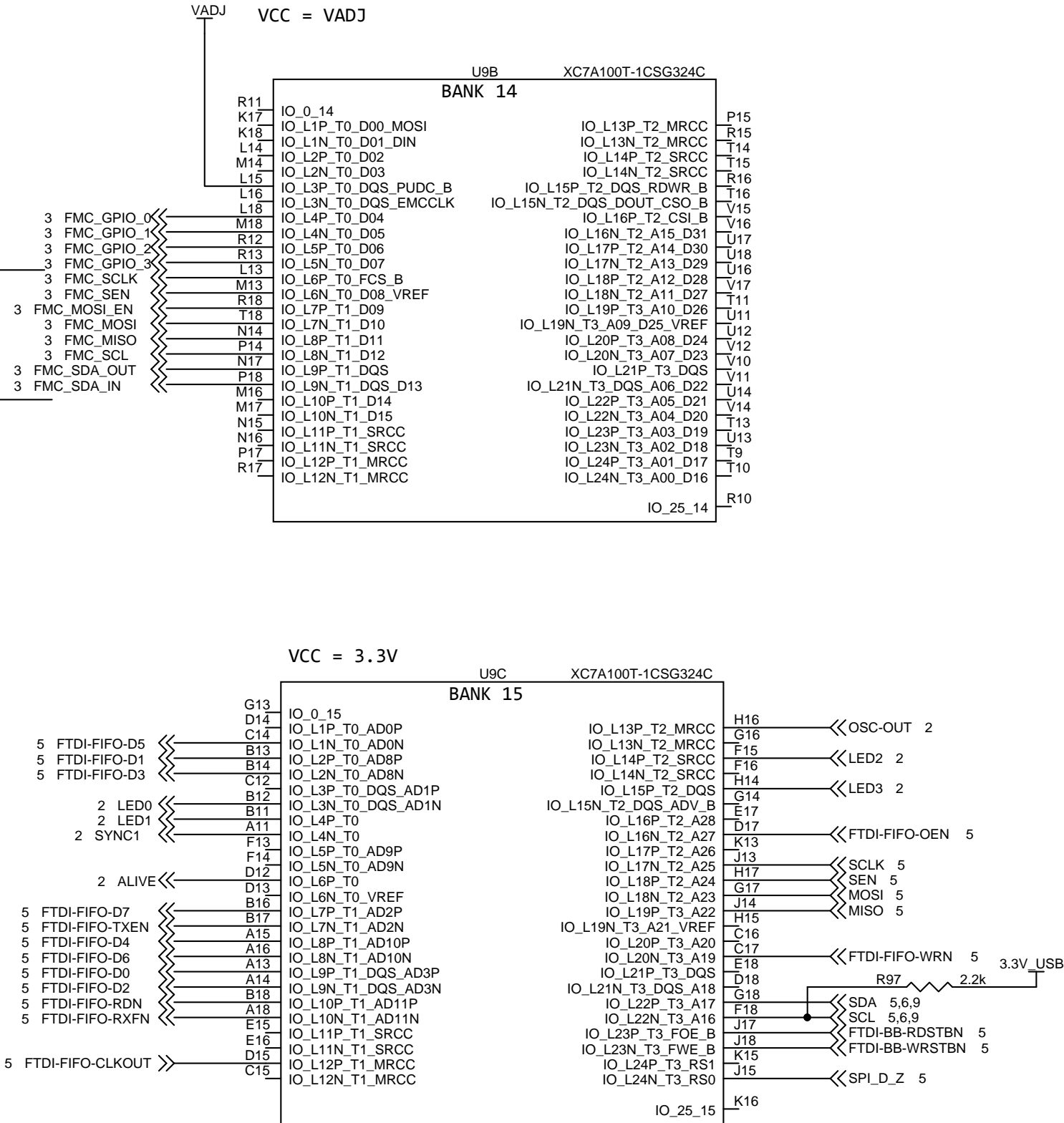
PCA9536 address 0x82

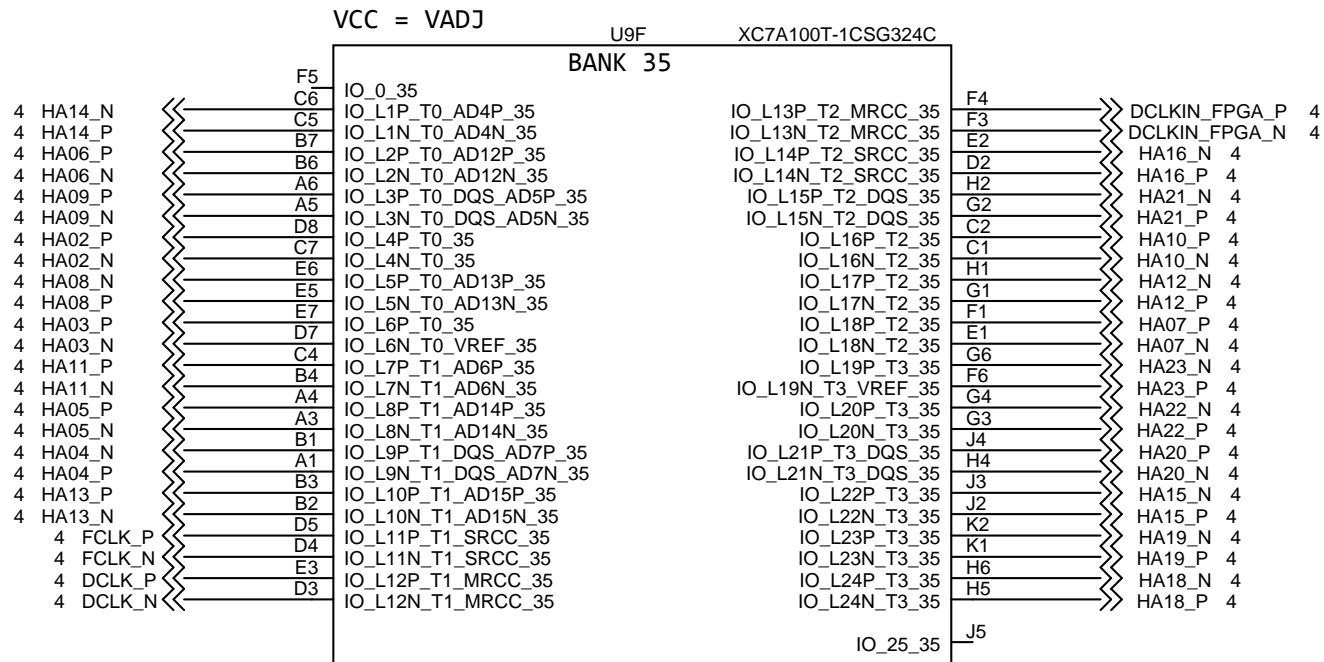
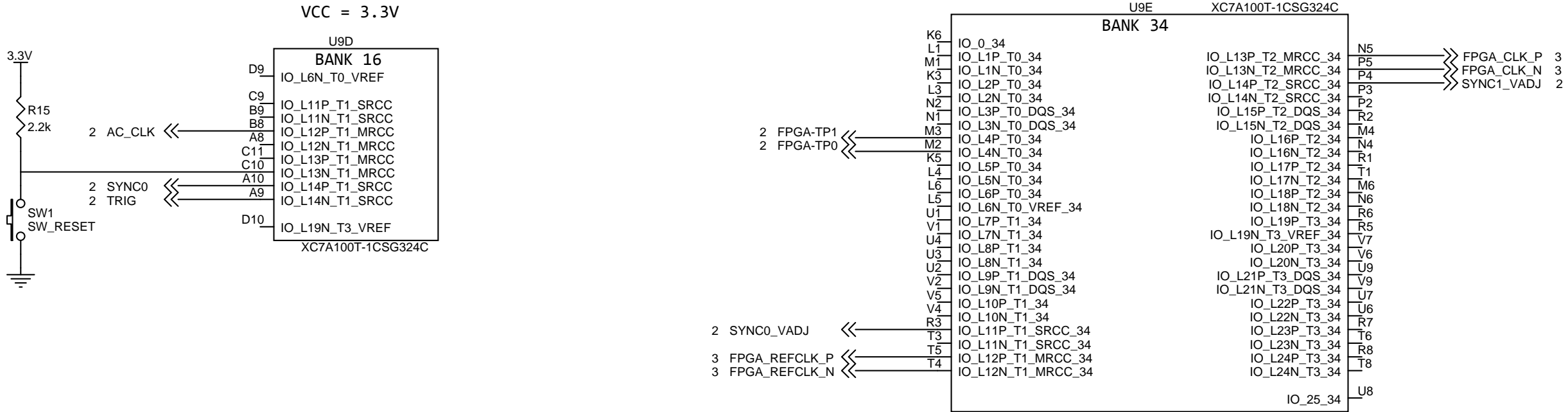
- All pins input at power up
- Configure 0x03 F6 (wrrw) at startup
- Read 0x00 [JTAG_SEL DONE INIT_B PROGRAM_B]
- Write 0X01 [JTAG_SEL X X PROGRAM_B]



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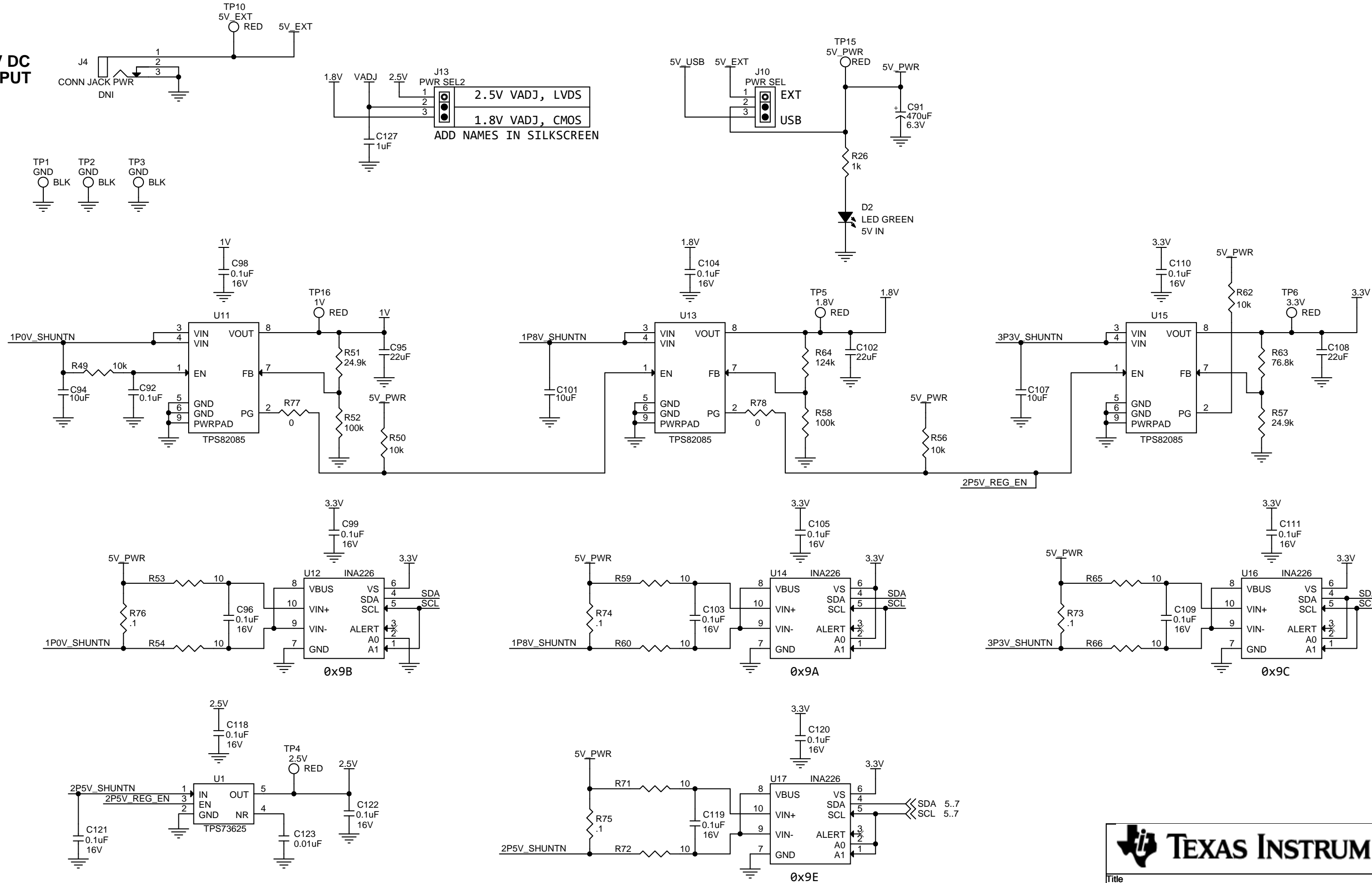
These signals are
wired through FPGA
to FMC

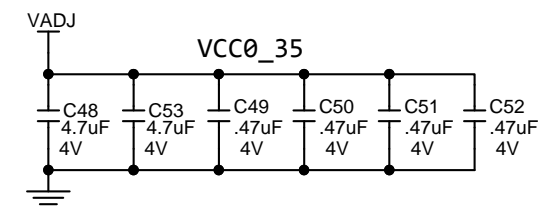
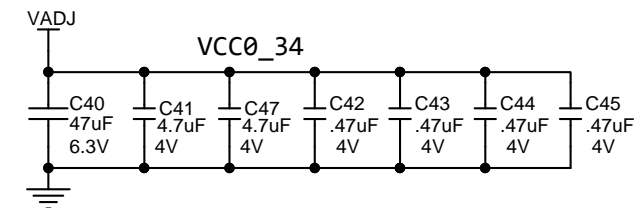
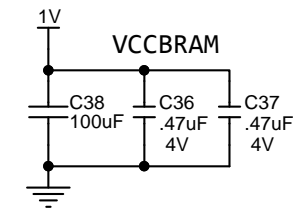
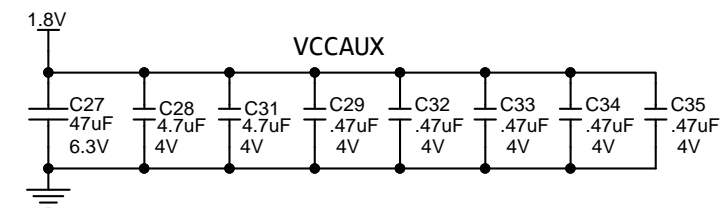
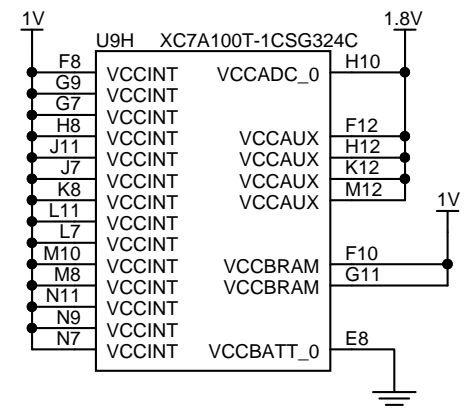
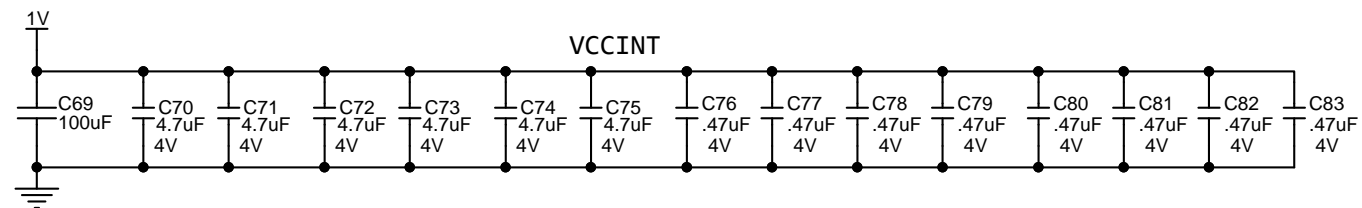
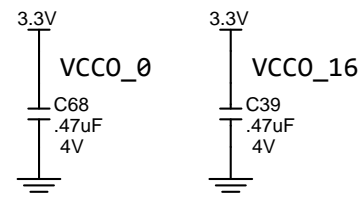
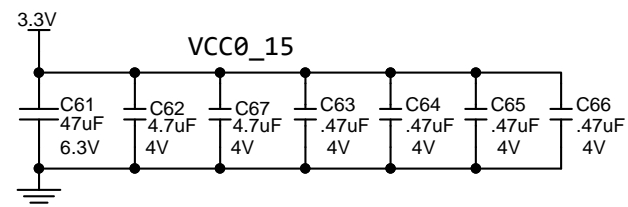
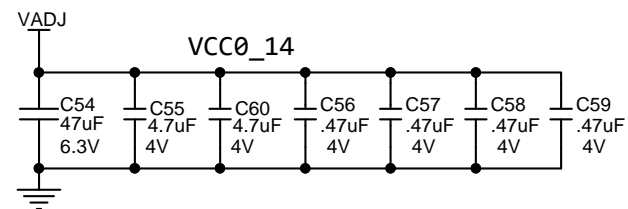
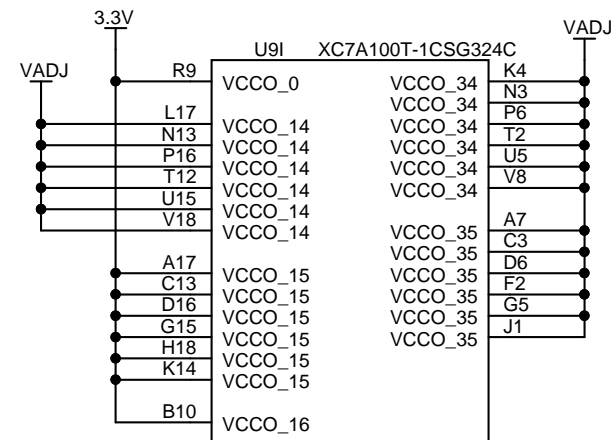
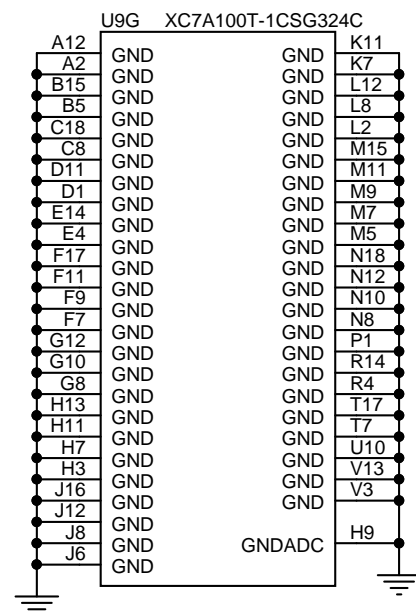




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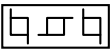
5V DC INPUT





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MECHANICAL PARTS



BARE BOARD, TSW1418

MT1



STANDOFF, FEMALE, 4-40 X 1 3/16"

MT2



STANDOFF, FEMALE, 4-40 X 1 3/16"

MT3



STANDOFF, FEMALE, 4-40 X 1 3/16"

MT4



STANDOFF, FEMALE, 4-40 X 1 3/16"



SCREW PANHEAD 4-40 x 3/8"




SCREW PANHEAD 4-40 x 3/8"



SCREW PANHEAD 4-40 x 3/8"



SCREW PANHEAD 4-40 x 3/8"

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