

Texas Instruments Application Report

DAC348x PCB Layout Guidelines for the Multi-Row QFN package

Russell Hoppenstein

Revision 1.0

Abstract

This document provides additional information related to the multi-row QFN package of the DAC3482 and DAC3484 for assistance in PCB layout of the device. This document is intended to augment and modify the standard mechanical information that is provided in the datasheet to provide a more robust design. The document will illustrate the recommended land pattern for the device and will provide recommendations for routing connections to additional circuitry and power supply planes.

Introduction

The DAC348x device employs a multi-row QFN package (mr-QFN). The mr-QFN package is a relatively new package style that is similar to a standard QFN package except that there is an additional inner row of pins. This approach allows for additional pin connections in an inexpensive package without having to resort to a much larger QFN package or a BGA package. Though the package is new and unfamiliar, utilizing the guidelines outlined in this report in conjunction with the standard mechanical information found in the device datasheet will yield a high quality, robust design.

The Problem

Layout and manufacturing with a standard QFN package is well established. With the standard QFN the pins are located on the edge of the device. It is easy to solder to these pins and verify visually a proper connection. The mr-QFN employs pins on an inner row. It is not possible to visually see the connection of those pins. Most of the manufacturing errors stem from insufficient soldering on those pins which results in opens or too much solder which results in shorts.

With a standard QFN, the device can float a little bit on the thermal pad's solder during reflow and still make a good connection to all of the outside row pins. Solder can wick up slightly during reflow to make a solid connection between the board and the device pin. On the mr-QFN package, the device can not withstand to float during the reflow process because the inner row pins will not have an easy path for the solder to make a secure connection from the board to the pin. It becomes important to design the PCB board to ensure the device is pulled in toward the board during reflow instead of allowed to float.

The Modified PCB Land pattern

The standard PCB land pattern per industry standard is shown in Figure 1. Texas Instruments recommends a few adjustments to the standard recommendation to improve board manufacturing. The modified PCB land pattern is shown in Figure 2.

The following list will identify and explain some of the key attributes of the modified land pattern for this device.

- Ground vias in the thermal pad should use a 0.2 mm or 8 mil drill. These vias should not be filled. This via will allow excess solder to weep through the via hole. This will keep the device from floating on the solder during reflow and will assist in wicking the device toward the board to make a solid connection of the thermal pad and all of the pins. A larger drill size will wick away too much solder and a smaller one will not wick away enough.
- Land pattern for the corner connections should be 0.9 mm square. This size is significantly bigger than the size of the corner pins. The extra area is to provide a path for solder to spread during reflow so that the device will not float.

- Solder mask around the pins' pads recommended to be the same size as the pad. This minimizes the chances of solder shorts between the pads and the traces routing between the pads.

RKD (S-MRQFN-N88)

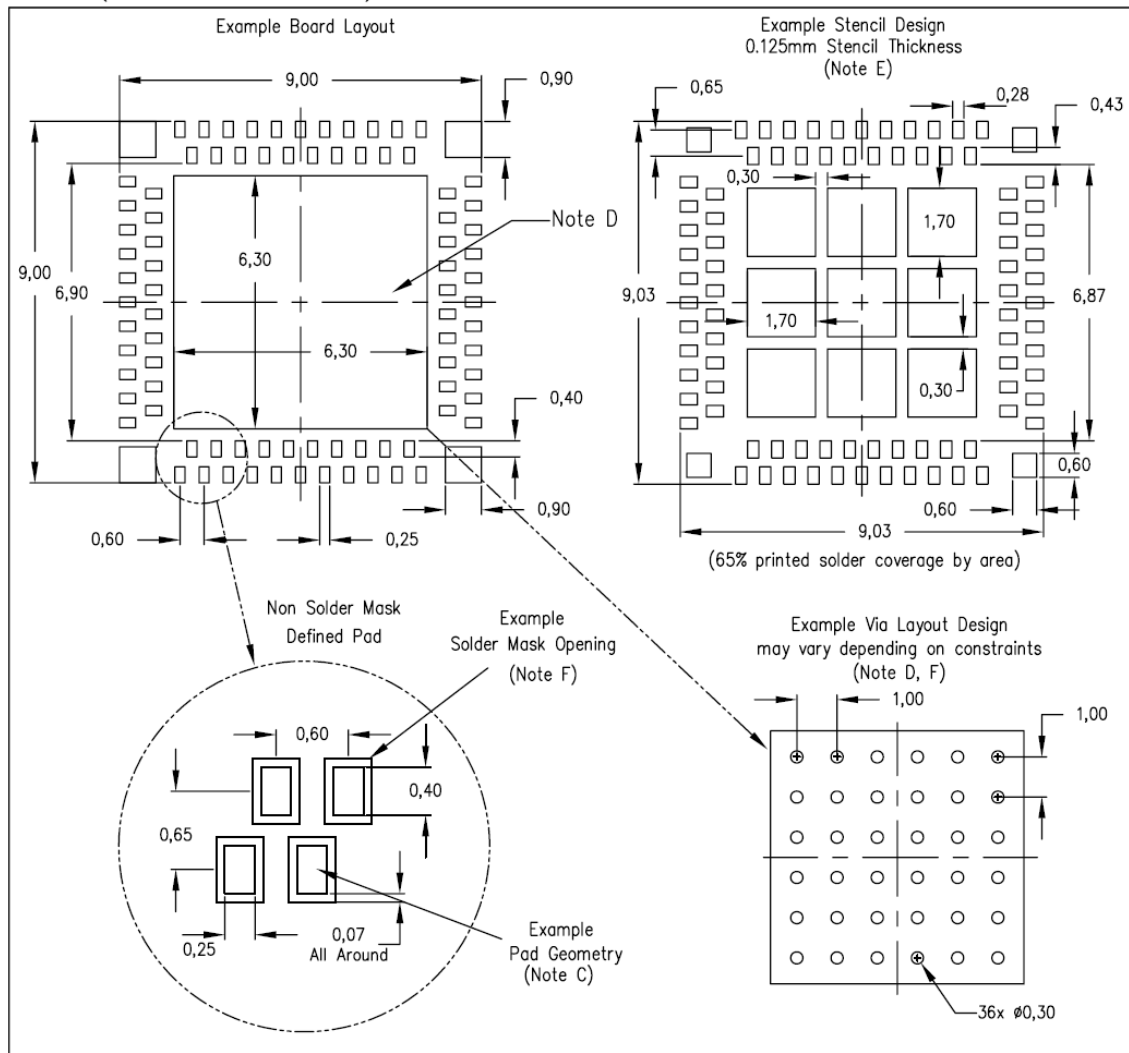


Figure 1: Industry Standard Layout Information

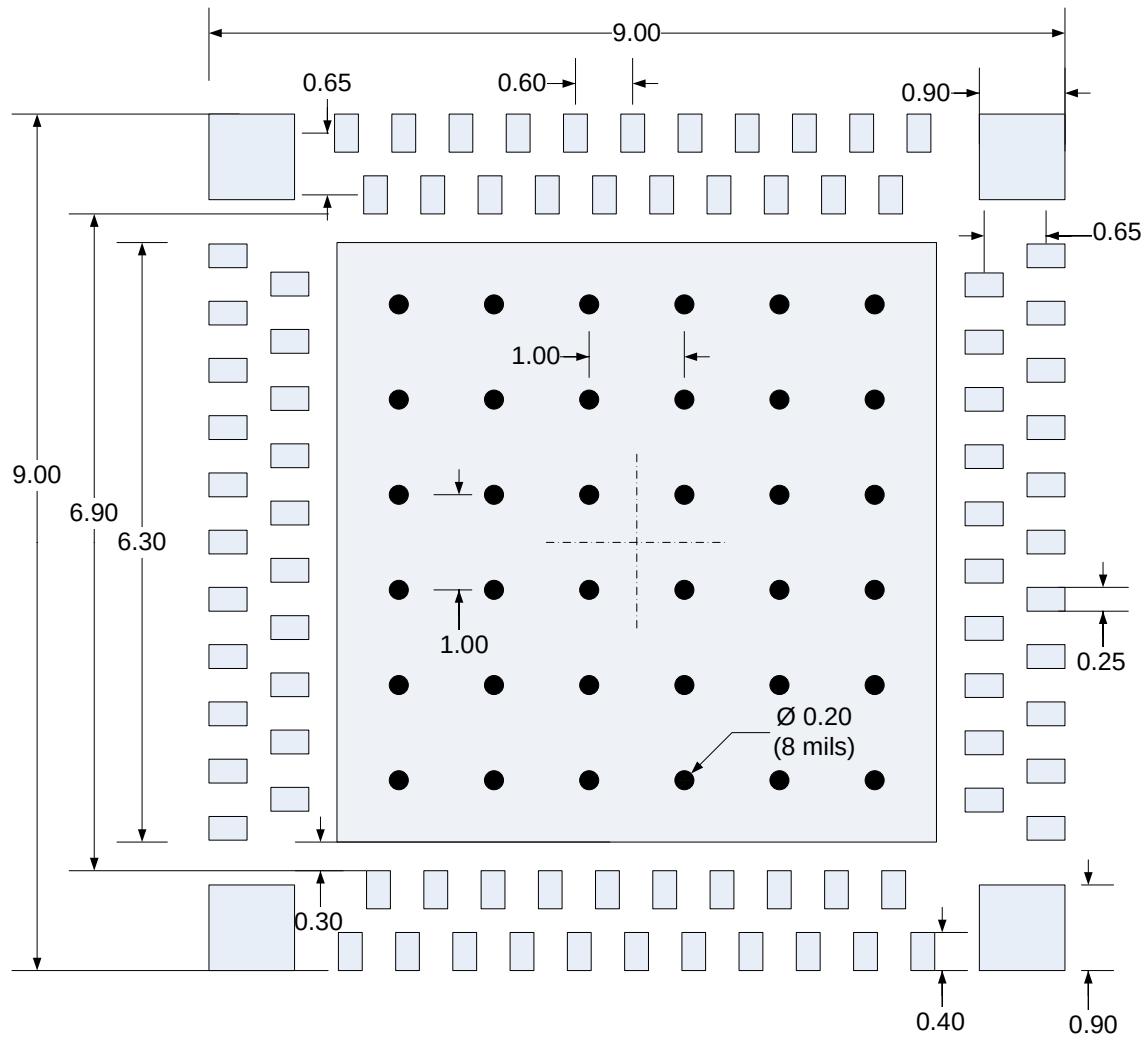


Figure 2: Modified PCB Land Pattern

Routing the Inner Row of Pins

The inner row of the mr-QFN package must be routed to necessary circuitry. The recommended approach is illustrated in Figure 3. The trace width should be kept at 0.13 mm (~5 mil). This will allow for a gap of 0.11 mm (4.3mils) between the trace and the pads for the pins in the outer row. This configuration is within the capabilities of most PCB fabrication houses. Once the trace has escaped the footprint of the part, the width can be expanded to support desired design rules or characteristic impedance. The solder mask keep-out is recommended to be made at the same dimensions as the pad. The industry document illustrates larger keep-out areas, but it will introduce a chance of the outer row pins shorting to the trace routed in between.

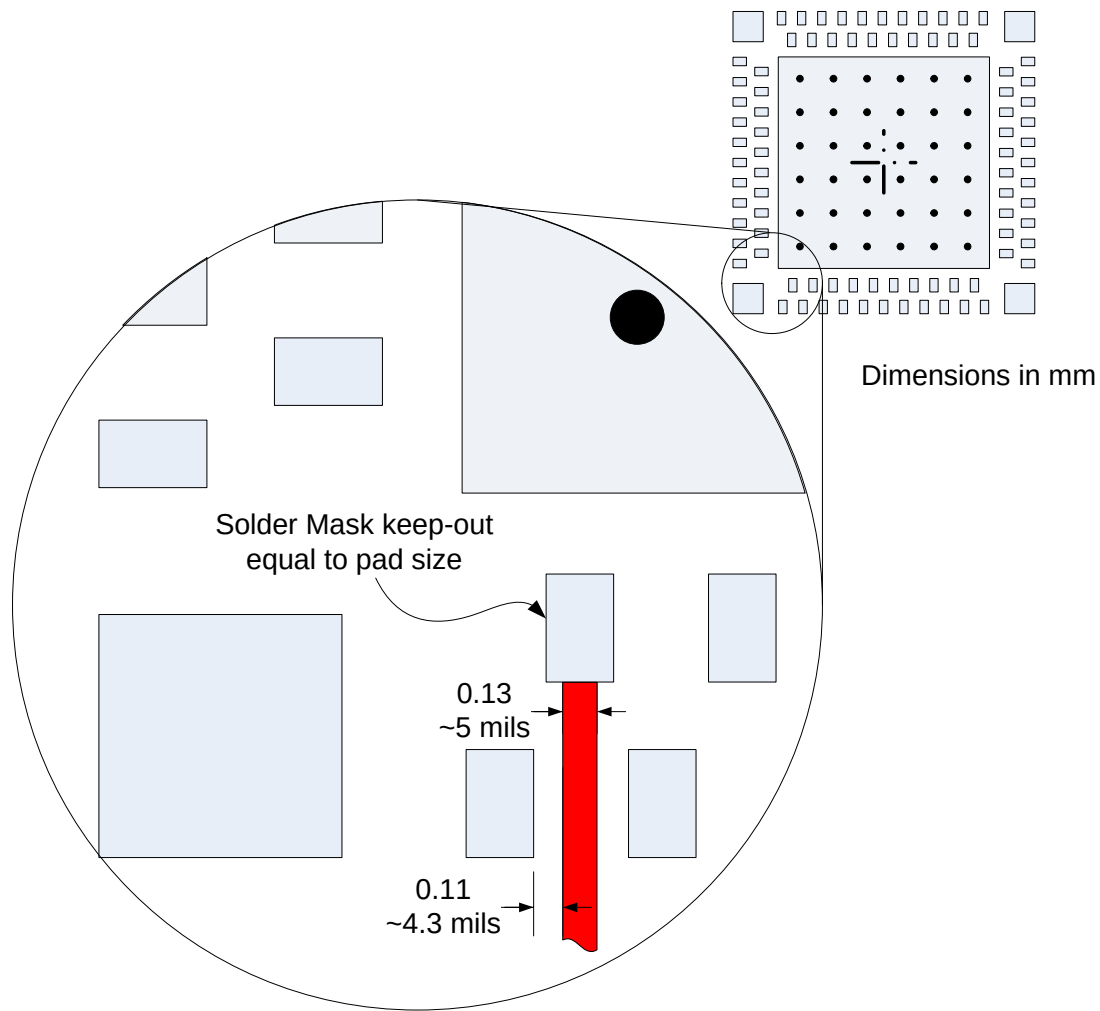


Figure 3: Escaping the Part

Standard Low-Cost Layout

The pins of the DAC348x include signal pins and power pins. The signal pins are generally routed to additional circuitry. The power pins are connected to an appropriate power plane layer and are connected to one or more bypass capacitors. Due to the number of pins and their close proximity to each other, the routing of all the connections is challenging.

Connections for all the pins of the device can be routed as previous shown in Figure 3 to escape the part. Providing good power supply connections for this device can result in some additional layout complexities. It is a good design practice to provide a low impedance connection to the power supply (the power plane in this case) with appropriate bypass capacitors located physically close to the pin. This technique provides the best noise immunity. Figure 4 shows one example on how to address the power supply pin

connections. The connection from the power supply pin is routed to escape the part. A 0.2mm drill via is placed just outside the land pattern of the device to make connection to the power plane layer. On the bottom side of the board, one or more bypass capacitors are placed that are connected to the power supply via. Ensure the other side of the capacitor(s) has a good connection to ground with at least one ground via close by. Alternatively, the bypass capacitors can be placed on the top side or a combination of top and bottom. This approach results in some layout challenges as the standard via size is 0.2 mm with a 0.4 mm pad. The size of the via pad requires the adjacent pins' routing to flare around the supply via to comply with PCB design rules. The next pins over must then flare even more and so on around the device. This approach impacts the routing of the entire part and may need to be mitigated by moving the power supply via farther out to provide more room for flaring the traces of the adjacent pins; however, attempt to keep the power supply traces as short as possible to minimize trace lead inductance.

Alternative Signal Routing with In-pad Vias

There is an alternate solution to ease the routing complexity and minimize the power supply trace lengths. Instead of having the power supply pin's trace escape the part before making a power plane connection with the via, the via can be placed in the device pad to provide the absolute shortest length to the bypass capacitor. Figure 5 shows one example of a connection with a via in the pad. This approach nearly eliminates the lead inductance of the connection to the bypass cap and it also provides more room for routing the other signal traces. The vias must be made smaller to fit within the pad. The via drill size is 0.15 mm and the via pad is 0.25 mm, exactly equal to the width of each pad. Further, the vias must be filled with a conductive epoxy to keep the pad smooth and flat so that the device pins will solder properly. The bypass caps are placed on the bottom side of the board right at the supply via and properly grounded as discussed previously. This approach results in lower trace inductance on the power supply connections and easier routing; however, there will likely be additional costs in the fabrication to account for the smaller drill size and the extra step needed to fill the vias.

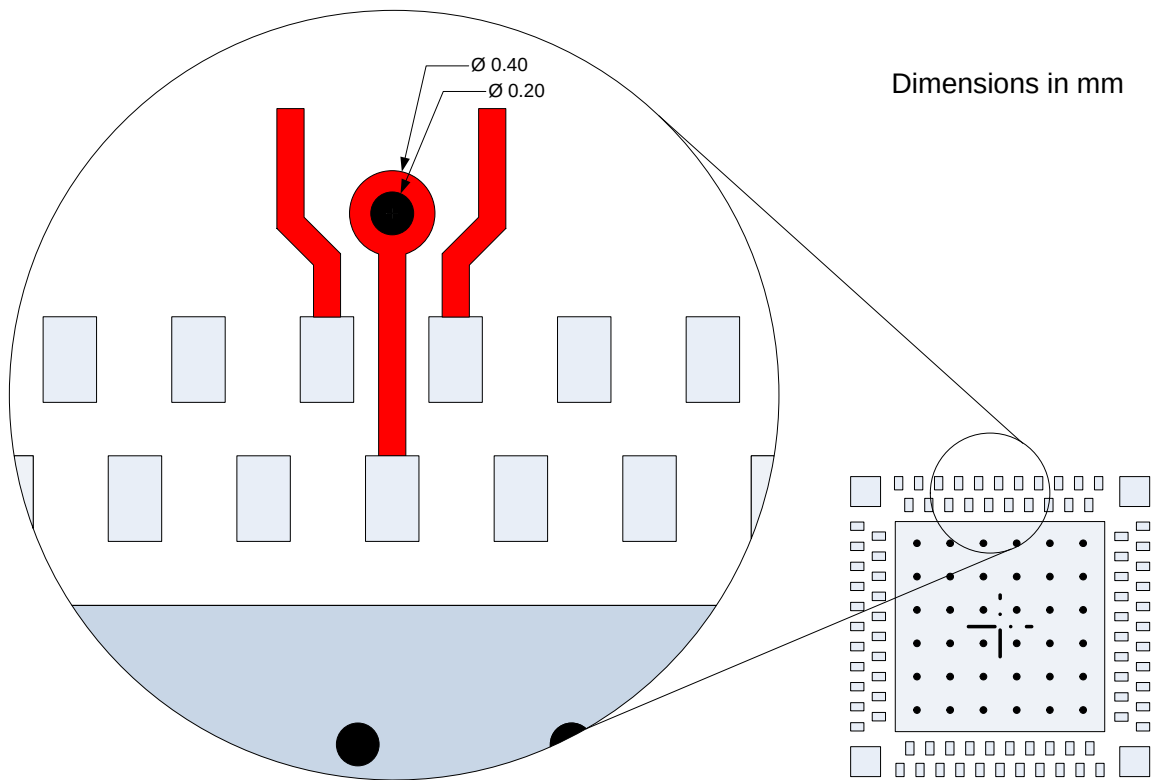


Figure 4: Example of a Power Supply Connection

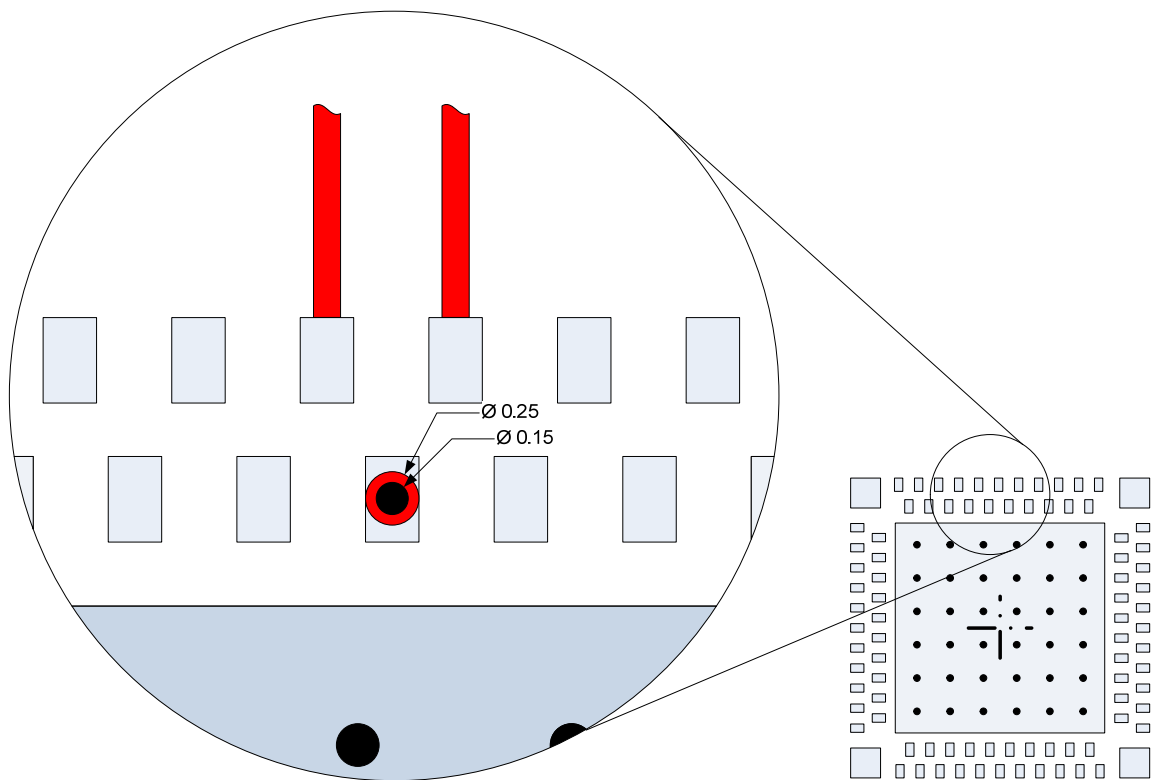


Figure 5: Alternate Example of Power Supply Connection with Via-in-Pad

Conclusion:

Utilizing the PCB layout recommendations in this document will ensure a quality device assembly utilizing the mr-QFN package. Additional information can be found on Texas Instrument's E2E forum by searching on the DAC3484 part number. If further questions arise relating to the manufacturing with the mr-QFN, Texas Instrument's application engineers and packaging engineers are available for support by posting to the E2E forum for High Speed Data Converters:

http://e2e.ti.com/support/data_converters/high_speed_data_converters/default.aspx