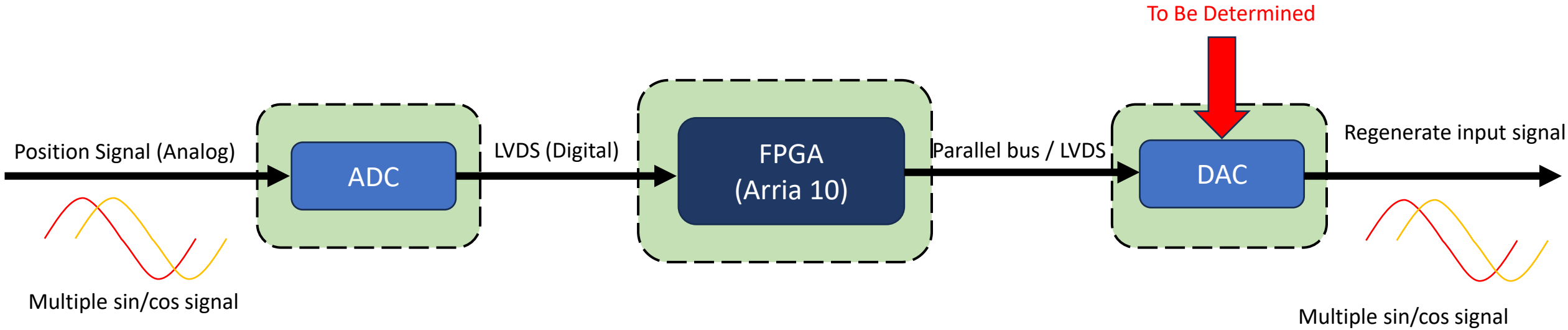
System Block Diagram – Related DACs



Differential Sin/Cos electrical:
1Vpp
2.5V DC biased
1k~5MHz

To regenerate sin/cos waveforms up to 5MHz from an FPGA (Arria 10):

1. High-speed DAC. (at least 100MSPS)
2. Resolution ≥14-bit.
3. Interface that compatible with FPGA. (Parallel bus or LVDS)
4. Prefer dual or quad channel output for multi sensor application.