Comments to your notes:

1.       “*I  inserted 8192 into the “No. of sample per cycle” field*”  - The Number of samples entered in the CER testing as per the following criteria. (shared previously in E2E post)



2.       “*I connected a 120KHz sine wave to input A of the ADC (I tried both 1dBm and 10dBm*” – The ADC input frequency must be coherent as per the following (shared previously in E2E post)



3.       “*In the “Threshold” field I inserted the number 100 (i did it only to threshold #1). Is it correct? how do you define this number?*” –In CER testing, the difference in the samples of a successive complete Sine cycle are compared with the threshold value entered in the HSDC pro GUI. Any difference which is above the entered threshold value is taken as an error and the error count is incremented.

For example:

              Threshold is set to 100.

In Sine cycle 1, at n instance ADC samples as 357890.

In next Sine cycle (say 2, 3…), at the same nth instance ADC samples as 357200

Difference = 357200-357890 = 690 > 100 (threshold) – This is taken as an error and the error the counter is incremented by one.

4.       “*BTW, why there are 5 thresholds*” – For computing CER testing for up to 5 different threshold values at a time. Please use as required.

5.       “*BTW, Is there a way to reset the counters without closing the program*” – There are no buttons to reset counters specifically. But the counters get reset when the user clicks on “Start Test” each time.

**Example:**

In ADS54J60 421 mode,

                Sampling Frequency      Fs   = 983.04 MHz

                Input Sine Frequency   Fin = 120 KHz

                Number of samples       N   = 81920 (greater than 65,536(2^n) and smaller than 131,072)

Now, to find the coherent input sine frequency, use the coherent calculator, as shown in next page.

                

The input sine frequency must be **changed to 132KHz** instead of 120KHz to obtain

coherency and then resume the test. In this case, 11 cycles are taken for CER testing.