Calibration scheme for AFE4900, AFE4410

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TEXAS INSTRUMENTS

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

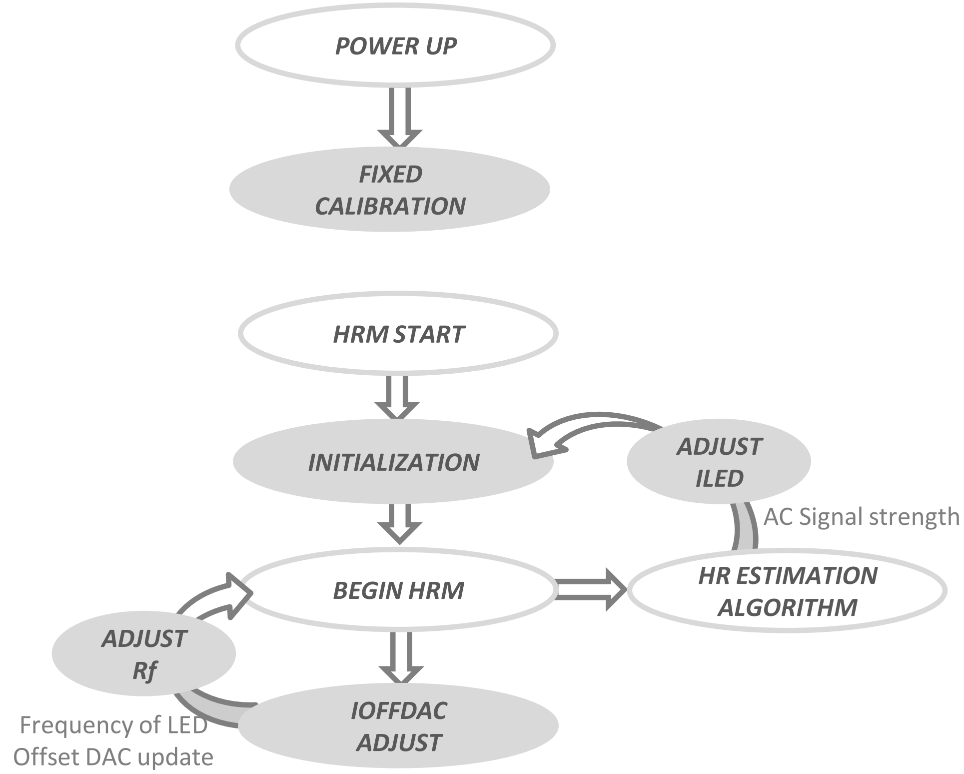
Objectives

The Calibration scheme has the following objectives:

- Adjust LED current to achieve a target DC current from the PD at which AC signal is good
- Enable operating at a high Rf setting by dynamically adjust Offset DAC in the Ambient (IOFFDAC_AMB) and LED (IOFFDAC_LED) phases so that signal in both LED and AMB phases stays within thresholds
- Make updates to the LED current and/or Rf if needed based on the HRM operation

The different routines in the Calibration scheme are tabulated below.

Routine	What it does	When to execute
Fixed calibration	Measures offset of channel (channel output for zero input) and accuracy of Offset DAC	One-time measurement on Power up
Initialization	Estimates Offset DAC needed to cancel DC from Ambient and LED. Also estimates LED current needed to achieve a target DC current in the Photodiode	Before start of HRM (Heart Rate Monitoring)
IOFFDAC adjust	Dynamically adjusts the Offset DAC in Ambient and LED phases by monitoring the phase outputs in every PRF cycle	During active HRM
Adjust Rf	Monitor LED phase signal level and if IOFFDAC_LED is being updated very frequently – determine if TIA gain need to be adjusted	Keep monitoring during HRM but use infrequently
Adjust ILED	Monitor AC Signal strength reported by HR Estimation algorithm and increase/ reduce LED current to tradeoff between SNR and Power	Keep monitoring during HRM but use infrequently – redo initialization for new ILED current setting



Guidelines for choice of AFE Filter Bandwidth:

The Calibration scheme outlined in this document involves dynamic updates to the Offset DAC. Every time the Offset DAC is updated, the AFE output in the LED and AMB phases changes a lot from one PRF cycle to the next. The Filter bandwidth and SAMP pulsewidth should therefore be chosen such that the filter is able to settle completely within one SAMP width. Set the SAMP width to about 3 times the Filter time constant.
Eg. Filter Bandwidth = 10 kHz (Filter time constant = 16 µs) => Choose SAMP width ≥ 48 µs.

Fixed calibration

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Estimate fixed parameters:

- Set Rf in Phases (1,2,3,4) as (**Rf_LO, Rf_HI, Rf_LO, Rf_HI**)
- Set PD_DISCONNECT to 1
- Set IOFFDAC in Phases (1,2,3,4) as (0 uA, 0 uA, IOFFDAC_MIN, IOFFDAC_MIN)
- Capture few AFE output codes in Phase (1,2,3,4) and take average (e.g. VOUT1 is average voltage of Phase 1)
- VOFFSET_LO = VOUT1
- VOFFSET_HI = VOUT2
- αIOFFDAC_LO = (VOUT3-VOUT1)/IOFFDAC_MIN
- αIOFFDAC_HI = (VOUT4-VOUT2)/IOFFDAC_MIN
- Set PD_DISCONNECT to 0

Perform this routine for all values of Rf_HI and store results for αIOFFDAC_HI

1b

Estimate fixed parameters:

1. Set Rf in Phases (1,2,3,4) as (**Rf_LO, Rf_LO, Rf_LO, Rf_LO**)
2. Set PD_DISCONNECT to 1
3. Create an array of size 128 as **VOFFDAC_ARRAY_RF_LO**
4. Set IOFFDAC in Phases (1,2,3,4) as (0 , 1LSB, 2LSBs, 3LSBs)
5. Capture few AFE output codes in Phase (1,2,3,4) and take average (e.g. VOUT1 is average voltage of Phase 1)
6. Store output of 4 Phases (i.e. VOUT1 to VOUT4) into first 4 location of **VOFFDAC_ARRAY_RF_LO**
7. Repeat step 4 to step 6 with each IOFFDAC values increased by 1 LSB and store the phase output into next 4 locations of VOFFDAC_ARRAY_RF_LO. This is done till all 127LSBs are set in step 4
8. Set PD_DISCONNECT to 0

Perform this routine for all values of IFS_OFFDAC

Description of parameters:

- **Rf_LO**: Low TIA gain setting (10 KΩ). Rf_LO = 10e3.
- **Rf_HI**: A set of high TIA gain settings to be used for HRM. Choosing too high a setting (like 2 MΩ) could cause the AFE output to saturate often leading to frequent recalibration. Therefore choose the set of Rf_HI after experimenting with the calibration routine running on the watch. An example set of Rf_HI could be {50e3, 100e3, 250e3, 500e3}.
- **IOFFDAC_MIN**: An Offset DAC current for which the AFE output will not saturate if TIA gain is set to Rf_HI. For example, setting IOFFDAC_MIN ~ 0.5V/(2*Rf_HI) will ensure that AFE output will be ~0.5V.
- Eg. If Rf_HI = 250e3: Choose IOFFDAC_MIN = 1e-6
- **VOUT***: AFE output in Volt.
- **VOFFDAC_ARRAY_RF_LO :** It is an 128 element array, which contains voltage output of AFE corresponding to all the codes of Offset DAC with TIA gain set to RF_LO. For example , with IFS_OFFDAC = 0,
  - 1st Element i.e. VOFFDAC_ARRAY_RF_LO[0] = 0*0.125uA*RF_LO,
  - 2nd Element i.e. VOFFDAC_ARRAY_RF_LO[1] = 1*0.125uA*RF_LO, similarly
  - 128th Element i.e. VOFFDAC_ARRAY_RF_LO[128] = 127*0.125uA*RF_LO

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Initialization

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Estimate IOFFDAC_AMB, CTR:

- Set Rf = **Rf_LO**
- Set IOFFDAC current to 0 in all phases
- Set LED current to **ILED0** in LED phase
- IOFFDAC_AMB = (VOUT_AMB-VOFFSET_LO)/ αIOFFDAC_LO
- IPD_LED0 = (VOUT_LED-VOUT_AMB)/ αIOFFDAC_LO
- CTR = IPD_LED0/ILED0

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Estimate IOFFDAC_LED:

- Set Rf = **Rf_LO**
- ILED_HRM = IPLETH/CTR
- Set ILED to ILED_HRM
- Set IOFFDAC in AMB and LED phases to IOFFDAC_AMB
- δIOFFDAC_LED = (VOUT_LED-VOUT_AMB)/ αIOFFDAC_LO
- IOFFDAC_LED = (IOFFDAC_AMB+δIOFFDAC_LED)

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Set HRM parameters:

- Set Rf = **Rf_HI**
- Set ILED to ILED_HRM
- Set IOFFDAC in AMB phase to IOFFDAC_AMB
- Set IOFFDAC in LED phase to IOFFDAC_LED
- Start HRM routine

During initial calibration, choose one Rf_HI from the set. This could be the value that gave good results during experimentation.

Description of parameters:

ILED0: An LED current setting used to estimate the CTR. Set to some low value like 5 mA. Needs to be chosen such that the AFE output does not saturate in Step 2. Eg. ILED0=5e-3

CTR: Current transfer ratio. Denotes ratio of the signal current in PD to the current drive of the LED.
Eg. ILED0=5e-3, IPD_LED0=1e-6: CTR=0.2e-3

IPLETH: Pleth current target. Refers to the DC component of the PPG signal current due to the LED. Since the AC current is proportional to the DC current, we set a preliminary target for the Pleth current as IPLETH. The value of IPLETH needs to be determined based on experimentation such that AC signal is good for choice of IPLETH. For eg. IPLETH=5e-6.

ILED_HRM: ILED current setting required to generate a Pleth current of ~IPLETH. Eg. IPLETH=5e-6, CTR=0.2e-3 → ILED_HRM=25e-3

IOFFDAC_AMB: Current setting of Offset DAC in Ambient phase to cancel the DC from Ambient

IOFFDAC_LED: Current setting of Offset DAC in LED phase to cancel the DC from both Ambient and LED

IOFFDAC adjust

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IOFFDAC_AMB update:

Monitor VOUT_AMB in every PRF cycle and do below updates if it goes outside ±VTHR_AMB:

- δIOFFDAC_AMB = (VOUT_AMB-VOFFSET_HI)/αIOFFDAC_HI
- Update IOFFDAC_AMB = IOFFDAC_AMB+ δIOFFDAC_AMB
- Update IOFFDAC_LED = (IOFFDAC_LED+δIOFFDAC_AMB)

Use αIOFFDAC_HI value corresponding to current Rf_HI setting

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IOFFDAC_LED update:

Monitor VOUT_LED in every PRF cycle and do below updates if it goes outside ± VTHR_LED:

- δIOFFDAC_LED = (VOUT_LED-VOUT_AMB)/αIOFFDAC_HI
- Update IOFFDAC_LED = (IOFFDAC_LED+δIOFFDAC_LED)

If in same PRF cycle, update happens in both Step 5 and Step 6, then IOFFDAC_LED is updated twice.

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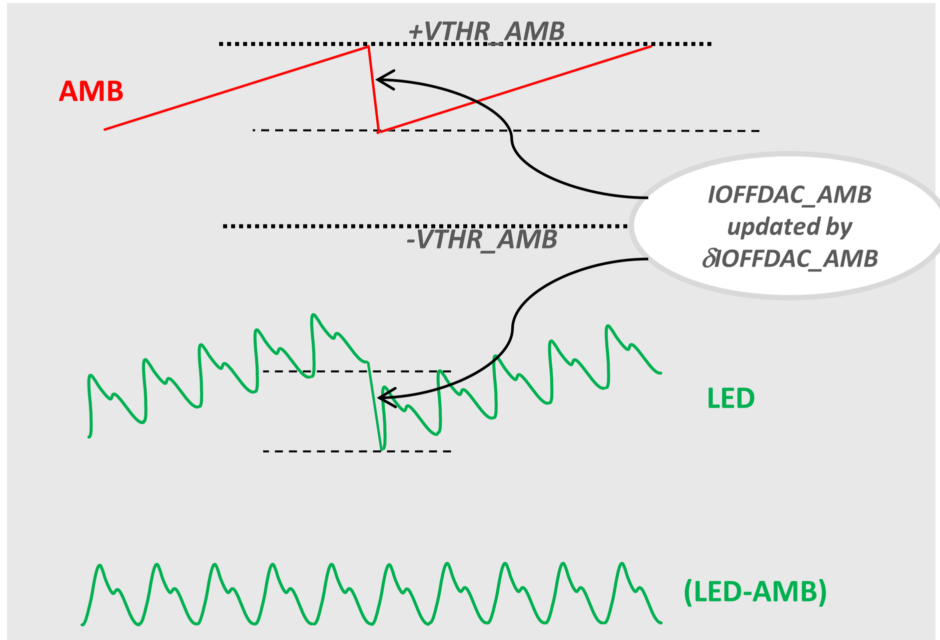
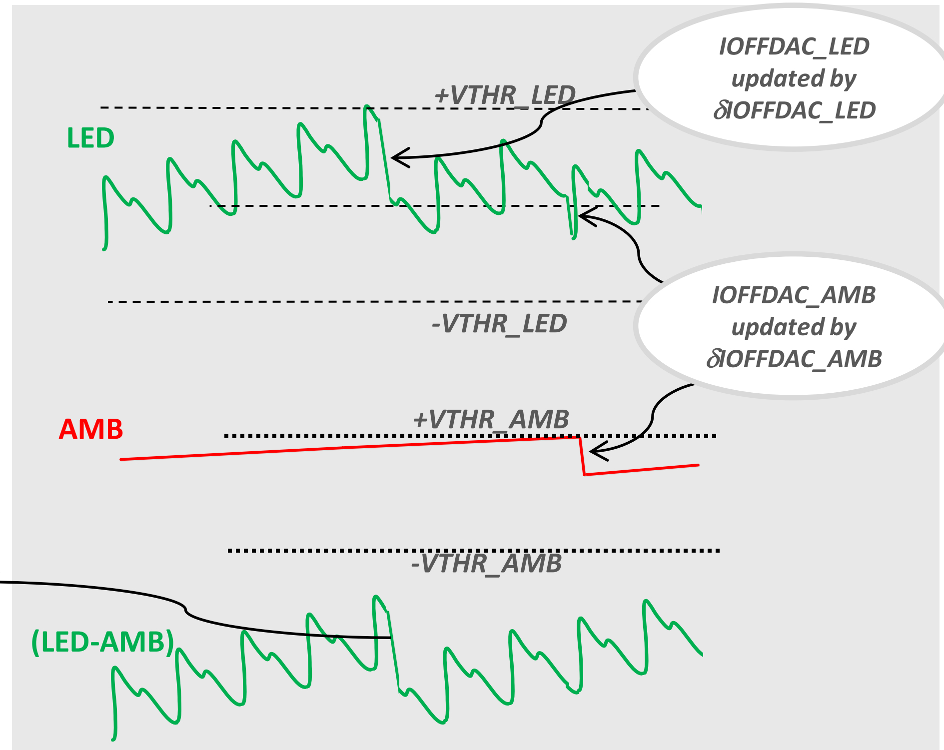
Restore DC cancelled by IOFFDAC_LED:

Perform following steps when IOFFDAC_LED or IOFFDAC_AMB is changed :

- V_AMB = element of VOFFDAC_ARRAY_RF_LO corresponding to IOFFDAC_AMB. For e.g. if code of 10 is used for IOFFDAC_AMB, then V_AMB = VOFFDAC_ARRAY_RF_LO[10]
- V_LED = element of VOFFDAC_ARRAY_RF_LO corresponding to IOFFDAC_LED. For e.g. if code of 15 is used for IOFFDAC_LED, then V_LED = VOFFDAC_ARRAY_RF_LO[15]
- RESTORED_LED_DC = (V_LED – V_AMB)* αIOFFDAC_HI / αIOFFDAC_LO





Change in IOFFDAC_LED results in a glitch in (LED-AMB) data. It might be undesirable for the HR Estimation algorithm to have frequent glitches. In the event of very frequent glitches, the output voltage level can be reduced by reducing Rf as shown in Step 7

Description of parameters:

VTHR_AMB: A threshold of output voltage for the Ambient phase output. For example, ±0.25V. If VOUT_AMB is within this range, then IOFFDAC_AMB is not updated. If VOUT_AMB goes outside this range, then IOFFDAC_AMB is updated to get VOUT_AMB close to 0. Choose VTHR_AMB based on experimentation with the calibration algorithm.

VTHR_LED: A threshold of output voltages for the LED phase output. For example, ± 0.75V. If VOUT_LED is within this range, then IOFFDAC_LED is not updated. If VOUT_LED goes outside this range, then IOFFDAC_LED is updated to get (VOUT_LED-VOUT_AMB) close to 0. Choose VTHR_LED based on experimentation with the calibration algorithm.

RESTORED_LED_DC: This is the DC cancelled in LED phase using IOFFDAC. This when added with VOUT_LED in each PRF cycle gives AC and DC component of LED /PPG signal

Adjust Rf

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Rf update:

If IOFFDAC_LED is being changed too frequently by Step 6:

- Decrease Rf_HI
- Go to Step 4

If output in LED phase is much below LED_RANGE:

- Increase Rf_HI
- Go to Step 4

Change in IOFFDAC_AMB is common between LED and AMB phases and therefore, ideally should not cause a glitch in (LED-AMB) data. However, it can result in a small glitch due to the non-linearity of the Offset DAC. Therefore, too frequent update in IOFFDAC_AMB may also not be desirable for the HR Estimation algorithm – evaluate for your specific case whether the “Adjust Rf” routine needs to also monitor and reduce Rf based on frequent changes in IOFFDAC_AMB also

Adjust ILED

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ILED update:

If AC signal is too low:

- Increase IPLETH
- Go to Step 2

If AC signal is too high:

- Decrease IPLETH
- Go to Step 2