

```

1
2 //AFE79xx
3 //START: Doing AFE Config
4
5
6 //Device Initialization for ChipVersion: 1.3
7
8
9 //*****System Parameters*****
10
11
12 //System Parameters:
13 // FRef      = 491.52
14 // FadcFb    = 2949.12
15 // FadcRx    = 2949.12
16 // Fdac      = 5898.24
17 // LMFSHdFb  = ['14810', '14810']
18 // LMFSHdRx  = ['181610', '181610', '181610', '181610']
19 // LMFSHdTxDsa = ['14810', '14810', '14810', '14810']
20 // RRFMode   = 1
21 // adcDataMuxEn = 1
22 // adcSelect0 = [0, 1, 2]
23 // adcSelect1 = [0, 1, 2]
24 // auxAdcEn   = False
25 // broadcastRxNcoSel = 0
26 // broadcastTxNcoSel = 0
27 // chipId     = 1
28 // chipType   = 0
29 // chipVersion = 19
30 // combineDucMode = [0, 0]
31 // continuousSysref = 0
32 // dacDataMuxEn = 1
33 // ddcFactorFb = [8, 8]
34 // ddcFactorRx = [16, 16, 16, 16]
35 // defaultFbDsa = [0, 0]
36 // defaultRxDsa = [0, 0, 0, 0]
37 // defaultTxDsa = [0, 0, 0, 0]
38 // ducFactorTx = [16, 16, 16, 16]
39 // enableDacInterleavedMode = False
40 // enableReliabilityDetector = True
41 // enableRxDsaCalibration = False
42 // enableTxDsaCalibration = False
43 // enableTxFbLoopbackLowLatencyMode = [False, False]
44 // executeLinkUpSequenceSeparately = False
45 // externalClockRx = False
46 // externalClockTx = False
47 // fbChainSelForDsaCalib = 0
48 // fbDataMux = [0, 1]
49 // fbDsaPerTx = [0, 0, 0, 0]
50 // fbDsaPerTxEn = False
51 // fbEnable = [True, False]
52 // fbJesdTxDsa = [1, 1]
53 // fbJesdTxDsa = [False, False]
54 // fbJesdTxDsaSyncMux = [0, 0]
55 // fbNco0 = [1800, 1800]
56 // fbNco1 = [1800, 2600]
57 // fbNco2 = [1800, 1900]
58 // fbNco3 = [1800, 1900]
59 // gpioMapping = { 'H8' : 'ADC_SYNC0',
60 //                 'H9' : 'DAC_SYNC0',
61 //                 'H16' : 'SPIB1_CSN',
62 //                 'K14' : 'FBABTDD',
63 //                 'H11' : 'INTBIPI_SPIB1_SDI',
64 //                 'P9' : 'DAC_SYNC3',
65 //                 'H7' : 'ADC_SYNC1',
66 //                 'G9' : 'DAC_SYNC1',
67 //                 'R6' : 'FBCDTDD',
68 //                 'N8' : 'ADC_SYNC2',
69 //                 'N9' : 'DAC_SYNC2',

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70 //      'H15'      : ['TXATDD', 'TXBTDD'],
71 //      'R15'      : ['RXCTDD', 'RXDTDD'],
72 //      'P14'      : 'GLOBAL_PDN',
73 //      'V5'       : ['TXCTDD', 'TXDTDD'],
74 //      'G16'      : 'SPIB1_CLK',
75 //      'E7'       : ['RXATDD', 'RXBTDD'],
76 //      'G12'      : 'SPIB1_SDO',
77 //      'N7'       : 'ADC_SYNC3',
78 //      }
79 //  gpioOverrideValSet = []
80 //  gpioPolarityInv = []
81 //  halfRateModeFb = [False, False]
82 //  halfRateModeRx = [False, False]
83 //  halfRateModeTx = [False, False]
84 //  intPinsParams[0] = {      'SPI'      :True,
85 //      'TXBPAP'      :True,
86 //      'TXCPAP'      :True,
87 //      'JESD'        :True,
88 //      'TXAPAP'      :True,
89 //      'PLL'         :True,
90 //      'TXDPAP'      :True,
91 //      }
92 //
93 //  intPinsParams[1] = {      'SPI'      :True,
94 //      'TXBPAP'      :True,
95 //      'TXCPAP'      :True,
96 //      'JESD'        :True,
97 //      'TXAPAP'      :True,
98 //      'PLL'         :True,
99 //      'TXDPAP'      :True,
100 //      }
101 //
102 //  jesdABLvdsSync = False
103 //  jesdCDLvdsSync = False
104 //  jesdLoopbackEn = 0
105 //  jesdRxK = [1, 1, 1, 1]
106 //  jesdRxLaneMux = [1, 3, 5, 6, 0, 2, 4, 7]
107 //  jesdRxProtocol = [2, 2]
108 //  jesdRxRbd = [4, 4]
109 //  jesdRxScr = [False, False, False, False]
110 //  jesdRxSyncMux = [0, 0, 0, 0]
111 //  jesdSendZeroesInTddOff = False
112 //  jesdSystemMode = [1, 1]
113 //  jesdTxIlaL = [4, 4, 2, 4, 4, 2]
114 //  jesdTxIlaLid = [0, 1, 2, 3, 4, 5, 6, 7]
115 //  jesdTxIlaM = [8, 8, 2, 8, 8, 2]
116 //  jesdTxLaneMux = [0, 2, 1, 3, 4, 5, 6, 7]
117 //  jesdTxProtocol = [2, 2]
118 //  libVersion = '1.7.3'
119 //  modeTdd = 0
120 //  ncoFbMode = 0
121 //  ncoFreqMode = '1KHz'
122 //  ncoRxMode = [0, 0]
123 //  ncoTxMode = [0, 0]
124 //  numBandsRx = [0, 0, 0, 0]
125 //  numBandsTx = [0, 0, 0, 0]
126 //  numFbNCO = 1
127 //  numRxNCO = 1
128 //  numRxNCOB0 = [1, 1, 1, 1]
129 //  numRxNCOB1 = [1, 1, 1, 1]
130 //  numTxNCO = 1
131 //  numTxNCOB0 = [1, 1, 1, 1]
132 //  numTxNCOB1 = [1, 1, 1, 1]
133 //  papParams[0] = {      'hpfWindowCntr' :0,
134 //      'triggerToRampDown' :50,
135 //      'triggerClearToRampUp' :50,
136 //      'hpfNumSample' :4,
137 //      'rampDownStartVal' :128,
138 //      'enable' :False,

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139 //      'maNumSample'      :128,
140 //      'alarmPinDynamicMode' :1,
141 //      'waitCounter'      :200,
142 //      'maWindowCntrTh'    :1,
143 //      'alarmMask' :64,
144 //      'detectInWaitState' :0,
145 //      'maThreshB0'      :90.0,
146 //      'maThreshB1'      :90.0,
147 //      'hpfWindowCntrTh'  :0,
148 //      'hpfEnable' :1,
149 //      'amplUpdateCycles' :2,
150 //      'alarmChannelMask' :14,
151 //      'maWindowCntr' :1,
152 //      'rampStickyMode'    :0,
153 //      'gainStepSize' :5,
154 //      'multMode' :0,
155 //      'alarmPulseGPIO'    :1000,
156 //      'hpfThreshComb' :30.0,
157 //      'maEnable' :1,
158 //      'attnStepSize' :5,
159 //      'maThreshComb' :90.0,
160 //      'hpfThreshB1' :30.0,
161 //      'hpfThreshB0' :30.0,
162 //      }
163 //
164 // papParams[1] = {      'hpfWindowCntr' :0,
165 //      'triggerToRampDown' :50,
166 //      'triggerClearToRampUp' :50,
167 //      'hpfNumSample' :4,
168 //      'rampDownStartVal' :128,
169 //      'enable' :False,
170 //      'maNumSample' :128,
171 //      'alarmPinDynamicMode' :1,
172 //      'waitCounter' :200,
173 //      'maWindowCntrTh' :1,
174 //      'alarmMask' :64,
175 //      'detectInWaitState' :0,
176 //      'maThreshB0' :90.0,
177 //      'maThreshB1' :90.0,
178 //      'hpfWindowCntrTh' :0,
179 //      'hpfEnable' :1,
180 //      'amplUpdateCycles' :2,
181 //      'alarmChannelMask' :14,
182 //      'maWindowCntr' :1,
183 //      'rampStickyMode' :0,
184 //      'gainStepSize' :5,
185 //      'multMode' :0,
186 //      'alarmPulseGPIO' :1000,
187 //      'hpfThreshComb' :30.0,
188 //      'maEnable' :1,
189 //      'attnStepSize' :5,
190 //      'maThreshComb' :90.0,
191 //      'hpfThreshB1' :30.0,
192 //      'hpfThreshB0' :30.0,
193 //      }
194 //
195 // papParams[2] = {      'hpfWindowCntr' :0,
196 //      'triggerToRampDown' :50,
197 //      'triggerClearToRampUp' :50,
198 //      'hpfNumSample' :4,
199 //      'rampDownStartVal' :128,
200 //      'enable' :False,
201 //      'maNumSample' :128,
202 //      'alarmPinDynamicMode' :1,
203 //      'waitCounter' :200,
204 //      'maWindowCntrTh' :1,
205 //      'alarmMask' :64,
206 //      'detectInWaitState' :0,
207 //      'maThreshB0' :90.0,

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208 //      'maThreshB1'      :90.0,
209 //      'hpfWindowCntrTh' :0,
210 //      'hpfEnable' :1,
211 //      'amplUpdateCycles' :2,
212 //      'alarmChannelMask' :14,
213 //      'maWindowCntr' :1,
214 //      'rampStickyMode' :0,
215 //      'gainStepSize' :5,
216 //      'multMode' :0,
217 //      'alarmPulseGPIO' :1000,
218 //      'hpfThreshComb' :30.0,
219 //      'maEnable' :1,
220 //      'attnStepSize' :5,
221 //      'maThreshComb' :90.0,
222 //      'hpfThreshB1' :30.0,
223 //      'hpfThreshB0' :30.0,
224 //      }
225 //
226 // papParams[3] = {      'hpfWindowCntr' :0,
227 //      'triggerToRampDown' :50,
228 //      'triggerClearToRampUp' :50,
229 //      'hpfNumSample' :4,
230 //      'rampDownStartVal' :128,
231 //      'enable' :False,
232 //      'maNumSample' :128,
233 //      'alarmPinDynamicMode' :1,
234 //      'waitCounter' :200,
235 //      'maWindowCntrTh' :1,
236 //      'alarmMask' :64,
237 //      'detectInWaitState' :0,
238 //      'maThreshB0' :90.0,
239 //      'maThreshB1' :90.0,
240 //      'hpfWindowCntrTh' :0,
241 //      'hpfEnable' :1,
242 //      'amplUpdateCycles' :2,
243 //      'alarmChannelMask' :14,
244 //      'maWindowCntr' :1,
245 //      'rampStickyMode' :0,
246 //      'gainStepSize' :5,
247 //      'multMode' :0,
248 //      'alarmPulseGPIO' :1000,
249 //      'hpfThreshComb' :30.0,
250 //      'maEnable' :1,
251 //      'attnStepSize' :5,
252 //      'maThreshComb' :90.0,
253 //      'hpfThreshB1' :30.0,
254 //      'hpfThreshB0' :30.0,
255 //      }
256 //
257 // pllGsmMode = False
258 // reliabilityDetectorDecayMode = 0
259 // rxChainSelForDsaCalib = 15
260 // rxDataMux = [0, 1, 2, 3, 4, 5, 6, 7]
261 // rxDsaBandCalibMode = 0
262 // rxDsaCalibMode = 0
263 // rxDsaGainRange = [0, 25]
264 // rxEnable = [True, True, True, True]
265 // rxJesdTxK = [1, 1, 1, 1]
266 // rxJesdTxScr = [False, False, False, False]
267 // rxJesdTxSyncMux = [0, 0, 0, 0]
268 // rxNco0 = [[1800, 2600], [1800, 2600], [1800, 2600], [1800, 2600]]
269 // rxNco1 = [[1800, 2600], [1800, 2600], [1800, 2600], [1800, 2600]]
270 // serdesFirmware = True
271 // serdesManualCTLE = [6, 6, 6, 6, 6, 6, 6, 6]
272 // serdesManualCTLEEn = False
273 // serdesRxLanePolarity = [False, False, False, False, False, False, False, False]
274 // serdesTxLanePolarity = [False, False, False, False, False, False, False, False]
275 // serdesTxMainCursor = [3, 0, 0, 0, 0, 0, 0, 3]
276 // serdesTxPostCursor = [0, 0, 0, 0, 0, 0, 0, 0]

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277 // serdesTxPreCursor = [0, 0, 0, 0, 0, 0, 0, 0, 0]
278 // setIlaParams = True
279 // spiMode = 1
280 // syncLoopBack = False
281 // sysrefTermination = 0
282 // txDataMux = [0, 1, 2, 3, 4, 5, 6, 7]
283 // txDsaBandCalibMode = 0
284 // txDsaCalibMode = 0
285 // txEnable = [True, True, True, True]
286 // txNco0 = [[1800, 2600], [1800, 2600], [1800, 2600], [1800, 2600]]
287 // txNco1 = [[1800, 2600], [1800, 2600], [1800, 2600], [1800, 2600]]
288 // txToFbMode = 0
289 // txdsaStartStop = [0, 29]
290 // useLcmClkForSysrefLatch = True
291 // useSpiSysref = False
292 // useTxForCalib = 0
293 //
294
295
296 //*****Configuration Starting*****
297 //
298
299
300 //EXTERNAL-ACTION: Toggle HW Reset
301
302
303 //STEP: rstDevice/step0
304
305 //START: Device Soft Reset and SPI Check
306
307 SPIWrite 0000,30 //global_soft_reset=0x0; Address(0x0[7:7])
308 SPIWrite 0000,b0 //global_soft_reset=0x1; Address(0x0[7:7])
309 SPIWrite 0000,30 //global_soft_reset=0x0; Address(0x0[7:7])
310 SPIWrite 0000,30 //global_4pin=0x1; Address(0x0[7:4])
311 SPIWrite 0000,30 //global_ascend=0x1; Address(0x0[7:5])
312 SPIRead 0003
313
314 //Read chip_type=0xa; Address(0x3[7:0],0x4[7:0])
315
316 SPIRead 0004
317 SPIRead 0005
318
319 //Read chip_id=0x78; Address(0x4[7:0],0x5[7:0],0x5[7:0],0x6[7:0])
320
321 SPIRead 0006
322
323 //Read chip_ver=0x11; Address(0x6[7:0],0x7[7:0])
324
325 SPIRead 0007
326 SPIRead 0008
327
328 //Read vendor_id=0x451; Address(0x7[7:0],0x8[7:0],0x8[7:0],0x9[7:0])
329
330
331 //END: Device Soft Reset and SPI Check
332
333
334 //STEP: rstDevice/step1
335
336 //START: Waking up device
337
338 SPIWrite 0015,80 //timing_controller=0x1; Address(0x15[7:7])
339 SPIWrite 0191,00 //force_tg_xx_A=0x0; Address(0x191[7:0])
340 SPIWrite 0231,00 //force_tg_xx_A=0x0; Address(0x231[7:0])
341 SPIWrite 02d1,00 //force_tg_xx_A=0x0; Address(0x2d1[7:0])
342 SPIWrite 0371,00 //force_tg_xx_A=0x0; Address(0x371[7:0])
343 SPIWrite 042a,00 //force_tg_xx_A=0x0; Address(0x42a[7:0])
344 SPIWrite 04e2,00 //force_tg_xx_A=0x0; Address(0x4e2[7:0])
345 SPIWrite 059a,00 //force_tg_xx_A=0x0; Address(0x59a[7:0])

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346 SPIWrite 0652,00 //force_tg_xx_A=0x0; Address(0x652[7:0])
347 SPIWrite 070a,00 //force_tg_xx_A=0x0; Address(0x70a[7:0])
348 SPIWrite 07c2,00 //force_tg_xx_A=0x0; Address(0x7c2[7:0])
349
350 //START: Setting TDD Pin in override state and setting override values.
351
352 SPIWrite 00ec,01 //use_reg_for_rxtdd=0x1; Address(0xec[7:0])
353 SPIWrite 00f4,01 //use_reg_for_fbtdd=0x1; Address(0xf4[7:0])
354 SPIWrite 00e4,01 //use_reg_for_txtdd=0x1; Address(0xe4[7:0])
355 SPIWrite 00ed,00 //reg_for_rxtdd=0x0; Address(0xed[7:0])
356 SPIWrite 00f5,00 //reg_for_fbtdd=0x0; Address(0xf5[7:0])
357 SPIWrite 00e5,00 //reg_for_txtdd=0x0; Address(0xe5[7:0])
358
359 //END: Setting TDD Pin in override state and setting override values.
360
361 SPIWrite 0015,00 //timing_controller=0x0; Address(0x15[7:7])
362 SPIWrite 0015,40 //digtop=0x1; Address(0x15[7:6])
363 SPIWrite 0190,03 //misc_spi_global_pdn_ctrl=0x1; Address(0x190[7:0])
364 SPIWrite 0190,01 //misc_spi_global_pdn_sig=0x0; Address(0x190[7:1])
365 SPIWrite 0015,00 //digtop=0x0; Address(0x15[7:6])
366
367 WAIT 0.005
368
369 //END: Done waking up device
370
371
372 //START: Changing termination to 100 ohm
373
374
375 //START: Requesting/releasing SPI Access to PLL Pages
376
377 SPIWrite 0015,40 //digtop=0x1; Address(0x15[7:6])
378 SPIWrite 0170,01 //pll_reg_spi_req_a=0x1; Address(0x170[7:0])
379 SPIWrite 0540,00 //pll_reg_spi_req_b1=0x0; Address(0x540[7:0])
380
381 SPIPoll 0171,0,0,01
382 SPIRead 0171
383
384 //Read pll_reg_spi_a_ack=0x1 (Meaning: );; Address(0x171[7:0])
385
386
387 //END: Requesting/releasing SPI Access to PLL Pages
388
389 SPIWrite 0015,00 //digtop=0x0; Address(0x15[7:6])
390 SPIWrite 0015,01 //pll=0x1; Address(0x15[7:0])
391 SPIWrite 0054,81
392 SPIWrite 0015,00 //pll=0x0; Address(0x15[7:0])
393
394 //START: Requesting/releasing SPI Access to PLL Pages
395
396 SPIWrite 0015,40 //digtop=0x1; Address(0x15[7:6])
397 SPIWrite 0170,00 //pll_reg_spi_req_a=0x0; Address(0x170[7:0])
398 SPIWrite 0540,00 //pll_reg_spi_req_b1=0x0; Address(0x540[7:0])
399
400 WAIT 0.2
401
402 //END: Requesting/releasing SPI Access to PLL Pages
403
404
405 //END: Changing termination to 100 ohm
406
407
408 //START: Setting CM4 Clock Div
409
410 SPIWrite 0015,00 //digtop=0x0; Address(0x15[7:6])
411 SPIWrite 0015,02 //ana_4t4r=0x1; Address(0x15[7:1])
412 SPIWrite 00c0,00 //CM4DIV_DIV=0x0; Address(0xc0[7:0])
413
414 //END: Setting CM4 Clock Div

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415
416 SPIWrite 0015,00 //ana_4t4r=0x0; Address(0x15[7:1])
417
418 //STEP: efuseChain/step0
419
420 //START: Loading Efuse Chain
421
422 SPIWrite 0015,40 //digtop=0x1; Address(0x15[7:6])
423 SPIWrite 08a8,02 //spi_ext_chain_ctrl_fusefarm1=0x2;
Address(0x8a8[7:0],0x8a9[7:0])
424 SPIWrite 0810,01 //spi_ovr_sys_clk_gate=0x1; Address(0x810[7:0])
425 SPIWrite 0830,01 //spi_ovr_sys_clk_gate=0x1; Address(0x830[7:0])
426 SPIWrite 0200,00 //spi_div_sys_clk_sel=0x0; Address(0x200[7:0])
427 SPIWrite 0210,00 //spi_div_sys_clk_sel=0x0; Address(0x210[7:0])
428 SPIWrite 0814,00 //spi_sys_rstn_ctrl=0x0; Address(0x814[7:0])
429 SPIWrite 0834,00 //spi_sys_rstn_ctrl=0x0; Address(0x834[7:0])
430 SPIWrite 0814,01 //spi_sys_rstn_ctrl=0x1; Address(0x814[7:0])
431 SPIWrite 0834,01 //spi_sys_rstn_ctrl=0x1; Address(0x834[7:0])
432 SPIWrite 0810,00 //spi_ovr_sys_clk_gate=0x0; Address(0x810[7:0])
433 SPIWrite 0830,00 //spi_ovr_sys_clk_gate=0x0; Address(0x830[7:0])
434 SPIWrite 0810,01 //spi_ovr_sys_clk_gate=0x1; Address(0x810[7:0])
435 SPIWrite 0830,01 //spi_ovr_sys_clk_gate=0x1; Address(0x830[7:0])
436 SPIWrite 0200,05 //spi_div_sys_clk_sel=0x5; Address(0x200[7:0])
437 SPIWrite 0210,00 //spi_div_sys_clk_sel=0x0; Address(0x210[7:0])
438 SPIWrite 0814,03 //spi_sys_rstn_ctrl=0x3; Address(0x814[7:0])
439 SPIWrite 0834,03 //spi_sys_rstn_ctrl=0x3; Address(0x834[7:0])
440 SPIWrite 0814,00 //spi_sys_rstn_ctrl=0x0; Address(0x814[7:0])
441 SPIWrite 0834,00 //spi_sys_rstn_ctrl=0x0; Address(0x834[7:0])
442 SPIWrite 0810,00 //spi_ovr_sys_clk_gate=0x0; Address(0x810[7:0])
443 SPIWrite 0830,00 //spi_ovr_sys_clk_gate=0x0; Address(0x830[7:0])
444 SPIWrite 0814,00 //spi_ovr_sys_autoload_chain=0x0; Address(0x814[7:2])
445 SPIWrite 0834,00 //spi_ovr_sys_autoload_chain=0x0; Address(0x834[7:2])
446 SPIWrite 0814,1c //spi_ovr_sys_autoload_chain=0x7; Address(0x814[7:2])
447 SPIWrite 0834,1c //spi_ovr_sys_autoload_chain=0x7; Address(0x834[7:2])
448 SPIWrite 0814,00 //spi_ovr_sys_autoload_chain=0x0; Address(0x814[7:2])
449 SPIWrite 0834,00 //spi_ovr_sys_autoload_chain=0x0; Address(0x834[7:2])
450
451 WAIT 0.05
452
453 //END: Loading Efuse Chain
454
455
456 //START: Checking for Efuse
457
458 SPIRead 0150
459
460 //Read obs_func_spi_chain_autoload_done=0xf; Address(0x150[7:0])
461
462 SPIRead 0150
463
464 //Read obs_func_spi_chain_autoload_error=0x0; Address(0x150[7:4])
465
466
467 //END: Checking for Efuse
468
469
470 //START: enabling Efuse Clock
471
472 SPIWrite 0830,01 //spi_ovr_sys_clk_gate=0x1; Address(0x830[7:0])
473 SPIWrite 0810,01 //spi_ovr_sys_clk_gate=0x1; Address(0x810[7:0])
474 SPIWrite 0910,0f //tx_dh_ahb_en=0xf; Address(0x910[7:0])
475 SPIWrite 0911,03 //fb_ec_ahb_en=0x3; Address(0x911[7:0])
476 SPIWrite 0912,0f //rx_ec_ahb_en=0xf; Address(0x912[7:0])
477
478 //END: enabling Efuse Clock
479
480 SPIWrite 0015,00 //digtop=0x0; Address(0x15[7:6])
481
482 //STEP:mcuWakeUp/step0

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```
483 SPIWrite 0018,20 //macro=0x1; Address(0x18[7:5])
484 SPIWrite 0140,01 //ss_reset_reg=0x1; Address(0x140[7:0])
485 SPIWrite 0140,00 //ss_reset_reg=0x0; Address(0x140[7:0])
486
487 WAIT 0.001
488 SPIRead 00f0
489
490 //Read MACRO_READY=0x1; Address(0xf0[7:0])
491
492
493 SPIPoll 00f0,0,0,1
494
495 SPIWrite 00a3,00 //MACRO_OPERAND_REG0=0x2;
Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
496 SPIWrite 00a2,00
497 SPIWrite 00a1,00
498 SPIWrite 00a0,02
499 SPIWrite 0193,01 //MACRO_OPCODE=0x1; Address(0x193[7:0],0x194[7:0])
500
501 WAIT 0.001
502 SPIRead 00f0
503
504 //Read MACRO_DONE=0x1; Address(0xf0[7:2])
505
506
507 SPIPoll 00f0,2,2,4
508
509 SPIRead 00f0
510
511 //Read MACRO_ERROR=0x0; Address(0xf0[7:3])
512
513 SPIRead 00f1
514
515 //Read MACRO_ERROR_OPCODE=0x0; Address(0xf1[7:0],0xf2[7:0])
516
517 SPIRead 00f0
518
519 //Read MACRO_ERROR_IN_OPCODE=0x0; Address(0xf0[7:4])
520
521 SPIRead 00f0
522
523 //Read MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0; Address(0xf0[7:5])
524
525 SPIRead 00f0
526
527 //Read MACRO_ERROR_IN_OPERAND=0x0; Address(0xf0[7:6])
528
529 SPIRead 00f0
530
531 //Read MACRO_ERROR_IN_EXECUTION=0x0; Address(0xf0[7:7])
532
533 SPIRead 00f3
534 SPIRead 00f2
535
536 //Read MACRO_ERROR_EXTENDED_CODE=0x0; Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
537
538 SPIRead 00f7
539 SPIRead 00f6
540 SPIRead 00f5
541 SPIRead 00f4
542
543 //Read MACRO_ERROR_EXTENDED_CODE_2=0x0;
Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
544
545 SPIRead 00fb
546 SPIRead 00fa
547 SPIRead 00f9
548 SPIRead 00f8
549
```



```

550 //Read MACRO_RESULT_REG0=0x13070a01;
Address(0xf8[7:0],0xf9[7:0],0xfa[7:0],0xfb[7:0],0xfc[7:0])
551
552 SPIRead 00ff
553 SPIRead 00fe
554 SPIRead 00fd
555 SPIRead 00fc
556
557 //Read MACRO_RESULT_REG1=0x2af8;
Address(0xfc[7:0],0xfd[7:0],0xfe[7:0],0xff[7:0],0x100[7:0])
558
559 SPIRead 00f0
560
561 //Read MACRO_READY=0x1; Address(0xf0[7:0])
562
563
564 SPIPoll 00f0,0,0,1
565
566 SPIWrite 00a3,00 //MACRO_OPERAND_REG0=0x0;
Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
567 SPIWrite 00a2,00
568 SPIWrite 00a1,00
569 SPIWrite 00a0,00
570 SPIWrite 0193,90 //MACRO_OPCODE=0x90; Address(0x193[7:0],0x194[7:0])
571
572 WAIT 0.001
573 SPIRead 00f0
574
575 //Read MACRO_DONE=0x1; Address(0xf0[7:2])
576
577
578 SPIPoll 00f0,2,2,4
579
580 SPIRead 00f0
581
582 //Read MACRO_ERROR=0x0; Address(0xf0[7:3])
583
584 SPIRead 00f1
585
586 //Read MACRO_ERROR_OPCODE=0x0; Address(0xf1[7:0],0xf2[7:0])
587
588 SPIRead 00f0
589
590 //Read MACRO_ERROR_IN_OPCODE=0x0; Address(0xf0[7:4])
591
592 SPIRead 00f0
593
594 //Read MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0; Address(0xf0[7:5])
595
596 SPIRead 00f0
597
598 //Read MACRO_ERROR_IN_OPERAND=0x0; Address(0xf0[7:6])
599
600 SPIRead 00f0
601
602 //Read MACRO_ERROR_IN_EXECUTION=0x0; Address(0xf0[7:7])
603
604 SPIRead 00f3
605 SPIRead 00f2
606
607 //Read MACRO_ERROR_EXTENDED_CODE=0x0; Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
608
609 SPIRead 00f7
610 SPIRead 00f6
611 SPIRead 00f5
612 SPIRead 00f4
613
614 //Read MACRO_ERROR_EXTENDED_CODE_2=0x0;
Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

```

```

615
616 SPIWrite 0144,08 //all_addr_high=0x2; Address(0x144[7:2])
617 SPIWrite 0018,00 //macro=0x0; Address(0x18[7:5])
618 SPIWrite 0018,08 //cm4top_dram=0x1; Address(0x18[7:3])
619 SPIWrite 03bf,00
620 SPIWrite 03be,07
621 SPIWrite 03bd,80
622 SPIWrite 03bc,00
623 SPIWrite 03c3,00
624 SPIWrite 03c2,04
625 SPIWrite 03c1,17
626 SPIWrite 03c0,46
627 SPIWrite 03d0,05
628 SPIWrite 03ac,1d
629 SPIWrite 03ad,1d
630 SPIWrite 1402,00
631 SPIWrite 1403,00
632 SPIWrite 1401,00
633 SPIWrite 0018,00 //cm4top_dram=0x0; Address(0x18[7:3])
634 SPIWrite 0018,20 //macro=0x1; Address(0x18[7:5])
635 SPIWrite 0144,08 //all_addr_high=0x2; Address(0x144[7:2])
636 SPIWrite 0018,00 //macro=0x0; Address(0x18[7:5])
637 SPIWrite 0018,08 //cm4top_dram=0x1; Address(0x18[7:3])
638 SPIWrite 1ee8,20
639 SPIWrite 1ee9,00
640 SPIWrite 0018,00 //cm4top_dram=0x0; Address(0x18[7:3])
641 SPIWrite 0018,20 //macro=0x1; Address(0x18[7:5])
642 SPIWrite 0144,08 //all_addr_high=0x2; Address(0x144[7:2])
643 SPIWrite 0018,00 //macro=0x0; Address(0x18[7:5])
644 SPIWrite 0018,08 //cm4top_dram=0x1; Address(0x18[7:3])
645 SPIWrite 1b5f,2c
646 SPIWrite 0018,00 //cm4top_dram=0x0; Address(0x18[7:3])
647 SPIWrite 0018,20 //macro=0x1; Address(0x18[7:5])
648 SPIWrite 0144,08 //all_addr_high=0x2; Address(0x144[7:2])
649 SPIWrite 0018,00 //macro=0x0; Address(0x18[7:5])
650 SPIWrite 0018,08 //cm4top_dram=0x1; Address(0x18[7:3])
651 SPIWrite 1b6f,07
652 SPIWrite 0018,00 //cm4top_dram=0x0; Address(0x18[7:3])
653 SPIWrite 0018,20 //macro=0x1; Address(0x18[7:5])
654 SPIWrite 0144,08 //all_addr_high=0x2; Address(0x144[7:2])
655 SPIWrite 0018,00 //macro=0x0; Address(0x18[7:5])
656 SPIWrite 0018,08 //cm4top_dram=0x1; Address(0x18[7:3])
657 SPIWrite 1e7d,09
658 SPIWrite 0018,00 //cm4top_dram=0x0; Address(0x18[7:3])
659 SPIWrite 0018,20 //macro=0x1; Address(0x18[7:5])
660 SPIWrite 0144,08 //all_addr_high=0x2; Address(0x144[7:2])
661 SPIWrite 0018,00 //macro=0x0; Address(0x18[7:5])
662 SPIWrite 0018,08 //cm4top_dram=0x1; Address(0x18[7:3])
663 SPIWrite 1a70,d0
664 SPIWrite 1a71,00
665 SPIWrite 0018,00 //cm4top_dram=0x0; Address(0x18[7:3])
666 SPIWrite 0018,20 //macro=0x1; Address(0x18[7:5])
667 SPIWrite 0144,08 //all_addr_high=0x2; Address(0x144[7:2])
668 SPIWrite 0018,00 //macro=0x0; Address(0x18[7:5])
669 SPIWrite 0018,08 //cm4top_dram=0x1; Address(0x18[7:3])
670 SPIWrite 1b20,c0
671 SPIWrite 1b21,00
672 SPIWrite 0018,00 //cm4top_dram=0x0; Address(0x18[7:3])
673 SPIWrite 0018,20 //macro=0x1; Address(0x18[7:5])
674 SPIRead 00f0
675
676 //Read MACRO_READY=0x1; Address(0xf0[7:0])
677
678
679 SPIPoll 00f0,0,0,1
680
681 SPIWrite 00a3,00 //MACRO_OPERAND_REG0=0x1;
Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
682 SPIWrite 00a2,00

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```

683 SPIWrite 00a1,00
684 SPIWrite 00a0,01
685 SPIWrite 0193,90 //MACRO_OPCODE=0x90; Address(0x193[7:0],0x194[7:0])
686
687 WAIT 0.001
688 SPIRead 00f0
689
690 //Read MACRO_DONE=0x1; Address(0xf0[7:2])
691
692
693 SPIPoll 00f0,2,2,4
694
695 SPIRead 00f0
696
697 //Read MACRO_ERROR=0x0; Address(0xf0[7:3])
698
699 SPIRead 00f1
700
701 //Read MACRO_ERROR_OPCODE=0x0; Address(0xf1[7:0],0xf2[7:0])
702
703 SPIRead 00f0
704
705 //Read MACRO_ERROR_IN_OPCODE=0x0; Address(0xf0[7:4])
706
707 SPIRead 00f0
708
709 //Read MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0; Address(0xf0[7:5])
710
711 SPIRead 00f0
712
713 //Read MACRO_ERROR_IN_OPERAND=0x0; Address(0xf0[7:6])
714
715 SPIRead 00f0
716
717 //Read MACRO_ERROR_IN_EXECUTION=0x0; Address(0xf0[7:7])
718
719 SPIRead 00f3
720 SPIRead 00f2
721
722 //Read MACRO_ERROR_EXTENDED_CODE=0x0; Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
723
724 SPIRead 00f7
725 SPIRead 00f6
726 SPIRead 00f5
727 SPIRead 00f4
728
729 //Read MACRO_ERROR_EXTENDED_CODE_2=0x0;
Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
730
731 SPIWrite 0018,00 //macro=0x0; Address(0x18[7:5])
732
733 //STEP: mcuWakeUp/step1
734 SPIWrite 0018,20 //macro=0x1; Address(0x18[7:5])
735 SPIWrite 0144,00 //all_addr_high=0x0; Address(0x144[7:2])
736 SPIWrite 0018,00 //macro=0x0; Address(0x18[7:5])
737 SPIWrite 0018,01 //sys_calib_macro_memory=0x1; Address(0x18[7:0])
738 SPIWrite 0020,00
739 SPIWrite 0021,00
740 SPIWrite 0022,00
741 SPIWrite 0023,00
742 SPIWrite 0024,8d
743 SPIWrite 0025,0c
744 SPIWrite 0026,03
745 SPIWrite 0027,00
746 SPIWrite 0028,b5
747 SPIWrite 0029,a4
748 SPIWrite 002a,6d
749 SPIWrite 002b,ea
750 SPIWrite 002c,7d

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751 SPIWrite 002d,19
752 SPIWrite 002e,ce
753 SPIWrite 002f,ca
754 SPIWrite 0030,01
755 SPIWrite 0031,07
756 SPIWrite 0032,08
757 SPIWrite 0033,12
758 SPIWrite 0034,14
759 SPIWrite 0035,00
760 SPIWrite 0036,01
761 SPIWrite 0037,0a
762 SPIWrite 0038,07
763 SPIWrite 0039,13
764 SPIWrite 003a,f8
765 SPIWrite 003b,2a
766 SPIWrite 003c,01
767 SPIWrite 003d,0a
768 SPIWrite 003e,07
769 SPIWrite 003f,13
770 SPIWrite 0040,f8
771 SPIWrite 0041,2a
772 SPIWrite 0042,00
773 SPIWrite 0043,00
774 SPIWrite 0044,00
775 SPIWrite 0045,00
776 SPIWrite 0046,00
777 SPIWrite 0047,00
778 SPIWrite 0048,00
779 SPIWrite 0049,00
780 SPIWrite 004a,00
781 SPIWrite 004b,00
782 SPIWrite 004c,00
783 SPIWrite 004d,00
784 SPIWrite 004e,00
785 SPIWrite 004f,00
786 SPIWrite 0050,f8
787 SPIWrite 0051,b5
788 SPIWrite 0052,76
789 SPIWrite 0053,48
790 SPIWrite 0054,77
791 SPIWrite 0055,4b
792 SPIWrite 0056,04
793 SPIWrite 0057,68
794 SPIWrite 0058,44
795 SPIWrite 0059,f0
796 SPIWrite 005a,40
797 SPIWrite 005b,01
798 SPIWrite 005c,d2
799 SPIWrite 005d,4f
800 SPIWrite 005e,01
801 SPIWrite 005f,60
802 SPIWrite 0060,1e
803 SPIWrite 0061,68
804 SPIWrite 0062,50
805 SPIWrite 0063,f8
806 SPIWrite 0064,c0
807 SPIWrite 0065,1c
808 SPIWrite 0066,72
809 SPIWrite 0067,48
810 SPIWrite 0068,00
811 SPIWrite 0069,91
812 SPIWrite 006a,01
813 SPIWrite 006b,68
814 SPIWrite 006c,41
815 SPIWrite 006d,f0
816 SPIWrite 006e,01
817 SPIWrite 006f,01
818 SPIWrite 0070,01
819 SPIWrite 0071,60

820 SPIWrite 0072,01
821 SPIWrite 0073,68
822 SPIWrite 0074,00
823 SPIWrite 0075,25
824 SPIWrite 0076,21
825 SPIWrite 0077,f0
826 SPIWrite 0078,02
827 SPIWrite 0079,01
828 SPIWrite 007a,01
829 SPIWrite 007b,60
830 SPIWrite 007c,02
831 SPIWrite 007d,68
832 SPIWrite 007e,3c
833 SPIWrite 007f,60
834 SPIWrite 0080,c6
835 SPIWrite 0081,f3
836 SPIWrite 0082,40
837 SPIWrite 0083,11
838 SPIWrite 0084,01
839 SPIWrite 0085,eb
840 SPIWrite 0086,96
841 SPIWrite 0087,11
842 SPIWrite 0088,42
843 SPIWrite 0089,f0
844 SPIWrite 008a,08
845 SPIWrite 008b,02
846 SPIWrite 008c,02
847 SPIWrite 008d,60
848 SPIWrite 008e,0f
849 SPIWrite 008f,e0
850 SPIWrite 0090,21
851 SPIWrite 0091,46
852 SPIWrite 0092,49
853 SPIWrite 0093,1e
854 SPIWrite 0094,fd
855 SPIWrite 0095,d1
856 SPIWrite 0096,00
857 SPIWrite 0097,bf
858 SPIWrite 0098,5b
859 SPIWrite 0099,1c
860 SPIWrite 009a,20
861 SPIWrite 009b,e0
862 SPIWrite 009c,22
863 SPIWrite 009d,46
864 SPIWrite 009e,52
865 SPIWrite 009f,1e
866 SPIWrite 00a0,fd
867 SPIWrite 00a1,d1
868 SPIWrite 00a2,00
869 SPIWrite 00a3,bf
870 SPIWrite 00a4,6d
871 SPIWrite 00a5,1c
872 SPIWrite 00a6,0d
873 SPIWrite 00a7,e0
874 SPIWrite 00a8,64
875 SPIWrite 00a9,1e
876 SPIWrite 00aa,fd
877 SPIWrite 00ab,d1
878 SPIWrite 00ac,00
879 SPIWrite 00ad,bf
880 SPIWrite 00ae,6d
881 SPIWrite 00af,1c
882 SPIWrite 00b0,13
883 SPIWrite 00b1,24
884 SPIWrite 00b2,a9
885 SPIWrite 00b3,42
886 SPIWrite 00b4,c0
887 SPIWrite 00b5,f2
888 SPIWrite 00b6,00

889 SPIWrite 00b7,04
890 SPIWrite 00b8,f6
891 SPIWrite 00b9,d8
892 SPIWrite 00ba,02
893 SPIWrite 00bb,68
894 SPIWrite 00bc,00
895 SPIWrite 00bd,25
896 SPIWrite 00be,22
897 SPIWrite 00bf,f0
898 SPIWrite 00c0,08
899 SPIWrite 00c1,02
900 SPIWrite 00c2,02
901 SPIWrite 00c3,60
902 SPIWrite 00c4,a9
903 SPIWrite 00c5,42
904 SPIWrite 00c6,e9
905 SPIWrite 00c7,d8
906 SPIWrite 00c8,08
907 SPIWrite 00c9,33
908 SPIWrite 00ca,01
909 SPIWrite 00cb,68
910 SPIWrite 00cc,1d
911 SPIWrite 00cd,68
912 SPIWrite 00ce,41
913 SPIWrite 00cf,f0
914 SPIWrite 00d0,02
915 SPIWrite 00d1,01
916 SPIWrite 00d2,c5
917 SPIWrite 00d3,f3
918 SPIWrite 00d4,40
919 SPIWrite 00d5,12
920 SPIWrite 00d6,00
921 SPIWrite 00d7,23
922 SPIWrite 00d8,01
923 SPIWrite 00d9,60
924 SPIWrite 00da,02
925 SPIWrite 00db,eb
926 SPIWrite 00dc,95
927 SPIWrite 00dd,10
928 SPIWrite 00de,98
929 SPIWrite 00df,42
930 SPIWrite 00e0,d6
931 SPIWrite 00e1,d8
932 SPIWrite 00e2,f8
933 SPIWrite 00e3,bd
934 SPIWrite 00e4,52
935 SPIWrite 00e5,4a
936 SPIWrite 00e6,c9
937 SPIWrite 00e7,4b
938 SPIWrite 00e8,11
939 SPIWrite 00e9,68
940 SPIWrite 00ea,06
941 SPIWrite 00eb,20
942 SPIWrite 00ec,21
943 SPIWrite 00ed,f0
944 SPIWrite 00ee,01
945 SPIWrite 00ef,01
946 SPIWrite 00f0,11
947 SPIWrite 00f1,60
948 SPIWrite 00f2,53
949 SPIWrite 00f3,f8
950 SPIWrite 00f4,04
951 SPIWrite 00f5,2b
952 SPIWrite 00f6,d2
953 SPIWrite 00f7,f8
954 SPIWrite 00f8,18
955 SPIWrite 00f9,11
956 SPIWrite 00fa,40
957 SPIWrite 00fb,1e

958 SPIWrite 00fc,21
959 SPIWrite 00fd,f4
960 SPIWrite 00fe,00
961 SPIWrite 00ff,71
962 SPIWrite 0100,c2
963 SPIWrite 0101,f8
964 SPIWrite 0102,18
965 SPIWrite 0103,11
966 SPIWrite 0104,f5
967 SPIWrite 0105,d1
968 SPIWrite 0106,d8
969 SPIWrite 0107,48
970 SPIWrite 0108,01
971 SPIWrite 0109,68
972 SPIWrite 010a,4a
973 SPIWrite 010b,4a
974 SPIWrite 010c,d1
975 SPIWrite 010d,f8
976 SPIWrite 010e,04
977 SPIWrite 010f,05
978 SPIWrite 0110,20
979 SPIWrite 0111,f0
980 SPIWrite 0112,3f
981 SPIWrite 0113,00
982 SPIWrite 0114,c1
983 SPIWrite 0115,f8
984 SPIWrite 0116,04
985 SPIWrite 0117,05
986 SPIWrite 0118,12
987 SPIWrite 0119,68
988 SPIWrite 011a,00
989 SPIWrite 011b,21
990 SPIWrite 011c,c2
991 SPIWrite 011d,f3
992 SPIWrite 011e,40
993 SPIWrite 011f,10
994 SPIWrite 0120,00
995 SPIWrite 0121,eb
996 SPIWrite 0122,92
997 SPIWrite 0123,10
998 SPIWrite 0124,06
999 SPIWrite 0125,e0
1000 SPIWrite 0126,13
1001 SPIWrite 0127,22
1002 SPIWrite 0128,c0
1003 SPIWrite 0129,f2
1004 SPIWrite 012a,00
1005 SPIWrite 012b,02
1006 SPIWrite 012c,52
1007 SPIWrite 012d,1e
1008 SPIWrite 012e,fd
1009 SPIWrite 012f,d1
1010 SPIWrite 0130,00
1011 SPIWrite 0131,bf
1012 SPIWrite 0132,49
1013 SPIWrite 0133,1c
1014 SPIWrite 0134,88
1015 SPIWrite 0135,42
1016 SPIWrite 0136,f6
1017 SPIWrite 0137,d8
1018 SPIWrite 0138,9b
1019 SPIWrite 0139,48
1020 SPIWrite 013a,3c
1021 SPIWrite 013b,49
1022 SPIWrite 013c,00
1023 SPIWrite 013d,68
1024 SPIWrite 013e,08
1025 SPIWrite 013f,60
1026 SPIWrite 0140,70

1027 SPIWrite 0141,47
1028 SPIWrite 0142,3b
1029 SPIWrite 0143,49
1030 SPIWrite 0144,01
1031 SPIWrite 0145,28
1032 SPIWrite 0146,f8
1033 SPIWrite 0147,b5
1034 SPIWrite 0148,09
1035 SPIWrite 0149,d0
1036 SPIWrite 014a,0a
1037 SPIWrite 014b,68
1038 SPIWrite 014c,22
1039 SPIWrite 014d,f4
1040 SPIWrite 014e,60
1041 SPIWrite 014f,02
1042 SPIWrite 0150,02
1043 SPIWrite 0151,f5
1044 SPIWrite 0152,00
1045 SPIWrite 0153,12
1046 SPIWrite 0154,0a
1047 SPIWrite 0155,60
1048 SPIWrite 0156,0a
1049 SPIWrite 0157,68
1050 SPIWrite 0158,22
1051 SPIWrite 0159,f4
1052 SPIWrite 015a,e0
1053 SPIWrite 015b,12
1054 SPIWrite 015c,08
1055 SPIWrite 015d,e0
1056 SPIWrite 015e,0a
1057 SPIWrite 015f,68
1058 SPIWrite 0160,22
1059 SPIWrite 0161,f4
1060 SPIWrite 0162,60
1061 SPIWrite 0163,02
1062 SPIWrite 0164,0a
1063 SPIWrite 0165,60
1064 SPIWrite 0166,0a
1065 SPIWrite 0167,68
1066 SPIWrite 0168,22
1067 SPIWrite 0169,f4
1068 SPIWrite 016a,e0
1069 SPIWrite 016b,12
1070 SPIWrite 016c,02
1071 SPIWrite 016d,f5
1072 SPIWrite 016e,80
1073 SPIWrite 016f,22
1074 SPIWrite 0170,30
1075 SPIWrite 0171,4d
1076 SPIWrite 0172,0a
1077 SPIWrite 0173,60
1078 SPIWrite 0174,00
1079 SPIWrite 0175,23
1080 SPIWrite 0176,2a
1081 SPIWrite 0177,1d
1082 SPIWrite 0178,0b
1083 SPIWrite 0179,75
1084 SPIWrite 017a,16
1085 SPIWrite 017b,68
1086 SPIWrite 017c,0c
1087 SPIWrite 017d,68
1088 SPIWrite 017e,1f
1089 SPIWrite 017f,46
1090 SPIWrite 0180,c6
1091 SPIWrite 0181,f3
1092 SPIWrite 0182,40
1093 SPIWrite 0183,12
1094 SPIWrite 0184,24
1095 SPIWrite 0185,f0

1096 SPIWrite 0186,02
1097 SPIWrite 0187,04
1098 SPIWrite 0188,02
1099 SPIWrite 0189,eb
1100 SPIWrite 018a,96
1101 SPIWrite 018b,12
1102 SPIWrite 018c,0c
1103 SPIWrite 018d,60
1104 SPIWrite 018e,0f
1105 SPIWrite 018f,e0
1106 SPIWrite 0190,34
1107 SPIWrite 0191,46
1108 SPIWrite 0192,64
1109 SPIWrite 0193,1e
1110 SPIWrite 0194,fd
1111 SPIWrite 0195,d1
1112 SPIWrite 0196,00
1113 SPIWrite 0197,bf
1114 SPIWrite 0198,5b
1115 SPIWrite 0199,1c
1116 SPIWrite 019a,1d
1117 SPIWrite 019b,e0
1118 SPIWrite 019c,37
1119 SPIWrite 019d,46
1120 SPIWrite 019e,7f
1121 SPIWrite 019f,1e
1122 SPIWrite 01a0,fd
1123 SPIWrite 01a1,d1
1124 SPIWrite 01a2,00
1125 SPIWrite 01a3,bf
1126 SPIWrite 01a4,6d
1127 SPIWrite 01a5,1c
1128 SPIWrite 01a6,13
1129 SPIWrite 01a7,e0
1130 SPIWrite 01a8,76
1131 SPIWrite 01a9,1e
1132 SPIWrite 01aa,fd
1133 SPIWrite 01ab,d1
1134 SPIWrite 01ac,00
1135 SPIWrite 01ad,bf
1136 SPIWrite 01ae,7f
1137 SPIWrite 01af,1c
1138 SPIWrite 01b0,13
1139 SPIWrite 01b1,26
1140 SPIWrite 01b2,ba
1141 SPIWrite 01b3,42
1142 SPIWrite 01b4,c0
1143 SPIWrite 01b5,f2
1144 SPIWrite 01b6,00
1145 SPIWrite 01b7,06
1146 SPIWrite 01b8,f6
1147 SPIWrite 01b9,d8
1148 SPIWrite 01ba,08
1149 SPIWrite 01bb,35
1150 SPIWrite 01bc,0c
1151 SPIWrite 01bd,68
1152 SPIWrite 01be,2f
1153 SPIWrite 01bf,68
1154 SPIWrite 01c0,44
1155 SPIWrite 01c1,f0
1156 SPIWrite 01c2,02
1157 SPIWrite 01c3,04
1158 SPIWrite 01c4,c7
1159 SPIWrite 01c5,f3
1160 SPIWrite 01c6,40
1161 SPIWrite 01c7,1c
1162 SPIWrite 01c8,1d
1163 SPIWrite 01c9,46
1164 SPIWrite 01ca,0c

1165 SPIWrite 01cb,60
1166 SPIWrite 01cc,0c
1167 SPIWrite 01cd,eb
1168 SPIWrite 01ce,97
1169 SPIWrite 01cf,14
1170 SPIWrite 01d0,ac
1171 SPIWrite 01d1,42
1172 SPIWrite 01d2,e3
1173 SPIWrite 01d3,d8
1174 SPIWrite 01d4,01
1175 SPIWrite 01d5,24
1176 SPIWrite 01d6,0c
1177 SPIWrite 01d7,75
1178 SPIWrite 01d8,9a
1179 SPIWrite 01d9,42
1180 SPIWrite 01da,d9
1181 SPIWrite 01db,d8
1182 SPIWrite 01dc,b1
1183 SPIWrite 01dd,f9
1184 SPIWrite 01de,10
1185 SPIWrite 01df,10
1186 SPIWrite 01e0,01
1187 SPIWrite 01e1,28
1188 SPIWrite 01e2,0c
1189 SPIWrite 01e3,bf
1190 SPIWrite 01e4,c1
1191 SPIWrite 01e5,f5
1192 SPIWrite 01e6,40
1193 SPIWrite 01e7,61
1194 SPIWrite 01e8,a1
1195 SPIWrite 01e9,f5
1196 SPIWrite 01ea,80
1197 SPIWrite 01eb,61
1198 SPIWrite 01ec,08
1199 SPIWrite 01ed,b2
1200 SPIWrite 01ee,f8
1201 SPIWrite 01ef,bd
1202 SPIWrite 01f0,af
1203 SPIWrite 01f1,4a
1204 SPIWrite 01f2,b2
1205 SPIWrite 01f3,f9
1206 SPIWrite 01f4,00
1207 SPIWrite 01f5,20
1208 SPIWrite 01f6,48
1209 SPIWrite 01f7,43
1210 SPIWrite 01f8,00
1211 SPIWrite 01f9,28
1212 SPIWrite 01fa,cc
1213 SPIWrite 01fb,bf
1214 SPIWrite 01fc,00
1215 SPIWrite 01fd,eb
1216 SPIWrite 01fe,62
1217 SPIWrite 01ff,00
1218 SPIWrite 0200,a0
1219 SPIWrite 0201,eb
1220 SPIWrite 0202,62
1221 SPIWrite 0203,00
1222 SPIWrite 0204,90
1223 SPIWrite 0205,fb
1224 SPIWrite 0206,f2
1225 SPIWrite 0207,f0
1226 SPIWrite 0208,70
1227 SPIWrite 0209,47
1228 SPIWrite 020a,03
1229 SPIWrite 020b,46
1230 SPIWrite 020c,00
1231 SPIWrite 020d,28
1232 SPIWrite 020e,b8
1233 SPIWrite 020f,bf

1234	SPIWrite	0210,40
1235	SPIWrite	0211,42
1236	SPIWrite	0212,49
1237	SPIWrite	0213,b2
1238	SPIWrite	0214,01
1239	SPIWrite	0215,22
1240	SPIWrite	0216,49
1241	SPIWrite	0217,1e
1242	SPIWrite	0218,c9
1243	SPIWrite	0219,b2
1244	SPIWrite	021a,8a
1245	SPIWrite	021b,40
1246	SPIWrite	021c,51
1247	SPIWrite	021d,1e
1248	SPIWrite	021e,81
1249	SPIWrite	021f,42
1250	SPIWrite	0220,38
1251	SPIWrite	0221,bf
1252	SPIWrite	0222,08
1253	SPIWrite	0223,1c
1254	SPIWrite	0224,00
1255	SPIWrite	0225,2b
1256	SPIWrite	0226,48
1257	SPIWrite	0227,bf
1258	SPIWrite	0228,10
1259	SPIWrite	0229,44
1260	SPIWrite	022a,70
1261	SPIWrite	022b,47
1262	SPIWrite	022c,c0
1263	SPIWrite	022d,00
1264	SPIWrite	022e,03
1265	SPIWrite	022f,ad
1266	SPIWrite	0230,00
1267	SPIWrite	0231,05
1268	SPIWrite	0232,02
1269	SPIWrite	0233,ac
1270	SPIWrite	0234,34
1271	SPIWrite	0235,22
1272	SPIWrite	0236,01
1273	SPIWrite	0237,20
1274	SPIWrite	0238,2d
1275	SPIWrite	0239,e9
1276	SPIWrite	023a,f0
1277	SPIWrite	023b,4f
1278	SPIWrite	023c,df
1279	SPIWrite	023d,f8
1280	SPIWrite	023e,74
1281	SPIWrite	023f,82
1282	SPIWrite	0240,d8
1283	SPIWrite	0241,f8
1284	SPIWrite	0242,00
1285	SPIWrite	0243,32
1286	SPIWrite	0244,0c
1287	SPIWrite	0245,46
1288	SPIWrite	0246,81
1289	SPIWrite	0247,46
1290	SPIWrite	0248,01
1291	SPIWrite	0249,21
1292	SPIWrite	024a,00
1293	SPIWrite	024b,20
1294	SPIWrite	024c,0a
1295	SPIWrite	024d,46
1296	SPIWrite	024e,ad
1297	SPIWrite	024f,f1
1298	SPIWrite	0250,1c
1299	SPIWrite	0251,0d
1300	SPIWrite	0252,98
1301	SPIWrite	0253,47
1302	SPIWrite	0254,ff

1303	SPIWrite	0255,f7
1304	SPIWrite	0256,fc
1305	SPIWrite	0257,fe
1306	SPIWrite	0258,48
1307	SPIWrite	0259,46
1308	SPIWrite	025a,00
1309	SPIWrite	025b,2c
1310	SPIWrite	025c,05
1311	SPIWrite	025d,94
1312	SPIWrite	025e,00
1313	SPIWrite	025f,f0
1314	SPIWrite	0260,f7
1315	SPIWrite	0261,80
1316	SPIWrite	0262,df
1317	SPIWrite	0263,f8
1318	SPIWrite	0264,54
1319	SPIWrite	0265,82
1320	SPIWrite	0266,95
1321	SPIWrite	0267,4f
1322	SPIWrite	0268,40
1323	SPIWrite	0269,1e
1324	SPIWrite	026a,4f
1325	SPIWrite	026b,f0
1326	SPIWrite	026c,00
1327	SPIWrite	026d,0b
1328	SPIWrite	026e,04
1329	SPIWrite	026f,90
1330	SPIWrite	0270,04
1331	SPIWrite	0271,98
1332	SPIWrite	0272,66
1333	SPIWrite	0273,4b
1334	SPIWrite	0274,03
1335	SPIWrite	0275,25
1336	SPIWrite	0276,06
1337	SPIWrite	0277,26
1338	SPIWrite	0278,10
1339	SPIWrite	0279,f8
1340	SPIWrite	027a,01
1341	SPIWrite	027b,cf
1342	SPIWrite	027c,04
1343	SPIWrite	027d,90
1344	SPIWrite	027e,9c
1345	SPIWrite	027f,fb
1346	SPIWrite	0280,f5
1347	SPIWrite	0281,f2
1348	SPIWrite	0282,53
1349	SPIWrite	0283,f8
1350	SPIWrite	0284,04
1351	SPIWrite	0285,1b
1352	SPIWrite	0286,d1
1353	SPIWrite	0287,f8
1354	SPIWrite	0288,18
1355	SPIWrite	0289,01
1356	SPIWrite	028a,20
1357	SPIWrite	028b,f4
1358	SPIWrite	028c,00
1359	SPIWrite	028d,70
1360	SPIWrite	028e,c1
1361	SPIWrite	028f,f8
1362	SPIWrite	0290,18
1363	SPIWrite	0291,01
1364	SPIWrite	0292,08
1365	SPIWrite	0293,6e
1366	SPIWrite	0294,76
1367	SPIWrite	0295,1e
1368	SPIWrite	0296,20
1369	SPIWrite	0297,f0
1370	SPIWrite	0298,00
1371	SPIWrite	0299,70

1372 SPIWrite 029a,08
1373 SPIWrite 029b,66
1374 SPIWrite 029c,f1
1375 SPIWrite 029d,d1
1376 SPIWrite 029e,5b
1377 SPIWrite 029f,48
1378 SPIWrite 02a0,50
1379 SPIWrite 02a1,f8
1380 SPIWrite 02a2,2c
1381 SPIWrite 02a3,40
1382 SPIWrite 02a4,d4
1383 SPIWrite 02a5,f8
1384 SPIWrite 02a6,18
1385 SPIWrite 02a7,01
1386 SPIWrite 02a8,40
1387 SPIWrite 02a9,f4
1388 SPIWrite 02aa,00
1389 SPIWrite 02ab,70
1390 SPIWrite 02ac,c4
1391 SPIWrite 02ad,f8
1392 SPIWrite 02ae,18
1393 SPIWrite 02af,01
1394 SPIWrite 02b0,20
1395 SPIWrite 02b1,6e
1396 SPIWrite 02b2,40
1397 SPIWrite 02b3,f0
1398 SPIWrite 02b4,80
1399 SPIWrite 02b5,60
1400 SPIWrite 02b6,20
1401 SPIWrite 02b7,66
1402 SPIWrite 02b8,20
1403 SPIWrite 02b9,68
1404 SPIWrite 02ba,01
1405 SPIWrite 02bb,2a
1406 SPIWrite 02bc,00
1407 SPIWrite 02bd,90
1408 SPIWrite 02be,0c
1409 SPIWrite 02bf,d0
1410 SPIWrite 02c0,d8
1411 SPIWrite 02c1,f8
1412 SPIWrite 02c2,00
1413 SPIWrite 02c3,00
1414 SPIWrite 02c4,20
1415 SPIWrite 02c5,f0
1416 SPIWrite 02c6,38
1417 SPIWrite 02c7,00
1418 SPIWrite 02c8,38
1419 SPIWrite 02c9,30
1420 SPIWrite 02ca,c8
1421 SPIWrite 02cb,f8
1422 SPIWrite 02cc,00
1423 SPIWrite 02cd,00
1424 SPIWrite 02ce,d8
1425 SPIWrite 02cf,f8
1426 SPIWrite 02d0,00
1427 SPIWrite 02d1,00
1428 SPIWrite 02d2,20
1429 SPIWrite 02d3,f0
1430 SPIWrite 02d4,07
1431 SPIWrite 02d5,00
1432 SPIWrite 02d6,c0
1433 SPIWrite 02d7,1d
1434 SPIWrite 02d8,0b
1435 SPIWrite 02d9,e0
1436 SPIWrite 02da,d8
1437 SPIWrite 02db,f8
1438 SPIWrite 02dc,00
1439 SPIWrite 02dd,00
1440 SPIWrite 02de,20

1441 SPIWrite 02df,f0
1442 SPIWrite 02e0,38
1443 SPIWrite 02e1,00
1444 SPIWrite 02e2,30
1445 SPIWrite 02e3,30
1446 SPIWrite 02e4,c8
1447 SPIWrite 02e5,f8
1448 SPIWrite 02e6,00
1449 SPIWrite 02e7,00
1450 SPIWrite 02e8,d8
1451 SPIWrite 02e9,f8
1452 SPIWrite 02ea,00
1453 SPIWrite 02eb,00
1454 SPIWrite 02ec,20
1455 SPIWrite 02ed,f0
1456 SPIWrite 02ee,07
1457 SPIWrite 02ef,00
1458 SPIWrite 02f0,80
1459 SPIWrite 02f1,1d
1460 SPIWrite 02f2,c8
1461 SPIWrite 02f3,f8
1462 SPIWrite 02f4,00
1463 SPIWrite 02f5,00
1464 SPIWrite 02f6,00
1465 SPIWrite 02f7,20
1466 SPIWrite 02f8,ff
1467 SPIWrite 02f9,f7
1468 SPIWrite 02fa,23
1469 SPIWrite 02fb,ff
1470 SPIWrite 02fc,05
1471 SPIWrite 02fd,46
1472 SPIWrite 02fe,01
1473 SPIWrite 02ff,20
1474 SPIWrite 0300,ff
1475 SPIWrite 0301,f7
1476 SPIWrite 0302,1f
1477 SPIWrite 0303,ff
1478 SPIWrite 0304,28
1479 SPIWrite 0305,49
1480 SPIWrite 0306,4d
1481 SPIWrite 0307,60
1482 SPIWrite 0308,0e
1483 SPIWrite 0309,46
1484 SPIWrite 030a,b0
1485 SPIWrite 030b,60
1486 SPIWrite 030c,21
1487 SPIWrite 030d,6e
1488 SPIWrite 030e,21
1489 SPIWrite 030f,f0
1490 SPIWrite 0310,80
1491 SPIWrite 0311,61
1492 SPIWrite 0312,21
1493 SPIWrite 0313,66
1494 SPIWrite 0314,21
1495 SPIWrite 0315,6e
1496 SPIWrite 0316,41
1497 SPIWrite 0317,f0
1498 SPIWrite 0318,00
1499 SPIWrite 0319,71
1500 SPIWrite 031a,21
1501 SPIWrite 031b,66
1502 SPIWrite 031c,61
1503 SPIWrite 031d,6e
1504 SPIWrite 031e,43
1505 SPIWrite 031f,19
1506 SPIWrite 0320,4f
1507 SPIWrite 0321,ea
1508 SPIWrite 0322,63
1509 SPIWrite 0323,0a

1510 SPIWrite 0324,00
1511 SPIWrite 0325,26
1512 SPIWrite 0326,c1
1513 SPIWrite 0327,f3
1514 SPIWrite 0328,c0
1515 SPIWrite 0329,45
1516 SPIWrite 032a,00
1517 SPIWrite 032b,2d
1518 SPIWrite 032c,5d
1519 SPIWrite 032d,d1
1520 SPIWrite 032e,35
1521 SPIWrite 032f,46
1522 SPIWrite 0330,b1
1523 SPIWrite 0331,46
1524 SPIWrite 0332,23
1525 SPIWrite 0333,e0
1526 SPIWrite 0334,28
1527 SPIWrite 0335,46
1528 SPIWrite 0336,ff
1529 SPIWrite 0337,f7
1530 SPIWrite 0338,04
1531 SPIWrite 0339,ff
1532 SPIWrite 033a,b7
1533 SPIWrite 033b,f9
1534 SPIWrite 033c,00
1535 SPIWrite 033d,10
1536 SPIWrite 033e,aa
1537 SPIWrite 033f,eb
1538 SPIWrite 0340,00
1539 SPIWrite 0341,00
1540 SPIWrite 0342,ff
1541 SPIWrite 0343,f7
1542 SPIWrite 0344,55
1543 SPIWrite 0345,ff
1544 SPIWrite 0346,36
1545 SPIWrite 0347,1a
1546 SPIWrite 0348,03
1547 SPIWrite 0349,d4
1548 SPIWrite 034a,10
1549 SPIWrite 034b,2e
1550 SPIWrite 034c,a8
1551 SPIWrite 034d,bf
1552 SPIWrite 034e,0f
1553 SPIWrite 034f,26
1554 SPIWrite 0350,04
1555 SPIWrite 0351,e0
1556 SPIWrite 0352,16
1557 SPIWrite 0353,f1
1558 SPIWrite 0354,0f
1559 SPIWrite 0355,0f
1560 SPIWrite 0356,b8
1561 SPIWrite 0357,bf
1562 SPIWrite 0358,6f
1563 SPIWrite 0359,f0
1564 SPIWrite 035a,0e
1565 SPIWrite 035b,06
1566 SPIWrite 035c,30
1567 SPIWrite 035d,46
1568 SPIWrite 035e,05
1569 SPIWrite 035f,21
1570 SPIWrite 0360,ff
1571 SPIWrite 0361,f7
1572 SPIWrite 0362,53
1573 SPIWrite 0363,ff
1574 SPIWrite 0364,d4
1575 SPIWrite 0365,f8
1576 SPIWrite 0366,80
1577 SPIWrite 0367,10
1578 SPIWrite 0368,60

1579 SPIWrite 0369,f3
1580 SPIWrite 036a,1c
1581 SPIWrite 036b,61
1582 SPIWrite 036c,c4
1583 SPIWrite 036d,f8
1584 SPIWrite 036e,80
1585 SPIWrite 036f,10
1586 SPIWrite 0370,20
1587 SPIWrite 0371,68
1588 SPIWrite 0372,09
1589 SPIWrite 0373,f1
1590 SPIWrite 0374,01
1591 SPIWrite 0375,03
1592 SPIWrite 0376,5f
1593 SPIWrite 0377,fa
1594 SPIWrite 0378,83
1595 SPIWrite 0379,f9
1596 SPIWrite 037a,01
1597 SPIWrite 037b,90
1598 SPIWrite 037c,b8
1599 SPIWrite 037d,79
1600 SPIWrite 037e,48
1601 SPIWrite 037f,45
1602 SPIWrite 0380,d8
1603 SPIWrite 0381,dc
1604 SPIWrite 0382,2e
1605 SPIWrite 0383,46
1606 SPIWrite 0384,b0
1607 SPIWrite 0385,42
1608 SPIWrite 0386,59
1609 SPIWrite 0387,dd
1610 SPIWrite 0388,01
1611 SPIWrite 0389,20
1612 SPIWrite 038a,ff
1613 SPIWrite 038b,f7
1614 SPIWrite 038c,da
1615 SPIWrite 038d,fe
1616 SPIWrite 038e,b7
1617 SPIWrite 038f,f9
1618 SPIWrite 0390,02
1619 SPIWrite 0391,10
1620 SPIWrite 0392,aa
1621 SPIWrite 0393,eb
1622 SPIWrite 0394,00
1623 SPIWrite 0395,00
1624 SPIWrite 0396,ff
1625 SPIWrite 0397,f7
1626 SPIWrite 0398,2b
1627 SPIWrite 0399,ff
1628 SPIWrite 039a,45
1629 SPIWrite 039b,19
1630 SPIWrite 039c,06
1631 SPIWrite 039d,d4
1632 SPIWrite 039e,08
1633 SPIWrite 039f,2d
1634 SPIWrite 03a0,a8
1635 SPIWrite 03a1,bf
1636 SPIWrite 03a2,07
1637 SPIWrite 03a3,25
1638 SPIWrite 03a4,07
1639 SPIWrite 03a5,e0
1640 SPIWrite 03a6,c0
1641 SPIWrite 03a7,46
1642 SPIWrite 03a8,40
1643 SPIWrite 03a9,22
1644 SPIWrite 03aa,01
1645 SPIWrite 03ab,20
1646 SPIWrite 03ac,15
1647 SPIWrite 03ad,f1

1648 SPIWrite 03ae,07
1649 SPIWrite 03af,0f
1650 SPIWrite 03b0,b8
1651 SPIWrite 03b1,bf
1652 SPIWrite 03b2,6f
1653 SPIWrite 03b3,f0
1654 SPIWrite 03b4,06
1655 SPIWrite 03b5,05
1656 SPIWrite 03b6,00
1657 SPIWrite 03b7,21
1658 SPIWrite 03b8,00
1659 SPIWrite 03b9,2d
1660 SPIWrite 03ba,d8
1661 SPIWrite 03bb,bf
1662 SPIWrite 03bc,01
1663 SPIWrite 03bd,21
1664 SPIWrite 03be,20
1665 SPIWrite 03bf,6f
1666 SPIWrite 03c0,20
1667 SPIWrite 03c1,f4
1668 SPIWrite 03c2,00
1669 SPIWrite 03c3,50
1670 SPIWrite 03c4,40
1671 SPIWrite 03c5,ea
1672 SPIWrite 03c6,41
1673 SPIWrite 03c7,30
1674 SPIWrite 03c8,20
1675 SPIWrite 03c9,67
1676 SPIWrite 03ca,29
1677 SPIWrite 03cb,46
1678 SPIWrite 03cc,00
1679 SPIWrite 03cd,29
1680 SPIWrite 03ce,b8
1681 SPIWrite 03cf,bf
1682 SPIWrite 03d0,49
1683 SPIWrite 03d1,42
1684 SPIWrite 03d2,d4
1685 SPIWrite 03d3,f8
1686 SPIWrite 03d4,84
1687 SPIWrite 03d5,00
1688 SPIWrite 03d6,61
1689 SPIWrite 03d7,f3
1690 SPIWrite 03d8,8c
1691 SPIWrite 03d9,20
1692 SPIWrite 03da,c4
1693 SPIWrite 03db,f8
1694 SPIWrite 03dc,84
1695 SPIWrite 03dd,00
1696 SPIWrite 03de,b8
1697 SPIWrite 03df,79
1698 SPIWrite 03e0,21
1699 SPIWrite 03e1,68
1700 SPIWrite 03e2,76
1701 SPIWrite 03e3,1c
1702 SPIWrite 03e4,f6
1703 SPIWrite 03e5,b2
1704 SPIWrite 03e6,02
1705 SPIWrite 03e7,91
1706 SPIWrite 03e8,cc
1707 SPIWrite 03e9,e7
1708 SPIWrite 03ea,35
1709 SPIWrite 03eb,46
1710 SPIWrite 03ec,23
1711 SPIWrite 03ed,e0
1712 SPIWrite 03ee,01
1713 SPIWrite 03ef,20
1714 SPIWrite 03f0,ff
1715 SPIWrite 03f1,f7
1716 SPIWrite 03f2,a7

1717 SPIWrite 03f3,fe
1718 SPIWrite 03f4,b7
1719 SPIWrite 03f5,f9
1720 SPIWrite 03f6,00
1721 SPIWrite 03f7,10
1722 SPIWrite 03f8,aa
1723 SPIWrite 03f9,eb
1724 SPIWrite 03fa,00
1725 SPIWrite 03fb,00
1726 SPIWrite 03fc,ff
1727 SPIWrite 03fd,f7
1728 SPIWrite 03fe,f8
1729 SPIWrite 03ff,fe
1730 SPIWrite 0400,36
1731 SPIWrite 0401,1a
1732 SPIWrite 0402,05
1733 SPIWrite 0403,d4
1734 SPIWrite 0404,10
1735 SPIWrite 0405,2e
1736 SPIWrite 0406,a8
1737 SPIWrite 0407,bf
1738 SPIWrite 0408,0f
1739 SPIWrite 0409,26
1740 SPIWrite 040a,06
1741 SPIWrite 040b,e0
1742 SPIWrite 040c,c0
1743 SPIWrite 040d,75
1744 SPIWrite 040e,02
1745 SPIWrite 040f,00
1746 SPIWrite 0410,16
1747 SPIWrite 0411,f1
1748 SPIWrite 0412,0f
1749 SPIWrite 0413,0f
1750 SPIWrite 0414,b8
1751 SPIWrite 0415,bf
1752 SPIWrite 0416,6f
1753 SPIWrite 0417,f0
1754 SPIWrite 0418,0e
1755 SPIWrite 0419,06
1756 SPIWrite 041a,30
1757 SPIWrite 041b,46
1758 SPIWrite 041c,05
1759 SPIWrite 041d,21
1760 SPIWrite 041e,ff
1761 SPIWrite 041f,f7
1762 SPIWrite 0420,f4
1763 SPIWrite 0421,fe
1764 SPIWrite 0422,d4
1765 SPIWrite 0423,f8
1766 SPIWrite 0424,80
1767 SPIWrite 0425,10
1768 SPIWrite 0426,60
1769 SPIWrite 0427,f3
1770 SPIWrite 0428,1c
1771 SPIWrite 0429,61
1772 SPIWrite 042a,c4
1773 SPIWrite 042b,f8
1774 SPIWrite 042c,80
1775 SPIWrite 042d,10
1776 SPIWrite 042e,20
1777 SPIWrite 042f,68
1778 SPIWrite 0430,6d
1779 SPIWrite 0431,1c
1780 SPIWrite 0432,ed
1781 SPIWrite 0433,b2
1782 SPIWrite 0434,03
1783 SPIWrite 0435,90
1784 SPIWrite 0436,b8
1785 SPIWrite 0437,79

1786 SPIWrite 0438,a8
1787 SPIWrite 0439,42
1788 SPIWrite 043a,d8
1789 SPIWrite 043b,dc
1790 SPIWrite 043c,20
1791 SPIWrite 043d,6e
1792 SPIWrite 043e,05
1793 SPIWrite 043f,9e
1794 SPIWrite 0440,0b
1795 SPIWrite 0441,f1
1796 SPIWrite 0442,01
1797 SPIWrite 0443,0b
1798 SPIWrite 0444,20
1799 SPIWrite 0445,f0
1800 SPIWrite 0446,00
1801 SPIWrite 0447,70
1802 SPIWrite 0448,5e
1803 SPIWrite 0449,45
1804 SPIWrite 044a,20
1805 SPIWrite 044b,66
1806 SPIWrite 044c,3f
1807 SPIWrite 044d,f7
1808 SPIWrite 044e,10
1809 SPIWrite 044f,af
1810 SPIWrite 0450,ff
1811 SPIWrite 0451,f7
1812 SPIWrite 0452,48
1813 SPIWrite 0453,fe
1814 SPIWrite 0454,17
1815 SPIWrite 0455,48
1816 SPIWrite 0456,d0
1817 SPIWrite 0457,f8
1818 SPIWrite 0458,04
1819 SPIWrite 0459,32
1820 SPIWrite 045a,01
1821 SPIWrite 045b,21
1822 SPIWrite 045c,0a
1823 SPIWrite 045d,46
1824 SPIWrite 045e,00
1825 SPIWrite 045f,20
1826 SPIWrite 0460,98
1827 SPIWrite 0461,47
1828 SPIWrite 0462,07
1829 SPIWrite 0463,b0
1830 SPIWrite 0464,bd
1831 SPIWrite 0465,e8
1832 SPIWrite 0466,f0
1833 SPIWrite 0467,8f
1834 SPIWrite 0468,5c
1835 SPIWrite 0469,22
1836 SPIWrite 046a,01
1837 SPIWrite 046b,20
1838 SPIWrite 046c,01
1839 SPIWrite 046d,22
1840 SPIWrite 046e,49
1841 SPIWrite 046f,1e
1842 SPIWrite 0470,8a
1843 SPIWrite 0471,40
1844 SPIWrite 0472,01
1845 SPIWrite 0473,46
1846 SPIWrite 0474,50
1847 SPIWrite 0475,1e
1848 SPIWrite 0476,11
1849 SPIWrite 0477,42
1850 SPIWrite 0478,01
1851 SPIWrite 0479,ea
1852 SPIWrite 047a,00
1853 SPIWrite 047b,00
1854 SPIWrite 047c,18

1855 SPIWrite 047d,bf
1856 SPIWrite 047e,40
1857 SPIWrite 047f,42
1858 SPIWrite 0480,70
1859 SPIWrite 0481,47
1860 SPIWrite 0482,01
1861 SPIWrite 0483,46
1862 SPIWrite 0484,1c
1863 SPIWrite 0485,b5
1864 SPIWrite 0486,00
1865 SPIWrite 0487,20
1866 SPIWrite 0488,01
1867 SPIWrite 0489,24
1868 SPIWrite 048a,02
1869 SPIWrite 048b,46
1870 SPIWrite 048c,04
1871 SPIWrite 048d,fa
1872 SPIWrite 048e,02
1873 SPIWrite 048f,f3
1874 SPIWrite 0490,19
1875 SPIWrite 0491,42
1876 SPIWrite 0492,03
1877 SPIWrite 0493,d0
1878 SPIWrite 0494,43
1879 SPIWrite 0495,1c
1880 SPIWrite 0496,00
1881 SPIWrite 0497,f8
1882 SPIWrite 0498,0d
1883 SPIWrite 0499,20
1884 SPIWrite 049a,d8
1885 SPIWrite 049b,b2
1886 SPIWrite 049c,52
1887 SPIWrite 049d,1c
1888 SPIWrite 049e,06
1889 SPIWrite 049f,2a
1890 SPIWrite 04a0,f4
1891 SPIWrite 04a1,db
1892 SPIWrite 04a2,18
1893 SPIWrite 04a3,b1
1894 SPIWrite 04a4,01
1895 SPIWrite 04a5,46
1896 SPIWrite 04a6,68
1897 SPIWrite 04a7,46
1898 SPIWrite 04a8,ff
1899 SPIWrite 04a9,f7
1900 SPIWrite 04aa,c6
1901 SPIWrite 04ab,fe
1902 SPIWrite 04ac,1c
1903 SPIWrite 04ad,bd
1904 SPIWrite 04ae,c0
1905 SPIWrite 04af,46
1906 SPIWrite 04b0,30
1907 SPIWrite 04b1,22
1908 SPIWrite 04b2,01
1909 SPIWrite 04b3,20
1910 SPIWrite 04b4,90
1911 SPIWrite 04b5,d6
1912 SPIWrite 04b6,00
1913 SPIWrite 04b7,20
1914 SPIWrite 04b8,04
1915 SPIWrite 04b9,05
1916 SPIWrite 04ba,02
1917 SPIWrite 04bb,ac
1918 SPIWrite 04bc,2c
1919 SPIWrite 04bd,22
1920 SPIWrite 04be,01
1921 SPIWrite 04bf,20
1922 SPIWrite 04c0,10
1923 SPIWrite 04c1,b5

1924 SPIWrite 04c2,b7
1925 SPIWrite 04c3,4b
1926 SPIWrite 04c4,b5
1927 SPIWrite 04c5,4c
1928 SPIWrite 04c6,03
1929 SPIWrite 04c7,22
1930 SPIWrite 04c8,10
1931 SPIWrite 04c9,fb
1932 SPIWrite 04ca,02
1933 SPIWrite 04cb,10
1934 SPIWrite 04cc,18
1935 SPIWrite 04cd,5c
1936 SPIWrite 04ce,20
1937 SPIWrite 04cf,5c
1938 SPIWrite 04d0,80
1939 SPIWrite 04d1,00
1940 SPIWrite 04d2,c0
1941 SPIWrite 04d3,b2
1942 SPIWrite 04d4,10
1943 SPIWrite 04d5,bd
1944 SPIWrite 04d6,2d
1945 SPIWrite 04d7,e9
1946 SPIWrite 04d8,f0
1947 SPIWrite 04d9,4f
1948 SPIWrite 04da,ad
1949 SPIWrite 04db,f1
1950 SPIWrite 04dc,34
1951 SPIWrite 04dd,0d
1952 SPIWrite 04de,08
1953 SPIWrite 04df,90
1954 SPIWrite 04e0,e8
1955 SPIWrite 04e1,f7
1956 SPIWrite 04e2,2c
1957 SPIWrite 04e3,fc
1958 SPIWrite 04e4,af
1959 SPIWrite 04e5,4a
1960 SPIWrite 04e6,06
1961 SPIWrite 04e7,27
1962 SPIWrite 04e8,10
1963 SPIWrite 04e9,46
1964 SPIWrite 04ea,00
1965 SPIWrite 04eb,21
1966 SPIWrite 04ec,7f
1967 SPIWrite 04ed,1e
1968 SPIWrite 04ee,00
1969 SPIWrite 04ef,f8
1970 SPIWrite 04f0,01
1971 SPIWrite 04f1,1b
1972 SPIWrite 04f2,fa
1973 SPIWrite 04f3,d1
1974 SPIWrite 04f4,aa
1975 SPIWrite 04f5,49
1976 SPIWrite 04f6,08
1977 SPIWrite 04f7,98
1978 SPIWrite 04f8,ac
1979 SPIWrite 04f9,4c
1980 SPIWrite 04fa,89
1981 SPIWrite 04fb,1f
1982 SPIWrite 04fc,08
1983 SPIWrite 04fd,18
1984 SPIWrite 04fe,80
1985 SPIWrite 04ff,78
1986 SPIWrite 0500,b1
1987 SPIWrite 0501,f8
1988 SPIWrite 0502,9e
1989 SPIWrite 0503,31
1990 SPIWrite 0504,20
1991 SPIWrite 0505,5c
1992 SPIWrite 0506,4f

1993	SPIWrite	0507,f0
1994	SPIWrite	0508,01
1995	SPIWrite	0509,0a
1996	SPIWrite	050a,89
1997	SPIWrite	050b,46
1998	SPIWrite	050c,58
1999	SPIWrite	050d,43
2000	SPIWrite	050e,09
2001	SPIWrite	050f,90
2002	SPIWrite	0510,a8
2003	SPIWrite	0511,48
2004	SPIWrite	0512,d0
2005	SPIWrite	0513,f8
2006	SPIWrite	0514,d8
2007	SPIWrite	0515,31
2008	SPIWrite	0516,04
2009	SPIWrite	0517,27
2010	SPIWrite	0518,51
2011	SPIWrite	0519,46
2012	SPIWrite	051a,6a
2013	SPIWrite	051b,46
2014	SPIWrite	051c,08
2015	SPIWrite	051d,98
2016	SPIWrite	051e,8d
2017	SPIWrite	051f,f8
2018	SPIWrite	0520,00
2019	SPIWrite	0521,70
2020	SPIWrite	0522,98
2021	SPIWrite	0523,47
2022	SPIWrite	0524,ad
2023	SPIWrite	0525,f1
2024	SPIWrite	0526,01
2025	SPIWrite	0527,06
2026	SPIWrite	0528,02
2027	SPIWrite	0529,96
2028	SPIWrite	052a,02
2029	SPIWrite	052b,20
2030	SPIWrite	052c,06
2031	SPIWrite	052d,90
2032	SPIWrite	052e,02
2033	SPIWrite	052f,98
2034	SPIWrite	0530,10
2035	SPIWrite	0531,f8
2036	SPIWrite	0532,01
2037	SPIWrite	0533,1f
2038	SPIWrite	0534,04
2039	SPIWrite	0535,29
2040	SPIWrite	0536,02
2041	SPIWrite	0537,90
2042	SPIWrite	0538,00
2043	SPIWrite	0539,f0
2044	SPIWrite	053a,90
2045	SPIWrite	053b,80
2046	SPIWrite	053c,9d
2047	SPIWrite	053d,48
2048	SPIWrite	053e,08
2049	SPIWrite	053f,9c
2050	SPIWrite	0540,d0
2051	SPIWrite	0541,f8
2052	SPIWrite	0542,f8
2053	SPIWrite	0543,21
2054	SPIWrite	0544,20
2055	SPIWrite	0545,46
2056	SPIWrite	0546,90
2057	SPIWrite	0547,47
2058	SPIWrite	0548,4f
2059	SPIWrite	0549,f0
2060	SPIWrite	054a,0d
2061	SPIWrite	054b,0b

2062 SPIWrite 054c,98
2063 SPIWrite 054d,49
2064 SPIWrite 054e,0a
2065 SPIWrite 054f,90
2066 SPIWrite 0550,0b
2067 SPIWrite 0551,fb
2068 SPIWrite 0552,00
2069 SPIWrite 0553,fb
2070 SPIWrite 0554,40
2071 SPIWrite 0555,18
2072 SPIWrite 0556,80
2073 SPIWrite 0557,7a
2074 SPIWrite 0558,0f
2075 SPIWrite 0559,46
2076 SPIWrite 055a,0b
2077 SPIWrite 055b,eb
2078 SPIWrite 055c,07
2079 SPIWrite 055d,01
2080 SPIWrite 055e,0b
2081 SPIWrite 055f,90
2082 SPIWrite 0560,91
2083 SPIWrite 0561,f8
2084 SPIWrite 0562,22
2085 SPIWrite 0563,00
2086 SPIWrite 0564,ba
2087 SPIWrite 0565,f1
2088 SPIWrite 0566,01
2089 SPIWrite 0567,0f
2090 SPIWrite 0568,0c
2091 SPIWrite 0569,90
2092 SPIWrite 056a,4f
2093 SPIWrite 056b,ea
2094 SPIWrite 056c,44
2095 SPIWrite 056d,00
2096 SPIWrite 056e,0a
2097 SPIWrite 056f,eb
2098 SPIWrite 0570,00
2099 SPIWrite 0571,02
2100 SPIWrite 0572,0a
2101 SPIWrite 0573,eb
2102 SPIWrite 0574,00
2103 SPIWrite 0575,01
2104 SPIWrite 0576,a2
2105 SPIWrite 0577,f1
2106 SPIWrite 0578,01
2107 SPIWrite 0579,02
2108 SPIWrite 057a,a1
2109 SPIWrite 057b,f1
2110 SPIWrite 057c,01
2111 SPIWrite 057d,01
2112 SPIWrite 057e,d3
2113 SPIWrite 057f,b2
2114 SPIWrite 0580,c9
2115 SPIWrite 0581,b2
2116 SPIWrite 0582,4f
2117 SPIWrite 0583,ea
2118 SPIWrite 0584,61
2119 SPIWrite 0585,02
2120 SPIWrite 0586,0c
2121 SPIWrite 0587,bf
2122 SPIWrite 0588,02
2123 SPIWrite 0589,21
2124 SPIWrite 058a,01
2125 SPIWrite 058b,21
2126 SPIWrite 058c,8d
2127 SPIWrite 058d,f8
2128 SPIWrite 058e,04
2129 SPIWrite 058f,30
2130 SPIWrite 0590,09

2131	SPIWrite	0591,18
2132	SPIWrite	0592,49
2133	SPIWrite	0593,1e
2134	SPIWrite	0594,09
2135	SPIWrite	0595,eb
2136	SPIWrite	0596,02
2137	SPIWrite	0597,00
2138	SPIWrite	0598,90
2139	SPIWrite	0599,f8
2140	SPIWrite	059a,ed
2141	SPIWrite	059b,70
2142	SPIWrite	059c,8d
2143	SPIWrite	059d,f8
2144	SPIWrite	059e,05
2145	SPIWrite	059f,10
2146	SPIWrite	05a0,00
2147	SPIWrite	05a1,2f
2148	SPIWrite	05a2,0c
2149	SPIWrite	05a3,bf
2150	SPIWrite	05a4,01
2151	SPIWrite	05a5,20
2152	SPIWrite	05a6,02
2153	SPIWrite	05a7,20
2154	SPIWrite	05a8,07
2155	SPIWrite	05a9,90
2156	SPIWrite	05aa,0d
2157	SPIWrite	05ab,f1
2158	SPIWrite	05ac,03
2159	SPIWrite	05ad,00
2160	SPIWrite	05ae,03
2161	SPIWrite	05af,90
2162	SPIWrite	05b0,03
2163	SPIWrite	05b1,98
2164	SPIWrite	05b2,10
2165	SPIWrite	05b3,f8
2166	SPIWrite	05b4,01
2167	SPIWrite	05b5,6f
2168	SPIWrite	05b6,03
2169	SPIWrite	05b7,90
2170	SPIWrite	05b8,06
2171	SPIWrite	05b9,eb
2172	SPIWrite	05ba,09
2173	SPIWrite	05bb,01
2174	SPIWrite	05bc,91
2175	SPIWrite	05bd,f8
2176	SPIWrite	05be,6e
2177	SPIWrite	05bf,00
2178	SPIWrite	05c0,40
2179	SPIWrite	05c1,1c
2180	SPIWrite	05c2,c7
2181	SPIWrite	05c3,b2
2182	SPIWrite	05c4,00
2183	SPIWrite	05c5,2f
2184	SPIWrite	05c6,45
2185	SPIWrite	05c7,d0
2186	SPIWrite	05c8,7b
2187	SPIWrite	05c9,48
2188	SPIWrite	05ca,dd
2189	SPIWrite	05cb,f8
2190	SPIWrite	05cc,28
2191	SPIWrite	05cd,80
2192	SPIWrite	05ce,75
2193	SPIWrite	05cf,4d
2194	SPIWrite	05d0,e1
2195	SPIWrite	05d1,31
2196	SPIWrite	05d2,00
2197	SPIWrite	05d3,24
2198	SPIWrite	05d4,04
2199	SPIWrite	05d5,91

2200	SPIWrite	05d6,30
2201	SPIWrite	05d7,18
2202	SPIWrite	05d8,11
2203	SPIWrite	05d9,30
2204	SPIWrite	05da,a8
2205	SPIWrite	05db,44
2206	SPIWrite	05dc,05
2207	SPIWrite	05dd,90
2208	SPIWrite	05de,05
2209	SPIWrite	05df,98
2210	SPIWrite	05e0,04
2211	SPIWrite	05e1,99
2212	SPIWrite	05e2,03
2213	SPIWrite	05e3,78
2214	SPIWrite	05e4,98
2215	SPIWrite	05e5,f8
2216	SPIWrite	05e6,00
2217	SPIWrite	05e7,50
2218	SPIWrite	05e8,08
2219	SPIWrite	05e9,78
2220	SPIWrite	05ea,23
2221	SPIWrite	05eb,b1
2222	SPIWrite	05ec,72
2223	SPIWrite	05ed,48
2224	SPIWrite	05ee,04
2225	SPIWrite	05ef,eb
2226	SPIWrite	05f0,46
2227	SPIWrite	05f1,01
2228	SPIWrite	05f2,40
2229	SPIWrite	05f3,18
2230	SPIWrite	05f4,40
2231	SPIWrite	05f5,7d
2232	SPIWrite	05f6,0c
2233	SPIWrite	05f7,99
2234	SPIWrite	05f8,a9
2235	SPIWrite	05f9,42
2236	SPIWrite	05fa,27
2237	SPIWrite	05fb,dd
2238	SPIWrite	05fc,0b
2239	SPIWrite	05fd,99
2240	SPIWrite	05fe,81
2241	SPIWrite	05ff,42
2242	SPIWrite	0600,24
2243	SPIWrite	0601,d1
2244	SPIWrite	0602,6c
2245	SPIWrite	0603,49
2246	SPIWrite	0604,d1
2247	SPIWrite	0605,f8
2248	SPIWrite	0606,2c
2249	SPIWrite	0607,c4
2250	SPIWrite	0608,99
2251	SPIWrite	0609,f8
2252	SPIWrite	060a,cc
2253	SPIWrite	060b,30
2254	SPIWrite	060c,0b
2255	SPIWrite	060d,9a
2256	SPIWrite	060e,e0
2257	SPIWrite	060f,00
2258	SPIWrite	0610,00
2259	SPIWrite	0611,eb
2260	SPIWrite	0612,06
2261	SPIWrite	0613,10
2262	SPIWrite	0614,48
2263	SPIWrite	0615,44
2264	SPIWrite	0616,09
2265	SPIWrite	0617,99
2266	SPIWrite	0618,c0
2267	SPIWrite	0619,68
2268	SPIWrite	061a,e0

2269 SPIWrite 061b,47
2270 SPIWrite 061c,64
2271 SPIWrite 061d,49
2272 SPIWrite 061e,4f
2273 SPIWrite 061f,f4
2274 SPIWrite 0620,7a
2275 SPIWrite 0621,72
2276 SPIWrite 0622,b0
2277 SPIWrite 0623,fb
2278 SPIWrite 0624,f2
2279 SPIWrite 0625,f0
2280 SPIWrite 0626,59
2281 SPIWrite 0627,44
2282 SPIWrite 0628,01
2283 SPIWrite 0629,eb
2284 SPIWrite 062a,45
2285 SPIWrite 062b,01
2286 SPIWrite 062c,a1
2287 SPIWrite 062d,f8
2288 SPIWrite 062e,23
2289 SPIWrite 062f,00
2290 SPIWrite 0630,08
2291 SPIWrite 0631,98
2292 SPIWrite 0632,51
2293 SPIWrite 0633,46
2294 SPIWrite 0634,ff
2295 SPIWrite 0635,f7
2296 SPIWrite 0636,44
2297 SPIWrite 0637,ff
2298 SPIWrite 0638,5d
2299 SPIWrite 0639,49
2300 SPIWrite 063a,98
2301 SPIWrite 063b,f8
2302 SPIWrite 063c,00
2303 SPIWrite 063d,30
2304 SPIWrite 063e,59
2305 SPIWrite 063f,44
2306 SPIWrite 0640,6d
2307 SPIWrite 0641,18
2308 SPIWrite 0642,85
2309 SPIWrite 0643,f8
2310 SPIWrite 0644,2b
2311 SPIWrite 0645,00
2312 SPIWrite 0646,59
2313 SPIWrite 0647,1c
2314 SPIWrite 0648,88
2315 SPIWrite 0649,f8
2316 SPIWrite 064a,00
2317 SPIWrite 064b,10
2318 SPIWrite 064c,7f
2319 SPIWrite 064d,1e
2320 SPIWrite 064e,04
2321 SPIWrite 064f,f1
2322 SPIWrite 0650,01
2323 SPIWrite 0651,04
2324 SPIWrite 0652,c4
2325 SPIWrite 0653,d1
2326 SPIWrite 0654,07
2327 SPIWrite 0655,98
2328 SPIWrite 0656,40
2329 SPIWrite 0657,1e
2330 SPIWrite 0658,07
2331 SPIWrite 0659,90
2332 SPIWrite 065a,a9
2333 SPIWrite 065b,d1
2334 SPIWrite 065c,06
2335 SPIWrite 065d,98
2336 SPIWrite 065e,40
2337 SPIWrite 065f,1e

2338 SPIWrite 0660,06
2339 SPIWrite 0661,90
2340 SPIWrite 0662,7f
2341 SPIWrite 0663,f4
2342 SPIWrite 0664,64
2343 SPIWrite 0665,af
2344 SPIWrite 0666,0a
2345 SPIWrite 0667,f1
2346 SPIWrite 0668,01
2347 SPIWrite 0669,0a
2348 SPIWrite 066a,ba
2349 SPIWrite 066b,f1
2350 SPIWrite 066c,03
2351 SPIWrite 066d,0f
2352 SPIWrite 066e,ff
2353 SPIWrite 066f,f6
2354 SPIWrite 0670,4f
2355 SPIWrite 0671,af
2356 SPIWrite 0672,0d
2357 SPIWrite 0673,b0
2358 SPIWrite 0674,bd
2359 SPIWrite 0675,e8
2360 SPIWrite 0676,f0
2361 SPIWrite 0677,8f
2362 SPIWrite 0678,2d
2363 SPIWrite 0679,e9
2364 SPIWrite 067a,f0
2365 SPIWrite 067b,4f
2366 SPIWrite 067c,81
2367 SPIWrite 067d,46
2368 SPIWrite 067e,ad
2369 SPIWrite 067f,f1
2370 SPIWrite 0680,24
2371 SPIWrite 0681,0d
2372 SPIWrite 0682,e8
2373 SPIWrite 0683,f7
2374 SPIWrite 0684,51
2375 SPIWrite 0685,fc
2376 SPIWrite 0686,48
2377 SPIWrite 0687,4c
2378 SPIWrite 0688,4a
2379 SPIWrite 0689,4f
2380 SPIWrite 068a,48
2381 SPIWrite 068b,4a
2382 SPIWrite 068c,05
2383 SPIWrite 068d,90
2384 SPIWrite 068e,04
2385 SPIWrite 068f,eb
2386 SPIWrite 0690,09
2387 SPIWrite 0691,00
2388 SPIWrite 0692,d7
2389 SPIWrite 0693,f8
2390 SPIWrite 0694,d8
2391 SPIWrite 0695,31
2392 SPIWrite 0696,b4
2393 SPIWrite 0697,f8
2394 SPIWrite 0698,9e
2395 SPIWrite 0699,61
2396 SPIWrite 069a,01
2397 SPIWrite 069b,79
2398 SPIWrite 069c,04
2399 SPIWrite 069d,20
2400 SPIWrite 069e,55
2401 SPIWrite 069f,5c
2402 SPIWrite 06a0,8d
2403 SPIWrite 06a1,f8
2404 SPIWrite 06a2,00
2405 SPIWrite 06a3,00
2406 SPIWrite 06a4,00

2407 SPIWrite 06a5,21
2408 SPIWrite 06a6,48
2409 SPIWrite 06a7,46
2410 SPIWrite 06a8,6a
2411 SPIWrite 06a9,46
2412 SPIWrite 06aa,98
2413 SPIWrite 06ab,47
2414 SPIWrite 06ac,4f
2415 SPIWrite 06ad,f0
2416 SPIWrite 06ae,02
2417 SPIWrite 06af,0b
2418 SPIWrite 06b0,75
2419 SPIWrite 06b1,43
2420 SPIWrite 06b2,ad
2421 SPIWrite 06b3,f1
2422 SPIWrite 06b4,01
2423 SPIWrite 06b5,00
2424 SPIWrite 06b6,06
2425 SPIWrite 06b7,95
2426 SPIWrite 06b8,df
2427 SPIWrite 06b9,f8
2428 SPIWrite 06ba,f4
2429 SPIWrite 06bb,a0
2430 SPIWrite 06bc,01
2431 SPIWrite 06bd,90
2432 SPIWrite 06be,09
2433 SPIWrite 06bf,eb
2434 SPIWrite 06c0,04
2435 SPIWrite 06c1,00
2436 SPIWrite 06c2,02
2437 SPIWrite 06c3,90
2438 SPIWrite 06c4,01
2439 SPIWrite 06c5,98
2440 SPIWrite 06c6,10
2441 SPIWrite 06c7,f8
2442 SPIWrite 06c8,01
2443 SPIWrite 06c9,1f
2444 SPIWrite 06ca,04
2445 SPIWrite 06cb,29
2446 SPIWrite 06cc,01
2447 SPIWrite 06cd,90
2448 SPIWrite 06ce,5e
2449 SPIWrite 06cf,d0
2450 SPIWrite 06d0,38
2451 SPIWrite 06d1,48
2452 SPIWrite 06d2,d0
2453 SPIWrite 06d3,f8
2454 SPIWrite 06d4,f8
2455 SPIWrite 06d5,21
2456 SPIWrite 06d6,48
2457 SPIWrite 06d7,46
2458 SPIWrite 06d8,90
2459 SPIWrite 06d9,47
2460 SPIWrite 06da,01
2461 SPIWrite 06db,46
2462 SPIWrite 06dc,02
2463 SPIWrite 06dd,98
2464 SPIWrite 06de,4f
2465 SPIWrite 06df,f0
2466 SPIWrite 06e0,0d
2467 SPIWrite 06e1,08
2468 SPIWrite 06e2,01
2469 SPIWrite 06e3,eb
2470 SPIWrite 06e4,0a
2471 SPIWrite 06e5,03
2472 SPIWrite 06e6,08
2473 SPIWrite 06e7,fb
2474 SPIWrite 06e8,01
2475 SPIWrite 06e9,f8

2476 SPIWrite 06ea,08
2477 SPIWrite 06eb,eb
2478 SPIWrite 06ec,0a
2479 SPIWrite 06ed,02
2480 SPIWrite 06ee,9b
2481 SPIWrite 06ef,7a
2482 SPIWrite 06f0,90
2483 SPIWrite 06f1,f8
2484 SPIWrite 06f2,df
2485 SPIWrite 06f3,00
2486 SPIWrite 06f4,92
2487 SPIWrite 06f5,f8
2488 SPIWrite 06f6,22
2489 SPIWrite 06f7,20
2490 SPIWrite 06f8,07
2491 SPIWrite 06f9,93
2492 SPIWrite 06fa,40
2493 SPIWrite 06fb,1c
2494 SPIWrite 06fc,c7
2495 SPIWrite 06fd,b2
2496 SPIWrite 06fe,08
2497 SPIWrite 06ff,92
2498 SPIWrite 0700,00
2499 SPIWrite 0701,2f
2500 SPIWrite 0702,44
2501 SPIWrite 0703,d0
2502 SPIWrite 0704,02
2503 SPIWrite 0705,9a
2504 SPIWrite 0706,2c
2505 SPIWrite 0707,48
2506 SPIWrite 0708,26
2507 SPIWrite 0709,4d
2508 SPIWrite 070a,00
2509 SPIWrite 070b,26
2510 SPIWrite 070c,e5
2511 SPIWrite 070d,32
2512 SPIWrite 070e,48
2513 SPIWrite 070f,44
2514 SPIWrite 0710,6d
2515 SPIWrite 0711,18
2516 SPIWrite 0712,03
2517 SPIWrite 0713,92
2518 SPIWrite 0714,21
2519 SPIWrite 0715,30
2520 SPIWrite 0716,04
2521 SPIWrite 0717,90
2522 SPIWrite 0718,04
2523 SPIWrite 0719,98
2524 SPIWrite 071a,03
2525 SPIWrite 071b,9a
2526 SPIWrite 071c,03
2527 SPIWrite 071d,78
2528 SPIWrite 071e,2c
2529 SPIWrite 071f,78
2530 SPIWrite 0720,10
2531 SPIWrite 0721,78
2532 SPIWrite 0722,2b
2533 SPIWrite 0723,b1
2534 SPIWrite 0724,24
2535 SPIWrite 0725,48
2536 SPIWrite 0726,06
2537 SPIWrite 0727,eb
2538 SPIWrite 0728,89
2539 SPIWrite 0729,01
2540 SPIWrite 072a,40
2541 SPIWrite 072b,18
2542 SPIWrite 072c,90
2543 SPIWrite 072d,f8
2544 SPIWrite 072e,23

2545 SPIWrite 072f,00
2546 SPIWrite 0730,08
2547 SPIWrite 0731,99
2548 SPIWrite 0732,a1
2549 SPIWrite 0733,42
2550 SPIWrite 0734,27
2551 SPIWrite 0735,dd
2552 SPIWrite 0736,07
2553 SPIWrite 0737,99
2554 SPIWrite 0738,81
2555 SPIWrite 0739,42
2556 SPIWrite 073a,24
2557 SPIWrite 073b,d1
2558 SPIWrite 073c,1d
2559 SPIWrite 073d,4b
2560 SPIWrite 073e,1a
2561 SPIWrite 073f,48
2562 SPIWrite 0740,d3
2563 SPIWrite 0741,f8
2564 SPIWrite 0742,2c
2565 SPIWrite 0743,c4
2566 SPIWrite 0744,07
2567 SPIWrite 0745,9a
2568 SPIWrite 0746,b1
2569 SPIWrite 0747,00
2570 SPIWrite 0748,01
2571 SPIWrite 0749,eb
2572 SPIWrite 074a,09
2573 SPIWrite 074b,11
2574 SPIWrite 074c,40
2575 SPIWrite 074d,18
2576 SPIWrite 074e,16
2577 SPIWrite 074f,49
2578 SPIWrite 0750,c0
2579 SPIWrite 0751,6c
2580 SPIWrite 0752,91
2581 SPIWrite 0753,f8
2582 SPIWrite 0754,ce
2583 SPIWrite 0755,30
2584 SPIWrite 0756,06
2585 SPIWrite 0757,99
2586 SPIWrite 0758,e0
2587 SPIWrite 0759,47
2588 SPIWrite 075a,08
2589 SPIWrite 075b,eb
2590 SPIWrite 075c,0a
2591 SPIWrite 075d,01
2592 SPIWrite 075e,4f
2593 SPIWrite 075f,f4
2594 SPIWrite 0760,7a
2595 SPIWrite 0761,72
2596 SPIWrite 0762,01
2597 SPIWrite 0763,eb
2598 SPIWrite 0764,44
2599 SPIWrite 0765,01
2600 SPIWrite 0766,b0
2601 SPIWrite 0767,fb
2602 SPIWrite 0768,f2
2603 SPIWrite 0769,f0
2604 SPIWrite 076a,a1
2605 SPIWrite 076b,f8
2606 SPIWrite 076c,23
2607 SPIWrite 076d,00
2608 SPIWrite 076e,00
2609 SPIWrite 076f,21
2610 SPIWrite 0770,48
2611 SPIWrite 0771,46
2612 SPIWrite 0772,ff
2613 SPIWrite 0773,f7

2614 SPIWrite 0774,a5
2615 SPIWrite 0775,fe
2616 SPIWrite 0776,2b
2617 SPIWrite 0777,78
2618 SPIWrite 0778,08
2619 SPIWrite 0779,eb
2620 SPIWrite 077a,0a
2621 SPIWrite 077b,01
2622 SPIWrite 077c,64
2623 SPIWrite 077d,18
2624 SPIWrite 077e,84
2625 SPIWrite 077f,f8
2626 SPIWrite 0780,2b
2627 SPIWrite 0781,00
2628 SPIWrite 0782,59
2629 SPIWrite 0783,1c
2630 SPIWrite 0784,29
2631 SPIWrite 0785,70
2632 SPIWrite 0786,7f
2633 SPIWrite 0787,1e
2634 SPIWrite 0788,06
2635 SPIWrite 0789,f1
2636 SPIWrite 078a,01
2637 SPIWrite 078b,06
2638 SPIWrite 078c,c4
2639 SPIWrite 078d,d1
2640 SPIWrite 078e,bb
2641 SPIWrite 078f,f1
2642 SPIWrite 0790,01
2643 SPIWrite 0791,0b
2644 SPIWrite 0792,97
2645 SPIWrite 0793,d1
2646 SPIWrite 0794,05
2647 SPIWrite 0795,98
2648 SPIWrite 0796,09
2649 SPIWrite 0797,b0
2650 SPIWrite 0798,bd
2651 SPIWrite 0799,e8
2652 SPIWrite 079a,f0
2653 SPIWrite 079b,8f
2654 SPIWrite 079c,31
2655 SPIWrite 079d,78
2656 SPIWrite 079e,02
2657 SPIWrite 079f,00
2658 SPIWrite 07a0,ba
2659 SPIWrite 07a1,01
2660 SPIWrite 07a2,01
2661 SPIWrite 07a3,20
2662 SPIWrite 07a4,54
2663 SPIWrite 07a5,22
2664 SPIWrite 07a6,01
2665 SPIWrite 07a7,20
2666 SPIWrite 07a8,b4
2667 SPIWrite 07a9,01
2668 SPIWrite 07aa,01
2669 SPIWrite 07ab,20
2670 SPIWrite 07ac,ac
2671 SPIWrite 07ad,78
2672 SPIWrite 07ae,02
2673 SPIWrite 07af,00
2674 SPIWrite 07b0,98
2675 SPIWrite 07b1,0e
2676 SPIWrite 07b2,01
2677 SPIWrite 07b3,20
2678 SPIWrite 07b4,90
2679 SPIWrite 07b5,d6
2680 SPIWrite 07b6,00
2681 SPIWrite 07b7,20
2682 SPIWrite 07b8,a0

2683 SPIWrite 07b9,13
2684 SPIWrite 07ba,01
2685 SPIWrite 07bb,20
2686 SPIWrite 07bc,2d
2687 SPIWrite 07bd,e9
2688 SPIWrite 07be,f8
2689 SPIWrite 07bf,4f
2690 SPIWrite 07c0,89
2691 SPIWrite 07c1,46
2692 SPIWrite 07c2,a5
2693 SPIWrite 07c3,4a
2694 SPIWrite 07c4,a5
2695 SPIWrite 07c5,49
2696 SPIWrite 07c6,80
2697 SPIWrite 07c7,46
2698 SPIWrite 07c8,4f
2699 SPIWrite 07c9,ea
2700 SPIWrite 07ca,68
2701 SPIWrite 07cb,00
2702 SPIWrite 07cc,a1
2703 SPIWrite 07cd,4b
2704 SPIWrite 07ce,12
2705 SPIWrite 07cf,5c
2706 SPIWrite 07d0,09
2707 SPIWrite 07d1,88
2708 SPIWrite 07d2,a4
2709 SPIWrite 07d3,48
2710 SPIWrite 07d4,9c
2711 SPIWrite 07d5,5c
2712 SPIWrite 07d6,00
2713 SPIWrite 07d7,68
2714 SPIWrite 07d8,a1
2715 SPIWrite 07d9,4a
2716 SPIWrite 07da,03
2717 SPIWrite 07db,46
2718 SPIWrite 07dc,4c
2719 SPIWrite 07dd,43
2720 SPIWrite 07de,02
2721 SPIWrite 07df,eb
2722 SPIWrite 07e0,c8
2723 SPIWrite 07e1,02
2724 SPIWrite 07e2,01
2725 SPIWrite 07e3,20
2726 SPIWrite 07e4,21
2727 SPIWrite 07e5,46
2728 SPIWrite 07e6,98
2729 SPIWrite 07e7,47
2730 SPIWrite 07e8,df
2731 SPIWrite 07e9,f8
2732 SPIWrite 07ea,7c
2733 SPIWrite 07eb,c2
2734 SPIWrite 07ec,4f
2735 SPIWrite 07ed,ea
2736 SPIWrite 07ee,08
2737 SPIWrite 07ef,1a
2738 SPIWrite 07f0,00
2739 SPIWrite 07f1,25
2740 SPIWrite 07f2,56
2741 SPIWrite 07f3,46
2742 SPIWrite 07f4,22
2743 SPIWrite 07f5,46
2744 SPIWrite 07f6,02
2745 SPIWrite 07f7,24
2746 SPIWrite 07f8,4f
2747 SPIWrite 07f9,ea
2748 SPIWrite 07fa,12
2749 SPIWrite 07fb,1e
2750 SPIWrite 07fc,0a
2751 SPIWrite 07fd,eb


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2752 SPIWrite 07fe,05
2753 SPIWrite 07ff,03
2754 SPIWrite 0800,06
2755 SPIWrite 0801,eb
2756 SPIWrite 0802,0c
2757 SPIWrite 0803,00
2758 SPIWrite 0804,02
2759 SPIWrite 0805,27
2760 SPIWrite 0806,63
2761 SPIWrite 0807,44
2762 SPIWrite 0808,90
2763 SPIWrite 0809,30
2764 SPIWrite 080a,03
2765 SPIWrite 080b,f5
2766 SPIWrite 080c,20
2767 SPIWrite 080d,7b
2768 SPIWrite 080e,50
2769 SPIWrite 080f,f8
2770 SPIWrite 0810,04
2771 SPIWrite 0811,3b
2772 SPIWrite 0812,19
2773 SPIWrite 0813,01
2774 SPIWrite 0814,7f
2775 SPIWrite 0815,1e
2776 SPIWrite 0816,b1
2777 SPIWrite 0817,fb
2778 SPIWrite 0818,f2
2779 SPIWrite 0819,f1
2780 SPIWrite 081a,0e
2781 SPIWrite 081b,fb
2782 SPIWrite 081c,11
2783 SPIWrite 081d,31
2784 SPIWrite 081e,4b
2785 SPIWrite 081f,f8
2786 SPIWrite 0018,00 //sys_calib_macro_memory=0x0; Address(0x18[7:0])
2787 SPIWrite 0018,20 //macro=0x1; Address(0x18[7:5])
2788 SPIRead 00f0
2789
2790 //Read MACRO_READY=0x1; Address(0xf0[7:0])
2791
2792
2793 SPIPoll 00f0,0,0,1
2794
2795 SPIWrite 00a3,08 //MACRO_OPERAND_REG0=0x8000000;
Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
2796 SPIWrite 00a2,00
2797 SPIWrite 00a1,00
2798 SPIWrite 00a0,00
2799 SPIWrite 00a7,00 //MACRO_OPERAND_REG1=0x0;
Address(0xa4[7:0],0xa5[7:0],0xa6[7:0],0xa7[7:0],0xa8[7:0])
2800 SPIWrite 00a6,00
2801 SPIWrite 00a5,00
2802 SPIWrite 00a4,00
2803 SPIWrite 0193,78 //MACRO_OPCODE=0x78; Address(0x193[7:0],0x194[7:0])
2804
2805 WAIT 0.001
2806 SPIRead 00f0
2807
2808 //Read MACRO_DONE=0x1; Address(0xf0[7:2])
2809
2810
2811 SPIPoll 00f0,2,2,4
2812
2813 SPIRead 00f0
2814
2815 //Read MACRO_ERROR=0x0; Address(0xf0[7:3])
2816
2817 SPIRead 00f1
2818
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2819 //Read  MACRO_ERROR_OPCODE=0x0;      Address(0xf1[7:0],0xf2[7:0])
2820
2821 SPIRead 00f0
2822
2823 //Read  MACRO_ERROR_IN_OPCODE=0x0;   Address(0xf0[7:4])
2824
2825 SPIRead 00f0
2826
2827 //Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;      Address(0xf0[7:5])
2828
2829 SPIRead 00f0
2830
2831 //Read  MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])
2832
2833 SPIRead 00f0
2834
2835 //Read  MACRO_ERROR_IN_EXECUTION=0x0;   Address(0xf0[7:7])
2836
2837 SPIRead 00f3
2838 SPIRead 00f2
2839
2840 //Read  MACRO_ERROR_EXTENDED_CODE=0x0;   Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
2841
2842 SPIRead 00f7
2843 SPIRead 00f6
2844 SPIRead 00f5
2845 SPIRead 00f4
2846
2847 //Read  MACRO_ERROR_EXTENDED_CODE_2=0x0;
Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
2848
2849 SPIWrite 0144,00 //all_addr_high=0x0;      Address(0x144[7:2])
2850 SPIWrite 0018,00 //macro=0x0;      Address(0x18[7:5])
2851 SPIWrite 0018,01 //sys_calib_macro_memory=0x1;   Address(0x18[7:0])
2852 SPIWrite 0020,08
2853 SPIWrite 0021,1b
2854 SPIWrite 0022,f4
2855 SPIWrite 0023,d1
2856 SPIWrite 0024,64
2857 SPIWrite 0025,1e
2858 SPIWrite 0026,06
2859 SPIWrite 0027,f1
2860 SPIWrite 0028,08
2861 SPIWrite 0029,06
2862 SPIWrite 002a,05
2863 SPIWrite 002b,f1
2864 SPIWrite 002c,04
2865 SPIWrite 002d,05
2866 SPIWrite 002e,e5
2867 SPIWrite 002f,d1
2868 SPIWrite 0030,40
2869 SPIWrite 0031,46
2870 SPIWrite 0032,49
2871 SPIWrite 0033,46
2872 SPIWrite 0034,e2
2873 SPIWrite 0035,f7
2874 SPIWrite 0036,7c
2875 SPIWrite 0037,f9
2876 SPIWrite 0038,bd
2877 SPIWrite 0039,e8
2878 SPIWrite 003a,f8
2879 SPIWrite 003b,8f
2880 SPIWrite 003c,70
2881 SPIWrite 003d,b5
2882 SPIWrite 003e,02
2883 SPIWrite 003f,46
2884 SPIWrite 0040,d2
2885 SPIWrite 0041,f8
2886 SPIWrite 0042,a4
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2887 SPIWrite 0043,60
2888 SPIWrite 0044,d2
2889 SPIWrite 0045,f8
2890 SPIWrite 0046,44
2891 SPIWrite 0047,51
2892 SPIWrite 0048,d2
2893 SPIWrite 0049,f8
2894 SPIWrite 004a,04
2895 SPIWrite 004b,41
2896 SPIWrite 004c,08
2897 SPIWrite 004d,46
2898 SPIWrite 004e,02
2899 SPIWrite 004f,28
2900 SPIWrite 0050,0d
2901 SPIWrite 0051,db
2902 SPIWrite 0052,40
2903 SPIWrite 0053,1e
2904 SPIWrite 0054,01
2905 SPIWrite 0055,21
2906 SPIWrite 0056,02
2907 SPIWrite 0057,eb
2908 SPIWrite 0058,81
2909 SPIWrite 0059,03
2910 SPIWrite 005a,c3
2911 SPIWrite 005b,f8
2912 SPIWrite 005c,a4
2913 SPIWrite 005d,60
2914 SPIWrite 005e,40
2915 SPIWrite 005f,1e
2916 SPIWrite 0060,c3
2917 SPIWrite 0061,f8
2918 SPIWrite 0062,44
2919 SPIWrite 0063,51
2920 SPIWrite 0064,01
2921 SPIWrite 0065,f1
2922 SPIWrite 0066,01
2923 SPIWrite 0067,01
2924 SPIWrite 0068,c3
2925 SPIWrite 0069,f8
2926 SPIWrite 006a,04
2927 SPIWrite 006b,41
2928 SPIWrite 006c,f3
2929 SPIWrite 006d,d1
2930 SPIWrite 006e,70
2931 SPIWrite 006f,bd
2932 SPIWrite 0070,10
2933 SPIWrite 0071,b5
2934 SPIWrite 0072,04
2935 SPIWrite 0073,46
2936 SPIWrite 0074,7d
2937 SPIWrite 0075,48
2938 SPIWrite 0076,04
2939 SPIWrite 0077,70
2940 SPIWrite 0078,20
2941 SPIWrite 0079,46
2942 SPIWrite 007a,e2
2943 SPIWrite 007b,f7
2944 SPIWrite 007c,9d
2945 SPIWrite 007d,fc
2946 SPIWrite 007e,7c
2947 SPIWrite 007f,48
2948 SPIWrite 0080,50
2949 SPIWrite 0081,f8
2950 SPIWrite 0082,24
2951 SPIWrite 0083,00
2952 SPIWrite 0084,0f
2953 SPIWrite 0085,21
2954 SPIWrite 0086,ff
2955 SPIWrite 0087,f7

2956 SPIWrite 0088,d9
2957 SPIWrite 0089,ff
2958 SPIWrite 008a,10
2959 SPIWrite 008b,bd
2960 SPIWrite 008c,70
2961 SPIWrite 008d,b5
2962 SPIWrite 008e,04
2963 SPIWrite 008f,46
2964 SPIWrite 0090,78
2965 SPIWrite 0091,48
2966 SPIWrite 0092,00
2967 SPIWrite 0093,68
2968 SPIWrite 0094,16
2969 SPIWrite 0095,46
2970 SPIWrite 0096,0d
2971 SPIWrite 0097,46
2972 SPIWrite 0098,80
2973 SPIWrite 0099,47
2974 SPIWrite 009a,01
2975 SPIWrite 009b,28
2976 SPIWrite 009c,31
2977 SPIWrite 009d,46
2978 SPIWrite 009e,3c
2979 SPIWrite 009f,d1
2980 SPIWrite 00a0,4f
2981 SPIWrite 00a1,f0
2982 SPIWrite 00a2,29
2983 SPIWrite 00a3,42
2984 SPIWrite 00a4,92
2985 SPIWrite 00a5,f8
2986 SPIWrite 00a6,77
2987 SPIWrite 00a7,00
2988 SPIWrite 00a8,40
2989 SPIWrite 00a9,f0
2990 SPIWrite 00aa,08
2991 SPIWrite 00ab,00
2992 SPIWrite 00ac,82
2993 SPIWrite 00ad,f8
2994 SPIWrite 00ae,77
2995 SPIWrite 00af,00
2996 SPIWrite 00b0,92
2997 SPIWrite 00b1,f8
2998 SPIWrite 00b2,82
2999 SPIWrite 00b3,00
3000 SPIWrite 00b4,00
3001 SPIWrite 00b5,f0
3002 SPIWrite 00b6,c3
3003 SPIWrite 00b7,00
3004 SPIWrite 00b8,0c
3005 SPIWrite 00b9,30
3006 SPIWrite 00ba,82
3007 SPIWrite 00bb,f8
3008 SPIWrite 00bc,82
3009 SPIWrite 00bd,00
3010 SPIWrite 00be,05
3011 SPIWrite 00bf,eb
3012 SPIWrite 00c0,04
3013 SPIWrite 00c1,15
3014 SPIWrite 00c2,82
3015 SPIWrite 00c3,f8
3016 SPIWrite 00c4,76
3017 SPIWrite 00c5,50
3018 SPIWrite 00c6,92
3019 SPIWrite 00c7,f8
3020 SPIWrite 00c8,77
3021 SPIWrite 00c9,00
3022 SPIWrite 00ca,01
3023 SPIWrite 00cb,f0
3024 SPIWrite 00cc,03

3025 SPIWrite 00cd,01
3026 SPIWrite 00ce,00
3027 SPIWrite 00cf,f0
3028 SPIWrite 00d0,fc
3029 SPIWrite 00d1,00
3030 SPIWrite 00d2,01
3031 SPIWrite 00d3,43
3032 SPIWrite 00d4,82
3033 SPIWrite 00d5,f8
3034 SPIWrite 00d6,77
3035 SPIWrite 00d7,10
3036 SPIWrite 00d8,92
3037 SPIWrite 00d9,f8
3038 SPIWrite 00da,77
3039 SPIWrite 00db,00
3040 SPIWrite 00dc,00
3041 SPIWrite 00dd,f0
3042 SPIWrite 00de,fb
3043 SPIWrite 00df,00
3044 SPIWrite 00e0,82
3045 SPIWrite 00e1,f8
3046 SPIWrite 00e2,77
3047 SPIWrite 00e3,00
3048 SPIWrite 00e4,92
3049 SPIWrite 00e5,f8
3050 SPIWrite 00e6,77
3051 SPIWrite 00e7,00
3052 SPIWrite 00e8,40
3053 SPIWrite 00e9,f0
3054 SPIWrite 00ea,04
3055 SPIWrite 00eb,00
3056 SPIWrite 00ec,82
3057 SPIWrite 00ed,f8
3058 SPIWrite 00ee,77
3059 SPIWrite 00ef,00
3060 SPIWrite 00f0,92
3061 SPIWrite 00f1,f8
3062 SPIWrite 00f2,77
3063 SPIWrite 00f3,00
3064 SPIWrite 00f4,00
3065 SPIWrite 00f5,f0
3066 SPIWrite 00f6,f7
3067 SPIWrite 00f7,00
3068 SPIWrite 00f8,82
3069 SPIWrite 00f9,f8
3070 SPIWrite 00fa,77
3071 SPIWrite 00fb,00
3072 SPIWrite 00fc,92
3073 SPIWrite 00fd,f8
3074 SPIWrite 00fe,82
3075 SPIWrite 00ff,00
3076 SPIWrite 0100,00
3077 SPIWrite 0101,f0
3078 SPIWrite 0102,c3
3079 SPIWrite 0103,00
3080 SPIWrite 0104,82
3081 SPIWrite 0105,f8
3082 SPIWrite 0106,82
3083 SPIWrite 0107,00
3084 SPIWrite 0108,00
3085 SPIWrite 0109,26
3086 SPIWrite 010a,82
3087 SPIWrite 010b,f8
3088 SPIWrite 010c,76
3089 SPIWrite 010d,60
3090 SPIWrite 010e,92
3091 SPIWrite 010f,f8
3092 SPIWrite 0110,77
3093 SPIWrite 0111,00

3094 SPIWrite 0112,00
3095 SPIWrite 0113,f0
3096 SPIWrite 0114,fc
3097 SPIWrite 0115,00
3098 SPIWrite 0116,82
3099 SPIWrite 0117,f8
3100 SPIWrite 0118,77
3101 SPIWrite 0119,00
3102 SPIWrite 011a,57
3103 SPIWrite 011b,48
3104 SPIWrite 011c,d0
3105 SPIWrite 011d,f8
3106 SPIWrite 011e,18
3107 SPIWrite 011f,04
3108 SPIWrite 0120,80
3109 SPIWrite 0121,47
3110 SPIWrite 0122,70
3111 SPIWrite 0123,bd
3112 SPIWrite 0124,70
3113 SPIWrite 0125,b5
3114 SPIWrite 0126,51
3115 SPIWrite 0127,4c
3116 SPIWrite 0128,54
3117 SPIWrite 0129,4b
3118 SPIWrite 012a,25
3119 SPIWrite 012b,78
3120 SPIWrite 012c,03
3121 SPIWrite 012d,eb
3122 SPIWrite 012e,65
3123 SPIWrite 012f,04
3124 SPIWrite 0130,a6
3125 SPIWrite 0131,79
3126 SPIWrite 0132,5b
3127 SPIWrite 0133,19
3128 SPIWrite 0134,9c
3129 SPIWrite 0135,7a
3130 SPIWrite 0136,52
3131 SPIWrite 0137,4d
3132 SPIWrite 0138,73
3133 SPIWrite 0139,00
3134 SPIWrite 013a,03
3135 SPIWrite 013b,eb
3136 SPIWrite 013c,c6
3137 SPIWrite 013d,03
3138 SPIWrite 013e,e4
3139 SPIWrite 013f,18
3140 SPIWrite 0140,2b
3141 SPIWrite 0141,5d
3142 SPIWrite 0142,06
3143 SPIWrite 0143,2b
3144 SPIWrite 0144,06
3145 SPIWrite 0145,da
3146 SPIWrite 0146,8a
3147 SPIWrite 0147,00
3148 SPIWrite 0148,83
3149 SPIWrite 0149,08
3150 SPIWrite 014a,b2
3151 SPIWrite 014b,fb
3152 SPIWrite 014c,f0
3153 SPIWrite 014d,f0
3154 SPIWrite 014e,03
3155 SPIWrite 014f,fb
3156 SPIWrite 0150,10
3157 SPIWrite 0151,10
3158 SPIWrite 0152,70
3159 SPIWrite 0153,bd
3160 SPIWrite 0154,e2
3161 SPIWrite 0155,f7
3162 SPIWrite 0156,4f

3163 SPIWrite 0157,ff
3164 SPIWrite 0158,70
3165 SPIWrite 0159,bd
3166 SPIWrite 015a,2d
3167 SPIWrite 015b,e9
3168 SPIWrite 015c,f0
3169 SPIWrite 015d,43
3170 SPIWrite 015e,4f
3171 SPIWrite 015f,f0
3172 SPIWrite 0160,00
3173 SPIWrite 0161,08
3174 SPIWrite 0162,04
3175 SPIWrite 0163,46
3176 SPIWrite 0164,15
3177 SPIWrite 0165,46
3178 SPIWrite 0166,ad
3179 SPIWrite 0167,f1
3180 SPIWrite 0168,14
3181 SPIWrite 0169,0d
3182 SPIWrite 016a,81
3183 SPIWrite 016b,f8
3184 SPIWrite 016c,00
3185 SPIWrite 016d,80
3186 SPIWrite 016e,e2
3187 SPIWrite 016f,f7
3188 SPIWrite 0170,5f
3189 SPIWrite 0171,ff
3190 SPIWrite 0172,42
3191 SPIWrite 0173,4a
3192 SPIWrite 0174,50
3193 SPIWrite 0175,78
3194 SPIWrite 0176,01
3195 SPIWrite 0177,21
3196 SPIWrite 0178,01
3197 SPIWrite 0179,fa
3198 SPIWrite 017a,04
3199 SPIWrite 017b,f3
3200 SPIWrite 017c,03
3201 SPIWrite 017d,42
3202 SPIWrite 017e,65
3203 SPIWrite 017f,d0
3204 SPIWrite 0180,42
3205 SPIWrite 0181,4b
3206 SPIWrite 0182,40
3207 SPIWrite 0183,4e
3208 SPIWrite 0184,14
3209 SPIWrite 0185,20
3210 SPIWrite 0186,17
3211 SPIWrite 0187,19
3212 SPIWrite 0188,14
3213 SPIWrite 0189,fb
3214 SPIWrite 018a,00
3215 SPIWrite 018b,f0
3216 SPIWrite 018c,1b
3217 SPIWrite 018d,58
3218 SPIWrite 018e,38
3219 SPIWrite 018f,7a
3220 SPIWrite 0190,3d
3221 SPIWrite 0191,4f
3222 SPIWrite 0192,30
3223 SPIWrite 0193,5c
3224 SPIWrite 0194,b7
3225 SPIWrite 0195,f8
3226 SPIWrite 0196,9e
3227 SPIWrite 0197,61
3228 SPIWrite 0198,70
3229 SPIWrite 0199,43
3230 SPIWrite 019a,18
3231 SPIWrite 019b,26

3232 SPIWrite 019c,14
3233 SPIWrite 019d,fb
3234 SPIWrite 019e,06
3235 SPIWrite 019f,2c
3236 SPIWrite 01a0,0c
3237 SPIWrite 01a1,eb
3238 SPIWrite 01a2,c5
3239 SPIWrite 01a3,0e
3240 SPIWrite 01a4,de
3241 SPIWrite 01a5,f8
3242 SPIWrite 01a6,d0
3243 SPIWrite 01a7,60
3244 SPIWrite 01a8,b2
3245 SPIWrite 01a9,00
3246 SPIWrite 01aa,b2
3247 SPIWrite 01ab,fb
3248 SPIWrite 01ac,f0
3249 SPIWrite 01ad,f9
3250 SPIWrite 01ae,82
3251 SPIWrite 01af,08
3252 SPIWrite 01b0,02
3253 SPIWrite 01b1,fb
3254 SPIWrite 01b2,19
3255 SPIWrite 01b3,66
3256 SPIWrite 01b4,00
3257 SPIWrite 01b5,96
3258 SPIWrite 01b6,de
3259 SPIWrite 01b7,f8
3260 SPIWrite 01b8,d4
3261 SPIWrite 01b9,60
3262 SPIWrite 01ba,4f
3263 SPIWrite 01bb,ea
3264 SPIWrite 01bc,86
3265 SPIWrite 01bd,0e
3266 SPIWrite 01be,be
3267 SPIWrite 01bf,fb
3268 SPIWrite 01c0,f0
3269 SPIWrite 01c1,fe
3270 SPIWrite 01c2,02
3271 SPIWrite 01c3,fb
3272 SPIWrite 01c4,1e
3273 SPIWrite 01c5,66
3274 SPIWrite 01c6,01
3275 SPIWrite 01c7,96
3276 SPIWrite 01c8,dc
3277 SPIWrite 01c9,f8
3278 SPIWrite 01ca,e0
3279 SPIWrite 01cb,60
3280 SPIWrite 01cc,4f
3281 SPIWrite 01cd,ea
3282 SPIWrite 01ce,86
3283 SPIWrite 01cf,0e
3284 SPIWrite 01d0,be
3285 SPIWrite 01d1,fb
3286 SPIWrite 01d2,f0
3287 SPIWrite 01d3,fe
3288 SPIWrite 01d4,02
3289 SPIWrite 01d5,fb
3290 SPIWrite 01d6,1e
3291 SPIWrite 01d7,66
3292 SPIWrite 01d8,02
3293 SPIWrite 01d9,96
3294 SPIWrite 01da,dc
3295 SPIWrite 01db,f8
3296 SPIWrite 01dc,e4
3297 SPIWrite 01dd,60
3298 SPIWrite 01de,3f
3299 SPIWrite 01df,19
3300 SPIWrite 01e0,4f

3301 SPIWrite 01e1,ea
3302 SPIWrite 01e2,86
3303 SPIWrite 01e3,0c
3304 SPIWrite 01e4,bc
3305 SPIWrite 01e5,fb
3306 SPIWrite 01e6,f0
3307 SPIWrite 01e7,f0
3308 SPIWrite 01e8,02
3309 SPIWrite 01e9,fb
3310 SPIWrite 01ea,10
3311 SPIWrite 01eb,60
3312 SPIWrite 01ec,03
3313 SPIWrite 01ed,90
3314 SPIWrite 01ee,97
3315 SPIWrite 01ef,f8
3316 SPIWrite 01f0,6c
3317 SPIWrite 01f1,00
3318 SPIWrite 01f2,0a
3319 SPIWrite 01f3,46
3320 SPIWrite 01f4,03
3321 SPIWrite 01f5,28
3322 SPIWrite 01f6,07
3323 SPIWrite 01f7,d0
3324 SPIWrite 01f8,0a
3325 SPIWrite 01f9,28
3326 SPIWrite 01fa,05
3327 SPIWrite 01fb,d0
3328 SPIWrite 01fc,0b
3329 SPIWrite 01fd,28
3330 SPIWrite 01fe,03
3331 SPIWrite 01ff,d0
3332 SPIWrite 0200,0c
3333 SPIWrite 0201,28
3334 SPIWrite 0202,1c
3335 SPIWrite 0203,bf
3336 SPIWrite 0204,0d
3337 SPIWrite 0205,28
3338 SPIWrite 0206,42
3339 SPIWrite 0207,46
3340 SPIWrite 0208,12
3341 SPIWrite 0209,fb
3342 SPIWrite 020a,05
3343 SPIWrite 020b,f0
3344 SPIWrite 020c,4f
3345 SPIWrite 020d,f4
3346 SPIWrite 020e,80
3347 SPIWrite 020f,72
3348 SPIWrite 0210,04
3349 SPIWrite 0211,27
3350 SPIWrite 0212,ec
3351 SPIWrite 0213,46
3352 SPIWrite 0214,02
3353 SPIWrite 0215,eb
3354 SPIWrite 0216,40
3355 SPIWrite 0217,12
3356 SPIWrite 0218,96
3357 SPIWrite 0219,b2
3358 SPIWrite 021a,40
3359 SPIWrite 021b,46
3360 SPIWrite 021c,5c
3361 SPIWrite 021d,f8
3362 SPIWrite 021e,04
3363 SPIWrite 021f,2b
3364 SPIWrite 0220,35
3365 SPIWrite 0221,18
3366 SPIWrite 0222,7f
3367 SPIWrite 0223,1e
3368 SPIWrite 0224,00
3369 SPIWrite 0225,f1

3370 SPIWrite 0226,04
3371 SPIWrite 0227,00
3372 SPIWrite 0228,5a
3373 SPIWrite 0229,51
3374 SPIWrite 022a,f7
3375 SPIWrite 022b,d1
3376 SPIWrite 022c,18
3377 SPIWrite 022d,4a
3378 SPIWrite 022e,15
3379 SPIWrite 022f,20
3380 SPIWrite 0230,14
3381 SPIWrite 0231,fb
3382 SPIWrite 0232,00
3383 SPIWrite 0233,f0
3384 SPIWrite 0234,10
3385 SPIWrite 0235,5c
3386 SPIWrite 0236,06
3387 SPIWrite 0237,28
3388 SPIWrite 0238,03
3389 SPIWrite 0239,d0
3390 SPIWrite 023a,40
3391 SPIWrite 023b,08
3392 SPIWrite 023c,2c
3393 SPIWrite 023d,bf
3394 SPIWrite 023e,0f
3395 SPIWrite 023f,21
3396 SPIWrite 0240,07
3397 SPIWrite 0241,21
3398 SPIWrite 0242,14
3399 SPIWrite 0243,48
3400 SPIWrite 0244,50
3401 SPIWrite 0245,f8
3402 SPIWrite 0246,24
3403 SPIWrite 0247,00
3404 SPIWrite 0248,ff
3405 SPIWrite 0249,f7
3406 SPIWrite 024a,f8
3407 SPIWrite 024b,fe
3408 SPIWrite 024c,05
3409 SPIWrite 024d,b0
3410 SPIWrite 024e,bd
3411 SPIWrite 024f,e8
3412 SPIWrite 0250,f0
3413 SPIWrite 0251,83
3414 SPIWrite 0252,c0
3415 SPIWrite 0253,46
3416 SPIWrite 0254,3b
3417 SPIWrite 0255,78
3418 SPIWrite 0256,02
3419 SPIWrite 0257,00
3420 SPIWrite 0258,17
3421 SPIWrite 0259,01
3422 SPIWrite 025a,01
3423 SPIWrite 025b,20
3424 SPIWrite 025c,52
3425 SPIWrite 025d,03
3426 SPIWrite 025e,01
3427 SPIWrite 025f,20
3428 SPIWrite 0260,34
3429 SPIWrite 0261,fe
3430 SPIWrite 0262,00
3431 SPIWrite 0263,20
3432 SPIWrite 0264,bc
3433 SPIWrite 0265,dc
3434 SPIWrite 0266,00
3435 SPIWrite 0267,20
3436 SPIWrite 0268,d4
3437 SPIWrite 0269,fb
3438 SPIWrite 026a,00

3439 SPIWrite 026b,20
3440 SPIWrite 026c,62
3441 SPIWrite 026d,22
3442 SPIWrite 026e,01
3443 SPIWrite 026f,20
3444 SPIWrite 0270,9c
3445 SPIWrite 0271,77
3446 SPIWrite 0272,02
3447 SPIWrite 0273,00
3448 SPIWrite 0274,a4
3449 SPIWrite 0275,da
3450 SPIWrite 0276,00
3451 SPIWrite 0277,20
3452 SPIWrite 0278,90
3453 SPIWrite 0279,d6
3454 SPIWrite 027a,00
3455 SPIWrite 027b,20
3456 SPIWrite 027c,18
3457 SPIWrite 027d,ff
3458 SPIWrite 027e,00
3459 SPIWrite 027f,20
3460 SPIWrite 0280,b8
3461 SPIWrite 0281,16
3462 SPIWrite 0282,01
3463 SPIWrite 0283,20
3464 SPIWrite 0284,ac
3465 SPIWrite 0285,78
3466 SPIWrite 0286,02
3467 SPIWrite 0287,00
3468 SPIWrite 0288,b4
3469 SPIWrite 0289,01
3470 SPIWrite 028a,01
3471 SPIWrite 028b,20
3472 SPIWrite 028c,d8
3473 SPIWrite 028d,74
3474 SPIWrite 028e,02
3475 SPIWrite 028f,00
3476 SPIWrite 0290,32
3477 SPIWrite 0291,d4
3478 SPIWrite 0292,00
3479 SPIWrite 0293,20
3480 SPIWrite 0294,90
3481 SPIWrite 0295,78
3482 SPIWrite 0296,02
3483 SPIWrite 0297,00
3484 SPIWrite 0298,70
3485 SPIWrite 0299,47
3486 SPIWrite 029a,f8
3487 SPIWrite 029b,b5
3488 SPIWrite 029c,78
3489 SPIWrite 029d,4c
3490 SPIWrite 029e,84
3491 SPIWrite 029f,46
3492 SPIWrite 02a0,e0
3493 SPIWrite 02a1,79
3494 SPIWrite 02a2,64
3495 SPIWrite 02a3,79
3496 SPIWrite 02a4,24
3497 SPIWrite 02a5,18
3498 SPIWrite 02a6,02
3499 SPIWrite 02a7,2c
3500 SPIWrite 02a8,3a
3501 SPIWrite 02a9,d1
3502 SPIWrite 02aa,57
3503 SPIWrite 02ab,78
3504 SPIWrite 02ac,37
3505 SPIWrite 02ad,f0
3506 SPIWrite 02ae,02
3507 SPIWrite 02af,07

3508 SPIWrite 02b0,36
3509 SPIWrite 02b1,d1
3510 SPIWrite 02b2,76
3511 SPIWrite 02b3,4c
3512 SPIWrite 02b4,74
3513 SPIWrite 02b5,4a
3514 SPIWrite 02b6,03
3515 SPIWrite 02b7,27
3516 SPIWrite 02b8,0c
3517 SPIWrite 02b9,20
3518 SPIWrite 02ba,1c
3519 SPIWrite 02bb,fb
3520 SPIWrite 02bc,07
3521 SPIWrite 02bd,15
3522 SPIWrite 02be,1c
3523 SPIWrite 02bf,fb
3524 SPIWrite 02c0,00
3525 SPIWrite 02c1,f0
3526 SPIWrite 02c2,00
3527 SPIWrite 02c3,eb
3528 SPIWrite 02c4,81
3529 SPIWrite 02c5,00
3530 SPIWrite 02c6,67
3531 SPIWrite 02c7,5d
3532 SPIWrite 02c8,12
3533 SPIWrite 02c9,58
3534 SPIWrite 02ca,6e
3535 SPIWrite 02cb,48
3536 SPIWrite 02cc,92
3537 SPIWrite 02cd,f9
3538 SPIWrite 02ce,90
3539 SPIWrite 02cf,54
3540 SPIWrite 02d0,dc
3541 SPIWrite 02d1,26
3542 SPIWrite 02d2,4f
3543 SPIWrite 02d3,f4
3544 SPIWrite 02d4,25
3545 SPIWrite 02d5,7e
3546 SPIWrite 02d6,11
3547 SPIWrite 02d7,fb
3548 SPIWrite 02d8,06
3549 SPIWrite 02d9,f6
3550 SPIWrite 02da,1c
3551 SPIWrite 02db,fb
3552 SPIWrite 02dc,0e
3553 SPIWrite 02dd,66
3554 SPIWrite 02de,94
3555 SPIWrite 02df,46
3556 SPIWrite 02e0,80
3557 SPIWrite 02e1,19
3558 SPIWrite 02e2,90
3559 SPIWrite 02e3,f9
3560 SPIWrite 02e4,89
3561 SPIWrite 02e5,10
3562 SPIWrite 02e6,90
3563 SPIWrite 02e7,f9
3564 SPIWrite 02e8,87
3565 SPIWrite 02e9,40
3566 SPIWrite 02ea,90
3567 SPIWrite 02eb,f9
3568 SPIWrite 02ec,86
3569 SPIWrite 02ed,20
3570 SPIWrite 02ee,9c
3571 SPIWrite 02ef,f9
3572 SPIWrite 02f0,91
3573 SPIWrite 02f1,64
3574 SPIWrite 02f2,90
3575 SPIWrite 02f3,f9
3576 SPIWrite 02f4,88

3577 SPIWrite 02f5,00
3578 SPIWrite 02f6,4f
3579 SPIWrite 02f7,b9
3580 SPIWrite 02f8,86
3581 SPIWrite 02f9,42
3582 SPIWrite 02fa,0e
3583 SPIWrite 02fb,bf
3584 SPIWrite 02fc,a5
3585 SPIWrite 02fd,42
3586 SPIWrite 02fe,01
3587 SPIWrite 02ff,21
3588 SPIWrite 0300,19
3589 SPIWrite 0301,70
3590 SPIWrite 0302,8c
3591 SPIWrite 0303,f8
3592 SPIWrite 0304,90
3593 SPIWrite 0305,44
3594 SPIWrite 0306,8c
3595 SPIWrite 0307,f8
3596 SPIWrite 0308,91
3597 SPIWrite 0309,04
3598 SPIWrite 030a,f8
3599 SPIWrite 030b,bd
3600 SPIWrite 030c,95
3601 SPIWrite 030d,42
3602 SPIWrite 030e,0e
3603 SPIWrite 030f,bf
3604 SPIWrite 0310,8e
3605 SPIWrite 0311,42
3606 SPIWrite 0312,01
3607 SPIWrite 0313,20
3608 SPIWrite 0314,18
3609 SPIWrite 0315,70
3610 SPIWrite 0316,8c
3611 SPIWrite 0317,f8
3612 SPIWrite 0318,91
3613 SPIWrite 0319,14
3614 SPIWrite 031a,8c
3615 SPIWrite 031b,f8
3616 SPIWrite 031c,90
3617 SPIWrite 031d,24
3618 SPIWrite 031e,f8
3619 SPIWrite 031f,bd
3620 SPIWrite 0320,60
3621 SPIWrite 0321,46
3622 SPIWrite 0322,ec
3623 SPIWrite 0323,f7
3624 SPIWrite 0324,29
3625 SPIWrite 0325,fe
3626 SPIWrite 0326,f8
3627 SPIWrite 0327,bd
3628 SPIWrite 0328,2d
3629 SPIWrite 0329,e9
3630 SPIWrite 032a,fe
3631 SPIWrite 032b,4f
3632 SPIWrite 032c,0c
3633 SPIWrite 032d,9e
3634 SPIWrite 032e,82
3635 SPIWrite 032f,46
3636 SPIWrite 0330,89
3637 SPIWrite 0331,46
3638 SPIWrite 0332,14
3639 SPIWrite 0333,46
3640 SPIWrite 0334,0d
3641 SPIWrite 0335,9f
3642 SPIWrite 0336,00
3643 SPIWrite 0337,96
3644 SPIWrite 0338,1d
3645 SPIWrite 0339,46

3646 SPIWrite 033a,01
3647 SPIWrite 033b,97
3648 SPIWrite 033c,ec
3649 SPIWrite 033d,f7
3650 SPIWrite 033e,4a
3651 SPIWrite 033f,ff
3652 SPIWrite 0340,df
3653 SPIWrite 0341,f8
3654 SPIWrite 0342,48
3655 SPIWrite 0343,b1
3656 SPIWrite 0344,20
3657 SPIWrite 0345,88
3658 SPIWrite 0346,20
3659 SPIWrite 0347,b9
3660 SPIWrite 0348,60
3661 SPIWrite 0349,88
3662 SPIWrite 034a,00
3663 SPIWrite 034b,28
3664 SPIWrite 034c,4f
3665 SPIWrite 034d,d0
3666 SPIWrite 034e,01
3667 SPIWrite 034f,20
3668 SPIWrite 0350,4e
3669 SPIWrite 0351,e0
3670 SPIWrite 0352,63
3671 SPIWrite 0353,88
3672 SPIWrite 0354,00
3673 SPIWrite 0355,2b
3674 SPIWrite 0356,4a
3675 SPIWrite 0357,d0
3676 SPIWrite 0358,ea
3677 SPIWrite 0359,f7
3678 SPIWrite 035a,77
3679 SPIWrite 035b,ff
3680 SPIWrite 035c,80
3681 SPIWrite 035d,46
3682 SPIWrite 035e,60
3683 SPIWrite 035f,88
3684 SPIWrite 0360,ea
3685 SPIWrite 0361,f7
3686 SPIWrite 0362,73
3687 SPIWrite 0363,ff
3688 SPIWrite 0364,69
3689 SPIWrite 0365,79
3690 SPIWrite 0366,00
3691 SPIWrite 0367,eb
3692 SPIWrite 0368,80
3693 SPIWrite 0369,00
3694 SPIWrite 036a,08
3695 SPIWrite 036b,eb
3696 SPIWrite 036c,88
3697 SPIWrite 036d,02
3698 SPIWrite 036e,c0
3699 SPIWrite 036f,13
3700 SPIWrite 0370,d2
3701 SPIWrite 0371,13
3702 SPIWrite 0372,01
3703 SPIWrite 0373,29
3704 SPIWrite 0374,44
3705 SPIWrite 0375,b2
3706 SPIWrite 0376,53
3707 SPIWrite 0377,b2
3708 SPIWrite 0378,3f
3709 SPIWrite 0379,d1
3710 SPIWrite 037a,42
3711 SPIWrite 037b,48
3712 SPIWrite 037c,dc
3713 SPIWrite 037d,21
3714 SPIWrite 037e,4f

3715 SPIWrite 037f,f4
3716 SPIWrite 0380,25
3717 SPIWrite 0381,72
3718 SPIWrite 0382,19
3719 SPIWrite 0383,fb
3720 SPIWrite 0384,01
3721 SPIWrite 0385,f1
3722 SPIWrite 0386,1a
3723 SPIWrite 0387,fb
3724 SPIWrite 0388,02
3725 SPIWrite 0389,11
3726 SPIWrite 038a,b2
3727 SPIWrite 038b,78
3728 SPIWrite 038c,40
3729 SPIWrite 038d,18
3730 SPIWrite 038e,71
3731 SPIWrite 038f,78
3732 SPIWrite 0390,b0
3733 SPIWrite 0391,f9
3734 SPIWrite 0392,5a
3735 SPIWrite 0393,c0
3736 SPIWrite 0394,b0
3737 SPIWrite 0395,f9
3738 SPIWrite 0396,5c
3739 SPIWrite 0397,60
3740 SPIWrite 0398,c2
3741 SPIWrite 0399,f1
3742 SPIWrite 039a,01
3743 SPIWrite 039b,02
3744 SPIWrite 039c,c1
3745 SPIWrite 039d,f1
3746 SPIWrite 039e,01
3747 SPIWrite 039f,01
3748 SPIWrite 03a0,11
3749 SPIWrite 03a1,fb
3750 SPIWrite 03a2,0c
3751 SPIWrite 03a3,f0
3752 SPIWrite 03a4,c0
3753 SPIWrite 03a5,eb
3754 SPIWrite 03a6,43
3755 SPIWrite 03a7,10
3756 SPIWrite 03a8,12
3757 SPIWrite 03a9,fb
3758 SPIWrite 03aa,06
3759 SPIWrite 03ab,f1
3760 SPIWrite 03ac,40
3761 SPIWrite 03ad,11
3762 SPIWrite 03ae,c1
3763 SPIWrite 03af,eb
3764 SPIWrite 03b0,44
3765 SPIWrite 03b1,11
3766 SPIWrite 03b2,a0
3767 SPIWrite 03b3,eb
3768 SPIWrite 03b4,61
3769 SPIWrite 03b5,10
3770 SPIWrite 03b6,41
3771 SPIWrite 03b7,b2
3772 SPIWrite 03b8,08
3773 SPIWrite 03b9,46
3774 SPIWrite 03ba,00
3775 SPIWrite 03bb,28
3776 SPIWrite 03bc,b8
3777 SPIWrite 03bd,bf
3778 SPIWrite 03be,40
3779 SPIWrite 03bf,42
3780 SPIWrite 03c0,c2
3781 SPIWrite 03c1,b2
3782 SPIWrite 03c2,00
3783 SPIWrite 03c3,29

3784 SPIWrite 03c4,4f
3785 SPIWrite 03c5,f0
3786 SPIWrite 03c6,00
3787 SPIWrite 03c7,00
3788 SPIWrite 03c8,d8
3789 SPIWrite 03c9,bf
3790 SPIWrite 03ca,01
3791 SPIWrite 03cb,20
3792 SPIWrite 03cc,a9
3793 SPIWrite 03cd,79
3794 SPIWrite 03ce,91
3795 SPIWrite 03cf,42
3796 SPIWrite 03d0,0e
3797 SPIWrite 03d1,da
3798 SPIWrite 03d2,2b
3799 SPIWrite 03d3,78
3800 SPIWrite 03d4,c9
3801 SPIWrite 03d5,18
3802 SPIWrite 03d6,91
3803 SPIWrite 03d7,42
3804 SPIWrite 03d8,0a
3805 SPIWrite 03d9,db
3806 SPIWrite 03da,03
3807 SPIWrite 03db,22
3808 SPIWrite 03dc,59
3809 SPIWrite 03dd,46
3810 SPIWrite 03de,1a
3811 SPIWrite 03df,fb
3812 SPIWrite 03e0,02
3813 SPIWrite 03e1,92
3814 SPIWrite 03e2,89
3815 SPIWrite 03e3,5c
3816 SPIWrite 03e4,81
3817 SPIWrite 03e5,42
3818 SPIWrite 03e6,1c
3819 SPIWrite 03e7,bf
3820 SPIWrite 03e8,01
3821 SPIWrite 03e9,21
3822 SPIWrite 03ea,79
3823 SPIWrite 03eb,70
3824 SPIWrite 03ec,00
3825 SPIWrite 03ed,e0
3826 SPIWrite 03ee,00
3827 SPIWrite 03ef,20
3828 SPIWrite 03f0,03
3829 SPIWrite 03f1,22
3830 SPIWrite 03f2,59
3831 SPIWrite 03f3,46
3832 SPIWrite 03f4,1a
3833 SPIWrite 03f5,fb
3834 SPIWrite 03f6,02
3835 SPIWrite 03f7,92
3836 SPIWrite 03f8,88
3837 SPIWrite 03f9,54
3838 SPIWrite 03fa,bd
3839 SPIWrite 03fb,e8
3840 SPIWrite 03fc,fe
3841 SPIWrite 03fd,8f
3842 SPIWrite 03fe,2d
3843 SPIWrite 03ff,e9
3844 SPIWrite 0400,fc
3845 SPIWrite 0401,47
3846 SPIWrite 0402,24
3847 SPIWrite 0403,48
3848 SPIWrite 0404,df
3849 SPIWrite 0405,f8
3850 SPIWrite 0406,88
3851 SPIWrite 0407,90
3852 SPIWrite 0408,c9

3853 SPIWrite 0409,f8
3854 SPIWrite 040a,3c
3855 SPIWrite 040b,01
3856 SPIWrite 040c,ed
3857 SPIWrite 040d,f7
3858 SPIWrite 040e,7e
3859 SPIWrite 040f,f8
3860 SPIWrite 0410,00
3861 SPIWrite 0411,24
3862 SPIWrite 0412,22
3863 SPIWrite 0413,4d
3864 SPIWrite 0414,20
3865 SPIWrite 0415,48
3866 SPIWrite 0416,df
3867 SPIWrite 0417,f8
3868 SPIWrite 0418,8c
3869 SPIWrite 0419,80
3870 SPIWrite 041a,23
3871 SPIWrite 041b,4f
3872 SPIWrite 041c,df
3873 SPIWrite 041d,f8
3874 SPIWrite 041e,80
3875 SPIWrite 041f,a0
3876 SPIWrite 0420,19
3877 SPIWrite 0421,4e
3878 SPIWrite 0422,8d
3879 SPIWrite 0423,f8
3880 SPIWrite 0424,04
3881 SPIWrite 0425,40
3882 SPIWrite 0426,6d
3883 SPIWrite 0427,1e
3884 SPIWrite 0428,c9
3885 SPIWrite 0429,f8
3886 SPIWrite 042a,3c
3887 SPIWrite 042b,01
3888 SPIWrite 042c,15
3889 SPIWrite 042d,f8
3890 SPIWrite 042e,01
3891 SPIWrite 042f,0f
3892 SPIWrite 0430,01
3893 SPIWrite 0431,28
3894 SPIWrite 0432,20
3895 SPIWrite 0433,d1
3896 SPIWrite 0434,1a
3897 SPIWrite 0435,f8
3898 SPIWrite 0436,04
3899 SPIWrite 0437,00
3900 SPIWrite 0438,e8
3901 SPIWrite 0439,b9
3902 SPIWrite 043a,18
3903 SPIWrite 043b,f8
3904 SPIWrite 043c,14
3905 SPIWrite 043d,10
3906 SPIWrite 043e,60
3907 SPIWrite 043f,00
3908 SPIWrite 0440,00
3909 SPIWrite 0441,eb
3910 SPIWrite 0442,84
3911 SPIWrite 0443,00
3912 SPIWrite 0444,3b
3913 SPIWrite 0445,18
3914 SPIWrite 0446,9a
3915 SPIWrite 0447,78
3916 SPIWrite 0448,60
3917 SPIWrite 0449,10
3918 SPIWrite 044a,01
3919 SPIWrite 044b,2a
3920 SPIWrite 044c,0c
3921 SPIWrite 044d,d0

3922 SPIWrite 044e,82
3923 SPIWrite 044f,00
3924 SPIWrite 0450,02
3925 SPIWrite 0451,eb
3926 SPIWrite 0452,c0
3927 SPIWrite 0453,02
3928 SPIWrite 0454,02
3929 SPIWrite 0455,eb
3930 SPIWrite 0456,81
3931 SPIWrite 0457,02
3932 SPIWrite 0458,b0
3933 SPIWrite 0459,58
3934 SPIWrite 045a,d0
3935 SPIWrite 045b,f8
3936 SPIWrite 045c,00
3937 SPIWrite 045d,14
3938 SPIWrite 045e,21
3939 SPIWrite 045f,f4
3940 SPIWrite 0460,80
3941 SPIWrite 0461,71
3942 SPIWrite 0462,c0
3943 SPIWrite 0463,f8
3944 SPIWrite 0464,00
3945 SPIWrite 0465,14
3946 SPIWrite 0466,06
3947 SPIWrite 0467,e0
3948 SPIWrite 0468,01
3949 SPIWrite 0469,aa
3950 SPIWrite 046a,00
3951 SPIWrite 046b,92
3952 SPIWrite 046c,d9
3953 SPIWrite 046d,f8
3954 SPIWrite 046e,3c
3955 SPIWrite 046f,c1
3956 SPIWrite 0470,da
3957 SPIWrite 0471,78
3958 SPIWrite 0472,1b
3959 SPIWrite 0473,1d
3960 SPIWrite 0474,e0
3961 SPIWrite 0475,47
3962 SPIWrite 0476,64
3963 SPIWrite 0477,1c
3964 SPIWrite 0478,04
3965 SPIWrite 0479,2c
3966 SPIWrite 047a,d7
3967 SPIWrite 047b,db
3968 SPIWrite 047c,bd
3969 SPIWrite 047d,e8
3970 SPIWrite 047e,fc
3971 SPIWrite 047f,87
3972 SPIWrite 0480,e6
3973 SPIWrite 0481,1d
3974 SPIWrite 0482,01
3975 SPIWrite 0483,20
3976 SPIWrite 0484,e0
3977 SPIWrite 0485,ab
3978 SPIWrite 0486,00
3979 SPIWrite 0487,20
3980 SPIWrite 0488,a8
3981 SPIWrite 0489,75
3982 SPIWrite 048a,02
3983 SPIWrite 048b,00
3984 SPIWrite 048c,4c
3985 SPIWrite 048d,22
3986 SPIWrite 048e,01
3987 SPIWrite 048f,20
3988 SPIWrite 0490,90
3989 SPIWrite 0491,d6
3990 SPIWrite 0492,00

3991 SPIWrite 0493,20
3992 SPIWrite 0494,79
3993 SPIWrite 0495,0a
3994 SPIWrite 0496,03
3995 SPIWrite 0497,00
3996 SPIWrite 0498,c5
3997 SPIWrite 0499,d6
3998 SPIWrite 049a,01
3999 SPIWrite 049b,00
4000 SPIWrite 049c,f0
4001 SPIWrite 049d,1e
4002 SPIWrite 049e,01
4003 SPIWrite 049f,20
4004 SPIWrite 04a0,f4
4005 SPIWrite 04a1,1e
4006 SPIWrite 04a2,01
4007 SPIWrite 04a3,20
4008 SPIWrite 04a4,06
4009 SPIWrite 04a5,d6
4010 SPIWrite 04a6,00
4011 SPIWrite 04a7,20
4012 SPIWrite 04a8,6c
4013 SPIWrite 04a9,1a
4014 SPIWrite 04aa,01
4015 SPIWrite 04ab,20
4016 SPIWrite 04ac,70
4017 SPIWrite 04ad,b5
4018 SPIWrite 04ae,46
4019 SPIWrite 04af,49
4020 SPIWrite 04b0,44
4021 SPIWrite 04b1,4c
4022 SPIWrite 04b2,c4
4023 SPIWrite 04b3,f8
4024 SPIWrite 04b4,fc
4025 SPIWrite 04b5,10
4026 SPIWrite 04b6,45
4027 SPIWrite 04b7,48
4028 SPIWrite 04b8,c4
4029 SPIWrite 04b9,f8
4030 SPIWrite 04ba,c4
4031 SPIWrite 04bb,00
4032 SPIWrite 04bc,44
4033 SPIWrite 04bd,49
4034 SPIWrite 04be,c4
4035 SPIWrite 04bf,f8
4036 SPIWrite 04c0,c0
4037 SPIWrite 04c1,10
4038 SPIWrite 04c2,44
4039 SPIWrite 04c3,48
4040 SPIWrite 04c4,c4
4041 SPIWrite 04c5,f8
4042 SPIWrite 04c6,30
4043 SPIWrite 04c7,01
4044 SPIWrite 04c8,43
4045 SPIWrite 04c9,49
4046 SPIWrite 04ca,c4
4047 SPIWrite 04cb,f8
4048 SPIWrite 04cc,40
4049 SPIWrite 04cd,11
4050 SPIWrite 04ce,43
4051 SPIWrite 04cf,48
4052 SPIWrite 04d0,c4
4053 SPIWrite 04d1,f8
4054 SPIWrite 04d2,38
4055 SPIWrite 04d3,01
4056 SPIWrite 04d4,4a
4057 SPIWrite 04d5,49
4058 SPIWrite 04d6,c4
4059 SPIWrite 04d7,f8

4060 SPIWrite 04d8,a8
4061 SPIWrite 04d9,16
4062 SPIWrite 04da,4a
4063 SPIWrite 04db,48
4064 SPIWrite 04dc,c4
4065 SPIWrite 04dd,f8
4066 SPIWrite 04de,ac
4067 SPIWrite 04df,06
4068 SPIWrite 04e0,49
4069 SPIWrite 04e1,49
4070 SPIWrite 04e2,c4
4071 SPIWrite 04e3,f8
4072 SPIWrite 04e4,f4
4073 SPIWrite 04e5,15
4074 SPIWrite 04e6,49
4075 SPIWrite 04e7,48
4076 SPIWrite 04e8,a0
4077 SPIWrite 04e9,64
4078 SPIWrite 04ea,3f
4079 SPIWrite 04eb,48
4080 SPIWrite 04ec,28
4081 SPIWrite 04ed,23
4082 SPIWrite 04ee,40
4083 SPIWrite 04ef,f2
4084 SPIWrite 04f0,b7
4085 SPIWrite 04f1,55
4086 SPIWrite 04f2,03
4087 SPIWrite 04f3,80
4088 SPIWrite 04f4,46
4089 SPIWrite 04f5,4a
4090 SPIWrite 04f6,85
4091 SPIWrite 04f7,80
4092 SPIWrite 04f8,46
4093 SPIWrite 04f9,49
4094 SPIWrite 04fa,c4
4095 SPIWrite 04fb,f8
4096 SPIWrite 04fc,3c
4097 SPIWrite 04fd,26
4098 SPIWrite 04fe,41
4099 SPIWrite 04ff,f2
4100 SPIWrite 0500,88
4101 SPIWrite 0501,33
4102 SPIWrite 0502,c3
4103 SPIWrite 0503,60
4104 SPIWrite 0504,00
4105 SPIWrite 0505,26
4106 SPIWrite 0506,c4
4107 SPIWrite 0507,f8
4108 SPIWrite 0508,30
4109 SPIWrite 0509,16
4110 SPIWrite 050a,a6
4111 SPIWrite 050b,21
4112 SPIWrite 050c,41
4113 SPIWrite 050d,80
4114 SPIWrite 050e,3b
4115 SPIWrite 050f,49
4116 SPIWrite 0510,41
4117 SPIWrite 0511,4a
4118 SPIWrite 0512,0e
4119 SPIWrite 0513,70
4120 SPIWrite 0514,35
4121 SPIWrite 0515,49
4122 SPIWrite 0516,c4
4123 SPIWrite 0517,f8
4124 SPIWrite 0518,40
4125 SPIWrite 0519,26
4126 SPIWrite 051a,31
4127 SPIWrite 051b,4b
4128 SPIWrite 051c,81

4129 SPIWrite 051d,60
4130 SPIWrite 051e,03
4131 SPIWrite 051f,22
4132 SPIWrite 0520,82
4133 SPIWrite 0521,71
4134 SPIWrite 0522,30
4135 SPIWrite 0523,4a
4136 SPIWrite 0524,1a
4137 SPIWrite 0525,60
4138 SPIWrite 0526,32
4139 SPIWrite 0527,4a
4140 SPIWrite 0528,32
4141 SPIWrite 0529,4d
4142 SPIWrite 052a,02
4143 SPIWrite 052b,61
4144 SPIWrite 052c,32
4145 SPIWrite 052d,48
4146 SPIWrite 052e,a8
4147 SPIWrite 052f,65
4148 SPIWrite 0530,3a
4149 SPIWrite 0531,48
4150 SPIWrite 0532,c4
4151 SPIWrite 0533,f8
4152 SPIWrite 0534,34
4153 SPIWrite 0535,06
4154 SPIWrite 0536,00
4155 SPIWrite 0537,f0
4156 SPIWrite 0538,77
4157 SPIWrite 0539,fc
4158 SPIWrite 053a,00
4159 SPIWrite 053b,f0
4160 SPIWrite 053c,06
4161 SPIWrite 053d,f9
4162 SPIWrite 053e,38
4163 SPIWrite 053f,48
4164 SPIWrite 0540,38
4165 SPIWrite 0541,49
4166 SPIWrite 0542,00
4167 SPIWrite 0543,f0
4168 SPIWrite 0544,a3
4169 SPIWrite 0545,f8
4170 SPIWrite 0546,39
4171 SPIWrite 0547,48
4172 SPIWrite 0548,3a
4173 SPIWrite 0549,49
4174 SPIWrite 054a,c4
4175 SPIWrite 054b,f8
4176 SPIWrite 054c,70
4177 SPIWrite 054d,09
4178 SPIWrite 054e,3a
4179 SPIWrite 054f,48
4180 SPIWrite 0550,c4
4181 SPIWrite 0551,f8
4182 SPIWrite 0552,4c
4183 SPIWrite 0553,15
4184 SPIWrite 0554,39
4185 SPIWrite 0555,49
4186 SPIWrite 0556,c4
4187 SPIWrite 0557,f8
4188 SPIWrite 0558,38
4189 SPIWrite 0559,06
4190 SPIWrite 055a,39
4191 SPIWrite 055b,48
4192 SPIWrite 055c,c4
4193 SPIWrite 055d,f8
4194 SPIWrite 055e,c4
4195 SPIWrite 055f,14
4196 SPIWrite 0560,38
4197 SPIWrite 0561,49

4198 SPIWrite 0562,c4
4199 SPIWrite 0563,f8
4200 SPIWrite 0564,94
4201 SPIWrite 0565,04
4202 SPIWrite 0566,38
4203 SPIWrite 0567,48
4204 SPIWrite 0568,c4
4205 SPIWrite 0569,f8
4206 SPIWrite 056a,98
4207 SPIWrite 056b,14
4208 SPIWrite 056c,37
4209 SPIWrite 056d,49
4210 SPIWrite 056e,c4
4211 SPIWrite 056f,f8
4212 SPIWrite 0570,00
4213 SPIWrite 0571,02
4214 SPIWrite 0572,38
4215 SPIWrite 0573,48
4216 SPIWrite 0574,c4
4217 SPIWrite 0575,f8
4218 SPIWrite 0576,04
4219 SPIWrite 0577,12
4220 SPIWrite 0578,37
4221 SPIWrite 0579,49
4222 SPIWrite 057a,c4
4223 SPIWrite 057b,f8
4224 SPIWrite 057c,24
4225 SPIWrite 057d,03
4226 SPIWrite 057e,37
4227 SPIWrite 057f,48
4228 SPIWrite 0580,c4
4229 SPIWrite 0581,f8
4230 SPIWrite 0582,94
4231 SPIWrite 0583,11
4232 SPIWrite 0584,2a
4233 SPIWrite 0585,49
4234 SPIWrite 0586,38
4235 SPIWrite 0587,4a
4236 SPIWrite 0588,0e
4237 SPIWrite 0589,70
4238 SPIWrite 058a,36
4239 SPIWrite 058b,49
4240 SPIWrite 058c,c4
4241 SPIWrite 058d,f8
4242 SPIWrite 058e,c4
4243 SPIWrite 058f,02
4244 SPIWrite 0590,33
4245 SPIWrite 0591,48
4246 SPIWrite 0592,c4
4247 SPIWrite 0593,f8
4248 SPIWrite 0594,4c
4249 SPIWrite 0595,24
4250 SPIWrite 0596,02
4251 SPIWrite 0597,22
4252 SPIWrite 0598,02
4253 SPIWrite 0599,70
4254 SPIWrite 059a,01
4255 SPIWrite 059b,20
4256 SPIWrite 059c,08
4257 SPIWrite 059d,80
4258 SPIWrite 059e,33
4259 SPIWrite 059f,49
4260 SPIWrite 05a0,0e
4261 SPIWrite 05a1,70
4262 SPIWrite 05a2,34
4263 SPIWrite 05a3,49
4264 SPIWrite 05a4,88
4265 SPIWrite 05a5,70
4266 SPIWrite 05a6,4a

4267 SPIWrite 05a7,70
4268 SPIWrite 05a8,14
4269 SPIWrite 05a9,20
4270 SPIWrite 05aa,c8
4271 SPIWrite 05ab,70
4272 SPIWrite 05ac,8e
4273 SPIWrite 05ad,20
4274 SPIWrite 05ae,88
4275 SPIWrite 05af,80
4276 SPIWrite 05b0,1d
4277 SPIWrite 05b1,48
4278 SPIWrite 05b2,c5
4279 SPIWrite 05b3,f8
4280 SPIWrite 05b4,34
4281 SPIWrite 05b5,02
4282 SPIWrite 05b6,26
4283 SPIWrite 05b7,48
4284 SPIWrite 05b8,c5
4285 SPIWrite 05b9,f8
4286 SPIWrite 05ba,f8
4287 SPIWrite 05bb,00
4288 SPIWrite 05bc,2c
4289 SPIWrite 05bd,48
4290 SPIWrite 05be,c4
4291 SPIWrite 05bf,f8
4292 SPIWrite 05c0,c8
4293 SPIWrite 05c1,04
4294 SPIWrite 05c2,70
4295 SPIWrite 05c3,bd
4296 SPIWrite 05c4,90
4297 SPIWrite 05c5,d6
4298 SPIWrite 05c6,00
4299 SPIWrite 05c7,20
4300 SPIWrite 05c8,bf
4301 SPIWrite 05c9,10
4302 SPIWrite 05ca,03
4303 SPIWrite 05cb,00
4304 SPIWrite 05cc,41
4305 SPIWrite 05cd,10
4306 SPIWrite 05ce,03
4307 SPIWrite 05cf,00
4308 SPIWrite 05d0,c1
4309 SPIWrite 05d1,0f
4310 SPIWrite 05d2,03
4311 SPIWrite 05d3,00
4312 SPIWrite 05d4,df
4313 SPIWrite 05d5,0b
4314 SPIWrite 05d6,03
4315 SPIWrite 05d7,00
4316 SPIWrite 05d8,7b
4317 SPIWrite 05d9,0a
4318 SPIWrite 05da,03
4319 SPIWrite 05db,00
4320 SPIWrite 05dc,09
4321 SPIWrite 05dd,0b
4322 SPIWrite 05de,03
4323 SPIWrite 05df,00
4324 SPIWrite 05e0,5c
4325 SPIWrite 05e1,22
4326 SPIWrite 05e2,01
4327 SPIWrite 05e3,20
4328 SPIWrite 05e4,00
4329 SPIWrite 05e5,00
4330 SPIWrite 05e6,02
4331 SPIWrite 05e7,ac
4332 SPIWrite 05e8,2c
4333 SPIWrite 05e9,22
4334 SPIWrite 05ea,01
4335 SPIWrite 05eb,20

4336 SPIWrite 05ec,40
4337 SPIWrite 05ed,78
4338 SPIWrite 05ee,7d
4339 SPIWrite 05ef,01
4340 SPIWrite 05f0,48
4341 SPIWrite 05f1,e8
4342 SPIWrite 05f2,01
4343 SPIWrite 05f3,00
4344 SPIWrite 05f4,d4
4345 SPIWrite 05f5,f7
4346 SPIWrite 05f6,00
4347 SPIWrite 05f7,20
4348 SPIWrite 05f8,09
4349 SPIWrite 05f9,11
4350 SPIWrite 05fa,03
4351 SPIWrite 05fb,00
4352 SPIWrite 05fc,2b
4353 SPIWrite 05fd,22
4354 SPIWrite 05fe,01
4355 SPIWrite 05ff,20
4356 SPIWrite 0600,57
4357 SPIWrite 0601,14
4358 SPIWrite 0602,03
4359 SPIWrite 0603,00
4360 SPIWrite 0604,4b
4361 SPIWrite 0605,14
4362 SPIWrite 0606,03
4363 SPIWrite 0607,00
4364 SPIWrite 0608,71
4365 SPIWrite 0609,15
4366 SPIWrite 060a,03
4367 SPIWrite 060b,00
4368 SPIWrite 060c,4b
4369 SPIWrite 060d,13
4370 SPIWrite 060e,03
4371 SPIWrite 060f,00
4372 SPIWrite 0610,9d
4373 SPIWrite 0611,07
4374 SPIWrite 0612,03
4375 SPIWrite 0613,00
4376 SPIWrite 0614,51
4377 SPIWrite 0615,08
4378 SPIWrite 0616,03
4379 SPIWrite 0617,00
4380 SPIWrite 0618,05
4381 SPIWrite 0619,09
4382 SPIWrite 061a,03
4383 SPIWrite 061b,00
4384 SPIWrite 061c,3b
4385 SPIWrite 061d,09
4386 SPIWrite 061e,03
4387 SPIWrite 061f,00
4388 SPIWrite 0620,38
4389 SPIWrite 0621,17
4390 SPIWrite 0622,03
4391 SPIWrite 0623,00
4392 SPIWrite 0624,60
4393 SPIWrite 0625,17
4394 SPIWrite 0626,03
4395 SPIWrite 0627,00
4396 SPIWrite 0628,05
4397 SPIWrite 0629,12
4398 SPIWrite 062a,03
4399 SPIWrite 062b,00
4400 SPIWrite 062c,67
4401 SPIWrite 062d,0f
4402 SPIWrite 062e,03
4403 SPIWrite 062f,00
4404 SPIWrite 0630,63

4405 SPIWrite 0631,22
4406 SPIWrite 0632,01
4407 SPIWrite 0633,20
4408 SPIWrite 0634,d5
4409 SPIWrite 0635,14
4410 SPIWrite 0636,03
4411 SPIWrite 0637,00
4412 SPIWrite 0638,f1
4413 SPIWrite 0639,0e
4414 SPIWrite 063a,03
4415 SPIWrite 063b,00
4416 SPIWrite 063c,f5
4417 SPIWrite 063d,15
4418 SPIWrite 063e,03
4419 SPIWrite 063f,00
4420 SPIWrite 0640,b7
4421 SPIWrite 0641,04
4422 SPIWrite 0642,03
4423 SPIWrite 0643,00
4424 SPIWrite 0644,59
4425 SPIWrite 0645,06
4426 SPIWrite 0646,03
4427 SPIWrite 0647,00
4428 SPIWrite 0648,a9
4429 SPIWrite 0649,15
4430 SPIWrite 064a,03
4431 SPIWrite 064b,00
4432 SPIWrite 064c,b7
4433 SPIWrite 064d,15
4434 SPIWrite 064e,03
4435 SPIWrite 064f,00
4436 SPIWrite 0650,1b
4437 SPIWrite 0651,11
4438 SPIWrite 0652,03
4439 SPIWrite 0653,00
4440 SPIWrite 0654,d9
4441 SPIWrite 0655,15
4442 SPIWrite 0656,03
4443 SPIWrite 0657,00
4444 SPIWrite 0658,31
4445 SPIWrite 0659,15
4446 SPIWrite 065a,03
4447 SPIWrite 065b,00
4448 SPIWrite 065c,a3
4449 SPIWrite 065d,14
4450 SPIWrite 065e,03
4451 SPIWrite 065f,00
4452 SPIWrite 0660,64
4453 SPIWrite 0661,22
4454 SPIWrite 0662,01
4455 SPIWrite 0663,20
4456 SPIWrite 0664,60
4457 SPIWrite 0665,22
4458 SPIWrite 0666,01
4459 SPIWrite 0667,20
4460 SPIWrite 0668,31
4461 SPIWrite 0669,12
4462 SPIWrite 066a,03
4463 SPIWrite 066b,00
4464 SPIWrite 066c,a1
4465 SPIWrite 066d,13
4466 SPIWrite 066e,01
4467 SPIWrite 066f,20
4468 SPIWrite 0670,f7
4469 SPIWrite 0671,15
4470 SPIWrite 0672,03
4471 SPIWrite 0673,00
4472 SPIWrite 0674,3c
4473 SPIWrite 0675,d6

4474 SPIWrite 0676,00
4475 SPIWrite 0677,20
4476 SPIWrite 0678,3a
4477 SPIWrite 0679,b1
4478 SPIWrite 067a,03
4479 SPIWrite 067b,46
4480 SPIWrite 067c,10
4481 SPIWrite 067d,46
4482 SPIWrite 067e,13
4483 SPIWrite 067f,f8
4484 SPIWrite 0680,01
4485 SPIWrite 0681,2b
4486 SPIWrite 0682,40
4487 SPIWrite 0683,1e
4488 SPIWrite 0684,01
4489 SPIWrite 0685,f8
4490 SPIWrite 0686,01
4491 SPIWrite 0687,2b
4492 SPIWrite 0688,f9
4493 SPIWrite 0689,d1
4494 SPIWrite 068a,70
4495 SPIWrite 068b,47
4496 SPIWrite 068c,38
4497 SPIWrite 068d,b5
4498 SPIWrite 068e,05
4499 SPIWrite 068f,46
4500 SPIWrite 0690,0c
4501 SPIWrite 0691,46
4502 SPIWrite 0692,28
4503 SPIWrite 0693,68
4504 SPIWrite 0694,21
4505 SPIWrite 0695,68
4506 SPIWrite 0696,0c
4507 SPIWrite 0697,22
4508 SPIWrite 0698,ff
4509 SPIWrite 0699,f7
4510 SPIWrite 069a,ee
4511 SPIWrite 069b,ff
4512 SPIWrite 069c,68
4513 SPIWrite 069d,68
4514 SPIWrite 069e,61
4515 SPIWrite 069f,68
4516 SPIWrite 06a0,05
4517 SPIWrite 06a1,22
4518 SPIWrite 06a2,ff
4519 SPIWrite 06a3,f7
4520 SPIWrite 06a4,e9
4521 SPIWrite 06a5,ff
4522 SPIWrite 06a6,a8
4523 SPIWrite 06a7,68
4524 SPIWrite 06a8,a1
4525 SPIWrite 06a9,68
4526 SPIWrite 06aa,18
4527 SPIWrite 06ab,22
4528 SPIWrite 06ac,ff
4529 SPIWrite 06ad,f7
4530 SPIWrite 06ae,e4
4531 SPIWrite 06af,ff
4532 SPIWrite 06b0,e8
4533 SPIWrite 06b1,68
4534 SPIWrite 06b2,e1
4535 SPIWrite 06b3,68
4536 SPIWrite 06b4,d2
4537 SPIWrite 06b5,22
4538 SPIWrite 06b6,ff
4539 SPIWrite 06b7,f7
4540 SPIWrite 06b8,df
4541 SPIWrite 06b9,ff
4542 SPIWrite 06ba,28

4543 SPIWrite 06bb,69
4544 SPIWrite 06bc,21
4545 SPIWrite 06bd,69
4546 SPIWrite 06be,96
4547 SPIWrite 06bf,22
4548 SPIWrite 06c0,ff
4549 SPIWrite 06c1,f7
4550 SPIWrite 06c2,da
4551 SPIWrite 06c3,ff
4552 SPIWrite 06c4,38
4553 SPIWrite 06c5,bd
4554 SPIWrite 06c6,b0
4555 SPIWrite 06c7,b5
4556 SPIWrite 06c8,39
4557 SPIWrite 06c9,49
4558 SPIWrite 06ca,3a
4559 SPIWrite 06cb,4d
4560 SPIWrite 06cc,00
4561 SPIWrite 06cd,f0
4562 SPIWrite 06ce,01
4563 SPIWrite 06cf,02
4564 SPIWrite 06d0,04
4565 SPIWrite 06d1,27
4566 SPIWrite 06d2,12
4567 SPIWrite 06d3,04
4568 SPIWrite 06d4,08
4569 SPIWrite 06d5,70
4570 SPIWrite 06d6,55
4571 SPIWrite 06d7,f8
4572 SPIWrite 06d8,04
4573 SPIWrite 06d9,4b
4574 SPIWrite 06da,d4
4575 SPIWrite 06db,f8
4576 SPIWrite 06dc,80
4577 SPIWrite 06dd,1b
4578 SPIWrite 06de,21
4579 SPIWrite 06df,f4
4580 SPIWrite 06e0,80
4581 SPIWrite 06e1,31
4582 SPIWrite 06e2,11
4583 SPIWrite 06e3,43
4584 SPIWrite 06e4,c4
4585 SPIWrite 06e5,f8
4586 SPIWrite 06e6,80
4587 SPIWrite 06e7,1b
4588 SPIWrite 06e8,d4
4589 SPIWrite 06e9,f8
4590 SPIWrite 06ea,48
4591 SPIWrite 06eb,3b
4592 SPIWrite 06ec,7f
4593 SPIWrite 06ed,1e
4594 SPIWrite 06ee,80
4595 SPIWrite 06ef,ea
4596 SPIWrite 06f0,03
4597 SPIWrite 06f1,01
4598 SPIWrite 06f2,01
4599 SPIWrite 06f3,f0
4600 SPIWrite 06f4,01
4601 SPIWrite 06f5,01
4602 SPIWrite 06f6,81
4603 SPIWrite 06f7,ea
4604 SPIWrite 06f8,03
4605 SPIWrite 06f9,01
4606 SPIWrite 06fa,c4
4607 SPIWrite 06fb,f8
4608 SPIWrite 06fc,48
4609 SPIWrite 06fd,1b
4610 SPIWrite 06fe,ea
4611 SPIWrite 06ff,d1

4612 SPIWrite 0700,01
4613 SPIWrite 0701,28
4614 SPIWrite 0702,0c
4615 SPIWrite 0703,bf
4616 SPIWrite 0704,2c
4617 SPIWrite 0705,48
4618 SPIWrite 0706,2d
4619 SPIWrite 0707,48
4620 SPIWrite 0708,2d
4621 SPIWrite 0709,49
4622 SPIWrite 070a,ff
4623 SPIWrite 070b,f7
4624 SPIWrite 070c,bf
4625 SPIWrite 070d,ff
4626 SPIWrite 070e,b0
4627 SPIWrite 070f,bd
4628 SPIWrite 0710,8c
4629 SPIWrite 0711,46
4630 SPIWrite 0712,2c
4631 SPIWrite 0713,49
4632 SPIWrite 0714,f8
4633 SPIWrite 0715,b5
4634 SPIWrite 0716,09
4635 SPIWrite 0717,5c
4636 SPIWrite 0718,01
4637 SPIWrite 0719,29
4638 SPIWrite 071a,12
4639 SPIWrite 071b,d1
4640 SPIWrite 071c,2a
4641 SPIWrite 071d,49
4642 SPIWrite 071e,46
4643 SPIWrite 071f,01
4644 SPIWrite 0720,02
4645 SPIWrite 0721,23
4646 SPIWrite 0722,00
4647 SPIWrite 0723,24
4648 SPIWrite 0724,32
4649 SPIWrite 0725,19
4650 SPIWrite 0726,02
4651 SPIWrite 0727,27
4652 SPIWrite 0728,8a
4653 SPIWrite 0729,18
4654 SPIWrite 072a,b2
4655 SPIWrite 072b,f9
4656 SPIWrite 072c,00
4657 SPIWrite 072d,50
4658 SPIWrite 072e,7f
4659 SPIWrite 072f,1e
4660 SPIWrite 0730,4f
4661 SPIWrite 0731,ea
4662 SPIWrite 0732,45
4663 SPIWrite 0733,05
4664 SPIWrite 0734,22
4665 SPIWrite 0735,f8
4666 SPIWrite 0736,10
4667 SPIWrite 0737,5b
4668 SPIWrite 0738,f7
4669 SPIWrite 0739,d1
4670 SPIWrite 073a,5b
4671 SPIWrite 073b,1e
4672 SPIWrite 073c,04
4673 SPIWrite 073d,f1
4674 SPIWrite 073e,08
4675 SPIWrite 073f,04
4676 SPIWrite 0740,f0
4677 SPIWrite 0741,d1
4678 SPIWrite 0742,61
4679 SPIWrite 0743,46
4680 SPIWrite 0744,e1

4681 SPIWrite 0745,f7
4682 SPIWrite 0746,f0
4683 SPIWrite 0747,fe
4684 SPIWrite 0748,f8
4685 SPIWrite 0749,bd
4686 SPIWrite 074a,98
4687 SPIWrite 074b,b5
4688 SPIWrite 074c,1f
4689 SPIWrite 074d,4c
4690 SPIWrite 074e,00
4691 SPIWrite 074f,21
4692 SPIWrite 0750,84
4693 SPIWrite 0751,f8
4694 SPIWrite 0752,24
4695 SPIWrite 0753,10
4696 SPIWrite 0754,1f
4697 SPIWrite 0755,48
4698 SPIWrite 0756,84
4699 SPIWrite 0757,f8
4700 SPIWrite 0758,25
4701 SPIWrite 0759,10
4702 SPIWrite 075a,03
4703 SPIWrite 075b,22
4704 SPIWrite 075c,84
4705 SPIWrite 075d,f8
4706 SPIWrite 075e,29
4707 SPIWrite 075f,10
4708 SPIWrite 0760,1b
4709 SPIWrite 0761,4b
4710 SPIWrite 0762,84
4711 SPIWrite 0763,f8
4712 SPIWrite 0764,2a
4713 SPIWrite 0765,10
4714 SPIWrite 0766,0a
4715 SPIWrite 0767,21
4716 SPIWrite 0768,40
4717 SPIWrite 0769,1e
4718 SPIWrite 076a,10
4719 SPIWrite 076b,f8
4720 SPIWrite 076c,01
4721 SPIWrite 076d,4f
4722 SPIWrite 076e,05
4723 SPIWrite 076f,27
4724 SPIWrite 0770,7f
4725 SPIWrite 0771,1e
4726 SPIWrite 0772,03
4727 SPIWrite 0773,f8
4728 SPIWrite 0774,01
4729 SPIWrite 0775,4b
4730 SPIWrite 0776,fb
4731 SPIWrite 0777,d1
4732 SPIWrite 0778,49
4733 SPIWrite 0779,1e
4734 SPIWrite 077a,f6
4735 SPIWrite 077b,d1
4736 SPIWrite 077c,52
4737 SPIWrite 077d,1e
4738 SPIWrite 077e,00
4739 SPIWrite 077f,f1
4740 SPIWrite 0780,01
4741 SPIWrite 0781,00
4742 SPIWrite 0782,f0
4743 SPIWrite 0783,d1
4744 SPIWrite 0784,98
4745 SPIWrite 0785,bd
4746 SPIWrite 0786,0a
4747 SPIWrite 0787,4a
4748 SPIWrite 0788,80
4749 SPIWrite 0789,b5

4750 SPIWrite 078a,12
4751 SPIWrite 078b,78
4752 SPIWrite 078c,01
4753 SPIWrite 078d,2a
4754 SPIWrite 078e,0c
4755 SPIWrite 078f,d1
4756 SPIWrite 0790,11
4757 SPIWrite 0791,4b
4758 SPIWrite 0792,42
4759 SPIWrite 0793,10
4760 SPIWrite 0794,9a
4761 SPIWrite 0795,5c
4762 SPIWrite 0796,92
4763 SPIWrite 0797,1e
4764 SPIWrite 0798,d7
4765 SPIWrite 0799,b2
4766 SPIWrite 079a,1f
4767 SPIWrite 079b,b1
4768 SPIWrite 079c,01
4769 SPIWrite 079d,2f
4770 SPIWrite 079e,04
4771 SPIWrite 079f,d1
4772 SPIWrite 07a0,05
4773 SPIWrite 07a1,22
4774 SPIWrite 07a2,00
4775 SPIWrite 07a3,e0
4776 SPIWrite 07a4,07
4777 SPIWrite 07a5,22
4778 SPIWrite 07a6,0d
4779 SPIWrite 07a7,4b
4780 SPIWrite 07a8,1a
4781 SPIWrite 07a9,70
4782 SPIWrite 07aa,d8
4783 SPIWrite 07ab,f7
4784 SPIWrite 07ac,bb
4785 SPIWrite 07ad,fc
4786 SPIWrite 07ae,80
4787 SPIWrite 07af,bd
4788 SPIWrite 07b0,63
4789 SPIWrite 07b1,22
4790 SPIWrite 07b2,01
4791 SPIWrite 07b3,20
4792 SPIWrite 07b4,bc
4793 SPIWrite 07b5,77
4794 SPIWrite 07b6,02
4795 SPIWrite 07b7,00
4796 SPIWrite 07b8,4c
4797 SPIWrite 07b9,17
4798 SPIWrite 07ba,03
4799 SPIWrite 07bb,00
4800 SPIWrite 07bc,60
4801 SPIWrite 07bd,17
4802 SPIWrite 07be,03
4803 SPIWrite 07bf,00
4804 SPIWrite 07c0,38
4805 SPIWrite 07c1,17
4806 SPIWrite 07c2,03
4807 SPIWrite 07c3,00
4808 SPIWrite 07c4,ac
4809 SPIWrite 07c5,fe
4810 SPIWrite 07c6,00
4811 SPIWrite 07c7,20
4812 SPIWrite 07c8,28
4813 SPIWrite 07c9,fd
4814 SPIWrite 07ca,00
4815 SPIWrite 07cb,20
4816 SPIWrite 07cc,4a
4817 SPIWrite 07cd,0c
4818 SPIWrite 07ce,01

4819 SPIWrite 07cf,20
4820 SPIWrite 07d0,fb
4821 SPIWrite 07d1,20
4822 SPIWrite 07d2,01
4823 SPIWrite 07d3,20
4824 SPIWrite 07d4,17
4825 SPIWrite 07d5,17
4826 SPIWrite 07d6,03
4827 SPIWrite 07d7,00
4828 SPIWrite 07d8,a2
4829 SPIWrite 07d9,01
4830 SPIWrite 07da,01
4831 SPIWrite 07db,20
4832 SPIWrite 07dc,d4
4833 SPIWrite 07dd,1e
4834 SPIWrite 07de,01
4835 SPIWrite 07df,20
4836 SPIWrite 07e0,2d
4837 SPIWrite 07e1,e9
4838 SPIWrite 07e2,f0
4839 SPIWrite 07e3,41
4840 SPIWrite 07e4,04
4841 SPIWrite 07e5,46
4842 SPIWrite 07e6,4a
4843 SPIWrite 07e7,48
4844 SPIWrite 07e8,0d
4845 SPIWrite 07e9,46
4846 SPIWrite 07ea,a7
4847 SPIWrite 07eb,00
4848 SPIWrite 07ec,c1
4849 SPIWrite 07ed,5d
4850 SPIWrite 07ee,1e
4851 SPIWrite 07ef,46
4852 SPIWrite 07f0,8d
4853 SPIWrite 07f1,42
4854 SPIWrite 07f2,07
4855 SPIWrite 07f3,44
4856 SPIWrite 07f4,08
4857 SPIWrite 07f5,d0
4858 SPIWrite 07f6,b9
4859 SPIWrite 07f7,78
4860 SPIWrite 07f8,8d
4861 SPIWrite 07f9,42
4862 SPIWrite 07fa,18
4863 SPIWrite 07fb,bf
4864 SPIWrite 07fc,04
4865 SPIWrite 07fd,27
4866 SPIWrite 07fe,13
4867 SPIWrite 07ff,d1
4868 SPIWrite 0800,01
4869 SPIWrite 0801,21
4870 SPIWrite 0802,01
4871 SPIWrite 0803,eb
4872 SPIWrite 0804,44
4873 SPIWrite 0805,01
4874 SPIWrite 0806,00
4875 SPIWrite 0807,e0
4876 SPIWrite 0808,61
4877 SPIWrite 0809,00
4878 SPIWrite 080a,cf
4879 SPIWrite 080b,b2
4880 SPIWrite 080c,04
4881 SPIWrite 080d,2f
4882 SPIWrite 080e,0b
4883 SPIWrite 080f,d0
4884 SPIWrite 0810,40
4885 SPIWrite 0811,49
4886 SPIWrite 0812,00
4887 SPIWrite 0813,eb

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4888 SPIWrite 0814,47
4889 SPIWrite 0815,00
4890 SPIWrite 0816,0a
4891 SPIWrite 0817,5d
4892 SPIWrite 0818,41
4893 SPIWrite 0819,78
4894 SPIWrite 081a,90
4895 SPIWrite 081b,46
4896 SPIWrite 081c,04
4897 SPIWrite 081d,29
4898 SPIWrite 081e,04
4899 SPIWrite 081f,d0
4900 SPIWrite 0018,00 //sys_calib_macro_memory=0x0; Address(0x18[7:0])
4901 SPIWrite 0018,20 //macro=0x1; Address(0x18[7:5])
4902 SPIRead 00f0
4903
4904 //Read MACRO_READY=0x1; Address(0xf0[7:0])
4905
4906
4907 SPIPoll 00f0,0,0,1
4908
4909 SPIWrite 00a3,08 //MACRO_OPERAND_REG0=0x8000000;
Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
4910 SPIWrite 00a2,00
4911 SPIWrite 00a1,00
4912 SPIWrite 00a0,00
4913 SPIWrite 00a7,00 //MACRO_OPERAND_REG1=0x800;
Address(0xa4[7:0],0xa5[7:0],0xa6[7:0],0xa7[7:0],0xa8[7:0])
4914 SPIWrite 00a6,00
4915 SPIWrite 00a5,08
4916 SPIWrite 00a4,00
4917 SPIWrite 0193,78 //MACRO_OPCODE=0x78; Address(0x193[7:0],0x194[7:0])
4918
4919 WAIT 0.001
4920 SPIRead 00f0
4921
4922 //Read MACRO_DONE=0x1; Address(0xf0[7:2])
4923
4924
4925 SPIPoll 00f0,2,2,4
4926
4927 SPIRead 00f0
4928
4929 //Read MACRO_ERROR=0x0; Address(0xf0[7:3])
4930
4931 SPIRead 00f1
4932
4933 //Read MACRO_ERROR_OPCODE=0x0; Address(0xf1[7:0],0xf2[7:0])
4934
4935 SPIRead 00f0
4936
4937 //Read MACRO_ERROR_IN_OPCODE=0x0; Address(0xf0[7:4])
4938
4939 SPIRead 00f0
4940
4941 //Read MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0; Address(0xf0[7:5])
4942
4943 SPIRead 00f0
4944
4945 //Read MACRO_ERROR_IN_OPERAND=0x0; Address(0xf0[7:6])
4946
4947 SPIRead 00f0
4948
4949 //Read MACRO_ERROR_IN_EXECUTION=0x0; Address(0xf0[7:7])
4950
4951 SPIRead 00f3
4952 SPIRead 00f2
4953
4954 //Read MACRO_ERROR_EXTENDED_CODE=0x0; Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

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4955
4956 SPIRead 00f7
4957 SPIRead 00f6
4958 SPIRead 00f5
4959 SPIRead 00f4
4960
4961 //Read MACRO_ERROR_EXTENDED_CODE 2=0x0;
Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
4962
4963 SPIWrite 0144,00 //all_addr_high=0x0; Address(0x144[7:2])
4964 SPIWrite 0018,00 //macro=0x0; Address(0x18[7:5])
4965 SPIWrite 0018,01 //sys_calib_macro_memory=0x1; Address(0x18[7:0])
4966 SPIWrite 0020,20
4967 SPIWrite 0021,46
4968 SPIWrite 0022,de
4969 SPIWrite 0023,f7
4970 SPIWrite 0024,15
4971 SPIWrite 0025,fb
4972 SPIWrite 0026,00
4973 SPIWrite 0027,e0
4974 SPIWrite 0028,90
4975 SPIWrite 0029,46
4976 SPIWrite 002a,20
4977 SPIWrite 002b,46
4978 SPIWrite 002c,29
4979 SPIWrite 002d,46
4980 SPIWrite 002e,33
4981 SPIWrite 002f,46
4982 SPIWrite 0030,42
4983 SPIWrite 0031,46
4984 SPIWrite 0032,de
4985 SPIWrite 0033,f7
4986 SPIWrite 0034,0d
4987 SPIWrite 0035,fb
4988 SPIWrite 0036,04
4989 SPIWrite 0037,2f
4990 SPIWrite 0038,10
4991 SPIWrite 0039,d0
4992 SPIWrite 003a,38
4993 SPIWrite 003b,4b
4994 SPIWrite 003c,36
4995 SPIWrite 003d,49
4996 SPIWrite 003e,0c
4997 SPIWrite 003f,20
4998 SPIWrite 0040,14
4999 SPIWrite 0041,fb
5000 SPIWrite 0042,00
5001 SPIWrite 0043,f0
5002 SPIWrite 0044,00
5003 SPIWrite 0045,eb
5004 SPIWrite 0046,85
5005 SPIWrite 0047,02
5006 SPIWrite 0048,13
5007 SPIWrite 0049,f8
5008 SPIWrite 004a,17
5009 SPIWrite 004b,30
5010 SPIWrite 004c,8a
5011 SPIWrite 004d,58
5012 SPIWrite 004e,00
5013 SPIWrite 004f,eb
5014 SPIWrite 0050,83
5015 SPIWrite 0051,00
5016 SPIWrite 0052,92
5017 SPIWrite 0053,f8
5018 SPIWrite 0054,02
5019 SPIWrite 0055,26
5020 SPIWrite 0056,08
5021 SPIWrite 0057,58
5022 SPIWrite 0058,80
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5023 SPIWrite 0059,f8
5024 SPIWrite 005a,02
5025 SPIWrite 005b,26
5026 SPIWrite 005c,bd
5027 SPIWrite 005d,e8
5028 SPIWrite 005e,f0
5029 SPIWrite 005f,81
5030 SPIWrite 0060,70
5031 SPIWrite 0061,b5
5032 SPIWrite 0062,05
5033 SPIWrite 0063,46
5034 SPIWrite 0064,0c
5035 SPIWrite 0065,46
5036 SPIWrite 0066,de
5037 SPIWrite 0067,f7
5038 SPIWrite 0068,a3
5039 SPIWrite 0069,ff
5040 SPIWrite 006a,2d
5041 SPIWrite 006b,48
5042 SPIWrite 006c,2a
5043 SPIWrite 006d,4a
5044 SPIWrite 006e,4f
5045 SPIWrite 006f,f4
5046 SPIWrite 0070,25
5047 SPIWrite 0071,76
5048 SPIWrite 0072,15
5049 SPIWrite 0073,fb
5050 SPIWrite 0074,06
5051 SPIWrite 0075,f6
5052 SPIWrite 0076,0c
5053 SPIWrite 0077,21
5054 SPIWrite 0078,dc
5055 SPIWrite 0079,23
5056 SPIWrite 007a,15
5057 SPIWrite 007b,fb
5058 SPIWrite 007c,01
5059 SPIWrite 007d,f1
5060 SPIWrite 007e,14
5061 SPIWrite 007f,fb
5062 SPIWrite 0080,03
5063 SPIWrite 0081,63
5064 SPIWrite 0082,01
5065 SPIWrite 0083,eb
5066 SPIWrite 0084,84
5067 SPIWrite 0085,01
5068 SPIWrite 0086,c0
5069 SPIWrite 0087,18
5070 SPIWrite 0088,54
5071 SPIWrite 0089,58
5072 SPIWrite 008a,90
5073 SPIWrite 008b,f8
5074 SPIWrite 008c,74
5075 SPIWrite 008d,10
5076 SPIWrite 008e,90
5077 SPIWrite 008f,f8
5078 SPIWrite 0090,42
5079 SPIWrite 0091,20
5080 SPIWrite 0092,d4
5081 SPIWrite 0093,f8
5082 SPIWrite 0094,3c
5083 SPIWrite 0095,66
5084 SPIWrite 0096,52
5085 SPIWrite 0097,18
5086 SPIWrite 0098,92
5087 SPIWrite 0099,1e
5088 SPIWrite 009a,06
5089 SPIWrite 009b,21
5090 SPIWrite 009c,d2
5091 SPIWrite 009d,b2

5092 SPIWrite 009e,0d
5093 SPIWrite 009f,46
5094 SPIWrite 00a0,b2
5095 SPIWrite 00a1,fb
5096 SPIWrite 00a2,f1
5097 SPIWrite 00a3,f1
5098 SPIWrite 00a4,11
5099 SPIWrite 00a5,fb
5100 SPIWrite 00a6,05
5101 SPIWrite 00a7,f3
5102 SPIWrite 00a8,d2
5103 SPIWrite 00a9,1a
5104 SPIWrite 00aa,6f
5105 SPIWrite 00ab,f0
5106 SPIWrite 00ac,02
5107 SPIWrite 00ad,03
5108 SPIWrite 00ae,d2
5109 SPIWrite 00af,b2
5110 SPIWrite 00b0,9b
5111 SPIWrite 00b1,1a
5112 SPIWrite 00b2,63
5113 SPIWrite 00b3,f3
5114 SPIWrite 00b4,12
5115 SPIWrite 00b5,46
5116 SPIWrite 00b6,c4
5117 SPIWrite 00b7,f8
5118 SPIWrite 00b8,3c
5119 SPIWrite 00b9,66
5120 SPIWrite 00ba,90
5121 SPIWrite 00bb,f8
5122 SPIWrite 00bc,42
5123 SPIWrite 00bd,00
5124 SPIWrite 00be,d4
5125 SPIWrite 00bf,f8
5126 SPIWrite 00c0,3c
5127 SPIWrite 00c1,26
5128 SPIWrite 00c2,00
5129 SPIWrite 00c3,1d
5130 SPIWrite 00c4,90
5131 SPIWrite 00c5,fb
5132 SPIWrite 00c6,f5
5133 SPIWrite 00c7,f3
5134 SPIWrite 00c8,4f
5135 SPIWrite 00c9,f4
5136 SPIWrite 00ca,00
5137 SPIWrite 00cb,20
5138 SPIWrite 00cc,c9
5139 SPIWrite 00cd,1a
5140 SPIWrite 00ce,00
5141 SPIWrite 00cf,eb
5142 SPIWrite 00d0,c1
5143 SPIWrite 00d1,40
5144 SPIWrite 00d2,c0
5145 SPIWrite 00d3,0c
5146 SPIWrite 00d4,60
5147 SPIWrite 00d5,f3
5148 SPIWrite 00d6,d7
5149 SPIWrite 00d7,42
5150 SPIWrite 00d8,c4
5151 SPIWrite 00d9,f8
5152 SPIWrite 00da,3c
5153 SPIWrite 00db,26
5154 SPIWrite 00dc,70
5155 SPIWrite 00dd,bd
5156 SPIWrite 00de,38
5157 SPIWrite 00df,b5
5158 SPIWrite 00e0,0f
5159 SPIWrite 00e1,4a
5160 SPIWrite 00e2,10

5161 SPIWrite 00e3,4c
5162 SPIWrite 00e4,4f
5163 SPIWrite 00e5,f4
5164 SPIWrite 00e6,25
5165 SPIWrite 00e7,75
5166 SPIWrite 00e8,dc
5167 SPIWrite 00e9,23
5168 SPIWrite 00ea,10
5169 SPIWrite 00eb,fb
5170 SPIWrite 00ec,05
5171 SPIWrite 00ed,f5
5172 SPIWrite 00ee,b1
5173 SPIWrite 00ef,32
5174 SPIWrite 00f0,11
5175 SPIWrite 00f1,fb
5176 SPIWrite 00f2,03
5177 SPIWrite 00f3,53
5178 SPIWrite 00f4,d2
5179 SPIWrite 00f5,5c
5180 SPIWrite 00f6,94
5181 SPIWrite 00f7,f9
5182 SPIWrite 00f8,01
5183 SPIWrite 00f9,50
5184 SPIWrite 00fa,03
5185 SPIWrite 00fb,2a
5186 SPIWrite 00fc,03
5187 SPIWrite 00fd,d0
5188 SPIWrite 00fe,94
5189 SPIWrite 00ff,f9
5190 SPIWrite 0100,01
5191 SPIWrite 0101,20
5192 SPIWrite 0102,92
5193 SPIWrite 0103,1f
5194 SPIWrite 0104,62
5195 SPIWrite 0105,70
5196 SPIWrite 0106,df
5197 SPIWrite 0107,f7
5198 SPIWrite 0108,99
5199 SPIWrite 0109,f9
5200 SPIWrite 010a,65
5201 SPIWrite 010b,70
5202 SPIWrite 010c,38
5203 SPIWrite 010d,bd
5204 SPIWrite 010e,c0
5205 SPIWrite 010f,46
5206 SPIWrite 0110,fe
5207 SPIWrite 0111,d5
5208 SPIWrite 0112,00
5209 SPIWrite 0113,20
5210 SPIWrite 0114,b6
5211 SPIWrite 0115,01
5212 SPIWrite 0116,01
5213 SPIWrite 0117,20
5214 SPIWrite 0118,a8
5215 SPIWrite 0119,75
5216 SPIWrite 011a,02
5217 SPIWrite 011b,00
5218 SPIWrite 011c,06
5219 SPIWrite 011d,d6
5220 SPIWrite 011e,00
5221 SPIWrite 011f,20
5222 SPIWrite 0120,e0
5223 SPIWrite 0121,ab
5224 SPIWrite 0122,00
5225 SPIWrite 0123,20
5226 SPIWrite 0124,36
5227 SPIWrite 0125,d6
5228 SPIWrite 0126,00
5229 SPIWrite 0127,20

5230 SPIWrite 0128,43
5231 SPIWrite 0129,48
5232 SPIWrite 012a,10
5233 SPIWrite 012b,b5
5234 SPIWrite 012c,00
5235 SPIWrite 012d,78
5236 SPIWrite 012e,0c
5237 SPIWrite 012f,46
5238 SPIWrite 0130,ff
5239 SPIWrite 0131,f7
5240 SPIWrite 0132,a7
5241 SPIWrite 0133,f9
5242 SPIWrite 0134,00
5243 SPIWrite 0135,20
5244 SPIWrite 0136,20
5245 SPIWrite 0137,70
5246 SPIWrite 0138,10
5247 SPIWrite 0139,bd
5248 SPIWrite 013a,3f
5249 SPIWrite 013b,48
5250 SPIWrite 013c,2d
5251 SPIWrite 013d,e9
5252 SPIWrite 013e,f0
5253 SPIWrite 013f,41
5254 SPIWrite 0140,05
5255 SPIWrite 0141,78
5256 SPIWrite 0142,3f
5257 SPIWrite 0143,4f
5258 SPIWrite 0144,3d
5259 SPIWrite 0145,48
5260 SPIWrite 0146,00
5261 SPIWrite 0147,22
5262 SPIWrite 0148,0c
5263 SPIWrite 0149,46
5264 SPIWrite 014a,2e
5265 SPIWrite 014b,01
5266 SPIWrite 014c,c7
5267 SPIWrite 014d,eb
5268 SPIWrite 014e,82
5269 SPIWrite 014f,01
5270 SPIWrite 0150,0b
5271 SPIWrite 0151,68
5272 SPIWrite 0152,02
5273 SPIWrite 0153,f0
5274 SPIWrite 0154,01
5275 SPIWrite 0155,0c
5276 SPIWrite 0156,42
5277 SPIWrite 0157,f3
5278 SPIWrite 0158,5d
5279 SPIWrite 0159,01
5280 SPIWrite 015a,52
5281 SPIWrite 015b,1c
5282 SPIWrite 015c,89
5283 SPIWrite 015d,00
5284 SPIWrite 015e,04
5285 SPIWrite 015f,2a
5286 SPIWrite 0160,01
5287 SPIWrite 0161,eb
5288 SPIWrite 0162,cc
5289 SPIWrite 0163,01
5290 SPIWrite 0164,31
5291 SPIWrite 0165,44
5292 SPIWrite 0166,01
5293 SPIWrite 0167,44
5294 SPIWrite 0168,cb
5295 SPIWrite 0169,67
5296 SPIWrite 016a,ef
5297 SPIWrite 016b,db
5298 SPIWrite 016c,df

5299 SPIWrite 016d,f8
5300 SPIWrite 016e,d8
5301 SPIWrite 016f,80
5302 SPIWrite 0170,34
5303 SPIWrite 0171,4f
5304 SPIWrite 0172,90
5305 SPIWrite 0173,f8
5306 SPIWrite 0174,c2
5307 SPIWrite 0175,20
5308 SPIWrite 0176,d8
5309 SPIWrite 0177,f8
5310 SPIWrite 0178,50
5311 SPIWrite 0179,37
5312 SPIWrite 017a,39
5313 SPIWrite 017b,46
5314 SPIWrite 017c,98
5315 SPIWrite 017d,47
5316 SPIWrite 017e,33
5317 SPIWrite 017f,4e
5318 SPIWrite 0180,d8
5319 SPIWrite 0181,f8
5320 SPIWrite 0182,68
5321 SPIWrite 0183,39
5322 SPIWrite 0184,28
5323 SPIWrite 0185,46
5324 SPIWrite 0186,39
5325 SPIWrite 0187,46
5326 SPIWrite 0188,32
5327 SPIWrite 0189,46
5328 SPIWrite 018a,98
5329 SPIWrite 018b,47
5330 SPIWrite 018c,a8
5331 SPIWrite 018d,19
5332 SPIWrite 018e,00
5333 SPIWrite 018f,f5
5334 SPIWrite 0190,33
5335 SPIWrite 0191,70
5336 SPIWrite 0192,07
5337 SPIWrite 0193,78
5338 SPIWrite 0194,00
5339 SPIWrite 0195,2f
5340 SPIWrite 0196,31
5341 SPIWrite 0197,d1
5342 SPIWrite 0198,d8
5343 SPIWrite 0199,f8
5344 SPIWrite 019a,60
5345 SPIWrite 019b,29
5346 SPIWrite 019c,28
5347 SPIWrite 019d,46
5348 SPIWrite 019e,21
5349 SPIWrite 019f,46
5350 SPIWrite 01a0,90
5351 SPIWrite 01a1,47
5352 SPIWrite 01a2,20
5353 SPIWrite 01a3,78
5354 SPIWrite 01a4,00
5355 SPIWrite 01a5,28
5356 SPIWrite 01a6,3b
5357 SPIWrite 01a7,d1
5358 SPIWrite 01a8,d8
5359 SPIWrite 01a9,f8
5360 SPIWrite 01aa,70
5361 SPIWrite 01ab,29
5362 SPIWrite 01ac,28
5363 SPIWrite 01ad,46
5364 SPIWrite 01ae,21
5365 SPIWrite 01af,46
5366 SPIWrite 01b0,90
5367 SPIWrite 01b1,47

5368 SPIWrite 01b2,20
5369 SPIWrite 01b3,78
5370 SPIWrite 01b4,a0
5371 SPIWrite 01b5,bb
5372 SPIWrite 01b6,d8
5373 SPIWrite 01b7,f8
5374 SPIWrite 01b8,38
5375 SPIWrite 01b9,26
5376 SPIWrite 01ba,28
5377 SPIWrite 01bb,46
5378 SPIWrite 01bc,21
5379 SPIWrite 01bd,46
5380 SPIWrite 01be,90
5381 SPIWrite 01bf,47
5382 SPIWrite 01c0,20
5383 SPIWrite 01c1,78
5384 SPIWrite 01c2,68
5385 SPIWrite 01c3,bb
5386 SPIWrite 01c4,d8
5387 SPIWrite 01c5,f8
5388 SPIWrite 01c6,3c
5389 SPIWrite 01c7,26
5390 SPIWrite 01c8,28
5391 SPIWrite 01c9,46
5392 SPIWrite 01ca,21
5393 SPIWrite 01cb,46
5394 SPIWrite 01cc,90
5395 SPIWrite 01cd,47
5396 SPIWrite 01ce,20
5397 SPIWrite 01cf,78
5398 SPIWrite 01d0,30
5399 SPIWrite 01d1,bb
5400 SPIWrite 01d2,d8
5401 SPIWrite 01d3,f8
5402 SPIWrite 01d4,50
5403 SPIWrite 01d5,16
5404 SPIWrite 01d6,28
5405 SPIWrite 01d7,46
5406 SPIWrite 01d8,88
5407 SPIWrite 01d9,47
5408 SPIWrite 01da,d8
5409 SPIWrite 01db,f8
5410 SPIWrite 01dc,54
5411 SPIWrite 01dd,16
5412 SPIWrite 01de,28
5413 SPIWrite 01df,46
5414 SPIWrite 01e0,88
5415 SPIWrite 01e1,47
5416 SPIWrite 01e2,d8
5417 SPIWrite 01e3,f8
5418 SPIWrite 01e4,58
5419 SPIWrite 01e5,16
5420 SPIWrite 01e6,28
5421 SPIWrite 01e7,46
5422 SPIWrite 01e8,88
5423 SPIWrite 01e9,47
5424 SPIWrite 01ea,01
5425 SPIWrite 01eb,20
5426 SPIWrite 01ec,00
5427 SPIWrite 01ed,21
5428 SPIWrite 01ee,a8
5429 SPIWrite 01ef,40
5430 SPIWrite 01f0,0a
5431 SPIWrite 01f1,46
5432 SPIWrite 01f2,c0
5433 SPIWrite 01f3,b2
5434 SPIWrite 01f4,ff
5435 SPIWrite 01f5,f7
5436 SPIWrite 01f6,4a

5437 SPIWrite 01f7,fb
5438 SPIWrite 01f8,bd
5439 SPIWrite 01f9,e8
5440 SPIWrite 01fa,f0
5441 SPIWrite 01fb,81
5442 SPIWrite 01fc,62
5443 SPIWrite 01fd,88
5444 SPIWrite 01fe,08
5445 SPIWrite 01ff,23
5446 SPIWrite 0200,01
5447 SPIWrite 0201,21
5448 SPIWrite 0202,66
5449 SPIWrite 0203,68
5450 SPIWrite 0204,23
5451 SPIWrite 0205,70
5452 SPIWrite 0206,42
5453 SPIWrite 0207,f4
5454 SPIWrite 0208,80
5455 SPIWrite 0209,42
5456 SPIWrite 020a,01
5457 SPIWrite 020b,fa
5458 SPIWrite 020c,05
5459 SPIWrite 020d,f3
5460 SPIWrite 020e,62
5461 SPIWrite 020f,80
5462 SPIWrite 0210,33
5463 SPIWrite 0211,43
5464 SPIWrite 0212,63
5465 SPIWrite 0213,60
5466 SPIWrite 0214,00
5467 SPIWrite 0215,78
5468 SPIWrite 0216,62
5469 SPIWrite 0217,68
5470 SPIWrite 0218,00
5471 SPIWrite 0219,1d
5472 SPIWrite 021a,81
5473 SPIWrite 021b,40
5474 SPIWrite 021c,11
5475 SPIWrite 021d,43
5476 SPIWrite 021e,61
5477 SPIWrite 021f,60
5478 SPIWrite 0220,bd
5479 SPIWrite 0221,e8
5480 SPIWrite 0222,f0
5481 SPIWrite 0223,81
5482 SPIWrite 0224,04
5483 SPIWrite 0225,48
5484 SPIWrite 0226,00
5485 SPIWrite 0227,78
5486 SPIWrite 0228,02
5487 SPIWrite 0229,28
5488 SPIWrite 022a,a4
5489 SPIWrite 022b,bf
5490 SPIWrite 022c,04
5491 SPIWrite 022d,20
5492 SPIWrite 022e,08
5493 SPIWrite 022f,70
5494 SPIWrite 0230,01
5495 SPIWrite 0231,da
5496 SPIWrite 0232,ff
5497 SPIWrite 0233,f7
5498 SPIWrite 0234,48
5499 SPIWrite 0235,be
5500 SPIWrite 0236,70
5501 SPIWrite 0237,47
5502 SPIWrite 0238,b4
5503 SPIWrite 0239,03
5504 SPIWrite 023a,00
5505 SPIWrite 023b,a2

5506 SPIWrite 023c,b4
5507 SPIWrite 023d,01
5508 SPIWrite 023e,01
5509 SPIWrite 023f,20
5510 SPIWrite 0240,4b
5511 SPIWrite 0241,fc
5512 SPIWrite 0242,ff
5513 SPIWrite 0243,5d
5514 SPIWrite 0244,18
5515 SPIWrite 0245,ff
5516 SPIWrite 0246,00
5517 SPIWrite 0247,20
5518 SPIWrite 0248,90
5519 SPIWrite 0249,d6
5520 SPIWrite 024a,00
5521 SPIWrite 024b,20
5522 SPIWrite 024c,d4
5523 SPIWrite 024d,fb
5524 SPIWrite 024e,00
5525 SPIWrite 024f,20
5526 SPIWrite 0250,0a
5527 SPIWrite 0251,46
5528 SPIWrite 0252,2d
5529 SPIWrite 0253,e9
5530 SPIWrite 0254,f8
5531 SPIWrite 0255,4f
5532 SPIWrite 0256,01
5533 SPIWrite 0257,46
5534 SPIWrite 0258,4f
5535 SPIWrite 0259,f0
5536 SPIWrite 025a,aa
5537 SPIWrite 025b,0a
5538 SPIWrite 025c,00
5539 SPIWrite 025d,20
5540 SPIWrite 025e,a1
5541 SPIWrite 025f,f1
5542 SPIWrite 0260,aa
5543 SPIWrite 0261,08
5544 SPIWrite 0262,d3
5545 SPIWrite 0263,46
5546 SPIWrite 0264,04
5547 SPIWrite 0265,46
5548 SPIWrite 0266,00
5549 SPIWrite 0267,92
5550 SPIWrite 0268,08
5551 SPIWrite 0269,f1
5552 SPIWrite 026a,aa
5553 SPIWrite 026b,08
5554 SPIWrite 026c,98
5555 SPIWrite 026d,f8
5556 SPIWrite 026e,a6
5557 SPIWrite 026f,20
5558 SPIWrite 0270,04
5559 SPIWrite 0271,2a
5560 SPIWrite 0272,56
5561 SPIWrite 0273,da
5562 SPIWrite 0274,98
5563 SPIWrite 0275,f8
5564 SPIWrite 0276,04
5565 SPIWrite 0277,70
5566 SPIWrite 0278,00
5567 SPIWrite 0279,2f
5568 SPIWrite 027a,52
5569 SPIWrite 027b,d0
5570 SPIWrite 027c,7f
5571 SPIWrite 027d,1e
5572 SPIWrite 027e,7a
5573 SPIWrite 027f,1c
5574 SPIWrite 0280,5f

5575 SPIWrite 0281,fa
5576 SPIWrite 0282,87
5577 SPIWrite 0283,f9
5578 SPIWrite 0284,d2
5579 SPIWrite 0285,b2
5580 SPIWrite 0286,06
5581 SPIWrite 0287,2a
5582 SPIWrite 0288,48
5583 SPIWrite 0289,da
5584 SPIWrite 028a,5b
5585 SPIWrite 028b,46
5586 SPIWrite 028c,03
5587 SPIWrite 028d,fb
5588 SPIWrite 028e,04
5589 SPIWrite 028f,13
5590 SPIWrite 0290,1d
5591 SPIWrite 0291,7c
5592 SPIWrite 0292,00
5593 SPIWrite 0293,23
5594 SPIWrite 0294,37
5595 SPIWrite 0295,e0
5596 SPIWrite 0296,c5
5597 SPIWrite 0297,18
5598 SPIWrite 0298,4d
5599 SPIWrite 0299,19
5600 SPIWrite 029a,ed
5601 SPIWrite 029b,7d
5602 SPIWrite 029c,09
5603 SPIWrite 029d,26
5604 SPIWrite 029e,19
5605 SPIWrite 029f,fb
5606 SPIWrite 02a0,06
5607 SPIWrite 02a1,f6
5608 SPIWrite 02a2,77
5609 SPIWrite 02a3,19
5610 SPIWrite 02a4,c7
5611 SPIWrite 02a5,19
5612 SPIWrite 02a6,cf
5613 SPIWrite 02a7,19
5614 SPIWrite 02a8,97
5615 SPIWrite 02a9,f9
5616 SPIWrite 02aa,22
5617 SPIWrite 02ab,e0
5618 SPIWrite 02ac,02
5619 SPIWrite 02ad,eb
5620 SPIWrite 02ae,c2
5621 SPIWrite 02af,0c
5622 SPIWrite 02b0,ae
5623 SPIWrite 02b1,19
5624 SPIWrite 02b2,86
5625 SPIWrite 02b3,19
5626 SPIWrite 02b4,47
5627 SPIWrite 02b5,19
5628 SPIWrite 02b6,8e
5629 SPIWrite 02b7,19
5630 SPIWrite 02b8,67
5631 SPIWrite 02b9,44
5632 SPIWrite 02ba,cf
5633 SPIWrite 02bb,19
5634 SPIWrite 02bc,87
5635 SPIWrite 02bd,f8
5636 SPIWrite 02be,22
5637 SPIWrite 02bf,e0
5638 SPIWrite 02c0,96
5639 SPIWrite 02c1,f9
5640 SPIWrite 02c2,58
5641 SPIWrite 02c3,70
5642 SPIWrite 02c4,46
5643 SPIWrite 02c5,19

5644 SPIWrite 02c6,0b
5645 SPIWrite 02c7,fb
5646 SPIWrite 02c8,04
5647 SPIWrite 02c9,f0
5648 SPIWrite 02ca,0c
5649 SPIWrite 02cb,eb
5650 SPIWrite 02cc,06
5651 SPIWrite 02cd,05
5652 SPIWrite 02ce,4e
5653 SPIWrite 02cf,19
5654 SPIWrite 02d0,0d
5655 SPIWrite 02d1,18
5656 SPIWrite 02d2,86
5657 SPIWrite 02d3,f8
5658 SPIWrite 02d4,58
5659 SPIWrite 02d5,70
5660 SPIWrite 02d6,ad
5661 SPIWrite 02d7,7d
5662 SPIWrite 02d8,5b
5663 SPIWrite 02d9,1c
5664 SPIWrite 02da,db
5665 SPIWrite 02db,b2
5666 SPIWrite 02dc,19
5667 SPIWrite 02dd,e0
5668 SPIWrite 02de,03
5669 SPIWrite 02df,25
5670 SPIWrite 02e0,19
5671 SPIWrite 02e1,fb
5672 SPIWrite 02e2,05
5673 SPIWrite 02e3,35
5674 SPIWrite 02e4,45
5675 SPIWrite 02e5,19
5676 SPIWrite 02e6,4d
5677 SPIWrite 02e7,19
5678 SPIWrite 02e8,95
5679 SPIWrite 02e9,f8
5680 SPIWrite 02ea,8e
5681 SPIWrite 02eb,70
5682 SPIWrite 02ec,02
5683 SPIWrite 02ed,eb
5684 SPIWrite 02ee,42
5685 SPIWrite 02ef,06
5686 SPIWrite 02f0,9d
5687 SPIWrite 02f1,19
5688 SPIWrite 02f2,45
5689 SPIWrite 02f3,19
5690 SPIWrite 02f4,0a
5691 SPIWrite 02f5,fb
5692 SPIWrite 02f6,04
5693 SPIWrite 02f7,f0
5694 SPIWrite 02f8,4e
5695 SPIWrite 02f9,19
5696 SPIWrite 02fa,0d
5697 SPIWrite 02fb,18
5698 SPIWrite 02fc,86
5699 SPIWrite 02fd,f8
5700 SPIWrite 02fe,8e
5701 SPIWrite 02ff,70
5702 SPIWrite 0300,2d
5703 SPIWrite 0301,7c
5704 SPIWrite 0302,5b
5705 SPIWrite 0303,1c
5706 SPIWrite 0304,db
5707 SPIWrite 0305,b2
5708 SPIWrite 0306,9d
5709 SPIWrite 0307,42
5710 SPIWrite 0308,e9
5711 SPIWrite 0309,dc
5712 SPIWrite 030a,0a

5713 SPIWrite 030b,fb
5714 SPIWrite 030c,04
5715 SPIWrite 030d,13
5716 SPIWrite 030e,9d
5717 SPIWrite 030f,7d
5718 SPIWrite 0310,00
5719 SPIWrite 0311,23
5720 SPIWrite 0312,9d
5721 SPIWrite 0313,42
5722 SPIWrite 0314,bf
5723 SPIWrite 0315,dc
5724 SPIWrite 0316,52
5725 SPIWrite 0317,1c
5726 SPIWrite 0318,06
5727 SPIWrite 0319,2a
5728 SPIWrite 031a,b6
5729 SPIWrite 031b,db
5730 SPIWrite 031c,06
5731 SPIWrite 031d,22
5732 SPIWrite 031e,88
5733 SPIWrite 031f,f8
5734 SPIWrite 0320,04
5735 SPIWrite 0321,20
5736 SPIWrite 0322,64
5737 SPIWrite 0323,1c
5738 SPIWrite 0324,aa
5739 SPIWrite 0325,30
5740 SPIWrite 0326,06
5741 SPIWrite 0327,2c
5742 SPIWrite 0328,9e
5743 SPIWrite 0329,db
5744 SPIWrite 032a,00
5745 SPIWrite 032b,9a
5746 SPIWrite 032c,08
5747 SPIWrite 032d,46
5748 SPIWrite 032e,11
5749 SPIWrite 032f,46
5750 SPIWrite 0330,e4
5751 SPIWrite 0331,f7
5752 SPIWrite 0332,48
5753 SPIWrite 0333,fa
5754 SPIWrite 0334,bd
5755 SPIWrite 0335,e8
5756 SPIWrite 0336,f8
5757 SPIWrite 0337,8f
5758 SPIWrite 0338,10
5759 SPIWrite 0339,b5
5760 SPIWrite 033a,30
5761 SPIWrite 033b,4a
5762 SPIWrite 033c,2e
5763 SPIWrite 033d,4c
5764 SPIWrite 033e,13
5765 SPIWrite 033f,78
5766 SPIWrite 0340,54
5767 SPIWrite 0341,f8
5768 SPIWrite 0342,20
5769 SPIWrite 0343,40
5770 SPIWrite 0344,84
5771 SPIWrite 0345,f8
5772 SPIWrite 0346,58
5773 SPIWrite 0347,3e
5774 SPIWrite 0348,06
5775 SPIWrite 0349,20
5776 SPIWrite 034a,c0
5777 SPIWrite 034b,f2
5778 SPIWrite 034c,00
5779 SPIWrite 034d,00
5780 SPIWrite 034e,03
5781 SPIWrite 034f,46

5782 SPIWrite 0350,5b
5783 SPIWrite 0351,1e
5784 SPIWrite 0352,fd
5785 SPIWrite 0353,d1
5786 SPIWrite 0354,53
5787 SPIWrite 0355,78
5788 SPIWrite 0356,04
5789 SPIWrite 0357,eb
5790 SPIWrite 0358,83
5791 SPIWrite 0359,03
5792 SPIWrite 035a,c3
5793 SPIWrite 035b,f8
5794 SPIWrite 035c,c0
5795 SPIWrite 035d,13
5796 SPIWrite 035e,40
5797 SPIWrite 035f,1e
5798 SPIWrite 0360,fd
5799 SPIWrite 0361,d1
5800 SPIWrite 0362,50
5801 SPIWrite 0363,78
5802 SPIWrite 0364,84
5803 SPIWrite 0365,f8
5804 SPIWrite 0366,58
5805 SPIWrite 0367,0e
5806 SPIWrite 0368,10
5807 SPIWrite 0369,bd
5808 SPIWrite 036a,f8
5809 SPIWrite 036b,b5
5810 SPIWrite 036c,dd
5811 SPIWrite 036d,f8
5812 SPIWrite 036e,18
5813 SPIWrite 036f,c0
5814 SPIWrite 0370,07
5815 SPIWrite 0371,46
5816 SPIWrite 0372,14
5817 SPIWrite 0373,46
5818 SPIWrite 0374,1d
5819 SPIWrite 0375,46
5820 SPIWrite 0376,0e
5821 SPIWrite 0377,46
5822 SPIWrite 0378,cd
5823 SPIWrite 0379,f8
5824 SPIWrite 037a,00
5825 SPIWrite 037b,c0
5826 SPIWrite 037c,eb
5827 SPIWrite 037d,f7
5828 SPIWrite 037e,28
5829 SPIWrite 037f,f8
5830 SPIWrite 0380,55
5831 SPIWrite 0381,ea
5832 SPIWrite 0382,04
5833 SPIWrite 0383,00
5834 SPIWrite 0384,37
5835 SPIWrite 0385,d1
5836 SPIWrite 0386,1e
5837 SPIWrite 0387,4b
5838 SPIWrite 0388,1e
5839 SPIWrite 0389,4a
5840 SPIWrite 038a,03
5841 SPIWrite 038b,eb
5842 SPIWrite 038c,67
5843 SPIWrite 038d,01
5844 SPIWrite 038e,73
5845 SPIWrite 038f,31
5846 SPIWrite 0390,08
5847 SPIWrite 0391,78
5848 SPIWrite 0392,b3
5849 SPIWrite 0393,f8
5850 SPIWrite 0394,9e

5851 SPIWrite 0395,41
5852 SPIWrite 0396,12
5853 SPIWrite 0397,5c
5854 SPIWrite 0398,38
5855 SPIWrite 0399,46
5856 SPIWrite 039a,54
5857 SPIWrite 039b,43
5858 SPIWrite 039c,47
5859 SPIWrite 039d,b1
5860 SPIWrite 039e,01
5861 SPIWrite 039f,2f
5862 SPIWrite 03a0,08
5863 SPIWrite 03a1,bf
5864 SPIWrite 03a2,00
5865 SPIWrite 03a3,25
5866 SPIWrite 03a4,05
5867 SPIWrite 03a5,d0
5868 SPIWrite 03a6,02
5869 SPIWrite 03a7,2f
5870 SPIWrite 03a8,0c
5871 SPIWrite 03a9,bf
5872 SPIWrite 03aa,03
5873 SPIWrite 03ab,25
5874 SPIWrite 03ac,02
5875 SPIWrite 03ad,25
5876 SPIWrite 03ae,00
5877 SPIWrite 03af,e0
5878 SPIWrite 03b0,01
5879 SPIWrite 03b1,25
5880 SPIWrite 03b2,15
5881 SPIWrite 03b3,4a
5882 SPIWrite 03b4,d2
5883 SPIWrite 03b5,5d
5884 SPIWrite 03b6,01
5885 SPIWrite 03b7,2a
5886 SPIWrite 03b8,02
5887 SPIWrite 03b9,d0
5888 SPIWrite 03ba,91
5889 SPIWrite 03bb,f8
5890 SPIWrite 03bc,7e
5891 SPIWrite 03bd,30
5892 SPIWrite 03be,23
5893 SPIWrite 03bf,b1
5894 SPIWrite 03c0,79
5895 SPIWrite 03c1,08
5896 SPIWrite 03c2,02
5897 SPIWrite 03c3,d3
5898 SPIWrite 03c4,28
5899 SPIWrite 03c5,46
5900 SPIWrite 03c6,41
5901 SPIWrite 03c7,1c
5902 SPIWrite 03c8,cd
5903 SPIWrite 03c9,b2
5904 SPIWrite 03ca,d6
5905 SPIWrite 03cb,f8
5906 SPIWrite 03cc,01
5907 SPIWrite 03cd,10
5908 SPIWrite 03ce,27
5909 SPIWrite 03cf,09
5910 SPIWrite 03d0,0a
5911 SPIWrite 03d1,01
5912 SPIWrite 03d2,b2
5913 SPIWrite 03d3,fb
5914 SPIWrite 03d4,f4
5915 SPIWrite 03d5,f2
5916 SPIWrite 03d6,07
5917 SPIWrite 03d7,fb
5918 SPIWrite 03d8,12
5919 SPIWrite 03d9,11

5920 SPIWrite 03da,ff
5921 SPIWrite 03db,f7
5922 SPIWrite 03dc,ad
5923 SPIWrite 03dd,ff
5924 SPIWrite 03de,30
5925 SPIWrite 03df,78
5926 SPIWrite 03e0,48
5927 SPIWrite 03e1,b1
5928 SPIWrite 03e2,d6
5929 SPIWrite 03e3,f8
5930 SPIWrite 03e4,06
5931 SPIWrite 03e5,00
5932 SPIWrite 03e6,01
5933 SPIWrite 03e7,01
5934 SPIWrite 03e8,b1
5935 SPIWrite 03e9,fb
5936 SPIWrite 03ea,f4
5937 SPIWrite 03eb,f1
5938 SPIWrite 03ec,07
5939 SPIWrite 03ed,fb
5940 SPIWrite 03ee,11
5941 SPIWrite 03ef,01
5942 SPIWrite 03f0,28
5943 SPIWrite 03f1,46
5944 SPIWrite 03f2,ff
5945 SPIWrite 03f3,f7
5946 SPIWrite 03f4,a1
5947 SPIWrite 03f5,ff
5948 SPIWrite 03f6,f8
5949 SPIWrite 03f7,bd
5950 SPIWrite 03f8,bc
5951 SPIWrite 03f9,77
5952 SPIWrite 03fa,02
5953 SPIWrite 03fb,00
5954 SPIWrite 03fc,96
5955 SPIWrite 03fd,19
5956 SPIWrite 03fe,01
5957 SPIWrite 03ff,20
5958 SPIWrite 0400,b4
5959 SPIWrite 0401,01
5960 SPIWrite 0402,01
5961 SPIWrite 0403,20
5962 SPIWrite 0404,3b
5963 SPIWrite 0405,78
5964 SPIWrite 0406,02
5965 SPIWrite 0407,00
5966 SPIWrite 0408,98
5967 SPIWrite 0409,fe
5968 SPIWrite 040a,00
5969 SPIWrite 040b,20
5970 SPIWrite 040c,1d
5971 SPIWrite 040d,48
5972 SPIWrite 040e,b0
5973 SPIWrite 040f,b5
5974 SPIWrite 0410,00
5975 SPIWrite 0411,78
5976 SPIWrite 0412,48
5977 SPIWrite 0413,bb
5978 SPIWrite 0414,1c
5979 SPIWrite 0415,48
5980 SPIWrite 0416,00
5981 SPIWrite 0417,78
5982 SPIWrite 0418,30
5983 SPIWrite 0419,bb
5984 SPIWrite 041a,1d
5985 SPIWrite 041b,48
5986 SPIWrite 041c,1b
5987 SPIWrite 041d,4a
5988 SPIWrite 041e,02

5989 SPIWrite 041f,21
5990 SPIWrite 0420,0c
5991 SPIWrite 0421,38
5992 SPIWrite 0422,50
5993 SPIWrite 0423,f8
5994 SPIWrite 0424,0c
5995 SPIWrite 0425,3f
5996 SPIWrite 0426,93
5997 SPIWrite 0427,f8
5998 SPIWrite 0428,40
5999 SPIWrite 0429,47
6000 SPIWrite 042a,93
6001 SPIWrite 042b,f8
6002 SPIWrite 042c,41
6003 SPIWrite 042d,77
6004 SPIWrite 042e,0f
6005 SPIWrite 042f,b9
6006 SPIWrite 0430,83
6007 SPIWrite 0431,f8
6008 SPIWrite 0432,70
6009 SPIWrite 0433,47
6010 SPIWrite 0434,52
6011 SPIWrite 0435,f8
6012 SPIWrite 0436,08
6013 SPIWrite 0437,4b
6014 SPIWrite 0438,94
6015 SPIWrite 0439,f8
6016 SPIWrite 043a,80
6017 SPIWrite 043b,5b
6018 SPIWrite 043c,d4
6019 SPIWrite 043d,f8
6020 SPIWrite 043e,80
6021 SPIWrite 043f,3b
6022 SPIWrite 0440,49
6023 SPIWrite 0441,1e
6024 SPIWrite 0442,65
6025 SPIWrite 0443,f3
6026 SPIWrite 0444,4d
6027 SPIWrite 0445,33
6028 SPIWrite 0446,c4
6029 SPIWrite 0447,f8
6030 SPIWrite 0448,80
6031 SPIWrite 0449,3b
6032 SPIWrite 044a,ea
6033 SPIWrite 044b,d1
6034 SPIWrite 044c,11
6035 SPIWrite 044d,4c
6036 SPIWrite 044e,04
6037 SPIWrite 044f,20
6038 SPIWrite 0450,54
6039 SPIWrite 0451,f8
6040 SPIWrite 0452,04
6041 SPIWrite 0453,3b
6042 SPIWrite 0454,93
6043 SPIWrite 0455,f8
6044 SPIWrite 0456,71
6045 SPIWrite 0457,27
6046 SPIWrite 0458,93
6047 SPIWrite 0459,f8
6048 SPIWrite 045a,72
6049 SPIWrite 045b,17
6050 SPIWrite 045c,40
6051 SPIWrite 045d,1e
6052 SPIWrite 045e,01
6053 SPIWrite 045f,ea
6054 SPIWrite 0460,02
6055 SPIWrite 0461,01
6056 SPIWrite 0462,83
6057 SPIWrite 0463,f8

6058 SPIWrite 0464,70
6059 SPIWrite 0465,17
6060 SPIWrite 0466,f3
6061 SPIWrite 0467,d1
6062 SPIWrite 0468,b0
6063 SPIWrite 0469,bd
6064 SPIWrite 046a,08
6065 SPIWrite 046b,b5
6066 SPIWrite 046c,d9
6067 SPIWrite 046d,f7
6068 SPIWrite 046e,f0
6069 SPIWrite 046f,fb
6070 SPIWrite 0470,ff
6071 SPIWrite 0471,f7
6072 SPIWrite 0472,cc
6073 SPIWrite 0473,ff
6074 SPIWrite 0474,08
6075 SPIWrite 0475,bd
6076 SPIWrite 0476,08
6077 SPIWrite 0477,b5
6078 SPIWrite 0478,d9
6079 SPIWrite 0479,f7
6080 SPIWrite 047a,9e
6081 SPIWrite 047b,fc
6082 SPIWrite 047c,ff
6083 SPIWrite 047d,f7
6084 SPIWrite 047e,c6
6085 SPIWrite 047f,ff
6086 SPIWrite 0480,08
6087 SPIWrite 0481,bd
6088 SPIWrite 0482,c0
6089 SPIWrite 0483,46
6090 SPIWrite 0484,c2
6091 SPIWrite 0485,19
6092 SPIWrite 0486,01
6093 SPIWrite 0487,20
6094 SPIWrite 0488,2b
6095 SPIWrite 0489,22
6096 SPIWrite 048a,01
6097 SPIWrite 048b,20
6098 SPIWrite 048c,bc
6099 SPIWrite 048d,77
6100 SPIWrite 048e,02
6101 SPIWrite 048f,00
6102 SPIWrite 0490,a8
6103 SPIWrite 0491,75
6104 SPIWrite 0492,02
6105 SPIWrite 0493,00
6106 SPIWrite 0494,9c
6107 SPIWrite 0495,77
6108 SPIWrite 0496,02
6109 SPIWrite 0497,00
6110 SPIWrite 0498,14
6111 SPIWrite 0499,49
6112 SPIWrite 049a,13
6113 SPIWrite 049b,48
6114 SPIWrite 049c,09
6115 SPIWrite 049d,68
6116 SPIWrite 049e,00
6117 SPIWrite 049f,88
6118 SPIWrite 04a0,00
6119 SPIWrite 04a1,22
6120 SPIWrite 04a2,48
6121 SPIWrite 04a3,43
6122 SPIWrite 04a4,c0
6123 SPIWrite 04a5,f3
6124 SPIWrite 04a6,40
6125 SPIWrite 04a7,11
6126 SPIWrite 04a8,01

6127 SPIWrite 04a9,eb
6128 SPIWrite 04aa,90
6129 SPIWrite 04ab,10
6130 SPIWrite 04ac,06
6131 SPIWrite 04ad,e0
6132 SPIWrite 04ae,13
6133 SPIWrite 04af,21
6134 SPIWrite 04b0,c0
6135 SPIWrite 04b1,f2
6136 SPIWrite 04b2,00
6137 SPIWrite 04b3,01
6138 SPIWrite 04b4,49
6139 SPIWrite 04b5,1e
6140 SPIWrite 04b6,fd
6141 SPIWrite 04b7,d1
6142 SPIWrite 04b8,00
6143 SPIWrite 04b9,bf
6144 SPIWrite 04ba,52
6145 SPIWrite 04bb,1c
6146 SPIWrite 04bc,90
6147 SPIWrite 04bd,42
6148 SPIWrite 04be,f6
6149 SPIWrite 04bf,d8
6150 SPIWrite 04c0,70
6151 SPIWrite 04c1,47
6152 SPIWrite 04c2,f8
6153 SPIWrite 04c3,b5
6154 SPIWrite 04c4,0a
6155 SPIWrite 04c5,4d
6156 SPIWrite 04c6,00
6157 SPIWrite 04c7,24
6158 SPIWrite 04c8,0e
6159 SPIWrite 04c9,46
6160 SPIWrite 04ca,07
6161 SPIWrite 04cb,46
6162 SPIWrite 04cc,07
6163 SPIWrite 04cd,e0
6164 SPIWrite 04ce,38
6165 SPIWrite 04cf,46
6166 SPIWrite 04d0,31
6167 SPIWrite 04d1,46
6168 SPIWrite 04d2,e6
6169 SPIWrite 04d3,f7
6170 SPIWrite 04d4,ad
6171 SPIWrite 04d5,fd
6172 SPIWrite 04d6,ff
6173 SPIWrite 04d7,f7
6174 SPIWrite 04d8,df
6175 SPIWrite 04d9,ff
6176 SPIWrite 04da,64
6177 SPIWrite 04db,1c
6178 SPIWrite 04dc,e4
6179 SPIWrite 04dd,b2
6180 SPIWrite 04de,28
6181 SPIWrite 04df,78
6182 SPIWrite 04e0,a0
6183 SPIWrite 04e1,42
6184 SPIWrite 04e2,f4
6185 SPIWrite 04e3,dc
6186 SPIWrite 04e4,f8
6187 SPIWrite 04e5,bd
6188 SPIWrite 04e6,c0
6189 SPIWrite 04e7,46
6190 SPIWrite 04e8,60
6191 SPIWrite 04e9,22
6192 SPIWrite 04ea,01
6193 SPIWrite 04eb,20
6194 SPIWrite 04ec,68
6195 SPIWrite 04ed,03

6196 SPIWrite 04ee,01
6197 SPIWrite 04ef,20
6198 SPIWrite 04f0,64
6199 SPIWrite 04f1,22
6200 SPIWrite 04f2,01
6201 SPIWrite 04f3,20
6202 SPIWrite 04f4,2d
6203 SPIWrite 04f5,e9
6204 SPIWrite 04f6,fe
6205 SPIWrite 04f7,4f
6206 SPIWrite 04f8,00
6207 SPIWrite 04f9,25
6208 SPIWrite 04fa,9b
6209 SPIWrite 04fb,46
6210 SPIWrite 04fc,91
6211 SPIWrite 04fd,46
6212 SPIWrite 04fe,80
6213 SPIWrite 04ff,46
6214 SPIWrite 0500,0c
6215 SPIWrite 0501,af
6216 SPIWrite 0502,01
6217 SPIWrite 0503,91
6218 SPIWrite 0504,97
6219 SPIWrite 0505,f8
6220 SPIWrite 0506,00
6221 SPIWrite 0507,a0
6222 SPIWrite 0508,01
6223 SPIWrite 0509,98
6224 SPIWrite 050a,08
6225 SPIWrite 050b,b9
6226 SPIWrite 050c,5d
6227 SPIWrite 050d,45
6228 SPIWrite 050e,19
6229 SPIWrite 050f,d1
6230 SPIWrite 0510,05
6231 SPIWrite 0511,eb
6232 SPIWrite 0512,49
6233 SPIWrite 0513,01
6234 SPIWrite 0514,08
6235 SPIWrite 0515,eb
6236 SPIWrite 0516,c5
6237 SPIWrite 0517,00
6238 SPIWrite 0518,08
6239 SPIWrite 0519,eb
6240 SPIWrite 051a,c1
6241 SPIWrite 051b,06
6242 SPIWrite 051c,b0
6243 SPIWrite 051d,f9
6244 SPIWrite 051e,a4
6245 SPIWrite 051f,7c
6246 SPIWrite 0520,b6
6247 SPIWrite 0521,f9
6248 SPIWrite 0522,24
6249 SPIWrite 0523,40
6250 SPIWrite 0524,4a
6251 SPIWrite 0525,46
6252 SPIWrite 0526,2b
6253 SPIWrite 0527,46
6254 SPIWrite 0528,40
6255 SPIWrite 0529,46
6256 SPIWrite 052a,00
6257 SPIWrite 052b,21
6258 SPIWrite 052c,cd
6259 SPIWrite 052d,f8
6260 SPIWrite 052e,00
6261 SPIWrite 052f,a0
6262 SPIWrite 0530,d4
6263 SPIWrite 0531,f7
6264 SPIWrite 0532,ff

6265 SPIWrite 0533,fe
6266 SPIWrite 0534,e4
6267 SPIWrite 0535,1b
6268 SPIWrite 0536,6f
6269 SPIWrite 0537,f3
6270 SPIWrite 0538,df
6271 SPIWrite 0539,34
6272 SPIWrite 053a,84
6273 SPIWrite 053b,f4
6274 SPIWrite 053c,80
6275 SPIWrite 053d,44
6276 SPIWrite 053e,a4
6277 SPIWrite 053f,f5
6278 SPIWrite 0540,80
6279 SPIWrite 0541,44
6280 SPIWrite 0542,b4
6281 SPIWrite 0543,84
6282 SPIWrite 0544,6d
6283 SPIWrite 0545,1c
6284 SPIWrite 0546,02
6285 SPIWrite 0547,2d
6286 SPIWrite 0548,de
6287 SPIWrite 0549,db
6288 SPIWrite 054a,bd
6289 SPIWrite 054b,e8
6290 SPIWrite 054c,fe
6291 SPIWrite 054d,8f
6292 SPIWrite 054e,00
6293 SPIWrite 054f,00
6294 SPIWrite 0550,98
6295 SPIWrite 0551,b5
6296 SPIWrite 0552,e7
6297 SPIWrite 0553,f7
6298 SPIWrite 0554,93
6299 SPIWrite 0555,f8
6300 SPIWrite 0556,0c
6301 SPIWrite 0557,48
6302 SPIWrite 0558,0c
6303 SPIWrite 0559,4a
6304 SPIWrite 055a,00
6305 SPIWrite 055b,27
6306 SPIWrite 055c,4f
6307 SPIWrite 055d,f6
6308 SPIWrite 055e,df
6309 SPIWrite 055f,73
6310 SPIWrite 0560,40
6311 SPIWrite 0561,1e
6312 SPIWrite 0562,10
6313 SPIWrite 0563,f8
6314 SPIWrite 0564,01
6315 SPIWrite 0565,1f
6316 SPIWrite 0566,01
6317 SPIWrite 0567,29
6318 SPIWrite 0568,09
6319 SPIWrite 0569,d1
6320 SPIWrite 056a,00
6321 SPIWrite 056b,2f
6322 SPIWrite 056c,14
6323 SPIWrite 056d,bf
6324 SPIWrite 056e,02
6325 SPIWrite 056f,f1
6326 SPIWrite 0570,b8
6327 SPIWrite 0571,04
6328 SPIWrite 0572,14
6329 SPIWrite 0573,1c
6330 SPIWrite 0574,21
6331 SPIWrite 0575,88
6332 SPIWrite 0576,19
6333 SPIWrite 0577,40

6334 SPIWrite 0578,41
6335 SPIWrite 0579,f4
6336 SPIWrite 057a,00
6337 SPIWrite 057b,51
6338 SPIWrite 057c,21
6339 SPIWrite 057d,80
6340 SPIWrite 057e,7f
6341 SPIWrite 057f,1c
6342 SPIWrite 0580,02
6343 SPIWrite 0581,2f
6344 SPIWrite 0582,ee
6345 SPIWrite 0583,db
6346 SPIWrite 0584,98
6347 SPIWrite 0585,bd
6348 SPIWrite 0586,c0
6349 SPIWrite 0587,46
6350 SPIWrite 0588,9e
6351 SPIWrite 0589,13
6352 SPIWrite 058a,01
6353 SPIWrite 058b,20
6354 SPIWrite 058c,06
6355 SPIWrite 058d,07
6356 SPIWrite 058e,06
6357 SPIWrite 058f,a8
6358 SPIWrite 0590,0b
6359 SPIWrite 0591,49
6360 SPIWrite 0592,0c
6361 SPIWrite 0593,4b
6362 SPIWrite 0594,0c
6363 SPIWrite 0595,22
6364 SPIWrite 0596,10
6365 SPIWrite 0597,b5
6366 SPIWrite 0598,09
6367 SPIWrite 0599,18
6368 SPIWrite 059a,10
6369 SPIWrite 059b,fb
6370 SPIWrite 059c,02
6371 SPIWrite 059d,33
6372 SPIWrite 059e,91
6373 SPIWrite 059f,f8
6374 SPIWrite 05a0,b8
6375 SPIWrite 05a1,21
6376 SPIWrite 05a2,5c
6377 SPIWrite 05a3,68
6378 SPIWrite 05a4,c2
6379 SPIWrite 05a5,f1
6380 SPIWrite 05a6,01
6381 SPIWrite 05a7,02
6382 SPIWrite 05a8,84
6383 SPIWrite 05a9,f8
6384 SPIWrite 05aa,70
6385 SPIWrite 05ab,27
6386 SPIWrite 05ac,9a
6387 SPIWrite 05ad,68
6388 SPIWrite 05ae,91
6389 SPIWrite 05af,f8
6390 SPIWrite 05b0,b8
6391 SPIWrite 05b1,11
6392 SPIWrite 05b2,c1
6393 SPIWrite 05b3,f1
6394 SPIWrite 05b4,01
6395 SPIWrite 05b5,01
6396 SPIWrite 05b6,82
6397 SPIWrite 05b7,f8
6398 SPIWrite 05b8,70
6399 SPIWrite 05b9,17
6400 SPIWrite 05ba,dd
6401 SPIWrite 05bb,f7
6402 SPIWrite 05bc,44

6403 SPIWrite 05bd,ff
6404 SPIWrite 05be,10
6405 SPIWrite 05bf,bd
6406 SPIWrite 05c0,b4
6407 SPIWrite 05c1,01
6408 SPIWrite 05c2,01
6409 SPIWrite 05c3,20
6410 SPIWrite 05c4,a8
6411 SPIWrite 05c5,75
6412 SPIWrite 05c6,02
6413 SPIWrite 05c7,00
6414 SPIWrite 05c8,08
6415 SPIWrite 05c9,b5
6416 SPIWrite 05ca,eb
6417 SPIWrite 05cb,f7
6418 SPIWrite 05cc,e1
6419 SPIWrite 05cd,ff
6420 SPIWrite 05ce,4f
6421 SPIWrite 05cf,f4
6422 SPIWrite 05d0,11
6423 SPIWrite 05d1,60
6424 SPIWrite 05d2,00
6425 SPIWrite 05d3,78
6426 SPIWrite 05d4,08
6427 SPIWrite 05d5,bd
6428 SPIWrite 05d6,38
6429 SPIWrite 05d7,b5
6430 SPIWrite 05d8,04
6431 SPIWrite 05d9,4d
6432 SPIWrite 05da,05
6433 SPIWrite 05db,4c
6434 SPIWrite 05dc,05
6435 SPIWrite 05dd,4b
6436 SPIWrite 05de,2d
6437 SPIWrite 05df,78
6438 SPIWrite 05e0,24
6439 SPIWrite 05e1,78
6440 SPIWrite 05e2,1b
6441 SPIWrite 05e3,78
6442 SPIWrite 05e4,ec
6443 SPIWrite 05e5,f7
6444 SPIWrite 05e6,1c
6445 SPIWrite 05e7,f8
6446 SPIWrite 05e8,38
6447 SPIWrite 05e9,bd
6448 SPIWrite 05ea,c0
6449 SPIWrite 05eb,46
6450 SPIWrite 05ec,20
6451 SPIWrite 05ed,00
6452 SPIWrite 05ee,00
6453 SPIWrite 05ef,64
6454 SPIWrite 05f0,20
6455 SPIWrite 05f1,00
6456 SPIWrite 05f2,00
6457 SPIWrite 05f3,54
6458 SPIWrite 05f4,20
6459 SPIWrite 05f5,00
6460 SPIWrite 05f6,00
6461 SPIWrite 05f7,74
6462 SPIWrite 05f8,38
6463 SPIWrite 05f9,b5
6464 SPIWrite 05fa,05
6465 SPIWrite 05fb,4d
6466 SPIWrite 05fc,00
6467 SPIWrite 05fd,24
6468 SPIWrite 05fe,28
6469 SPIWrite 05ff,68
6470 SPIWrite 0600,01
6471 SPIWrite 0601,46

6472 SPIWrite 0602,20
6473 SPIWrite 0603,46
6474 SPIWrite 0604,88
6475 SPIWrite 0605,47
6476 SPIWrite 0606,64
6477 SPIWrite 0607,1c
6478 SPIWrite 0608,04
6479 SPIWrite 0609,2c
6480 SPIWrite 060a,f8
6481 SPIWrite 060b,db
6482 SPIWrite 060c,38
6483 SPIWrite 060d,bd
6484 SPIWrite 060e,c0
6485 SPIWrite 060f,46
6486 SPIWrite 0610,ec
6487 SPIWrite 0611,de
6488 SPIWrite 0612,00
6489 SPIWrite 0613,20
6490 SPIWrite 0614,70
6491 SPIWrite 0615,47
6492 SPIWrite 0616,03
6493 SPIWrite 0617,48
6494 SPIWrite 0618,00
6495 SPIWrite 0619,78
6496 SPIWrite 061a,08
6497 SPIWrite 061b,b9
6498 SPIWrite 061c,ef
6499 SPIWrite 061d,f7
6500 SPIWrite 061e,e4
6501 SPIWrite 061f,bc
6502 SPIWrite 0620,70
6503 SPIWrite 0621,47
6504 SPIWrite 0622,c0
6505 SPIWrite 0623,46
6506 SPIWrite 0624,a1
6507 SPIWrite 0625,13
6508 SPIWrite 0626,01
6509 SPIWrite 0627,20
6510 SPIWrite 0628,03
6511 SPIWrite 0629,48
6512 SPIWrite 062a,08
6513 SPIWrite 062b,21
6514 SPIWrite 062c,41
6515 SPIWrite 062d,76
6516 SPIWrite 062e,09
6517 SPIWrite 062f,21
6518 SPIWrite 0630,c1
6519 SPIWrite 0631,76
6520 SPIWrite 0632,41
6521 SPIWrite 0633,77
6522 SPIWrite 0634,70
6523 SPIWrite 0635,47
6524 SPIWrite 0636,c0
6525 SPIWrite 0637,46
6526 SPIWrite 0638,88
6527 SPIWrite 0639,18
6528 SPIWrite 063a,01
6529 SPIWrite 063b,20
6530 SPIWrite 063c,00
6531 SPIWrite 063d,04
6532 SPIWrite 063e,07
6533 SPIWrite 063f,07
6534 SPIWrite 0640,00
6535 SPIWrite 0641,00
6536 SPIWrite 0642,03
6537 SPIWrite 0643,07
6538 SPIWrite 0644,00
6539 SPIWrite 0645,00
6540 SPIWrite 0646,00

6541 SPIWrite 0647,07
6542 SPIWrite 0648,00
6543 SPIWrite 0649,05
6544 SPIWrite 064a,05
6545 SPIWrite 064b,07
6546 SPIWrite 064c,07
6547 SPIWrite 064d,00
6548 SPIWrite 064e,0a
6549 SPIWrite 064f,0c
6550 SPIWrite 0650,0a
6551 SPIWrite 0651,16
6552 SPIWrite 0652,14
6553 SPIWrite 0653,16
6554 SPIWrite 0654,14
6555 SPIWrite 0655,00
6556 SPIWrite 0656,16
6557 SPIWrite 0657,00
6558 SPIWrite 0658,16
6559 SPIWrite 0659,16
6560 SPIWrite 065a,14
6561 SPIWrite 065b,16
6562 SPIWrite 065c,14
6563 SPIWrite 065d,00
6564 SPIWrite 065e,00
6565 SPIWrite 065f,00
6566 SPIWrite 0660,00
6567 SPIWrite 0661,16
6568 SPIWrite 0662,14
6569 SPIWrite 0663,16
6570 SPIWrite 0664,14
6571 SPIWrite 0665,00
6572 SPIWrite 0666,15
6573 SPIWrite 0667,00
6574 SPIWrite 0668,00
6575 SPIWrite 0669,00
6576 SPIWrite 066a,00
6577 SPIWrite 066b,00
6578 SPIWrite 066c,00
6579 SPIWrite 066d,01
6580 SPIWrite 066e,02
6581 SPIWrite 066f,01
6582 SPIWrite 0670,10
6583 SPIWrite 0671,0a
6584 SPIWrite 0672,10
6585 SPIWrite 0673,00
6586 SPIWrite 0674,00
6587 SPIWrite 0675,00
6588 SPIWrite 0676,00
6589 SPIWrite 0677,00
6590 SPIWrite 0678,00
6591 SPIWrite 0679,00
6592 SPIWrite 067a,00
6593 SPIWrite 067b,06
6594 SPIWrite 067c,02
6595 SPIWrite 067d,01
6596 SPIWrite 067e,10
6597 SPIWrite 067f,0a
6598 SPIWrite 0680,10
6599 SPIWrite 0681,00
6600 SPIWrite 0682,07
6601 SPIWrite 0683,00
6602 SPIWrite 0684,01
6603 SPIWrite 0685,00
6604 SPIWrite 0686,0a
6605 SPIWrite 0687,00
6606 SPIWrite 0688,00
6607 SPIWrite 0689,16
6608 SPIWrite 068a,00
6609 SPIWrite 068b,00

6610 SPIWrite 068c,00
6611 SPIWrite 068d,0a
6612 SPIWrite 068e,00
6613 SPIWrite 068f,00
6614 SPIWrite 0690,01
6615 SPIWrite 0691,10
6616 SPIWrite 0692,01
6617 SPIWrite 0693,10
6618 SPIWrite 0694,0a
6619 SPIWrite 0695,00
6620 SPIWrite 0696,00
6621 SPIWrite 0697,07
6622 SPIWrite 0698,10
6623 SPIWrite 0699,01
6624 SPIWrite 069a,0f
6625 SPIWrite 069b,0a
6626 SPIWrite 069c,00
6627 SPIWrite 069d,00
6628 SPIWrite 069e,00
6629 SPIWrite 069f,00
6630 SPIWrite 06a0,08
6631 SPIWrite 06a1,00
6632 SPIWrite 06a2,00
6633 SPIWrite 06a3,00
6634 SPIWrite 06a4,00
6635 SPIWrite 06a5,01
6636 SPIWrite 06a6,10
6637 SPIWrite 06a7,0a
6638 SPIWrite 06a8,00
6639 SPIWrite 06a9,00
6640 SPIWrite 06aa,00
6641 SPIWrite 06ab,00
6642 SPIWrite 06ac,00
6643 SPIWrite 06ad,02
6644 SPIWrite 06ae,00
6645 SPIWrite 06af,00
6646 SPIWrite 06b0,00
6647 SPIWrite 06b1,00
6648 SPIWrite 06b2,00
6649 SPIWrite 06b3,00
6650 SPIWrite 06b4,00
6651 SPIWrite 06b5,00
6652 SPIWrite 06b6,00
6653 SPIWrite 06b7,00
6654 SPIWrite 06b8,00
6655 SPIWrite 06b9,00
6656 SPIWrite 06ba,00
6657 SPIWrite 06bb,00
6658 SPIWrite 06bc,00
6659 SPIWrite 06bd,00
6660 SPIWrite 06be,00
6661 SPIWrite 06bf,00
6662 SPIWrite 06c0,00
6663 SPIWrite 06c1,00
6664 SPIWrite 06c2,11
6665 SPIWrite 06c3,00
6666 SPIWrite 06c4,00
6667 SPIWrite 06c5,00
6668 SPIWrite 06c6,00
6669 SPIWrite 06c7,00
6670 SPIWrite 06c8,01
6671 SPIWrite 06c9,16
6672 SPIWrite 06ca,01
6673 SPIWrite 06cb,10
6674 SPIWrite 06cc,0a
6675 SPIWrite 06cd,10
6676 SPIWrite 06ce,00
6677 SPIWrite 06cf,01
6678 SPIWrite 06d0,03

6679 SPIWrite 06d1,01
6680 SPIWrite 06d2,10
6681 SPIWrite 06d3,0a
6682 SPIWrite 06d4,10
6683 SPIWrite 06d5,00
6684 SPIWrite 06d6,00
6685 SPIWrite 06d7,12
6686 SPIWrite 06d8,01
6687 SPIWrite 06d9,10
6688 SPIWrite 06da,0a
6689 SPIWrite 06db,00
6690 SPIWrite 06dc,00
6691 SPIWrite 06dd,00
6692 SPIWrite 06de,11
6693 SPIWrite 06df,01
6694 SPIWrite 06e0,10
6695 SPIWrite 06e1,0a
6696 SPIWrite 06e2,00
6697 SPIWrite 06e3,00
6698 SPIWrite 06e4,01
6699 SPIWrite 06e5,10
6700 SPIWrite 06e6,01
6701 SPIWrite 06e7,0e
6702 SPIWrite 06e8,0a
6703 SPIWrite 06e9,00
6704 SPIWrite 06ea,00
6705 SPIWrite 06eb,01
6706 SPIWrite 06ec,0f
6707 SPIWrite 06ed,0a
6708 SPIWrite 06ee,00
6709 SPIWrite 06ef,00
6710 SPIWrite 06f0,00
6711 SPIWrite 06f1,00
6712 SPIWrite 06f2,00
6713 SPIWrite 06f3,00
6714 SPIWrite 06f4,00
6715 SPIWrite 06f5,00
6716 SPIWrite 06f6,00
6717 SPIWrite 06f7,00
6718 SPIWrite 06f8,00
6719 SPIWrite 06f9,00
6720 SPIWrite 06fa,00
6721 SPIWrite 06fb,00
6722 SPIWrite 06fc,00
6723 SPIWrite 06fd,00
6724 SPIWrite 06fe,00
6725 SPIWrite 06ff,00
6726 SPIWrite 0700,00
6727 SPIWrite 0701,00
6728 SPIWrite 0702,00
6729 SPIWrite 0703,00
6730 SPIWrite 0704,00
6731 SPIWrite 0705,00
6732 SPIWrite 0706,00
6733 SPIWrite 0707,00
6734 SPIWrite 0708,03
6735 SPIWrite 0709,00
6736 SPIWrite 070a,00
6737 SPIWrite 070b,00
6738 SPIWrite 070c,00
6739 SPIWrite 070d,00
6740 SPIWrite 070e,00
6741 SPIWrite 070f,00
6742 SPIWrite 0710,00
6743 SPIWrite 0711,00
6744 SPIWrite 0712,00
6745 SPIWrite 0713,00
6746 SPIWrite 0714,00
6747 SPIWrite 0715,07

6748	SPIWrite	0716,00
6749	SPIWrite	0717,00
6750	SPIWrite	0718,00
6751	SPIWrite	0719,00
6752	SPIWrite	071a,00
6753	SPIWrite	071b,00
6754	SPIWrite	071c,01
6755	SPIWrite	071d,03
6756	SPIWrite	071e,01
6757	SPIWrite	071f,10
6758	SPIWrite	0720,0a
6759	SPIWrite	0721,10
6760	SPIWrite	0722,00
6761	SPIWrite	0723,09
6762	SPIWrite	0724,02
6763	SPIWrite	0725,01
6764	SPIWrite	0726,10
6765	SPIWrite	0727,0a
6766	SPIWrite	0728,10
6767	SPIWrite	0729,00
6768	SPIWrite	072a,07
6769	SPIWrite	072b,00
6770	SPIWrite	072c,01
6771	SPIWrite	072d,00
6772	SPIWrite	072e,0a
6773	SPIWrite	072f,00
6774	SPIWrite	0730,00
6775	SPIWrite	0731,01
6776	SPIWrite	0732,10
6777	SPIWrite	0733,0a
6778	SPIWrite	0734,10
6779	SPIWrite	0735,0a
6780	SPIWrite	0736,00
6781	SPIWrite	0737,00
6782	SPIWrite	0738,00
6783	SPIWrite	0739,00
6784	SPIWrite	073a,00
6785	SPIWrite	073b,00
6786	SPIWrite	073c,00
6787	SPIWrite	073d,02
6788	SPIWrite	073e,00
6789	SPIWrite	073f,02
6790	SPIWrite	0740,06
6791	SPIWrite	0741,00
6792	SPIWrite	0742,00
6793	SPIWrite	0743,00
6794	SPIWrite	0744,00
6795	SPIWrite	0745,00
6796	SPIWrite	0746,00
6797	SPIWrite	0747,00
6798	SPIWrite	0748,00
6799	SPIWrite	0749,02
6800	SPIWrite	074a,06
6801	SPIWrite	074b,00
6802	SPIWrite	074c,00
6803	SPIWrite	074d,00
6804	SPIWrite	074e,00
6805	SPIWrite	074f,00
6806	SPIWrite	0750,00
6807	SPIWrite	0751,00
6808	SPIWrite	0752,00
6809	SPIWrite	0753,00
6810	SPIWrite	0754,06
6811	SPIWrite	0755,00
6812	SPIWrite	0756,00
6813	SPIWrite	0757,00
6814	SPIWrite	0758,7c
6815	SPIWrite	0759,1c
6816	SPIWrite	075a,01

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6817     SPIWrite 075b,20
6818     SPIWrite 075c,d1
6819     SPIWrite 075d,1e
6820     SPIWrite 075e,01
6821     SPIWrite 075f,20
6822     SPIWrite 0760,84
6823     SPIWrite 0761,1a
6824     SPIWrite 0762,01
6825     SPIWrite 0763,20
6826     SPIWrite 0764,26
6827     SPIWrite 0765,07
6828     SPIWrite 0766,01
6829     SPIWrite 0767,20
6830     SPIWrite 0768,4a
6831     SPIWrite 0769,0c
6832     SPIWrite 076a,01
6833     SPIWrite 076b,20
6834     SPIWrite 076c,1c
6835     SPIWrite 076d,16
6836     SPIWrite 076e,03
6837     SPIWrite 076f,00
6838     SPIWrite 0770,28
6839     SPIWrite 0771,16
6840     SPIWrite 0772,03
6841     SPIWrite 0773,00
6842     SPIWrite 0774,2d
6843     SPIWrite 0775,16
6844     SPIWrite 0776,03
6845     SPIWrite 0777,00
6846     SPIWrite 0778,45
6847     SPIWrite 0779,16
6848     SPIWrite 077a,03
6849     SPIWrite 077b,00
6850     SPIWrite 077c,fb
6851     SPIWrite 077d,20
6852     SPIWrite 077e,01
6853     SPIWrite 077f,20
6854     SPIWrite 0780,00
6855     SPIWrite 0781,20
6856     SPIWrite 0782,01
6857     SPIWrite 0783,20
6858     SPIWrite 0784,0c
6859     SPIWrite 0785,20
6860     SPIWrite 0786,01
6861     SPIWrite 0787,20
6862     SPIWrite 0788,11
6863     SPIWrite 0789,20
6864     SPIWrite 078a,01
6865     SPIWrite 078b,20
6866     SPIWrite 078c,29
6867     SPIWrite 078d,20
6868     SPIWrite 078e,01
6869     SPIWrite 078f,20
6870     SPIWrite 0790,93
6871     SPIWrite 0791,21
6872     SPIWrite 0792,01
6873     SPIWrite 0793,20
6874     SPIWrite 0794,00
6875     SPIWrite 0018,00     //sys_calib_macro_memory=0x0;   Address(0x18[7:0])
6876     SPIWrite 0018,20     //macro=0x1;       Address(0x18[7:5])
6877     SPIRead 00f0
6878
6879     //Read  MACRO_READY=0x1;   Address(0xf0[7:0])
6880
6881
6882     SPIPoll 00f0,0,0,1
6883
6884     SPIWrite 00a3,07     //MACRO_OPERAND_REG0=0x7750000;
        Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])

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6885 SPIWrite 00a2,75
6886 SPIWrite 00a1,00
6887 SPIWrite 00a0,00
6888 SPIWrite 00a7,00 //MACRO_OPERAND_REG1=0x1000;
Address(0xa4[7:0],0xa5[7:0],0xa6[7:0],0xa7[7:0],0xa8[7:0])
6889 SPIWrite 00a6,00
6890 SPIWrite 00a5,10
6891 SPIWrite 00a4,00
6892 SPIWrite 0193,78 //MACRO_OPCODE=0x78; Address(0x193[7:0],0x194[7:0])
6893
6894 WAIT 0.001
6895 SPIRead 00f0
6896
6897 //Read MACRO_DONE=0x1; Address(0xf0[7:2])
6898
6899
6900 SPIPoll 00f0,2,2,4
6901
6902 SPIRead 00f0
6903
6904 //Read MACRO_ERROR=0x0; Address(0xf0[7:3])
6905
6906 SPIRead 00f1
6907
6908 //Read MACRO_ERROR_OPCODE=0x0; Address(0xf1[7:0],0xf2[7:0])
6909
6910 SPIRead 00f0
6911
6912 //Read MACRO_ERROR_IN_OPCODE=0x0; Address(0xf0[7:4])
6913
6914 SPIRead 00f0
6915
6916 //Read MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0; Address(0xf0[7:5])
6917
6918 SPIRead 00f0
6919
6920 //Read MACRO_ERROR_IN_OPERAND=0x0; Address(0xf0[7:6])
6921
6922 SPIRead 00f0
6923
6924 //Read MACRO_ERROR_IN_EXECUTION=0x0; Address(0xf0[7:7])
6925
6926 SPIRead 00f3
6927 SPIRead 00f2
6928
6929 //Read MACRO_ERROR_EXTENDED_CODE=0x0; Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
6930
6931 SPIRead 00f7
6932 SPIRead 00f6
6933 SPIRead 00f5
6934 SPIRead 00f4
6935
6936 //Read MACRO_ERROR_EXTENDED_CODE_2=0x0;
Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
6937
6938 SPIRead 00f0
6939
6940 //Read MACRO_READY=0x1; Address(0xf0[7:0])
6941
6942
6943 SPIPoll 00f0,0,0,1
6944
6945 SPIWrite 00a3,00 //MACRO_OPERAND_REG0=0x1;
Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
6946 SPIWrite 00a2,00
6947 SPIWrite 00a1,00
6948 SPIWrite 00a0,01
6949 SPIWrite 0193,78 //MACRO_OPCODE=0x78; Address(0x193[7:0],0x194[7:0])
6950

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```
6951 WAIT 0.001
6952 SPIRead 00f0
6953
6954 //Read MACRO_DONE=0x1;      Address(0xf0[7:2])
6955
6956
6957 SPIPoll 00f0,2,2,4
6958
6959 SPIRead 00f0
6960
6961 //Read MACRO_ERROR=0x0;      Address(0xf0[7:3])
6962
6963 SPIRead 00f1
6964
6965 //Read MACRO_ERROR_OPCODE=0x0;      Address(0xf1[7:0],0xf2[7:0])
6966
6967 SPIRead 00f0
6968
6969 //Read MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])
6970
6971 SPIRead 00f0
6972
6973 //Read MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;      Address(0xf0[7:5])
6974
6975 SPIRead 00f0
6976
6977 //Read MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])
6978
6979 SPIRead 00f0
6980
6981 //Read MACRO_ERROR_IN_EXECUTION=0x0;  Address(0xf0[7:7])
6982
6983 SPIRead 00f3
6984 SPIRead 00f2
6985
6986 //Read MACRO_ERROR_EXTENDED_CODE=0x0;  Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
6987
6988 SPIRead 00f7
6989 SPIRead 00f6
6990 SPIRead 00f5
6991 SPIRead 00f4
6992
6993 //Read MACRO_ERROR_EXTENDED_CODE_2=0x0;
Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
6994
6995 SPIRead 00f0
6996
6997 //Read MACRO_READY=0x1;      Address(0xf0[7:0])
6998
6999
7000 SPIPoll 00f0,0,0,1
7001
7002 SPIWrite 00a3,00      //MACRO_OPERAND_REG0=0x3;
Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
7003 SPIWrite 00a2,00
7004 SPIWrite 00a1,00
7005 SPIWrite 00a0,03
7006 SPIWrite 0193,01      //MACRO_OPCODE=0x1;      Address(0x193[7:0],0x194[7:0])
7007
7008 WAIT 0.001
7009 SPIRead 00f0
7010
7011 //Read MACRO_DONE=0x1;      Address(0xf0[7:2])
7012
7013
7014 SPIPoll 00f0,2,2,4
7015
7016 SPIRead 00f0
7017
```

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7018 //Read  MACRO_ERROR=0x0;      Address(0xf0[7:3])
7019
7020 SPIRead 00f1
7021
7022 //Read  MACRO_ERROR_OPCODE=0x0;      Address(0xf1[7:0],0xf2[7:0])
7023
7024 SPIRead 00f0
7025
7026 //Read  MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])
7027
7028 SPIRead 00f0
7029
7030 //Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;      Address(0xf0[7:5])
7031
7032 SPIRead 00f0
7033
7034 //Read  MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])
7035
7036 SPIRead 00f0
7037
7038 //Read  MACRO_ERROR_IN_EXECUTION=0x0;  Address(0xf0[7:7])
7039
7040 SPIRead 00f3
7041 SPIRead 00f2
7042
7043 //Read  MACRO_ERROR_EXTENDED_CODE=0x0;  Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
7044
7045 SPIRead 00f7
7046 SPIRead 00f6
7047 SPIRead 00f5
7048 SPIRead 00f4
7049
7050 //Read  MACRO_ERROR_EXTENDED_CODE_2=0x0;
Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
7051
7052 SPIRead 00fb
7053 SPIRead 00fa
7054 SPIRead 00f9
7055 SPIRead 00f8
7056
7057 //Read  MACRO_RESULT_REG0=0x14010200;
Address(0xf8[7:0],0xf9[7:0],0xfa[7:0],0xfb[7:0],0xfc[7:0])
7058
7059 SPIRead 00ff
7060 SPIRead 00fe
7061 SPIRead 00fd
7062 SPIRead 00fc
7063
7064 //Read  MACRO_RESULT_REG1=0x8e;
Address(0xfc[7:0],0xfd[7:0],0xfe[7:0],0xff[7:0],0x100[7:0])
7065
7066 SPIWrite 0018,00 //macro=0x0;      Address(0x18[7:5])
7067
7068 //STEP: pllEfuse/step0
7069
7070 //START: Enabling Temp Sense
7071
7072 SPIWrite 0015,02 //ana_4t4r=0x1;      Address(0x15[7:1])
7073 SPIWrite 00c0,80 //EN_CLK_TEMP_SENSE=0x1;      Address(0xc0[7:7])
7074 SPIWrite 0015,00 //ana_4t4r=0x0;      Address(0x15[7:1])
7075 SPIWrite 0015,40 //digtop=0x1;      Address(0x15[7:6])
7076 SPIWrite 02a3,00 //temp_sensel_cfg0=0x7e;
Address(0x2a0[7:0],0x2a1[7:0],0x2a2[7:0],0x2a3[7:0],0x2a4[7:0])
7077 SPIWrite 02a2,00
7078 SPIWrite 02a1,00
7079 SPIWrite 02a0,7e
7080 SPIWrite 02a7,01 //temp_sensel_cfg1=0x1000000;
Address(0x2a4[7:0],0x2a5[7:0],0x2a6[7:0],0x2a7[7:0],0x2a8[7:0])
7081 SPIWrite 02a6,00

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```
7082 SPIWrite 02a5,00
7083 SPIWrite 02a4,00
7084
7085 //END: Enabling Temp Sense
7086
7087
7088 //START: Loading PLL EFuse trims
7089
7090 SPIWrite 0015,00 //digtop=0x0; Address(0x15[7:6])
7091 SPIWrite 0018,20 //macro=0x1; Address(0x18[7:5])
7092 SPIRead 00f0
7093
7094 //Read MACRO_READY=0x1; Address(0xf0[7:0])
7095
7096
7097 SPIPoll 00f0,0,0,1
7098
7099 SPIWrite 00a3,00 //MACRO_OPERAND_REG0=0x21f;
Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
7100 SPIWrite 00a2,00
7101 SPIWrite 00a1,02
7102 SPIWrite 00a0,1f
7103 SPIWrite 0193,33 //MACRO_OPCODE=0x33; Address(0x193[7:0],0x194[7:0])
7104
7105 WAIT 0.001
7106 SPIRead 00f0
7107
7108 //Read MACRO_DONE=0x1; Address(0xf0[7:2])
7109
7110
7111 SPIPoll 00f0,2,2,4
7112
7113 SPIRead 00f0
7114
7115 //Read MACRO_ERROR=0x0; Address(0xf0[7:3])
7116
7117 SPIRead 00f1
7118
7119 //Read MACRO_ERROR_OPCODE=0x0; Address(0xf1[7:0],0xf2[7:0])
7120
7121 SPIRead 00f0
7122
7123 //Read MACRO_ERROR_IN_OPCODE=0x0; Address(0xf0[7:4])
7124
7125 SPIRead 00f0
7126
7127 //Read MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0; Address(0xf0[7:5])
7128
7129 SPIRead 00f0
7130
7131 //Read MACRO_ERROR_IN_OPERAND=0x0; Address(0xf0[7:6])
7132
7133 SPIRead 00f0
7134
7135 //Read MACRO_ERROR_IN_EXECUTION=0x0; Address(0xf0[7:7])
7136
7137 SPIRead 00f3
7138 SPIRead 00f2
7139
7140 //Read MACRO_ERROR_EXTENDED_CODE=0x0; Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
7141
7142 SPIRead 00f7
7143 SPIRead 00f6
7144 SPIRead 00f5
7145 SPIRead 00f4
7146
7147 //Read MACRO_ERROR_EXTENDED_CODE_2=0x0;
Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
7148
```



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7149 SPIRead 00f0
7150
7151 //Read  MACRO_READY=0x1;      Address(0xf0[7:0])
7152
7153
7154 SPIPoll 00f0,0,0,1
7155
7156 SPIWrite 00a3,00      //MACRO_OPERAND_REG0=0x10f;
Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
7157 SPIWrite 00a2,00
7158 SPIWrite 00a1,01
7159 SPIWrite 00a0,0f
7160 SPIWrite 0193,34      //MACRO_OPCODE=0x34;      Address(0x193[7:0],0x194[7:0])
7161
7162 WAIT 0.001
7163 SPIRead 00f0
7164
7165 //Read  MACRO_DONE=0x1;      Address(0xf0[7:2])
7166
7167
7168 SPIPoll 00f0,2,2,4
7169
7170 SPIRead 00f0
7171
7172 //Read  MACRO_ERROR=0x0;      Address(0xf0[7:3])
7173
7174 SPIRead 00f1
7175
7176 //Read  MACRO_ERROR_OPCODE=0x0;      Address(0xf1[7:0],0xf2[7:0])
7177
7178 SPIRead 00f0
7179
7180 //Read  MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])
7181
7182 SPIRead 00f0
7183
7184 //Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;      Address(0xf0[7:5])
7185
7186 SPIRead 00f0
7187
7188 //Read  MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])
7189
7190 SPIRead 00f0
7191
7192 //Read  MACRO_ERROR_IN_EXECUTION=0x0;  Address(0xf0[7:7])
7193
7194 SPIRead 00f3
7195 SPIRead 00f2
7196
7197 //Read  MACRO_ERROR_EXTENDED_CODE=0x0;  Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
7198
7199 SPIRead 00f7
7200 SPIRead 00f6
7201 SPIRead 00f5
7202 SPIRead 00f4
7203
7204 //Read  MACRO_ERROR_EXTENDED_CODE_2=0x0;
Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
7205
7206 SPIRead 00f0
7207
7208 //Read  MACRO_READY=0x1;      Address(0xf0[7:0])
7209
7210
7211 SPIPoll 00f0,0,0,1
7212
7213 SPIWrite 00a3,00      //MACRO_OPERAND_REG0=0x1;
Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
7214 SPIWrite 00a2,00

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```

7215     SPIWrite 00a1,00
7216     SPIWrite 00a0,01
7217     SPIWrite 0193,72      //MACRO_OPCODE=0x72;      Address(0x193[7:0],0x194[7:0])
7218
7219     WAIT 0.001
7220     SPIRead 00f0
7221
7222     //Read  MACRO_DONE=0x1;      Address(0xf0[7:2])
7223
7224
7225     SPIPoll 00f0,2,2,4
7226
7227     SPIRead 00f0
7228
7229     //Read  MACRO_ERROR=0x0;      Address(0xf0[7:3])
7230
7231     SPIRead 00f1
7232
7233     //Read  MACRO_ERROR_OPCODE=0x0;      Address(0xf1[7:0],0xf2[7:0])
7234
7235     SPIRead 00f0
7236
7237     //Read  MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])
7238
7239     SPIRead 00f0
7240
7241     //Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;      Address(0xf0[7:5])
7242
7243     SPIRead 00f0
7244
7245     //Read  MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])
7246
7247     SPIRead 00f0
7248
7249     //Read  MACRO_ERROR_IN_EXECUTION=0x0;  Address(0xf0[7:7])
7250
7251     SPIRead 00f3
7252     SPIRead 00f2
7253
7254     //Read  MACRO_ERROR_EXTENDED_CODE=0x0;  Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
7255
7256     SPIRead 00f7
7257     SPIRead 00f6
7258     SPIRead 00f5
7259     SPIRead 00f4
7260
7261     //Read  MACRO_ERROR_EXTENDED_CODE_2=0x0;
Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
7262
7263     SPIRead 00f0
7264
7265     //Read  MACRO_READY=0x1;      Address(0xf0[7:0])
7266
7267
7268     SPIPoll 00f0,0,0,1
7269
7270     SPIWrite 00a3,00      //MACRO_OPERAND_REG0=0xe0100;
Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
7271     SPIWrite 00a2,0e
7272     SPIWrite 00a1,01
7273     SPIWrite 00a0,00
7274     SPIWrite 0193,71      //MACRO_OPCODE=0x71;      Address(0x193[7:0],0x194[7:0])
7275
7276     WAIT 0.001
7277     SPIRead 00f0
7278
7279     //Read  MACRO_DONE=0x1;      Address(0xf0[7:2])
7280
7281

```

```
7282 SPIPoll 00f0,2,2,4
7283
7284 SPIRead 00f0
7285
7286 //Read MACRO_ERROR=0x0; Address(0xf0[7:3])
7287
7288 SPIRead 00f1
7289
7290 //Read MACRO_ERROR_OPCODE=0x0; Address(0xf1[7:0],0xf2[7:0])
7291
7292 SPIRead 00f0
7293
7294 //Read MACRO_ERROR_IN_OPCODE=0x0; Address(0xf0[7:4])
7295
7296 SPIRead 00f0
7297
7298 //Read MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0; Address(0xf0[7:5])
7299
7300 SPIRead 00f0
7301
7302 //Read MACRO_ERROR_IN_OPERAND=0x0; Address(0xf0[7:6])
7303
7304 SPIRead 00f0
7305
7306 //Read MACRO_ERROR_IN_EXECUTION=0x0; Address(0xf0[7:7])
7307
7308 SPIRead 00f3
7309 SPIRead 00f2
7310
7311 //Read MACRO_ERROR_EXTENDED_CODE=0x0; Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
7312
7313 SPIRead 00f7
7314 SPIRead 00f6
7315 SPIRead 00f5
7316 SPIRead 00f4
7317
7318 //Read MACRO_ERROR_EXTENDED_CODE_2=0x0;
Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
7319
7320
7321 //END: Done Loading PLL EFuse trims
7322
7323 SPIRead 00f0
7324
7325 //Read MACRO_READY=0x1; Address(0xf0[7:0])
7326
7327
7328 SPIPoll 00f0,0,0,1
7329
7330 SPIWrite 00a3,00 //MACRO_OPERAND_REG0=0x10101;
Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
7331 SPIWrite 00a2,01
7332 SPIWrite 00a1,01
7333 SPIWrite 00a0,01
7334 SPIWrite 0193,73 //MACRO_OPCODE=0x73; Address(0x193[7:0],0x194[7:0])
7335
7336 WAIT 0.001
7337 SPIRead 00f0
7338
7339 //Read MACRO_DONE=0x1; Address(0xf0[7:2])
7340
7341
7342 SPIPoll 00f0,2,2,4
7343
7344 SPIRead 00f0
7345
7346 //Read MACRO_ERROR=0x0; Address(0xf0[7:3])
7347
7348 SPIRead 00f1
```

```

7349
7350 //Read  MACRO_ERROR_OPCODE=0x0;      Address(0xf1[7:0],0xf2[7:0])
7351
7352 SPIRead 00f0
7353
7354 //Read  MACRO_ERROR_IN_OPCODE=0x0;   Address(0xf0[7:4])
7355
7356 SPIRead 00f0
7357
7358 //Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;      Address(0xf0[7:5])
7359
7360 SPIRead 00f0
7361
7362 //Read  MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])
7363
7364 SPIRead 00f0
7365
7366 //Read  MACRO_ERROR_IN_EXECUTION=0x0;   Address(0xf0[7:7])
7367
7368 SPIRead 00f3
7369 SPIRead 00f2
7370
7371 //Read  MACRO_ERROR_EXTENDED_CODE=0x0;   Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
7372
7373 SPIRead 00f7
7374 SPIRead 00f6
7375 SPIRead 00f5
7376 SPIRead 00f4
7377
7378 //Read  MACRO_ERROR_EXTENDED_CODE_2=0x0;
Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
7379
7380 SPIWrite 0018,00 //macro=0x0;      Address(0x18[7:5])
7381 SPIWrite 0012,01 //rxdig=0x1;      Address(0x12[7:0])
7382 SPIWrite 0761,0a //cfg_fmixon_hbw_pmode=0x0;   Address(0x761[7:4])
7383 SPIWrite 0012,02 //rxdig=0x2;      Address(0x12[7:0])
7384 SPIWrite 0761,0a //cfg_fmixon_hbw_pmode=0x0;   Address(0x761[7:4])
7385 SPIWrite 0012,04 //rxdig=0x4;      Address(0x12[7:0])
7386 SPIWrite 0761,0a //cfg_fmixon_hbw_pmode=0x0;   Address(0x761[7:4])
7387 SPIWrite 0012,08 //rxdig=0x8;      Address(0x12[7:0])
7388 SPIWrite 0761,0a //cfg_fmixon_hbw_pmode=0x0;   Address(0x761[7:4])
7389 SPIWrite 0012,00 //rxdig=0x0;      Address(0x12[7:0])
7390
7391 //STEP: pllConfig/step0
7392
7393 //START: Configuring PLL
7394
7395 SPIWrite 0015,08 //rx=0x2;      Address(0x15[7:2])
7396 SPIWrite 0043,00 //po_to_rx_2r_rxab_config_6=0x0;
Address(0x40[7:0],0x41[7:0],0x42[7:0],0x43[7:0],0x44[7:0])
7397 SPIWrite 0042,00
7398 SPIWrite 0041,00
7399 SPIWrite 0040,00
7400 SPIWrite 0015,00 //rx=0x0;      Address(0x15[7:2])
7401 SPIWrite 0015,02 //ana_4t4r=0x1;      Address(0x15[7:1])
7402 SPIWrite 00c1,60 //DIS_DIGCLK=0x3;   Address(0xc1[7:5])
7403
7404 //START: Requesting/releasing SPI Access to PLL Pages
7405
7406 SPIWrite 0015,00 //ana_4t4r=0x0;      Address(0x15[7:1])
7407 SPIWrite 0015,40 //digtop=0x1;   Address(0x15[7:6])
7408 SPIWrite 0170,01 //pll_reg_spi_req_a=0x1;   Address(0x170[7:0])
7409 SPIWrite 0540,00 //pll_reg_spi_req_b1=0x0;   Address(0x540[7:0])
7410
7411 SPIPoll 0171,0,0,01
7412 SPIRead 0171
7413
7414 //Read  pll_reg_spi_a_ack=0x1(Meaning: );;   Address(0x171[7:0])
7415

```

```
7416
7417 //END: Requesting/releasing SPI Access to PLL Pages
7418
7419 SPIWrite 0015,00 //digtop=0x0; Address(0x15[7:6])
7420 SPIWrite 0015,01 //pll=0x1; Address(0x15[7:0])
7421 SPIWrite 003f,08 //EN_CP=0x1; Address(0x3f[7:3])
7422 SPIWrite 0028,01 //EN_BIAS=0x1; Address(0x28[7:0])
7423 SPIWrite 0035,10 //EN_LDO_ANA=0x1; Address(0x35[7:4])
7424 SPIWrite 0036,40 //EN_LDO_RF=0x1; Address(0x36[7:6])
7425 SPIWrite 0038,08 //EN_LDO_TXFB=0x1; Address(0x38[7:3])
7426 SPIWrite 0039,20 //EN_LDO_RX=0x1; Address(0x39[7:5])
7427 SPIWrite 003b,08 //EN_LDO_REFD2S=0x1; Address(0x3b[7:3])
7428 SPIWrite 0046,60 //EN_VCO=0x1; Address(0x46[7:5])
7429 SPIWrite 0046,60 //EN_VCO_PKDET=0x1; Address(0x46[7:6])
7430 SPIWrite 0043,18 //EN_VCTRL_ADC=0x1; Address(0x43[7:4])
7431 SPIWrite 0043,18 //EN_VREF_CAL=0x1; Address(0x43[7:3])
7432 SPIWrite 004c,00 //CTL_VCO_BUF_ATT=0x0; Address(0x4c[7:0])
7433 SPIWrite 003c,e0 //EN_REFDIV_DIV=0x1; Address(0x3c[7:5])
7434 SPIWrite 0015,00 //pll=0x0; Address(0x15[7:0])
7435 SPIWrite 0015,02 //ana_4t4r=0x1; Address(0x15[7:1])
7436 SPIWrite 010c,00 //EN_REFDIV_DMP=0x0; Address(0x10c[7:0])
7437 SPIWrite 0015,00 //ana_4t4r=0x0; Address(0x15[7:1])
7438 SPIWrite 0015,01 //pll=0x1; Address(0x15[7:0])
7439 SPIWrite 003c,60 //EN_REFDIV_DMP=0x0; Address(0x3c[7:7])
7440 SPIWrite 003c,20 //EN_REFDIV_SYNC=0x0; Address(0x3c[7:6])
7441 SPIWrite 003d,00 //CTL_REFDIV_EDGE_SEL=0x0; Address(0x3d[7:0])
7442 SPIWrite 0015,00 //pll=0x0; Address(0x15[7:0])
7443 SPIWrite 0015,02 //ana_4t4r=0x1; Address(0x15[7:1])
7444 SPIWrite 010d,01 //CTL_REFDIV_DIV=0x1; Address(0x10d[7:0])
7445 SPIWrite 0015,00 //ana_4t4r=0x0; Address(0x15[7:1])
7446 SPIWrite 0015,01 //pll=0x1; Address(0x15[7:0])
7447 SPIWrite 0056,43 //CTL_SYNC_SYSREF_CLK_MUX=0x1; Address(0x56[7:6])
7448 SPIWrite 0056,c3 //CTL_SYNC_SYSREF_MUX=0x1; Address(0x56[7:7])
7449 SPIWrite 0056,c3 //CTL_SYNC_LCM_MUX=0x0; Address(0x56[7:3])
7450 SPIWrite 0056,f3 //CTL_SYNC_LCMDIV=0x3; Address(0x56[7:4])
7451 SPIWrite 0057,02 //CTL_SYNC_SYSREF_OUT_MUX=0x1; Address(0x57[7:1])
7452 SPIWrite 0015,00 //pll=0x0; Address(0x15[7:0])
7453 SPIWrite 0015,80 //timing_controller=0x1; Address(0x15[7:7])
7454 SPIWrite 07f5,01 //count_len_sysref=0x17f; Address(0x7f4[7:0],0x7f5[7:0],0x7f6[7:0])
7455 SPIWrite 07f4,7f
7456 SPIWrite 0015,00 //timing_controller=0x0; Address(0x15[7:7])
7457 SPIWrite 0015,01 //pll=0x1; Address(0x15[7:0])
7458 SPIWrite 006d,01 //LCMGEN_DIV=0x17f; Address(0x6c[7:0],0x6d[7:0],0x6e[7:0])
7459 SPIWrite 006c,7f
7460 SPIWrite 0062,00 //NO_OF_SYSREFS_REFDIV=0x0; Address(0x62[7:4])
7461 SPIWrite 0015,00 //pll=0x0; Address(0x15[7:0])
7462 SPIWrite 0015,02 //ana_4t4r=0x1; Address(0x15[7:1])
7463 SPIWrite 010f,18 //CTL_FBDIV_DIV=0x18; Address(0x10f[7:0])
7464 SPIWrite 010e,00 //CTL_FBDIV_DIVBY2=0x0; Address(0x10e[7:0])
7465 SPIWrite 0015,00 //ana_4t4r=0x0; Address(0x15[7:1])
7466 SPIWrite 0015,01 //pll=0x1; Address(0x15[7:0])
7467 SPIWrite 0050,fe //EN_OUTDIV_MUX_TX=0x3; Address(0x50[7:1])
7468 SPIWrite 0050,fe //EN_OUTDIV_MUX_RX=0x3; Address(0x50[7:3])
7469 SPIWrite 0050,fe //EN_OUTDIV_MUX_FB=0x3; Address(0x50[7:5])
7470 SPIWrite 0015,00 //pll=0x0; Address(0x15[7:0])
7471 SPIWrite 0015,02 //ana_4t4r=0x1; Address(0x15[7:1])
7472 SPIWrite 0110,01 //CTL_OUTDIV_MUX_TX=0x1; Address(0x110[7:0])
7473 SPIWrite 0015,00 //ana_4t4r=0x0; Address(0x15[7:1])
7474 SPIWrite 0015,01 //pll=0x1; Address(0x15[7:0])
7475 SPIWrite 0051,3f //EN_OUTDIV_DIV_TX=0x1; Address(0x51[7:1])
7476 SPIWrite 0015,00 //pll=0x0; Address(0x15[7:0])
7477 SPIWrite 0015,02 //ana_4t4r=0x1; Address(0x15[7:1])
7478 SPIWrite 0111,01 //CTL_OUTDIV_DIV_TX=0x1; Address(0x111[7:0])
7479 SPIWrite 0015,00 //ana_4t4r=0x0; Address(0x15[7:1])
7480 SPIWrite 0015,01 //pll=0x1; Address(0x15[7:0])
7481 SPIWrite 007f,00 //MASK_EN_OUTDIV_MAIN_CLK_TX=0x0; Address(0x7f[7:6])
7482 SPIWrite 0015,00 //pll=0x0; Address(0x15[7:0])
7483 SPIWrite 0015,02 //ana_4t4r=0x1; Address(0x15[7:1])
7484 SPIWrite 0112,01 //CTL_OUTDIV_MUX_RX=0x1; Address(0x112[7:0])
```

```

7485 SPIWrite 0015,00 //ana_4t4r=0x0; Address(0x15[7:1])
7486 SPIWrite 0015,01 //pll=0x1; Address(0x15[7:0])
7487 SPIWrite 0051,3f //EN_OUTDIV_DIV_RX=0x1; Address(0x51[7:2])
7488 SPIWrite 0015,00 //pll=0x0; Address(0x15[7:0])
7489 SPIWrite 0015,02 //ana_4t4r=0x1; Address(0x15[7:1])
7490 SPIWrite 0113,03 //CTL_OUTDIV_DIV_RX=0x3; Address(0x113[7:0])
7491 SPIWrite 0015,00 //ana_4t4r=0x0; Address(0x15[7:1])
7492 SPIWrite 0015,01 //pll=0x1; Address(0x15[7:0])
7493 SPIWrite 007f,00 //MASK_EN_OUTDIV_MAIN_CLK_RX=0x0; Address(0x7f[7:7])
7494 SPIWrite 0015,00 //pll=0x0; Address(0x15[7:0])
7495 SPIWrite 0015,02 //ana_4t4r=0x1; Address(0x15[7:1])
7496 SPIWrite 0114,01 //CTL_OUTDIV_MUX_FB=0x1; Address(0x114[7:0])
7497 SPIWrite 0015,00 //ana_4t4r=0x0; Address(0x15[7:1])
7498 SPIWrite 0015,01 //pll=0x1; Address(0x15[7:0])
7499 SPIWrite 0051,3f //EN_OUTDIV_DIV_FB=0x1; Address(0x51[7:3])
7500 SPIWrite 0015,00 //pll=0x0; Address(0x15[7:0])
7501 SPIWrite 0015,02 //ana_4t4r=0x1; Address(0x15[7:1])
7502 SPIWrite 0115,01 //CTL_OUTDIV_DIV_FB=0x1; Address(0x115[7:0])
7503 SPIWrite 0015,00 //ana_4t4r=0x0; Address(0x15[7:1])
7504 SPIWrite 0015,01 //pll=0x1; Address(0x15[7:0])
7505 SPIWrite 0051,2f //EN_OUTDIV_MUX3_TX_JESD=0x0; Address(0x51[7:4])
7506 SPIWrite 0063,01 //NO_OF_SYSREFS_OUTDIV=0x1; Address(0x63[7:0])
7507 SPIWrite 0072,02 //SYSREF_PULSE_CNT_DIG=0x2; Address(0x72[7:0],0x73[7:0])
7508 SPIWrite 006f,05 //SYSREF_PULSE_CNT_TX=0x5; Address(0x6f[7:0],0x70[7:0])
7509 SPIWrite 0070,02 //SYSREF_PULSE_CNT_RX=0x2; Address(0x70[7:0],0x71[7:0])
7510 SPIWrite 0071,02 //SYSREF_PULSE_CNT_FB=0x2; Address(0x71[7:0],0x72[7:0])
7511 SPIWrite 006d,01 //LCMGEN_DIV=0x17f; Address(0x6c[7:0],0x6d[7:0],0x6e[7:0])
7512 SPIWrite 006c,7f
7513 SPIWrite 007c,04 //SYSREF_WIDTH=0x4; Address(0x7c[7:0])
7514 SPIWrite 0055,ff //EN_SYNC_LCM_MUX=0x1; Address(0x55[7:0])
7515 SPIWrite 0055,ff //EN_SYNC_SYSREF_CLK_MUX=0x1; Address(0x55[7:7])
7516 SPIWrite 0055,ff //EN_SYNC_LCMDIV_CLKBUFF=0x1; Address(0x55[7:1])
7517 SPIWrite 0055,ff //EN_SYNC_LCMDIV_STG=0xf; Address(0x55[7:2])
7518 SPIWrite 0055,ff //EN_SYNC_LCMDIV_MUX=0x1; Address(0x55[7:6])
7519 SPIWrite 0059,01 //EN_SYNC_SYSREF_TO_OUTDIV_HANDOFF_CLK_MUX=0x1;
Address(0x59[7:0])
7520 SPIWrite 0058,00 //CTL_SYNC_SYSREF_TO_OUTDIV_HANDOFF_CLK_MUX=0x0;
Address(0x58[7:7])
7521 SPIWrite 0059,01 //EN_SYNC_SYSREF_MODE3=0x0; Address(0x59[7:2])
7522 SPIWrite 0059,01 //DIS_SYNC_SYSREF_MODE12=0x0; Address(0x59[7:3])
7523 SPIWrite 005c,00 //EN_DIV_STG_SERDES=0x0; Address(0x5c[7:3])
7524 SPIWrite 005d,04 //SEL_CLK_SERDES=0x2; Address(0x5d[7:1])
7525 SPIWrite 005d,0c //SEL_REF_CLK_SERDES=0x1; Address(0x5d[7:3])
7526 SPIWrite 003d,01 //CTL_REFDIV_EDGE_SEL=0x1; Address(0x3d[7:0])
7527 SPIWrite 0053,03 //ESR_1P2_TXFB_CLKTOP=0x3; Address(0x53[7:0])
7528 SPIWrite 003e,0c //ESR_1P8_CP=0x3; Address(0x3e[7:2])
7529 SPIWrite 0065,6a //ESR_1P8_ANA_PLLTOP_LSB=0x1; Address(0x65[7:6])
7530 SPIWrite 004e,01 //ESR_1P8_ANA_PLLTOP_MSB=0x1; Address(0x4e[7:0])
7531 SPIWrite 0052,00 //ESR_1P2_RX_CLKTOP=0x0; Address(0x52[7:5])
7532 SPIWrite 0065,62 //ESR_1P2_RX_PLLTOP=0x0; Address(0x65[7:2])
7533 SPIWrite 0052,00 //ESR_1P2_TXFB_CML_MSB=0x0; Address(0x52[7:0])
7534 SPIWrite 0052,00 //ESR_1P2_TXFB_CML_LSB=0x0; Address(0x52[7:4])
7535 SPIWrite 0053,03 //ESR_1P8_BIAS_CLKTOP=0x0; Address(0x53[7:2])
7536 SPIWrite 005e,00 //ESR_1P8_BIAS_CLKTOP2=0x0; Address(0x5e[7:1])
7537 SPIWrite 0052,00 //ESR_1P2_VCO_CLKTOP_MSB=0x0; Address(0x52[7:3])
7538 SPIWrite 0052,00 //ESR_1P2_VCO_CLKTOP_LSB=0x0; Address(0x52[7:7])
7539 SPIWrite 003e,0c //ESR_1P2_TXFB_PLLTOP=0x0; Address(0x3e[7:4],0x3f[7:1])
7540 SPIWrite 003f,08
7541 SPIWrite 0065,60 //ESR_1P2_VCO_PLLTOP=0x0; Address(0x65[7:0])
7542 SPIWrite 0087,00 //ESR_1P2_VCOTOP=0x0; Address(0x87[7:5])
7543 SPIWrite 005e,00 //ESR_1P8_VCO_CLKTOP=0x0; Address(0x5e[7:3])
7544 SPIWrite 0087,00 //ESR_1P8_VCOTOP=0x0; Address(0x87[7:1])
7545 SPIWrite 0087,00 //ESR_PLL_LDOOUT=0x0; Address(0x87[7:3])
7546 SPIWrite 003e,0c //ESR_1P2_CP=0x0; Address(0x3e[7:0])
7547 SPIWrite 0051,2f //ESR_1P2_DIG_MISCTOP=0x0; Address(0x51[7:6])
7548 SPIWrite 0052,00 //ESR_1P2_REF_MISCTOP=0x0; Address(0x52[7:1])
7549 SPIWrite 0065,40 //ESR_1P2_ANA_PLLTOP=0x0; Address(0x65[7:4])
7550 SPIWrite 0084,10 //CTL_LDOVCO_VREF=0x1; Address(0x84[7:4])
7551 SPIWrite 0084,90 //CTL_LDOVCO_FBRES=0x2; Address(0x84[7:6])

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7552 SPIWrite 0069,47 //LOCK_DETECT_DELTA2_PROG=0x47; Address(0x69[7:0],0x6a[7:0])
7553 SPIWrite 0045,20 //CTL_VREF_CAL_EXT2INT=0x1; Address(0x45[7:5])
7554 SPIWrite 0032,00 //CTL_VCO_300U=0x0; Address(0x32[7:2])
7555 SPIWrite 0049,38 //CTL_VCO_IB_VAR_SLOPE=0x7; Address(0x49[7:3])
7556 SPIWrite 0049,3d //CTL_VCO_IB_VAR=0x5; Address(0x49[7:0])
7557 SPIWrite 004a,00 //CTL_VCO_IB_GM_SLOPE=0x0; Address(0x4a[7:3])
7558 SPIWrite 004b,00 //CTL_VCO_IB_TAIL_SLOPE=0x0; Address(0x4b[7:4])
7559 SPIWrite 004d,c0 //CTL_VCO_VAR_BIAS=0x0; Address(0x4d[7:0])
7560 SPIWrite 004a,04 //CTL_VCO_IB_GM=0x4; Address(0x4a[7:0])
7561 SPIWrite 004b,0f //CTL_VCO_IB_TAIL=0xf; Address(0x4b[7:0])
7562 SPIWrite 004b,3f //CTL_VCO_IB_TAIL_SLOPE=0x3; Address(0x4b[7:4])
7563 SPIWrite 0051,2f //CTL_VCO_IB_TAIL_SLOPE_SIGN=0x1; Address(0x51[7:0])
7564 SPIWrite 0040,40 //CTL_CP_CURR=0x2; Address(0x40[7:5])
7565 SPIWrite 0041,00 //CTL_CP_BIAS=0x0; Address(0x41[7:1])
7566 SPIWrite 0043,f8 //CTL_LPF_R=0x7; Address(0x43[7:5])
7567 SPIWrite 0075,08 //CAL_BYPASS=0x1; Address(0x75[7:3])
7568 SPIWrite 0075,0e //VCO_SEL_IN=0x6; Address(0x75[7:0])
7569 SPIWrite 0045,24 //CTL_VREF_CAL_SLOPE=0x4; Address(0x45[7:0])
7570 SPIWrite 0031,40 //CTL_LPF_50U_0=0x1; Address(0x31[7:6])
7571 SPIWrite 0046,63 //CTL_VCTRL_ADC_VL_LVL=0x3; Address(0x46[7:0])
7572 SPIWrite 0045,24 //CTL_VCTRL_ADC_VH_LVL=0x0; Address(0x45[7:6])
7573 SPIWrite 0064,07 //M_IN_PROG=0x7; Address(0x64[7:0])
7574 SPIWrite 0073,20 //EN_SYNC_SYSREF_BUFF=0x1; Address(0x73[7:5])
7575 SPIWrite 0056,f1 //EN_SYNC_SYSREF_OUT_MUX=0x0; Address(0x56[7:1])
7576 SPIWrite 0058,00 //CTL_SYNC_LCMDIV_SYSREF_PULSE=0x0; Address(0x58[7:2])
7577 SPIWrite 0062,00 //NO_OF_SYSREFS_REFDIV=0x0; Address(0x62[7:4])
7578 SPIWrite 0066,00 //EN_CAL=0x0; Address(0x66[7:0])
7579 SPIWrite 0066,01 //EN_CAL=0x1; Address(0x66[7:0])
7580
7581 WAIT 0.005
7582 SPIWrite 0066,03 //EN_LOCK_DETECT=0x1; Address(0x66[7:1])
7583
7584 WAIT 0.005
7585 SPIWrite 0063,41 //CLR_FLAG_LOCK_LOST=0x1; Address(0x63[7:6])
7586 SPIWrite 0063,01 //CLR_FLAG_LOCK_LOST=0x0; Address(0x63[7:6])
7587
7588 WAIT 0.005
7589 SPIRead 0066
7590
7591 //Read LOCK_OUT_STICKY=0x1; Address(0x66[7:5])
7592
7593 SPIRead 0066
7594
7595 //Read LOCK_LOST_STICKY=0x0; Address(0x66[7:6])
7596
7597 SPIRead 0066
7598
7599 //Read LOCK=0x1; Address(0x66[7:4])
7600
7601 SPIRead 0066
7602
7603 //Read LOCK_LOST_STICKY=0x0; Address(0x66[7:6])
7604
7605 SPIWrite 0066,31 //EN_LOCK_DETECT=0x0; Address(0x66[7:1])
7606 SPIWrite 0063,81 //CLR_FLAG_LOCK_OUT=0x1; Address(0x63[7:7])
7607 SPIWrite 0063,c1 //CLR_FLAG_LOCK_LOST=0x1; Address(0x63[7:6])
7608 SPIWrite 0063,c2 //NO_OF_SYSREFS_OUTDIV=0x2; Address(0x63[7:0])
7609
7610 //START: Sending Sysref to device
7611
7612 SPIWrite 0015,00 //pll=0x0; Address(0x15[7:0])
7613 SPIWrite 0015,80 //timing_controller=0x1; Address(0x15[7:7])
7614 SPIWrite 085b,00 //spare_reg_port=0x0;
Address(0x858[7:0],0x859[7:0],0x85a[7:0],0x85b[7:0],0x85c[7:0])
7615 SPIWrite 085a,00
7616 SPIWrite 0859,00
7617 SPIWrite 0858,00
7618 SPIWrite 085b,00 //spare_reg_port=0x101;
Address(0x858[7:0],0x859[7:0],0x85a[7:0],0x85b[7:0],0x85c[7:0])

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7619 SPIWrite 085a,00
7620 SPIWrite 0859,01
7621 SPIWrite 0858,01
7622 SPIWrite 085b,00 //spare_reg_port=0x0;
Address(0x858[7:0],0x859[7:0],0x85a[7:0],0x85b[7:0],0x85c[7:0])
7623 SPIWrite 085a,00
7624 SPIWrite 0859,00
7625 SPIWrite 0858,00
7626 SPIWrite 0015,00 //timing_controller=0x0; Address(0x15[7:7])
7627 SPIWrite 0015,01 //pll=0x1; Address(0x15[7:0])
7628 SPIWrite 006a,00 //LCMGEN_SYNC_ENA=0x0; Address(0x6a[7:1])
7629 SPIWrite 006e,00 //LCMGEN_USE_SPI_SYSREF=0x0; Address(0x6e[7:0])
7630 SPIWrite 006a,00 //LCMGEN_SYNC_ENA=0x0; Address(0x6a[7:1])
7631 SPIWrite 006a,02 //LCMGEN_SYNC_ENA=0x1; Address(0x6a[7:1])
7632 SPIWrite 0015,00 //pll=0x0; Address(0x15[7:0])
7633
7634 //STEP: pllConfig/step1
7635
7636 //External-Action: Give Sysref Here.
7637
7638
7639 WAIT 0.001
7640
7641 //END: Sending Sysref to device
7642
7643 SPIWrite 0015,01 //pll=0x1; Address(0x15[7:0])
7644 SPIWrite 0063,c0 //NO_OF_SYSREFS_OUTDIV=0x0; Address(0x63[7:0])
7645 SPIWrite 0015,00 //pll=0x0; Address(0x15[7:0])
7646 SPIWrite 0015,02 //ana_4t4r=0x1; Address(0x15[7:1])
7647 SPIWrite 00c1,00 //DIS_DIGCLK=0x0; Address(0xc1[7:5])
7648 SPIWrite 0015,00 //ana_4t4r=0x0; Address(0x15[7:1])
7649 SPIWrite 0015,01 //pll=0x1; Address(0x15[7:0])
7650 SPIWrite 0063,40 //CLR_FLAG_LOCK_OUT=0x0; Address(0x63[7:7])
7651 SPIWrite 0063,00 //CLR_FLAG_LOCK_LOST=0x0; Address(0x63[7:6])
7652 SPIWrite 0066,33 //EN_LOCK_DETECT=0x1; Address(0x66[7:1])
7653
7654 //START: Requesting/releasing SPI Access to PLL Pages
7655
7656 SPIWrite 0015,00 //pll=0x0; Address(0x15[7:0])
7657 SPIWrite 0015,40 //digtop=0x1; Address(0x15[7:6])
7658 SPIWrite 0170,00 //pll_reg_spi_req_a=0x0; Address(0x170[7:0])
7659 SPIWrite 0540,00 //pll_reg_spi_req_b1=0x0; Address(0x540[7:0])
7660
7661 WAIT 0.2
7662
7663 //END: Requesting/releasing SPI Access to PLL Pages
7664
7665 SPIWrite 0015,00 //digtop=0x0; Address(0x15[7:6])
7666 SPIWrite 0015,80 //timing_controller=0x1; Address(0x15[7:7])
7667 SPIWrite 010d,03 //config_rise_xx_A_4=0x31f;
Address(0x10c[7:0],0x10d[7:0],0x10e[7:0])
7668 SPIWrite 010c,1f
7669 SPIWrite 01ad,03 //config_rise_xx_A_4=0x31f;
Address(0x1ac[7:0],0x1ad[7:0],0x1ae[7:0])
7670 SPIWrite 01ac,1f
7671 SPIWrite 024d,03 //config_rise_xx_A_4=0x31f;
Address(0x24c[7:0],0x24d[7:0],0x24e[7:0])
7672 SPIWrite 024c,1f
7673 SPIWrite 02ed,03 //config_rise_xx_A_4=0x31f;
Address(0x2ec[7:0],0x2ed[7:0],0x2ee[7:0])
7674 SPIWrite 02ec,1f
7675 SPIWrite 0421,01 //config_rise_xx_A_41=0x190;
Address(0x420[7:0],0x421[7:0],0x422[7:0])
7676 SPIWrite 0420,90
7677 SPIWrite 04d9,01 //config_rise_xx_A_41=0x190;
Address(0x4d8[7:0],0x4d9[7:0],0x4da[7:0])
7678 SPIWrite 04d8,90
7679 SPIWrite 0591,01 //config_rise_xx_A_41=0x190;
Address(0x590[7:0],0x591[7:0],0x592[7:0])

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7680 SPIWrite 0590,90
7681 SPIWrite 0649,01 //config_rise_xx_A_41=0x190;
Address(0x648[7:0],0x649[7:0],0x64a[7:0])
7682 SPIWrite 0648,90
7683 SPIWrite 0701,01 //config_rise_xx_A_41=0x190;
Address(0x700[7:0],0x701[7:0],0x702[7:0])
7684 SPIWrite 0700,90
7685 SPIWrite 07b9,01 //config_rise_xx_A_41=0x190;
Address(0x7b8[7:0],0x7b9[7:0],0x7ba[7:0])
7686 SPIWrite 07b8,90
7687
7688 //END: Configuring PLL
7689
7690 SPIWrite 0015,00 //timing_controller=0x0; Address(0x15[7:7])
7691
7692 //STEP: pllConfig/step2
7693 SPIWrite 0018,40 //cm4_internal=0x1; Address(0x18[7:6])
7694 SPIWrite 0086,01 //cfg_dithered_mode_en=0x1; Address(0x86[7:0])
7695 SPIWrite 0082,10 //cfg_divide_factor=0x10; Address(0x82[7:0])
7696 SPIWrite 0083,01 //cfg_divide_factor_odd=0x1; Address(0x83[7:0])
7697 SPIWrite 0084,00 //cfg_divide_factor_load_enable=0x0; Address(0x84[7:0])
7698 SPIWrite 0084,01 //cfg_divide_factor_load_enable=0x1; Address(0x84[7:0])
7699 SPIWrite 0084,00 //cfg_divide_factor_load_enable=0x0; Address(0x84[7:0])
7700 SPIWrite 0018,00 //cm4_internal=0x0; Address(0x18[7:6])
7701 SPIWrite 0018,20 //macro=0x1; Address(0x18[7:5])
7702 SPIRead 00f0
7703
7704 //Read MACRO_READY=0x1; Address(0xf0[7:0])
7705
7706
7707 SPIPoll 00f0,0,0,1
7708
7709 SPIWrite 0193,12 //MACRO_OPCODE=0x12; Address(0x193[7:0],0x194[7:0])
7710
7711 WAIT 0.001
7712 SPIRead 00f0
7713
7714 //Read MACRO_DONE=0x1; Address(0xf0[7:2])
7715
7716
7717 SPIPoll 00f0,2,2,4
7718
7719 SPIRead 00f0
7720
7721 //Read MACRO_ERROR=0x0; Address(0xf0[7:3])
7722
7723 SPIRead 00f1
7724
7725 //Read MACRO_ERROR_OPCODE=0x0; Address(0xf1[7:0],0xf2[7:0])
7726
7727 SPIRead 00f0
7728
7729 //Read MACRO_ERROR_IN_OPCODE=0x0; Address(0xf0[7:4])
7730
7731 SPIRead 00f0
7732
7733 //Read MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0; Address(0xf0[7:5])
7734
7735 SPIRead 00f0
7736
7737 //Read MACRO_ERROR_IN_OPERAND=0x0; Address(0xf0[7:6])
7738
7739 SPIRead 00f0
7740
7741 //Read MACRO_ERROR_IN_EXECUTION=0x0; Address(0xf0[7:7])
7742
7743 SPIRead 00f3
7744 SPIRead 00f2
7745

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7746 //Read  MACRO_ERROR_EXTENDED_CODE=0x0;  Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
7747
7748 SPIRead 00f7
7749 SPIRead 00f6
7750 SPIRead 00f5
7751 SPIRead 00f4
7752
7753 //Read  MACRO_ERROR_EXTENDED_CODE_2=0x0;
Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
7754
7755 SPIWrite 0018,00 //macro=0x0;  Address(0x18[7:5])
7756
7757 //STEP: serdesConfig/step0
7758
7759 //START: Enabling access to SERDES
7760
7761 SPIWrite 0016,10 //jesd_subchip=0x1;  Address(0x16[7:4])
7762 SPIWrite 00c0,02 //apb_clk_disable=0x0;  Address(0xc0[7:0])
7763 SPIWrite 00c0,00 //apb_clk_dithered_mode_en=0x0;  Address(0xc0[7:1])
7764 SPIWrite 00c4,01 //apb_clk_from_cm4_clk_en=0x1;  Address(0xc4[7:0])
7765 SPIWrite 0020,12 //serdesab_apb_page_addr_index=0x2;  Address(0x20[7:0])
7766 SPIWrite 0021,12 //serdescd_apb_page_addr_index=0x2;  Address(0x21[7:0])
7767 SPIWrite 0020,12 //serdesab_apb_mode_16b=0x1;  Address(0x20[7:4])
7768 SPIWrite 0021,12 //serdescd_apb_mode_16b=0x1;  Address(0x21[7:4])
7769 SPIWrite 0020,12 //serdesab_apb_pin_intf_en=0x0;  Address(0x20[7:2])
7770 SPIWrite 0021,12 //serdescd_apb_pin_intf_en=0x0;  Address(0x21[7:2])
7771 SPIWrite 00c0,40 //apb_clk_sysref_sel=0x1;  Address(0xc0[7:6])
7772 SPIWrite 00c0,40 //apb_clk_sysref_val=0x0;  Address(0xc0[7:7])
7773 SPIWrite 00c0,c0 //apb_clk_sysref_val=0x1;  Address(0xc0[7:7])
7774 SPIWrite 00c0,40 //apb_clk_sysref_val=0x0;  Address(0xc0[7:7])
7775 SPIWrite 0016,00 //jesd_subchip=0x0;  Address(0x16[7:4])
7776 SPIWrite 0016,20 //serdes_jesd=0x1;  Address(0x16[7:5])
7777 SPIWrite 7007,00 //BUS_WIDTH_LANE3=0x0;  Address(0x9803[7:3])
7778 SPIWrite 7006,00
7779 SPIWrite 7007,00 //BUS_WIDTH_LANE2=0x0;  Address(0x9803[7:2])
7780 SPIWrite 7006,00
7781 SPIWrite 7007,00 //BUS_WIDTH_LANE1=0x0;  Address(0x9803[7:1])
7782 SPIWrite 7006,00
7783 SPIWrite 7007,00 //BUS_WIDTH_LANE0=0x0;  Address(0x9803[7:0])
7784 SPIWrite 7006,00
7785 SPIWrite 0016,40 //serdes_jesd=0x2;  Address(0x16[7:5])
7786 SPIWrite 7007,00 //BUS_WIDTH_LANE3=0x0;  Address(0x9803[7:3])
7787 SPIWrite 7006,00
7788 SPIWrite 7007,00 //BUS_WIDTH_LANE2=0x0;  Address(0x9803[7:2])
7789 SPIWrite 7006,00
7790 SPIWrite 7007,00 //BUS_WIDTH_LANE1=0x0;  Address(0x9803[7:1])
7791 SPIWrite 7006,00
7792 SPIWrite 7007,00 //BUS_WIDTH_LANE0=0x0;  Address(0x9803[7:0])
7793 SPIWrite 7006,00
7794
7795 //END: Done enabling access to SERDES
7796
7797
7798 //START: Setting Serdes Reference Clock Divs
7799
7800 SPIWrite 0016,00 //serdes_jesd=0x0;  Address(0x16[7:5])
7801 SPIWrite 0015,02 //ana_4t4r=0x1;  Address(0x15[7:1])
7802 SPIWrite 0107,00 //po_common_digtop_spare_0=0x801;
Address(0x104[7:0],0x105[7:0],0x106[7:0],0x107[7:0],0x108[7:0])
7803 SPIWrite 0106,00
7804 SPIWrite 0105,08
7805 SPIWrite 0104,01
7806
7807 //END: Setting Serdes Reference Clock Divs
7808
7809 SPIWrite 0015,00 //ana_4t4r=0x0;  Address(0x15[7:1])
7810
7811 //STEP: serdesConfig/step1
7812

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7813 //START: Resetting Serdes
7814
7815 SPIWrite 0016,20 //serdes_jesd=0x1; Address(0x16[7:5])
7816 SPIWrite 701b,08 //DOMAIN_RESET=0x888; Address(0x980d[3:0],0x980e[7:0])
7817 SPIWrite 701a,88
7818 SPIWrite 701b,00 //DOMAIN_RESET=0x0; Address(0x980d[3:0],0x980e[7:0])
7819 SPIWrite 701a,00
7820
7821 WAIT 0.1
7822 SPIWrite 701b,07 //DOMAIN_RESET=0x777; Address(0x980d[3:0],0x980e[7:0])
7823 SPIWrite 701a,77
7824 SPIWrite 701b,00 //DOMAIN_RESET=0x0; Address(0x980d[3:0],0x980e[7:0])
7825 SPIWrite 701a,00
7826
7827 WAIT 0.1
7828
7829 //END: Done resetting Serdes
7830
7831
7832 //START: Resetting Serdes
7833
7834 SPIWrite 0016,40 //serdes_jesd=0x2; Address(0x16[7:5])
7835 SPIWrite 701b,08 //DOMAIN_RESET=0x888; Address(0x980d[3:0],0x980e[7:0])
7836 SPIWrite 701a,88
7837 SPIWrite 701b,00 //DOMAIN_RESET=0x0; Address(0x980d[3:0],0x980e[7:0])
7838 SPIWrite 701a,00
7839
7840 WAIT 0.1
7841 SPIWrite 701b,07 //DOMAIN_RESET=0x777; Address(0x980d[3:0],0x980e[7:0])
7842 SPIWrite 701a,77
7843 SPIWrite 701b,00 //DOMAIN_RESET=0x0; Address(0x980d[3:0],0x980e[7:0])
7844 SPIWrite 701a,00
7845
7846 WAIT 0.1
7847
7848 //END: Done resetting Serdes
7849
7850 SPIWrite 0016,00 //serdes_jesd=0x0; Address(0x16[7:5])
7851
7852 //STEP: serdesConfig/step2
7853
7854 //START: Configuring the SERDES
7855
7856 SPIWrite 0016,10 //jesd_subchip=0x1; Address(0x16[7:4])
7857 SPIWrite 00c1,02 //apb_clk_div_factor=0x2; Address(0xc1[7:0])
7858 SPIWrite 00c0,40 //apb_clk_disable=0x0; Address(0xc0[7:0])
7859 SPIWrite 0020,12 //serdesab_apb_page_addr_index=0x2; Address(0x20[7:0])
7860 SPIWrite 0021,12 //serdescd_apb_page_addr_index=0x2; Address(0x21[7:0])
7861 SPIWrite 0016,00 //jesd_subchip=0x0; Address(0x16[7:4])
7862 SPIWrite 0016,60 //serdes_jesd=0x3; Address(0x16[7:5])
7863 SPIWrite 7029,ff
7864 SPIWrite 7028,f0
7865 SPIWrite 701b,0a
7866 SPIWrite 701a,aa
7867 SPIWrite 701b,00
7868 SPIWrite 701a,00
7869 SPIWrite 7007,00
7870 SPIWrite 7006,00
7871 SPIWrite 0016,20 //serdes_jesd=0x1; Address(0x16[7:5])
7872 SPIWrite 49f1,92
7873 SPIWrite 49f0,40
7874 SPIWrite 49f3,ea
7875 SPIWrite 49f2,80
7876 SPIWrite 49e3,f0
7877 SPIWrite 49e2,00
7878 SPIWrite 49b5,47
7879 SPIWrite 49b4,47
7880 SPIWrite 49ff,fd
7881 SPIWrite 49fe,b0

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7882 SPIWrite 49ed,1d
7883 SPIWrite 49ec,c0
7884 SPIWrite 49e7,52
7885 SPIWrite 49e6,26
7886 SPIWrite 49e5,6e
7887 SPIWrite 49e4,b6
7888 SPIWrite 49df,a8
7889 SPIWrite 49de,28
7890 SPIWrite 49eb,63
7891 SPIWrite 49ea,98
7892 SPIWrite 49e9,b2
7893 SPIWrite 49e8,44
7894 SPIWrite 49fd,63
7895 SPIWrite 49fc,98
7896 SPIWrite 49fb,b2
7897 SPIWrite 49fa,48
7898 SPIWrite 49f9,4a
7899 SPIWrite 49f8,44
7900 SPIWrite 49f7,79
7901 SPIWrite 49f6,b6
7902 SPIWrite 49d9,6c
7903 SPIWrite 49d8,06
7904 SPIWrite 4201,10
7905 SPIWrite 4200,6b
7906 SPIWrite 4203,64
7907 SPIWrite 4202,80
7908 SPIWrite 4205,62
7909 SPIWrite 4204,00
7910 SPIWrite 4207,7b
7911 SPIWrite 4206,33
7912 SPIWrite 4209,70
7913 SPIWrite 4208,0a
7914 SPIWrite 420b,bd
7915 SPIWrite 420a,68
7916 SPIWrite 420d,76
7917 SPIWrite 420c,2d
7918 SPIWrite 420f,66
7919 SPIWrite 420e,ab
7920 SPIWrite 4211,d0
7921 SPIWrite 4210,08
7922 SPIWrite 4213,00
7923 SPIWrite 4212,18
7924 SPIWrite 4215,66
7925 SPIWrite 4214,2c
7926 SPIWrite 4217,3d
7927 SPIWrite 4216,15
7928 SPIWrite 4219,00
7929 SPIWrite 4218,80
7930 SPIWrite 421b,00
7931 SPIWrite 421a,02
7932 SPIWrite 421d,34
7933 SPIWrite 421c,00
7934 SPIWrite 421f,00
7935 SPIWrite 421e,00
7936 SPIWrite 4221,10
7937 SPIWrite 4220,1a
7938 SPIWrite 4239,03
7939 SPIWrite 4238,40
7940 SPIWrite 423b,00
7941 SPIWrite 423a,60
7942 SPIWrite 423d,00
7943 SPIWrite 423c,00
7944 SPIWrite 423f,00
7945 SPIWrite 423e,80
7946 SPIWrite 4277,00
7947 SPIWrite 4276,00
7948 SPIWrite 4279,00
7949 SPIWrite 4278,00
7950 SPIWrite 427b,00

7951	SPIWrite	427a,00
7952	SPIWrite	427d,00
7953	SPIWrite	427c,00
7954	SPIWrite	4283,9f
7955	SPIWrite	4282,df
7956	SPIWrite	4285,b3
7957	SPIWrite	4284,c0
7958	SPIWrite	428f,24
7959	SPIWrite	428e,a2
7960	SPIWrite	4291,cc
7961	SPIWrite	4290,34
7962	SPIWrite	4293,e3
7963	SPIWrite	4292,d7
7964	SPIWrite	4295,74
7965	SPIWrite	4294,60
7966	SPIWrite	4297,06
7967	SPIWrite	4296,db
7968	SPIWrite	4341,03
7969	SPIWrite	4340,01
7970	SPIWrite	43e7,00
7971	SPIWrite	43e6,80
7972	SPIWrite	43e9,fc
7973	SPIWrite	43e8,00
7974	SPIWrite	43eb,9f
7975	SPIWrite	43ea,fe
7976	SPIWrite	43ed,00
7977	SPIWrite	43ec,60
7978	SPIWrite	43ef,10
7979	SPIWrite	43ee,00
7980	SPIWrite	43f1,68
7981	SPIWrite	43f0,64
7982	SPIWrite	43f3,92
7983	SPIWrite	43f2,30
7984	SPIWrite	43f5,00
7985	SPIWrite	43f4,00
7986	SPIWrite	43f7,6d
7987	SPIWrite	43f6,87
7988	SPIWrite	43f9,db
7989	SPIWrite	43f8,6c
7990	SPIWrite	43fb,42
7991	SPIWrite	43fa,6e
7992	SPIWrite	43fd,62
7993	SPIWrite	43fc,7c
7994	SPIWrite	43ff,88
7995	SPIWrite	43fe,c8
7996	SPIWrite	4001,10
7997	SPIWrite	4000,6b
7998	SPIWrite	4003,64
7999	SPIWrite	4002,80
8000	SPIWrite	4005,62
8001	SPIWrite	4004,00
8002	SPIWrite	4007,7b
8003	SPIWrite	4006,33
8004	SPIWrite	4009,70
8005	SPIWrite	4008,0a
8006	SPIWrite	400b,bd
8007	SPIWrite	400a,68
8008	SPIWrite	400d,76
8009	SPIWrite	400c,2d
8010	SPIWrite	400f,66
8011	SPIWrite	400e,ab
8012	SPIWrite	4011,d0
8013	SPIWrite	4010,08
8014	SPIWrite	4013,00
8015	SPIWrite	4012,18
8016	SPIWrite	4015,66
8017	SPIWrite	4014,2c
8018	SPIWrite	4017,3d
8019	SPIWrite	4016,15

8020	SPIWrite	4019,00
8021	SPIWrite	4018,80
8022	SPIWrite	401b,00
8023	SPIWrite	401a,02
8024	SPIWrite	401d,34
8025	SPIWrite	401c,00
8026	SPIWrite	401f,00
8027	SPIWrite	401e,00
8028	SPIWrite	4021,10
8029	SPIWrite	4020,1a
8030	SPIWrite	4039,03
8031	SPIWrite	4038,40
8032	SPIWrite	403b,00
8033	SPIWrite	403a,60
8034	SPIWrite	403d,00
8035	SPIWrite	403c,00
8036	SPIWrite	403f,00
8037	SPIWrite	403e,80
8038	SPIWrite	4077,00
8039	SPIWrite	4076,00
8040	SPIWrite	4079,00
8041	SPIWrite	4078,00
8042	SPIWrite	407b,00
8043	SPIWrite	407a,00
8044	SPIWrite	407d,00
8045	SPIWrite	407c,00
8046	SPIWrite	4083,9f
8047	SPIWrite	4082,df
8048	SPIWrite	4085,b3
8049	SPIWrite	4084,c0
8050	SPIWrite	408f,24
8051	SPIWrite	408e,a2
8052	SPIWrite	4091,cc
8053	SPIWrite	4090,34
8054	SPIWrite	4093,e3
8055	SPIWrite	4092,d7
8056	SPIWrite	4095,74
8057	SPIWrite	4094,60
8058	SPIWrite	4097,06
8059	SPIWrite	4096,db
8060	SPIWrite	4141,03
8061	SPIWrite	4140,01
8062	SPIWrite	41e7,00
8063	SPIWrite	41e6,80
8064	SPIWrite	41e9,fc
8065	SPIWrite	41e8,00
8066	SPIWrite	41eb,9f
8067	SPIWrite	41ea,fe
8068	SPIWrite	41ed,00
8069	SPIWrite	41ec,00
8070	SPIWrite	41ef,10
8071	SPIWrite	41ee,00
8072	SPIWrite	41f1,68
8073	SPIWrite	41f0,64
8074	SPIWrite	41f3,92
8075	SPIWrite	41f2,30
8076	SPIWrite	41f5,00
8077	SPIWrite	41f4,00
8078	SPIWrite	41f7,6d
8079	SPIWrite	41f6,87
8080	SPIWrite	41f9,db
8081	SPIWrite	41f8,6c
8082	SPIWrite	41fb,42
8083	SPIWrite	41fa,6e
8084	SPIWrite	41fd,62
8085	SPIWrite	41fc,7c
8086	SPIWrite	41ff,88
8087	SPIWrite	41fe,c8
8088	SPIWrite	4401,10

8089	SPIWrite	4400,6b
8090	SPIWrite	4403,64
8091	SPIWrite	4402,80
8092	SPIWrite	4405,62
8093	SPIWrite	4404,00
8094	SPIWrite	4407,7b
8095	SPIWrite	4406,33
8096	SPIWrite	4409,70
8097	SPIWrite	4408,0a
8098	SPIWrite	440b,bd
8099	SPIWrite	440a,68
8100	SPIWrite	440d,76
8101	SPIWrite	440c,2d
8102	SPIWrite	440f,66
8103	SPIWrite	440e,ab
8104	SPIWrite	4411,d0
8105	SPIWrite	4410,08
8106	SPIWrite	4413,00
8107	SPIWrite	4412,18
8108	SPIWrite	4415,66
8109	SPIWrite	4414,2c
8110	SPIWrite	4417,3d
8111	SPIWrite	4416,15
8112	SPIWrite	4419,00
8113	SPIWrite	4418,80
8114	SPIWrite	441b,00
8115	SPIWrite	441a,02
8116	SPIWrite	441d,34
8117	SPIWrite	441c,00
8118	SPIWrite	441f,00
8119	SPIWrite	441e,00
8120	SPIWrite	4421,10
8121	SPIWrite	4420,1a
8122	SPIWrite	4439,03
8123	SPIWrite	4438,40
8124	SPIWrite	443b,00
8125	SPIWrite	443a,60
8126	SPIWrite	443d,00
8127	SPIWrite	443c,00
8128	SPIWrite	443f,00
8129	SPIWrite	443e,80
8130	SPIWrite	4477,00
8131	SPIWrite	4476,00
8132	SPIWrite	4479,00
8133	SPIWrite	4478,00
8134	SPIWrite	447b,00
8135	SPIWrite	447a,00
8136	SPIWrite	447d,00
8137	SPIWrite	447c,00
8138	SPIWrite	4483,9f
8139	SPIWrite	4482,df
8140	SPIWrite	4485,b3
8141	SPIWrite	4484,c0
8142	SPIWrite	448f,24
8143	SPIWrite	448e,a2
8144	SPIWrite	4491,cc
8145	SPIWrite	4490,34
8146	SPIWrite	4493,e3
8147	SPIWrite	4492,d7
8148	SPIWrite	4495,74
8149	SPIWrite	4494,60
8150	SPIWrite	4497,06
8151	SPIWrite	4496,db
8152	SPIWrite	4541,03
8153	SPIWrite	4540,01
8154	SPIWrite	45e7,00
8155	SPIWrite	45e6,80
8156	SPIWrite	45e9,fc
8157	SPIWrite	45e8,00

8158 SPIWrite 45eb,9f
8159 SPIWrite 45ea,fe
8160 SPIWrite 45ed,00
8161 SPIWrite 45ec,00
8162 SPIWrite 45ef,10
8163 SPIWrite 45ee,00
8164 SPIWrite 45f1,68
8165 SPIWrite 45f0,64
8166 SPIWrite 45f3,92
8167 SPIWrite 45f2,30
8168 SPIWrite 45f5,00
8169 SPIWrite 45f4,00
8170 SPIWrite 45f7,6d
8171 SPIWrite 45f6,87
8172 SPIWrite 45f9,db
8173 SPIWrite 45f8,6c
8174 SPIWrite 45fb,42
8175 SPIWrite 45fa,6e
8176 SPIWrite 45fd,62
8177 SPIWrite 45fc,7c
8178 SPIWrite 45ff,88
8179 SPIWrite 45fe,c8
8180 SPIWrite 4601,10
8181 SPIWrite 4600,6b
8182 SPIWrite 4603,64
8183 SPIWrite 4602,80
8184 SPIWrite 4605,62
8185 SPIWrite 4604,00
8186 SPIWrite 4607,7b
8187 SPIWrite 4606,33
8188 SPIWrite 4609,70
8189 SPIWrite 4608,0a
8190 SPIWrite 460b,bd
8191 SPIWrite 460a,68
8192 SPIWrite 460d,76
8193 SPIWrite 460c,2d
8194 SPIWrite 460f,66
8195 SPIWrite 460e,ab
8196 SPIWrite 4611,d0
8197 SPIWrite 4610,08
8198 SPIWrite 4613,00
8199 SPIWrite 4612,18
8200 SPIWrite 4615,66
8201 SPIWrite 4614,2c
8202 SPIWrite 4617,3d
8203 SPIWrite 4616,15
8204 SPIWrite 4619,00
8205 SPIWrite 4618,80
8206 SPIWrite 461b,00
8207 SPIWrite 461a,02
8208 SPIWrite 461d,34
8209 SPIWrite 461c,00
8210 SPIWrite 461f,00
8211 SPIWrite 461e,00
8212 SPIWrite 4621,10
8213 SPIWrite 4620,1a
8214 SPIWrite 4639,03
8215 SPIWrite 4638,40
8216 SPIWrite 463b,00
8217 SPIWrite 463a,60
8218 SPIWrite 463d,00
8219 SPIWrite 463c,00
8220 SPIWrite 463f,00
8221 SPIWrite 463e,80
8222 SPIWrite 4677,00
8223 SPIWrite 4676,00
8224 SPIWrite 4679,00
8225 SPIWrite 4678,00
8226 SPIWrite 467b,00

8227 SPIWrite 467a,00
8228 SPIWrite 467d,00
8229 SPIWrite 467c,00
8230 SPIWrite 4683,9f
8231 SPIWrite 4682,df
8232 SPIWrite 4685,b3
8233 SPIWrite 4684,c0
8234 SPIWrite 468f,24
8235 SPIWrite 468e,a2
8236 SPIWrite 4691,cc
8237 SPIWrite 4690,34
8238 SPIWrite 4693,e3
8239 SPIWrite 4692,d7
8240 SPIWrite 4695,74
8241 SPIWrite 4694,60
8242 SPIWrite 4697,06
8243 SPIWrite 4696,db
8244 SPIWrite 4741,03
8245 SPIWrite 4740,01
8246 SPIWrite 47e7,00
8247 SPIWrite 47e6,80
8248 SPIWrite 47e9,fc
8249 SPIWrite 47e8,00
8250 SPIWrite 47eb,9f
8251 SPIWrite 47ea,fe
8252 SPIWrite 47ed,00
8253 SPIWrite 47ec,00
8254 SPIWrite 47ef,10
8255 SPIWrite 47ee,00
8256 SPIWrite 47f1,68
8257 SPIWrite 47f0,64
8258 SPIWrite 47f3,92
8259 SPIWrite 47f2,30
8260 SPIWrite 47f5,00
8261 SPIWrite 47f4,00
8262 SPIWrite 47f7,6d
8263 SPIWrite 47f6,87
8264 SPIWrite 47f9,db
8265 SPIWrite 47f8,6c
8266 SPIWrite 47fb,42
8267 SPIWrite 47fa,6e
8268 SPIWrite 47fd,62
8269 SPIWrite 47fc,7c
8270 SPIWrite 47ff,88
8271 SPIWrite 47fe,c8
8272 SPIWrite 0016,40
8273 SPIWrite 49f1,82
8274 SPIWrite 49f0,40
8275 SPIWrite 49f3,e2
8276 SPIWrite 49f2,80
8277 SPIWrite 49e3,b0
8278 SPIWrite 49e2,00
8279 SPIWrite 49b5,47
8280 SPIWrite 49b4,47
8281 SPIWrite 49ff,ed
8282 SPIWrite 49fe,b0
8283 SPIWrite 49ed,0d
8284 SPIWrite 49ec,c0
8285 SPIWrite 49e7,52
8286 SPIWrite 49e6,26
8287 SPIWrite 49e5,6e
8288 SPIWrite 49e4,b6
8289 SPIWrite 49df,a8
8290 SPIWrite 49de,28
8291 SPIWrite 49eb,63
8292 SPIWrite 49ea,18
8293 SPIWrite 49e9,b2
8294 SPIWrite 49e8,44
8295 SPIWrite 49fd,63

//serdes_jesd=0x2; Address(0x16[7:5])

8296 SPIWrite 49fc,18
8297 SPIWrite 49fb,b2
8298 SPIWrite 49fa,48
8299 SPIWrite 49f9,4a
8300 SPIWrite 49f8,44
8301 SPIWrite 49f7,79
8302 SPIWrite 49f6,b6
8303 SPIWrite 49d9,6c
8304 SPIWrite 49d8,06
8305 SPIWrite 4601,10
8306 SPIWrite 4600,6b
8307 SPIWrite 4603,64
8308 SPIWrite 4602,80
8309 SPIWrite 4605,62
8310 SPIWrite 4604,00
8311 SPIWrite 4607,7b
8312 SPIWrite 4606,33
8313 SPIWrite 4609,70
8314 SPIWrite 4608,0a
8315 SPIWrite 460b,bd
8316 SPIWrite 460a,68
8317 SPIWrite 460d,76
8318 SPIWrite 460c,2d
8319 SPIWrite 460f,66
8320 SPIWrite 460e,ab
8321 SPIWrite 4611,d0
8322 SPIWrite 4610,08
8323 SPIWrite 4613,00
8324 SPIWrite 4612,18
8325 SPIWrite 4615,66
8326 SPIWrite 4614,2c
8327 SPIWrite 4617,3d
8328 SPIWrite 4616,15
8329 SPIWrite 4619,00
8330 SPIWrite 4618,80
8331 SPIWrite 461b,00
8332 SPIWrite 461a,02
8333 SPIWrite 461d,34
8334 SPIWrite 461c,00
8335 SPIWrite 461f,00
8336 SPIWrite 461e,00
8337 SPIWrite 4621,10
8338 SPIWrite 4620,1a
8339 SPIWrite 4639,03
8340 SPIWrite 4638,40
8341 SPIWrite 463b,00
8342 SPIWrite 463a,60
8343 SPIWrite 463d,00
8344 SPIWrite 463c,00
8345 SPIWrite 463f,00
8346 SPIWrite 463e,80
8347 SPIWrite 4677,00
8348 SPIWrite 4676,00
8349 SPIWrite 4679,00
8350 SPIWrite 4678,00
8351 SPIWrite 467b,00
8352 SPIWrite 467a,00
8353 SPIWrite 467d,00
8354 SPIWrite 467c,00
8355 SPIWrite 4683,9f
8356 SPIWrite 4682,df
8357 SPIWrite 4685,b3
8358 SPIWrite 4684,c0
8359 SPIWrite 468f,24
8360 SPIWrite 468e,a2
8361 SPIWrite 4691,cc
8362 SPIWrite 4690,34
8363 SPIWrite 4693,e3
8364 SPIWrite 4692,d7

8365 SPIWrite 4695,74
8366 SPIWrite 4694,60
8367 SPIWrite 4697,06
8368 SPIWrite 4696,db
8369 SPIWrite 4741,03
8370 SPIWrite 4740,01
8371 SPIWrite 47e7,00
8372 SPIWrite 47e6,80
8373 SPIWrite 47e9,fc
8374 SPIWrite 47e8,00
8375 SPIWrite 47eb,1f
8376 SPIWrite 47ea,fe
8377 SPIWrite 47ed,00
8378 SPIWrite 47ec,00
8379 SPIWrite 47ef,10
8380 SPIWrite 47ee,00
8381 SPIWrite 47f1,68
8382 SPIWrite 47f0,64
8383 SPIWrite 47f3,92
8384 SPIWrite 47f2,30
8385 SPIWrite 47f5,00
8386 SPIWrite 47f4,00
8387 SPIWrite 47f7,6d
8388 SPIWrite 47f6,83
8389 SPIWrite 47f9,db
8390 SPIWrite 47f8,6c
8391 SPIWrite 47fb,42
8392 SPIWrite 47fa,6e
8393 SPIWrite 47fd,62
8394 SPIWrite 47fc,78
8395 SPIWrite 47ff,08
8396 SPIWrite 47fe,c8
8397 SPIWrite 4401,10
8398 SPIWrite 4400,6b
8399 SPIWrite 4403,64
8400 SPIWrite 4402,80
8401 SPIWrite 4405,62
8402 SPIWrite 4404,00
8403 SPIWrite 4407,7b
8404 SPIWrite 4406,33
8405 SPIWrite 4409,70
8406 SPIWrite 4408,0a
8407 SPIWrite 440b,bd
8408 SPIWrite 440a,68
8409 SPIWrite 440d,76
8410 SPIWrite 440c,2d
8411 SPIWrite 440f,66
8412 SPIWrite 440e,ab
8413 SPIWrite 4411,d0
8414 SPIWrite 4410,08
8415 SPIWrite 4413,00
8416 SPIWrite 4412,18
8417 SPIWrite 4415,66
8418 SPIWrite 4414,2c
8419 SPIWrite 4417,3d
8420 SPIWrite 4416,15
8421 SPIWrite 4419,00
8422 SPIWrite 4418,80
8423 SPIWrite 441b,00
8424 SPIWrite 441a,02
8425 SPIWrite 441d,34
8426 SPIWrite 441c,00
8427 SPIWrite 441f,00
8428 SPIWrite 441e,00
8429 SPIWrite 4421,10
8430 SPIWrite 4420,1a
8431 SPIWrite 4439,03
8432 SPIWrite 4438,40
8433 SPIWrite 443b,00

8434 SPIWrite 443a,60
8435 SPIWrite 443d,00
8436 SPIWrite 443c,00
8437 SPIWrite 443f,00
8438 SPIWrite 443e,80
8439 SPIWrite 4477,00
8440 SPIWrite 4476,00
8441 SPIWrite 4479,00
8442 SPIWrite 4478,00
8443 SPIWrite 447b,00
8444 SPIWrite 447a,00
8445 SPIWrite 447d,00
8446 SPIWrite 447c,00
8447 SPIWrite 4483,9f
8448 SPIWrite 4482,df
8449 SPIWrite 4485,b3
8450 SPIWrite 4484,c0
8451 SPIWrite 448f,24
8452 SPIWrite 448e,a2
8453 SPIWrite 4491,cc
8454 SPIWrite 4490,34
8455 SPIWrite 4493,e3
8456 SPIWrite 4492,d7
8457 SPIWrite 4495,74
8458 SPIWrite 4494,60
8459 SPIWrite 4497,06
8460 SPIWrite 4496,db
8461 SPIWrite 4541,03
8462 SPIWrite 4540,01
8463 SPIWrite 45e7,00
8464 SPIWrite 45e6,80
8465 SPIWrite 45e9,fc
8466 SPIWrite 45e8,00
8467 SPIWrite 45eb,1f
8468 SPIWrite 45ea,fe
8469 SPIWrite 45ed,00
8470 SPIWrite 45ec,00
8471 SPIWrite 45ef,10
8472 SPIWrite 45ee,00
8473 SPIWrite 45f1,68
8474 SPIWrite 45f0,64
8475 SPIWrite 45f3,92
8476 SPIWrite 45f2,30
8477 SPIWrite 45f5,00
8478 SPIWrite 45f4,00
8479 SPIWrite 45f7,6d
8480 SPIWrite 45f6,83
8481 SPIWrite 45f9,db
8482 SPIWrite 45f8,6c
8483 SPIWrite 45fb,42
8484 SPIWrite 45fa,6e
8485 SPIWrite 45fd,62
8486 SPIWrite 45fc,78
8487 SPIWrite 45ff,08
8488 SPIWrite 45fe,c8
8489 SPIWrite 4001,10
8490 SPIWrite 4000,6b
8491 SPIWrite 4003,64
8492 SPIWrite 4002,80
8493 SPIWrite 4005,62
8494 SPIWrite 4004,00
8495 SPIWrite 4007,7b
8496 SPIWrite 4006,33
8497 SPIWrite 4009,70
8498 SPIWrite 4008,0a
8499 SPIWrite 400b,bd
8500 SPIWrite 400a,68
8501 SPIWrite 400d,76
8502 SPIWrite 400c,2d

8503	SPIWrite	400f,66
8504	SPIWrite	400e,ab
8505	SPIWrite	4011,d0
8506	SPIWrite	4010,08
8507	SPIWrite	4013,00
8508	SPIWrite	4012,18
8509	SPIWrite	4015,66
8510	SPIWrite	4014,2c
8511	SPIWrite	4017,3d
8512	SPIWrite	4016,15
8513	SPIWrite	4019,00
8514	SPIWrite	4018,80
8515	SPIWrite	401b,00
8516	SPIWrite	401a,02
8517	SPIWrite	401d,34
8518	SPIWrite	401c,00
8519	SPIWrite	401f,00
8520	SPIWrite	401e,00
8521	SPIWrite	4021,10
8522	SPIWrite	4020,1a
8523	SPIWrite	4039,03
8524	SPIWrite	4038,40
8525	SPIWrite	403b,00
8526	SPIWrite	403a,60
8527	SPIWrite	403d,00
8528	SPIWrite	403c,00
8529	SPIWrite	403f,00
8530	SPIWrite	403e,80
8531	SPIWrite	4077,00
8532	SPIWrite	4076,00
8533	SPIWrite	4079,00
8534	SPIWrite	4078,00
8535	SPIWrite	407b,00
8536	SPIWrite	407a,00
8537	SPIWrite	407d,00
8538	SPIWrite	407c,00
8539	SPIWrite	4083,9f
8540	SPIWrite	4082,df
8541	SPIWrite	4085,b3
8542	SPIWrite	4084,c0
8543	SPIWrite	408f,24
8544	SPIWrite	408e,a2
8545	SPIWrite	4091,cc
8546	SPIWrite	4090,34
8547	SPIWrite	4093,e3
8548	SPIWrite	4092,d7
8549	SPIWrite	4095,74
8550	SPIWrite	4094,60
8551	SPIWrite	4097,06
8552	SPIWrite	4096,db
8553	SPIWrite	4141,03
8554	SPIWrite	4140,01
8555	SPIWrite	41e7,00
8556	SPIWrite	41e6,80
8557	SPIWrite	41e9,fc
8558	SPIWrite	41e8,00
8559	SPIWrite	41eb,1f
8560	SPIWrite	41ea,fe
8561	SPIWrite	41ed,00
8562	SPIWrite	41ec,00
8563	SPIWrite	41ef,10
8564	SPIWrite	41ee,00
8565	SPIWrite	41f1,68
8566	SPIWrite	41f0,64
8567	SPIWrite	41f3,92
8568	SPIWrite	41f2,30
8569	SPIWrite	41f5,00
8570	SPIWrite	41f4,00
8571	SPIWrite	41f7,6d

8572	SPIWrite	41f6,83
8573	SPIWrite	41f9,db
8574	SPIWrite	41f8,6c
8575	SPIWrite	41fb,42
8576	SPIWrite	41fa,6e
8577	SPIWrite	41fd,62
8578	SPIWrite	41fc,78
8579	SPIWrite	41ff,08
8580	SPIWrite	41fe,c8
8581	SPIWrite	4201,10
8582	SPIWrite	4200,6b
8583	SPIWrite	4203,64
8584	SPIWrite	4202,80
8585	SPIWrite	4205,62
8586	SPIWrite	4204,00
8587	SPIWrite	4207,7b
8588	SPIWrite	4206,33
8589	SPIWrite	4209,70
8590	SPIWrite	4208,0a
8591	SPIWrite	420b,bd
8592	SPIWrite	420a,68
8593	SPIWrite	420d,76
8594	SPIWrite	420c,2d
8595	SPIWrite	420f,66
8596	SPIWrite	420e,ab
8597	SPIWrite	4211,d0
8598	SPIWrite	4210,08
8599	SPIWrite	4213,00
8600	SPIWrite	4212,18
8601	SPIWrite	4215,66
8602	SPIWrite	4214,2c
8603	SPIWrite	4217,3d
8604	SPIWrite	4216,15
8605	SPIWrite	4219,00
8606	SPIWrite	4218,80
8607	SPIWrite	421b,00
8608	SPIWrite	421a,02
8609	SPIWrite	421d,34
8610	SPIWrite	421c,00
8611	SPIWrite	421f,00
8612	SPIWrite	421e,00
8613	SPIWrite	4221,10
8614	SPIWrite	4220,1a
8615	SPIWrite	4239,03
8616	SPIWrite	4238,40
8617	SPIWrite	423b,00
8618	SPIWrite	423a,60
8619	SPIWrite	423d,00
8620	SPIWrite	423c,00
8621	SPIWrite	423f,00
8622	SPIWrite	423e,80
8623	SPIWrite	4277,00
8624	SPIWrite	4276,00
8625	SPIWrite	4279,00
8626	SPIWrite	4278,00
8627	SPIWrite	427b,00
8628	SPIWrite	427a,00
8629	SPIWrite	427d,00
8630	SPIWrite	427c,00
8631	SPIWrite	4283,9f
8632	SPIWrite	4282,df
8633	SPIWrite	4285,b3
8634	SPIWrite	4284,c0
8635	SPIWrite	428f,24
8636	SPIWrite	428e,a2
8637	SPIWrite	4291,cc
8638	SPIWrite	4290,34
8639	SPIWrite	4293,e3
8640	SPIWrite	4292,d7

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8641 SPIWrite 4295,74
8642 SPIWrite 4294,60
8643 SPIWrite 4297,06
8644 SPIWrite 4296,db
8645 SPIWrite 4341,03
8646 SPIWrite 4340,01
8647 SPIWrite 43e7,00
8648 SPIWrite 43e6,80
8649 SPIWrite 43e9,fc
8650 SPIWrite 43e8,00
8651 SPIWrite 43eb,1f
8652 SPIWrite 43ea,fe
8653 SPIWrite 43ed,00
8654 SPIWrite 43ec,60
8655 SPIWrite 43ef,10
8656 SPIWrite 43ee,00
8657 SPIWrite 43f1,68
8658 SPIWrite 43f0,64
8659 SPIWrite 43f3,92
8660 SPIWrite 43f2,30
8661 SPIWrite 43f5,00
8662 SPIWrite 43f4,00
8663 SPIWrite 43f7,6d
8664 SPIWrite 43f6,83
8665 SPIWrite 43f9,db
8666 SPIWrite 43f8,6c
8667 SPIWrite 43fb,42
8668 SPIWrite 43fa,6e
8669 SPIWrite 43fd,62
8670 SPIWrite 43fc,78
8671 SPIWrite 43ff,08
8672 SPIWrite 43fe,c8
8673 SPIWrite 0016,60 //serdes_jesd=0x3; Address(0x16[7:5])
8674 SPIWrite 7007,00 //BUS_WIDTH_LANE0=0x0; Address(0x9803[7:0])
8675 SPIWrite 7006,00
8676 SPIWrite 7007,00 //BUS_WIDTH_LANE1=0x0; Address(0x9803[7:1])
8677 SPIWrite 7006,00
8678 SPIWrite 7007,00 //BUS_WIDTH_LANE2=0x0; Address(0x9803[7:2])
8679 SPIWrite 7006,00
8680 SPIWrite 7007,00 //BUS_WIDTH_LANE3=0x0; Address(0x9803[7:3])
8681 SPIWrite 7006,00
8682 SPIWrite 0016,00 //serdes_jesd=0x0; Address(0x16[7:5])
8683
8684 //END: Done configuring the SERDES
8685
8686
8687 //STEP: serdesConfig/step3
8688
8689 //START: Loading Serdes Firmware.
8690
8691 SPIWrite 0018,20 //macro=0x1; Address(0x18[7:5])
8692 SPIRead 00f0
8693
8694 //Read MACRO_READY=0x1; Address(0xf0[7:0])
8695
8696
8697 SPIPoll 00f0,0,0,1
8698
8699 SPIWrite 00a3,00 //MACRO_OPERAND_REG0=0x10300;
Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
8700 SPIWrite 00a2,01
8701 SPIWrite 00a1,03
8702 SPIWrite 00a0,00
8703 SPIWrite 0193,79 //MACRO_OPCODE=0x79; Address(0x193[7:0],0x194[7:0])
8704
8705 WAIT 0.001
8706 SPIRead 00f0
8707
8708 //Read MACRO_DONE=0x1; Address(0xf0[7:2])

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8709
8710
8711 SPIPoll 00f0,2,2,4
8712
8713 SPIRead 00f0
8714
8715 //Read MACRO_ERROR=0x0; Address(0xf0[7:3])
8716
8717 SPIRead 00f1
8718
8719 //Read MACRO_ERROR_OPCODE=0x0; Address(0xf1[7:0],0xf2[7:0])
8720
8721 SPIRead 00f0
8722
8723 //Read MACRO_ERROR_IN_OPCODE=0x0; Address(0xf0[7:4])
8724
8725 SPIRead 00f0
8726
8727 //Read MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0; Address(0xf0[7:5])
8728
8729 SPIRead 00f0
8730
8731 //Read MACRO_ERROR_IN_OPERAND=0x0; Address(0xf0[7:6])
8732
8733 SPIRead 00f0
8734
8735 //Read MACRO_ERROR_IN_EXECUTION=0x0; Address(0xf0[7:7])
8736
8737 SPIRead 00f3
8738 SPIRead 00f2
8739
8740 //Read MACRO_ERROR_EXTENDED_CODE=0x0; Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
8741
8742 SPIRead 00f7
8743 SPIRead 00f6
8744 SPIRead 00f5
8745 SPIRead 00f4
8746
8747 //Read MACRO_ERROR_EXTENDED_CODE_2=0x0;
Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
8748
8749 SPIRead 00f0
8750
8751 //Read MACRO_READY=0x1; Address(0xf0[7:0])
8752
8753
8754 SPIPoll 00f0,0,0,1
8755
8756 SPIWrite 00a3,00 //MACRO_OPERAND_REG0=0x10301;
Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
8757 SPIWrite 00a2,01
8758 SPIWrite 00a1,03
8759 SPIWrite 00a0,01
8760 SPIWrite 0193,79 //MACRO_OPCODE=0x79; Address(0x193[7:0],0x194[7:0])
8761
8762 WAIT 0.001
8763 SPIRead 00f0
8764
8765 //Read MACRO_DONE=0x1; Address(0xf0[7:2])
8766
8767
8768 SPIPoll 00f0,2,2,4
8769
8770 SPIRead 00f0
8771
8772 //Read MACRO_ERROR=0x0; Address(0xf0[7:3])
8773
8774 SPIRead 00f1
8775

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8776 //Read  MACRO_ERROR_OPCODE=0x0;      Address(0xf1[7:0],0xf2[7:0])
8777
8778 SPIRead 00f0
8779
8780 //Read  MACRO_ERROR_IN_OPCODE=0x0;   Address(0xf0[7:4])
8781
8782 SPIRead 00f0
8783
8784 //Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;      Address(0xf0[7:5])
8785
8786 SPIRead 00f0
8787
8788 //Read  MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])
8789
8790 SPIRead 00f0
8791
8792 //Read  MACRO_ERROR_IN_EXECUTION=0x0;   Address(0xf0[7:7])
8793
8794 SPIRead 00f3
8795 SPIRead 00f2
8796
8797 //Read  MACRO_ERROR_EXTENDED_CODE=0x0;   Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
8798
8799 SPIRead 00f7
8800 SPIRead 00f6
8801 SPIRead 00f5
8802 SPIRead 00f4
8803
8804 //Read  MACRO_ERROR_EXTENDED_CODE_2=0x0;
Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
8805
8806 SPIWrite 0018,00 //macro=0x0;      Address(0x18[7:5])
8807 SPIWrite 0016,60 //serdes_jesd=0x3;   Address(0x16[7:5])
8808 SPIWrite 702d,00
8809 SPIWrite 702c,05
8810 SPIWrite 7025,00
8811 SPIWrite 7024,08
8812 SPIWrite 702b,e0
8813 SPIWrite 702a,20
8814
8815 WAIT 0.01
8816 SPIWrite 702d,00
8817 SPIWrite 702c,02
8818 SPIWrite 7025,00
8819 SPIWrite 7024,50
8820 SPIWrite 702b,e0
8821 SPIWrite 702a,20
8822
8823 WAIT 0.01
8824 SPIWrite 701b,07 //DOMAIN_RESET=0x777;   Address(0x980d[3:0],0x980e[7:0])
8825 SPIWrite 701a,77
8826 SPIWrite 701b,00 //DOMAIN_RESET=0x0;      Address(0x980d[3:0],0x980e[7:0])
8827 SPIWrite 701a,00
8828
8829 WAIT 5
8830 SPIWrite 0016,00 //serdes_jesd=0x0;   Address(0x16[7:5])
8831
8832 //END: Done loading Serdes Firmware.
8833
8834
8835 //STEP: topConfig/step0
8836
8837 //START: Setting Top Control Modes
8838
8839 SPIWrite 0015,80 //timing_controller=0x1;   Address(0x15[7:7])
8840 SPIWrite 0081,00 //fdd_mode=0x0;      Address(0x81[7:0])
8841 SPIWrite 0080,01 //mode_2t2r=0x1;      Address(0x80[7:0])
8842 SPIWrite 008c,01 //use_per_ch_txab_tdd=0x1;   Address(0x8c[7:0])
8843 SPIWrite 008d,01 //use_per_ch_txcd_tdd=0x1;   Address(0x8d[7:0])

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8844 SPIWrite 00a0,01 //use_per_ch_rxab_tdd=0x1; Address(0xa0[7:0])
8845 SPIWrite 00a1,01 //use_per_ch_rxcd_tdd=0x1; Address(0xa1[7:0])
8846 SPIWrite 0015,00 //timing_controller=0x0; Address(0x15[7:7])
8847 SPIWrite 0015,02 //ana_4t4r=0x1; Address(0x15[7:1])
8848 SPIWrite 0129,00 //tx_dac_div2=0x0; Address(0x129[7:0])
8849 SPIWrite 012a,00 //rx_adc_div2=0x0; Address(0x12a[7:0])
8850 SPIWrite 012b,00 //fb_adc_div2=0x0; Address(0x12b[7:0])
8851 SPIWrite 00dc,00 //clk_out_sel_tx_ab=0x0; Address(0xdc[7:0])
8852 SPIWrite 00df,00 //clk_out_sel_tx_cd=0x0; Address(0xdf[7:0])
8853 SPIWrite 00c4,00 //clk_out_sel_fb_ab=0x0; Address(0xc4[7:0])
8854 SPIWrite 00c7,00 //clk_out_sel_fb_cd=0x0; Address(0xc7[7:0])
8855 SPIWrite 00cc,00 //clk_out_sel_rx_ab=0x0; Address(0xcc[7:0])
8856 SPIWrite 00cf,00 //clk_out_sel_rx_cd=0x0; Address(0xcf[7:0])
8857 SPIWrite 0015,00 //ana_4t4r=0x0; Address(0x15[7:1])
8858 SPIWrite 0015,80 //timing_controller=0x1; Address(0x15[7:7])
8859 SPIWrite 0399,00 //config_rise_xx_A_7=0x0; Address(0x399[7:0],0x399[7:0],0x39a[7:0])
8860 SPIWrite 0398,00
8861 SPIWrite 039b,00 //config_fall_xx_A_7=0xe1; Address(0x39a[7:0],0x39b[7:0],0x39c[7:0])
8862 SPIWrite 039a,e1
8863 SPIWrite 0451,00 //config_rise_xx_A_7=0x0; Address(0x450[7:0],0x451[7:0],0x452[7:0])
8864 SPIWrite 0450,00
8865 SPIWrite 0453,00 //config_fall_xx_A_7=0xe1; Address(0x452[7:0],0x453[7:0],0x454[7:0])
8866 SPIWrite 0452,e1
8867 SPIWrite 0509,00 //config_rise_xx_A_7=0x0; Address(0x508[7:0],0x509[7:0],0x50a[7:0])
8868 SPIWrite 0508,00
8869 SPIWrite 050b,00 //config_fall_xx_A_7=0xe1; Address(0x50a[7:0],0x50b[7:0],0x50c[7:0])
8870 SPIWrite 050a,e1
8871 SPIWrite 05c1,00 //config_rise_xx_A_7=0x0; Address(0x5c0[7:0],0x5c1[7:0],0x5c2[7:0])
8872 SPIWrite 05c0,00
8873 SPIWrite 05c3,00 //config_fall_xx_A_7=0xe1; Address(0x5c2[7:0],0x5c3[7:0],0x5c4[7:0])
8874 SPIWrite 05c2,e1
8875 SPIWrite 0679,00 //config_rise_xx_A_7=0x0; Address(0x678[7:0],0x679[7:0],0x67a[7:0])
8876 SPIWrite 0678,00
8877 SPIWrite 067b,00 //config_fall_xx_A_7=0xe1; Address(0x67a[7:0],0x67b[7:0],0x67c[7:0])
8878 SPIWrite 067a,e1
8879 SPIWrite 0731,00 //config_rise_xx_A_7=0x0; Address(0x730[7:0],0x731[7:0],0x732[7:0])
8880 SPIWrite 0730,00
8881 SPIWrite 0733,00 //config_fall_xx_A_7=0xe1; Address(0x732[7:0],0x733[7:0],0x734[7:0])
8882 SPIWrite 0732,e1
8883
8884 //END: Setting Top Control Modes
8885
8886 SPIWrite 0015,00 //timing_controller=0x0; Address(0x15[7:7])
8887 SPIWrite 0015,40 //digtop=0x1; Address(0x15[7:6])
8888 SPIWrite 0180,00 //spi_ids_dsa_ab=0x0; Address(0x180[7:0])
8889 SPIWrite 0181,00 //spi_ids_dsa_cd=0x0; Address(0x181[7:0])
8890 SPIWrite 0015,00 //digtop=0x0; Address(0x15[7:6])
8891
8892 //STEP: topConfig/step1
8893 SPIWrite 0013,40 //dsa_page1=0x1; Address(0x13[7:6])
8894 SPIWrite 054e,00 //tm_gate_clk=0x0; Address(0x54e[7:0])
8895 SPIWrite 0013,80 //dsa_page1=0x2; Address(0x13[7:6])
8896 SPIWrite 054e,00 //tm_gate_clk=0x0; Address(0x54e[7:0])
8897 SPIWrite 0013,c0 //dsa_page1=0x3; Address(0x13[7:6])
8898 SPIWrite 0444,03
8899 SPIWrite 0445,00
8900 SPIWrite 0446,00
8901 SPIWrite 0447,00
8902 SPIWrite 0448,0b
8903 SPIWrite 0449,84
8904 SPIWrite 044a,00
8905 SPIWrite 044b,00
8906 SPIWrite 044c,1f
8907 SPIWrite 044d,08
8908 SPIWrite 044e,01
8909 SPIWrite 044f,00
8910 SPIWrite 0450,33
8911 SPIWrite 0451,8c
8912 SPIWrite 0452,01

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8913	SPIWrite	0453,00
8914	SPIWrite	0454,47
8915	SPIWrite	0455,90
8916	SPIWrite	0456,02
8917	SPIWrite	0457,00
8918	SPIWrite	0458,5b
8919	SPIWrite	0459,14
8920	SPIWrite	045a,03
8921	SPIWrite	045b,01
8922	SPIWrite	045c,6f
8923	SPIWrite	045d,18
8924	SPIWrite	045e,04
8925	SPIWrite	045f,01
8926	SPIWrite	0460,83
8927	SPIWrite	0461,9c
8928	SPIWrite	0462,04
8929	SPIWrite	0463,01
8930	SPIWrite	0464,9b
8931	SPIWrite	0465,a0
8932	SPIWrite	0466,05
8933	SPIWrite	0467,02
8934	SPIWrite	0468,b3
8935	SPIWrite	0469,a4
8936	SPIWrite	046a,06
8937	SPIWrite	046b,02
8938	SPIWrite	046c,c7
8939	SPIWrite	046d,a8
8940	SPIWrite	046e,07
8941	SPIWrite	046f,03
8942	SPIWrite	0470,df
8943	SPIWrite	0471,ac
8944	SPIWrite	0472,08
8945	SPIWrite	0473,03
8946	SPIWrite	0474,f7
8947	SPIWrite	0475,b0
8948	SPIWrite	0476,09
8949	SPIWrite	0477,04
8950	SPIWrite	0478,17
8951	SPIWrite	0479,b5
8952	SPIWrite	047a,0a
8953	SPIWrite	047b,04
8954	SPIWrite	047c,37
8955	SPIWrite	047d,b9
8956	SPIWrite	047e,0b
8957	SPIWrite	047f,04
8958	SPIWrite	0480,4f
8959	SPIWrite	0481,bd
8960	SPIWrite	0482,0c
8961	SPIWrite	0483,05
8962	SPIWrite	0484,6b
8963	SPIWrite	0485,c1
8964	SPIWrite	0486,0d
8965	SPIWrite	0487,07
8966	SPIWrite	0488,87
8967	SPIWrite	0489,c5
8968	SPIWrite	048a,0e
8969	SPIWrite	048b,07
8970	SPIWrite	048c,9f
8971	SPIWrite	048d,c9
8972	SPIWrite	048e,0f
8973	SPIWrite	048f,07
8974	SPIWrite	0490,a7
8975	SPIWrite	0491,49
8976	SPIWrite	0492,10
8977	SPIWrite	0493,07
8978	SPIWrite	0494,bb
8979	SPIWrite	0495,4d
8980	SPIWrite	0496,11
8981	SPIWrite	0497,08

8982 SPIWrite 0498,d3
8983 SPIWrite 0499,51
8984 SPIWrite 049a,12
8985 SPIWrite 049b,09
8986 SPIWrite 049c,eb
8987 SPIWrite 049d,55
8988 SPIWrite 049e,13
8989 SPIWrite 049f,0a
8990 SPIWrite 04a0,0b
8991 SPIWrite 04a1,da
8992 SPIWrite 04a2,14
8993 SPIWrite 04a3,0b
8994 SPIWrite 04a4,23
8995 SPIWrite 04a5,de
8996 SPIWrite 04a6,15
8997 SPIWrite 04a7,0c
8998 SPIWrite 04a8,3b
8999 SPIWrite 04a9,e2
9000 SPIWrite 04aa,16
9001 SPIWrite 04ab,0e
9002 SPIWrite 04ac,4f
9003 SPIWrite 04ad,66
9004 SPIWrite 04ae,17
9005 SPIWrite 04af,0e
9006 SPIWrite 04b0,63
9007 SPIWrite 04b1,ea
9008 SPIWrite 04b2,17
9009 SPIWrite 04b3,11
9010 SPIWrite 04b4,77
9011 SPIWrite 04b5,6e
9012 SPIWrite 04b6,18
9013 SPIWrite 04b7,11
9014 SPIWrite 04b8,8b
9015 SPIWrite 04b9,f2
9016 SPIWrite 04ba,18
9017 SPIWrite 04bb,13
9018 SPIWrite 04bc,9f
9019 SPIWrite 04bd,72
9020 SPIWrite 04be,19
9021 SPIWrite 04bf,15
9022 SPIWrite 04c0,b3
9023 SPIWrite 04c1,f6
9024 SPIWrite 04c2,19
9025 SPIWrite 04c3,16
9026 SPIWrite 04c4,c3
9027 SPIWrite 04c5,76
9028 SPIWrite 04c6,1a
9029 SPIWrite 04c7,18
9030 SPIWrite 04c8,d7
9031 SPIWrite 04c9,f6
9032 SPIWrite 04ca,1a
9033 SPIWrite 04cb,19
9034 SPIWrite 04cc,eb
9035 SPIWrite 04cd,76
9036 SPIWrite 04ce,1b
9037 SPIWrite 04cf,1b
9038 SPIWrite 04d0,ff
9039 SPIWrite 04d1,f6
9040 SPIWrite 04d2,1b
9041 SPIWrite 04d3,1d
9042 SPIWrite 04d4,13
9043 SPIWrite 04d5,77
9044 SPIWrite 04d6,1c
9045 SPIWrite 04d7,1f
9046 SPIWrite 04d8,23
9047 SPIWrite 04d9,f7
9048 SPIWrite 04da,1c
9049 SPIWrite 04db,1f
9050 SPIWrite 04dc,33

9051 SPIWrite 04dd,77
9052 SPIWrite 04de,1d
9053 SPIWrite 04df,1f
9054 SPIWrite 04e0,3f
9055 SPIWrite 04e1,f7
9056 SPIWrite 04e2,1d
9057 SPIWrite 04e3,1f
9058 SPIWrite 04e4,4b
9059 SPIWrite 04e5,77
9060 SPIWrite 04e6,1e
9061 SPIWrite 04e7,1f
9062 SPIWrite 04e8,57
9063 SPIWrite 04e9,f7
9064 SPIWrite 04ea,1e
9065 SPIWrite 04eb,1f
9066 SPIWrite 04ec,5f
9067 SPIWrite 04ed,77
9068 SPIWrite 04ee,1f
9069 SPIWrite 04ef,1f
9070 SPIWrite 04f0,67
9071 SPIWrite 04f1,f7
9072 SPIWrite 04f2,1f
9073 SPIWrite 04f3,1f
9074 SPIWrite 04f4,73
9075 SPIWrite 04f5,f7
9076 SPIWrite 04f6,1f
9077 SPIWrite 04f7,1f
9078 SPIWrite 04f8,7b
9079 SPIWrite 04f9,f7
9080 SPIWrite 04fa,1f
9081 SPIWrite 04fb,1f
9082 SPIWrite 04fc,87
9083 SPIWrite 04fd,f7
9084 SPIWrite 04fe,1f
9085 SPIWrite 04ff,1f
9086 SPIWrite 0500,8f
9087 SPIWrite 0501,f7
9088 SPIWrite 0502,1f
9089 SPIWrite 0503,1f
9090 SPIWrite 0504,97
9091 SPIWrite 0505,f7
9092 SPIWrite 0506,1f
9093 SPIWrite 0507,1f
9094 SPIWrite 0508,9b
9095 SPIWrite 0509,f7
9096 SPIWrite 050a,1f
9097 SPIWrite 050b,1f
9098 SPIWrite 0744,03
9099 SPIWrite 0745,00
9100 SPIWrite 0746,00
9101 SPIWrite 0747,00
9102 SPIWrite 0748,0b
9103 SPIWrite 0749,84
9104 SPIWrite 074a,00
9105 SPIWrite 074b,00
9106 SPIWrite 074c,1f
9107 SPIWrite 074d,08
9108 SPIWrite 074e,01
9109 SPIWrite 074f,00
9110 SPIWrite 0750,33
9111 SPIWrite 0751,8c
9112 SPIWrite 0752,01
9113 SPIWrite 0753,00
9114 SPIWrite 0754,47
9115 SPIWrite 0755,90
9116 SPIWrite 0756,02
9117 SPIWrite 0757,00
9118 SPIWrite 0758,5b
9119 SPIWrite 0759,14

9120 SPIWrite 075a,03
9121 SPIWrite 075b,01
9122 SPIWrite 075c,6f
9123 SPIWrite 075d,18
9124 SPIWrite 075e,04
9125 SPIWrite 075f,01
9126 SPIWrite 0760,83
9127 SPIWrite 0761,9c
9128 SPIWrite 0762,04
9129 SPIWrite 0763,01
9130 SPIWrite 0764,9b
9131 SPIWrite 0765,a0
9132 SPIWrite 0766,05
9133 SPIWrite 0767,02
9134 SPIWrite 0768,b3
9135 SPIWrite 0769,a4
9136 SPIWrite 076a,06
9137 SPIWrite 076b,02
9138 SPIWrite 076c,c7
9139 SPIWrite 076d,a8
9140 SPIWrite 076e,07
9141 SPIWrite 076f,03
9142 SPIWrite 0770,df
9143 SPIWrite 0771,ac
9144 SPIWrite 0772,08
9145 SPIWrite 0773,03
9146 SPIWrite 0774,f7
9147 SPIWrite 0775,b0
9148 SPIWrite 0776,09
9149 SPIWrite 0777,04
9150 SPIWrite 0778,17
9151 SPIWrite 0779,b5
9152 SPIWrite 077a,0a
9153 SPIWrite 077b,04
9154 SPIWrite 077c,37
9155 SPIWrite 077d,b9
9156 SPIWrite 077e,0b
9157 SPIWrite 077f,04
9158 SPIWrite 0780,4f
9159 SPIWrite 0781,bd
9160 SPIWrite 0782,0c
9161 SPIWrite 0783,05
9162 SPIWrite 0784,6b
9163 SPIWrite 0785,c1
9164 SPIWrite 0786,0d
9165 SPIWrite 0787,07
9166 SPIWrite 0788,87
9167 SPIWrite 0789,c5
9168 SPIWrite 078a,0e
9169 SPIWrite 078b,07
9170 SPIWrite 078c,9f
9171 SPIWrite 078d,c9
9172 SPIWrite 078e,0f
9173 SPIWrite 078f,07
9174 SPIWrite 0790,a7
9175 SPIWrite 0791,49
9176 SPIWrite 0792,10
9177 SPIWrite 0793,07
9178 SPIWrite 0794,bb
9179 SPIWrite 0795,4d
9180 SPIWrite 0796,11
9181 SPIWrite 0797,08
9182 SPIWrite 0798,d3
9183 SPIWrite 0799,51
9184 SPIWrite 079a,12
9185 SPIWrite 079b,09
9186 SPIWrite 079c,eb
9187 SPIWrite 079d,55
9188 SPIWrite 079e,13

9189 SPIWrite 079f,0a
9190 SPIWrite 07a0,0b
9191 SPIWrite 07a1,da
9192 SPIWrite 07a2,14
9193 SPIWrite 07a3,0b
9194 SPIWrite 07a4,23
9195 SPIWrite 07a5,de
9196 SPIWrite 07a6,15
9197 SPIWrite 07a7,0c
9198 SPIWrite 07a8,3b
9199 SPIWrite 07a9,e2
9200 SPIWrite 07aa,16
9201 SPIWrite 07ab,0e
9202 SPIWrite 07ac,4f
9203 SPIWrite 07ad,66
9204 SPIWrite 07ae,17
9205 SPIWrite 07af,0e
9206 SPIWrite 07b0,63
9207 SPIWrite 07b1,ea
9208 SPIWrite 07b2,17
9209 SPIWrite 07b3,11
9210 SPIWrite 07b4,77
9211 SPIWrite 07b5,6e
9212 SPIWrite 07b6,18
9213 SPIWrite 07b7,11
9214 SPIWrite 07b8,8b
9215 SPIWrite 07b9,f2
9216 SPIWrite 07ba,18
9217 SPIWrite 07bb,13
9218 SPIWrite 07bc,9f
9219 SPIWrite 07bd,72
9220 SPIWrite 07be,19
9221 SPIWrite 07bf,15
9222 SPIWrite 07c0,b3
9223 SPIWrite 07c1,f6
9224 SPIWrite 07c2,19
9225 SPIWrite 07c3,16
9226 SPIWrite 07c4,c3
9227 SPIWrite 07c5,76
9228 SPIWrite 07c6,1a
9229 SPIWrite 07c7,18
9230 SPIWrite 07c8,d7
9231 SPIWrite 07c9,f6
9232 SPIWrite 07ca,1a
9233 SPIWrite 07cb,19
9234 SPIWrite 07cc,eb
9235 SPIWrite 07cd,76
9236 SPIWrite 07ce,1b
9237 SPIWrite 07cf,1b
9238 SPIWrite 07d0,ff
9239 SPIWrite 07d1,f6
9240 SPIWrite 07d2,1b
9241 SPIWrite 07d3,1d
9242 SPIWrite 07d4,13
9243 SPIWrite 07d5,77
9244 SPIWrite 07d6,1c
9245 SPIWrite 07d7,1f
9246 SPIWrite 07d8,23
9247 SPIWrite 07d9,f7
9248 SPIWrite 07da,1c
9249 SPIWrite 07db,1f
9250 SPIWrite 07dc,33
9251 SPIWrite 07dd,77
9252 SPIWrite 07de,1d
9253 SPIWrite 07df,1f
9254 SPIWrite 07e0,3f
9255 SPIWrite 07e1,f7
9256 SPIWrite 07e2,1d
9257 SPIWrite 07e3,1f

9258 SPIWrite 07e4,4b
9259 SPIWrite 07e5,77
9260 SPIWrite 07e6,1e
9261 SPIWrite 07e7,1f
9262 SPIWrite 07e8,57
9263 SPIWrite 07e9,f7
9264 SPIWrite 07ea,1e
9265 SPIWrite 07eb,1f
9266 SPIWrite 07ec,5f
9267 SPIWrite 07ed,77
9268 SPIWrite 07ee,1f
9269 SPIWrite 07ef,1f
9270 SPIWrite 07f0,67
9271 SPIWrite 07f1,f7
9272 SPIWrite 07f2,1f
9273 SPIWrite 07f3,1f
9274 SPIWrite 07f4,73
9275 SPIWrite 07f5,f7
9276 SPIWrite 07f6,1f
9277 SPIWrite 07f7,1f
9278 SPIWrite 07f8,7b
9279 SPIWrite 07f9,f7
9280 SPIWrite 07fa,1f
9281 SPIWrite 07fb,1f
9282 SPIWrite 07fc,87
9283 SPIWrite 07fd,f7
9284 SPIWrite 07fe,1f
9285 SPIWrite 07ff,1f
9286 SPIWrite 0800,8f
9287 SPIWrite 0801,f7
9288 SPIWrite 0802,1f
9289 SPIWrite 0803,1f
9290 SPIWrite 0804,97
9291 SPIWrite 0805,f7
9292 SPIWrite 0806,1f
9293 SPIWrite 0807,1f
9294 SPIWrite 0808,9b
9295 SPIWrite 0809,f7
9296 SPIWrite 080a,1f
9297 SPIWrite 080b,1f
9298 SPIWrite 0844,03
9299 SPIWrite 0845,00
9300 SPIWrite 0846,00
9301 SPIWrite 0847,00
9302 SPIWrite 0848,0b
9303 SPIWrite 0849,84
9304 SPIWrite 084a,00
9305 SPIWrite 084b,00
9306 SPIWrite 084c,1f
9307 SPIWrite 084d,08
9308 SPIWrite 084e,01
9309 SPIWrite 084f,00
9310 SPIWrite 0850,33
9311 SPIWrite 0851,8c
9312 SPIWrite 0852,01
9313 SPIWrite 0853,00
9314 SPIWrite 0854,47
9315 SPIWrite 0855,90
9316 SPIWrite 0856,02
9317 SPIWrite 0857,00
9318 SPIWrite 0858,5b
9319 SPIWrite 0859,14
9320 SPIWrite 085a,03
9321 SPIWrite 085b,01
9322 SPIWrite 085c,6f
9323 SPIWrite 085d,18
9324 SPIWrite 085e,04
9325 SPIWrite 085f,01
9326 SPIWrite 0860,83

9327 SPIWrite 0861,9c
9328 SPIWrite 0862,04
9329 SPIWrite 0863,01
9330 SPIWrite 0864,9b
9331 SPIWrite 0865,a0
9332 SPIWrite 0866,05
9333 SPIWrite 0867,02
9334 SPIWrite 0868,b3
9335 SPIWrite 0869,a4
9336 SPIWrite 086a,06
9337 SPIWrite 086b,02
9338 SPIWrite 086c,c7
9339 SPIWrite 086d,a8
9340 SPIWrite 086e,07
9341 SPIWrite 086f,03
9342 SPIWrite 0870,df
9343 SPIWrite 0871,ac
9344 SPIWrite 0872,08
9345 SPIWrite 0873,03
9346 SPIWrite 0874,f7
9347 SPIWrite 0875,b0
9348 SPIWrite 0876,09
9349 SPIWrite 0877,04
9350 SPIWrite 0878,17
9351 SPIWrite 0879,b5
9352 SPIWrite 087a,0a
9353 SPIWrite 087b,04
9354 SPIWrite 087c,37
9355 SPIWrite 087d,b9
9356 SPIWrite 087e,0b
9357 SPIWrite 087f,04
9358 SPIWrite 0880,4f
9359 SPIWrite 0881,bd
9360 SPIWrite 0882,0c
9361 SPIWrite 0883,05
9362 SPIWrite 0884,6b
9363 SPIWrite 0885,c1
9364 SPIWrite 0886,0d
9365 SPIWrite 0887,07
9366 SPIWrite 0888,87
9367 SPIWrite 0889,c5
9368 SPIWrite 088a,0e
9369 SPIWrite 088b,07
9370 SPIWrite 088c,9f
9371 SPIWrite 088d,c9
9372 SPIWrite 088e,0f
9373 SPIWrite 088f,07
9374 SPIWrite 0890,a7
9375 SPIWrite 0891,49
9376 SPIWrite 0892,10
9377 SPIWrite 0893,07
9378 SPIWrite 0894,bb
9379 SPIWrite 0895,4d
9380 SPIWrite 0896,11
9381 SPIWrite 0897,08
9382 SPIWrite 0898,d3
9383 SPIWrite 0899,51
9384 SPIWrite 089a,12
9385 SPIWrite 089b,09
9386 SPIWrite 089c,eb
9387 SPIWrite 089d,55
9388 SPIWrite 089e,13
9389 SPIWrite 089f,0a
9390 SPIWrite 08a0,0b
9391 SPIWrite 08a1,da
9392 SPIWrite 08a2,14
9393 SPIWrite 08a3,0b
9394 SPIWrite 08a4,23
9395 SPIWrite 08a5,de

9396 SPIWrite 08a6,15
9397 SPIWrite 08a7,0c
9398 SPIWrite 08a8,3b
9399 SPIWrite 08a9,e2
9400 SPIWrite 08aa,16
9401 SPIWrite 08ab,0e
9402 SPIWrite 08ac,4f
9403 SPIWrite 08ad,66
9404 SPIWrite 08ae,17
9405 SPIWrite 08af,0e
9406 SPIWrite 08b0,63
9407 SPIWrite 08b1,ea
9408 SPIWrite 08b2,17
9409 SPIWrite 08b3,11
9410 SPIWrite 08b4,77
9411 SPIWrite 08b5,6e
9412 SPIWrite 08b6,18
9413 SPIWrite 08b7,11
9414 SPIWrite 08b8,8b
9415 SPIWrite 08b9,f2
9416 SPIWrite 08ba,18
9417 SPIWrite 08bb,13
9418 SPIWrite 08bc,9f
9419 SPIWrite 08bd,72
9420 SPIWrite 08be,19
9421 SPIWrite 08bf,15
9422 SPIWrite 08c0,b3
9423 SPIWrite 08c1,f6
9424 SPIWrite 08c2,19
9425 SPIWrite 08c3,16
9426 SPIWrite 08c4,c3
9427 SPIWrite 08c5,76
9428 SPIWrite 08c6,1a
9429 SPIWrite 08c7,18
9430 SPIWrite 08c8,d7
9431 SPIWrite 08c9,f6
9432 SPIWrite 08ca,1a
9433 SPIWrite 08cb,19
9434 SPIWrite 08cc,eb
9435 SPIWrite 08cd,76
9436 SPIWrite 08ce,1b
9437 SPIWrite 08cf,1b
9438 SPIWrite 08d0,ff
9439 SPIWrite 08d1,f6
9440 SPIWrite 08d2,1b
9441 SPIWrite 08d3,1d
9442 SPIWrite 08d4,13
9443 SPIWrite 08d5,77
9444 SPIWrite 08d6,1c
9445 SPIWrite 08d7,1f
9446 SPIWrite 08d8,23
9447 SPIWrite 08d9,f7
9448 SPIWrite 08da,1c
9449 SPIWrite 08db,1f
9450 SPIWrite 08dc,33
9451 SPIWrite 08dd,77
9452 SPIWrite 08de,1d
9453 SPIWrite 08df,1f
9454 SPIWrite 08e0,3f
9455 SPIWrite 08e1,f7
9456 SPIWrite 08e2,1d
9457 SPIWrite 08e3,1f
9458 SPIWrite 08e4,4b
9459 SPIWrite 08e5,77
9460 SPIWrite 08e6,1e
9461 SPIWrite 08e7,1f
9462 SPIWrite 08e8,57
9463 SPIWrite 08e9,f7
9464 SPIWrite 08ea,1e

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9465 SPIWrite 08eb,1f
9466 SPIWrite 08ec,5f
9467 SPIWrite 08ed,77
9468 SPIWrite 08ee,1f
9469 SPIWrite 08ef,1f
9470 SPIWrite 08f0,67
9471 SPIWrite 08f1,f7
9472 SPIWrite 08f2,1f
9473 SPIWrite 08f3,1f
9474 SPIWrite 08f4,73
9475 SPIWrite 08f5,f7
9476 SPIWrite 08f6,1f
9477 SPIWrite 08f7,1f
9478 SPIWrite 08f8,7b
9479 SPIWrite 08f9,f7
9480 SPIWrite 08fa,1f
9481 SPIWrite 08fb,1f
9482 SPIWrite 08fc,87
9483 SPIWrite 08fd,f7
9484 SPIWrite 08fe,1f
9485 SPIWrite 08ff,1f
9486 SPIWrite 0900,8f
9487 SPIWrite 0901,f7
9488 SPIWrite 0902,1f
9489 SPIWrite 0903,1f
9490 SPIWrite 0904,97
9491 SPIWrite 0905,f7
9492 SPIWrite 0906,1f
9493 SPIWrite 0907,1f
9494 SPIWrite 0908,9b
9495 SPIWrite 0909,f7
9496 SPIWrite 090a,1f
9497 SPIWrite 090b,1f
9498 SPIWrite 00d1,06 //dig_gain_range=0x6; Address(0xd1[7:0])
9499 SPIWrite 0124,01 //spi_agc_dsa_A=0x1; Address(0x124[7:0])
9500 SPIWrite 0124,00 //spi_agc_dsa_A=0x0; Address(0x124[7:0])
9501 SPIWrite 0174,01 //spi_agc_dsa_B=0x1; Address(0x174[7:0])
9502 SPIWrite 0174,00 //spi_agc_dsa_B=0x0; Address(0x174[7:0])
9503 SPIWrite 0013,00 //dsa_page1=0x0; Address(0x13[7:6])
9504 SPIWrite 0013,10 //dsa_page0=0x1; Address(0x13[7:4])
9505 SPIWrite 006c,01 //spi_agc_dsa_fb=0x1; Address(0x6c[7:0])
9506 SPIWrite 006c,00 //spi_agc_dsa_fb=0x0; Address(0x6c[7:0])
9507 SPIWrite 0013,00 //dsa_page0=0x0; Address(0x13[7:4])
9508 SPIWrite 0013,80 //dsa_page1=0x2; Address(0x13[7:6])
9509 SPIWrite 00d1,06 //dig_gain_range=0x6; Address(0xd1[7:0])
9510 SPIWrite 0124,01 //spi_agc_dsa_A=0x1; Address(0x124[7:0])
9511 SPIWrite 0124,00 //spi_agc_dsa_A=0x0; Address(0x124[7:0])
9512 SPIWrite 0174,01 //spi_agc_dsa_B=0x1; Address(0x174[7:0])
9513 SPIWrite 0174,00 //spi_agc_dsa_B=0x0; Address(0x174[7:0])
9514 SPIWrite 0013,00 //dsa_page1=0x0; Address(0x13[7:6])
9515 SPIWrite 0013,20 //dsa_page0=0x2; Address(0x13[7:4])
9516 SPIWrite 006c,01 //spi_agc_dsa_fb=0x1; Address(0x6c[7:0])
9517 SPIWrite 006c,00 //spi_agc_dsa_fb=0x0; Address(0x6c[7:0])
9518 SPIWrite 0013,00 //dsa_page0=0x0; Address(0x13[7:4])
9519 SPIWrite 0015,40 //digtop=0x1; Address(0x15[7:6])
9520 SPIWrite 0940,00 //disable_pkdet_regs_ab=0x0; Address(0x940[7:0])
9521 SPIWrite 0941,00 //disable_pkdet_regs_cd=0x0; Address(0x941[7:0])
9522 SPIWrite 0015,00 //digtop=0x0; Address(0x15[7:6])
9523 SPIWrite 0013,c0 //dsa_page1=0x3; Address(0x13[7:6])
9524 SPIWrite 00d1,03 //dig_gain_range=0x3; Address(0xd1[7:0])
9525 SPIWrite 0545,06 //tm_rel_index_step=0x6; Address(0x545[7:0])
9526 SPIWrite 054a,06 //tm_rel_cust_diff=0x6; Address(0x54a[7:0])
9527 SPIWrite 05a4,2c //tm_pkdet_index_limit=0x2c; Address(0x5a4[7:0])
9528 SPIWrite 05a5,18 //tm_pkdet_index_add=0x18; Address(0x5a5[7:0])
9529 SPIWrite 0577,00 //tm_rel_en_exit_decay=0x0; Address(0x577[7:0])
9530 SPIWrite 056f,01 //tm_rel_en_exit_count=0x1; Address(0x56f[7:0])
9531 SPIWrite 05a1,00 //tm_rel_use_cust_pkdet=0x0; Address(0x5a1[7:0])
9532 SPIWrite 0013,00 //dsa_page1=0x0; Address(0x13[7:6])
9533

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9534 //STEP: topConfig/step2
9535 SPIWrite 0013,10 //dsa_page0=0x1; Address(0x13[7:4])
9536 SPIWrite 00d0,18 //txa_dsa_dig0_gain=0x18; Address(0xd0[7:0],0xd1[7:0])
9537 SPIWrite 00d4,18 //txb_dsa_dig0_gain=0x18; Address(0xd4[7:0],0xd5[7:0])
9538 SPIWrite 0013,20 //dsa_page0=0x2; Address(0x13[7:4])
9539 SPIWrite 00d0,18 //txa_dsa_dig0_gain=0x18; Address(0xd0[7:0],0xd1[7:0])
9540 SPIWrite 00d4,18 //txb_dsa_dig0_gain=0x18; Address(0xd4[7:0],0xd5[7:0])
9541 SPIWrite 0013,00 //dsa_page0=0x0; Address(0x13[7:4])
9542 SPIWrite 0013,c0 //dsa_page1=0x3; Address(0x13[7:6])
9543 SPIWrite 0a37,40
9544 SPIWrite 0a3f,40
9545 SPIWrite 0a4f,40
9546 SPIWrite 0a5f,40
9547 SPIWrite 0a77,40
9548 SPIWrite 0a7f,40
9549 SPIWrite 0a97,40
9550 SPIWrite 0a9f,40
9551 SPIWrite 0aa7,40
9552 SPIWrite 0aaf,40
9553 SPIWrite 0c37,40
9554 SPIWrite 0c3f,40
9555 SPIWrite 0c4f,40
9556 SPIWrite 0c5f,40
9557 SPIWrite 0c77,40
9558 SPIWrite 0c7f,40
9559 SPIWrite 0c97,40
9560 SPIWrite 0c9f,40
9561 SPIWrite 0ca7,40
9562 SPIWrite 0caf,40
9563 SPIWrite 0013,00 //dsa_page1=0x0; Address(0x13[7:6])
9564
9565 //STEP: sysConfig/step0
9566
9567 //START: Configuring RRF Mode to TOP MCU
9568
9569 SPIWrite 0018,20 //macro=0x1; Address(0x18[7:5])
9570 SPIRead 00f0
9571
9572 //Read MACRO_READY=0x1; Address(0xf0[7:0])
9573
9574
9575 SPIPoll 00f0,0,0,1
9576
9577 SPIWrite 00a3,00 //MACRO_OPERAND_REG0=0x3;
Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
9578 SPIWrite 00a2,00
9579 SPIWrite 00a1,00
9580 SPIWrite 00a0,03
9581 SPIWrite 0193,22 //MACRO_OPCODE=0x22; Address(0x193[7:0],0x194[7:0])
9582
9583 WAIT 0.001
9584 SPIRead 00f0
9585
9586 //Read MACRO_DONE=0x1; Address(0xf0[7:2])
9587
9588
9589 SPIPoll 00f0,2,2,4
9590
9591 SPIRead 00f0
9592
9593 //Read MACRO_ERROR=0x0; Address(0xf0[7:3])
9594
9595 SPIRead 00f1
9596
9597 //Read MACRO_ERROR_OPCODE=0x0; Address(0xf1[7:0],0xf2[7:0])
9598
9599 SPIRead 00f0
9600
9601 //Read MACRO_ERROR_IN_OPCODE=0x0; Address(0xf0[7:4])

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9602
9603 SPIRead 00f0
9604
9605 //Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;      Address(0xf0[7:5])
9606
9607 SPIRead 00f0
9608
9609 //Read  MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])
9610
9611 SPIRead 00f0
9612
9613 //Read  MACRO_ERROR_IN_EXECUTION=0x0;      Address(0xf0[7:7])
9614
9615 SPIRead 00f3
9616 SPIRead 00f2
9617
9618 //Read  MACRO_ERROR_EXTENDED_CODE=0x0;      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
9619
9620 SPIRead 00f7
9621 SPIRead 00f6
9622 SPIRead 00f5
9623 SPIRead 00f4
9624
9625 //Read  MACRO_ERROR_EXTENDED_CODE_2=0x0;
Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
9626
9627 SPIRead 00f0
9628
9629 //Read  MACRO_READY=0x1;      Address(0xf0[7:0])
9630
9631
9632 SPIPoll 00f0,0,0,1
9633
9634 SPIWrite 00a3,00      //MACRO_OPERAND_REG0=0xf010f;
Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
9635 SPIWrite 00a2,0f
9636 SPIWrite 00a1,01
9637 SPIWrite 00a0,0f
9638 SPIWrite 0193,21      //MACRO_OPCODE=0x21;      Address(0x193[7:0],0x194[7:0])
9639
9640 WAIT 0.001
9641 SPIRead 00f0
9642
9643 //Read  MACRO_DONE=0x1;      Address(0xf0[7:2])
9644
9645
9646 SPIPoll 00f0,2,2,4
9647
9648 SPIRead 00f0
9649
9650 //Read  MACRO_ERROR=0x0;      Address(0xf0[7:3])
9651
9652 SPIRead 00f1
9653
9654 //Read  MACRO_ERROR_OPCODE=0x0;      Address(0xf1[7:0],0xf2[7:0])
9655
9656 SPIRead 00f0
9657
9658 //Read  MACRO_ERROR_IN_OPCODE=0x0;      Address(0xf0[7:4])
9659
9660 SPIRead 00f0
9661
9662 //Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;      Address(0xf0[7:5])
9663
9664 SPIRead 00f0
9665
9666 //Read  MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])
9667
9668 SPIRead 00f0
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9669
9670 //Read  MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])
9671
9672 SPIRead 00f3
9673 SPIRead 00f2
9674
9675 //Read  MACRO_ERROR_EXTENDED_CODE=0x0;    Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
9676
9677 SPIRead 00f7
9678 SPIRead 00f6
9679 SPIRead 00f5
9680 SPIRead 00f4
9681
9682 //Read  MACRO_ERROR_EXTENDED_CODE_2=0x0;
Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
9683
9684 SPIRead 00f0
9685
9686 //Read  MACRO_READY=0x1;    Address(0xf0[7:0])
9687
9688
9689 SPIPoll 00f0,0,0,1
9690
9691 SPIWrite 00a3,00    //MACRO_OPERAND_REG0=0x0;
Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
9692 SPIWrite 00a2,00
9693 SPIWrite 00a1,00
9694 SPIWrite 00a0,00
9695 SPIWrite 0193,2f    //MACRO_OPCODE=0x2f;    Address(0x193[7:0],0x194[7:0])
9696
9697 WAIT 0.001
9698 SPIRead 00f0
9699
9700 //Read  MACRO_DONE=0x1;    Address(0xf0[7:2])
9701
9702
9703 SPIPoll 00f0,2,2,4
9704
9705 SPIRead 00f0
9706
9707 //Read  MACRO_ERROR=0x0;    Address(0xf0[7:3])
9708
9709 SPIRead 00f1
9710
9711 //Read  MACRO_ERROR_OPCODE=0x0;    Address(0xf1[7:0],0xf2[7:0])
9712
9713 SPIRead 00f0
9714
9715 //Read  MACRO_ERROR_IN_OPCODE=0x0;    Address(0xf0[7:4])
9716
9717 SPIRead 00f0
9718
9719 //Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;    Address(0xf0[7:5])
9720
9721 SPIRead 00f0
9722
9723 //Read  MACRO_ERROR_IN_OPERAND=0x0;    Address(0xf0[7:6])
9724
9725 SPIRead 00f0
9726
9727 //Read  MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])
9728
9729 SPIRead 00f3
9730 SPIRead 00f2
9731
9732 //Read  MACRO_ERROR_EXTENDED_CODE=0x0;    Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
9733
9734 SPIRead 00f7
9735 SPIRead 00f6
```

```
9736 SPIRead 00f5
9737 SPIRead 00f4
9738
9739 //Read MACRO_ERROR_EXTENDED_CODE_2=0x0;
Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

9740
9741
9742 //END: Configuring RRF Mode to TOP MCU
9743
9744 SPIWrite 0018,00 //macro=0x0; Address(0x18[7:5])
9745
9746 //STEP: sysConfig/step1
9747
9748 //START: Configuring RX Chain Parameters to TOP MCU
9749
9750 SPIWrite 0018,20 //macro=0x1; Address(0x18[7:5])
9751 SPIRead 00f0
9752
9753 //Read MACRO_READY=0x1; Address(0xf0[7:0])
9754
9755
9756 SPIPoll 00f0,0,0,1
9757
9758 SPIWrite 00a3,00 //MACRO_OPERAND_REG0=0x703;
Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
9759 SPIWrite 00a2,00
9760 SPIWrite 00a1,07
9761 SPIWrite 00a0,03
9762 SPIWrite 0193,2c //MACRO_OPCODE=0x2c; Address(0x193[7:0],0x194[7:0])
9763
9764 WAIT 0.001
9765 SPIRead 00f0
9766
9767 //Read MACRO_DONE=0x1; Address(0xf0[7:2])
9768
9769
9770 SPIPoll 00f0,2,2,4
9771
9772 SPIRead 00f0
9773
9774 //Read MACRO_ERROR=0x0; Address(0xf0[7:3])
9775
9776 SPIRead 00f1
9777
9778 //Read MACRO_ERROR_OPCODE=0x0; Address(0xf1[7:0],0xf2[7:0])
9779
9780 SPIRead 00f0
9781
9782 //Read MACRO_ERROR_IN_OPCODE=0x0; Address(0xf0[7:4])
9783
9784 SPIRead 00f0
9785
9786 //Read MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0; Address(0xf0[7:5])
9787
9788 SPIRead 00f0
9789
9790 //Read MACRO_ERROR_IN_OPERAND=0x0; Address(0xf0[7:6])
9791
9792 SPIRead 00f0
9793
9794 //Read MACRO_ERROR_IN_EXECUTION=0x0; Address(0xf0[7:7])
9795
9796 SPIRead 00f3
9797 SPIRead 00f2
9798
9799 //Read MACRO_ERROR_EXTENDED_CODE=0x0; Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
9800
9801 SPIRead 00f7
9802 SPIRead 00f6
```

```

9803 SPIRead 00f5
9804 SPIRead 00f4
9805
9806 //Read MACRO_ERROR_EXTENDED_CODE_2=0x0;
Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
9807
9808 SPIRead 00f0
9809
9810 //Read MACRO_READY=0x1; Address(0xf0[7:0])
9811
9812
9813 SPIPoll 00f0,0,0,1
9814
9815 SPIWrite 00a3,00 //MACRO_OPERAND_REG0=0x301;
Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
9816 SPIWrite 00a2,00
9817 SPIWrite 00a1,03
9818 SPIWrite 00a0,01
9819 SPIWrite 0193,29 //MACRO_OPCODE=0x29; Address(0x193[7:0],0x194[7:0])
9820
9821 WAIT 0.001
9822 SPIRead 00f0
9823
9824 //Read MACRO_DONE=0x1; Address(0xf0[7:2])
9825
9826
9827 SPIPoll 00f0,2,2,4
9828
9829 SPIRead 00f0
9830
9831 //Read MACRO_ERROR=0x0; Address(0xf0[7:3])
9832
9833 SPIRead 00f1
9834
9835 //Read MACRO_ERROR_OPCODE=0x0; Address(0xf1[7:0],0xf2[7:0])
9836
9837 SPIRead 00f0
9838
9839 //Read MACRO_ERROR_IN_OPCODE=0x0; Address(0xf0[7:4])
9840
9841 SPIRead 00f0
9842
9843 //Read MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0; Address(0xf0[7:5])
9844
9845 SPIRead 00f0
9846
9847 //Read MACRO_ERROR_IN_OPERAND=0x0; Address(0xf0[7:6])
9848
9849 SPIRead 00f0
9850
9851 //Read MACRO_ERROR_IN_EXECUTION=0x0; Address(0xf0[7:7])
9852
9853 SPIRead 00f3
9854 SPIRead 00f2
9855
9856 //Read MACRO_ERROR_EXTENDED_CODE=0x0; Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
9857
9858 SPIRead 00f7
9859 SPIRead 00f6
9860 SPIRead 00f5
9861 SPIRead 00f4
9862
9863 //Read MACRO_ERROR_EXTENDED_CODE_2=0x0;
Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
9864
9865 SPIRead 00f0
9866
9867 //Read MACRO_READY=0x1; Address(0xf0[7:0])
9868

```



```

9869
9870 SPIPoll 00f0,0,0,1
9871
9872 SPIWrite 00a3,00 //MACRO_OPERAND_REG0=0x101;
Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
9873 SPIWrite 00a2,00
9874 SPIWrite 00a1,01
9875 SPIWrite 00a0,01
9876 SPIWrite 0193,23 //MACRO_OPCODE=0x23; Address(0x193[7:0],0x194[7:0])
9877
9878 WAIT 0.001
9879 SPIRead 00f0
9880
9881 //Read MACRO_DONE=0x1; Address(0xf0[7:2])
9882
9883
9884 SPIPoll 00f0,2,2,4
9885
9886 SPIRead 00f0
9887
9888 //Read MACRO_ERROR=0x0; Address(0xf0[7:3])
9889
9890 SPIRead 00f1
9891
9892 //Read MACRO_ERROR_OPCODE=0x0; Address(0xf1[7:0],0xf2[7:0])
9893
9894 SPIRead 00f0
9895
9896 //Read MACRO_ERROR_IN_OPCODE=0x0; Address(0xf0[7:4])
9897
9898 SPIRead 00f0
9899
9900 //Read MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0; Address(0xf0[7:5])
9901
9902 SPIRead 00f0
9903
9904 //Read MACRO_ERROR_IN_OPERAND=0x0; Address(0xf0[7:6])
9905
9906 SPIRead 00f0
9907
9908 //Read MACRO_ERROR_IN_EXECUTION=0x0; Address(0xf0[7:7])
9909
9910 SPIRead 00f3
9911 SPIRead 00f2
9912
9913 //Read MACRO_ERROR_EXTENDED_CODE=0x0; Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
9914
9915 SPIRead 00f7
9916 SPIRead 00f6
9917 SPIRead 00f5
9918 SPIRead 00f4
9919
9920 //Read MACRO_ERROR_EXTENDED_CODE_2=0x0;
Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
9921
9922 SPIRead 00f0
9923
9924 //Read MACRO_READY=0x1; Address(0xf0[7:0])
9925
9926
9927 SPIPoll 00f0,0,0,1
9928
9929 SPIWrite 00a3,77 //MACRO_OPERAND_REG0=0x77400001;
Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
9930 SPIWrite 00a2,40
9931 SPIWrite 00a1,00
9932 SPIWrite 00a0,01
9933 SPIWrite 00a7,ac //MACRO_OPERAND_REG1=0xac40001b;
Address(0xa4[7:0],0xa5[7:0],0xa6[7:0],0xa7[7:0],0xa8[7:0])

```

```

9934 SPIWrite 00a6,40
9935 SPIWrite 00a5,00
9936 SPIWrite 00a4,1b
9937 SPIWrite 00ab,77 //MACRO_OPERAND_REG2=0x77400027;
Address(0xa8[7:0],0xa9[7:0],0xaa[7:0],0xab[7:0],0xac[7:0])
9938 SPIWrite 00aa,40
9939 SPIWrite 00a9,00
9940 SPIWrite 00a8,27
9941 SPIWrite 00af,ac //MACRO_OPERAND_REG3=0xac40001b;
Address(0xac[7:0],0xad[7:0],0xae[7:0],0xaf[7:0],0xb0[7:0])
9942 SPIWrite 00ae,40
9943 SPIWrite 00ad,00
9944 SPIWrite 00ac,1b
9945 SPIWrite 00b3,00 //MACRO_OPERAND_REG4=0x27;
Address(0xb0[7:0],0xb1[7:0],0xb2[7:0],0xb3[7:0],0xb4[7:0])
9946 SPIWrite 00b2,00
9947 SPIWrite 00b1,00
9948 SPIWrite 00b0,27
9949 SPIWrite 0193,31 //MACRO_OPCODE=0x31; Address(0x193[7:0],0x194[7:0])
9950
9951 WAIT 0.001
9952 SPIRead 00f0
9953
9954 //Read MACRO_DONE=0x1; Address(0xf0[7:2])
9955
9956
9957 SPIPoll 00f0,2,2,4
9958
9959 SPIRead 00f0
9960
9961 //Read MACRO_ERROR=0x0; Address(0xf0[7:3])
9962
9963 SPIRead 00f1
9964
9965 //Read MACRO_ERROR_OPCODE=0x0; Address(0xf1[7:0],0xf2[7:0])
9966
9967 SPIRead 00f0
9968
9969 //Read MACRO_ERROR_IN_OPCODE=0x0; Address(0xf0[7:4])
9970
9971 SPIRead 00f0
9972
9973 //Read MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0; Address(0xf0[7:5])
9974
9975 SPIRead 00f0
9976
9977 //Read MACRO_ERROR_IN_OPERAND=0x0; Address(0xf0[7:6])
9978
9979 SPIRead 00f0
9980
9981 //Read MACRO_ERROR_IN_EXECUTION=0x0; Address(0xf0[7:7])
9982
9983 SPIRead 00f3
9984 SPIRead 00f2
9985
9986 //Read MACRO_ERROR_EXTENDED_CODE=0x0; Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
9987
9988 SPIRead 00f7
9989 SPIRead 00f6
9990 SPIRead 00f5
9991 SPIRead 00f4
9992
9993 //Read MACRO_ERROR_EXTENDED_CODE_2=0x0;
Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
9994
9995 SPIRead 00f0
9996
9997 //Read MACRO_READY=0x1; Address(0xf0[7:0])
9998

```

```

9999
10000 SPIPoll 00f0,0,0,1
10001
10002 SPIWrite 00a3,00 //MACRO_OPERAND_REG0=0x302;
Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
10003 SPIWrite 00a2,00
10004 SPIWrite 00a1,03
10005 SPIWrite 00a0,02
10006 SPIWrite 0193,29 //MACRO_OPCODE=0x29; Address(0x193[7:0],0x194[7:0])
10007
10008 WAIT 0.001
10009 SPIRead 00f0
10010
10011 //Read MACRO_DONE=0x1; Address(0xf0[7:2])
10012
10013
10014 SPIPoll 00f0,2,2,4
10015
10016 SPIRead 00f0
10017
10018 //Read MACRO_ERROR=0x0; Address(0xf0[7:3])
10019
10020 SPIRead 00f1
10021
10022 //Read MACRO_ERROR_OPCODE=0x0; Address(0xf1[7:0],0xf2[7:0])
10023
10024 SPIRead 00f0
10025
10026 //Read MACRO_ERROR_IN_OPCODE=0x0; Address(0xf0[7:4])
10027
10028 SPIRead 00f0
10029
10030 //Read MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0; Address(0xf0[7:5])
10031
10032 SPIRead 00f0
10033
10034 //Read MACRO_ERROR_IN_OPERAND=0x0; Address(0xf0[7:6])
10035
10036 SPIRead 00f0
10037
10038 //Read MACRO_ERROR_IN_EXECUTION=0x0; Address(0xf0[7:7])
10039
10040 SPIRead 00f3
10041 SPIRead 00f2
10042
10043 //Read MACRO_ERROR_EXTENDED_CODE=0x0; Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
10044
10045 SPIRead 00f7
10046 SPIRead 00f6
10047 SPIRead 00f5
10048 SPIRead 00f4
10049
10050 //Read MACRO_ERROR_EXTENDED_CODE_2=0x0;
Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
10051
10052 SPIRead 00f0
10053
10054 //Read MACRO_READY=0x1; Address(0xf0[7:0])
10055
10056
10057 SPIPoll 00f0,0,0,1
10058
10059 SPIWrite 00a3,00 //MACRO_OPERAND_REG0=0x102;
Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
10060 SPIWrite 00a2,00
10061 SPIWrite 00a1,01
10062 SPIWrite 00a0,02
10063 SPIWrite 0193,23 //MACRO_OPCODE=0x23; Address(0x193[7:0],0x194[7:0])
10064

```

```
10065 WAIT 0.001
10066 SPIRead 00f0
10067
10068 //Read MACRO_DONE=0x1; Address(0xf0[7:2])
10069
10070
10071 SPIPoll 00f0,2,2,4
10072
10073 SPIRead 00f0
10074
10075 //Read MACRO_ERROR=0x0; Address(0xf0[7:3])
10076
10077 SPIRead 00f1
10078
10079 //Read MACRO_ERROR_OPCODE=0x0; Address(0xf1[7:0],0xf2[7:0])
10080
10081 SPIRead 00f0
10082
10083 //Read MACRO_ERROR_IN_OPCODE=0x0; Address(0xf0[7:4])
10084
10085 SPIRead 00f0
10086
10087 //Read MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0; Address(0xf0[7:5])
10088
10089 SPIRead 00f0
10090
10091 //Read MACRO_ERROR_IN_OPERAND=0x0; Address(0xf0[7:6])
10092
10093 SPIRead 00f0
10094
10095 //Read MACRO_ERROR_IN_EXECUTION=0x0; Address(0xf0[7:7])
10096
10097 SPIRead 00f3
10098 SPIRead 00f2
10099
10100 //Read MACRO_ERROR_EXTENDED_CODE=0x0; Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
10101
10102 SPIRead 00f7
10103 SPIRead 00f6
10104 SPIRead 00f5
10105 SPIRead 00f4
10106
10107 //Read MACRO_ERROR_EXTENDED_CODE_2=0x0;
Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
10108
10109 SPIRead 00f0
10110
10111 //Read MACRO_READY=0x1; Address(0xf0[7:0])
10112
10113
10114 SPIPoll 00f0,0,0,1
10115
10116 SPIWrite 00a3,77 //MACRO_OPERAND_REG0=0x77400002;
Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
10117 SPIWrite 00a2,40
10118 SPIWrite 00a1,00
10119 SPIWrite 00a0,02
10120 SPIWrite 00a7,ac //MACRO_OPERAND_REG1=0xac40001b;
Address(0xa4[7:0],0xa5[7:0],0xa6[7:0],0xa7[7:0],0xa8[7:0])
10121 SPIWrite 00a6,40
10122 SPIWrite 00a5,00
10123 SPIWrite 00a4,1b
10124 SPIWrite 00ab,77 //MACRO_OPERAND_REG2=0x77400027;
Address(0xa8[7:0],0xa9[7:0],0xaa[7:0],0xab[7:0],0xac[7:0])
10125 SPIWrite 00aa,40
10126 SPIWrite 00a9,00
10127 SPIWrite 00a8,27
10128 SPIWrite 00af,ac //MACRO_OPERAND_REG3=0xac40001b;
Address(0xac[7:0],0xad[7:0],0xae[7:0],0xaf[7:0],0xb0[7:0])
```

```

10129 SPIWrite 00ae,40
10130 SPIWrite 00ad,00
10131 SPIWrite 00ac,1b
10132 SPIWrite 00b3,00 //MACRO_OPERAND_REG4=0x27;
Address(0xb0[7:0],0xb1[7:0],0xb2[7:0],0xb3[7:0],0xb4[7:0])
10133 SPIWrite 00b2,00
10134 SPIWrite 00b1,00
10135 SPIWrite 00b0,27
10136 SPIWrite 0193,31 //MACRO_OPCODE=0x31; Address(0x193[7:0],0x194[7:0])
10137
10138 WAIT 0.001
10139 SPIRead 00f0
10140
10141 //Read MACRO_DONE=0x1; Address(0xf0[7:2])
10142
10143
10144 SPIPoll 00f0,2,2,4
10145
10146 SPIRead 00f0
10147
10148 //Read MACRO_ERROR=0x0; Address(0xf0[7:3])
10149
10150 SPIRead 00f1
10151
10152 //Read MACRO_ERROR_OPCODE=0x0; Address(0xf1[7:0],0xf2[7:0])
10153
10154 SPIRead 00f0
10155
10156 //Read MACRO_ERROR_IN_OPCODE=0x0; Address(0xf0[7:4])
10157
10158 SPIRead 00f0
10159
10160 //Read MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0; Address(0xf0[7:5])
10161
10162 SPIRead 00f0
10163
10164 //Read MACRO_ERROR_IN_OPERAND=0x0; Address(0xf0[7:6])
10165
10166 SPIRead 00f0
10167
10168 //Read MACRO_ERROR_IN_EXECUTION=0x0; Address(0xf0[7:7])
10169
10170 SPIRead 00f3
10171 SPIRead 00f2
10172
10173 //Read MACRO_ERROR_EXTENDED_CODE=0x0; Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
10174
10175 SPIRead 00f7
10176 SPIRead 00f6
10177 SPIRead 00f5
10178 SPIRead 00f4
10179
10180 //Read MACRO_ERROR_EXTENDED_CODE_2=0x0;
Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
10181
10182 SPIRead 00f0
10183
10184 //Read MACRO_READY=0x1; Address(0xf0[7:0])
10185
10186
10187 SPIPoll 00f0,0,0,1
10188
10189 SPIWrite 00a3,00 //MACRO_OPERAND_REG0=0x304;
Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
10190 SPIWrite 00a2,00
10191 SPIWrite 00a1,03
10192 SPIWrite 00a0,04
10193 SPIWrite 0193,29 //MACRO_OPCODE=0x29; Address(0x193[7:0],0x194[7:0])
10194

```

```
10195 WAIT 0.001
10196 SPIRead 00f0
10197
10198 //Read MACRO_DONE=0x1; Address(0xf0[7:2])
10199
10200
10201 SPIPoll 00f0,2,2,4
10202
10203 SPIRead 00f0
10204
10205 //Read MACRO_ERROR=0x0; Address(0xf0[7:3])
10206
10207 SPIRead 00f1
10208
10209 //Read MACRO_ERROR_OPCODE=0x0; Address(0xf1[7:0],0xf2[7:0])
10210
10211 SPIRead 00f0
10212
10213 //Read MACRO_ERROR_IN_OPCODE=0x0; Address(0xf0[7:4])
10214
10215 SPIRead 00f0
10216
10217 //Read MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0; Address(0xf0[7:5])
10218
10219 SPIRead 00f0
10220
10221 //Read MACRO_ERROR_IN_OPERAND=0x0; Address(0xf0[7:6])
10222
10223 SPIRead 00f0
10224
10225 //Read MACRO_ERROR_IN_EXECUTION=0x0; Address(0xf0[7:7])
10226
10227 SPIRead 00f3
10228 SPIRead 00f2
10229
10230 //Read MACRO_ERROR_EXTENDED_CODE=0x0; Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
10231
10232 SPIRead 00f7
10233 SPIRead 00f6
10234 SPIRead 00f5
10235 SPIRead 00f4
10236
10237 //Read MACRO_ERROR_EXTENDED_CODE_2=0x0;
Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
10238
10239 SPIRead 00f0
10240
10241 //Read MACRO_READY=0x1; Address(0xf0[7:0])
10242
10243
10244 SPIPoll 00f0,0,0,1
10245
10246 SPIWrite 00a3,00 //MACRO_OPERAND_REG0=0x104;
Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
10247 SPIWrite 00a2,00
10248 SPIWrite 00a1,01
10249 SPIWrite 00a0,04
10250 SPIWrite 0193,23 //MACRO_OPCODE=0x23; Address(0x193[7:0],0x194[7:0])
10251
10252 WAIT 0.001
10253 SPIRead 00f0
10254
10255 //Read MACRO_DONE=0x1; Address(0xf0[7:2])
10256
10257
10258 SPIPoll 00f0,2,2,4
10259
10260 SPIRead 00f0
10261
```

```

10262 //Read  MACRO_ERROR=0x0;      Address(0xf0[7:3])
10263
10264 SPIRead 00f1
10265
10266 //Read  MACRO_ERROR_OPCODE=0x0;      Address(0xf1[7:0],0xf2[7:0])
10267
10268 SPIRead 00f0
10269
10270 //Read  MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])
10271
10272 SPIRead 00f0
10273
10274 //Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;      Address(0xf0[7:5])
10275
10276 SPIRead 00f0
10277
10278 //Read  MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])
10279
10280 SPIRead 00f0
10281
10282 //Read  MACRO_ERROR_IN_EXECUTION=0x0;  Address(0xf0[7:7])
10283
10284 SPIRead 00f3
10285 SPIRead 00f2
10286
10287 //Read  MACRO_ERROR_EXTENDED_CODE=0x0;  Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
10288
10289 SPIRead 00f7
10290 SPIRead 00f6
10291 SPIRead 00f5
10292 SPIRead 00f4
10293
10294 //Read  MACRO_ERROR_EXTENDED_CODE_2=0x0;
Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
10295
10296 SPIRead 00f0
10297
10298 //Read  MACRO_READY=0x1;      Address(0xf0[7:0])
10299
10300
10301 SPIPoll 00f0,0,0,1
10302
10303 SPIWrite 00a3,77 //MACRO_OPERAND_REG0=0x77400004;
Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
10304 SPIWrite 00a2,40
10305 SPIWrite 00a1,00
10306 SPIWrite 00a0,04
10307 SPIWrite 00a7,ac //MACRO_OPERAND_REG1=0xac40001b;
Address(0xa4[7:0],0xa5[7:0],0xa6[7:0],0xa7[7:0],0xa8[7:0])
10308 SPIWrite 00a6,40
10309 SPIWrite 00a5,00
10310 SPIWrite 00a4,1b
10311 SPIWrite 00ab,77 //MACRO_OPERAND_REG2=0x77400027;
Address(0xa8[7:0],0xa9[7:0],0xaa[7:0],0xab[7:0],0xac[7:0])
10312 SPIWrite 00aa,40
10313 SPIWrite 00a9,00
10314 SPIWrite 00a8,27
10315 SPIWrite 00af,ac //MACRO_OPERAND_REG3=0xac40001b;
Address(0xac[7:0],0xad[7:0],0xae[7:0],0xaf[7:0],0xb0[7:0])
10316 SPIWrite 00ae,40
10317 SPIWrite 00ad,00
10318 SPIWrite 00ac,1b
10319 SPIWrite 00b3,00 //MACRO_OPERAND_REG4=0x27;
Address(0xb0[7:0],0xb1[7:0],0xb2[7:0],0xb3[7:0],0xb4[7:0])
10320 SPIWrite 00b2,00
10321 SPIWrite 00b1,00
10322 SPIWrite 00b0,27
10323 SPIWrite 0193,31 //MACRO_OPCODE=0x31;      Address(0x193[7:0],0x194[7:0])
10324

```

```
10325 WAIT 0.001
10326 SPIRead 00f0
10327
10328 //Read MACRO_DONE=0x1;      Address(0xf0[7:2])
10329
10330
10331 SPIPoll 00f0,2,2,4
10332
10333 SPIRead 00f0
10334
10335 //Read MACRO_ERROR=0x0;      Address(0xf0[7:3])
10336
10337 SPIRead 00f1
10338
10339 //Read MACRO_ERROR_OPCODE=0x0;      Address(0xf1[7:0],0xf2[7:0])
10340
10341 SPIRead 00f0
10342
10343 //Read MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])
10344
10345 SPIRead 00f0
10346
10347 //Read MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;      Address(0xf0[7:5])
10348
10349 SPIRead 00f0
10350
10351 //Read MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])
10352
10353 SPIRead 00f0
10354
10355 //Read MACRO_ERROR_IN_EXECUTION=0x0;  Address(0xf0[7:7])
10356
10357 SPIRead 00f3
10358 SPIRead 00f2
10359
10360 //Read MACRO_ERROR_EXTENDED_CODE=0x0;  Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
10361
10362 SPIRead 00f7
10363 SPIRead 00f6
10364 SPIRead 00f5
10365 SPIRead 00f4
10366
10367 //Read MACRO_ERROR_EXTENDED_CODE_2=0x0;
Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
10368
10369 SPIRead 00f0
10370
10371 //Read MACRO_READY=0x1;      Address(0xf0[7:0])
10372
10373
10374 SPIPoll 00f0,0,0,1
10375
10376 SPIWrite 00a3,00      //MACRO_OPERAND_REG0=0x308;
Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
10377 SPIWrite 00a2,00
10378 SPIWrite 00a1,03
10379 SPIWrite 00a0,08
10380 SPIWrite 0193,29      //MACRO_OPCODE=0x29;      Address(0x193[7:0],0x194[7:0])
10381
10382 WAIT 0.001
10383 SPIRead 00f0
10384
10385 //Read MACRO_DONE=0x1;      Address(0xf0[7:2])
10386
10387
10388 SPIPoll 00f0,2,2,4
10389
10390 SPIRead 00f0
10391
```



```
10392 //Read MACRO_ERROR=0x0; Address(0xf0[7:3])
10393
10394 SPIRead 00f1
10395
10396 //Read MACRO_ERROR_OPCODE=0x0; Address(0xf1[7:0],0xf2[7:0])
10397
10398 SPIRead 00f0
10399
10400 //Read MACRO_ERROR_IN_OPCODE=0x0; Address(0xf0[7:4])
10401
10402 SPIRead 00f0
10403
10404 //Read MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0; Address(0xf0[7:5])
10405
10406 SPIRead 00f0
10407
10408 //Read MACRO_ERROR_IN_OPERAND=0x0; Address(0xf0[7:6])
10409
10410 SPIRead 00f0
10411
10412 //Read MACRO_ERROR_IN_EXECUTION=0x0; Address(0xf0[7:7])
10413
10414 SPIRead 00f3
10415 SPIRead 00f2
10416
10417 //Read MACRO_ERROR_EXTENDED_CODE=0x0; Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
10418
10419 SPIRead 00f7
10420 SPIRead 00f6
10421 SPIRead 00f5
10422 SPIRead 00f4
10423
10424 //Read MACRO_ERROR_EXTENDED_CODE_2=0x0;
Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
10425
10426 SPIRead 00f0
10427
10428 //Read MACRO_READY=0x1; Address(0xf0[7:0])
10429
10430
10431 SPIPoll 00f0,0,0,1
10432
10433 SPIWrite 00a3,00 //MACRO_OPERAND_REG0=0x108;
Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
10434 SPIWrite 00a2,00
10435 SPIWrite 00a1,01
10436 SPIWrite 00a0,08
10437 SPIWrite 0193,23 //MACRO_OPCODE=0x23; Address(0x193[7:0],0x194[7:0])
10438
10439 WAIT 0.001
10440 SPIRead 00f0
10441
10442 //Read MACRO_DONE=0x1; Address(0xf0[7:2])
10443
10444
10445 SPIPoll 00f0,2,2,4
10446
10447 SPIRead 00f0
10448
10449 //Read MACRO_ERROR=0x0; Address(0xf0[7:3])
10450
10451 SPIRead 00f1
10452
10453 //Read MACRO_ERROR_OPCODE=0x0; Address(0xf1[7:0],0xf2[7:0])
10454
10455 SPIRead 00f0
10456
10457 //Read MACRO_ERROR_IN_OPCODE=0x0; Address(0xf0[7:4])
10458
```

```

10459 SPIRead 00f0
10460
10461 //Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;      Address(0xf0[7:5])
10462
10463 SPIRead 00f0
10464
10465 //Read  MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])
10466
10467 SPIRead 00f0
10468
10469 //Read  MACRO_ERROR_IN_EXECUTION=0x0;      Address(0xf0[7:7])
10470
10471 SPIRead 00f3
10472 SPIRead 00f2
10473
10474 //Read  MACRO_ERROR_EXTENDED_CODE=0x0;      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
10475
10476 SPIRead 00f7
10477 SPIRead 00f6
10478 SPIRead 00f5
10479 SPIRead 00f4
10480
10481 //Read  MACRO_ERROR_EXTENDED_CODE_2=0x0;
Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
10482
10483 SPIRead 00f0
10484
10485 //Read  MACRO_READY=0x1;      Address(0xf0[7:0])
10486
10487
10488 SPIPoll 00f0,0,0,1
10489
10490 SPIWrite 00a3,77      //MACRO_OPERAND_REG0=0x77400008;
Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
10491 SPIWrite 00a2,40
10492 SPIWrite 00a1,00
10493 SPIWrite 00a0,08
10494 SPIWrite 00a7,ac      //MACRO_OPERAND_REG1=0xac40001b;
Address(0xa4[7:0],0xa5[7:0],0xa6[7:0],0xa7[7:0],0xa8[7:0])
10495 SPIWrite 00a6,40
10496 SPIWrite 00a5,00
10497 SPIWrite 00a4,1b
10498 SPIWrite 00ab,77      //MACRO_OPERAND_REG2=0x77400027;
Address(0xa8[7:0],0xa9[7:0],0xaa[7:0],0xab[7:0],0xac[7:0])
10499 SPIWrite 00aa,40
10500 SPIWrite 00a9,00
10501 SPIWrite 00a8,27
10502 SPIWrite 00af,ac      //MACRO_OPERAND_REG3=0xac40001b;
Address(0xac[7:0],0xad[7:0],0xae[7:0],0xaf[7:0],0xb0[7:0])
10503 SPIWrite 00ae,40
10504 SPIWrite 00ad,00
10505 SPIWrite 00ac,1b
10506 SPIWrite 00b3,00      //MACRO_OPERAND_REG4=0x27;
Address(0xb0[7:0],0xb1[7:0],0xb2[7:0],0xb3[7:0],0xb4[7:0])
10507 SPIWrite 00b2,00
10508 SPIWrite 00b1,00
10509 SPIWrite 00b0,27
10510 SPIWrite 0193,31      //MACRO_OPCODE=0x31;      Address(0x193[7:0],0x194[7:0])
10511
10512 WAIT 0.001
10513 SPIRead 00f0
10514
10515 //Read  MACRO_DONE=0x1;      Address(0xf0[7:2])
10516
10517
10518 SPIPoll 00f0,2,2,4
10519
10520 SPIRead 00f0
10521

```

```
10522 //Read  MACRO_ERROR=0x0;      Address(0xf0[7:3])
10523
10524 SPIRead 00f1
10525
10526 //Read  MACRO_ERROR_OPCODE=0x0;      Address(0xf1[7:0],0xf2[7:0])
10527
10528 SPIRead 00f0
10529
10530 //Read  MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])
10531
10532 SPIRead 00f0
10533
10534 //Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;      Address(0xf0[7:5])
10535
10536 SPIRead 00f0
10537
10538 //Read  MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])
10539
10540 SPIRead 00f0
10541
10542 //Read  MACRO_ERROR_IN_EXECUTION=0x0;  Address(0xf0[7:7])
10543
10544 SPIRead 00f3
10545 SPIRead 00f2
10546
10547 //Read  MACRO_ERROR_EXTENDED_CODE=0x0;  Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
10548
10549 SPIRead 00f7
10550 SPIRead 00f6
10551 SPIRead 00f5
10552 SPIRead 00f4
10553
10554 //Read  MACRO_ERROR_EXTENDED_CODE_2=0x0;
Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
10555
10556
10557 //END: Configuring RX Chain Parameters to TOP MCU
10558
10559 SPIWrite 0018,00 //macro=0x0;      Address(0x18[7:5])
10560
10561 //STEP: sysConfig/step2
10562
10563 //START: Configuring FB Chain Parameters to TOP MCU
10564
10565 SPIWrite 0018,20 //macro=0x1;      Address(0x18[7:5])
10566 SPIRead 00f0
10567
10568 //Read  MACRO_READY=0x1;      Address(0xf0[7:0])
10569
10570
10571 SPIPoll 00f0,0,0,1
10572
10573 SPIWrite 00a3,00 //MACRO_OPERAND_REG0=0x701;
Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
10574 SPIWrite 00a2,00
10575 SPIWrite 00a1,07
10576 SPIWrite 00a0,01
10577 SPIWrite 0193,2d //MACRO_OPCODE=0x2d;      Address(0x193[7:0],0x194[7:0])
10578
10579 WAIT 0.001
10580 SPIRead 00f0
10581
10582 //Read  MACRO_DONE=0x1;      Address(0xf0[7:2])
10583
10584
10585 SPIPoll 00f0,2,2,4
10586
10587 SPIRead 00f0
10588
```

```
10589 //Read  MACRO_ERROR=0x0;      Address(0xf0[7:3])
10590
10591 SPIRead 00f1
10592
10593 //Read  MACRO_ERROR_OPCODE=0x0;      Address(0xf1[7:0],0xf2[7:0])
10594
10595 SPIRead 00f0
10596
10597 //Read  MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])
10598
10599 SPIRead 00f0
10600
10601 //Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;      Address(0xf0[7:5])
10602
10603 SPIRead 00f0
10604
10605 //Read  MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])
10606
10607 SPIRead 00f0
10608
10609 //Read  MACRO_ERROR_IN_EXECUTION=0x0;  Address(0xf0[7:7])
10610
10611 SPIRead 00f3
10612 SPIRead 00f2
10613
10614 //Read  MACRO_ERROR_EXTENDED_CODE=0x0;  Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
10615
10616 SPIRead 00f7
10617 SPIRead 00f6
10618 SPIRead 00f5
10619 SPIRead 00f4
10620
10621 //Read  MACRO_ERROR_EXTENDED_CODE_2=0x0;
Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
10622
10623 SPIRead 00f0
10624
10625 //Read  MACRO_READY=0x1;      Address(0xf0[7:0])
10626
10627
10628 SPIPoll 00f0,0,0,1
10629
10630 SPIWrite 00a3,00 //MACRO_OPERAND_REG0=0x501;
Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
10631 SPIWrite 00a2,00
10632 SPIWrite 00a1,05
10633 SPIWrite 00a0,01
10634 SPIWrite 0193,2a //MACRO_OPCODE=0x2a;      Address(0x193[7:0],0x194[7:0])
10635
10636 WAIT 0.001
10637 SPIRead 00f0
10638
10639 //Read  MACRO_DONE=0x1;      Address(0xf0[7:2])
10640
10641
10642 SPIPoll 00f0,2,2,4
10643
10644 SPIRead 00f0
10645
10646 //Read  MACRO_ERROR=0x0;      Address(0xf0[7:3])
10647
10648 SPIRead 00f1
10649
10650 //Read  MACRO_ERROR_OPCODE=0x0;      Address(0xf1[7:0],0xf2[7:0])
10651
10652 SPIRead 00f0
10653
10654 //Read  MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])
10655
```

```
10656 SPIRead 00f0
10657
10658 //Read MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0; Address(0xf0[7:5])
10659
10660 SPIRead 00f0
10661
10662 //Read MACRO_ERROR_IN_OPERAND=0x0; Address(0xf0[7:6])
10663
10664 SPIRead 00f0
10665
10666 //Read MACRO_ERROR_IN_EXECUTION=0x0; Address(0xf0[7:7])
10667
10668 SPIRead 00f3
10669 SPIRead 00f2
10670
10671 //Read MACRO_ERROR_EXTENDED_CODE=0x0; Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
10672
10673 SPIRead 00f7
10674 SPIRead 00f6
10675 SPIRead 00f5
10676 SPIRead 00f4
10677
10678 //Read MACRO_ERROR_EXTENDED_CODE_2=0x0;
Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
10679
10680 SPIRead 00f0
10681
10682 //Read MACRO_READY=0x1; Address(0xf0[7:0])
10683
10684
10685 SPIPoll 00f0,0,0,1
10686
10687 SPIWrite 00a3,77 //MACRO_OPERAND_REG0=0x77400001;
Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
10688 SPIWrite 00a2,40
10689 SPIWrite 00a1,00
10690 SPIWrite 00a0,01
10691 SPIWrite 00a7,00 //MACRO_OPERAND_REG1=0x1b;
Address(0xa4[7:0],0xa5[7:0],0xa6[7:0],0xa7[7:0],0xa8[7:0])
10692 SPIWrite 00a6,00
10693 SPIWrite 00a5,00
10694 SPIWrite 00a4,1b
10695 SPIWrite 0193,32 //MACRO_OPCODE=0x32; Address(0x193[7:0],0x194[7:0])
10696
10697 WAIT 0.001
10698 SPIRead 00f0
10699
10700 //Read MACRO_DONE=0x1; Address(0xf0[7:2])
10701
10702
10703 SPIPoll 00f0,2,2,4
10704
10705 SPIRead 00f0
10706
10707 //Read MACRO_ERROR=0x0; Address(0xf0[7:3])
10708
10709 SPIRead 00f1
10710
10711 //Read MACRO_ERROR_OPCODE=0x0; Address(0xf1[7:0],0xf2[7:0])
10712
10713 SPIRead 00f0
10714
10715 //Read MACRO_ERROR_IN_OPCODE=0x0; Address(0xf0[7:4])
10716
10717 SPIRead 00f0
10718
10719 //Read MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0; Address(0xf0[7:5])
10720
10721 SPIRead 00f0
```

```
10722
10723 //Read  MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])
10724
10725 SPIRead 00f0
10726
10727 //Read  MACRO_ERROR_IN_EXECUTION=0x0;      Address(0xf0[7:7])
10728
10729 SPIRead 00f3
10730 SPIRead 00f2
10731
10732 //Read  MACRO_ERROR_EXTENDED_CODE=0x0;      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
10733
10734 SPIRead 00f7
10735 SPIRead 00f6
10736 SPIRead 00f5
10737 SPIRead 00f4
10738
10739 //Read  MACRO_ERROR_EXTENDED_CODE_2=0x0;
Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
10740
10741 SPIRead 00f0
10742
10743 //Read  MACRO_READY=0x1;      Address(0xf0[7:0])
10744
10745
10746 SPIPoll 00f0,0,0,1
10747
10748 SPIWrite 00a3,00      //MACRO_OPERAND_REG0=0x502;
Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
10749 SPIWrite 00a2,00
10750 SPIWrite 00a1,05
10751 SPIWrite 00a0,02
10752 SPIWrite 0193,2a      //MACRO_OPCODE=0x2a;      Address(0x193[7:0],0x194[7:0])
10753
10754 WAIT 0.001
10755 SPIRead 00f0
10756
10757 //Read  MACRO_DONE=0x1;      Address(0xf0[7:2])
10758
10759
10760 SPIPoll 00f0,2,2,4
10761
10762 SPIRead 00f0
10763
10764 //Read  MACRO_ERROR=0x0;      Address(0xf0[7:3])
10765
10766 SPIRead 00f1
10767
10768 //Read  MACRO_ERROR_OPCODE=0x0;      Address(0xf1[7:0],0xf2[7:0])
10769
10770 SPIRead 00f0
10771
10772 //Read  MACRO_ERROR_IN_OPCODE=0x0;      Address(0xf0[7:4])
10773
10774 SPIRead 00f0
10775
10776 //Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;      Address(0xf0[7:5])
10777
10778 SPIRead 00f0
10779
10780 //Read  MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])
10781
10782 SPIRead 00f0
10783
10784 //Read  MACRO_ERROR_IN_EXECUTION=0x0;      Address(0xf0[7:7])
10785
10786 SPIRead 00f3
10787 SPIRead 00f2
10788
```

```

10789 //Read  MACRO_ERROR_EXTENDED_CODE=0x0;  Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
10790
10791 SPIRead 00f7
10792 SPIRead 00f6
10793 SPIRead 00f5
10794 SPIRead 00f4
10795
10796 //Read  MACRO_ERROR_EXTENDED_CODE_2=0x0;
Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
10797
10798 SPIRead 00f0
10799
10800 //Read  MACRO_READY=0x1;  Address(0xf0[7:0])
10801
10802
10803 SPIPoll 00f0,0,0,1
10804
10805 SPIWrite 00a3,77 //MACRO_OPERAND_REG0=0x77400002;
Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
10806 SPIWrite 00a2,40
10807 SPIWrite 00a1,00
10808 SPIWrite 00a0,02
10809 SPIWrite 00a7,00 //MACRO_OPERAND_REG1=0x1b;
Address(0xa4[7:0],0xa5[7:0],0xa6[7:0],0xa7[7:0],0xa8[7:0])
10810 SPIWrite 00a6,00
10811 SPIWrite 00a5,00
10812 SPIWrite 00a4,1b
10813 SPIWrite 0193,32 //MACRO_OPCODE=0x32;  Address(0x193[7:0],0x194[7:0])
10814
10815 WAIT 0.001
10816 SPIRead 00f0
10817
10818 //Read  MACRO_DONE=0x1;  Address(0xf0[7:2])
10819
10820
10821 SPIPoll 00f0,2,2,4
10822
10823 SPIRead 00f0
10824
10825 //Read  MACRO_ERROR=0x0;  Address(0xf0[7:3])
10826
10827 SPIRead 00f1
10828
10829 //Read  MACRO_ERROR_OPCODE=0x0;  Address(0xf1[7:0],0xf2[7:0])
10830
10831 SPIRead 00f0
10832
10833 //Read  MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])
10834
10835 SPIRead 00f0
10836
10837 //Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;  Address(0xf0[7:5])
10838
10839 SPIRead 00f0
10840
10841 //Read  MACRO_ERROR_IN_OPERAND=0x0;  Address(0xf0[7:6])
10842
10843 SPIRead 00f0
10844
10845 //Read  MACRO_ERROR_IN_EXECUTION=0x0;  Address(0xf0[7:7])
10846
10847 SPIRead 00f3
10848 SPIRead 00f2
10849
10850 //Read  MACRO_ERROR_EXTENDED_CODE=0x0;  Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
10851
10852 SPIRead 00f7
10853 SPIRead 00f6
10854 SPIRead 00f5

```

```
10855 SPIRead 00f4
10856
10857 //Read MACRO_ERROR_EXTENDED_CODE_2=0x0;
Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

10858
10859
10860 //END: Configuring FB Chain Parameters to TOP MCU
10861
10862 SPIWrite 0018,00 //macro=0x0; Address(0x18[7:5])
10863
10864 //STEP: sysConfig/step3
10865
10866 //START: Configuring TX Chain Parameters to TOP MCU
10867
10868 SPIWrite 0018,20 //macro=0x1; Address(0x18[7:5])
10869 SPIRead 00f0
10870
10871 //Read MACRO_READY=0x1; Address(0xf0[7:0])
10872
10873
10874 SPIPoll 00f0,0,0,1
10875
10876 SPIWrite 00a3,00 //MACRO_OPERAND_REG0=0x0;
Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
10877 SPIWrite 00a2,00
10878 SPIWrite 00a1,00
10879 SPIWrite 00a0,00
10880 SPIWrite 0193,8d //MACRO_OPCODE=0x8d; Address(0x193[7:0],0x194[7:0])
10881
10882 WAIT 0.001
10883 SPIRead 00f0
10884
10885 //Read MACRO_DONE=0x1; Address(0xf0[7:2])
10886
10887
10888 SPIPoll 00f0,2,2,4
10889
10890 SPIRead 00f0
10891
10892 //Read MACRO_ERROR=0x0; Address(0xf0[7:3])
10893
10894 SPIRead 00f1
10895
10896 //Read MACRO_ERROR_OPCODE=0x0; Address(0xf1[7:0],0xf2[7:0])
10897
10898 SPIRead 00f0
10899
10900 //Read MACRO_ERROR_IN_OPCODE=0x0; Address(0xf0[7:4])
10901
10902 SPIRead 00f0
10903
10904 //Read MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0; Address(0xf0[7:5])
10905
10906 SPIRead 00f0
10907
10908 //Read MACRO_ERROR_IN_OPERAND=0x0; Address(0xf0[7:6])
10909
10910 SPIRead 00f0
10911
10912 //Read MACRO_ERROR_IN_EXECUTION=0x0; Address(0xf0[7:7])
10913
10914 SPIRead 00f3
10915 SPIRead 00f2
10916
10917 //Read MACRO_ERROR_EXTENDED_CODE=0x0; Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
10918
10919 SPIRead 00f7
10920 SPIRead 00f6
10921 SPIRead 00f5
```



```
10922 SPIRead 00f4
10923
10924 //Read MACRO_ERROR_EXTENDED_CODE_2=0x0;
Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
10925
10926 SPIRead 00f0
10927
10928 //Read MACRO_READY=0x1; Address(0xf0[7:0])
10929
10930
10931 SPIPoll 00f0,0,0,1
10932
10933 SPIWrite 00a3,00 //MACRO_OPERAND_REG0=0xc03;
Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
10934 SPIWrite 00a2,00
10935 SPIWrite 00a1,0c
10936 SPIWrite 00a0,03
10937 SPIWrite 0193,2e //MACRO_OPCODE=0x2e; Address(0x193[7:0],0x194[7:0])
10938
10939 WAIT 0.001
10940 SPIRead 00f0
10941
10942 //Read MACRO_DONE=0x1; Address(0xf0[7:2])
10943
10944
10945 SPIPoll 00f0,2,2,4
10946
10947 SPIRead 00f0
10948
10949 //Read MACRO_ERROR=0x0; Address(0xf0[7:3])
10950
10951 SPIRead 00f1
10952
10953 //Read MACRO_ERROR_OPCODE=0x0; Address(0xf1[7:0],0xf2[7:0])
10954
10955 SPIRead 00f0
10956
10957 //Read MACRO_ERROR_IN_OPCODE=0x0; Address(0xf0[7:4])
10958
10959 SPIRead 00f0
10960
10961 //Read MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0; Address(0xf0[7:5])
10962
10963 SPIRead 00f0
10964
10965 //Read MACRO_ERROR_IN_OPERAND=0x0; Address(0xf0[7:6])
10966
10967 SPIRead 00f0
10968
10969 //Read MACRO_ERROR_IN_EXECUTION=0x0; Address(0xf0[7:7])
10970
10971 SPIRead 00f3
10972 SPIRead 00f2
10973
10974 //Read MACRO_ERROR_EXTENDED_CODE=0x0; Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
10975
10976 SPIRead 00f7
10977 SPIRead 00f6
10978 SPIRead 00f5
10979 SPIRead 00f4
10980
10981 //Read MACRO_ERROR_EXTENDED_CODE_2=0x0;
Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
10982
10983 SPIRead 00f0
10984
10985 //Read MACRO_READY=0x1; Address(0xf0[7:0])
10986
10987
```

```

10988 SPIPoll 00f0,0,0,1
10989
10990 SPIWrite 00a3,00 //MACRO_OPERAND_REG0=0x50f;
Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
10991 SPIWrite 00a2,00
10992 SPIWrite 00a1,05
10993 SPIWrite 00a0,0f
10994 SPIWrite 0193,2b //MACRO_OPCODE=0x2b; Address(0x193[7:0],0x194[7:0])
10995
10996 WAIT 0.001
10997 SPIRead 00f0
10998
10999 //Read MACRO_DONE=0x1; Address(0xf0[7:2])
11000
11001
11002 SPIPoll 00f0,2,2,4
11003
11004 SPIRead 00f0
11005
11006 //Read MACRO_ERROR=0x0; Address(0xf0[7:3])
11007
11008 SPIRead 00f1
11009
11010 //Read MACRO_ERROR_OPCODE=0x0; Address(0xf1[7:0],0xf2[7:0])
11011
11012 SPIRead 00f0
11013
11014 //Read MACRO_ERROR_IN_OPCODE=0x0; Address(0xf0[7:4])
11015
11016 SPIRead 00f0
11017
11018 //Read MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0; Address(0xf0[7:5])
11019
11020 SPIRead 00f0
11021
11022 //Read MACRO_ERROR_IN_OPERAND=0x0; Address(0xf0[7:6])
11023
11024 SPIRead 00f0
11025
11026 //Read MACRO_ERROR_IN_EXECUTION=0x0; Address(0xf0[7:7])
11027
11028 SPIRead 00f3
11029 SPIRead 00f2
11030
11031 //Read MACRO_ERROR_EXTENDED_CODE=0x0; Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
11032
11033 SPIRead 00f7
11034 SPIRead 00f6
11035 SPIRead 00f5
11036 SPIRead 00f4
11037
11038 //Read MACRO_ERROR_EXTENDED_CODE_2=0x0;
Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
11039
11040 SPIRead 00f0
11041
11042 //Read MACRO_READY=0x1; Address(0xf0[7:0])
11043
11044
11045 SPIPoll 00f0,0,0,1
11046
11047 SPIWrite 00a3,00 //MACRO_OPERAND_REG0=0x1f0;
Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
11048 SPIWrite 00a2,00
11049 SPIWrite 00a1,01
11050 SPIWrite 00a0,f0
11051 SPIWrite 0193,23 //MACRO_OPCODE=0x23; Address(0x193[7:0],0x194[7:0])
11052
11053 WAIT 0.001

```

```
11054 SPIRead 00f0
11055
11056 //Read MACRO_DONE=0x1;      Address(0xf0[7:2])
11057
11058
11059 SPIPoll 00f0,2,2,4
11060
11061 SPIRead 00f0
11062
11063 //Read MACRO_ERROR=0x0;      Address(0xf0[7:3])
11064
11065 SPIRead 00f1
11066
11067 //Read MACRO_ERROR_OPCODE=0x0;      Address(0xf1[7:0],0xf2[7:0])
11068
11069 SPIRead 00f0
11070
11071 //Read MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])
11072
11073 SPIRead 00f0
11074
11075 //Read MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;      Address(0xf0[7:5])
11076
11077 SPIRead 00f0
11078
11079 //Read MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])
11080
11081 SPIRead 00f0
11082
11083 //Read MACRO_ERROR_IN_EXECUTION=0x0;  Address(0xf0[7:7])
11084
11085 SPIRead 00f3
11086 SPIRead 00f2
11087
11088 //Read MACRO_ERROR_EXTENDED_CODE=0x0;  Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
11089
11090 SPIRead 00f7
11091 SPIRead 00f6
11092 SPIRead 00f5
11093 SPIRead 00f4
11094
11095 //Read MACRO_ERROR_EXTENDED_CODE_2=0x0;
Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
11096
11097 SPIRead 00f0
11098
11099 //Read MACRO_READY=0x1;      Address(0xf0[7:0])
11100
11101
11102 SPIPoll 00f0,0,0,1
11103
11104 SPIWrite 00a3,77      //MACRO_OPERAND_REG0=0x7740000f;
Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
11105 SPIWrite 00a2,40
11106 SPIWrite 00a1,00
11107 SPIWrite 00a0,0f
11108 SPIWrite 00a7,ac      //MACRO_OPERAND_REG1=0xac40001b;
Address(0xa4[7:0],0xa5[7:0],0xa6[7:0],0xa7[7:0],0xa8[7:0])
11109 SPIWrite 00a6,40
11110 SPIWrite 00a5,00
11111 SPIWrite 00a4,1b
11112 SPIWrite 00ab,77      //MACRO_OPERAND_REG2=0x77400027;
Address(0xa8[7:0],0xa9[7:0],0xaa[7:0],0xab[7:0],0xac[7:0])
11113 SPIWrite 00aa,40
11114 SPIWrite 00a9,00
11115 SPIWrite 00a8,27
11116 SPIWrite 00af,ac      //MACRO_OPERAND_REG3=0xac40001b;
Address(0xac[7:0],0xad[7:0],0xae[7:0],0xaf[7:0],0xb0[7:0])
11117 SPIWrite 00ae,40
```

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11118 SPIWrite 00ad,00
11119 SPIWrite 00ac,1b
11120 SPIWrite 00b3,00 //MACRO_OPERAND_REG4=0x27;
Address(0xb0[7:0],0xb1[7:0],0xb2[7:0],0xb3[7:0],0xb4[7:0])
11121 SPIWrite 00b2,00
11122 SPIWrite 00b1,00
11123 SPIWrite 00b0,27
11124 SPIWrite 0193,30 //MACRO_OPCODE=0x30; Address(0x193[7:0],0x194[7:0])
11125
11126 WAIT 0.001
11127 SPIRead 00f0
11128
11129 //Read MACRO_DONE=0x1; Address(0xf0[7:2])
11130
11131
11132 SPIPoll 00f0,2,2,4
11133
11134 SPIRead 00f0
11135
11136 //Read MACRO_ERROR=0x0; Address(0xf0[7:3])
11137
11138 SPIRead 00f1
11139
11140 //Read MACRO_ERROR_OPCODE=0x0; Address(0xf1[7:0],0xf2[7:0])
11141
11142 SPIRead 00f0
11143
11144 //Read MACRO_ERROR_IN_OPCODE=0x0; Address(0xf0[7:4])
11145
11146 SPIRead 00f0
11147
11148 //Read MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0; Address(0xf0[7:5])
11149
11150 SPIRead 00f0
11151
11152 //Read MACRO_ERROR_IN_OPERAND=0x0; Address(0xf0[7:6])
11153
11154 SPIRead 00f0
11155
11156 //Read MACRO_ERROR_IN_EXECUTION=0x0; Address(0xf0[7:7])
11157
11158 SPIRead 00f3
11159 SPIRead 00f2
11160
11161 //Read MACRO_ERROR_EXTENDED_CODE=0x0; Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
11162
11163 SPIRead 00f7
11164 SPIRead 00f6
11165 SPIRead 00f5
11166 SPIRead 00f4
11167
11168 //Read MACRO_ERROR_EXTENDED_CODE_2=0x0;
Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
11169
11170
11171 //END: Configuring TX Chain Parameters to TOP MCU
11172
11173 SPIWrite 0018,00 //macro=0x0; Address(0x18[7:5])
11174
11175 //STEP: configTune/step0
11176
11177 //START: Configuring Digital Chain
11178
11179 SPIWrite 0018,20 //macro=0x1; Address(0x18[7:5])
11180 SPIRead 00f0
11181
11182 //Read MACRO_READY=0x1; Address(0xf0[7:0])
11183
11184

```

```

11185 SPIPoll 00f0,0,0,1
11186
11187 SPIWrite 00a3,00 //MACRO_OPERAND_REG0=0xf1f;
Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
11188 SPIWrite 00a2,00
11189 SPIWrite 00a1,0f
11190 SPIWrite 00a0,1f
11191 SPIWrite 0193,36 //MACRO_OPCODE=0x36; Address(0x193[7:0],0x194[7:0])
11192
11193 WAIT 0.001
11194 SPIRead 00f0
11195
11196 //Read MACRO_DONE=0x1; Address(0xf0[7:2])
11197
11198
11199 SPIPoll 00f0,2,2,4
11200
11201 SPIRead 00f0
11202
11203 //Read MACRO_ERROR=0x0; Address(0xf0[7:3])
11204
11205 SPIRead 00f1
11206
11207 //Read MACRO_ERROR_OPCODE=0x0; Address(0xf1[7:0],0xf2[7:0])
11208
11209 SPIRead 00f0
11210
11211 //Read MACRO_ERROR_IN_OPCODE=0x0; Address(0xf0[7:4])
11212
11213 SPIRead 00f0
11214
11215 //Read MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0; Address(0xf0[7:5])
11216
11217 SPIRead 00f0
11218
11219 //Read MACRO_ERROR_IN_OPERAND=0x0; Address(0xf0[7:6])
11220
11221 SPIRead 00f0
11222
11223 //Read MACRO_ERROR_IN_EXECUTION=0x0; Address(0xf0[7:7])
11224
11225 SPIRead 00f3
11226 SPIRead 00f2
11227
11228 //Read MACRO_ERROR_EXTENDED_CODE=0x0; Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
11229
11230 SPIRead 00f7
11231 SPIRead 00f6
11232 SPIRead 00f5
11233 SPIRead 00f4
11234
11235 //Read MACRO_ERROR_EXTENDED_CODE_2=0x0;
Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
11236
11237
11238 //END: Configuring Digital Chain
11239
11240 SPIWrite 0018,00 //macro=0x0; Address(0x18[7:5])
11241
11242 //STEP: configTune/step1
11243
11244 //START: Setting FIFO Pointers
11245
11246 SPIWrite 0012,01 //rxdig=0x1; Address(0x12[7:0])
11247 SPIWrite 0060,46 //async_fifo_ptr_offset_p0=0x6; Address(0x60[7:0])
11248 SPIWrite 0060,66 //async_fifo_ptr_offset_p1=0x6; Address(0x60[7:4])
11249 SPIWrite 0061,46 //async_fifo_ptr_offset_p2=0x6; Address(0x61[7:0])
11250 SPIWrite 0061,66 //async_fifo_ptr_offset_p3=0x6; Address(0x61[7:4])
11251 SPIWrite 0012,02 //rxdig=0x2; Address(0x12[7:0])

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```

11252 SPIWrite 0060,46 //async_fifo_ptr_offset_p0=0x6; Address(0x60[7:0])
11253 SPIWrite 0060,66 //async_fifo_ptr_offset_p1=0x6; Address(0x60[7:4])
11254 SPIWrite 0061,46 //async_fifo_ptr_offset_p2=0x6; Address(0x61[7:0])
11255 SPIWrite 0061,66 //async_fifo_ptr_offset_p3=0x6; Address(0x61[7:4])
11256 SPIWrite 0012,04 //rxdig=0x4; Address(0x12[7:0])
11257 SPIWrite 0060,46 //async_fifo_ptr_offset_p0=0x6; Address(0x60[7:0])
11258 SPIWrite 0060,66 //async_fifo_ptr_offset_p1=0x6; Address(0x60[7:4])
11259 SPIWrite 0061,46 //async_fifo_ptr_offset_p2=0x6; Address(0x61[7:0])
11260 SPIWrite 0061,66 //async_fifo_ptr_offset_p3=0x6; Address(0x61[7:4])
11261 SPIWrite 0012,08 //rxdig=0x8; Address(0x12[7:0])
11262 SPIWrite 0060,46 //async_fifo_ptr_offset_p0=0x6; Address(0x60[7:0])
11263 SPIWrite 0060,66 //async_fifo_ptr_offset_p1=0x6; Address(0x60[7:4])
11264 SPIWrite 0061,46 //async_fifo_ptr_offset_p2=0x6; Address(0x61[7:0])
11265 SPIWrite 0061,66 //async_fifo_ptr_offset_p3=0x6; Address(0x61[7:4])
11266 SPIWrite 0012,00 //rxdig=0x0; Address(0x12[7:0])
11267 SPIWrite 0012,10 //fbdig=0x1; Address(0x12[7:4])
11268 SPIWrite 0060,46 //async_fifo_ptr_offset_p0=0x6; Address(0x60[7:0])
11269 SPIWrite 0060,66 //async_fifo_ptr_offset_p1=0x6; Address(0x60[7:4])
11270 SPIWrite 0061,46 //async_fifo_ptr_offset_p2=0x6; Address(0x61[7:0])
11271 SPIWrite 0061,66 //async_fifo_ptr_offset_p3=0x6; Address(0x61[7:4])
11272 SPIWrite 0012,20 //fbdig=0x2; Address(0x12[7:4])
11273 SPIWrite 0060,46 //async_fifo_ptr_offset_p0=0x6; Address(0x60[7:0])
11274 SPIWrite 0060,66 //async_fifo_ptr_offset_p1=0x6; Address(0x60[7:4])
11275 SPIWrite 0061,46 //async_fifo_ptr_offset_p2=0x6; Address(0x61[7:0])
11276 SPIWrite 0061,66 //async_fifo_ptr_offset_p3=0x6; Address(0x61[7:4])
11277 SPIWrite 0012,00 //fbdig=0x0; Address(0x12[7:4])
11278 SPIWrite 0019,10 //txdig=0x1; Address(0x19[7:4])
11279 SPIWrite 0062,06 //cfg_rd_ptr_out_async_fifo=0x6; Address(0x62[7:0])
11280 SPIWrite 0019,20 //txdig=0x2; Address(0x19[7:4])
11281 SPIWrite 0062,06 //cfg_rd_ptr_out_async_fifo=0x6; Address(0x62[7:0])
11282 SPIWrite 0019,40 //txdig=0x4; Address(0x19[7:4])
11283 SPIWrite 0062,06 //cfg_rd_ptr_out_async_fifo=0x6; Address(0x62[7:0])
11284 SPIWrite 0019,80 //txdig=0x8; Address(0x19[7:4])
11285 SPIWrite 0062,06 //cfg_rd_ptr_out_async_fifo=0x6; Address(0x62[7:0])
11286 SPIWrite 0019,10 //txdig=0x1; Address(0x19[7:4])
11287 SPIWrite 0060,00 //cfg_wr_ptr_async_fifo_offset_val=0x0; Address(0x60[7:0])
11288 SPIWrite 0019,20 //txdig=0x2; Address(0x19[7:4])
11289 SPIWrite 0060,00 //cfg_wr_ptr_async_fifo_offset_val=0x0; Address(0x60[7:0])
11290 SPIWrite 0019,40 //txdig=0x4; Address(0x19[7:4])
11291 SPIWrite 0060,00 //cfg_wr_ptr_async_fifo_offset_val=0x0; Address(0x60[7:0])
11292 SPIWrite 0019,80 //txdig=0x8; Address(0x19[7:4])
11293 SPIWrite 0060,00 //cfg_wr_ptr_async_fifo_offset_val=0x0; Address(0x60[7:0])
11294 SPIWrite 0019,00 //txdig=0x0; Address(0x19[7:4])
11295 SPIWrite 0016,10 //jesd_subchip=0x1; Address(0x16[7:4])
11296 SPIWrite 0030,8c //rxa_afifo_offset=0xc; Address(0x30[7:0])
11297 SPIWrite 0030,cc //rxb_afifo_offset=0xc; Address(0x30[7:4])
11298 SPIWrite 0031,8c //rxc_afifo_offset=0xc; Address(0x31[7:0])
11299 SPIWrite 0031,cc //rxd_afifo_offset=0xc; Address(0x31[7:4])
11300 SPIWrite 0032,80 //fba_afifo_offset=0x0; Address(0x32[7:0])
11301 SPIWrite 0032,00 //fbc_afifo_offset=0x0; Address(0x32[7:4])
11302
11303 //END: Setting FIFO Pointers
11304
11305 SPIWrite 0016,00 //jesd_subchip=0x0; Address(0x16[7:4])
11306 SPIWrite 0018,20 //macro=0x1; Address(0x18[7:5])
11307 SPIRead 00f0
11308
11309 //Read MACRO_READY=0x1; Address(0xf0[7:0])
11310
11311
11312 SPIPoll 00f0,0,0,1
11313
11314 SPIWrite 0193,3d //MACRO_OPCODE=0x3d; Address(0x193[7:0],0x194[7:0])
11315
11316 WAIT 0.001
11317 SPIRead 00f0
11318
11319 //Read MACRO_DONE=0x1; Address(0xf0[7:2])
11320

```

```

11321
11322 SPIPoll 00f0,2,2,4
11323
11324 SPIRead 00f0
11325
11326 //Read MACRO_ERROR=0x0; Address(0xf0[7:3])
11327
11328 SPIRead 00f1
11329
11330 //Read MACRO_ERROR_OPCODE=0x0; Address(0xf1[7:0],0xf2[7:0])
11331
11332 SPIRead 00f0
11333
11334 //Read MACRO_ERROR_IN_OPCODE=0x0; Address(0xf0[7:4])
11335
11336 SPIRead 00f0
11337
11338 //Read MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0; Address(0xf0[7:5])
11339
11340 SPIRead 00f0
11341
11342 //Read MACRO_ERROR_IN_OPERAND=0x0; Address(0xf0[7:6])
11343
11344 SPIRead 00f0
11345
11346 //Read MACRO_ERROR_IN_EXECUTION=0x0; Address(0xf0[7:7])
11347
11348 SPIRead 00f3
11349 SPIRead 00f2
11350
11351 //Read MACRO_ERROR_EXTENDED_CODE=0x0; Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
11352
11353 SPIRead 00f7
11354 SPIRead 00f6
11355 SPIRead 00f5
11356 SPIRead 00f4
11357
11358 //Read MACRO_ERROR_EXTENDED_CODE_2=0x0;
Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
11359
11360 SPIWrite 0018,00 //macro=0x0; Address(0x18[7:5])
11361
11362 //STEP: analogWrites/step0
11363 SPIWrite 0011,3f //ec_ana=0x3f; Address(0x11[7:0])
11364 SPIWrite 0075,00 //NCTRL_CTRL=0x6; Address(0x75[7:7],0x76[7:0])
11365 SPIWrite 0076,03
11366 SPIWrite 0071,04 //TRIM_VR_LATPP=0x2; Address(0x71[7:1])
11367 SPIWrite 0071,14 //PK_MEASURE_CC=0x1; Address(0x71[7:4])
11368 SPIWrite 0084,80 //INV_PF_CTRL=0xe; Address(0x84[7:6],0x85[7:0])
11369 SPIWrite 0085,03
11370 SPIWrite 0011,00 //ec_ana=0x0; Address(0x11[7:0])
11371 SPIWrite 0018,20 //macro=0x1; Address(0x18[7:5])
11372 SPIRead 00f0
11373
11374 //Read MACRO_READY=0x1; Address(0xf0[7:0])
11375
11376
11377 SPIPoll 00f0,0,0,1
11378
11379 SPIWrite 00a3,00 //MACRO_OPERAND_REG0=0x124;
Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
11380 SPIWrite 00a2,00
11381 SPIWrite 00a1,01
11382 SPIWrite 00a0,24
11383 SPIWrite 0193,72 //MACRO_OPCODE=0x72; Address(0x193[7:0],0x194[7:0])
11384
11385 WAIT 0.001
11386 SPIRead 00f0
11387

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```
11388 //Read MACRO_DONE=0x1; Address(0xf0[7:2])
11389
11390
11391 SPIPoll 00f0,2,2,4
11392
11393 SPIRead 00f0
11394
11395 //Read MACRO_ERROR=0x0; Address(0xf0[7:3])
11396
11397 SPIRead 00f1
11398
11399 //Read MACRO_ERROR_OPCODE=0x0; Address(0xf1[7:0],0xf2[7:0])
11400
11401 SPIRead 00f0
11402
11403 //Read MACRO_ERROR_IN_OPCODE=0x0; Address(0xf0[7:4])
11404
11405 SPIRead 00f0
11406
11407 //Read MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0; Address(0xf0[7:5])
11408
11409 SPIRead 00f0
11410
11411 //Read MACRO_ERROR_IN_OPERAND=0x0; Address(0xf0[7:6])
11412
11413 SPIRead 00f0
11414
11415 //Read MACRO_ERROR_IN_EXECUTION=0x0; Address(0xf0[7:7])
11416
11417 SPIRead 00f3
11418 SPIRead 00f2
11419
11420 //Read MACRO_ERROR_EXTENDED_CODE=0x0; Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
11421
11422 SPIRead 00f7
11423 SPIRead 00f6
11424 SPIRead 00f5
11425 SPIRead 00f4
11426
11427 //Read MACRO_ERROR_EXTENDED_CODE_2=0x0;
Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
11428
11429 SPIRead 00f0
11430
11431 //Read MACRO_READY=0x1; Address(0xf0[7:0])
11432
11433
11434 SPIPoll 00f0,0,0,1
11435
11436 SPIWrite 00a3,01 //MACRO_OPERAND_REG0=0x1000600;
Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
11437 SPIWrite 00a2,00
11438 SPIWrite 00a1,06
11439 SPIWrite 00a0,00
11440 SPIWrite 00a7,05 //MACRO_OPERAND_REG1=0x5040302;
Address(0xa4[7:0],0xa5[7:0],0xa6[7:0],0xa7[7:0],0xa8[7:0])
11441 SPIWrite 00a6,04
11442 SPIWrite 00a5,03
11443 SPIWrite 00a4,02
11444 SPIWrite 0193,71 //MACRO_OPCODE=0x71; Address(0x193[7:0],0x194[7:0])
11445
11446 WAIT 0.001
11447 SPIRead 00f0
11448
11449 //Read MACRO_DONE=0x1; Address(0xf0[7:2])
11450
11451
11452 SPIPoll 00f0,2,2,4
11453
```



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11454 SPIRead 00f0
11455
11456 //Read  MACRO_ERROR=0x0;      Address(0xf0[7:3])
11457
11458 SPIRead 00f1
11459
11460 //Read  MACRO_ERROR_OPCODE=0x0;      Address(0xf1[7:0],0xf2[7:0])
11461
11462 SPIRead 00f0
11463
11464 //Read  MACRO_ERROR_IN_OPCODE=0x0;   Address(0xf0[7:4])
11465
11466 SPIRead 00f0
11467
11468 //Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;      Address(0xf0[7:5])
11469
11470 SPIRead 00f0
11471
11472 //Read  MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])
11473
11474 SPIRead 00f0
11475
11476 //Read  MACRO_ERROR_IN_EXECUTION=0x0;   Address(0xf0[7:7])
11477
11478 SPIRead 00f3
11479 SPIRead 00f2
11480
11481 //Read  MACRO_ERROR_EXTENDED_CODE=0x0;   Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
11482
11483 SPIRead 00f7
11484 SPIRead 00f6
11485 SPIRead 00f5
11486 SPIRead 00f4
11487
11488 //Read  MACRO_ERROR_EXTENDED_CODE_2=0x0;
Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
11489
11490 SPIWrite 0018,00      //macro=0x0;      Address(0x18[7:5])
11491 SPIWrite 0011,3f      //ec_ana=0x3f;   Address(0x11[7:0])
11492 SPIWrite 0060,01      //TM_DLL_RESET=0x1;      Address(0x60[7:0])
11493 SPIWrite 0060,00      //TM_DLL_RESET=0x0;      Address(0x60[7:0])
11494 SPIWrite 0011,00      //ec_ana=0x0;   Address(0x11[7:0])
11495
11496 //STEP: analogWrites/step1
11497
11498 //START: Removing TDD Pin Overrides.
11499
11500 SPIWrite 0015,80      //timing_controller=0x1;   Address(0x15[7:7])
11501 SPIWrite 00ed,00      //reg_for_rxtdd=0x0;   Address(0xed[7:0])
11502 SPIWrite 00f5,00      //reg_for_fbtdd=0x0;   Address(0xf5[7:0])
11503 SPIWrite 00e5,0f      //reg_for_txtdd=0xf;   Address(0xe5[7:0])
11504
11505 //END: Removing TDD Pin Overrides.
11506
11507
11508 //START: DAC Analog Writes
11509
11510 SPIWrite 0015,00      //timing_controller=0x0;   Address(0x15[7:7])
11511 SPIWrite 0013,0f      //txdh=0xf;      Address(0x13[7:0])
11512 SPIWrite 015a,20      //po_ppa_corr_pdn=0x1;   Address(0x15a[7:5])
11513 SPIWrite 01bd,00      //po_ana_spare8=0x1;   Address(0x1bc[7:0],0x1bd[7:0],0x1be[7:0])
11514 SPIWrite 01bc,01
11515 SPIWrite 015a,22      //po_ppa_pdn=0x1;   Address(0x15a[7:1])
11516 SPIWrite 0070,27      //dsa_dac_decode1_th1=0x27;   Address(0x70[7:0])
11517 SPIWrite 0071,27      //dsa_dac_decode1_th2=0x27;   Address(0x71[7:0])
11518 SPIWrite 0072,27      //dsa_dac_decode1_th3=0x27;   Address(0x72[7:0])
11519 SPIWrite 0074,27      //dsa_dac_decode2_th1=0x27;   Address(0x74[7:0])
11520 SPIWrite 0075,27      //dsa_dac_decode2_th2=0x27;   Address(0x75[7:0])
11521 SPIWrite 0076,27      //dsa_dac_decode2_th3=0x27;   Address(0x76[7:0])

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11522 SPIWrite 0078,27 //dsa_dac_decode3_th1=0x27; Address(0x78[7:0])
11523 SPIWrite 0079,27 //dsa_dac_decode3_th2=0x27; Address(0x79[7:0])
11524 SPIWrite 007a,27 //dsa_dac_decode3_th3=0x27; Address(0x7a[7:0])
11525 SPIWrite 015a,26 //po_caldac_ldo_pdn=0x1; Address(0x15a[7:2])
11526 SPIWrite 015a,26 //po_caldac_ldo_pdn=0x1; Address(0x15a[7:2])
11527 SPIWrite 0025,00 //twos_complement_mode=0x0; Address(0x25[7:0])
11528 SPIWrite 015a,27 //po_cg_pdn=0x1; Address(0x15a[7:0])
11529 SPIWrite 0168,01 //po_dac1_common_resetz=0x1; Address(0x168[7:0])
11530 SPIWrite 017c,01 //po_dac2_common_resetz=0x1; Address(0x17c[7:0])
11531 SPIWrite 01b1,00 //po_ana_spare5=0x10; Address(0x1b0[7:0],0x1b1[7:0],0x1b2[7:0])
11532 SPIWrite 01b0,10
11533 SPIWrite 0158,01 //po_caldac1_pdn=0x1; Address(0x158[7:0])
11534 SPIWrite 0159,01 //po_caldac2_pdn=0x1; Address(0x159[7:0])
11535 SPIWrite 0177,00 //po_dac1_enc_tm_lv=0x800000001;
Address(0x174[7:0],0x175[7:0],0x176[7:0],0x177[7:0],0x178[7:0],0x178[7:0])
11536 SPIWrite 0176,00
11537 SPIWrite 0175,00
11538 SPIWrite 0174,01
11539 SPIWrite 0178,08
11540 SPIWrite 018b,00 //po_dac2_enc_tm_lv=0x800000001;
Address(0x188[7:0],0x189[7:0],0x18a[7:0],0x18b[7:0],0x18c[7:0],0x18c[7:0])
11541 SPIWrite 018a,00
11542 SPIWrite 0189,00
11543 SPIWrite 0188,01
11544 SPIWrite 018c,08
11545 SPIWrite 011a,00 //po_dac1_tm=0x0; Address(0x118[4:0],0x119[4:0],0x11a[7:0])
11546 SPIWrite 0119,00
11547 SPIWrite 0118,00
11548 SPIWrite 0126,00 //po_dac2_tm=0x0; Address(0x124[4:0],0x125[4:0],0x126[7:0])
11549 SPIWrite 0125,00
11550 SPIWrite 0124,00
11551 SPIWrite 01c5,3d //po_ana_spare10=0x3de0; Address(0x1c4[7:0],0x1c5[7:0],0x1c6[7:0])
11552 SPIWrite 01c4,e0
11553 SPIWrite 0133,00 //po_ppa_tm=0x1fe0;
Address(0x130[7:0],0x131[7:0],0x132[7:0],0x133[7:0],0x134[7:0],0x134[6:0],0x135[7:0])
11554 SPIWrite 0132,00
11555 SPIWrite 0131,1f
11556 SPIWrite 0130,e0
11557 SPIWrite 0135,00
11558 SPIWrite 0134,00
11559 SPIWrite 0029,00 //dh_lsb_xor_enc=0x0; Address(0x29[7:0])
11560 SPIWrite 018e,01 //po_en_lsb_xor=0x1; Address(0x18e[7:0])
11561 SPIWrite 0112,00 //po_cml_tm=0x0; Address(0x110[2:0],0x111[2:0],0x112[7:0])
11562 SPIWrite 0111,00
11563 SPIWrite 0110,00
11564 SPIWrite 0151,0e //po_mix_delay_prog=0xed3; Address(0x150[7:0],0x151[7:0],0x152[7:0])
11565 SPIWrite 0150,d3
11566 SPIWrite 01ad,00 //po_ana_spare4=0xff; Address(0x1ac[7:0],0x1ad[7:0],0x1ae[7:0])
11567 SPIWrite 01ac,ff
11568 SPIWrite 0162,00 //po_dac1_clk_prog=0x0; Address(0x162[7:0])
11569 SPIWrite 0163,00 //po_dac2_clk_prog=0x0; Address(0x163[7:0])
11570 SPIWrite 0013,00 //txdh=0x0; Address(0x13[7:0])
11571
11572 //START: Requesting/releasing SPI Access to PLL Pages
11573
11574 SPIWrite 0015,40 //digtop=0x1; Address(0x15[7:6])
11575 SPIWrite 0170,01 //pll_reg_spi_req_a=0x1; Address(0x170[7:0])
11576 SPIWrite 0540,00 //pll_reg_spi_req_b1=0x0; Address(0x540[7:0])
11577
11578 SPIPoll 0171,0,0,01
11579 SPIRead 0171
11580
11581 //Read pll_reg_spi_a_ack=0x1 (Meaning: );; Address(0x171[7:0])
11582
11583
11584 //END: Requesting/releasing SPI Access to PLL Pages
11585
11586 SPIWrite 0015,00 //digtop=0x0; Address(0x15[7:6])
11587 SPIWrite 0014,ff //txcalib=0xff; Address(0x14[7:0],0x15[7:0])

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11588 SPIWrite 0119,00 //caldac_spare=0x1; Address(0x118[7:0],0x119[7:0],0x11a[7:0])
11589 SPIWrite 0118,01
11590
11591 WAIT 0.1
11592 SPIWrite 0119,00 //caldac_spare=0x0; Address(0x118[7:0],0x119[7:0],0x11a[7:0])
11593 SPIWrite 0118,00
11594
11595 //START: Requesting/releasing SPI Access to PLL Pages
11596
11597 SPIWrite 0014,00 //txcalib=0x0; Address(0x14[7:0],0x15[7:0])
11598 SPIWrite 0015,40 //digtop=0x1; Address(0x15[7:6])
11599 SPIWrite 0170,00 //pll_reg_spi_req_a=0x0; Address(0x170[7:0])
11600 SPIWrite 0540,00 //pll_reg_spi_req_b1=0x0; Address(0x540[7:0])
11601
11602 WAIT 0.2
11603
11604 //END: Requesting/releasing SPI Access to PLL Pages
11605
11606 SPIWrite 0015,00 //digtop=0x0; Address(0x15[7:6])
11607 SPIWrite 0019,f0 //txdig=0xf; Address(0x19[7:4])
11608 SPIWrite 07d3,01 //EnDacDataRandomization=0x1; Address(0x7d3[7:0])
11609 SPIWrite 0019,00 //txdig=0x0; Address(0x19[7:4])
11610 SPIWrite 0019,f0 //txdig=0xf; Address(0x19[7:4])
11611 SPIWrite 0320,00 //dither_freq_shift_ctrl0=0x0; Address(0x320[7:0])
11612 SPIWrite 0019,00 //txdig=0x0; Address(0x19[7:4])
11613 SPIWrite 0013,01 //txdh=0x1; Address(0x13[7:0])
11614 SPIWrite 0107,f0 //po_cg_tm=0xf0000040;
Address(0x104[7:0],0x105[7:0],0x106[7:0],0x107[7:0],0x108[7:0],0x108[3:0],0x109[3:0],0x10
a[7:0])
11615 SPIWrite 0106,00
11616 SPIWrite 0105,00
11617 SPIWrite 0104,40
11618 SPIWrite 010a,00
11619 SPIWrite 0109,00
11620 SPIWrite 0108,00
11621 SPIWrite 0013,02 //txdh=0x2; Address(0x13[7:0])
11622 SPIWrite 0107,f0 //po_cg_tm=0xf0000040;
Address(0x104[7:0],0x105[7:0],0x106[7:0],0x107[7:0],0x108[7:0],0x108[3:0],0x109[3:0],0x10
a[7:0])
11623 SPIWrite 0106,00
11624 SPIWrite 0105,00
11625 SPIWrite 0104,40
11626 SPIWrite 010a,00
11627 SPIWrite 0109,00
11628 SPIWrite 0108,00
11629 SPIWrite 0013,04 //txdh=0x4; Address(0x13[7:0])
11630 SPIWrite 0107,f0 //po_cg_tm=0xf0000040;
Address(0x104[7:0],0x105[7:0],0x106[7:0],0x107[7:0],0x108[7:0],0x108[3:0],0x109[3:0],0x10
a[7:0])
11631 SPIWrite 0106,00
11632 SPIWrite 0105,00
11633 SPIWrite 0104,40
11634 SPIWrite 010a,00
11635 SPIWrite 0109,00
11636 SPIWrite 0108,00
11637 SPIWrite 0013,08 //txdh=0x8; Address(0x13[7:0])
11638 SPIWrite 0107,f0 //po_cg_tm=0xf0000040;
Address(0x104[7:0],0x105[7:0],0x106[7:0],0x107[7:0],0x108[7:0],0x108[3:0],0x109[3:0],0x10
a[7:0])
11639 SPIWrite 0106,00
11640 SPIWrite 0105,00
11641 SPIWrite 0104,40
11642 SPIWrite 010a,00
11643 SPIWrite 0109,00
11644 SPIWrite 0108,00
11645 SPIWrite 0013,0f //txdh=0xf; Address(0x13[7:0])
11646 SPIWrite 0024,00 //data_handoff_mode=0x0; Address(0x24[7:0])
11647 SPIWrite 0013,00 //txdh=0x0; Address(0x13[7:0])
11648 SPIWrite 0019,f0 //txdig=0xf; Address(0x19[7:4])

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11649 SPIWrite 030c,01 //nyq_sel=0x1; Address(0x30c[7:0])
11650 SPIWrite 0019,00 //txdig=0x0; Address(0x19[7:4])
11651 SPIWrite 0013,0f //txdh=0xf; Address(0x13[7:0])
11652 SPIWrite 011a,00 //po_dac1_tm=0x2000; Address(0x118[4:0],0x119[4:0],0x11a[7:0])
11653 SPIWrite 0119,20
11654 SPIWrite 0118,00
11655 SPIWrite 0126,00 //po_dac2_tm=0x2000; Address(0x124[4:0],0x125[4:0],0x126[7:0])
11656 SPIWrite 0125,20
11657 SPIWrite 0124,00
11658 SPIWrite 015a,25 //po_ppa_pdn=0x0; Address(0x15a[7:1])
11659 SPIWrite 0013,00 //txdh=0x0; Address(0x13[7:0])
11660 SPIWrite 0015,80 //timing_controller=0x1; Address(0x15[7:7])
11661 SPIWrite 00fd,01 //config_rise_xx_A_0=0x180;
Address(0xfc[7:0],0xfd[7:0],0xfe[7:0])
11662 SPIWrite 00fc,80
11663 SPIWrite 0101,01 //config_rise_xx_A_1=0x180;
Address(0x100[7:0],0x101[7:0],0x102[7:0])
11664 SPIWrite 0100,80
11665 SPIWrite 019d,01 //config_rise_xx_A_0=0x180;
Address(0x19c[7:0],0x19d[7:0],0x19e[7:0])
11666 SPIWrite 019c,80
11667 SPIWrite 01a1,01 //config_rise_xx_A_1=0x180;
Address(0x1a0[7:0],0x1a1[7:0],0x1a2[7:0])
11668 SPIWrite 01a0,80
11669 SPIWrite 023d,01 //config_rise_xx_A_0=0x180;
Address(0x23c[7:0],0x23d[7:0],0x23e[7:0])
11670 SPIWrite 023c,80
11671 SPIWrite 0241,01 //config_rise_xx_A_1=0x180;
Address(0x240[7:0],0x241[7:0],0x242[7:0])
11672 SPIWrite 0240,80
11673 SPIWrite 02dd,01 //config_rise_xx_A_0=0x180;
Address(0x2dc[7:0],0x2dd[7:0],0x2de[7:0])
11674 SPIWrite 02dc,80
11675 SPIWrite 02e1,01 //config_rise_xx_A_1=0x180;
Address(0x2e0[7:0],0x2e1[7:0],0x2e2[7:0])
11676 SPIWrite 02e0,80
11677 SPIWrite 0135,0c //config_rise_xx_A_14=0xc00;
Address(0x134[7:0],0x135[7:0],0x136[7:0])
11678 SPIWrite 0134,00
11679 SPIWrite 01d5,0c //config_rise_xx_A_14=0xc00;
Address(0x1d4[7:0],0x1d5[7:0],0x1d6[7:0])
11680 SPIWrite 01d4,00
11681 SPIWrite 0275,0c //config_rise_xx_A_14=0xc00;
Address(0x274[7:0],0x275[7:0],0x276[7:0])
11682 SPIWrite 0274,00
11683 SPIWrite 0315,0c //config_rise_xx_A_14=0xc00;
Address(0x314[7:0],0x315[7:0],0x316[7:0])
11684 SPIWrite 0314,00
11685 SPIWrite 0015,00 //timing_controller=0x0; Address(0x15[7:7])
11686 SPIWrite 0013,0f //txdh=0xf; Address(0x13[7:0])
11687 SPIWrite 0167,02 //po_mask_tdd=0x2000000;
Address(0x164[3:0],0x165[3:0],0x166[3:0],0x167[7:0])
11688 SPIWrite 0166,00
11689 SPIWrite 0165,00
11690 SPIWrite 0164,00
11691 SPIWrite 01b1,00 //po_ana_spare5=0x30; Address(0x1b0[7:0],0x1b1[7:0],0x1b2[7:0])
11692 SPIWrite 01b0,30
11693 SPIWrite 0112,01 //po_cml_tm=0x10000; Address(0x110[2:0],0x111[2:0],0x112[7:0])
11694 SPIWrite 0111,00
11695 SPIWrite 0110,00
11696 SPIWrite 0013,00 //txdh=0x0; Address(0x13[7:0])
11697
11698 //END: DAC Analog Writes
11699
11700 SPIWrite 0018,20 //macro=0x1; Address(0x18[7:5])
11701 SPIRead 00f0
11702
11703 //Read MACRO_READY=0x1; Address(0xf0[7:0])
11704

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11705
11706 SPIPoll 00f0,0,0,1
11707
11708 SPIWrite 00a3,0a //MACRO_OPERAND_REG0=0xa040414;
Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
11709 SPIWrite 00a2,04
11710 SPIWrite 00a1,04
11711 SPIWrite 00a0,14
11712 SPIWrite 00a7,1f //MACRO_OPERAND_REG1=0x1f010100;
Address(0xa4[7:0],0xa5[7:0],0xa6[7:0],0xa7[7:0],0xa8[7:0])
11713 SPIWrite 00a6,01
11714 SPIWrite 00a5,01
11715 SPIWrite 00a4,00
11716 SPIWrite 00ab,03 //MACRO_OPERAND_REG2=0x303041f;
Address(0xa8[7:0],0xa9[7:0],0xaa[7:0],0xab[7:0],0xac[7:0])
11717 SPIWrite 00aa,03
11718 SPIWrite 00a9,04
11719 SPIWrite 00a8,1f
11720 SPIWrite 00af,00 //MACRO_OPERAND_REG3=0x101;
Address(0xac[7:0],0xad[7:0],0xae[7:0],0xaf[7:0],0xb0[7:0])
11721 SPIWrite 00ae,00
11722 SPIWrite 00ad,01
11723 SPIWrite 00ac,01
11724 SPIWrite 0193,88 //MACRO_OPCODE=0x88; Address(0x193[7:0],0x194[7:0])
11725
11726 WAIT 0.001
11727 SPIRead 00f0
11728
11729 //Read MACRO_DONE=0x1; Address(0xf0[7:2])
11730
11731
11732 SPIPoll 00f0,2,2,4
11733
11734 SPIRead 00f0
11735
11736 //Read MACRO_ERROR=0x0; Address(0xf0[7:3])
11737
11738 SPIRead 00f1
11739
11740 //Read MACRO_ERROR_OPCODE=0x0; Address(0xf1[7:0],0xf2[7:0])
11741
11742 SPIRead 00f0
11743
11744 //Read MACRO_ERROR_IN_OPCODE=0x0; Address(0xf0[7:4])
11745
11746 SPIRead 00f0
11747
11748 //Read MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0; Address(0xf0[7:5])
11749
11750 SPIRead 00f0
11751
11752 //Read MACRO_ERROR_IN_OPERAND=0x0; Address(0xf0[7:6])
11753
11754 SPIRead 00f0
11755
11756 //Read MACRO_ERROR_IN_EXECUTION=0x0; Address(0xf0[7:7])
11757
11758 SPIRead 00f3
11759 SPIRead 00f2
11760
11761 //Read MACRO_ERROR_EXTENDED_CODE=0x0; Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
11762
11763 SPIRead 00f7
11764 SPIRead 00f6
11765 SPIRead 00f5
11766 SPIRead 00f4
11767
11768 //Read MACRO_ERROR_EXTENDED_CODE_2=0x0;
Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

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11769
11770 SPIRead 00f0
11771
11772 //Read  MACRO_READY=0x1;      Address(0xf0[7:0])
11773
11774
11775 SPIPoll 00f0,0,0,1
11776
11777 SPIWrite 00a3,00      //MACRO_OPERAND_REG0=0x0;
Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
11778 SPIWrite 00a2,00
11779 SPIWrite 00a1,00
11780 SPIWrite 00a0,00
11781 SPIWrite 0193,90      //MACRO_OPCODE=0x90;      Address(0x193[7:0],0x194[7:0])
11782
11783 WAIT 0.001
11784 SPIRead 00f0
11785
11786 //Read  MACRO_DONE=0x1;      Address(0xf0[7:2])
11787
11788
11789 SPIPoll 00f0,2,2,4
11790
11791 SPIRead 00f0
11792
11793 //Read  MACRO_ERROR=0x0;      Address(0xf0[7:3])
11794
11795 SPIRead 00f1
11796
11797 //Read  MACRO_ERROR_OPCODE=0x0;      Address(0xf1[7:0],0xf2[7:0])
11798
11799 SPIRead 00f0
11800
11801 //Read  MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])
11802
11803 SPIRead 00f0
11804
11805 //Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;      Address(0xf0[7:5])
11806
11807 SPIRead 00f0
11808
11809 //Read  MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])
11810
11811 SPIRead 00f0
11812
11813 //Read  MACRO_ERROR_IN_EXECUTION=0x0;  Address(0xf0[7:7])
11814
11815 SPIRead 00f3
11816 SPIRead 00f2
11817
11818 //Read  MACRO_ERROR_EXTENDED_CODE=0x0;  Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
11819
11820 SPIRead 00f7
11821 SPIRead 00f6
11822 SPIRead 00f5
11823 SPIRead 00f4
11824
11825 //Read  MACRO_ERROR_EXTENDED_CODE_2=0x0;
Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
11826
11827 SPIWrite 0144,08      //all_addr_high=0x2;      Address(0x144[7:2])
11828 SPIWrite 0018,00      //macro=0x0;      Address(0x18[7:5])
11829 SPIWrite 0018,08      //cm4top_dram=0x1;  Address(0x18[7:3])
11830 SPIWrite 1f96,00
11831 SPIWrite 0018,00      //cm4top_dram=0x0;  Address(0x18[7:3])
11832 SPIWrite 0018,20      //macro=0x1;      Address(0x18[7:5])
11833 SPIRead 00f0
11834
11835 //Read  MACRO_READY=0x1;      Address(0xf0[7:0])

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11836
11837
11838 SPIPoll 00f0,0,0,1
11839
11840 SPIWrite 00a3,00 //MACRO_OPERAND_REG0=0x1;
Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
11841 SPIWrite 00a2,00
11842 SPIWrite 00a1,00
11843 SPIWrite 00a0,01
11844 SPIWrite 0193,90 //MACRO_OPCODE=0x90; Address(0x193[7:0],0x194[7:0])
11845
11846 WAIT 0.001
11847 SPIRead 00f0
11848
11849 //Read MACRO_DONE=0x1; Address(0xf0[7:2])
11850
11851
11852 SPIPoll 00f0,2,2,4
11853
11854 SPIRead 00f0
11855
11856 //Read MACRO_ERROR=0x0; Address(0xf0[7:3])
11857
11858 SPIRead 00f1
11859
11860 //Read MACRO_ERROR_OPCODE=0x0; Address(0xf1[7:0],0xf2[7:0])
11861
11862 SPIRead 00f0
11863
11864 //Read MACRO_ERROR_IN_OPCODE=0x0; Address(0xf0[7:4])
11865
11866 SPIRead 00f0
11867
11868 //Read MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0; Address(0xf0[7:5])
11869
11870 SPIRead 00f0
11871
11872 //Read MACRO_ERROR_IN_OPERAND=0x0; Address(0xf0[7:6])
11873
11874 SPIRead 00f0
11875
11876 //Read MACRO_ERROR_IN_EXECUTION=0x0; Address(0xf0[7:7])
11877
11878 SPIRead 00f3
11879 SPIRead 00f2
11880
11881 //Read MACRO_ERROR_EXTENDED_CODE=0x0; Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
11882
11883 SPIRead 00f7
11884 SPIRead 00f6
11885 SPIRead 00f5
11886 SPIRead 00f4
11887
11888 //Read MACRO_ERROR_EXTENDED_CODE_2=0x0;
Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
11889
11890
11891 //START: Configuring AUX ADC
11892
11893 SPIWrite 0018,00 //macro=0x0; Address(0x18[7:5])
11894 SPIWrite 0015,02 //ana_4t4r=0x1; Address(0x15[7:1])
11895 SPIWrite 00c0,c0 //EN_CLK_SAR=0x1; Address(0xc0[7:6])
11896 SPIWrite 0015,00 //ana_4t4r=0x0; Address(0x15[7:1])
11897 SPIWrite 0015,40 //digtop=0x1; Address(0x15[7:6])
11898 SPIWrite 0500,01 //auxadc_powerup=0x1; Address(0x500[7:0])
11899 SPIWrite 0500,01 //auxadc_en_conv=0x0; Address(0x500[7:1])
11900 SPIWrite 0500,09 //auxadc_soft_reset=0x1; Address(0x500[7:3])
11901 SPIWrite 0506,01 //auxadc_sar_bit_mode=0x1; Address(0x506[7:0])
11902 SPIWrite 0502,00 //auxadc_INP_MUX=0x0; Address(0x502[7:5])

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11903 SPIWrite 0502,00 //auxadc_INM_MUX=0x0; Address(0x502[7:2])
11904 SPIWrite 0501,08 //auxadc_clk_div=0x1; Address(0x501[7:3])
11905 SPIWrite 0501,0a //auxadc_duty_cycle_clk=0x2; Address(0x501[7:0])
11906 SPIWrite 0508,00 //auxadc_offset_estim_phase_en=0x0; Address(0x508[7:5])
11907 SPIWrite 0505,a0 //auxadc_sar_averaging=0x5; Address(0x505[7:5])
11908 SPIWrite 0505,a1 //auxadc_sar_logic_niter=0x1; Address(0x505[7:0])
11909 SPIWrite 0506,05 //auxadc_inp_buf_chop=0x2; Address(0x506[7:1])
11910 SPIWrite 0506,15 //auxadc_incm_buf_chop=0x2; Address(0x506[7:3])
11911 SPIWrite 0506,15 //auxadc_inp_buf_mux_ctrl=0x0; Address(0x506[7:5])
11912 SPIWrite 0505,a1 //auxadc_sar_logic_state_start=0x0; Address(0x505[7:2])
11913 SPIWrite 0508,00 //auxadc_offset_data_out=0x0; Address(0x508[7:6])
11914 SPIWrite 0508,00 //auxadc_offsetvalue_force_en=0x0; Address(0x508[7:4])
11915 SPIWrite 0503,00 //auxadc_inp_res_term_imeas=0x0; Address(0x503[7:6])
11916 SPIWrite 0502,00 //auxadc_preampl_curr_prog=0x0; Address(0x502[7:0])
11917
11918 WAIT 0.01
11919 SPIWrite 0500,01 //auxadc_soft_reset=0x0; Address(0x500[7:3])
11920
11921 WAIT 0.01
11922 SPIWrite 0500,03 //auxadc_en_conv=0x1; Address(0x500[7:1])
11923
11924 //END: Configuring AUX ADC
11925
11926 SPIWrite 0015,00 //digtop=0x0; Address(0x15[7:6])
11927
11928 //STEP: analogWrites/step2
11929
11930 //START: Removing TDD Pin Overrides.
11931
11932 SPIWrite 0015,80 //timing_controller=0x1; Address(0x15[7:7])
11933 SPIWrite 00ed,0f //reg_for_rxtdd=0xf; Address(0xed[7:0])
11934 SPIWrite 00f5,00 //reg_for_fbtd=0x0; Address(0xf5[7:0])
11935 SPIWrite 00e5,00 //reg_for_txtdd=0x0; Address(0xe5[7:0])
11936
11937 //END: Removing TDD Pin Overrides.
11938
11939 SPIWrite 0015,00 //timing_controller=0x0; Address(0x15[7:7])
11940 SPIWrite 0018,20 //macro=0x1; Address(0x18[7:5])
11941 SPIRead 00f0
11942
11943 //Read MACRO_READY=0x1; Address(0xf0[7:0])
11944
11945
11946 SPIPoll 00f0,0,0,1
11947
11948 SPIWrite 00a3,00 //MACRO_OPERAND_REG0=0x36;
Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
11949 SPIWrite 00a2,00
11950 SPIWrite 00a1,00
11951 SPIWrite 00a0,36
11952 SPIWrite 0193,16 //MACRO_OPCODE=0x16; Address(0x193[7:0],0x194[7:0])
11953
11954 WAIT 0.2
11955 SPIRead 00f0
11956
11957 //Read MACRO_DONE=0x0; Address(0xf0[7:2])
11958
11959 SPIRead 00f0
11960
11961 //Read MACRO_DONE=0x0; Address(0xf0[7:2])
11962
11963 SPIRead 00f0
11964
11965 //Read MACRO_DONE=0x1; Address(0xf0[7:2])
11966
11967
11968 SPIPoll 00f0,2,2,4
11969
11970 SPIRead 00f0

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11971
11972 //Read  MACRO_ERROR=0x0;      Address(0xf0[7:3])
11973
11974 SPIRead 00f1
11975
11976 //Read  MACRO_ERROR_OPCODE=0x0;      Address(0xf1[7:0],0xf2[7:0])
11977
11978 SPIRead 00f0
11979
11980 //Read  MACRO_ERROR_IN_OPCODE=0x0;   Address(0xf0[7:4])
11981
11982 SPIRead 00f0
11983
11984 //Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;      Address(0xf0[7:5])
11985
11986 SPIRead 00f0
11987
11988 //Read  MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])
11989
11990 SPIRead 00f0
11991
11992 //Read  MACRO_ERROR_IN_EXECUTION=0x0;   Address(0xf0[7:7])
11993
11994 SPIRead 00f3
11995 SPIRead 00f2
11996
11997 //Read  MACRO_ERROR_EXTENDED_CODE=0x0;   Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
11998
11999 SPIRead 00f7
12000 SPIRead 00f6
12001 SPIRead 00f5
12002 SPIRead 00f4
12003
12004 //Read  MACRO_ERROR_EXTENDED_CODE_2=0x0;
Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
12005
12006 SPIWrite 0018,00 //macro=0x0;      Address(0x18[7:5])
12007 SPIWrite 0011,3f //ec_ana=0x3f;   Address(0x11[7:0])
12008 SPIWrite 0063,80 //SYNC_DIVBY2_LATCHEDGE_FLIPZ=0x1;   Address(0x63[7:7])
12009 SPIWrite 0067,10 //VREF_PK_DET=0x1;   Address(0x67[7:4])
12010 SPIWrite 0077,0c //PCTRL_CTRL=0x6;    Address(0x77[7:1])
12011 SPIWrite 0076,53 //INVNEG_NF_CTRL=0x5;   Address(0x76[7:4])
12012 SPIWrite 0082,80 //POS_REF_CTRL=0x2;    Address(0x82[7:6])
12013 SPIWrite 0082,a0 //VREF_CTRL=0x4;      Address(0x82[7:3])
12014 SPIWrite 0081,30 //NEG_REF_CTRL=0x3;    Address(0x81[7:4])
12015 SPIWrite 0086,c0 //INV_NF_CTRL=0xe;     Address(0x86[7:5],0x87[7:0])
12016 SPIWrite 0087,01
12017 SPIWrite 0084,85 //INVNEG_PF_CTRL=0x5;   Address(0x84[7:0])
12018 SPIWrite 0087,05 //TRIM_VF_LATP2=0x2;    Address(0x87[7:1])
12019 SPIWrite 00f9,00 //INTR_80N_NL_DITH_DAC_LARGE=0xc;   Address(0xf9[7:7],0xfa[7:0])
12020 SPIWrite 00fa,06
12021 SPIWrite 00e8,80 //CONST_200N_D2S_0=0x4;   Address(0xe8[7:5])
12022 SPIWrite 014e,01 //PRG_V1P4_REG_SP=0x1;   Address(0x14e[7:0])
12023 SPIWrite 014d,1c //PRG_V0P4_REG_SP=0x7;   Address(0x14d[7:2])
12024 SPIWrite 014c,20 //PRG_FLREG_1V=0x4;      Address(0x14c[7:3])
12025 SPIWrite 0138,18 //TM_ANA_DITH_FL=0x3;    Address(0x138[7:3])
12026 SPIWrite 013e,40 //DIS_CM_SW_1P8V=0x1;    Address(0x13e[7:6])
12027 SPIWrite 004a,60 //ITRIM_CORRREFM_BE=0x6;   Address(0x4a[7:4])
12028 SPIWrite 0049,80 //ITRIM_CORRREFP_BE=0x6;   Address(0x49[7:6],0x4a[7:0])
12029 SPIWrite 004a,61
12030 SPIWrite 00c2,c0 //ITRIM_CORRREFM_FE=0x6;   Address(0xc2[7:5])
12031 SPIWrite 00c1,60 //ITRIM_CORRREFP_FE=0x6;   Address(0xc1[7:4])
12032 SPIWrite 00b6,0c //DEL_1V=0x3;           Address(0xb6[7:2])
12033 SPIWrite 004f,0c //DEL_1V=0x3;           Address(0x4f[7:2])
12034 SPIWrite 012e,80 //RES_SER_SEL_REL_1P8=0x7;   Address(0x12e[7:7],0x12f[7:0])
12035 SPIWrite 012f,03
12036 SPIWrite 012e,f0 //RES_SER_SEL_CUST_1P8=0x7;   Address(0x12e[7:4])
12037 SPIWrite 012f,03 //RES_BIAS_SEL_1P8=0x0;     Address(0x12f[7:2])
12038 SPIWrite 0011,00 //ec_ana=0x0;           Address(0x11[7:0])

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12039 SPIWrite 0010,3f //ec_dig=0x3f; Address(0x10[7:0])
12040 SPIWrite 00c1,5a //nl_ana_dith_val=0x5a; Address(0xc1[7:0])
12041 SPIWrite 0078,60 //s2_therm_ms_loop_en=0x0; Address(0x78[7:7])
12042 SPIWrite 00c0,17 //nl_therm_ms_loop_en=0x0; Address(0xc0[7:3])
12043 SPIWrite 00d5,00 //s1_g_pattern_del=0x0; Address(0xd5[7:0])
12044 SPIWrite 00d5,08 //s1_m_pattern_del=0x2; Address(0xd5[7:2])
12045 SPIWrite 0150,30 //dir_pu=0x0; Address(0x150[7:3])
12046 SPIWrite 00f8,51 //calib_seq_avg=0xa8c0c5051;
Address(0xf8[7:0],0xf9[7:0],0xf9[7:0],0xfa[7:0],0xfa[7:0],0xfb[7:0],0xfb[7:0],0xfc[7:0],0
xfc[7:0],0xfd[7:0])
12047 SPIWrite 00f9,50
12048 SPIWrite 00fa,0c
12049 SPIWrite 00fb,8c
12050 SPIWrite 00fc,0a
12051 SPIWrite 0168,02 //freeze_pu=0x1; Address(0x168[7:1])
12052 SPIWrite 00ef,08 //s1_ad_pu_unfreeze_loops=0x0; Address(0xef[7:6])
12053 SPIWrite 0178,71 //dir_corr=0x1; Address(0x178[7:4])
12054 SPIWrite 0075,b5 //s1_sat_del_en=0x1; Address(0x75[7:4])
12055 SPIWrite 0168,06 //reset=0x1; Address(0x168[7:2])
12056 SPIWrite 0168,02 //reset=0x0; Address(0x168[7:2])
12057 SPIWrite 0169,b9 //avg_bg=0xb; Address(0x169[7:0])
12058 SPIWrite 0074,7a //s1_metastab_table_dis=0x0; Address(0x74[7:7])
12059 SPIWrite 013c,fe //dir_lower=0x6bffffe;
Address(0x13c[7:0],0x13d[7:0],0x13d[7:0],0x13e[7:0],0x13e[7:0],0x13f[7:0])
12060 SPIWrite 013d,ff
12061 SPIWrite 013e,6b
12062 SPIWrite 0124,fe //dir_bg=0x6bffffe;
Address(0x124[7:0],0x125[7:0],0x125[7:0],0x126[7:0],0x126[7:0],0x127[7:0])
12063 SPIWrite 0125,ff
12064 SPIWrite 0126,6b
12065 SPIWrite 0129,24 //zone_sel_pu=0x4; Address(0x129[7:0])
12066 SPIWrite 0130,76 //border_checks=0x1; Address(0x130[7:2])
12067 SPIWrite 0130,7e //cycle_zone=0x1; Address(0x130[7:3])
12068 SPIWrite 0010,2f //ec_dig=0x2f; Address(0x10[7:0])
12069 SPIWrite 0044,01 //freeze_all_loops=0x1; Address(0x44[7:0])
12070 SPIWrite 003c,01 //ec_reset=0x1; Address(0x3c[7:0])
12071
12072 WAIT 0.001
12073 SPIWrite 003c,00 //ec_reset=0x0; Address(0x3c[7:0])
12074 SPIWrite 0044,00 //freeze_all_loops=0x0; Address(0x44[7:0])
12075 SPIWrite 00e8,00 //calib_start=0x0; Address(0xe8[7:0])
12076 SPIWrite 00e8,01 //calib_start=0x1; Address(0xe8[7:0])
12077 SPIWrite 0010,00 //ec_dig=0x0; Address(0x10[7:0])
12078 SPIWrite 0015,04 //rx=0x1; Address(0x15[7:2])
12079 SPIWrite 0063,00 //po_common_to_2r_rx_spare_0=0x40000;
Address(0x60[7:0],0x61[7:0],0x62[7:0],0x63[7:0],0x64[7:0])
12080 SPIWrite 0062,04
12081 SPIWrite 0061,00
12082 SPIWrite 0060,00
12083 SPIWrite 0038,b0
12084 SPIWrite 0028,04
12085 SPIWrite 0015,08 //rx=0x2; Address(0x15[7:2])
12086 SPIWrite 0063,00 //po_common_to_2r_rx_spare_0=0x40000;
Address(0x60[7:0],0x61[7:0],0x62[7:0],0x63[7:0],0x64[7:0])
12087 SPIWrite 0062,04
12088 SPIWrite 0061,00
12089 SPIWrite 0060,00
12090 SPIWrite 0038,b0
12091 SPIWrite 0028,04
12092 SPIWrite 0015,00 //rx=0x0; Address(0x15[7:2])
12093 SPIWrite 0015,02 //ana_4t4r=0x1; Address(0x15[7:1])
12094 SPIWrite 006b,00 //po_common_to_pll_spare_1=0x8;
Address(0x68[7:0],0x69[7:0],0x6a[7:0],0x6b[7:0],0x6c[7:0])
12095 SPIWrite 006a,00
12096 SPIWrite 0069,00
12097 SPIWrite 0068,08
12098 SPIWrite 0067,00 //po_common_to_pll_spare_0=0x4000;
Address(0x64[7:0],0x65[7:0],0x66[7:0],0x67[7:0],0x68[7:0])
12099 SPIWrite 0066,00

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12100 SPIWrite 0065,40
12101 SPIWrite 0064,00
12102 SPIWrite 0015,00 //ana_4t4r=0x0; Address(0x15[7:1])
12103 SPIWrite 0012,0f //rxdig=0xf; Address(0x12[7:0])
12104 SPIWrite 20f4,32 //DSAGainRange0=0x32; Address(0x20f4[7:0])
12105 SPIWrite 20f5,32 //DSAGainRange1=0x32; Address(0x20f5[7:0])
12106 SPIWrite 20f6,32 //DSAGainRange2=0x32; Address(0x20f6[7:0])
12107 SPIWrite 20f7,32 //DSAGainRange3=0x32; Address(0x20f7[7:0])
12108 SPIWrite 20f8,32 //DSAGainRange4=0x32; Address(0x20f8[7:0])
12109 SPIWrite 20f9,32 //DSAGainRange5=0x32; Address(0x20f9[7:0])
12110 SPIWrite 0012,00 //rxdig=0x0; Address(0x12[7:0])
12111 SPIWrite 0012,30 //fbdig=0x3; Address(0x12[7:4])
12112 SPIWrite 20f4,32 //DSAGainRange0=0x32; Address(0x20f4[7:0])
12113 SPIWrite 20f5,32 //DSAGainRange1=0x32; Address(0x20f5[7:0])
12114 SPIWrite 20f6,32 //DSAGainRange2=0x32; Address(0x20f6[7:0])
12115 SPIWrite 20f7,32 //DSAGainRange3=0x32; Address(0x20f7[7:0])
12116 SPIWrite 20f8,32 //DSAGainRange4=0x32; Address(0x20f8[7:0])
12117 SPIWrite 20f9,32 //DSAGainRange5=0x32; Address(0x20f9[7:0])
12118 SPIWrite 0012,00 //fbdig=0x0; Address(0x12[7:4])
12119
12120 //STEP: analogWrites/step3
12121
12122 //START: Removing TDD Pin Overrides.
12123
12124 SPIWrite 0015,80 //timing_controller=0x1; Address(0x15[7:7])
12125 SPIWrite 00ed,00 //reg_for_rxtdd=0x0; Address(0xed[7:0])
12126 SPIWrite 00f5,03 //reg_for_fbtdd=0x3; Address(0xf5[7:0])
12127 SPIWrite 00e5,00 //reg_for_txtdd=0x0; Address(0xe5[7:0])
12128
12129 //END: Removing TDD Pin Overrides.
12130
12131 SPIWrite 0015,00 //timing_controller=0x0; Address(0x15[7:7])
12132 SPIWrite 0018,20 //macro=0x1; Address(0x18[7:5])
12133 SPIRead 00f0
12134
12135 //Read MACRO_READY=0x1; Address(0xf0[7:0])
12136
12137
12138 SPIPoll 00f0,0,0,1
12139
12140 SPIWrite 00a3,00 //MACRO_OPERAND_REG0=0x1;
Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
12141 SPIWrite 00a2,00
12142 SPIWrite 00a1,00
12143 SPIWrite 00a0,01
12144 SPIWrite 0193,16 //MACRO_OPCODE=0x16; Address(0x193[7:0],0x194[7:0])
12145
12146 WAIT 0.2
12147 SPIRead 00f0
12148
12149 //Read MACRO_DONE=0x0; Address(0xf0[7:2])
12150
12151 SPIRead 00f0
12152
12153 //Read MACRO_DONE=0x0; Address(0xf0[7:2])
12154
12155 SPIRead 00f0
12156
12157 //Read MACRO_DONE=0x1; Address(0xf0[7:2])
12158
12159
12160 SPIPoll 00f0,2,2,4
12161
12162 SPIRead 00f0
12163
12164 //Read MACRO_ERROR=0x0; Address(0xf0[7:3])
12165
12166 SPIRead 00f1
12167

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12168 //Read  MACRO_ERROR_OPCODE=0x0;      Address(0xf1[7:0],0xf2[7:0])
12169
12170 SPIRead 00f0
12171
12172 //Read  MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])
12173
12174 SPIRead 00f0
12175
12176 //Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;      Address(0xf0[7:5])
12177
12178 SPIRead 00f0
12179
12180 //Read  MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])
12181
12182 SPIRead 00f0
12183
12184 //Read  MACRO_ERROR_IN_EXECUTION=0x0;  Address(0xf0[7:7])
12185
12186 SPIRead 00f3
12187 SPIRead 00f2
12188
12189 //Read  MACRO_ERROR_EXTENDED_CODE=0x0;  Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
12190
12191 SPIRead 00f7
12192 SPIRead 00f6
12193 SPIRead 00f5
12194 SPIRead 00f4
12195
12196 //Read  MACRO_ERROR_EXTENDED_CODE_2=0x0;
Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
12197
12198 SPIWrite 0018,00 //macro=0x0;      Address(0x18[7:5])
12199 SPIWrite 0010,10 //ec_dig=0x10;  Address(0x10[7:0])
12200 SPIWrite 0044,01 //freeze_all_loops=0x1;      Address(0x44[7:0])
12201 SPIWrite 003c,01 //ec_reset=0x1;      Address(0x3c[7:0])
12202 SPIWrite 003c,00 //ec_reset=0x0;      Address(0x3c[7:0])
12203 SPIWrite 0044,00 //freeze_all_loops=0x0;      Address(0x44[7:0])
12204 SPIWrite 00e8,00 //calib_start=0x0;  Address(0xe8[7:0])
12205 SPIWrite 00e8,01 //calib_start=0x1;  Address(0xe8[7:0])
12206 SPIWrite 0010,00 //ec_dig=0x0;      Address(0x10[7:0])
12207
12208 //STEP: analogWrites/step4
12209
12210 //START: PLL Ana Trims
12211
12212
12213 //START: Requesting/releasing SPI Access to PLL Pages
12214
12215 SPIWrite 0015,40 //digtop=0x1;      Address(0x15[7:6])
12216 SPIWrite 0170,01 //pll_reg_spi_req_a=0x1;      Address(0x170[7:0])
12217 SPIWrite 0540,00 //pll_reg_spi_req_b1=0x0;      Address(0x540[7:0])
12218
12219 SPIPoll 0171,0,0,01
12220 SPIRead 0171
12221
12222 //Read  pll_reg_spi_a_ack=0x1 (Meaning: );;  Address(0x171[7:0])
12223
12224
12225 //END: Requesting/releasing SPI Access to PLL Pages
12226
12227 SPIWrite 0015,00 //digtop=0x0;      Address(0x15[7:6])
12228 SPIWrite 0015,01 //pll=0x1;      Address(0x15[7:0])
12229 SPIWrite 005e,01 //ENCLK_CSETAMP=0x1;      Address(0x5e[7:0])
12230 SPIWrite 005d,ec //TRIM_CSETAMP_CUR=0x7;      Address(0x5d[7:5])
12231
12232 //START: Requesting/releasing SPI Access to PLL Pages
12233
12234 SPIWrite 0015,00 //pll=0x0;      Address(0x15[7:0])
12235 SPIWrite 0015,40 //digtop=0x1;      Address(0x15[7:6])

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12236 SPIWrite 0170,00 //pll_reg_spi_req_a=0x0; Address(0x170[7:0])
12237 SPIWrite 0540,00 //pll_reg_spi_req_b1=0x0; Address(0x540[7:0])
12238
12239 WAIT 0.2
12240
12241 //END: Requesting/releasing SPI Access to PLL Pages
12242
12243 SPIWrite 050f,00 //auxadc_cfg3=0xc0000;
Address(0x50c[7:0],0x50d[7:0],0x50e[7:0],0x50f[7:0],0x510[7:0])
12244 SPIWrite 050e,0c
12245 SPIWrite 050d,00
12246 SPIWrite 050c,00
12247 SPIWrite 0015,00 //digtop=0x0; Address(0x15[7:6])
12248 SPIWrite 0015,02 //ana_4t4r=0x1; Address(0x15[7:1])
12249 SPIWrite 00bb,00 //po_txc_interface_control=0x0;
Address(0xb8[7:0],0xb9[7:0],0xba[7:0],0xbb[7:0],0xbc[7:0])
12250 SPIWrite 00ba,00
12251 SPIWrite 00b9,00
12252 SPIWrite 00b8,00
12253 SPIWrite 00bb,00 //po_txc_interface_control=0x8000;
Address(0xb8[7:0],0xb9[7:0],0xba[7:0],0xbb[7:0],0xbc[7:0])
12254 SPIWrite 00ba,00
12255 SPIWrite 00b9,80
12256 SPIWrite 00b8,00
12257 SPIWrite 00bb,00 //po_txc_interface_control=0x0;
Address(0xb8[7:0],0xb9[7:0],0xba[7:0],0xbb[7:0],0xbc[7:0])
12258 SPIWrite 00ba,00
12259 SPIWrite 00b9,00
12260 SPIWrite 00b8,00
12261
12262 WAIT 0.1
12263
12264 //END: PLL Ana Trims
12265
12266 SPIWrite 0015,00 //ana_4t4r=0x0; Address(0x15[7:1])
12267
12268 //STEP: jesdConfig/step0
12269
12270 //START: Configuring JESD Muxes and Pointers
12271
12272
12273 //START: Configuring JESD TX Lane Mux
12274
12275 SPIWrite 0016,10 //jesd_subchip=0x1; Address(0x16[7:4])
12276 SPIWrite 0048,10 //txoctetpath0_sel=0x0; Address(0x48[7:0])
12277 SPIWrite 0048,20 //txoctetpath1_sel=0x2; Address(0x48[7:4])
12278 SPIWrite 0049,31 //txoctetpath2_sel=0x1; Address(0x49[7:0])
12279 SPIWrite 0049,31 //txoctetpath3_sel=0x3; Address(0x49[7:4])
12280 SPIWrite 004a,54 //txoctetpath4_sel=0x4; Address(0x4a[7:0])
12281 SPIWrite 004a,54 //txoctetpath5_sel=0x5; Address(0x4a[7:4])
12282 SPIWrite 004b,76 //txoctetpath6_sel=0x6; Address(0x4b[7:0])
12283 SPIWrite 004b,76 //txoctetpath7_sel=0x7; Address(0x4b[7:4])
12284 SPIWrite 004c,10 //txoctetpath0_clk_sel=0x0; Address(0x4c[7:0])
12285 SPIWrite 004c,20 //txoctetpath1_clk_sel=0x2; Address(0x4c[7:4])
12286 SPIWrite 004d,31 //txoctetpath2_clk_sel=0x1; Address(0x4d[7:0])
12287 SPIWrite 004d,31 //txoctetpath3_clk_sel=0x3; Address(0x4d[7:4])
12288 SPIWrite 004e,54 //txoctetpath4_clk_sel=0x4; Address(0x4e[7:0])
12289 SPIWrite 004e,54 //txoctetpath5_clk_sel=0x5; Address(0x4e[7:4])
12290 SPIWrite 004f,76 //txoctetpath6_clk_sel=0x6; Address(0x4f[7:0])
12291 SPIWrite 004f,76 //txoctetpath7_clk_sel=0x7; Address(0x4f[7:4])
12292
12293 //END: Configuring JESD TX Lane Mux
12294
12295
12296 //START: Configuring JESD RX Lane Mux
12297
12298 SPIWrite 0068,11 //rxoctetpath0_sel=0x1; Address(0x68[7:0])
12299 SPIWrite 0068,31 //rxoctetpath1_sel=0x3; Address(0x68[7:4])
12300 SPIWrite 0069,35 //rxoctetpath2_sel=0x5; Address(0x69[7:0])

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12301 SPIWrite 0069,65 //rxoctetpath3_sel=0x6; Address(0x69[7:4])
12302 SPIWrite 006a,50 //rxoctetpath4_sel=0x0; Address(0x6a[7:0])
12303 SPIWrite 006a,20 //rxoctetpath5_sel=0x2; Address(0x6a[7:4])
12304 SPIWrite 006b,74 //rxoctetpath6_sel=0x4; Address(0x6b[7:0])
12305 SPIWrite 006b,74 //rxoctetpath7_sel=0x7; Address(0x6b[7:4])
12306 SPIWrite 006c,14 //rxoctetpath0_clk_sel=0x4; Address(0x6c[7:0])
12307 SPIWrite 006c,04 //rxoctetpath1_clk_sel=0x0; Address(0x6c[7:4])
12308 SPIWrite 006d,35 //rxoctetpath2_clk_sel=0x5; Address(0x6d[7:0])
12309 SPIWrite 006d,15 //rxoctetpath3_clk_sel=0x1; Address(0x6d[7:4])
12310 SPIWrite 006e,56 //rxoctetpath4_clk_sel=0x6; Address(0x6e[7:0])
12311 SPIWrite 006e,26 //rxoctetpath5_clk_sel=0x2; Address(0x6e[7:4])
12312 SPIWrite 006f,73 //rxoctetpath6_clk_sel=0x3; Address(0x6f[7:0])
12313 SPIWrite 006f,73 //rxoctetpath7_clk_sel=0x7; Address(0x6f[7:4])
12314
12315 //END: Configuring JESD RX Lane Mux
12316
12317
12318 //START: Configuring the DDC-JESD Data Muxes
12319
12320 SPIWrite 0034,00 //mux_sel_rxa_b1_i_for_2r1f_ab=0x0; Address(0x34[7:0])
12321 SPIWrite 0034,00 //mux_sel_rxa_b1_q_for_2r1f_ab=0x0; Address(0x34[7:4])
12322 SPIWrite 0035,22 //mux_sel_rxa_b2_i_for_2r1f_ab=0x2; Address(0x35[7:0])
12323 SPIWrite 0035,22 //mux_sel_rxa_b2_q_for_2r1f_ab=0x2; Address(0x35[7:4])
12324 SPIWrite 0036,44 //mux_sel_rxb_b1_i_for_2r1f_ab=0x4; Address(0x36[7:0])
12325 SPIWrite 0036,44 //mux_sel_rxb_b1_q_for_2r1f_ab=0x4; Address(0x36[7:4])
12326 SPIWrite 0037,66 //mux_sel_rxb_b2_i_for_2r1f_ab=0x6; Address(0x37[7:0])
12327 SPIWrite 0037,66 //mux_sel_rxb_b2_q_for_2r1f_ab=0x6; Address(0x37[7:4])
12328 SPIWrite 0038,40 //mux_sel_rxc_b1_i_for_2r1f_ab=0x0; Address(0x38[7:0])
12329 SPIWrite 0038,00 //mux_sel_rxc_b1_q_for_2r1f_ab=0x0; Address(0x38[7:4])
12330 SPIWrite 0039,52 //mux_sel_rxc_b2_i_for_2r1f_ab=0x2; Address(0x39[7:0])
12331 SPIWrite 0039,22 //mux_sel_rxc_b2_q_for_2r1f_ab=0x2; Address(0x39[7:4])
12332 SPIWrite 003a,64 //mux_sel_rxd_b1_i_for_2r1f_ab=0x4; Address(0x3a[7:0])
12333 SPIWrite 003a,44 //mux_sel_rxd_b1_q_for_2r1f_ab=0x4; Address(0x3a[7:4])
12334 SPIWrite 003b,76 //mux_sel_rxd_b2_i_for_2r1f_ab=0x6; Address(0x3b[7:0])
12335 SPIWrite 003b,66 //mux_sel_rxd_b2_q_for_2r1f_ab=0x6; Address(0x3b[7:4])
12336 SPIWrite 0040,00 //mux_sel_rxc_b1_i_for_2r1f_cd=0x0; Address(0x40[7:0])
12337 SPIWrite 0040,00 //mux_sel_rxc_b1_q_for_2r1f_cd=0x0; Address(0x40[7:4])
12338 SPIWrite 0041,22 //mux_sel_rxc_b2_i_for_2r1f_cd=0x2; Address(0x41[7:0])
12339 SPIWrite 0041,22 //mux_sel_rxc_b2_q_for_2r1f_cd=0x2; Address(0x41[7:4])
12340 SPIWrite 0042,24 //mux_sel_rxd_b1_i_for_2r1f_cd=0x4; Address(0x42[7:0])
12341 SPIWrite 0042,44 //mux_sel_rxd_b1_q_for_2r1f_cd=0x4; Address(0x42[7:4])
12342 SPIWrite 0043,36 //mux_sel_rxd_b2_i_for_2r1f_cd=0x6; Address(0x43[7:0])
12343 SPIWrite 0043,66 //mux_sel_rxd_b2_q_for_2r1f_cd=0x6; Address(0x43[7:4])
12344 SPIWrite 0044,50 //mux_sel_fba_i0_for_2r1f_ab=0x0; Address(0x44[7:0])
12345 SPIWrite 0044,50 //mux_sel_fba_q0_for_2r1f_ab=0x0; Address(0x44[7:2])
12346 SPIWrite 0044,50 //mux_sel_fba_i1_for_2r1f_ab=0x1; Address(0x44[7:4])
12347 SPIWrite 0044,50 //mux_sel_fba_q1_for_2r1f_ab=0x1; Address(0x44[7:6])
12348 SPIWrite 0045,fa //mux_sel_fbc_i0_for_2r1f_ab=0x2; Address(0x45[7:0])
12349 SPIWrite 0045,fa //mux_sel_fbc_q0_for_2r1f_ab=0x2; Address(0x45[7:2])
12350 SPIWrite 0045,fa //mux_sel_fbc_i1_for_2r1f_ab=0x3; Address(0x45[7:4])
12351 SPIWrite 0045,fa //mux_sel_fbc_q1_for_2r1f_ab=0x3; Address(0x45[7:6])
12352 SPIWrite 0046,fa //mux_sel_fba_i0_for_2r1f_cd=0x2; Address(0x46[7:0])
12353 SPIWrite 0046,fa //mux_sel_fba_q0_for_2r1f_cd=0x2; Address(0x46[7:2])
12354 SPIWrite 0046,fa //mux_sel_fba_i1_for_2r1f_cd=0x3; Address(0x46[7:4])
12355 SPIWrite 0046,fa //mux_sel_fba_q1_for_2r1f_cd=0x3; Address(0x46[7:6])
12356 SPIWrite 0047,50 //mux_sel_fbc_i0_for_2r1f_cd=0x0; Address(0x47[7:0])
12357 SPIWrite 0047,50 //mux_sel_fbc_q0_for_2r1f_cd=0x0; Address(0x47[7:2])
12358 SPIWrite 0047,50 //mux_sel_fbc_i1_for_2r1f_cd=0x1; Address(0x47[7:4])
12359 SPIWrite 0047,50 //mux_sel_fbc_q1_for_2r1f_cd=0x1; Address(0x47[7:6])
12360
12361 //END: Configuring the DDC-JESD Data Muxes
12362
12363
12364 //START: Configuring the JESD-DUC Data Muxes
12365
12366 SPIWrite 00cc,00 //mux_sel_for_txa_b0_i=0x0; Address(0xcc[7:0])
12367 SPIWrite 00cc,00 //mux_sel_for_txa_b0_q=0x0; Address(0xcc[7:4])
12368 SPIWrite 00cd,11 //mux_sel_for_txa_b1_i=0x1; Address(0xcd[7:0])
12369 SPIWrite 00cd,11 //mux_sel_for_txa_b1_q=0x1; Address(0xcd[7:4])

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12370 SPIWrite 00ce,22 //mux_sel_for_txb_b0_i=0x2; Address(0xce[7:0])
12371 SPIWrite 00ce,22 //mux_sel_for_txb_b0_q=0x2; Address(0xce[7:4])
12372 SPIWrite 00cf,33 //mux_sel_for_txb_b1_i=0x3; Address(0xcf[7:0])
12373 SPIWrite 00cf,33 //mux_sel_for_txb_b1_q=0x3; Address(0xcf[7:4])
12374 SPIWrite 00d0,48 //mux_sel_for_txc_b0_i=0x8; Address(0xd0[7:0])
12375 SPIWrite 00d0,88 //mux_sel_for_txc_b0_q=0x8; Address(0xd0[7:4])
12376 SPIWrite 00d1,59 //mux_sel_for_txc_b1_i=0x9; Address(0xd1[7:0])
12377 SPIWrite 00d1,99 //mux_sel_for_txc_b1_q=0x9; Address(0xd1[7:4])
12378 SPIWrite 00d2,6a //mux_sel_for_txd_b0_i=0xa; Address(0xd2[7:0])
12379 SPIWrite 00d2,aa //mux_sel_for_txd_b0_q=0xa; Address(0xd2[7:4])
12380 SPIWrite 00d3,7b //mux_sel_for_txd_b1_i=0xb; Address(0xd3[7:0])
12381 SPIWrite 00d3,bb //mux_sel_for_txd_b1_q=0xb; Address(0xd3[7:4])
12382 SPIWrite 0060,10 //mux_sel_for_txa_ctrl=0x0; Address(0x60[7:0])
12383 SPIWrite 0060,10 //mux_sel_for_txb_ctrl=0x1; Address(0x60[7:4])
12384 SPIWrite 0061,34 //mux_sel_for_txc_ctrl=0x4; Address(0x61[7:0])
12385 SPIWrite 0061,54 //mux_sel_for_txd_ctrl=0x5; Address(0x61[7:4])
12386
12387 //END: Configuring the JESD-DUC Data Muxes
12388
12389
12390 //START: Configuring JESD TX Sync Mux
12391
12392 SPIWrite 0054,00 //adc_jesd_sync_n0_mux_sel=0x0; Address(0x54[7:0])
12393 SPIWrite 0054,00 //adc_jesd_sync_n1_mux_sel=0x0; Address(0x54[7:4])
12394 SPIWrite 0055,30 //adc_jesd_sync_n2_mux_sel=0x0; Address(0x55[7:0])
12395 SPIWrite 0055,00 //adc_jesd_sync_n3_mux_sel=0x0; Address(0x55[7:4])
12396 SPIWrite 0056,50 //adc_jesd_sync_n4_mux_sel=0x0; Address(0x56[7:0])
12397 SPIWrite 0056,00 //adc_jesd_sync_n5_mux_sel=0x0; Address(0x56[7:4])
12398
12399 //END: Configuring JESD TX Sync Mux
12400
12401
12402 //START: Configuring JESD RX Sync Mux
12403
12404 SPIWrite 00ca,e4 //dac_jesd_sync_n0_mux_sel=0x0; Address(0xca[7:0])
12405 SPIWrite 00ca,e0 //dac_jesd_sync_n1_mux_sel=0x0; Address(0xca[7:2])
12406 SPIWrite 00ca,c0 //dac_jesd_sync_n2_mux_sel=0x0; Address(0xca[7:4])
12407 SPIWrite 00ca,00 //dac_jesd_sync_n3_mux_sel=0x0; Address(0xca[7:6])
12408
12409 //END: Configuring JESD RX Sync Mux
12410
12411 SPIWrite 009c,03 //rx_clk_dithered_mode_en=0x1; Address(0x9c[7:1])
12412 SPIWrite 009e,03 //fb_clk_dithered_mode_en=0x1; Address(0x9e[7:1])
12413 SPIWrite 009c,03 //rx_clk_disable=0x1; Address(0x9c[7:0])
12414 SPIWrite 00a0,02 //tx_clk_disable=0x0; Address(0xa0[7:0])
12415 SPIWrite 00a0,00 //tx_clk_dithered_mode_en=0x0; Address(0xa0[7:1])
12416
12417 //END: Configuring JESD Muxes and Pointers
12418
12419
12420 //START: Setting JESD SyncB Pin Mode
12421
12422
12423 //END: Setting JESD SyncB Pin Mode
12424
12425 SPIWrite 0016,00 //jesd_subchip=0x0; Address(0x16[7:4])
12426
12427 //STEP: jesdConfig/step1
12428
12429 //START: Configuring ADC JESD TX
12430
12431 SPIWrite 0016,01 //adc_jesd=0x1; Address(0x16[7:0])
12432 SPIWrite 006d,07 //link0_init_state=0x1; Address(0x6d[7:0])
12433 SPIWrite 006d,07 //link1_init_state=0x1; Address(0x6d[7:1])
12434 SPIWrite 006d,07 //link2_init_state=0x1; Address(0x6d[7:2])
12435 SPIWrite 006f,02 //init_state_gearbox_spi_ovr=0x1; Address(0x6f[7:1])
12436 SPIWrite 006c,0f //lane0_gearbox_init_state=0x1; Address(0x6c[7:0])
12437 SPIWrite 006c,0f //lane1_gearbox_init_state=0x1; Address(0x6c[7:1])
12438 SPIWrite 006c,0f //lane2_gearbox_init_state=0x1; Address(0x6c[7:2])

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12439 SPIWrite 006c,0f //lane3_gearbox_init_state=0x1; Address(0x6c[7:3])
12440 SPIWrite 006c,0e //lane0_gearbox_init_state=0x0; Address(0x6c[7:0])
12441 SPIWrite 006c,0c //lane1_gearbox_init_state=0x0; Address(0x6c[7:1])
12442 SPIWrite 006c,08 //lane2_gearbox_init_state=0x0; Address(0x6c[7:2])
12443 SPIWrite 006c,00 //lane3_gearbox_init_state=0x0; Address(0x6c[7:3])
12444 SPIWrite 006e,0f //lane0_serdes_fifo_init_state=0x1; Address(0x6e[7:0])
12445 SPIWrite 006e,0f //lane1_serdes_fifo_init_state=0x1; Address(0x6e[7:1])
12446 SPIWrite 006e,0f //lane2_serdes_fifo_init_state=0x1; Address(0x6e[7:2])
12447 SPIWrite 006e,0f //lane3_serdes_fifo_init_state=0x1; Address(0x6e[7:3])
12448 SPIWrite 005c,1f //rx_root_clk_dither_en=0x1; Address(0x5c[7:0])
12449 SPIWrite 005c,1f //fb_root_clk_dither_en=0x1; Address(0x5c[7:1])
12450 SPIWrite 005c,1b //ddc_rd_clk_dither_en=0x0; Address(0x5c[7:2])
12451 SPIWrite 005c,13 //jesd_clk_dither_en=0x0; Address(0x5c[7:3])
12452 SPIWrite 005c,03 //jesd_clk_div2_dither_en=0x0; Address(0x5c[7:4])
12453 SPIWrite 0021,01 //jesd_system_mode=0x1; Address(0x21[7:0])
12454 SPIWrite 005d,01 //rx_adc_clk_sysref_mux=0x1; Address(0x5d[7:0])
12455 SPIWrite 005d,01 //fb_adc_clk_sysref_mux=0x0; Address(0x5d[7:1])
12456 SPIWrite 0024,0f //jesd_clear_data=0xf; Address(0x24[7:0])
12457 SPIWrite 0069,8c //serdes_fifo_read_dly_lane0=0xc; Address(0x69[7:0])
12458 SPIWrite 0069,cc //serdes_fifo_read_dly_lane1=0xc; Address(0x69[7:4])
12459 SPIWrite 006a,8c //serdes_fifo_read_dly_lane2=0xc; Address(0x6a[7:0])
12460 SPIWrite 006a,cc //serdes_fifo_read_dly_lane3=0xc; Address(0x6a[7:4])
12461 SPIWrite 0040,01 //rx1_root_clk_div_m=0x1; Address(0x40[7:0])
12462 SPIWrite 0041,00 //rx1_root_clk_div_n_m1=0x0; Address(0x41[7:0])
12463 SPIWrite 0046,01 //ddc_rd_clk_rx1_div_m=0x1; Address(0x46[7:0])
12464 SPIWrite 0047,03 //ddc_rd_clk_rx1_div_n_m1=0x3; Address(0x47[7:0])
12465 SPIWrite 004c,01 //jesd_clk_rx1_div_m=0x1; Address(0x4c[7:0])
12466 SPIWrite 004d,00 //jesd_clk_rx1_div_n_m1=0x0; Address(0x4d[7:0])
12467 SPIWrite 0034,14 //rx1_jesd_mode=0x14; Address(0x34[7:0])
12468 SPIWrite 0084,00 //link0_k_m1=0x0; Address(0x84[7:0],0x85[7:0])
12469 SPIWrite 0079,00 //link0_ila_k_m1=0x0; Address(0x79[7:0],0x7a[7:0])
12470 SPIWrite 0042,01 //rx2_root_clk_div_m=0x1; Address(0x42[7:0])
12471 SPIWrite 0043,00 //rx2_root_clk_div_n_m1=0x0; Address(0x43[7:0])
12472 SPIWrite 0048,01 //ddc_rd_clk_rx2_div_m=0x1; Address(0x48[7:0])
12473 SPIWrite 0049,03 //ddc_rd_clk_rx2_div_n_m1=0x3; Address(0x49[7:0])
12474 SPIWrite 004e,01 //jesd_clk_rx2_div_m=0x1; Address(0x4e[7:0])
12475 SPIWrite 004f,00 //jesd_clk_rx2_div_n_m1=0x0; Address(0x4f[7:0])
12476 SPIWrite 0035,14 //rx2_jesd_mode=0x14; Address(0x35[7:0])
12477 SPIWrite 009c,00 //link1_k_m1=0x0; Address(0x9c[7:0],0x9d[7:0])
12478 SPIWrite 0091,00 //link1_ila_k_m1=0x0; Address(0x91[7:0],0x92[7:0])
12479 SPIWrite 0044,01 //fb_root_clk_div_m=0x1; Address(0x44[7:0])
12480 SPIWrite 0045,00 //fb_root_clk_div_n_m1=0x0; Address(0x45[7:0])
12481 SPIWrite 004a,01 //ddc_rd_clk_fb_div_m=0x1; Address(0x4a[7:0])
12482 SPIWrite 004b,03 //ddc_rd_clk_fb_div_n_m1=0x3; Address(0x4b[7:0])
12483 SPIWrite 0050,01 //jesd_clk_fb_div_m=0x1; Address(0x50[7:0])
12484 SPIWrite 0051,00 //jesd_clk_fb_div_n_m1=0x0; Address(0x51[7:0])
12485 SPIWrite 0036,0b //fb_jesd_mode=0xb; Address(0x36[7:0])
12486 SPIWrite 00b4,00 //link2_k_m1=0x0; Address(0xb4[7:0],0xb5[7:0])
12487 SPIWrite 00a9,00 //link2_ila_k_m1=0x0; Address(0xa9[7:0],0xaa[7:0])
12488 SPIWrite 0020,02 //jesd_std_sel=0x2; Address(0x20[7:0])
12489 SPIWrite 0077,01 //link0_scr=0x0; Address(0x77[7:7])
12490 SPIWrite 008f,01 //link1_scr=0x0; Address(0x8f[7:7])
12491 SPIWrite 00a7,01 //link2_scr=0x0; Address(0xa7[7:7])
12492 SPIWrite 0023,05 //lane_ena=0x5; Address(0x23[7:0])
12493 SPIWrite 003c,02 //sel_rx1_jesd_mode_1s_2s_ovr=0x1; Address(0x3c[7:1])
12494 SPIWrite 003c,02 //sel_rx1_jesd_mode_1s_2s_val=0x0; Address(0x3c[7:0])
12495 SPIWrite 003c,0a //sel_rx2_jesd_mode_1s_2s_ovr=0x1; Address(0x3c[7:3])
12496 SPIWrite 003c,0a //sel_rx2_jesd_mode_1s_2s_val=0x0; Address(0x3c[7:2])
12497 SPIWrite 003c,2a //sel_fb_jesd_mode_1s_2s_ovr=0x1; Address(0x3c[7:5])
12498 SPIWrite 003c,3a //sel_fb_jesd_mode_1s_2s_val=0x1; Address(0x3c[7:4])
12499 SPIWrite 0083,01 //link0_jesd_ila_config_override=0x1; Address(0x83[7:0])
12500 SPIWrite 009b,01 //link1_jesd_ila_config_override=0x1; Address(0x9b[7:0])
12501 SPIWrite 0078,0f //link0_ila_f_m1=0xf; Address(0x78[7:0],0x79[7:0])
12502 SPIWrite 0090,0f //link1_ila_f_m1=0xf; Address(0x90[7:0],0x91[7:0])
12503 SPIWrite 00a8,07 //link2_ila_f_m1=0x7; Address(0xa8[7:0],0xa9[7:0])
12504 SPIWrite 007a,07 //link0_ila_m_m1=0x7; Address(0x7a[7:0],0x7b[7:0])
12505 SPIWrite 0092,07 //link1_ila_m_m1=0x7; Address(0x92[7:0],0x93[7:0])
12506 SPIWrite 00aa,01 //link2_ila_m_m1=0x1; Address(0xaa[7:0],0xab[7:0])
12507 SPIWrite 0077,03 //link0_ila_l_m1=0x3; Address(0x77[7:0])
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12508 SPIWrite 008f,03 //link1_ila_l_m1=0x3; Address(0x8f[7:0])
12509 SPIWrite 00a7,01 //link2_ila_l_m1=0x1; Address(0xa7[7:0])
12510 SPIWrite 007b,0f //link0_ila_n_m1=0xf; Address(0x7b[7:0])
12511 SPIWrite 0093,0f //link1_ila_n_m1=0xf; Address(0x93[7:0])
12512 SPIWrite 00ab,0f //link2_ila_n_m1=0xf; Address(0xab[7:0])
12513 SPIWrite 00bc,00 //lid0=0x0; Address(0xbc[7:0])
12514 SPIWrite 00bd,01 //lid1=0x1; Address(0xbd[7:0])
12515 SPIWrite 00be,02 //lid2=0x2; Address(0xbe[7:0])
12516 SPIWrite 00bf,03 //lid3=0x3; Address(0xbf[7:0])
12517 SPIWrite 00e4,42 //msf_rx1_offset_default_mode0=0x2; Address(0xe4[7:0])
12518 SPIWrite 00e4,22 //msf_rx1_offset_default_mode1=0x2; Address(0xe4[7:4])
12519 SPIWrite 00e5,83 //msf_rx1_offset_default_mode2=0x3; Address(0xe5[7:0])
12520 SPIWrite 00e5,43 //msf_rx1_offset_default_mode3=0x4; Address(0xe5[7:4])
12521 SPIWrite 00e6,42 //msf_rx2_offset_default_mode0=0x2; Address(0xe6[7:0])
12522 SPIWrite 00e6,22 //msf_rx2_offset_default_mode1=0x2; Address(0xe6[7:4])
12523 SPIWrite 00e7,83 //msf_rx2_offset_default_mode2=0x3; Address(0xe7[7:0])
12524 SPIWrite 00e7,43 //msf_rx2_offset_default_mode3=0x4; Address(0xe7[7:4])
12525 SPIWrite 00e8,42 //msf_fb_offset_default_mode0=0x2; Address(0xe8[7:0])
12526 SPIWrite 00e8,22 //msf_fb_offset_default_mode1=0x2; Address(0xe8[7:4])
12527 SPIWrite 00e9,83 //msf_fb_offset_default_mode2=0x3; Address(0xe9[7:0])
12528 SPIWrite 00e9,43 //msf_fb_offset_default_mode3=0x4; Address(0xe9[7:4])
12529 SPIWrite 0037,06 //rx1_ctrlmode_12b_trunc_en=0x0; Address(0x37[7:0])
12530 SPIWrite 0037,04 //rx2_ctrlmode_12b_trunc_en=0x0; Address(0x37[7:1])
12531 SPIWrite 0037,00 //fb_ctrlmode_12b_trunc_en=0x0; Address(0x37[7:2])
12532
12533 //END: Done Configuring ADC JESD TX
12534
12535
12536 //START: Configuring ADC JESD TX
12537
12538 SPIWrite 0016,02 //adc_jesd=0x2; Address(0x16[7:0])
12539 SPIWrite 006d,07 //link0_init_state=0x1; Address(0x6d[7:0])
12540 SPIWrite 006d,07 //link1_init_state=0x1; Address(0x6d[7:1])
12541 SPIWrite 006d,07 //link2_init_state=0x1; Address(0x6d[7:2])
12542 SPIWrite 006f,02 //init_state_gearbox_spi_ovr=0x1; Address(0x6f[7:1])
12543 SPIWrite 006c,0f //lane0_gearbox_init_state=0x1; Address(0x6c[7:0])
12544 SPIWrite 006c,0f //lane1_gearbox_init_state=0x1; Address(0x6c[7:1])
12545 SPIWrite 006c,0f //lane2_gearbox_init_state=0x1; Address(0x6c[7:2])
12546 SPIWrite 006c,0f //lane3_gearbox_init_state=0x1; Address(0x6c[7:3])
12547 SPIWrite 006c,0e //lane0_gearbox_init_state=0x0; Address(0x6c[7:0])
12548 SPIWrite 006c,0c //lane1_gearbox_init_state=0x0; Address(0x6c[7:1])
12549 SPIWrite 006c,08 //lane2_gearbox_init_state=0x0; Address(0x6c[7:2])
12550 SPIWrite 006c,00 //lane3_gearbox_init_state=0x0; Address(0x6c[7:3])
12551 SPIWrite 006e,0f //lane0_serdes_fifo_init_state=0x1; Address(0x6e[7:0])
12552 SPIWrite 006e,0f //lane1_serdes_fifo_init_state=0x1; Address(0x6e[7:1])
12553 SPIWrite 006e,0f //lane2_serdes_fifo_init_state=0x1; Address(0x6e[7:2])
12554 SPIWrite 006e,0f //lane3_serdes_fifo_init_state=0x1; Address(0x6e[7:3])
12555 SPIWrite 005c,1f //rx_root_clk_dither_en=0x1; Address(0x5c[7:0])
12556 SPIWrite 005c,1f //fb_root_clk_dither_en=0x1; Address(0x5c[7:1])
12557 SPIWrite 005c,1b //ddc_rd_clk_dither_en=0x0; Address(0x5c[7:2])
12558 SPIWrite 005c,13 //jesd_clk_dither_en=0x0; Address(0x5c[7:3])
12559 SPIWrite 005c,03 //jesd_clk_div2_dither_en=0x0; Address(0x5c[7:4])
12560 SPIWrite 0021,01 //jesd_system_mode=0x1; Address(0x21[7:0])
12561 SPIWrite 005d,01 //rx_adc_clk_sysref_mux=0x1; Address(0x5d[7:0])
12562 SPIWrite 005d,01 //fb_adc_clk_sysref_mux=0x0; Address(0x5d[7:1])
12563 SPIWrite 0024,0f //jesd_clear_data=0xf; Address(0x24[7:0])
12564 SPIWrite 0069,8c //serdes_fifo_read_dly_lane0=0xc; Address(0x69[7:0])
12565 SPIWrite 0069,cc //serdes_fifo_read_dly_lane1=0xc; Address(0x69[7:4])
12566 SPIWrite 006a,8c //serdes_fifo_read_dly_lane2=0xc; Address(0x6a[7:0])
12567 SPIWrite 006a,cc //serdes_fifo_read_dly_lane3=0xc; Address(0x6a[7:4])
12568 SPIWrite 0040,01 //rx1_root_clk_div_m=0x1; Address(0x40[7:0])
12569 SPIWrite 0041,00 //rx1_root_clk_div_n_m1=0x0; Address(0x41[7:0])
12570 SPIWrite 0046,01 //ddc_rd_clk_rx1_div_m=0x1; Address(0x46[7:0])
12571 SPIWrite 0047,03 //ddc_rd_clk_rx1_div_n_m1=0x3; Address(0x47[7:0])
12572 SPIWrite 004c,01 //jesd_clk_rx1_div_m=0x1; Address(0x4c[7:0])
12573 SPIWrite 004d,00 //jesd_clk_rx1_div_n_m1=0x0; Address(0x4d[7:0])
12574 SPIWrite 0034,14 //rx1_jesd_mode=0x14; Address(0x34[7:0])
12575 SPIWrite 0084,00 //link0_k_m1=0x0; Address(0x84[7:0],0x85[7:0])
12576 SPIWrite 0079,00 //link0_ila_k_m1=0x0; Address(0x79[7:0],0x7a[7:0])

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12577 SPIWrite 0042,01 //rx2_root_clk_div_m=0x1; Address(0x42[7:0])
12578 SPIWrite 0043,00 //rx2_root_clk_div_n_m1=0x0; Address(0x43[7:0])
12579 SPIWrite 0048,01 //ddc_rd_clk_rx2_div_m=0x1; Address(0x48[7:0])
12580 SPIWrite 0049,03 //ddc_rd_clk_rx2_div_n_m1=0x3; Address(0x49[7:0])
12581 SPIWrite 004e,01 //jesd_clk_rx2_div_m=0x1; Address(0x4e[7:0])
12582 SPIWrite 004f,00 //jesd_clk_rx2_div_n_m1=0x0; Address(0x4f[7:0])
12583 SPIWrite 0035,14 //rx2_jesd_mode=0x14; Address(0x35[7:0])
12584 SPIWrite 009c,00 //link1_k_m1=0x0; Address(0x9c[7:0],0x9d[7:0])
12585 SPIWrite 0091,00 //link1_ila_k_m1=0x0; Address(0x91[7:0],0x92[7:0])
12586 SPIWrite 0044,01 //fb_root_clk_div_m=0x1; Address(0x44[7:0])
12587 SPIWrite 0045,00 //fb_root_clk_div_n_m1=0x0; Address(0x45[7:0])
12588 SPIWrite 004a,01 //ddc_rd_clk_fb_div_m=0x1; Address(0x4a[7:0])
12589 SPIWrite 004b,03 //ddc_rd_clk_fb_div_n_m1=0x3; Address(0x4b[7:0])
12590 SPIWrite 0050,01 //jesd_clk_fb_div_m=0x1; Address(0x50[7:0])
12591 SPIWrite 0051,00 //jesd_clk_fb_div_n_m1=0x0; Address(0x51[7:0])
12592 SPIWrite 0036,0b //fb_jesd_mode=0xb; Address(0x36[7:0])
12593 SPIWrite 00b4,00 //link2_k_m1=0x0; Address(0xb4[7:0],0xb5[7:0])
12594 SPIWrite 00a9,00 //link2_ila_k_m1=0x0; Address(0xa9[7:0],0xaa[7:0])
12595 SPIWrite 0020,02 //jesd_std_sel=0x2; Address(0x20[7:0])
12596 SPIWrite 0077,01 //link0_scr=0x0; Address(0x77[7:7])
12597 SPIWrite 008f,01 //link1_scr=0x0; Address(0x8f[7:7])
12598 SPIWrite 00a7,01 //link2_scr=0x0; Address(0xa7[7:7])
12599 SPIWrite 0023,00 //lane_ena=0x0; Address(0x23[7:0])
12600 SPIWrite 003c,02 //sel_rx1_jesd_mode_1s_2s_ovr=0x1; Address(0x3c[7:1])
12601 SPIWrite 003c,02 //sel_rx1_jesd_mode_1s_2s_val=0x0; Address(0x3c[7:0])
12602 SPIWrite 003c,0a //sel_rx2_jesd_mode_1s_2s_ovr=0x1; Address(0x3c[7:3])
12603 SPIWrite 003c,0a //sel_rx2_jesd_mode_1s_2s_val=0x0; Address(0x3c[7:2])
12604 SPIWrite 003c,2a //sel_fb_jesd_mode_1s_2s_ovr=0x1; Address(0x3c[7:5])
12605 SPIWrite 003c,3a //sel_fb_jesd_mode_1s_2s_val=0x1; Address(0x3c[7:4])
12606 SPIWrite 0083,01 //link0_jesd_ila_config_override=0x1; Address(0x83[7:0])
12607 SPIWrite 009b,01 //link1_jesd_ila_config_override=0x1; Address(0x9b[7:0])
12608 SPIWrite 0078,0f //link0_ila_f_m1=0xf; Address(0x78[7:0],0x79[7:0])
12609 SPIWrite 0090,0f //link1_ila_f_m1=0xf; Address(0x90[7:0],0x91[7:0])
12610 SPIWrite 00a8,07 //link2_ila_f_m1=0x7; Address(0xa8[7:0],0xa9[7:0])
12611 SPIWrite 007a,07 //link0_ila_m_m1=0x7; Address(0x7a[7:0],0x7b[7:0])
12612 SPIWrite 0092,07 //link1_ila_m_m1=0x7; Address(0x92[7:0],0x93[7:0])
12613 SPIWrite 00aa,01 //link2_ila_m_m1=0x1; Address(0xaa[7:0],0xab[7:0])
12614 SPIWrite 0077,03 //link0_ila_l_m1=0x3; Address(0x77[7:0])
12615 SPIWrite 008f,03 //link1_ila_l_m1=0x3; Address(0x8f[7:0])
12616 SPIWrite 00a7,01 //link2_ila_l_m1=0x1; Address(0xa7[7:0])
12617 SPIWrite 007b,0f //link0_ila_n_m1=0xf; Address(0x7b[7:0])
12618 SPIWrite 0093,0f //link1_ila_n_m1=0xf; Address(0x93[7:0])
12619 SPIWrite 00ab,0f //link2_ila_n_m1=0xf; Address(0xab[7:0])
12620 SPIWrite 00bc,04 //lid0=0x4; Address(0xbc[7:0])
12621 SPIWrite 00bd,05 //lid1=0x5; Address(0xbd[7:0])
12622 SPIWrite 00be,06 //lid2=0x6; Address(0xbe[7:0])
12623 SPIWrite 00bf,07 //lid3=0x7; Address(0xbf[7:0])
12624 SPIWrite 00e4,42 //msf_rx1_offset_default_mode0=0x2; Address(0xe4[7:0])
12625 SPIWrite 00e4,22 //msf_rx1_offset_default_mode1=0x2; Address(0xe4[7:4])
12626 SPIWrite 00e5,83 //msf_rx1_offset_default_mode2=0x3; Address(0xe5[7:0])
12627 SPIWrite 00e5,43 //msf_rx1_offset_default_mode3=0x4; Address(0xe5[7:4])
12628 SPIWrite 00e6,42 //msf_rx2_offset_default_mode0=0x2; Address(0xe6[7:0])
12629 SPIWrite 00e6,22 //msf_rx2_offset_default_mode1=0x2; Address(0xe6[7:4])
12630 SPIWrite 00e7,83 //msf_rx2_offset_default_mode2=0x3; Address(0xe7[7:0])
12631 SPIWrite 00e7,43 //msf_rx2_offset_default_mode3=0x4; Address(0xe7[7:4])
12632 SPIWrite 00e8,42 //msf_fb_offset_default_mode0=0x2; Address(0xe8[7:0])
12633 SPIWrite 00e8,22 //msf_fb_offset_default_mode1=0x2; Address(0xe8[7:4])
12634 SPIWrite 00e9,83 //msf_fb_offset_default_mode2=0x3; Address(0xe9[7:0])
12635 SPIWrite 00e9,43 //msf_fb_offset_default_mode3=0x4; Address(0xe9[7:4])
12636 SPIWrite 0037,06 //rx1_ctrlmode_12b_trunc_en=0x0; Address(0x37[7:0])
12637 SPIWrite 0037,04 //rx2_ctrlmode_12b_trunc_en=0x0; Address(0x37[7:1])
12638 SPIWrite 0037,00 //fb_ctrlmode_12b_trunc_en=0x0; Address(0x37[7:2])
12639
12640 //END: Done Configuring ADC JESD TX
12641
12642 SPIWrite 0016,00 //adc_jesd=0x0; Address(0x16[7:0])
12643
12644 //STEP: jesdConfig/step2
12645

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12646 //START: Configuring DAC JESD RX
12647
12648 SPIWrite 0016,04 //dac_jesd=0x1; Address(0x16[7:2])
12649 SPIWrite 006c,00 //link0_k_m1=0x0; Address(0x6c[7:0],0x6d[7:0])
12650 SPIWrite 006d,00 //link1_k_m1=0x0; Address(0x6d[7:0],0x6e[7:0])
12651 SPIWrite 0057,00 //link1_ila_k_m1=0x0; Address(0x57[7:0],0x58[7:0])
12652 SPIWrite 0049,00 //link0_ila_k_m1=0x0; Address(0x49[7:0],0x4a[7:0])
12653 SPIWrite 0069,00 //link0_rbd_m1=0x3; Address(0x68[7:0],0x69[7:0],0x6a[7:0])
12654 SPIWrite 0068,03
12655 SPIWrite 006b,00 //link1_rbd_m1=0x3; Address(0x6a[7:0],0x6b[7:0],0x6c[7:0])
12656 SPIWrite 006a,03
12657 SPIWrite 0024,5e //gearbox_init_state_ovr=0x1; Address(0x24[7:6])
12658 SPIWrite 0025,ff //gearbox_init_state_lane0_val=0x1; Address(0x25[7:0])
12659 SPIWrite 0025,ff //gearbox_init_state_lane1_val=0x1; Address(0x25[7:1])
12660 SPIWrite 0025,ff //gearbox_init_state_lane2_val=0x1; Address(0x25[7:2])
12661 SPIWrite 0025,ff //gearbox_init_state_lane3_val=0x1; Address(0x25[7:3])
12662 SPIWrite 0025,fe //gearbox_init_state_lane0_val=0x0; Address(0x25[7:0])
12663 SPIWrite 0025,fc //gearbox_init_state_lane1_val=0x0; Address(0x25[7:1])
12664 SPIWrite 0025,f8 //gearbox_init_state_lane2_val=0x0; Address(0x25[7:2])
12665 SPIWrite 0025,f0 //gearbox_init_state_lane3_val=0x0; Address(0x25[7:3])
12666 SPIWrite 0020,03 //link0_init_state=0x1; Address(0x20[7:0])
12667 SPIWrite 0020,03 //link1_init_state=0x1; Address(0x20[7:1])
12668 SPIWrite 0064,ff //jesd_clear_data=0xf; Address(0x64[7:4])
12669 SPIWrite 0040,04 //link0_comma_align_lock_reset_disable=0x1; Address(0x40[7:2])
12670 SPIWrite 0040,0c //link1_comma_align_lock_reset_disable=0x1; Address(0x40[7:3])
12671 SPIWrite 00ac,04 //link0_emb_align_lock_reset_disable=0x1; Address(0xac[7:2])
12672 SPIWrite 00ac,0c //link1_emb_align_lock_reset_disable=0x1; Address(0xac[7:3])
12673 SPIWrite 002c,01 //root_clk_tx1_div_m=0x1; Address(0x2c[7:0])
12674 SPIWrite 002d,00 //root_clk_tx1_div_n_m1=0x0; Address(0x2d[7:0])
12675 SPIWrite 002e,01 //root_clk_tx2_div_m=0x1; Address(0x2e[7:0])
12676 SPIWrite 002f,00 //root_clk_tx2_div_n_m1=0x0; Address(0x2f[7:0])
12677 SPIWrite 0030,01 //duc_clk_tx1_div_m=0x1; Address(0x30[7:0])
12678 SPIWrite 0031,01 //duc_clk_tx1_div_n_m1=0x1; Address(0x31[7:0])
12679 SPIWrite 0032,01 //duc_clk_tx2_div_m=0x1; Address(0x32[7:0])
12680 SPIWrite 0033,01 //duc_clk_tx2_div_n_m1=0x1; Address(0x33[7:0])
12681 SPIWrite 0034,01 //jesd_clk_tx1_div_m=0x1; Address(0x34[7:0])
12682 SPIWrite 0035,00 //jesd_clk_tx1_div_n_m1=0x0; Address(0x35[7:0])
12683 SPIWrite 0036,01 //jesd_clk_tx2_div_m=0x1; Address(0x36[7:0])
12684 SPIWrite 0037,00 //jesd_clk_tx2_div_n_m1=0x0; Address(0x37[7:0])
12685 SPIWrite 0022,41 //link0_jesd_mode=0x1; Address(0x22[7:0])
12686 SPIWrite 0023,41 //link1_jesd_mode=0x1; Address(0x23[7:0])
12687 SPIWrite 0022,41 //link0_jesd_sample_mode=0x1; Address(0x22[7:6])
12688 SPIWrite 0023,41 //link1_jesd_sample_mode=0x1; Address(0x23[7:6])
12689 SPIWrite 0038,1f //tx_root_clk_div_dither_en=0x1; Address(0x38[7:0])
12690 SPIWrite 0038,1d //duc_clk_io_div_dither_en=0x0; Address(0x38[7:1])
12691 SPIWrite 0038,19 //duc_clk_div_dither_en=0x0; Address(0x38[7:2])
12692 SPIWrite 0038,11 //jesd_clk_div_dither_en=0x0; Address(0x38[7:3])
12693 SPIWrite 0038,01 //jesd_clk_div2_div_dither_en=0x0; Address(0x38[7:4])
12694 SPIWrite 0026,00 //num_links=0x0; Address(0x26[7:2])
12695 SPIWrite 0042,7f //comma_align_valid_thresh=0x7f; Address(0x42[7:0])
12696 SPIWrite 00ad,86 //emb_align_valid_thresh=0x6; Address(0xad[7:0])
12697 SPIWrite 0078,00 //link0_sync_request_ena=0x0; Address(0x78[7:0],0x79[7:0])
12698 SPIWrite 0079,00 //link1_sync_request_ena=0x0; Address(0x79[7:0],0x7a[7:0])
12699 SPIWrite 007a,00 //link0_error_ena=0x0; Address(0x7a[7:0],0x7b[7:0])
12700 SPIWrite 007b,00 //link1_error_ena=0x0; Address(0x7b[7:0],0x7c[7:0])
12701 SPIWrite 0103,00 //alarms_clear=0xe1e1e1e1000000bf;
Address(0x100[7:0],0x101[7:0],0x102[7:0],0x103[7:0],0x104[7:0],0x104[7:0],0x105[7:0],0x10
6[7:0],0x107[7:0],0x108[7:0])
12702 SPIWrite 0102,00
12703 SPIWrite 0101,00
12704 SPIWrite 0100,bf
12705 SPIWrite 0107,e1
12706 SPIWrite 0106,e1
12707 SPIWrite 0105,e1
12708 SPIWrite 0104,e1
12709 SPIWrite 00fb,00 //alarms_mask=0xe1e1e1e1000000bf;
Address(0xf8[7:0],0xf9[7:0],0xfa[7:0],0xfb[7:0],0xfc[7:0],0xfc[7:0],0xfd[7:0],0xfe[7:0],0
xff[7:0],0x100[7:0])
12710 SPIWrite 00fa,00

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12711 SPIWrite 00f9,00
12712 SPIWrite 00f8,bf
12713 SPIWrite 00ff,e1
12714 SPIWrite 00fe,e1
12715 SPIWrite 00fd,e1
12716 SPIWrite 00fc,e1
12717 SPIWrite 0113,00 //alarms_to_pap_clear=0xe1e1e1e1000000bf;
Address(0x110[7:0],0x111[7:0],0x112[7:0],0x113[7:0],0x114[7:0],0x114[7:0],0x115[7:0],0x11
6[7:0],0x117[7:0],0x118[7:0])
12718 SPIWrite 0112,00
12719 SPIWrite 0111,00
12720 SPIWrite 0110,bf
12721 SPIWrite 0117,e1
12722 SPIWrite 0116,e1
12723 SPIWrite 0115,e1
12724 SPIWrite 0114,e1
12725 SPIWrite 010b,00 //alarms_to_pap_mask=0xe1e1e1e1000000bf;
Address(0x108[7:0],0x109[7:0],0x10a[7:0],0x10b[7:0],0x10c[7:0],0x10c[7:0],0x10d[7:0],0x10
e[7:0],0x10f[7:0],0x110[7:0])
12726 SPIWrite 010a,00
12727 SPIWrite 0109,00
12728 SPIWrite 0108,bf
12729 SPIWrite 010f,e1
12730 SPIWrite 010e,e1
12731 SPIWrite 010d,e1
12732 SPIWrite 010c,e1
12733 SPIWrite 0024,5c //alarm_zeros_jesd_data_ena=0x0; Address(0x24[7:1])
12734 SPIWrite 003c,82 //serdes_fifo_offset_lane0=0x2; Address(0x3c[7:0])
12735 SPIWrite 003c,22 //serdes_fifo_offset_lane1=0x2; Address(0x3c[7:4])
12736 SPIWrite 003d,82 //serdes_fifo_offset_lane2=0x2; Address(0x3d[7:0])
12737 SPIWrite 003d,22 //serdes_fifo_offset_lane3=0x2; Address(0x3d[7:4])
12738 SPIWrite 0026,02 //jesd_std_sel=0x2; Address(0x26[7:0])
12739 SPIWrite 0047,01 //link0_scr=0x0; Address(0x47[7:7])
12740 SPIWrite 0055,01 //link1_scr=0x0; Address(0x55[7:7])
12741 SPIWrite 0064,f1 //lane_ena=0x1; Address(0x64[7:0])
12742 SPIWrite 0081,f1 //rbd_buf_overflow_err_cnt_thresh=0xf; Address(0x81[7:4])
12743 SPIWrite 0083,1f //dec_8b10b_code_err_cnt_thresh=0xf; Address(0x83[7:0])
12744 SPIWrite 0083,ff //dec_8b10b_disp_err_cnt_thresh=0xf; Address(0x83[7:4])
12745 SPIWrite 0081,ff //link_config_err_cnt_thresh=0xf; Address(0x81[7:0])
12746 SPIWrite 0080,1f //multiframe_align_err_cnt_thresh=0xf; Address(0x80[7:0])
12747 SPIWrite 0080,ff //frame_align_err_cnt_thresh=0xf; Address(0x80[7:4])
12748 SPIWrite 00a8,02 //code_err_disable=0x1; Address(0xa8[7:1])
12749 SPIWrite 0024,58 //zero_invalid_data=0x0; Address(0x24[7:2])
12750 SPIWrite 0024,50 //fifo_error_zeros_data_ena=0x0; Address(0x24[7:3])
12751
12752 //END: Done Configuring DAC JESD RX
12753
12754
12755 //START: Configuring DAC JESD RX
12756
12757 SPIWrite 0016,08 //dac_jesd=0x2; Address(0x16[7:2])
12758 SPIWrite 006c,00 //link0_k_m1=0x0; Address(0x6c[7:0],0x6d[7:0])
12759 SPIWrite 006d,00 //link1_k_m1=0x0; Address(0x6d[7:0],0x6e[7:0])
12760 SPIWrite 0057,00 //link1_ila_k_m1=0x0; Address(0x57[7:0],0x58[7:0])
12761 SPIWrite 0049,00 //link0_ila_k_m1=0x0; Address(0x49[7:0],0x4a[7:0])
12762 SPIWrite 0069,00 //link0_rbd_m1=0x3; Address(0x68[7:0],0x69[7:0],0x6a[7:0])
12763 SPIWrite 0068,03
12764 SPIWrite 006b,00 //link1_rbd_m1=0x3; Address(0x6a[7:0],0x6b[7:0],0x6c[7:0])
12765 SPIWrite 006a,03
12766 SPIWrite 0024,5e //gearbox_init_state_ovr=0x1; Address(0x24[7:6])
12767 SPIWrite 0025,ff //gearbox_init_state_lane0_val=0x1; Address(0x25[7:0])
12768 SPIWrite 0025,ff //gearbox_init_state_lane1_val=0x1; Address(0x25[7:1])
12769 SPIWrite 0025,ff //gearbox_init_state_lane2_val=0x1; Address(0x25[7:2])
12770 SPIWrite 0025,ff //gearbox_init_state_lane3_val=0x1; Address(0x25[7:3])
12771 SPIWrite 0025,fe //gearbox_init_state_lane0_val=0x0; Address(0x25[7:0])
12772 SPIWrite 0025,fc //gearbox_init_state_lane1_val=0x0; Address(0x25[7:1])
12773 SPIWrite 0025,f8 //gearbox_init_state_lane2_val=0x0; Address(0x25[7:2])
12774 SPIWrite 0025,f0 //gearbox_init_state_lane3_val=0x0; Address(0x25[7:3])
12775 SPIWrite 0020,03 //link0_init_state=0x1; Address(0x20[7:0])

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12776 SPIWrite 0020,03 //link1_init_state=0x1; Address(0x20[7:1])
12777 SPIWrite 0064,ff //jesd_clear_data=0xf; Address(0x64[7:4])
12778 SPIWrite 0040,04 //link0_comma_align_lock_reset_disable=0x1; Address(0x40[7:2])
12779 SPIWrite 0040,0c //link1_comma_align_lock_reset_disable=0x1; Address(0x40[7:3])
12780 SPIWrite 00ac,04 //link0_emb_align_lock_reset_disable=0x1; Address(0xac[7:2])
12781 SPIWrite 00ac,0c //link1_emb_align_lock_reset_disable=0x1; Address(0xac[7:3])
12782 SPIWrite 002c,01 //root_clk_tx1_div_m=0x1; Address(0x2c[7:0])
12783 SPIWrite 002d,00 //root_clk_tx1_div_n_m1=0x0; Address(0x2d[7:0])
12784 SPIWrite 002e,01 //root_clk_tx2_div_m=0x1; Address(0x2e[7:0])
12785 SPIWrite 002f,00 //root_clk_tx2_div_n_m1=0x0; Address(0x2f[7:0])
12786 SPIWrite 0030,01 //duc_clk_tx1_div_m=0x1; Address(0x30[7:0])
12787 SPIWrite 0031,01 //duc_clk_tx1_div_n_m1=0x1; Address(0x31[7:0])
12788 SPIWrite 0032,01 //duc_clk_tx2_div_m=0x1; Address(0x32[7:0])
12789 SPIWrite 0033,01 //duc_clk_tx2_div_n_m1=0x1; Address(0x33[7:0])
12790 SPIWrite 0034,01 //jesd_clk_tx1_div_m=0x1; Address(0x34[7:0])
12791 SPIWrite 0035,00 //jesd_clk_tx1_div_n_m1=0x0; Address(0x35[7:0])
12792 SPIWrite 0036,01 //jesd_clk_tx2_div_m=0x1; Address(0x36[7:0])
12793 SPIWrite 0037,00 //jesd_clk_tx2_div_n_m1=0x0; Address(0x37[7:0])
12794 SPIWrite 0022,41 //link0_jesd_mode=0x1; Address(0x22[7:0])
12795 SPIWrite 0023,41 //link1_jesd_mode=0x1; Address(0x23[7:0])
12796 SPIWrite 0022,41 //link0_jesd_sample_mode=0x1; Address(0x22[7:6])
12797 SPIWrite 0023,41 //link1_jesd_sample_mode=0x1; Address(0x23[7:6])
12798 SPIWrite 0038,1f //tx_root_clk_div_dither_en=0x1; Address(0x38[7:0])
12799 SPIWrite 0038,1d //duc_clk_io_div_dither_en=0x0; Address(0x38[7:1])
12800 SPIWrite 0038,19 //duc_clk_div_dither_en=0x0; Address(0x38[7:2])
12801 SPIWrite 0038,11 //jesd_clk_div_dither_en=0x0; Address(0x38[7:3])
12802 SPIWrite 0038,01 //jesd_clk_div2_div_dither_en=0x0; Address(0x38[7:4])
12803 SPIWrite 0026,00 //num_links=0x0; Address(0x26[7:2])
12804 SPIWrite 0042,7f //comma_align_valid_thresh=0x7f; Address(0x42[7:0])
12805 SPIWrite 00ad,86 //emb_align_valid_thresh=0x6; Address(0xad[7:0])
12806 SPIWrite 0078,00 //link0_sync_request_ena=0x0; Address(0x78[7:0],0x79[7:0])
12807 SPIWrite 0079,00 //link1_sync_request_ena=0x0; Address(0x79[7:0],0x7a[7:0])
12808 SPIWrite 007a,00 //link0_error_ena=0x0; Address(0x7a[7:0],0x7b[7:0])
12809 SPIWrite 007b,00 //link1_error_ena=0x0; Address(0x7b[7:0],0x7c[7:0])
12810 SPIWrite 0103,00 //alarms_clear=0xe1e1e1e1000000bf;
Address(0x100[7:0],0x101[7:0],0x102[7:0],0x103[7:0],0x104[7:0],0x104[7:0],0x105[7:0],0x10
6[7:0],0x107[7:0],0x108[7:0])
12811 SPIWrite 0102,00
12812 SPIWrite 0101,00
12813 SPIWrite 0100,bf
12814 SPIWrite 0107,e1
12815 SPIWrite 0106,e1
12816 SPIWrite 0105,e1
12817 SPIWrite 0104,e1
12818 SPIWrite 00fb,00 //alarms_mask=0xe1e1e1e1000000bf;
Address(0xf8[7:0],0xf9[7:0],0xfa[7:0],0xfb[7:0],0xfc[7:0],0xfc[7:0],0xfd[7:0],0xfe[7:0],0
xff[7:0],0x100[7:0])
12819 SPIWrite 00fa,00
12820 SPIWrite 00f9,00
12821 SPIWrite 00f8,bf
12822 SPIWrite 00ff,e1
12823 SPIWrite 00fe,e1
12824 SPIWrite 00fd,e1
12825 SPIWrite 00fc,e1
12826 SPIWrite 0113,00 //alarms_to_pap_clear=0xe1e1e1e1000000bf;
Address(0x110[7:0],0x111[7:0],0x112[7:0],0x113[7:0],0x114[7:0],0x114[7:0],0x115[7:0],0x11
6[7:0],0x117[7:0],0x118[7:0])
12827 SPIWrite 0112,00
12828 SPIWrite 0111,00
12829 SPIWrite 0110,bf
12830 SPIWrite 0117,e1
12831 SPIWrite 0116,e1
12832 SPIWrite 0115,e1
12833 SPIWrite 0114,e1
12834 SPIWrite 010b,00 //alarms_to_pap_mask=0xe1e1e1e1000000bf;
Address(0x108[7:0],0x109[7:0],0x10a[7:0],0x10b[7:0],0x10c[7:0],0x10c[7:0],0x10d[7:0],0x10
e[7:0],0x10f[7:0],0x110[7:0])
12835 SPIWrite 010a,00
12836 SPIWrite 0109,00

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12837 SPIWrite 0108,bf
12838 SPIWrite 010f,e1
12839 SPIWrite 010e,e1
12840 SPIWrite 010d,e1
12841 SPIWrite 010c,e1
12842 SPIWrite 0024,5c //alarm_zeros_jesd_data_ena=0x0; Address(0x24[7:1])
12843 SPIWrite 003c,82 //serdes_fifo_offset_lane0=0x2; Address(0x3c[7:0])
12844 SPIWrite 003c,22 //serdes_fifo_offset_lane1=0x2; Address(0x3c[7:4])
12845 SPIWrite 003d,82 //serdes_fifo_offset_lane2=0x2; Address(0x3d[7:0])
12846 SPIWrite 003d,22 //serdes_fifo_offset_lane3=0x2; Address(0x3d[7:4])
12847 SPIWrite 0026,02 //jesd_std_sel=0x2; Address(0x26[7:0])
12848 SPIWrite 0047,01 //link0_scr=0x0; Address(0x47[7:7])
12849 SPIWrite 0055,01 //link1_scr=0x0; Address(0x55[7:7])
12850 SPIWrite 0064,f1 //lane_ena=0x1; Address(0x64[7:0])
12851 SPIWrite 0081,f1 //rbd_buf_overflow_err_cnt_thresh=0xf; Address(0x81[7:4])
12852 SPIWrite 0083,1f //dec_8b10b_code_err_cnt_thresh=0xf; Address(0x83[7:0])
12853 SPIWrite 0083,ff //dec_8b10b_disp_err_cnt_thresh=0xf; Address(0x83[7:4])
12854 SPIWrite 0081,ff //link_config_err_cnt_thresh=0xf; Address(0x81[7:0])
12855 SPIWrite 0080,1f //multiframe_align_err_cnt_thresh=0xf; Address(0x80[7:0])
12856 SPIWrite 0080,ff //frame_align_err_cnt_thresh=0xf; Address(0x80[7:4])
12857 SPIWrite 00a8,02 //code_err_disable=0x1; Address(0xa8[7:1])
12858 SPIWrite 0024,58 //zero_invalid_data=0x0; Address(0x24[7:2])
12859 SPIWrite 0024,50 //fifo_error_zeros_data_ena=0x0; Address(0x24[7:3])
12860
12861 //END: Done Configuring DAC JESD RX
12862
12863 SPIWrite 0016,00 //dac_jesd=0x0; Address(0x16[7:2])
12864
12865 //STEP: jesdConfig/step3
12866 SPIWrite 0016,10 //jesd_subchip=0x1; Address(0x16[7:4])
12867 SPIWrite 007c,c3 //lp_rx_on_a_sel_2r1f_ab_mask=0x3; Address(0x7c[7:0])
12868 SPIWrite 007c,c3 //lp_rx_on_b_sel_2r1f_ab_mask=0xc; Address(0x7c[7:4])
12869 SPIWrite 007d,03 //lp_rx_on_c_sel_2r1f_ab_mask=0x3; Address(0x7d[7:0])
12870 SPIWrite 007d,c3 //lp_rx_on_d_sel_2r1f_ab_mask=0xc; Address(0x7d[7:4])
12871 SPIWrite 007e,09 //lp_fb_on_a_sel_2r1f_ab_mask=0x1; Address(0x7e[7:0])
12872 SPIWrite 007e,09 //lp_fb_on_c_sel_2r1f_ab_mask=0x2; Address(0x7e[7:2])
12873 SPIWrite 0016,00 //jesd_subchip=0x0; Address(0x16[7:4])
12874 SPIWrite 0016,01 //adc_jesd=0x1; Address(0x16[7:0])
12875 SPIWrite 0120,00 //ctrl_rx1_msf_sig_invalid=0x0; Address(0x120[7:0])
12876 SPIWrite 0120,00 //ctrl_rx2_msf_sig_invalid=0x0; Address(0x120[7:2])
12877 SPIWrite 0120,30 //ctrl_rx3_rx4_msf_sig_invalid=0x3; Address(0x120[7:4])
12878 SPIWrite 0121,00 //ctrl_fb1_msf_sig_invalid=0x0; Address(0x121[7:0])
12879 SPIWrite 0121,00 //ctrl_fb2_msf_sig_invalid=0x0; Address(0x121[7:2])
12880 SPIWrite 0016,00 //adc_jesd=0x0; Address(0x16[7:0])
12881 SPIWrite 0016,10 //jesd_subchip=0x1; Address(0x16[7:4])
12882 SPIWrite 0029,02 //dual_2t2r1f_mode_ab=0x0; Address(0x29[7:0])
12883 SPIWrite 0029,00 //dual_2t2r1f_mode_cd=0x0; Address(0x29[7:1])
12884 SPIWrite 0081,03 //lp_rx_on_c_sel_2r1f_cd_mask=0x3; Address(0x81[7:0])
12885 SPIWrite 0081,c3 //lp_rx_on_d_sel_2r1f_cd_mask=0xc; Address(0x81[7:4])
12886 SPIWrite 0082,04 //lp_fb_on_c_sel_2r1f_cd_mask=0x1; Address(0x82[7:2])
12887 SPIWrite 0082,06 //lp_fb_on_a_sel_2r1f_cd_mask=0x2; Address(0x82[7:0])
12888 SPIWrite 0016,00 //jesd_subchip=0x0; Address(0x16[7:4])
12889 SPIWrite 0016,02 //adc_jesd=0x2; Address(0x16[7:0])
12890 SPIWrite 0120,00 //ctrl_rx1_msf_sig_invalid=0x0; Address(0x120[7:0])
12891 SPIWrite 0120,00 //ctrl_rx2_msf_sig_invalid=0x0; Address(0x120[7:2])
12892 SPIWrite 0120,30 //ctrl_rx3_rx4_msf_sig_invalid=0x3; Address(0x120[7:4])
12893 SPIWrite 0121,00 //ctrl_fb1_msf_sig_invalid=0x0; Address(0x121[7:0])
12894 SPIWrite 0121,00 //ctrl_fb2_msf_sig_invalid=0x0; Address(0x121[7:2])
12895 SPIWrite 0016,00 //adc_jesd=0x0; Address(0x16[7:0])
12896 SPIWrite 0016,10 //jesd_subchip=0x1; Address(0x16[7:4])
12897 SPIWrite 0029,00 //dual_2t2r1f_mode_ab=0x0; Address(0x29[7:0])
12898 SPIWrite 0029,00 //dual_2t2r1f_mode_cd=0x0; Address(0x29[7:1])
12899 SPIWrite 0016,00 //jesd_subchip=0x0; Address(0x16[7:4])
12900
12901 //STEP: agcConfig/step0
12902 SPIWrite 0013,40 //dsa_page1=0x1; Address(0x13[7:6])
12903 SPIWrite 00d0,03 //gain_ctrl=0x3; Address(0xd0[7:0])
12904 SPIWrite 0013,80 //dsa_page1=0x2; Address(0x13[7:6])
12905 SPIWrite 00d0,03 //gain_ctrl=0x3; Address(0xd0[7:0])

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12906 SPIWrite 0013,00 //dsa_page1=0x0; Address(0x13[7:6])
12907 SPIWrite 0012,01 //rxdig=0x1; Address(0x12[7:0])
12908 SPIWrite 0773,01 //cfg_agc_pdn=0x1; Address(0x773[7:0])
12909 SPIWrite 0773,01 //cfg_agc_pdn=0x1; Address(0x773[7:0])
12910 SPIWrite 0012,08 //rxdig=0x8; Address(0x12[7:0])
12911 SPIWrite 0773,01 //cfg_agc_pdn=0x1; Address(0x773[7:0])
12912 SPIWrite 0773,01 //cfg_agc_pdn=0x1; Address(0x773[7:0])
12913 SPIWrite 0012,00 //rxdig=0x0; Address(0x12[7:0])
12914
12915 //STEP: miscConfig/step0
12916
12917 //START: Configuring Interrupt Pins
12918
12919 SPIWrite 0015,40 //digtop=0x1; Address(0x15[7:6])
12920 SPIWrite 0101,02 //alarm_mask_lsb_for_alarm0=0x23f;
Address(0x100[7:0],0x101[7:0],0x102[7:0])
12921 SPIWrite 0100,3f
12922 SPIWrite 0103,00 //alarm_mask_msb_for_alarm0=0x0;
Address(0x102[7:0],0x103[7:0],0x104[7:0])
12923 SPIWrite 0102,00
12924 SPIWrite 0105,02 //alarm_mask_lsb_for_alarm1=0x23f;
Address(0x104[7:0],0x105[7:0],0x106[7:0])
12925 SPIWrite 0104,3f
12926 SPIWrite 0107,00 //alarm_mask_msb_for_alarm1=0x0;
Address(0x106[7:0],0x107[7:0],0x108[7:0])
12927 SPIWrite 0106,00
12928
12929 //END: Done configuring Interrupt Pins
12930
12931
12932 //START: Power Saving Options
12933
12934 SPIWrite 0931,02 //misc_spi_force_ctrl_gbl_pdn_fbana_cd=0x1; Address(0x931[7:1])
12935 SPIWrite 0015,00 //digtop=0x0; Address(0x15[7:6])
12936 SPIWrite 0011,3f //ec_ana=0x3f; Address(0x11[7:0])
12937 SPIWrite 00ce,20 //PDN_NL_BUF=0x1; Address(0xce[7:5])
12938 SPIWrite 00cb,04 //PDN_NL_DITH=0x1; Address(0xcb[7:2])
12939 SPIWrite 00ca,20 //PDN_NL_SAMP=0x1; Address(0xca[7:5])
12940 SPIWrite 00ce,30 //PDN_NL_BE=0x1; Address(0xce[7:4])
12941 SPIWrite 00c3,40 //OVR_PDN_NL_BE_WO_CLK=0x1; Address(0xc3[7:6])
12942 SPIWrite 00c0,01 //PDN_NL_BE_WO_CLK_SPI=0x1; Address(0xc0[7:0])
12943 SPIWrite 00b9,40 //OVR_PDN_NL_DITH_WO_CLK=0x1; Address(0xb9[7:6])
12944 SPIWrite 00b9,50 //PDN_NL_DITH_WO_CLK_SPI=0x1; Address(0xb9[7:4])
12945 SPIWrite 00b9,70 //OVR_PDN_NL_SAMP_WO_CLK=0x1; Address(0xb9[7:5])
12946 SPIWrite 00b9,78 //PDN_NL_SAMP_WO_CLK_SPI=0x1; Address(0xb9[7:3])
12947 SPIWrite 0011,00 //ec_ana=0x0; Address(0x11[7:0])
12948 SPIWrite 0010,3f //ec_dig=0x3f; Address(0x10[7:0])
12949 SPIWrite 00b0,30 //gate_all_clocks=0x1; Address(0xb0[7:5])
12950 SPIWrite 00b4,30 //gate_all_clocks=0x1; Address(0xb4[7:5])
12951 SPIWrite 0010,00 //ec_dig=0x0; Address(0x10[7:0])
12952 SPIWrite 0019,01 //NL_reg0=0x1; Address(0x19[7:0])
12953 SPIWrite 039c,01 //cfg_ref_adc_pdn_rxa=0x1; Address(0x39c[7:0])
12954 SPIWrite 039d,01 //cfg_ref_adc_pdn_rxb=0x1; Address(0x39d[7:0])
12955 SPIWrite 039e,01 //cfg_ref_adc_pdn_rxc=0x1; Address(0x39e[7:0])
12956 SPIWrite 039f,01 //cfg_ref_adc_pdn_rxd=0x1; Address(0x39f[7:0])
12957 SPIWrite 03a0,01 //cfg_ref_adc_pdn_fba=0x1; Address(0x3a0[7:0])
12958 SPIWrite 03a1,01 //cfg_ref_adc_pdn_fbc=0x1; Address(0x3a1[7:0])
12959
12960 //END: Power Saving Options
12961
12962 SPIWrite 0019,00 //NL_reg0=0x0; Address(0x19[7:0])
12963
12964 //STEP: miscConfig/step1
12965 SPIWrite 0013,40 //dsa_page1=0x1; Address(0x13[7:6])
12966 SPIWrite 0124,00 //spi_agc_dsa_A=0x0; Address(0x124[7:0])
12967 SPIWrite 0174,00 //spi_agc_dsa_B=0x0; Address(0x174[7:0])
12968 SPIWrite 0013,80 //dsa_page1=0x2; Address(0x13[7:6])
12969 SPIWrite 0124,00 //spi_agc_dsa_A=0x0; Address(0x124[7:0])
12970 SPIWrite 0174,00 //spi_agc_dsa_B=0x0; Address(0x174[7:0])

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12971 SPIWrite 0013,00 //dsa_page1=0x0; Address(0x13[7:6])
12972 SPIWrite 0013,10 //dsa_page0=0x1; Address(0x13[7:4])
12973 SPIWrite 00c8,00 //txa_dsa_index=0x0; Address(0xc8[7:0])
12974 SPIWrite 00cc,00 //txb_dsa_index=0x0; Address(0xcc[7:0])
12975 SPIWrite 0013,20 //dsa_page0=0x2; Address(0x13[7:4])
12976 SPIWrite 00c8,00 //txa_dsa_index=0x0; Address(0xc8[7:0])
12977 SPIWrite 00cc,00 //txb_dsa_index=0x0; Address(0xcc[7:0])
12978 SPIWrite 0013,10 //dsa_page0=0x1; Address(0x13[7:4])
12979 SPIWrite 006c,00 //spi_agc_dsa_fb=0x0; Address(0x6c[7:0])
12980 SPIWrite 0013,20 //dsa_page0=0x2; Address(0x13[7:4])
12981 SPIWrite 006c,00 //spi_agc_dsa_fb=0x0; Address(0x6c[7:0])
12982 SPIWrite 0013,00 //dsa_page0=0x0; Address(0x13[7:4])
12983
12984 //STEP: gpioConfig/step0
12985 SPIWrite 0015,10 //io_wrap=0x1; Address(0x15[7:4])
12986 SPIWrite 04c0,05 //preferred_input_sel_gpio_48=0x1; Address(0x4c0[7:2])
12987 SPIWrite 04c0,05 //buf_dir_ctrl_gpio_48=0x1; Address(0x4c0[7:0])
12988 SPIWrite 08a1,00 //ovr_sel_intpi_adc_sync_n_ab_0=0x0; Address(0x8a1[7:1])
12989 SPIWrite 04bc,21 //preferred_output_sel_gpio_47=0x1; Address(0x4bc[7:5])
12990 SPIWrite 04bc,22 //buf_dir_ctrl_gpio_47=0x2; Address(0x4bc[7:0])
12991 SPIWrite 10c5,00 //ovr_sel_intpo_dac_sync_n_ab_0=0x0; Address(0x10c5[7:1])
12992 SPIWrite 0438,05 //preferred_input_sel_gpio_14=0x1; Address(0x438[7:2])
12993 SPIWrite 0438,05 //buf_dir_ctrl_gpio_14=0x1; Address(0x438[7:0])
12994 SPIWrite 0899,00 //ovr_sel_intpi_spib1_cs_n=0x0; Address(0x899[7:1])
12995 SPIWrite 0420,01 //preferred_input_sel_gpio_8=0x0; Address(0x420[7:2])
12996 SPIWrite 0420,01 //buf_dir_ctrl_gpio_8=0x1; Address(0x420[7:0])
12997 SPIWrite 08c9,00 //ovr_sel_intpi_tdd_en_fbab=0x0; Address(0x8c9[7:1])
12998 SPIWrite 08ca,09 //crossbar_sel_intpi_tdd_en_fbab=0x9;
Address(0x8ca[7:0],0x8cb[7:0])
12999 SPIWrite 0420,01 //preferred_input_sel_gpio_8=0x0; Address(0x420[7:2])
13000 SPIWrite 0420,01 //buf_dir_ctrl_gpio_8=0x1; Address(0x420[7:0])
13001 SPIWrite 08cd,00 //ovr_sel_intpi_tdd_en_fbcd=0x0; Address(0x8cd[7:1])
13002 SPIWrite 08ce,09 //crossbar_sel_intpi_tdd_en_fbcd=0x9;
Address(0x8ce[7:0],0x8cf[7:0])
13003 SPIWrite 0430,05 //preferred_input_sel_gpio_12=0x1; Address(0x430[7:2])
13004 SPIWrite 0430,05 //buf_dir_ctrl_gpio_12=0x1; Address(0x430[7:0])
13005 SPIWrite 0701,00 //ovr_sel_intbipi_spib1_sdi=0x0; Address(0x701[7:1])
13006 SPIWrite 0514,21 //preferred_output_sel_gpio_69=0x1; Address(0x514[7:5])
13007 SPIWrite 0514,22 //buf_dir_ctrl_gpio_69=0x2; Address(0x514[7:0])
13008 SPIWrite 10f5,00 //ovr_sel_intpo_dac_sync_n_cd_1=0x0; Address(0x10f5[7:1])
13009 SPIWrite 04e4,05 //preferred_input_sel_gpio_57=0x1; Address(0x4e4[7:2])
13010 SPIWrite 04e4,05 //buf_dir_ctrl_gpio_57=0x1; Address(0x4e4[7:0])
13011 SPIWrite 08a5,00 //ovr_sel_intpi_adc_sync_n_ab_1=0x0; Address(0x8a5[7:1])
13012 SPIWrite 04c4,21 //preferred_output_sel_gpio_49=0x1; Address(0x4c4[7:5])
13013 SPIWrite 04c4,22 //buf_dir_ctrl_gpio_49=0x2; Address(0x4c4[7:0])
13014 SPIWrite 10c9,00 //ovr_sel_intpo_dac_sync_n_ab_1=0x0; Address(0x10c9[7:1])
13015 SPIWrite 0510,01 //preferred_input_sel_gpio_68=0x0; Address(0x510[7:2])
13016 SPIWrite 0510,01 //buf_dir_ctrl_gpio_68=0x1; Address(0x510[7:0])
13017 SPIWrite 08ad,00 //ovr_sel_intpi_adc_sync_n_cd_0=0x0; Address(0x8ad[7:1])
13018 SPIWrite 08ae,3e //crossbar_sel_intpi_adc_sync_n_cd_0=0x3e;
Address(0x8ae[7:0],0x8af[7:0])
13019 SPIWrite 050c,21 //preferred_output_sel_gpio_67=0x1; Address(0x50c[7:5])
13020 SPIWrite 050c,22 //buf_dir_ctrl_gpio_67=0x2; Address(0x50c[7:0])
13021 SPIWrite 10f1,00 //ovr_sel_intpo_dac_sync_n_cd_0=0x0; Address(0x10f1[7:1])
13022 SPIWrite 040c,01 //preferred_input_sel_gpio_3=0x0; Address(0x40c[7:2])
13023 SPIWrite 040c,01 //buf_dir_ctrl_gpio_3=0x1; Address(0x40c[7:0])
13024 SPIWrite 08b9,00 //ovr_sel_intpi_tdd_en_txa=0x0; Address(0x8b9[7:1])
13025 SPIWrite 08ba,04 //crossbar_sel_intpi_tdd_en_txa=0x4;
Address(0x8ba[7:0],0x8bb[7:0])
13026 SPIWrite 040c,01 //preferred_input_sel_gpio_3=0x0; Address(0x40c[7:2])
13027 SPIWrite 040c,01 //buf_dir_ctrl_gpio_3=0x1; Address(0x40c[7:0])
13028 SPIWrite 08bd,00 //ovr_sel_intpi_tdd_en_txb=0x0; Address(0x8bd[7:1])
13029 SPIWrite 08be,04 //crossbar_sel_intpi_tdd_en_txb=0x4;
Address(0x8be[7:0],0x8bf[7:0])
13030 SPIWrite 040c,01 //preferred_input_sel_gpio_3=0x0; Address(0x40c[7:2])
13031 SPIWrite 040c,01 //buf_dir_ctrl_gpio_3=0x1; Address(0x40c[7:0])
13032 SPIWrite 08c1,00 //ovr_sel_intpi_tdd_en_txc=0x0; Address(0x8c1[7:1])
13033 SPIWrite 08c2,04 //crossbar_sel_intpi_tdd_en_txc=0x4;
Address(0x8c2[7:0],0x8c3[7:0])

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13034 SPIWrite 040c,01 //preferred_input_sel_gpio_3=0x0; Address(0x40c[7:2])
13035 SPIWrite 040c,01 //buf_dir_ctrl_gpio_3=0x1; Address(0x40c[7:0])
13036 SPIWrite 08c5,00 //ovr_sel_intpi_tdd_en_txd=0x0; Address(0x8c5[7:1])
13037 SPIWrite 08c6,04 //crossbar_sel_intpi_tdd_en_txd=0x4;
Address(0x8c6[7:0],0x8c7[7:0])
13038 SPIWrite 0454,05 //preferred_input_sel_gpio_21=0x1; Address(0x454[7:2])
13039 SPIWrite 0454,05 //buf_dir_ctrl_gpio_21=0x1; Address(0x454[7:0])
13040 SPIWrite 0905,00 //ovr_sel_intpi_global_pdn=0x0; Address(0x905[7:1])
13041 SPIWrite 0444,05 //preferred_input_sel_gpio_17=0x1; Address(0x444[7:2])
13042 SPIWrite 0444,05 //buf_dir_ctrl_gpio_17=0x1; Address(0x444[7:0])
13043 SPIWrite 089d,00 //ovr_sel_intpi_spib1_clk=0x0; Address(0x89d[7:1])
13044 SPIWrite 04cc,01 //preferred_input_sel_gpio_51=0x0; Address(0x4cc[7:2])
13045 SPIWrite 04cc,01 //buf_dir_ctrl_gpio_51=0x1; Address(0x4cc[7:0])
13046 SPIWrite 09d5,00 //ovr_sel_intpi_tdd_en_rxa=0x0; Address(0x9d5[7:1])
13047 SPIWrite 09d6,2d //crossbar_sel_intpi_tdd_en_rxa=0x2d;
Address(0x9d6[7:0],0x9d7[7:0])
13048 SPIWrite 04cc,01 //preferred_input_sel_gpio_51=0x0; Address(0x4cc[7:2])
13049 SPIWrite 04cc,01 //buf_dir_ctrl_gpio_51=0x1; Address(0x4cc[7:0])
13050 SPIWrite 09d9,00 //ovr_sel_intpi_tdd_en_rxb=0x0; Address(0x9d9[7:1])
13051 SPIWrite 09da,2d //crossbar_sel_intpi_tdd_en_rxb=0x2d;
Address(0x9da[7:0],0x9db[7:0])
13052 SPIWrite 04cc,01 //preferred_input_sel_gpio_51=0x0; Address(0x4cc[7:2])
13053 SPIWrite 04cc,01 //buf_dir_ctrl_gpio_51=0x1; Address(0x4cc[7:0])
13054 SPIWrite 09dd,00 //ovr_sel_intpi_tdd_en_rxc=0x0; Address(0x9dd[7:1])
13055 SPIWrite 09de,2d //crossbar_sel_intpi_tdd_en_rxc=0x2d;
Address(0x9de[7:0],0x9df[7:0])
13056 SPIWrite 04cc,01 //preferred_input_sel_gpio_51=0x0; Address(0x4cc[7:2])
13057 SPIWrite 04cc,01 //buf_dir_ctrl_gpio_51=0x1; Address(0x4cc[7:0])
13058 SPIWrite 09e1,00 //ovr_sel_intpi_tdd_en_rxd=0x0; Address(0x9e1[7:1])
13059 SPIWrite 09e2,2d //crossbar_sel_intpi_tdd_en_rxd=0x2d;
Address(0x9e2[7:0],0x9e3[7:0])
13060 SPIWrite 042c,21 //preferred_output_sel_gpio_11=0x1; Address(0x42c[7:5])
13061 SPIWrite 042c,22 //buf_dir_ctrl_gpio_11=0x2; Address(0x42c[7:0])
13062 SPIWrite 1005,00 //ovr_sel_intpo_spib1_sdo=0x0; Address(0x1005[7:1])
13063 SPIWrite 0534,05 //preferred_input_sel_gpio_77=0x1; Address(0x534[7:2])
13064 SPIWrite 0534,05 //buf_dir_ctrl_gpio_77=0x1; Address(0x534[7:0])
13065 SPIWrite 08b1,00 //ovr_sel_intpi_adc_sync_n_cd_1=0x0; Address(0x8b1[7:1])
13066 SPIWrite 0015,00 //io_wrap=0x0; Address(0x15[7:4])
13067
13068 //STEP: sysrefJesdLinkup/step0
13069 SPIWrite 0016,03 //adc_jesd=0x3; Address(0x16[7:0])
13070 SPIWrite 006d,06 //link0_init_state=0x0; Address(0x6d[7:0])
13071 SPIWrite 006d,02 //link2_init_state=0x0; Address(0x6d[7:2])
13072 SPIWrite 006d,00 //link1_init_state=0x0; Address(0x6d[7:1])
13073 SPIWrite 006e,0e //lane0_serdes_fifo_init_state=0x0; Address(0x6e[7:0])
13074 SPIWrite 006e,0c //lane1_serdes_fifo_init_state=0x0; Address(0x6e[7:1])
13075 SPIWrite 006e,08 //lane2_serdes_fifo_init_state=0x0; Address(0x6e[7:2])
13076 SPIWrite 006e,00 //lane3_serdes_fifo_init_state=0x0; Address(0x6e[7:3])
13077 SPIWrite 0016,00 //adc_jesd=0x0; Address(0x16[7:0])
13078 SPIWrite 0016,0c //dac_jesd=0x3; Address(0x16[7:2])
13079 SPIWrite 0020,02 //link0_init_state=0x0; Address(0x20[7:0])
13080 SPIWrite 0020,00 //link1_init_state=0x0; Address(0x20[7:1])
13081 SPIWrite 0016,00 //dac_jesd=0x0; Address(0x16[7:2])
13082
13083 //STEP: sysrefJesdLinkup/step1
13084
13085 //START: Clearing Sysref Flags
13086
13087 SPIWrite 0016,03 //adc_jesd=0x3; Address(0x16[7:0])
13088 SPIWrite 0124,08 //clear_jesd_clk_rx1_p0=0x1; Address(0x124[7:3])
13089 SPIWrite 0128,08 //clear_jesd_sysref_rx1_p0=0x1; Address(0x128[7:3])
13090 SPIWrite 0124,00 //clear_jesd_clk_rx1_p0=0x0; Address(0x124[7:3])
13091 SPIWrite 0128,00 //clear_jesd_sysref_rx1_p0=0x0; Address(0x128[7:3])
13092 SPIWrite 0016,00 //adc_jesd=0x0; Address(0x16[7:0])
13093 SPIWrite 0016,04 //dac_jesd=0x1; Address(0x16[7:2])
13094 SPIWrite 00eb,f0 //clear_jesd_sysref_flag=0xf; Address(0xeb[7:4])
13095 SPIWrite 00eb,ff //clear_jesd_clk_flag=0xf; Address(0xeb[7:0])
13096 SPIWrite 00eb,0f //clear_jesd_sysref_flag=0x0; Address(0xeb[7:4])
13097 SPIWrite 00eb,00 //clear_jesd_clk_flag=0x0; Address(0xeb[7:0])

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13098 SPIWrite 0016,00 //dac_jesd=0x0; Address(0x16[7:2])
13099 SPIWrite 0015,02 //ana_4t4r=0x1; Address(0x15[7:1])
13100 SPIWrite 00dc,10 //sys_ind_clr_tx_ab=0x1; Address(0xdc[7:4])
13101 SPIWrite 00df,10 //sys_ind_clr_tx_cd=0x1; Address(0xdf[7:4])
13102 SPIWrite 0100,10 //sys_ind_clr_digtop=0x1; Address(0x100[7:4])
13103 SPIWrite 00c4,10 //sys_ind_clr_fb_ab=0x1; Address(0xc4[7:4])
13104 SPIWrite 00c7,10 //sys_ind_clr_fb_cd=0x1; Address(0xc7[7:4])
13105 SPIWrite 00cc,10 //sys_ind_clr_rx_ab=0x1; Address(0xcc[7:4])
13106 SPIWrite 00cf,10 //sys_ind_clr_rx_cd=0x1; Address(0xcf[7:4])
13107 SPIWrite 00d8,10 //sys_ind_clr_jesd_dac=0x1; Address(0xd8[7:4])
13108 SPIWrite 00d4,10 //sys_ind_clr_jesd_adc=0x1; Address(0xd4[7:4])
13109 SPIWrite 00dc,00 //sys_ind_clr_tx_ab=0x0; Address(0xdc[7:4])
13110 SPIWrite 00df,00 //sys_ind_clr_tx_cd=0x0; Address(0xdf[7:4])
13111 SPIWrite 0100,00 //sys_ind_clr_digtop=0x0; Address(0x100[7:4])
13112 SPIWrite 00c4,00 //sys_ind_clr_fb_ab=0x0; Address(0xc4[7:4])
13113 SPIWrite 00c7,00 //sys_ind_clr_fb_cd=0x0; Address(0xc7[7:4])
13114 SPIWrite 00cc,00 //sys_ind_clr_rx_ab=0x0; Address(0xcc[7:4])
13115 SPIWrite 00cf,00 //sys_ind_clr_rx_cd=0x0; Address(0xcf[7:4])
13116 SPIWrite 00d8,00 //sys_ind_clr_jesd_dac=0x0; Address(0xd8[7:4])
13117 SPIWrite 00d4,00 //sys_ind_clr_jesd_adc=0x0; Address(0xd4[7:4])
13118
13119 //END: Done clearing Sysref Flags
13120
13121 SPIWrite 0015,00 //ana_4t4r=0x0; Address(0x15[7:1])
13122
13123 //STEP: sysrefJesdLinkup/step2
13124
13125 //START: Sending Sysref to device
13126
13127
13128 //START: Requesting/releasing SPI Access to PLL Pages
13129
13130 SPIWrite 0015,40 //digtop=0x1; Address(0x15[7:6])
13131 SPIWrite 0170,01 //pll_reg_spi_req_a=0x1; Address(0x170[7:0])
13132 SPIWrite 0540,00 //pll_reg_spi_req_b1=0x0; Address(0x540[7:0])
13133
13134 SPIPoll 0171,0,0,01
13135 SPIRead 0171
13136
13137 //Read pll_reg_spi_a_ack=0x1 (Meaning: );; Address(0x171[7:0])
13138
13139
13140 //END: Requesting/releasing SPI Access to PLL Pages
13141
13142 SPIWrite 0015,00 //digtop=0x0; Address(0x15[7:6])
13143 SPIWrite 0015,80 //timing_controller=0x1; Address(0x15[7:7])
13144 SPIWrite 085b,00 //spare_reg_port=0x0;
Address(0x858[7:0],0x859[7:0],0x85a[7:0],0x85b[7:0],0x85c[7:0])
13145 SPIWrite 085a,00
13146 SPIWrite 0859,00
13147 SPIWrite 0858,00
13148 SPIWrite 085b,00 //spare_reg_port=0x101;
Address(0x858[7:0],0x859[7:0],0x85a[7:0],0x85b[7:0],0x85c[7:0])
13149 SPIWrite 085a,00
13150 SPIWrite 0859,01
13151 SPIWrite 0858,01
13152 SPIWrite 085b,00 //spare_reg_port=0x0;
Address(0x858[7:0],0x859[7:0],0x85a[7:0],0x85b[7:0],0x85c[7:0])
13153 SPIWrite 085a,00
13154 SPIWrite 0859,00
13155 SPIWrite 0858,00
13156 SPIWrite 0015,00 //timing_controller=0x0; Address(0x15[7:7])
13157 SPIWrite 0015,01 //pll=0x1; Address(0x15[7:0])
13158 SPIWrite 006a,00 //LCMGEN_SYNC_ENA=0x0; Address(0x6a[7:1])
13159 SPIWrite 006e,00 //LCMGEN_USE_SPI_SYSREF=0x0; Address(0x6e[7:0])
13160 SPIWrite 006a,00 //LCMGEN_SYNC_ENA=0x0; Address(0x6a[7:1])
13161 SPIWrite 006a,02 //LCMGEN_SYNC_ENA=0x1; Address(0x6a[7:1])
13162 SPIWrite 0015,00 //pll=0x0; Address(0x15[7:0])
13163

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13164 //STEP: sysrefJesdLinkup/step3
13165
13166 //External-Action: Give Sysref Here.
13167
13168
13169 WAIT 0.001
13170
13171 //START: Requesting/releasing SPI Access to PLL Pages
13172
13173 SPIWrite 0015,40 //digtop=0x1; Address(0x15[7:6])
13174 SPIWrite 0170,00 //pll_reg_spi_req_a=0x0; Address(0x170[7:0])
13175 SPIWrite 0540,00 //pll_reg_spi_req_b1=0x0; Address(0x540[7:0])
13176
13177 WAIT 0.2
13178
13179 //END: Requesting/releasing SPI Access to PLL Pages
13180
13181
13182 //END: Sending Sysref to device
13183
13184 SPIWrite 0015,00 //digtop=0x0; Address(0x15[7:6])
13185
13186 //STEP: sysrefJesdLinkup/step4
13187
13188 //START: Checking Sysref Flags
13189
13190 SPIWrite 0016,01 //adc_jesd=0x1; Address(0x16[7:0])
13191 SPIRead 012c
13192
13193 //Read monitor_jesd_clk_rx1_p0=0x1; Address(0x12c[7:3])
13194
13195 SPIRead 0130
13196
13197 //Read monitor_jesd_sysref_rx1_p0=0x1; Address(0x130[7:3])
13198
13199
13200 //END: Done checking Sysref Flags
13201
13202 SPIWrite 0016,00 //adc_jesd=0x0; Address(0x16[7:0])
13203
13204 //STEP: sysrefJesdLinkup/step5
13205 SPIWrite 0016,03 //adc_jesd=0x3; Address(0x16[7:0])
13206 SPIWrite 0024,00 //jesd_clear_data=0x0; Address(0x24[7:0])
13207 SPIWrite 00f0,0f //alarms_serdes_fifo_errors_clear=0xf; Address(0xf0[7:0])
13208 SPIWrite 00f0,00 //alarms_serdes_fifo_errors_clear=0x0; Address(0xf0[7:0])
13209 SPIWrite 0016,00 //adc_jesd=0x0; Address(0x16[7:0])
13210 SPIWrite 0016,0c //dac_jesd=0x3; Address(0x16[7:2])
13211 SPIWrite 0064,01 //jesd_clear_data=0x0; Address(0x64[7:4])
13212 SPIWrite 0128,01 //clear_all_alarms=0x1; Address(0x128[7:0])
13213 SPIWrite 0128,00 //clear_all_alarms=0x0; Address(0x128[7:0])
13214 SPIWrite 0128,04 //clear_all_alarms_to_pap=0x1; Address(0x128[7:2])
13215 SPIWrite 0128,00 //clear_all_alarms_to_pap=0x0; Address(0x128[7:2])
13216 SPIWrite 0016,00 //dac_jesd=0x0; Address(0x16[7:2])
13217 SPIWrite 0015,00 //digtop=0x0; Address(0x15[7:6])
13218
13219 //STEP: postLinkUp/step0
13220
13221 //START: Writing Post Link up SERDES writes
13222
13223 SPIWrite 0016,60 //serdes_jesd=0x3; Address(0x16[7:5])
13224 SPIWrite 0016,20 //serdes_jesd=0x1; Address(0x16[7:5])
13225 SPIWrite 0016,60 //serdes_jesd=0x3; Address(0x16[7:5])
13226 SPIWrite 41fb,02
13227 SPIWrite 41fa,6e
13228 SPIWrite 43fb,02
13229 SPIWrite 43fa,6e
13230 SPIWrite 45fb,02
13231 SPIWrite 45fa,6e
13232 SPIWrite 47fb,02
```

```
13233 SPIWrite 47fa,6e
13234
13235 //END: Done writing Post Link up SERDES writes
13236
13237 SPIWrite 0016,00 //serdes_jesd=0x0; Address(0x16[7:5])
13238
13239 //STEP: postLinkUp/step1
13240
13241 //START: Removing TDD Pin Overrides.
13242
13243 SPIWrite 0015,80 //timing_controller=0x1; Address(0x15[7:7])
13244 SPIWrite 00ed,00 //reg_for_rxtdd=0x0; Address(0xed[7:0])
13245 SPIWrite 00f5,00 //reg_for_fbtd=0x0; Address(0xf5[7:0])
13246 SPIWrite 00e5,0f //reg_for_txtdd=0xf; Address(0xe5[7:0])
13247
13248 //END: Removing TDD Pin Overrides.
13249
13250 SPIWrite 0015,00 //timing_controller=0x0; Address(0x15[7:7])
13251 SPIWrite 0018,20 //macro=0x1; Address(0x18[7:5])
13252 SPIRead 00f0
13253
13254 //Read MACRO_READY=0x1; Address(0xf0[7:0])
13255
13256
13257 SPIPoll 00f0,0,0,1
13258
13259 SPIWrite 00a3,00 //MACRO_OPERAND_REG0=0x10f;
Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
13260 SPIWrite 00a2,00
13261 SPIWrite 00a1,01
13262 SPIWrite 00a0,0f
13263 SPIWrite 00a7,00 //MACRO_OPERAND_REG1=0x1;
Address(0xa4[7:0],0xa5[7:0],0xa6[7:0],0xa7[7:0],0xa8[7:0])
13264 SPIWrite 00a6,00
13265 SPIWrite 00a5,00
13266 SPIWrite 00a4,01
13267 SPIWrite 0193,52 //MACRO_OPCODE=0x52; Address(0x193[7:0],0x194[7:0])
13268
13269 WAIT 0.001
13270 SPIRead 00f0
13271
13272 //Read MACRO_DONE=0x1; Address(0xf0[7:2])
13273
13274
13275 SPIPoll 00f0,2,2,4
13276
13277 SPIRead 00f0
13278
13279 //Read MACRO_ERROR=0x0; Address(0xf0[7:3])
13280
13281 SPIRead 00f1
13282
13283 //Read MACRO_ERROR_OPCODE=0x0; Address(0xf1[7:0],0xf2[7:0])
13284
13285 SPIRead 00f0
13286
13287 //Read MACRO_ERROR_IN_OPCODE=0x0; Address(0xf0[7:4])
13288
13289 SPIRead 00f0
13290
13291 //Read MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0; Address(0xf0[7:5])
13292
13293 SPIRead 00f0
13294
13295 //Read MACRO_ERROR_IN_OPERAND=0x0; Address(0xf0[7:6])
13296
13297 SPIRead 00f0
13298
13299 //Read MACRO_ERROR_IN_EXECUTION=0x0; Address(0xf0[7:7])
```

```
13300
13301 SPIRead 00f3
13302 SPIRead 00f2
13303
13304 //Read MACRO_ERROR_EXTENDED_CODE=0x0; Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
13305
13306 SPIRead 00f7
13307 SPIRead 00f6
13308 SPIRead 00f5
13309 SPIRead 00f4
13310
13311 //Read MACRO_ERROR_EXTENDED_CODE_2=0x0;
Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
13312
13313 SPIRead 00f0
13314
13315 //Read MACRO_READY=0x1; Address(0xf0[7:0])
13316
13317
13318 SPIPoll 00f0,0,0,1
13319
13320 SPIWrite 00a3,00 //MACRO_OPERAND_REG0=0x30f;
Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
13321 SPIWrite 00a2,00
13322 SPIWrite 00a1,03
13323 SPIWrite 00a0,0f
13324 SPIWrite 0193,53 //MACRO_OPCODE=0x53; Address(0x193[7:0],0x194[7:0])
13325
13326 WAIT 0.001
13327 SPIRead 00f0
13328
13329 //Read MACRO_DONE=0x1; Address(0xf0[7:2])
13330
13331
13332 SPIPoll 00f0,2,2,4
13333
13334 SPIRead 00f0
13335
13336 //Read MACRO_ERROR=0x0; Address(0xf0[7:3])
13337
13338 SPIRead 00f1
13339
13340 //Read MACRO_ERROR_OPCODE=0x0; Address(0xf1[7:0],0xf2[7:0])
13341
13342 SPIRead 00f0
13343
13344 //Read MACRO_ERROR_IN_OPCODE=0x0; Address(0xf0[7:4])
13345
13346 SPIRead 00f0
13347
13348 //Read MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0; Address(0xf0[7:5])
13349
13350 SPIRead 00f0
13351
13352 //Read MACRO_ERROR_IN_OPERAND=0x0; Address(0xf0[7:6])
13353
13354 SPIRead 00f0
13355
13356 //Read MACRO_ERROR_IN_EXECUTION=0x0; Address(0xf0[7:7])
13357
13358 SPIRead 00f3
13359 SPIRead 00f2
13360
13361 //Read MACRO_ERROR_EXTENDED_CODE=0x0; Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
13362
13363 SPIRead 00f7
13364 SPIRead 00f6
13365 SPIRead 00f5
13366 SPIRead 00f4
```

```

13367
13368 //Read  MACRO_ERROR_EXTENDED_CODE_2=0x0;
Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

13369
13370 SPIRead 00f0
13371
13372 //Read  MACRO_READY=0x1;      Address(0xf0[7:0])
13373
13374
13375 SPIPoll 00f0,0,0,1
13376
13377 SPIWrite 00a3,00      //MACRO_OPERAND_REG0=0x0;
Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
13378 SPIWrite 00a2,00
13379 SPIWrite 00a1,00
13380 SPIWrite 00a0,00
13381 SPIWrite 0193,90      //MACRO_OPCODE=0x90;      Address(0x193[7:0],0x194[7:0])
13382
13383 WAIT 0.001
13384 SPIRead 00f0
13385
13386 //Read  MACRO_DONE=0x1;      Address(0xf0[7:2])
13387
13388
13389 SPIPoll 00f0,2,2,4
13390
13391 SPIRead 00f0
13392
13393 //Read  MACRO_ERROR=0x0;      Address(0xf0[7:3])
13394
13395 SPIRead 00f1
13396
13397 //Read  MACRO_ERROR_OPCODE=0x0;      Address(0xf1[7:0],0xf2[7:0])
13398
13399 SPIRead 00f0
13400
13401 //Read  MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])
13402
13403 SPIRead 00f0
13404
13405 //Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;      Address(0xf0[7:5])
13406
13407 SPIRead 00f0
13408
13409 //Read  MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])
13410
13411 SPIRead 00f0
13412
13413 //Read  MACRO_ERROR_IN_EXECUTION=0x0;  Address(0xf0[7:7])
13414
13415 SPIRead 00f3
13416 SPIRead 00f2
13417
13418 //Read  MACRO_ERROR_EXTENDED_CODE=0x0;  Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
13419
13420 SPIRead 00f7
13421 SPIRead 00f6
13422 SPIRead 00f5
13423 SPIRead 00f4
13424
13425 //Read  MACRO_ERROR_EXTENDED_CODE_2=0x0;
Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

13426
13427 SPIWrite 0144,08      //all_addr_high=0x2;      Address(0x144[7:2])
13428 SPIWrite 0018,00      //macro=0x0;      Address(0x18[7:5])
13429 SPIWrite 0018,08      //cm4top_dram=0x1;  Address(0x18[7:3])
13430 SPIWrite 1f8f,64
13431 SPIWrite 0018,00      //cm4top_dram=0x0;  Address(0x18[7:3])
13432 SPIWrite 0018,20      //macro=0x1;      Address(0x18[7:5])

```

```

13433 SPIRead 00f0
13434
13435 //Read  MACRO_READY=0x1;      Address(0xf0[7:0])
13436
13437
13438 SPIPoll 00f0,0,0,1
13439
13440 SPIWrite 00a3,00      //MACRO_OPERAND_REG0=0x1;
Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
13441 SPIWrite 00a2,00
13442 SPIWrite 00a1,00
13443 SPIWrite 00a0,01
13444 SPIWrite 0193,90      //MACRO_OPCODE=0x90;      Address(0x193[7:0],0x194[7:0])
13445
13446 WAIT 0.001
13447 SPIRead 00f0
13448
13449 //Read  MACRO_DONE=0x1;      Address(0xf0[7:2])
13450
13451
13452 SPIPoll 00f0,2,2,4
13453
13454 SPIRead 00f0
13455
13456 //Read  MACRO_ERROR=0x0;      Address(0xf0[7:3])
13457
13458 SPIRead 00f1
13459
13460 //Read  MACRO_ERROR_OPCODE=0x0;      Address(0xf1[7:0],0xf2[7:0])
13461
13462 SPIRead 00f0
13463
13464 //Read  MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])
13465
13466 SPIRead 00f0
13467
13468 //Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;      Address(0xf0[7:5])
13469
13470 SPIRead 00f0
13471
13472 //Read  MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])
13473
13474 SPIRead 00f0
13475
13476 //Read  MACRO_ERROR_IN_EXECUTION=0x0;  Address(0xf0[7:7])
13477
13478 SPIRead 00f3
13479 SPIRead 00f2
13480
13481 //Read  MACRO_ERROR_EXTENDED_CODE=0x0;  Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
13482
13483 SPIRead 00f7
13484 SPIRead 00f6
13485 SPIRead 00f5
13486 SPIRead 00f4
13487
13488 //Read  MACRO_ERROR_EXTENDED_CODE_2=0x0;
Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
13489
13490 SPIRead 00f0
13491
13492 //Read  MACRO_READY=0x1;      Address(0xf0[7:0])
13493
13494
13495 SPIPoll 00f0,0,0,1
13496
13497 SPIWrite 00a3,01      //MACRO_OPERAND_REG0=0x101010f;
Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
13498 SPIWrite 00a2,01

```

```
13499 SPIWrite 00a1,01
13500 SPIWrite 00a0,0f
13501 SPIWrite 0193,9f //MACRO_OPCODE=0x9f; Address(0x193[7:0],0x194[7:0])
13502
13503 WAIT 0.001
13504 SPIRead 00f0
13505
13506 //Read MACRO_DONE=0x1; Address(0xf0[7:2])
13507
13508
13509 SPIPoll 00f0,2,2,4
13510
13511 SPIRead 00f0
13512
13513 //Read MACRO_ERROR=0x0; Address(0xf0[7:3])
13514
13515 SPIRead 00f1
13516
13517 //Read MACRO_ERROR_OPCODE=0x0; Address(0xf1[7:0],0xf2[7:0])
13518
13519 SPIRead 00f0
13520
13521 //Read MACRO_ERROR_IN_OPCODE=0x0; Address(0xf0[7:4])
13522
13523 SPIRead 00f0
13524
13525 //Read MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0; Address(0xf0[7:5])
13526
13527 SPIRead 00f0
13528
13529 //Read MACRO_ERROR_IN_OPERAND=0x0; Address(0xf0[7:6])
13530
13531 SPIRead 00f0
13532
13533 //Read MACRO_ERROR_IN_EXECUTION=0x0; Address(0xf0[7:7])
13534
13535 SPIRead 00f3
13536 SPIRead 00f2
13537
13538 //Read MACRO_ERROR_EXTENDED_CODE=0x0; Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
13539
13540 SPIRead 00f7
13541 SPIRead 00f6
13542 SPIRead 00f5
13543 SPIRead 00f4
13544
13545 //Read MACRO_ERROR_EXTENDED_CODE_2=0x0;
Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
13546
13547 SPIRead 00f0
13548
13549 //Read MACRO_READY=0x1; Address(0xf0[7:0])
13550
13551
13552 SPIPoll 00f0,0,0,1
13553
13554 SPIWrite 00a3,00 //MACRO_OPERAND_REG0=0xb010f;
Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
13555 SPIWrite 00a2,0b
13556 SPIWrite 00a1,01
13557 SPIWrite 00a0,0f
13558 SPIWrite 0193,49 //MACRO_OPCODE=0x49; Address(0x193[7:0],0x194[7:0])
13559
13560 WAIT 0.001
13561 SPIRead 00f0
13562
13563 //Read MACRO_DONE=0x1; Address(0xf0[7:2])
13564
13565
```



```
13566 SPIPoll 00f0,2,2,4
13567
13568 SPIRead 00f0
13569
13570 //Read MACRO_ERROR=0x0; Address(0xf0[7:3])
13571
13572 SPIRead 00f1
13573
13574 //Read MACRO_ERROR_OPCODE=0x0; Address(0xf1[7:0],0xf2[7:0])
13575
13576 SPIRead 00f0
13577
13578 //Read MACRO_ERROR_IN_OPCODE=0x0; Address(0xf0[7:4])
13579
13580 SPIRead 00f0
13581
13582 //Read MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0; Address(0xf0[7:5])
13583
13584 SPIRead 00f0
13585
13586 //Read MACRO_ERROR_IN_OPERAND=0x0; Address(0xf0[7:6])
13587
13588 SPIRead 00f0
13589
13590 //Read MACRO_ERROR_IN_EXECUTION=0x0; Address(0xf0[7:7])
13591
13592 SPIRead 00f3
13593 SPIRead 00f2
13594
13595 //Read MACRO_ERROR_EXTENDED_CODE=0x0; Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
13596
13597 SPIRead 00f7
13598 SPIRead 00f6
13599 SPIRead 00f5
13600 SPIRead 00f4
13601
13602 //Read MACRO_ERROR_EXTENDED_CODE_2=0x0;
Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
13603
13604 SPIRead 00f0
13605
13606 //Read MACRO_READY=0x1; Address(0xf0[7:0])
13607
13608
13609 SPIPoll 00f0,0,0,1
13610
13611 SPIWrite 00a3,00 //MACRO_OPERAND_REG0=0x1010f;
Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
13612 SPIWrite 00a2,01
13613 SPIWrite 00a1,01
13614 SPIWrite 00a0,0f
13615 SPIWrite 0193,4b //MACRO_OPCODE=0x4b; Address(0x193[7:0],0x194[7:0])
13616
13617 WAIT 0.001
13618 SPIRead 00f0
13619
13620 //Read MACRO_DONE=0x1; Address(0xf0[7:2])
13621
13622
13623 SPIPoll 00f0,2,2,4
13624
13625 SPIRead 00f0
13626
13627 //Read MACRO_ERROR=0x0; Address(0xf0[7:3])
13628
13629 SPIRead 00f1
13630
13631 //Read MACRO_ERROR_OPCODE=0x0; Address(0xf1[7:0],0xf2[7:0])
13632
```

```
13633 SPIRead 00f0
13634
13635 //Read MACRO_ERROR_IN_OPCODE=0x0; Address(0xf0[7:4])
13636
13637 SPIRead 00f0
13638
13639 //Read MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0; Address(0xf0[7:5])
13640
13641 SPIRead 00f0
13642
13643 //Read MACRO_ERROR_IN_OPERAND=0x0; Address(0xf0[7:6])
13644
13645 SPIRead 00f0
13646
13647 //Read MACRO_ERROR_IN_EXECUTION=0x0; Address(0xf0[7:7])
13648
13649 SPIRead 00f3
13650 SPIRead 00f2
13651
13652 //Read MACRO_ERROR_EXTENDED_CODE=0x0; Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
13653
13654 SPIRead 00f7
13655 SPIRead 00f6
13656 SPIRead 00f5
13657 SPIRead 00f4
13658
13659 //Read MACRO_ERROR_EXTENDED_CODE_2=0x0;
Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
13660
13661 SPIRead 00f0
13662
13663 //Read MACRO_READY=0x1; Address(0xf0[7:0])
13664
13665
13666 SPIPoll 00f0,0,0,1
13667
13668 SPIWrite 00a3,01 //MACRO_OPERAND_REG0=0x10100ff;
Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
13669 SPIWrite 00a2,01
13670 SPIWrite 00a1,00
13671 SPIWrite 00a0,ff
13672 SPIWrite 00a7,00 //MACRO_OPERAND_REG1=0x0;
Address(0xa4[7:0],0xa5[7:0],0xa6[7:0],0xa7[7:0],0xa8[7:0])
13673 SPIWrite 00a6,00
13674 SPIWrite 00a5,00
13675 SPIWrite 00a4,00
13676 SPIWrite 0193,13 //MACRO_OPCODE=0x13; Address(0x193[7:0],0x194[7:0])
13677
13678 WAIT 0.001
13679 SPIRead 00f0
13680
13681 //Read MACRO_DONE=0x0; Address(0xf0[7:2])
13682
13683 SPIRead 00f0
13684
13685 //Read MACRO_DONE=0x0; Address(0xf0[7:2])
13686
13687 SPIRead 00f0
13688
13689 //Read MACRO_DONE=0x0; Address(0xf0[7:2])
13690
13691 SPIRead 00f0
13692
13693 //Read MACRO_DONE=0x0; Address(0xf0[7:2])
13694
13695 SPIRead 00f0
13696
13697 //Read MACRO_DONE=0x0; Address(0xf0[7:2])
13698
```

```
13699 SPIRead 00f0
13700
13701 //Read MACRO_DONE=0x0; Address(0xf0[7:2])
13702
13703 SPIRead 00f0
13704
13705 //Read MACRO_DONE=0x0; Address(0xf0[7:2])
13706
13707 SPIRead 00f0
13708
13709 //Read MACRO_DONE=0x0; Address(0xf0[7:2])
13710
13711 SPIRead 00f0
13712
13713 //Read MACRO_DONE=0x0; Address(0xf0[7:2])
13714
13715 SPIRead 00f0
13716
13717 //Read MACRO_DONE=0x0; Address(0xf0[7:2])
13718
13719 SPIRead 00f0
13720
13721 //Read MACRO_DONE=0x0; Address(0xf0[7:2])
13722
13723 SPIRead 00f0
13724
13725 //Read MACRO_DONE=0x1; Address(0xf0[7:2])
13726
13727
13728 SPIPoll 00f0,2,2,4
13729
13730 SPIRead 00f0
13731
13732 //Read MACRO_ERROR=0x0; Address(0xf0[7:3])
13733
13734 SPIRead 00f1
13735
13736 //Read MACRO_ERROR_OPCODE=0x0; Address(0xf1[7:0],0xf2[7:0])
13737
13738 SPIRead 00f0
13739
13740 //Read MACRO_ERROR_IN_OPCODE=0x0; Address(0xf0[7:4])
13741
13742 SPIRead 00f0
13743
13744 //Read MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0; Address(0xf0[7:5])
13745
13746 SPIRead 00f0
13747
13748 //Read MACRO_ERROR_IN_OPERAND=0x0; Address(0xf0[7:6])
13749
13750 SPIRead 00f0
13751
13752 //Read MACRO_ERROR_IN_EXECUTION=0x0; Address(0xf0[7:7])
13753
13754 SPIRead 00f3
13755 SPIRead 00f2
13756
13757 //Read MACRO_ERROR_EXTENDED_CODE=0x0; Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
13758
13759 SPIRead 00f7
13760 SPIRead 00f6
13761 SPIRead 00f5
13762 SPIRead 00f4
13763
13764 //Read MACRO_ERROR_EXTENDED_CODE_2=0x0;
Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
13765
13766 SPIWrite 0018,00 //macro=0x0; Address(0x18[7:5])
```

```

13767 SPIWrite 0012,01 //rxdig=0x1; Address(0x12[7:0])
13768 SPIWrite 14c4,00 //dc_corr_fw_pause=0x0; Address(0x14c4[7:0])
13769 SPIWrite 0012,02 //rxdig=0x2; Address(0x12[7:0])
13770 SPIWrite 14c4,00 //dc_corr_fw_pause=0x0; Address(0x14c4[7:0])
13771 SPIWrite 0012,04 //rxdig=0x4; Address(0x12[7:0])
13772 SPIWrite 14c4,00 //dc_corr_fw_pause=0x0; Address(0x14c4[7:0])
13773 SPIWrite 0012,08 //rxdig=0x8; Address(0x12[7:0])
13774 SPIWrite 14c4,00 //dc_corr_fw_pause=0x0; Address(0x14c4[7:0])
13775 SPIWrite 0012,00 //rxdig=0x0; Address(0x12[7:0])
13776 SPIWrite 0012,10 //fbdig=0x1; Address(0x12[7:4])
13777 SPIWrite 14c4,00 //dc_corr_fw_pause=0x0; Address(0x14c4[7:0])
13778 SPIWrite 0012,20 //fbdig=0x2; Address(0x12[7:4])
13779 SPIWrite 14c4,00 //dc_corr_fw_pause=0x0; Address(0x14c4[7:0])
13780
13781 //START: Removing TDD Pin Overrides.
13782
13783 SPIWrite 0012,00 //fbdig=0x0; Address(0x12[7:4])
13784 SPIWrite 0015,80 //timing_controller=0x1; Address(0x15[7:7])
13785 SPIWrite 00ed,00 //reg_for_rxtdd=0x0; Address(0xed[7:0])
13786 SPIWrite 00f5,03 //reg_for_fbtdd=0x3; Address(0xf5[7:0])
13787 SPIWrite 00e5,00 //reg_for_txtdd=0x0; Address(0xe5[7:0])
13788
13789 //END: Removing TDD Pin Overrides.
13790
13791
13792 //START: Removing TDD Pin Overrides.
13793
13794 SPIWrite 00ed,0f //reg_for_rxtdd=0xf; Address(0xed[7:0])
13795 SPIWrite 00f5,00 //reg_for_fbtdd=0x0; Address(0xf5[7:0])
13796 SPIWrite 00e5,00 //reg_for_txtdd=0x0; Address(0xe5[7:0])
13797
13798 //END: Removing TDD Pin Overrides.
13799
13800
13801 //START: Removing TDD Pin Overrides.
13802
13803 SPIWrite 00ec,00 //use_reg_for_rxtdd=0x0; Address(0xec[7:0])
13804 SPIWrite 00f4,00 //use_reg_for_fbtdd=0x0; Address(0xf4[7:0])
13805 SPIWrite 00e4,00 //use_reg_for_txtdd=0x0; Address(0xe4[7:0])
13806
13807 //END: Removing TDD Pin Overrides.
13808
13809 SPIWrite 0015,00 //timing_controller=0x0; Address(0x15[7:7])
13810 SPIWrite 0018,20 //macro=0x1; Address(0x18[7:5])
13811 SPIRead 00f0
13812
13813 //Read MACRO_READY=0x1; Address(0xf0[7:0])
13814
13815
13816 SPIPoll 00f0,0,0,1
13817
13818 SPIWrite 00a3,00 //MACRO_OPERAND_REG0=0x0;
Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
13819 SPIWrite 00a2,00
13820 SPIWrite 00a1,00
13821 SPIWrite 00a0,00
13822 SPIWrite 0193,15 //MACRO_OPCODE=0x15; Address(0x193[7:0],0x194[7:0])
13823
13824 WAIT 0.001
13825 SPIRead 00f0
13826
13827 //Read MACRO_DONE=0x1; Address(0xf0[7:2])
13828
13829
13830 SPIPoll 00f0,2,2,4
13831
13832 SPIRead 00f0
13833
13834 //Read MACRO_ERROR=0x0; Address(0xf0[7:3])

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13835
13836 SPIRead 00f1
13837
13838 //Read MACRO_ERROR_OPCODE=0x0; Address(0xf1[7:0],0xf2[7:0])
13839
13840 SPIRead 00f0
13841
13842 //Read MACRO_ERROR_IN_OPCODE=0x0; Address(0xf0[7:4])
13843
13844 SPIRead 00f0
13845
13846 //Read MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0; Address(0xf0[7:5])
13847
13848 SPIRead 00f0
13849
13850 //Read MACRO_ERROR_IN_OPERAND=0x0; Address(0xf0[7:6])
13851
13852 SPIRead 00f0
13853
13854 //Read MACRO_ERROR_IN_EXECUTION=0x0; Address(0xf0[7:7])
13855
13856 SPIRead 00f3
13857 SPIRead 00f2
13858
13859 //Read MACRO_ERROR_EXTENDED_CODE=0x0; Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
13860
13861 SPIRead 00f7
13862 SPIRead 00f6
13863 SPIRead 00f5
13864 SPIRead 00f4
13865
13866 //Read MACRO_ERROR_EXTENDED_CODE_2=0x0;
Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
13867
13868 SPIWrite 0018,00 //macro=0x0; Address(0x18[7:5])
13869
13870 //STEP: postLinkUp/step2
13871 SPIWrite 0016,03 //adc_jesd=0x3; Address(0x16[7:0])
13872 SPIWrite 0024,00 //jesd_clear_data=0x0; Address(0x24[7:0])
13873 SPIWrite 00f0,0f //alarms_serdes_fifo_errors_clear=0xf; Address(0xf0[7:0])
13874 SPIWrite 00f0,00 //alarms_serdes_fifo_errors_clear=0x0; Address(0xf0[7:0])
13875 SPIWrite 0016,00 //adc_jesd=0x0; Address(0x16[7:0])
13876 SPIWrite 0016,0c //dac_jesd=0x3; Address(0x16[7:2])
13877 SPIWrite 0064,01 //jesd_clear_data=0x0; Address(0x64[7:4])
13878 SPIWrite 0128,01 //clear_all_alarms=0x1; Address(0x128[7:0])
13879 SPIWrite 0128,00 //clear_all_alarms=0x0; Address(0x128[7:0])
13880 SPIWrite 0128,04 //clear_all_alarms_to_pap=0x1; Address(0x128[7:2])
13881 SPIWrite 0128,00 //clear_all_alarms_to_pap=0x0; Address(0x128[7:2])
13882 SPIWrite 0016,00 //dac_jesd=0x0; Address(0x16[7:2])
13883 SPIWrite 0019,30 //txdig=0x3; Address(0x19[7:4])
13884 SPIWrite 0a40,0f //HBF59OvrClr=0xf; Address(0xa40[7:0])
13885 SPIWrite 0a41,0f //HBF23HROvrClr=0xf; Address(0xa41[7:0])
13886 SPIWrite 0a44,0f //mixerOvrClr=0xf; Address(0xa44[7:0])
13887 SPIWrite 0a45,0f //isincOvrClr=0xf; Address(0xa45[7:0])
13888 SPIWrite 0a46,0f //dacDitherOvrClr=0xf; Address(0xa46[7:0])
13889 SPIWrite 0a40,00 //HBF59OvrClr=0x0; Address(0xa40[7:0])
13890 SPIWrite 0a41,00 //HBF23HROvrClr=0x0; Address(0xa41[7:0])
13891 SPIWrite 0a44,00 //mixerOvrClr=0x0; Address(0xa44[7:0])
13892 SPIWrite 0a45,00 //isincOvrClr=0x0; Address(0xa45[7:0])
13893 SPIWrite 0a46,00 //dacDitherOvrClr=0x0; Address(0xa46[7:0])
13894 SPIWrite 054d,07 //txa_pap_alarm_clr=0x7ff; Address(0x54c[2:0],0x54d[7:0])
13895 SPIWrite 054c,ff
13896 SPIWrite 0580,07 //pap_det_alarm_clr=0x7; Address(0x580[7:0])
13897 SPIWrite 0589,07 //ip_pap_det_alarm_clr=0x7; Address(0x589[7:0])
13898 SPIWrite 06b4,01 //pap_hw_alarm_act_alc_clr=0x1; Address(0x6b4[7:0])
13899 SPIWrite 06b4,03 //pap_hw_alarm_act_lmt_clr=0x1; Address(0x6b4[7:1])
13900 SPIWrite 054d,00 //txa_pap_alarm_clr=0x0; Address(0x54c[2:0],0x54d[7:0])
13901 SPIWrite 054c,00
13902 SPIWrite 0580,00 //pap_det_alarm_clr=0x0; Address(0x580[7:0])

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13903 SPIWrite 0589,00 //ip_pap_det_alarm_clr=0x0; Address(0x589[7:0])
13904 SPIWrite 06b4,02 //pap_hw_alarm_act_alc_clr=0x0; Address(0x6b4[7:0])
13905 SPIWrite 06b4,00 //pap_hw_alarm_act_lmt_clr=0x0; Address(0x6b4[7:1])
13906 SPIWrite 052c,1f //pap_alarm_clr=0x1f; Address(0x52c[7:0])
13907 SPIWrite 052c,00 //pap_alarm_clr=0x0; Address(0x52c[7:0])
13908 SPIWrite 0019,00 //txdig=0x0; Address(0x19[7:4])
13909
13910 //STEP: dlJesdLinkupCheck/step0
13911
13912 //START: Reading the JESD RX states to check if link is established
13913
13914
13915 WAIT 0.001
13916 SPIWrite 0016,04 //dac_jesd=0x1; Address(0x16[7:2])
13917 SPIRead 011b
13918 SPIRead 011a
13919 SPIRead 0119
13920 SPIRead 0118
13921 SPIRead 011f
13922 SPIRead 011e
13923 SPIRead 011d
13924 SPIRead 011c
13925
13926 //Read alarms=0x0;
Address(0x118[7:0],0x119[7:0],0x11a[7:0],0x11b[7:0],0x11c[7:0],0x11c[7:0],0x11d[7:0],0x11
e[7:0],0x11f[7:0],0x120[7:0])
13927
13928 SPIRead 00ee
13929
13930 //Read comma_align_lock_flag=0x1; Address(0xee[7:0])
13931
13932 SPIRead 00a2
13933
13934 //Read jesd_cs_state=0x2; Address(0xa2[7:0],0xa3[7:0])
13935
13936 SPIRead 00a6
13937
13938 //Read jesd_buf_state=0x3; Address(0xa6[7:0],0xa7[7:0])
13939
13940
13941 //END: Done reading the JESD RX states to check if link is established
13942
13943
13944 //START: Reading the JESD RX states to check if link is established
13945
13946
13947 WAIT 0.001
13948 SPIWrite 0016,08 //dac_jesd=0x2; Address(0x16[7:2])
13949 SPIRead 011b
13950 SPIRead 011a
13951 SPIRead 0119
13952 SPIRead 0118
13953 SPIRead 011f
13954 SPIRead 011e
13955 SPIRead 011d
13956 SPIRead 011c
13957
13958 //Read alarms=0x200000000;
Address(0x118[7:0],0x119[7:0],0x11a[7:0],0x11b[7:0],0x11c[7:0],0x11c[7:0],0x11d[7:0],0x11
e[7:0],0x11f[7:0],0x120[7:0])
13959
13960 SPIRead 00ee
13961
13962 //Read comma_align_lock_flag=0x1; Address(0xee[7:0])
13963
13964 SPIRead 00a2
13965
13966 //Read jesd_cs_state=0x2; Address(0xa2[7:0],0xa3[7:0])
13967

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13968 SPIRead 00a6
13969
13970 //Read jesd_buf_state=0x3;      Address(0xa6[7:0],0xa7[7:0])
13971
13972
13973 //END: Done reading the JESD RX states to check if link is established
13974
13975 SPIWrite 0016,00 //dac_jesd=0x0;      Address(0x16[7:2])
13976
13977 //END: Device Config Complete
13978
13979
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