```
1
2   //AFE79xx
3   //START: Doing AFE Config
4
5
6   //Device Initialization for ChipVersion: 1.3
7
8
9   //**********System Parameters**********
10
11
12  //System Parameters:
13  //  FRef    =   491.52
14  //  FadcFb  =   2949.12
15  //  FadcRx  =   2949.12
16  //  Fdac    =   5898.24
17  //  LMFSHdFb    =   ['14810', '14810']
18  //  LMFSHdRx    =   ['181610', '181610', '181610', '181610']
19  //  LMFSHdTx    =   ['14810', '14810', '14810', '14810']
20  //  RRFMode =   1
21  //  adcDataMuxEn    =   1
22  //  adcSelect0  =   [0, 1, 2]
23  //  adcSelect1  =   [0, 1, 2]
24  //  auxAdcEn    =   False
25  //  broadcastRxNcoSel   =   0
26  //  broadcastTxNcoSel   =   0
27  //  chipId  =   1
28  //  chipType    =   0
29  //  chipVersion =   19
30  //  combineDucMode  =   [0, 0]
31  //  continuousSysref    =   0
32  //  dacDataMuxEn    =   1
33  //  ddcFactorFb =   [8, 8]
34  //  ddcFactorRx =   [16, 16, 16, 16]
35  //  defaultFbDsa    =   [0, 0]
36  //  defaultRxDsa    =   [0, 0, 0, 0]
37  //  defaultTxDsa    =   [0, 0, 0, 0]
38  //  ducFactorTx =   [16, 16, 16, 16]
39  //  enableDacInterleavedMode    =   False
40  //  enableReliabilityDetector   =   True
41  //  enableRxDsaCalibration  =   False
42  //  enableTxDsaCalibration  =   False
43  //  enableTxFbLoopbackLowLatencyMode    =   [False, False]
44  //  executeLinkUpSequenceSeparately =   False
45  //  externalClockRx =   False
46  //  externalClockTx =   False
47  //  fbChainSelForDsaCalib   =   0
48  //  fbDataMux   =   [0, 1]
49  //  fbDsaPerTx  =   [0, 0, 0, 0]
50  //  fbDsaPerTxEn    =   False
51  //  fbEnable    =   [True, False]
52  //  fbJesdTxK   =   [1, 1]
53  //  fbJesdTxScr =   [False, False]
54  //  fbJesdTxSyncMux =   [0, 0]
55  //  fbNco0  =   [1800, 1800]
56  //  fbNco1  =   [1800, 2600]
57  //  fbNco2  =   [1800, 1900]
58  //  fbNco3  =   [1800, 1900]
59  //  gpioMapping = {     'H8'    :'ADC_SYNC0',
60  //          'H9'    :'DAC_SYNC0',
61  //          'H16'   :'SPIB1_CSN',
62  //          'K14'   :'FBABTDD',
63  //          'H11'   :'INTBIPI_SPIB1_SDI',
64  //          'P9'    :'DAC_SYNC3',
65  //          'H7'    :'ADC_SYNC1',
66  //          'G9'    :'DAC_SYNC1',
67  //          'R6'    :'FBCDTDD',
68  //          'N8'    :'ADC_SYNC2',
69  //          'N9'    :'DAC_SYNC2',
```

```
70  //          'H15'   :['TXATDD', 'TXBTDD'],
71  //          'R15'   :['RXCTDD', 'RXDTDD'],
72  //          'P14'   :'GLOBAL_PDN',
73  //          'V5'    :['TXCTDD', 'TXDTDD'],
74  //          'G16'   :'SPIB1_CLK',
75  //          'E7'    :['RXATDD', 'RXBTDD'],
76  //          'G12'   :'SPIB1_SDO',
77  //          'N7'    :'ADC_SYNC3',
78  //          }
79  //  gpioOverrideValSet  =   []
80  //  gpioPolarityInv =   []
81  //  halfRateModeFb  =   [False, False]
82  //  halfRateModeRx  =   [False, False]
83  //  halfRateModeTx  =   [False, False]
84  //  intPinsParams[0] = {        'SPI'   :True,
85  //          'TXBPAP'    :True,
86  //          'TXCPAP'    :True,
87  //          'JESD'  :True,
88  //          'TXAPAP'    :True,
89  //          'PLL'   :True,
90  //          'TXDPAP'    :True,
91  //          }
92  //
93  //  intPinsParams[1] = {        'SPI'   :True,
94  //          'TXBPAP'    :True,
95  //          'TXCPAP'    :True,
96  //          'JESD'  :True,
97  //          'TXAPAP'    :True,
98  //          'PLL'   :True,
99  //          'TXDPAP'    :True,
100 //          }
101 //
102 //  jesdABLvdsSync  =   False
103 //  jesdCDLvdsSync  =   False
104 //  jesdLoopbackEn  =   0
105 //  jesdRxK =   [1, 1, 1, 1]
106 //  jesdRxLaneMux   =   [1, 3, 5, 6, 0, 2, 4, 7]
107 //  jesdRxProtocol  =   [2, 2]
108 //  jesdRxRbd   =   [4, 4]
109 //  jesdRxScr   =   [False, False, False, False]
110 //  jesdRxSyncMux   =   [0, 0, 0, 0]
111 //  jesdSendZeroesInTddOff  =   False
112 //  jesdSystemMode  =   [1, 1]
113 //  jesdTxIlaL  =   [4, 4, 2, 4, 4, 2]
114 //  jesdTxIlaLid    =   [0, 1, 2, 3, 4, 5, 6, 7]
115 //  jesdTxIlaM  =   [8, 8, 2, 8, 8, 2]
116 //  jesdTxLaneMux   =   [0, 2, 1, 3, 4, 5, 6, 7]
117 //  jesdTxProtocol  =   [2, 2]
118 //  libVersion  =   '1.7.3'
119 //  modeTdd =   0
120 //  ncoFbMode   =   0
121 //  ncoFreqMode =   '1KHz'
122 //  ncoRxMode   =   [0, 0]
123 //  ncoTxMode   =   [0, 0]
124 //  numBandsRx  =   [0, 0, 0, 0]
125 //  numBandsTx  =   [0, 0, 0, 0]
126 //  numFbNCO    =   1
127 //  numRxNCO    =   1
128 //  numRxNCOB0  =   [1, 1, 1, 1]
129 //  numRxNCOB1  =   [1, 1, 1, 1]
130 //  numTxNCO    =   1
131 //  numTxNCOB0  =   [1, 1, 1, 1]
132 //  numTxNCOB1  =   [1, 1, 1, 1]
133 //  papParams[0] = {        'hpfWindowCntr' :0,
134 //          'triggerToRampDown' :50,
135 //          'triggerClearToRampUp'  :50,
136 //          'hpfNumSample'  :4,
137 //          'rampDownStartVal'  :128,
138 //          'enable'    :False,
```

```
139   //          'maNumSample'   :128,
140   //          'alarmPinDynamicMode'   :1,
141   //          'waitCounter'   :200,
142   //          'maWindowCntrTh'    :1,
143   //          'alarmMask' :64,
144   //          'detectInWaitState' :0,
145   //          'maThreshB0'    :90.0,
146   //          'maThreshB1'    :90.0,
147   //          'hpfWindowCntrTh'   :0,
148   //          'hpfEnable' :1,
149   //          'amplUpdateCycles'  :2,
150   //          'alarmChannelMask'  :14,
151   //          'maWindowCntr'  :1,
152   //          'rampStickyMode'    :0,
153   //          'gainStepSize'  :5,
154   //          'multMode'  :0,
155   //          'alarmPulseGPIO'    :1000,
156   //          'hpfThreshComb' :30.0,
157   //          'maEnable'  :1,
158   //          'attnStepSize'  :5,
159   //          'maThreshComb'  :90.0,
160   //          'hpfThreshB1'   :30.0,
161   //          'hpfThreshB0'   :30.0,
162   //          }
163   //
164   //  papParams[1] = {        'hpfWindowCntr' :0,
165   //          'triggerToRampDown' :50,
166   //          'triggerClearToRampUp'  :50,
167   //          'hpfNumSample'  :4,
168   //          'rampDownStartVal'  :128,
169   //          'enable'    :False,
170   //          'maNumSample'   :128,
171   //          'alarmPinDynamicMode'   :1,
172   //          'waitCounter'   :200,
173   //          'maWindowCntrTh'    :1,
174   //          'alarmMask' :64,
175   //          'detectInWaitState' :0,
176   //          'maThreshB0'    :90.0,
177   //          'maThreshB1'    :90.0,
178   //          'hpfWindowCntrTh'   :0,
179   //          'hpfEnable' :1,
180   //          'amplUpdateCycles'  :2,
181   //          'alarmChannelMask'  :14,
182   //          'maWindowCntr'  :1,
183   //          'rampStickyMode'    :0,
184   //          'gainStepSize'  :5,
185   //          'multMode'  :0,
186   //          'alarmPulseGPIO'    :1000,
187   //          'hpfThreshComb' :30.0,
188   //          'maEnable'  :1,
189   //          'attnStepSize'  :5,
190   //          'maThreshComb'  :90.0,
191   //          'hpfThreshB1'   :30.0,
192   //          'hpfThreshB0'   :30.0,
193   //          }
194   //
195   //  papParams[2] = {        'hpfWindowCntr' :0,
196   //          'triggerToRampDown' :50,
197   //          'triggerClearToRampUp'  :50,
198   //          'hpfNumSample'  :4,
199   //          'rampDownStartVal'  :128,
200   //          'enable'    :False,
201   //          'maNumSample'   :128,
202   //          'alarmPinDynamicMode'   :1,
203   //          'waitCounter'   :200,
204   //          'maWindowCntrTh'    :1,
205   //          'alarmMask' :64,
206   //          'detectInWaitState' :0,
207   //          'maThreshB0'    :90.0,
```

```
208   //          'maThreshB1'    :90.0,
209   //          'hpfWindowCntrTh'   :0,
210   //          'hpfEnable' :1,
211   //          'amplUpdateCycles'  :2,
212   //          'alarmChannelMask'  :14,
213   //          'maWindowCntr'  :1,
214   //          'rampStickyMode'    :0,
215   //          'gainStepSize'  :5,
216   //          'multMode'  :0,
217   //          'alarmPulseGPIO'    :1000,
218   //          'hpfThreshComb' :30.0,
219   //          'maEnable'  :1,
220   //          'attnStepSize'  :5,
221   //          'maThreshComb'  :90.0,
222   //          'hpfThreshB1'   :30.0,
223   //          'hpfThreshB0'   :30.0,
224   //          }
225   //
226   //  papParams[3] = {        'hpfWindowCntr' :0,
227   //          'triggerToRampDown' :50,
228   //          'triggerClearToRampUp'  :50,
229   //          'hpfNumSample'  :4,
230   //          'rampDownStartVal'  :128,
231   //          'enable'    :False,
232   //          'maNumSample'   :128,
233   //          'alarmPinDynamicMode'   :1,
234   //          'waitCounter'   :200,
235   //          'maWindowCntrTh'    :1,
236   //          'alarmMask' :64,
237   //          'detectInWaitState' :0,
238   //          'maThreshB0'    :90.0,
239   //          'maThreshB1'    :90.0,
240   //          'hpfWindowCntrTh'   :0,
241   //          'hpfEnable' :1,
242   //          'amplUpdateCycles'  :2,
243   //          'alarmChannelMask'  :14,
244   //          'maWindowCntr'  :1,
245   //          'rampStickyMode'    :0,
246   //          'gainStepSize'  :5,
247   //          'multMode'  :0,
248   //          'alarmPulseGPIO'    :1000,
249   //          'hpfThreshComb' :30.0,
250   //          'maEnable'  :1,
251   //          'attnStepSize'  :5,
252   //          'maThreshComb'  :90.0,
253   //          'hpfThreshB1'   :30.0,
254   //          'hpfThreshB0'   :30.0,
255   //          }
256   //
257   //  pllGsmMode  =   False
258   //  reliabilityDetectorDecayMode    =   0
259   //  rxChainSelForDsaCalib   =   15
260   //  rxDataMux   =   [0, 1, 2, 3, 4, 5, 6, 7]
261   //  rxDsaBandCalibMode  =   0
262   //  rxDsaCalibMode  =   0
263   //  rxDsaGainRange  =   [0, 25]
264   //  rxEnable    =   [True, True, True, True]
265   //  rxJesdTxK   =   [1, 1, 1, 1]
266   //  rxJesdTxScr =   [False, False, False, False]
267   //  rxJesdTxSyncMux =   [0, 0, 0, 0]
268   //  rxNco0  =   [[1800, 2600], [1800, 2600], [1800, 2600], [1800, 2600]]
269   //  rxNco1  =   [[1800, 2600], [1800, 2600], [1800, 2600], [1800, 2600]]
270   //  serdesFirmware  =   True
271   //  serdesManualCTLE    =   [6, 6, 6, 6, 6, 6, 6, 6]
272   //  serdesManualCTLEEn  =   False
273   //  serdesRxLanePolarity    =   [False, False, False, False, False, False, False, False]
274   //  serdesTxLanePolarity    =   [False, False, False, False, False, False, False, False]
275   //  serdesTxMainCursor  =   [3, 0, 0, 0, 0, 0, 0, 3]
276   //  serdesTxPostCursor  =   [0, 0, 0, 0, 0, 0, 0, 0]
```

```
//  serdesTxPreCursor   =   [0, 0, 0, 0, 0, 0, 0, 0]
//  setIlaParams    =   True
//  spiMode =   1
//  syncLoopBack    =   False
//  sysrefTermination   =   0
//  txDataMux   =   [0, 1, 2, 3, 4, 5, 6, 7]
//  txDsaBandCalibMode  =   0
//  txDsaCalibMode  =   0
//  txEnable    =   [True, True, True, True]
//  txNco0  =   [[1800, 2600], [1800, 2600], [1800, 2600], [1800, 2600]]
//  txNco1  =   [[1800, 2600], [1800, 2600], [1800, 2600], [1800, 2600]]
//  txToFbMode  =   0
//  txdsaStartStop  =   [0, 29]
//  useLcmClkForSysrefLatch =   True
//  useSpiSysref    =   False
//  useTxForCalib   =   0
//


//**********Configuration Starting**********
//


//EXTERNAL-ACTION: Toggle HW Reset


//STEP: rstDevice/step0

//START: Device Soft Reset and SPI Check

SPIWrite 0000,30    //global_soft_reset=0x0;    Address(0x0[7:7])
SPIWrite 0000,b0    //global_soft_reset=0x1;    Address(0x0[7:7])
SPIWrite 0000,30    //global_soft_reset=0x0;    Address(0x0[7:7])
SPIWrite 0000,30    //global_4pin=0x1;  Address(0x0[7:4])
SPIWrite 0000,30    //global_ascend=0x1;    Address(0x0[7:5])
SPIRead 0003

//Read  chip_type=0xa;  Address(0x3[7:0],0x4[7:0])

SPIRead 0004
SPIRead 0005

//Read  chip_id=0x78;   Address(0x4[7:0],0x5[7:0],0x5[7:0],0x6[7:0])

SPIRead 0006

//Read  chip_ver=0x11;  Address(0x6[7:0],0x7[7:0])

SPIRead 0007
SPIRead 0008

//Read  vendor_id=0x451;    Address(0x7[7:0],0x8[7:0],0x8[7:0],0x9[7:0])


//END: Device Soft Reset and SPI Check


//STEP: rstDevice/step1

//START: Waking up device

SPIWrite 0015,80    //timing_controller=0x1;    Address(0x15[7:7])
SPIWrite 0191,00    //force_tg_xx_A=0x0;    Address(0x191[7:0])
SPIWrite 0231,00    //force_tg_xx_A=0x0;    Address(0x231[7:0])
SPIWrite 02d1,00    //force_tg_xx_A=0x0;    Address(0x2d1[7:0])
SPIWrite 0371,00    //force_tg_xx_A=0x0;    Address(0x371[7:0])
SPIWrite 042a,00    //force_tg_xx_A=0x0;    Address(0x42a[7:0])
SPIWrite 04e2,00    //force_tg_xx_A=0x0;    Address(0x4e2[7:0])
SPIWrite 059a,00    //force_tg_xx_A=0x0;    Address(0x59a[7:0])
```

```
SPIWrite 0652,00    //force_tg_xx_A=0x0;    Address(0x652[7:0])
SPIWrite 070a,00    //force_tg_xx_A=0x0;    Address(0x70a[7:0])
SPIWrite 07c2,00    //force_tg_xx_A=0x0;    Address(0x7c2[7:0])

//START: Setting TDD Pin in override state and setting override values.

SPIWrite 00ec,01    //use_reg_for_rxtdd=0x1;    Address(0xec[7:0])
SPIWrite 00f4,01    //use_reg_for_fbtdd=0x1;    Address(0xf4[7:0])
SPIWrite 00e4,01    //use_reg_for_txtdd=0x1;    Address(0xe4[7:0])
SPIWrite 00ed,00    //reg_for_rxtdd=0x0;    Address(0xed[7:0])
SPIWrite 00f5,00    //reg_for_fbtdd=0x0;    Address(0xf5[7:0])
SPIWrite 00e5,00    //reg_for_txtdd=0x0;    Address(0xe5[7:0])

//END: Setting TDD Pin in override state and setting override values.

SPIWrite 0015,00    //timing_controller=0x0;    Address(0x15[7:7])
SPIWrite 0015,40    //digtop=0x1;   Address(0x15[7:6])
SPIWrite 0190,03    //misc_spi_global_pdn_ctrl=0x1;     Address(0x190[7:0])
SPIWrite 0190,01    //misc_spi_global_pdn_sig=0x0;  Address(0x190[7:1])
SPIWrite 0015,00    //digtop=0x0;   Address(0x15[7:6])

WAIT 0.005

//END: Done waking up device


//START: Changing termination to 100 ohm


//START: Requesting/releasing SPI Access to PLL Pages

SPIWrite 0015,40    //digtop=0x1;   Address(0x15[7:6])
SPIWrite 0170,01    //pll_reg_spi_req_a=0x1;    Address(0x170[7:0])
SPIWrite 0540,00    //pll_reg_spi_req_b1=0x0;   Address(0x540[7:0])

SPIPoll 0171,0,0,01
SPIRead 0171

//Read  pll_reg_spi_a_ack=0x1(Meaning: );;  Address(0x171[7:0])


//END: Requesting/releasing SPI Access to PLL Pages

SPIWrite 0015,00    //digtop=0x0;   Address(0x15[7:6])
SPIWrite 0015,01    //pll=0x1;  Address(0x15[7:0])
SPIWrite 0054,81
SPIWrite 0015,00    //pll=0x0;  Address(0x15[7:0])

//START: Requesting/releasing SPI Access to PLL Pages

SPIWrite 0015,40    //digtop=0x1;   Address(0x15[7:6])
SPIWrite 0170,00    //pll_reg_spi_req_a=0x0;    Address(0x170[7:0])
SPIWrite 0540,00    //pll_reg_spi_req_b1=0x0;   Address(0x540[7:0])

WAIT 0.2

//END: Requesting/releasing SPI Access to PLL Pages


//END: Changing termination to 100 ohm


//START: Setting CM4 Clock Div

SPIWrite 0015,00    //digtop=0x0;   Address(0x15[7:6])
SPIWrite 0015,02    //ana_4t4r=0x1;     Address(0x15[7:1])
SPIWrite 00c0,00    //CM4DIV_DIV=0x0;   Address(0xc0[7:0])

//END: Setting CM4 Clock Div
```

```
415
416   SPIWrite 0015,00    //ana_4t4r=0x0;     Address(0x15[7:1])
417
418   //STEP: efuseChain/step0
419
420   //START: Loading Efuse Chain
421
422   SPIWrite 0015,40    //digtop=0x1;   Address(0x15[7:6])
423   SPIWrite 08a8,02    //spi_ext_chain_ctrl_fusefarm1=0x2;
      Address(0x8a8[7:0],0x8a9[7:0])
424   SPIWrite 0810,01    //spi_ovr_sys_clk_gate=0x1;     Address(0x810[7:0])
425   SPIWrite 0830,01    //spi_ovr_sys_clk_gate=0x1;     Address(0x830[7:0])
426   SPIWrite 0200,00    //spi_div_sys_clk_sel=0x0;  Address(0x200[7:0])
427   SPIWrite 0210,00    //spi_div_sys_clk_sel=0x0;  Address(0x210[7:0])
428   SPIWrite 0814,00    //spi_sys_rstn_ctrl=0x0;    Address(0x814[7:0])
429   SPIWrite 0834,00    //spi_sys_rstn_ctrl=0x0;    Address(0x834[7:0])
430   SPIWrite 0814,01    //spi_sys_rstn_ctrl=0x1;    Address(0x814[7:0])
431   SPIWrite 0834,01    //spi_sys_rstn_ctrl=0x1;    Address(0x834[7:0])
432   SPIWrite 0810,00    //spi_ovr_sys_clk_gate=0x0;     Address(0x810[7:0])
433   SPIWrite 0830,00    //spi_ovr_sys_clk_gate=0x0;     Address(0x830[7:0])
434   SPIWrite 0810,01    //spi_ovr_sys_clk_gate=0x1;     Address(0x810[7:0])
435   SPIWrite 0830,01    //spi_ovr_sys_clk_gate=0x1;     Address(0x830[7:0])
436   SPIWrite 0200,05    //spi_div_sys_clk_sel=0x5;  Address(0x200[7:0])
437   SPIWrite 0210,00    //spi_div_sys_clk_sel=0x0;  Address(0x210[7:0])
438   SPIWrite 0814,03    //spi_sys_rstn_ctrl=0x3;    Address(0x814[7:0])
439   SPIWrite 0834,03    //spi_sys_rstn_ctrl=0x3;    Address(0x834[7:0])
440   SPIWrite 0814,00    //spi_sys_rstn_ctrl=0x0;    Address(0x814[7:0])
441   SPIWrite 0834,00    //spi_sys_rstn_ctrl=0x0;    Address(0x834[7:0])
442   SPIWrite 0810,00    //spi_ovr_sys_clk_gate=0x0;     Address(0x810[7:0])
443   SPIWrite 0830,00    //spi_ovr_sys_clk_gate=0x0;     Address(0x830[7:0])
444   SPIWrite 0814,00    //spi_ovr_sys_autoload_chain=0x0;   Address(0x814[7:2])
445   SPIWrite 0834,00    //spi_ovr_sys_autoload_chain=0x0;   Address(0x834[7:2])
446   SPIWrite 0814,1c    //spi_ovr_sys_autoload_chain=0x7;   Address(0x814[7:2])
447   SPIWrite 0834,1c    //spi_ovr_sys_autoload_chain=0x7;   Address(0x834[7:2])
448   SPIWrite 0814,00    //spi_ovr_sys_autoload_chain=0x0;   Address(0x814[7:2])
449   SPIWrite 0834,00    //spi_ovr_sys_autoload_chain=0x0;   Address(0x834[7:2])
450
451   WAIT 0.05
452
453   //END: Loading Efuse Chain
454
455
456   //START: Checking for Efuse
457
458   SPIRead 0150
459
460   //Read  obs_func_spi_chain_autoload_done=0xf;   Address(0x150[7:0])
461
462   SPIRead 0150
463
464   //Read  obs_func_spi_chain_autoload_error=0x0;  Address(0x150[7:4])
465
466
467   //END: Checking for Efuse
468
469
470   //START: enabling Efuse Clock
471
472   SPIWrite 0830,01    //spi_ovr_sys_clk_gate=0x1;     Address(0x830[7:0])
473   SPIWrite 0810,01    //spi_ovr_sys_clk_gate=0x1;     Address(0x810[7:0])
474   SPIWrite 0910,0f    //tx_dh_ahb_en=0xf;     Address(0x910[7:0])
475   SPIWrite 0911,03    //fb_ec_ahb_en=0x3;     Address(0x911[7:0])
476   SPIWrite 0912,0f    //rx_ec_ahb_en=0xf;     Address(0x912[7:0])
477
478   //END: enabling Efuse Clock
479
480   SPIWrite 0015,00    //digtop=0x0;   Address(0x15[7:6])
481
482   //STEP: mcuWakeUp/step0
```

```
SPIWrite 0018,20    //macro=0x1;    Address(0x18[7:5])
SPIWrite 0140,01    //ss_reset_reg=0x1;     Address(0x140[7:0])
SPIWrite 0140,00    //ss_reset_reg=0x0;     Address(0x140[7:0])

WAIT 0.001
SPIRead 00f0

//Read  MACRO_READY=0x1;    Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00    //MACRO_OPERAND_REG0=0x2;
Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00
SPIWrite 00a1,00
SPIWrite 00a0,02
SPIWrite 0193,01    //MACRO_OPCODE=0x1;     Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0

//Read  MACRO_DONE=0x1;     Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIRead 00f0

//Read  MACRO_ERROR=0x0;    Address(0xf0[7:3])

SPIRead 00f1

//Read  MACRO_ERROR_OPCODE=0x0;     Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0

//Read  MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0

//Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;     Address(0xf0[7:5])

SPIRead 00f0

//Read  MACRO_ERROR_IN_OPERAND=0x0;     Address(0xf0[7:6])

SPIRead 00f0

//Read  MACRO_ERROR_IN_EXECUTION=0x0;   Address(0xf0[7:7])

SPIRead 00f3
SPIRead 00f2

//Read  MACRO_ERROR_EXTENDED_CODE=0x0;  Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7
SPIRead 00f6
SPIRead 00f5
SPIRead 00f4

//Read  MACRO_ERROR_EXTENDED_CODE_2=0x0;
Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00fb
SPIRead 00fa
SPIRead 00f9
SPIRead 00f8

```

```
//Read  MACRO_RESULT_REG0=0x13070a01;
Address(0xf8[7:0],0xf9[7:0],0xfa[7:0],0xfb[7:0],0xfc[7:0])

SPIRead 00ff
SPIRead 00fe
SPIRead 00fd
SPIRead 00fc

//Read  MACRO_RESULT_REG1=0x2af8;
Address(0xfc[7:0],0xfd[7:0],0xfe[7:0],0xff[7:0],0x100[7:0])

SPIRead 00f0

//Read  MACRO_READY=0x1;    Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00    //MACRO_OPERAND_REG0=0x0;
Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00
SPIWrite 00a1,00
SPIWrite 00a0,00
SPIWrite 0193,90    //MACRO_OPCODE=0x90;    Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0

//Read  MACRO_DONE=0x1;     Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIRead 00f0

//Read  MACRO_ERROR=0x0;    Address(0xf0[7:3])

SPIRead 00f1

//Read  MACRO_ERROR_OPCODE=0x0;     Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0

//Read  MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0

//Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;     Address(0xf0[7:5])

SPIRead 00f0

//Read  MACRO_ERROR_IN_OPERAND=0x0;     Address(0xf0[7:6])

SPIRead 00f0

//Read  MACRO_ERROR_IN_EXECUTION=0x0;   Address(0xf0[7:7])

SPIRead 00f3
SPIRead 00f2

//Read  MACRO_ERROR_EXTENDED_CODE=0x0;  Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7
SPIRead 00f6
SPIRead 00f5
SPIRead 00f4

//Read  MACRO_ERROR_EXTENDED_CODE_2=0x0;
Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
```

```
615
616   SPIWrite 0144,08    //all_addr_high=0x2;    Address(0x144[7:2])
617   SPIWrite 0018,00    //macro=0x0;    Address(0x18[7:5])
618   SPIWrite 0018,08    //cm4top_dram=0x1;  Address(0x18[7:3])
619   SPIWrite 03bf,00
620   SPIWrite 03be,07
621   SPIWrite 03bd,80
622   SPIWrite 03bc,00
623   SPIWrite 03c3,00
624   SPIWrite 03c2,04
625   SPIWrite 03c1,17
626   SPIWrite 03c0,46
627   SPIWrite 03d0,05
628   SPIWrite 03ac,1d
629   SPIWrite 03ad,1d
630   SPIWrite 1402,00
631   SPIWrite 1403,00
632   SPIWrite 1401,00
633   SPIWrite 0018,00    //cm4top_dram=0x0;  Address(0x18[7:3])
634   SPIWrite 0018,20    //macro=0x1;    Address(0x18[7:5])
635   SPIWrite 0144,08    //all_addr_high=0x2;    Address(0x144[7:2])
636   SPIWrite 0018,00    //macro=0x0;    Address(0x18[7:5])
637   SPIWrite 0018,08    //cm4top_dram=0x1;  Address(0x18[7:3])
638   SPIWrite 1ee8,20
639   SPIWrite 1ee9,00
640   SPIWrite 0018,00    //cm4top_dram=0x0;  Address(0x18[7:3])
641   SPIWrite 0018,20    //macro=0x1;    Address(0x18[7:5])
642   SPIWrite 0144,08    //all_addr_high=0x2;    Address(0x144[7:2])
643   SPIWrite 0018,00    //macro=0x0;    Address(0x18[7:5])
644   SPIWrite 0018,08    //cm4top_dram=0x1;  Address(0x18[7:3])
645   SPIWrite 1b5f,2c
646   SPIWrite 0018,00    //cm4top_dram=0x0;  Address(0x18[7:3])
647   SPIWrite 0018,20    //macro=0x1;    Address(0x18[7:5])
648   SPIWrite 0144,08    //all_addr_high=0x2;    Address(0x144[7:2])
649   SPIWrite 0018,00    //macro=0x0;    Address(0x18[7:5])
650   SPIWrite 0018,08    //cm4top_dram=0x1;  Address(0x18[7:3])
651   SPIWrite 1b6f,07
652   SPIWrite 0018,00    //cm4top_dram=0x0;  Address(0x18[7:3])
653   SPIWrite 0018,20    //macro=0x1;    Address(0x18[7:5])
654   SPIWrite 0144,08    //all_addr_high=0x2;    Address(0x144[7:2])
655   SPIWrite 0018,00    //macro=0x0;    Address(0x18[7:5])
656   SPIWrite 0018,08    //cm4top_dram=0x1;  Address(0x18[7:3])
657   SPIWrite 1e7d,09
658   SPIWrite 0018,00    //cm4top_dram=0x0;  Address(0x18[7:3])
659   SPIWrite 0018,20    //macro=0x1;    Address(0x18[7:5])
660   SPIWrite 0144,08    //all_addr_high=0x2;    Address(0x144[7:2])
661   SPIWrite 0018,00    //macro=0x0;    Address(0x18[7:5])
662   SPIWrite 0018,08    //cm4top_dram=0x1;  Address(0x18[7:3])
663   SPIWrite 1a70,d0
664   SPIWrite 1a71,00
665   SPIWrite 0018,00    //cm4top_dram=0x0;  Address(0x18[7:3])
666   SPIWrite 0018,20    //macro=0x1;    Address(0x18[7:5])
667   SPIWrite 0144,08    //all_addr_high=0x2;    Address(0x144[7:2])
668   SPIWrite 0018,00    //macro=0x0;    Address(0x18[7:5])
669   SPIWrite 0018,08    //cm4top_dram=0x1;  Address(0x18[7:3])
670   SPIWrite 1b20,c0
671   SPIWrite 1b21,00
672   SPIWrite 0018,00    //cm4top_dram=0x0;  Address(0x18[7:3])
673   SPIWrite 0018,20    //macro=0x1;    Address(0x18[7:5])
674   SPIRead 00f0
675
676   //Read  MACRO_READY=0x1;    Address(0xf0[7:0])
677
678
679   SPIPoll 00f0,0,0,1
680
681   SPIWrite 00a3,00    //MACRO_OPERAND_REG0=0x1;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
682   SPIWrite 00a2,00
```

```
SPIWrite 00a1,00
SPIWrite 00a0,01
SPIWrite 0193,90    //MACRO_OPCODE=0x90;    Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0

//Read  MACRO_DONE=0x1;     Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIRead 00f0

//Read  MACRO_ERROR=0x0;    Address(0xf0[7:3])

SPIRead 00f1

//Read  MACRO_ERROR_OPCODE=0x0;     Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0

//Read  MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0

//Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;     Address(0xf0[7:5])

SPIRead 00f0

//Read  MACRO_ERROR_IN_OPERAND=0x0;     Address(0xf0[7:6])

SPIRead 00f0

//Read  MACRO_ERROR_IN_EXECUTION=0x0;   Address(0xf0[7:7])

SPIRead 00f3
SPIRead 00f2

//Read  MACRO_ERROR_EXTENDED_CODE=0x0;  Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7
SPIRead 00f6
SPIRead 00f5
SPIRead 00f4

//Read  MACRO_ERROR_EXTENDED_CODE_2=0x0;
Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIWrite 0018,00    //macro=0x0;    Address(0x18[7:5])

//STEP: mcuWakeUp/step1
SPIWrite 0018,20    //macro=0x1;    Address(0x18[7:5])
SPIWrite 0144,00    //all_addr_high=0x0;    Address(0x144[7:2])
SPIWrite 0018,00    //macro=0x0;    Address(0x18[7:5])
SPIWrite 0018,01    //sys_calib_macro_memory=0x1;   Address(0x18[7:0])
SPIWrite 0020,00
SPIWrite 0021,00
SPIWrite 0022,00
SPIWrite 0023,00
SPIWrite 0024,8d
SPIWrite 0025,0c
SPIWrite 0026,03
SPIWrite 0027,00
SPIWrite 0028,b5
SPIWrite 0029,a4
SPIWrite 002a,6d
SPIWrite 002b,ea
SPIWrite 002c,7d
```

```
SPIWrite 002d,19
SPIWrite 002e,ce
SPIWrite 002f,ca
SPIWrite 0030,01
SPIWrite 0031,07
SPIWrite 0032,08
SPIWrite 0033,12
SPIWrite 0034,14
SPIWrite 0035,00
SPIWrite 0036,01
SPIWrite 0037,0a
SPIWrite 0038,07
SPIWrite 0039,13
SPIWrite 003a,f8
SPIWrite 003b,2a
SPIWrite 003c,01
SPIWrite 003d,0a
SPIWrite 003e,07
SPIWrite 003f,13
SPIWrite 0040,f8
SPIWrite 0041,2a
SPIWrite 0042,00
SPIWrite 0043,00
SPIWrite 0044,00
SPIWrite 0045,00
SPIWrite 0046,00
SPIWrite 0047,00
SPIWrite 0048,00
SPIWrite 0049,00
SPIWrite 004a,00
SPIWrite 004b,00
SPIWrite 004c,00
SPIWrite 004d,00
SPIWrite 004e,00
SPIWrite 004f,00
SPIWrite 0050,f8
SPIWrite 0051,b5
SPIWrite 0052,76
SPIWrite 0053,48
SPIWrite 0054,77
SPIWrite 0055,4b
SPIWrite 0056,04
SPIWrite 0057,68
SPIWrite 0058,44
SPIWrite 0059,f0
SPIWrite 005a,40
SPIWrite 005b,01
SPIWrite 005c,d2
SPIWrite 005d,4f
SPIWrite 005e,01
SPIWrite 005f,60
SPIWrite 0060,1e
SPIWrite 0061,68
SPIWrite 0062,50
SPIWrite 0063,f8
SPIWrite 0064,c0
SPIWrite 0065,1c
SPIWrite 0066,72
SPIWrite 0067,48
SPIWrite 0068,00
SPIWrite 0069,91
SPIWrite 006a,01
SPIWrite 006b,68
SPIWrite 006c,41
SPIWrite 006d,f0
SPIWrite 006e,01
SPIWrite 006f,01
SPIWrite 0070,01
SPIWrite 0071,60
```

```
SPIWrite 0072,01
SPIWrite 0073,68
SPIWrite 0074,00
SPIWrite 0075,25
SPIWrite 0076,21
SPIWrite 0077,f0
SPIWrite 0078,02
SPIWrite 0079,01
SPIWrite 007a,01
SPIWrite 007b,60
SPIWrite 007c,02
SPIWrite 007d,68
SPIWrite 007e,3c
SPIWrite 007f,60
SPIWrite 0080,c6
SPIWrite 0081,f3
SPIWrite 0082,40
SPIWrite 0083,11
SPIWrite 0084,01
SPIWrite 0085,eb
SPIWrite 0086,96
SPIWrite 0087,11
SPIWrite 0088,42
SPIWrite 0089,f0
SPIWrite 008a,08
SPIWrite 008b,02
SPIWrite 008c,02
SPIWrite 008d,60
SPIWrite 008e,0f
SPIWrite 008f,e0
SPIWrite 0090,21
SPIWrite 0091,46
SPIWrite 0092,49
SPIWrite 0093,1e
SPIWrite 0094,fd
SPIWrite 0095,d1
SPIWrite 0096,00
SPIWrite 0097,bf
SPIWrite 0098,5b
SPIWrite 0099,1c
SPIWrite 009a,20
SPIWrite 009b,e0
SPIWrite 009c,22
SPIWrite 009d,46
SPIWrite 009e,52
SPIWrite 009f,1e
SPIWrite 00a0,fd
SPIWrite 00a1,d1
SPIWrite 00a2,00
SPIWrite 00a3,bf
SPIWrite 00a4,6d
SPIWrite 00a5,1c
SPIWrite 00a6,0d
SPIWrite 00a7,e0
SPIWrite 00a8,64
SPIWrite 00a9,1e
SPIWrite 00aa,fd
SPIWrite 00ab,d1
SPIWrite 00ac,00
SPIWrite 00ad,bf
SPIWrite 00ae,6d
SPIWrite 00af,1c
SPIWrite 00b0,13
SPIWrite 00b1,24
SPIWrite 00b2,a9
SPIWrite 00b3,42
SPIWrite 00b4,c0
SPIWrite 00b5,f2
SPIWrite 00b6,00
```

```
  SPIWrite 00b7,04
  SPIWrite 00b8,f6
  SPIWrite 00b9,d8
  SPIWrite 00ba,02
  SPIWrite 00bb,68
  SPIWrite 00bc,00
  SPIWrite 00bd,25
  SPIWrite 00be,22
  SPIWrite 00bf,f0
  SPIWrite 00c0,08
  SPIWrite 00c1,02
  SPIWrite 00c2,02
  SPIWrite 00c3,60
  SPIWrite 00c4,a9
  SPIWrite 00c5,42
  SPIWrite 00c6,e9
  SPIWrite 00c7,d8
  SPIWrite 00c8,08
  SPIWrite 00c9,33
  SPIWrite 00ca,01
  SPIWrite 00cb,68
  SPIWrite 00cc,1d
  SPIWrite 00cd,68
  SPIWrite 00ce,41
  SPIWrite 00cf,f0
  SPIWrite 00d0,02
  SPIWrite 00d1,01
  SPIWrite 00d2,c5
  SPIWrite 00d3,f3
  SPIWrite 00d4,40
  SPIWrite 00d5,12
  SPIWrite 00d6,00
  SPIWrite 00d7,23
  SPIWrite 00d8,01
  SPIWrite 00d9,60
  SPIWrite 00da,02
  SPIWrite 00db,eb
  SPIWrite 00dc,95
  SPIWrite 00dd,10
  SPIWrite 00de,98
  SPIWrite 00df,42
  SPIWrite 00e0,d6
  SPIWrite 00e1,d8
  SPIWrite 00e2,f8
  SPIWrite 00e3,bd
  SPIWrite 00e4,52
  SPIWrite 00e5,4a
  SPIWrite 00e6,c9
  SPIWrite 00e7,4b
  SPIWrite 00e8,11
  SPIWrite 00e9,68
  SPIWrite 00ea,06
  SPIWrite 00eb,20
  SPIWrite 00ec,21
  SPIWrite 00ed,f0
  SPIWrite 00ee,01
  SPIWrite 00ef,01
  SPIWrite 00f0,11
  SPIWrite 00f1,60
  SPIWrite 00f2,53
  SPIWrite 00f3,f8
  SPIWrite 00f4,04
  SPIWrite 00f5,2b
  SPIWrite 00f6,d2
  SPIWrite 00f7,f8
  SPIWrite 00f8,18
  SPIWrite 00f9,11
  SPIWrite 00fa,40
  SPIWrite 00fb,1e
```

```
  SPIWrite 00fc,21
  SPIWrite 00fd,f4
  SPIWrite 00fe,00
  SPIWrite 00ff,71
  SPIWrite 0100,c2
  SPIWrite 0101,f8
  SPIWrite 0102,18
  SPIWrite 0103,11
  SPIWrite 0104,f5
  SPIWrite 0105,d1
  SPIWrite 0106,d8
  SPIWrite 0107,48
  SPIWrite 0108,01
  SPIWrite 0109,68
  SPIWrite 010a,4a
  SPIWrite 010b,4a
  SPIWrite 010c,d1
  SPIWrite 010d,f8
  SPIWrite 010e,04
  SPIWrite 010f,05
  SPIWrite 0110,20
  SPIWrite 0111,f0
  SPIWrite 0112,3f
  SPIWrite 0113,00
  SPIWrite 0114,c1
  SPIWrite 0115,f8
  SPIWrite 0116,04
  SPIWrite 0117,05
  SPIWrite 0118,12
  SPIWrite 0119,68
  SPIWrite 011a,00
  SPIWrite 011b,21
  SPIWrite 011c,c2
  SPIWrite 011d,f3
  SPIWrite 011e,40
  SPIWrite 011f,10
  SPIWrite 0120,00
  SPIWrite 0121,eb
  SPIWrite 0122,92
  SPIWrite 0123,10
  SPIWrite 0124,06
  SPIWrite 0125,e0
  SPIWrite 0126,13
  SPIWrite 0127,22
  SPIWrite 0128,c0
  SPIWrite 0129,f2
  SPIWrite 012a,00
  SPIWrite 012b,02
  SPIWrite 012c,52
  SPIWrite 012d,1e
  SPIWrite 012e,fd
  SPIWrite 012f,d1
  SPIWrite 0130,00
  SPIWrite 0131,bf
  SPIWrite 0132,49
  SPIWrite 0133,1c
  SPIWrite 0134,88
  SPIWrite 0135,42
  SPIWrite 0136,f6
  SPIWrite 0137,d8
  SPIWrite 0138,9b
  SPIWrite 0139,48
  SPIWrite 013a,3c
  SPIWrite 013b,49
  SPIWrite 013c,00
  SPIWrite 013d,68
  SPIWrite 013e,08
  SPIWrite 013f,60
  SPIWrite 0140,70
```

```
SPIWrite 0141,47
SPIWrite 0142,3b
SPIWrite 0143,49
SPIWrite 0144,01
SPIWrite 0145,28
SPIWrite 0146,f8
SPIWrite 0147,b5
SPIWrite 0148,09
SPIWrite 0149,d0
SPIWrite 014a,0a
SPIWrite 014b,68
SPIWrite 014c,22
SPIWrite 014d,f4
SPIWrite 014e,60
SPIWrite 014f,02
SPIWrite 0150,02
SPIWrite 0151,f5
SPIWrite 0152,00
SPIWrite 0153,12
SPIWrite 0154,0a
SPIWrite 0155,60
SPIWrite 0156,0a
SPIWrite 0157,68
SPIWrite 0158,22
SPIWrite 0159,f4
SPIWrite 015a,e0
SPIWrite 015b,12
SPIWrite 015c,08
SPIWrite 015d,e0
SPIWrite 015e,0a
SPIWrite 015f,68
SPIWrite 0160,22
SPIWrite 0161,f4
SPIWrite 0162,60
SPIWrite 0163,02
SPIWrite 0164,0a
SPIWrite 0165,60
SPIWrite 0166,0a
SPIWrite 0167,68
SPIWrite 0168,22
SPIWrite 0169,f4
SPIWrite 016a,e0
SPIWrite 016b,12
SPIWrite 016c,02
SPIWrite 016d,f5
SPIWrite 016e,80
SPIWrite 016f,22
SPIWrite 0170,30
SPIWrite 0171,4d
SPIWrite 0172,0a
SPIWrite 0173,60
SPIWrite 0174,00
SPIWrite 0175,23
SPIWrite 0176,2a
SPIWrite 0177,1d
SPIWrite 0178,0b
SPIWrite 0179,75
SPIWrite 017a,16
SPIWrite 017b,68
SPIWrite 017c,0c
SPIWrite 017d,68
SPIWrite 017e,1f
SPIWrite 017f,46
SPIWrite 0180,c6
SPIWrite 0181,f3
SPIWrite 0182,40
SPIWrite 0183,12
SPIWrite 0184,24
SPIWrite 0185,f0
```

```
SPIWrite 0186,02
SPIWrite 0187,04
SPIWrite 0188,02
SPIWrite 0189,eb
SPIWrite 018a,96
SPIWrite 018b,12
SPIWrite 018c,0c
SPIWrite 018d,60
SPIWrite 018e,0f
SPIWrite 018f,e0
SPIWrite 0190,34
SPIWrite 0191,46
SPIWrite 0192,64
SPIWrite 0193,1e
SPIWrite 0194,fd
SPIWrite 0195,d1
SPIWrite 0196,00
SPIWrite 0197,bf
SPIWrite 0198,5b
SPIWrite 0199,1c
SPIWrite 019a,1d
SPIWrite 019b,e0
SPIWrite 019c,37
SPIWrite 019d,46
SPIWrite 019e,7f
SPIWrite 019f,1e
SPIWrite 01a0,fd
SPIWrite 01a1,d1
SPIWrite 01a2,00
SPIWrite 01a3,bf
SPIWrite 01a4,6d
SPIWrite 01a5,1c
SPIWrite 01a6,13
SPIWrite 01a7,e0
SPIWrite 01a8,76
SPIWrite 01a9,1e
SPIWrite 01aa,fd
SPIWrite 01ab,d1
SPIWrite 01ac,00
SPIWrite 01ad,bf
SPIWrite 01ae,7f
SPIWrite 01af,1c
SPIWrite 01b0,13
SPIWrite 01b1,26
SPIWrite 01b2,ba
SPIWrite 01b3,42
SPIWrite 01b4,c0
SPIWrite 01b5,f2
SPIWrite 01b6,00
SPIWrite 01b7,06
SPIWrite 01b8,f6
SPIWrite 01b9,d8
SPIWrite 01ba,08
SPIWrite 01bb,35
SPIWrite 01bc,0c
SPIWrite 01bd,68
SPIWrite 01be,2f
SPIWrite 01bf,68
SPIWrite 01c0,44
SPIWrite 01c1,f0
SPIWrite 01c2,02
SPIWrite 01c3,04
SPIWrite 01c4,c7
SPIWrite 01c5,f3
SPIWrite 01c6,40
SPIWrite 01c7,1c
SPIWrite 01c8,1d
SPIWrite 01c9,46
SPIWrite 01ca,0c
```

```
SPIWrite 01cb,60
SPIWrite 01cc,0c
SPIWrite 01cd,eb
SPIWrite 01ce,97
SPIWrite 01cf,14
SPIWrite 01d0,ac
SPIWrite 01d1,42
SPIWrite 01d2,e3
SPIWrite 01d3,d8
SPIWrite 01d4,01
SPIWrite 01d5,24
SPIWrite 01d6,0c
SPIWrite 01d7,75
SPIWrite 01d8,9a
SPIWrite 01d9,42
SPIWrite 01da,d9
SPIWrite 01db,d8
SPIWrite 01dc,b1
SPIWrite 01dd,f9
SPIWrite 01de,10
SPIWrite 01df,10
SPIWrite 01e0,01
SPIWrite 01e1,28
SPIWrite 01e2,0c
SPIWrite 01e3,bf
SPIWrite 01e4,c1
SPIWrite 01e5,f5
SPIWrite 01e6,40
SPIWrite 01e7,61
SPIWrite 01e8,a1
SPIWrite 01e9,f5
SPIWrite 01ea,80
SPIWrite 01eb,61
SPIWrite 01ec,08
SPIWrite 01ed,b2
SPIWrite 01ee,f8
SPIWrite 01ef,bd
SPIWrite 01f0,af
SPIWrite 01f1,4a
SPIWrite 01f2,b2
SPIWrite 01f3,f9
SPIWrite 01f4,00
SPIWrite 01f5,20
SPIWrite 01f6,48
SPIWrite 01f7,43
SPIWrite 01f8,00
SPIWrite 01f9,28
SPIWrite 01fa,cc
SPIWrite 01fb,bf
SPIWrite 01fc,00
SPIWrite 01fd,eb
SPIWrite 01fe,62
SPIWrite 01ff,00
SPIWrite 0200,a0
SPIWrite 0201,eb
SPIWrite 0202,62
SPIWrite 0203,00
SPIWrite 0204,90
SPIWrite 0205,fb
SPIWrite 0206,f2
SPIWrite 0207,f0
SPIWrite 0208,70
SPIWrite 0209,47
SPIWrite 020a,03
SPIWrite 020b,46
SPIWrite 020c,00
SPIWrite 020d,28
SPIWrite 020e,b8
SPIWrite 020f,bf
```

```
1234   SPIWrite 0210,40
1235   SPIWrite 0211,42
1236   SPIWrite 0212,49
1237   SPIWrite 0213,b2
1238   SPIWrite 0214,01
1239   SPIWrite 0215,22
1240   SPIWrite 0216,49
1241   SPIWrite 0217,1e
1242   SPIWrite 0218,c9
1243   SPIWrite 0219,b2
1244   SPIWrite 021a,8a
1245   SPIWrite 021b,40
1246   SPIWrite 021c,51
1247   SPIWrite 021d,1e
1248   SPIWrite 021e,81
1249   SPIWrite 021f,42
1250   SPIWrite 0220,38
1251   SPIWrite 0221,bf
1252   SPIWrite 0222,08
1253   SPIWrite 0223,1c
1254   SPIWrite 0224,00
1255   SPIWrite 0225,2b
1256   SPIWrite 0226,48
1257   SPIWrite 0227,bf
1258   SPIWrite 0228,10
1259   SPIWrite 0229,44
1260   SPIWrite 022a,70
1261   SPIWrite 022b,47
1262   SPIWrite 022c,c0
1263   SPIWrite 022d,00
1264   SPIWrite 022e,03
1265   SPIWrite 022f,ad
1266   SPIWrite 0230,00
1267   SPIWrite 0231,05
1268   SPIWrite 0232,02
1269   SPIWrite 0233,ac
1270   SPIWrite 0234,34
1271   SPIWrite 0235,22
1272   SPIWrite 0236,01
1273   SPIWrite 0237,20
1274   SPIWrite 0238,2d
1275   SPIWrite 0239,e9
1276   SPIWrite 023a,f0
1277   SPIWrite 023b,4f
1278   SPIWrite 023c,df
1279   SPIWrite 023d,f8
1280   SPIWrite 023e,74
1281   SPIWrite 023f,82
1282   SPIWrite 0240,d8
1283   SPIWrite 0241,f8
1284   SPIWrite 0242,00
1285   SPIWrite 0243,32
1286   SPIWrite 0244,0c
1287   SPIWrite 0245,46
1288   SPIWrite 0246,81
1289   SPIWrite 0247,46
1290   SPIWrite 0248,01
1291   SPIWrite 0249,21
1292   SPIWrite 024a,00
1293   SPIWrite 024b,20
1294   SPIWrite 024c,0a
1295   SPIWrite 024d,46
1296   SPIWrite 024e,ad
1297   SPIWrite 024f,f1
1298   SPIWrite 0250,1c
1299   SPIWrite 0251,0d
1300   SPIWrite 0252,98
1301   SPIWrite 0253,47
1302   SPIWrite 0254,ff
```

```
  SPIWrite 0255,f7
  SPIWrite 0256,fc
  SPIWrite 0257,fe
  SPIWrite 0258,48
  SPIWrite 0259,46
  SPIWrite 025a,00
  SPIWrite 025b,2c
  SPIWrite 025c,05
  SPIWrite 025d,94
  SPIWrite 025e,00
  SPIWrite 025f,f0
  SPIWrite 0260,f7
  SPIWrite 0261,80
  SPIWrite 0262,df
  SPIWrite 0263,f8
  SPIWrite 0264,54
  SPIWrite 0265,82
  SPIWrite 0266,95
  SPIWrite 0267,4f
  SPIWrite 0268,40
  SPIWrite 0269,1e
  SPIWrite 026a,4f
  SPIWrite 026b,f0
  SPIWrite 026c,00
  SPIWrite 026d,0b
  SPIWrite 026e,04
  SPIWrite 026f,90
  SPIWrite 0270,04
  SPIWrite 0271,98
  SPIWrite 0272,66
  SPIWrite 0273,4b
  SPIWrite 0274,03
  SPIWrite 0275,25
  SPIWrite 0276,06
  SPIWrite 0277,26
  SPIWrite 0278,10
  SPIWrite 0279,f8
  SPIWrite 027a,01
  SPIWrite 027b,cf
  SPIWrite 027c,04
  SPIWrite 027d,90
  SPIWrite 027e,9c
  SPIWrite 027f,fb
  SPIWrite 0280,f5
  SPIWrite 0281,f2
  SPIWrite 0282,53
  SPIWrite 0283,f8
  SPIWrite 0284,04
  SPIWrite 0285,1b
  SPIWrite 0286,d1
  SPIWrite 0287,f8
  SPIWrite 0288,18
  SPIWrite 0289,01
  SPIWrite 028a,20
  SPIWrite 028b,f4
  SPIWrite 028c,00
  SPIWrite 028d,70
  SPIWrite 028e,c1
  SPIWrite 028f,f8
  SPIWrite 0290,18
  SPIWrite 0291,01
  SPIWrite 0292,08
  SPIWrite 0293,6e
  SPIWrite 0294,76
  SPIWrite 0295,1e
  SPIWrite 0296,20
  SPIWrite 0297,f0
  SPIWrite 0298,00
  SPIWrite 0299,70
```

```
SPIWrite 029a,08
SPIWrite 029b,66
SPIWrite 029c,f1
SPIWrite 029d,d1
SPIWrite 029e,5b
SPIWrite 029f,48
SPIWrite 02a0,50
SPIWrite 02a1,f8
SPIWrite 02a2,2c
SPIWrite 02a3,40
SPIWrite 02a4,d4
SPIWrite 02a5,f8
SPIWrite 02a6,18
SPIWrite 02a7,01
SPIWrite 02a8,40
SPIWrite 02a9,f4
SPIWrite 02aa,00
SPIWrite 02ab,70
SPIWrite 02ac,c4
SPIWrite 02ad,f8
SPIWrite 02ae,18
SPIWrite 02af,01
SPIWrite 02b0,20
SPIWrite 02b1,6e
SPIWrite 02b2,40
SPIWrite 02b3,f0
SPIWrite 02b4,80
SPIWrite 02b5,60
SPIWrite 02b6,20
SPIWrite 02b7,66
SPIWrite 02b8,20
SPIWrite 02b9,68
SPIWrite 02ba,01
SPIWrite 02bb,2a
SPIWrite 02bc,00
SPIWrite 02bd,90
SPIWrite 02be,0c
SPIWrite 02bf,d0
SPIWrite 02c0,d8
SPIWrite 02c1,f8
SPIWrite 02c2,00
SPIWrite 02c3,00
SPIWrite 02c4,20
SPIWrite 02c5,f0
SPIWrite 02c6,38
SPIWrite 02c7,00
SPIWrite 02c8,38
SPIWrite 02c9,30
SPIWrite 02ca,c8
SPIWrite 02cb,f8
SPIWrite 02cc,00
SPIWrite 02cd,00
SPIWrite 02ce,d8
SPIWrite 02cf,f8
SPIWrite 02d0,00
SPIWrite 02d1,00
SPIWrite 02d2,20
SPIWrite 02d3,f0
SPIWrite 02d4,07
SPIWrite 02d5,00
SPIWrite 02d6,c0
SPIWrite 02d7,1d
SPIWrite 02d8,0b
SPIWrite 02d9,e0
SPIWrite 02da,d8
SPIWrite 02db,f8
SPIWrite 02dc,00
SPIWrite 02dd,00
SPIWrite 02de,20
```

```
SPIWrite 02df,f0
SPIWrite 02e0,38
SPIWrite 02e1,00
SPIWrite 02e2,30
SPIWrite 02e3,30
SPIWrite 02e4,c8
SPIWrite 02e5,f8
SPIWrite 02e6,00
SPIWrite 02e7,00
SPIWrite 02e8,d8
SPIWrite 02e9,f8
SPIWrite 02ea,00
SPIWrite 02eb,00
SPIWrite 02ec,20
SPIWrite 02ed,f0
SPIWrite 02ee,07
SPIWrite 02ef,00
SPIWrite 02f0,80
SPIWrite 02f1,1d
SPIWrite 02f2,c8
SPIWrite 02f3,f8
SPIWrite 02f4,00
SPIWrite 02f5,00
SPIWrite 02f6,00
SPIWrite 02f7,20
SPIWrite 02f8,ff
SPIWrite 02f9,f7
SPIWrite 02fa,23
SPIWrite 02fb,ff
SPIWrite 02fc,05
SPIWrite 02fd,46
SPIWrite 02fe,01
SPIWrite 02ff,20
SPIWrite 0300,ff
SPIWrite 0301,f7
SPIWrite 0302,1f
SPIWrite 0303,ff
SPIWrite 0304,28
SPIWrite 0305,49
SPIWrite 0306,4d
SPIWrite 0307,60
SPIWrite 0308,0e
SPIWrite 0309,46
SPIWrite 030a,b0
SPIWrite 030b,60
SPIWrite 030c,21
SPIWrite 030d,6e
SPIWrite 030e,21
SPIWrite 030f,f0
SPIWrite 0310,80
SPIWrite 0311,61
SPIWrite 0312,21
SPIWrite 0313,66
SPIWrite 0314,21
SPIWrite 0315,6e
SPIWrite 0316,41
SPIWrite 0317,f0
SPIWrite 0318,00
SPIWrite 0319,71
SPIWrite 031a,21
SPIWrite 031b,66
SPIWrite 031c,61
SPIWrite 031d,6e
SPIWrite 031e,43
SPIWrite 031f,19
SPIWrite 0320,4f
SPIWrite 0321,ea
SPIWrite 0322,63
SPIWrite 0323,0a
```

```
  SPIWrite 0324,00
  SPIWrite 0325,26
  SPIWrite 0326,c1
  SPIWrite 0327,f3
  SPIWrite 0328,c0
  SPIWrite 0329,45
  SPIWrite 032a,00
  SPIWrite 032b,2d
  SPIWrite 032c,5d
  SPIWrite 032d,d1
  SPIWrite 032e,35
  SPIWrite 032f,46
  SPIWrite 0330,b1
  SPIWrite 0331,46
  SPIWrite 0332,23
  SPIWrite 0333,e0
  SPIWrite 0334,28
  SPIWrite 0335,46
  SPIWrite 0336,ff
  SPIWrite 0337,f7
  SPIWrite 0338,04
  SPIWrite 0339,ff
  SPIWrite 033a,b7
  SPIWrite 033b,f9
  SPIWrite 033c,00
  SPIWrite 033d,10
  SPIWrite 033e,aa
  SPIWrite 033f,eb
  SPIWrite 0340,00
  SPIWrite 0341,00
  SPIWrite 0342,ff
  SPIWrite 0343,f7
  SPIWrite 0344,55
  SPIWrite 0345,ff
  SPIWrite 0346,36
  SPIWrite 0347,1a
  SPIWrite 0348,03
  SPIWrite 0349,d4
  SPIWrite 034a,10
  SPIWrite 034b,2e
  SPIWrite 034c,a8
  SPIWrite 034d,bf
  SPIWrite 034e,0f
  SPIWrite 034f,26
  SPIWrite 0350,04
  SPIWrite 0351,e0
  SPIWrite 0352,16
  SPIWrite 0353,f1
  SPIWrite 0354,0f
  SPIWrite 0355,0f
  SPIWrite 0356,b8
  SPIWrite 0357,bf
  SPIWrite 0358,6f
  SPIWrite 0359,f0
  SPIWrite 035a,0e
  SPIWrite 035b,06
  SPIWrite 035c,30
  SPIWrite 035d,46
  SPIWrite 035e,05
  SPIWrite 035f,21
  SPIWrite 0360,ff
  SPIWrite 0361,f7
  SPIWrite 0362,53
  SPIWrite 0363,ff
  SPIWrite 0364,d4
  SPIWrite 0365,f8
  SPIWrite 0366,80
  SPIWrite 0367,10
  SPIWrite 0368,60
```

```
SPIWrite 0369,f3
SPIWrite 036a,1c
SPIWrite 036b,61
SPIWrite 036c,c4
SPIWrite 036d,f8
SPIWrite 036e,80
SPIWrite 036f,10
SPIWrite 0370,20
SPIWrite 0371,68
SPIWrite 0372,09
SPIWrite 0373,f1
SPIWrite 0374,01
SPIWrite 0375,03
SPIWrite 0376,5f
SPIWrite 0377,fa
SPIWrite 0378,83
SPIWrite 0379,f9
SPIWrite 037a,01
SPIWrite 037b,90
SPIWrite 037c,b8
SPIWrite 037d,79
SPIWrite 037e,48
SPIWrite 037f,45
SPIWrite 0380,d8
SPIWrite 0381,dc
SPIWrite 0382,2e
SPIWrite 0383,46
SPIWrite 0384,b0
SPIWrite 0385,42
SPIWrite 0386,59
SPIWrite 0387,dd
SPIWrite 0388,01
SPIWrite 0389,20
SPIWrite 038a,ff
SPIWrite 038b,f7
SPIWrite 038c,da
SPIWrite 038d,fe
SPIWrite 038e,b7
SPIWrite 038f,f9
SPIWrite 0390,02
SPIWrite 0391,10
SPIWrite 0392,aa
SPIWrite 0393,eb
SPIWrite 0394,00
SPIWrite 0395,00
SPIWrite 0396,ff
SPIWrite 0397,f7
SPIWrite 0398,2b
SPIWrite 0399,ff
SPIWrite 039a,45
SPIWrite 039b,19
SPIWrite 039c,06
SPIWrite 039d,d4
SPIWrite 039e,08
SPIWrite 039f,2d
SPIWrite 03a0,a8
SPIWrite 03a1,bf
SPIWrite 03a2,07
SPIWrite 03a3,25
SPIWrite 03a4,07
SPIWrite 03a5,e0
SPIWrite 03a6,c0
SPIWrite 03a7,46
SPIWrite 03a8,40
SPIWrite 03a9,22
SPIWrite 03aa,01
SPIWrite 03ab,20
SPIWrite 03ac,15
SPIWrite 03ad,f1
```

```
SPIWrite 03ae,07
SPIWrite 03af,0f
SPIWrite 03b0,b8
SPIWrite 03b1,bf
SPIWrite 03b2,6f
SPIWrite 03b3,f0
SPIWrite 03b4,06
SPIWrite 03b5,05
SPIWrite 03b6,00
SPIWrite 03b7,21
SPIWrite 03b8,00
SPIWrite 03b9,2d
SPIWrite 03ba,d8
SPIWrite 03bb,bf
SPIWrite 03bc,01
SPIWrite 03bd,21
SPIWrite 03be,20
SPIWrite 03bf,6f
SPIWrite 03c0,20
SPIWrite 03c1,f4
SPIWrite 03c2,00
SPIWrite 03c3,50
SPIWrite 03c4,40
SPIWrite 03c5,ea
SPIWrite 03c6,41
SPIWrite 03c7,30
SPIWrite 03c8,20
SPIWrite 03c9,67
SPIWrite 03ca,29
SPIWrite 03cb,46
SPIWrite 03cc,00
SPIWrite 03cd,29
SPIWrite 03ce,b8
SPIWrite 03cf,bf
SPIWrite 03d0,49
SPIWrite 03d1,42
SPIWrite 03d2,d4
SPIWrite 03d3,f8
SPIWrite 03d4,84
SPIWrite 03d5,00
SPIWrite 03d6,61
SPIWrite 03d7,f3
SPIWrite 03d8,8c
SPIWrite 03d9,20
SPIWrite 03da,c4
SPIWrite 03db,f8
SPIWrite 03dc,84
SPIWrite 03dd,00
SPIWrite 03de,b8
SPIWrite 03df,79
SPIWrite 03e0,21
SPIWrite 03e1,68
SPIWrite 03e2,76
SPIWrite 03e3,1c
SPIWrite 03e4,f6
SPIWrite 03e5,b2
SPIWrite 03e6,02
SPIWrite 03e7,91
SPIWrite 03e8,cc
SPIWrite 03e9,e7
SPIWrite 03ea,35
SPIWrite 03eb,46
SPIWrite 03ec,23
SPIWrite 03ed,e0
SPIWrite 03ee,01
SPIWrite 03ef,20
SPIWrite 03f0,ff
SPIWrite 03f1,f7
SPIWrite 03f2,a7
```

```
1717   SPIWrite 03f3,fe
1718   SPIWrite 03f4,b7
1719   SPIWrite 03f5,f9
1720   SPIWrite 03f6,00
1721   SPIWrite 03f7,10
1722   SPIWrite 03f8,aa
1723   SPIWrite 03f9,eb
1724   SPIWrite 03fa,00
1725   SPIWrite 03fb,00
1726   SPIWrite 03fc,ff
1727   SPIWrite 03fd,f7
1728   SPIWrite 03fe,f8
1729   SPIWrite 03ff,fe
1730   SPIWrite 0400,36
1731   SPIWrite 0401,1a
1732   SPIWrite 0402,05
1733   SPIWrite 0403,d4
1734   SPIWrite 0404,10
1735   SPIWrite 0405,2e
1736   SPIWrite 0406,a8
1737   SPIWrite 0407,bf
1738   SPIWrite 0408,0f
1739   SPIWrite 0409,26
1740   SPIWrite 040a,06
1741   SPIWrite 040b,e0
1742   SPIWrite 040c,c0
1743   SPIWrite 040d,75
1744   SPIWrite 040e,02
1745   SPIWrite 040f,00
1746   SPIWrite 0410,16
1747   SPIWrite 0411,f1
1748   SPIWrite 0412,0f
1749   SPIWrite 0413,0f
1750   SPIWrite 0414,b8
1751   SPIWrite 0415,bf
1752   SPIWrite 0416,6f
1753   SPIWrite 0417,f0
1754   SPIWrite 0418,0e
1755   SPIWrite 0419,06
1756   SPIWrite 041a,30
1757   SPIWrite 041b,46
1758   SPIWrite 041c,05
1759   SPIWrite 041d,21
1760   SPIWrite 041e,ff
1761   SPIWrite 041f,f7
1762   SPIWrite 0420,f4
1763   SPIWrite 0421,fe
1764   SPIWrite 0422,d4
1765   SPIWrite 0423,f8
1766   SPIWrite 0424,80
1767   SPIWrite 0425,10
1768   SPIWrite 0426,60
1769   SPIWrite 0427,f3
1770   SPIWrite 0428,1c
1771   SPIWrite 0429,61
1772   SPIWrite 042a,c4
1773   SPIWrite 042b,f8
1774   SPIWrite 042c,80
1775   SPIWrite 042d,10
1776   SPIWrite 042e,20
1777   SPIWrite 042f,68
1778   SPIWrite 0430,6d
1779   SPIWrite 0431,1c
1780   SPIWrite 0432,ed
1781   SPIWrite 0433,b2
1782   SPIWrite 0434,03
1783   SPIWrite 0435,90
1784   SPIWrite 0436,b8
1785   SPIWrite 0437,79
```

```
SPIWrite 0438,a8
SPIWrite 0439,42
SPIWrite 043a,d8
SPIWrite 043b,dc
SPIWrite 043c,20
SPIWrite 043d,6e
SPIWrite 043e,05
SPIWrite 043f,9e
SPIWrite 0440,0b
SPIWrite 0441,f1
SPIWrite 0442,01
SPIWrite 0443,0b
SPIWrite 0444,20
SPIWrite 0445,f0
SPIWrite 0446,00
SPIWrite 0447,70
SPIWrite 0448,5e
SPIWrite 0449,45
SPIWrite 044a,20
SPIWrite 044b,66
SPIWrite 044c,3f
SPIWrite 044d,f7
SPIWrite 044e,10
SPIWrite 044f,af
SPIWrite 0450,ff
SPIWrite 0451,f7
SPIWrite 0452,48
SPIWrite 0453,fe
SPIWrite 0454,17
SPIWrite 0455,48
SPIWrite 0456,d0
SPIWrite 0457,f8
SPIWrite 0458,04
SPIWrite 0459,32
SPIWrite 045a,01
SPIWrite 045b,21
SPIWrite 045c,0a
SPIWrite 045d,46
SPIWrite 045e,00
SPIWrite 045f,20
SPIWrite 0460,98
SPIWrite 0461,47
SPIWrite 0462,07
SPIWrite 0463,b0
SPIWrite 0464,bd
SPIWrite 0465,e8
SPIWrite 0466,f0
SPIWrite 0467,8f
SPIWrite 0468,5c
SPIWrite 0469,22
SPIWrite 046a,01
SPIWrite 046b,20
SPIWrite 046c,01
SPIWrite 046d,22
SPIWrite 046e,49
SPIWrite 046f,1e
SPIWrite 0470,8a
SPIWrite 0471,40
SPIWrite 0472,01
SPIWrite 0473,46
SPIWrite 0474,50
SPIWrite 0475,1e
SPIWrite 0476,11
SPIWrite 0477,42
SPIWrite 0478,01
SPIWrite 0479,ea
SPIWrite 047a,00
SPIWrite 047b,00
SPIWrite 047c,18
```

```
SPIWrite 047d,bf
SPIWrite 047e,40
SPIWrite 047f,42
SPIWrite 0480,70
SPIWrite 0481,47
SPIWrite 0482,01
SPIWrite 0483,46
SPIWrite 0484,1c
SPIWrite 0485,b5
SPIWrite 0486,00
SPIWrite 0487,20
SPIWrite 0488,01
SPIWrite 0489,24
SPIWrite 048a,02
SPIWrite 048b,46
SPIWrite 048c,04
SPIWrite 048d,fa
SPIWrite 048e,02
SPIWrite 048f,f3
SPIWrite 0490,19
SPIWrite 0491,42
SPIWrite 0492,03
SPIWrite 0493,d0
SPIWrite 0494,43
SPIWrite 0495,1c
SPIWrite 0496,00
SPIWrite 0497,f8
SPIWrite 0498,0d
SPIWrite 0499,20
SPIWrite 049a,d8
SPIWrite 049b,b2
SPIWrite 049c,52
SPIWrite 049d,1c
SPIWrite 049e,06
SPIWrite 049f,2a
SPIWrite 04a0,f4
SPIWrite 04a1,db
SPIWrite 04a2,18
SPIWrite 04a3,b1
SPIWrite 04a4,01
SPIWrite 04a5,46
SPIWrite 04a6,68
SPIWrite 04a7,46
SPIWrite 04a8,ff
SPIWrite 04a9,f7
SPIWrite 04aa,c6
SPIWrite 04ab,fe
SPIWrite 04ac,1c
SPIWrite 04ad,bd
SPIWrite 04ae,c0
SPIWrite 04af,46
SPIWrite 04b0,30
SPIWrite 04b1,22
SPIWrite 04b2,01
SPIWrite 04b3,20
SPIWrite 04b4,90
SPIWrite 04b5,d6
SPIWrite 04b6,00
SPIWrite 04b7,20
SPIWrite 04b8,04
SPIWrite 04b9,05
SPIWrite 04ba,02
SPIWrite 04bb,ac
SPIWrite 04bc,2c
SPIWrite 04bd,22
SPIWrite 04be,01
SPIWrite 04bf,20
SPIWrite 04c0,10
SPIWrite 04c1,b5
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```
SPIWrite 04c2,b7
SPIWrite 04c3,4b
SPIWrite 04c4,b5
SPIWrite 04c5,4c
SPIWrite 04c6,03
SPIWrite 04c7,22
SPIWrite 04c8,10
SPIWrite 04c9,fb
SPIWrite 04ca,02
SPIWrite 04cb,10
SPIWrite 04cc,18
SPIWrite 04cd,5c
SPIWrite 04ce,20
SPIWrite 04cf,5c
SPIWrite 04d0,80
SPIWrite 04d1,00
SPIWrite 04d2,c0
SPIWrite 04d3,b2
SPIWrite 04d4,10
SPIWrite 04d5,bd
SPIWrite 04d6,2d
SPIWrite 04d7,e9
SPIWrite 04d8,f0
SPIWrite 04d9,4f
SPIWrite 04da,ad
SPIWrite 04db,f1
SPIWrite 04dc,34
SPIWrite 04dd,0d
SPIWrite 04de,08
SPIWrite 04df,90
SPIWrite 04e0,e8
SPIWrite 04e1,f7
SPIWrite 04e2,2c
SPIWrite 04e3,fc
SPIWrite 04e4,af
SPIWrite 04e5,4a
SPIWrite 04e6,06
SPIWrite 04e7,27
SPIWrite 04e8,10
SPIWrite 04e9,46
SPIWrite 04ea,00
SPIWrite 04eb,21
SPIWrite 04ec,7f
SPIWrite 04ed,1e
SPIWrite 04ee,00
SPIWrite 04ef,f8
SPIWrite 04f0,01
SPIWrite 04f1,1b
SPIWrite 04f2,fa
SPIWrite 04f3,d1
SPIWrite 04f4,aa
SPIWrite 04f5,49
SPIWrite 04f6,08
SPIWrite 04f7,98
SPIWrite 04f8,ac
SPIWrite 04f9,4c
SPIWrite 04fa,89
SPIWrite 04fb,1f
SPIWrite 04fc,08
SPIWrite 04fd,18
SPIWrite 04fe,80
SPIWrite 04ff,78
SPIWrite 0500,b1
SPIWrite 0501,f8
SPIWrite 0502,9e
SPIWrite 0503,31
SPIWrite 0504,20
SPIWrite 0505,5c
SPIWrite 0506,4f
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```
SPIWrite 0507,f0
SPIWrite 0508,01
SPIWrite 0509,0a
SPIWrite 050a,89
SPIWrite 050b,46
SPIWrite 050c,58
SPIWrite 050d,43
SPIWrite 050e,09
SPIWrite 050f,90
SPIWrite 0510,a8
SPIWrite 0511,48
SPIWrite 0512,d0
SPIWrite 0513,f8
SPIWrite 0514,d8
SPIWrite 0515,31
SPIWrite 0516,04
SPIWrite 0517,27
SPIWrite 0518,51
SPIWrite 0519,46
SPIWrite 051a,6a
SPIWrite 051b,46
SPIWrite 051c,08
SPIWrite 051d,98
SPIWrite 051e,8d
SPIWrite 051f,f8
SPIWrite 0520,00
SPIWrite 0521,70
SPIWrite 0522,98
SPIWrite 0523,47
SPIWrite 0524,ad
SPIWrite 0525,f1
SPIWrite 0526,01
SPIWrite 0527,06
SPIWrite 0528,02
SPIWrite 0529,96
SPIWrite 052a,02
SPIWrite 052b,20
SPIWrite 052c,06
SPIWrite 052d,90
SPIWrite 052e,02
SPIWrite 052f,98
SPIWrite 0530,10
SPIWrite 0531,f8
SPIWrite 0532,01
SPIWrite 0533,1f
SPIWrite 0534,04
SPIWrite 0535,29
SPIWrite 0536,02
SPIWrite 0537,90
SPIWrite 0538,00
SPIWrite 0539,f0
SPIWrite 053a,90
SPIWrite 053b,80
SPIWrite 053c,9d
SPIWrite 053d,48
SPIWrite 053e,08
SPIWrite 053f,9c
SPIWrite 0540,d0
SPIWrite 0541,f8
SPIWrite 0542,f8
SPIWrite 0543,21
SPIWrite 0544,20
SPIWrite 0545,46
SPIWrite 0546,90
SPIWrite 0547,47
SPIWrite 0548,4f
SPIWrite 0549,f0
SPIWrite 054a,0d
SPIWrite 054b,0b
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SPIWrite 054c,98
SPIWrite 054d,49
SPIWrite 054e,0a
SPIWrite 054f,90
SPIWrite 0550,0b
SPIWrite 0551,fb
SPIWrite 0552,00
SPIWrite 0553,fb
SPIWrite 0554,40
SPIWrite 0555,18
SPIWrite 0556,80
SPIWrite 0557,7a
SPIWrite 0558,0f
SPIWrite 0559,46
SPIWrite 055a,0b
SPIWrite 055b,eb
SPIWrite 055c,07
SPIWrite 055d,01
SPIWrite 055e,0b
SPIWrite 055f,90
SPIWrite 0560,91
SPIWrite 0561,f8
SPIWrite 0562,22
SPIWrite 0563,00
SPIWrite 0564,ba
SPIWrite 0565,f1
SPIWrite 0566,01
SPIWrite 0567,0f
SPIWrite 0568,0c
SPIWrite 0569,90
SPIWrite 056a,4f
SPIWrite 056b,ea
SPIWrite 056c,44
SPIWrite 056d,00
SPIWrite 056e,0a
SPIWrite 056f,eb
SPIWrite 0570,00
SPIWrite 0571,02
SPIWrite 0572,0a
SPIWrite 0573,eb
SPIWrite 0574,00
SPIWrite 0575,01
SPIWrite 0576,a2
SPIWrite 0577,f1
SPIWrite 0578,01
SPIWrite 0579,02
SPIWrite 057a,a1
SPIWrite 057b,f1
SPIWrite 057c,01
SPIWrite 057d,01
SPIWrite 057e,d3
SPIWrite 057f,b2
SPIWrite 0580,c9
SPIWrite 0581,b2
SPIWrite 0582,4f
SPIWrite 0583,ea
SPIWrite 0584,61
SPIWrite 0585,02
SPIWrite 0586,0c
SPIWrite 0587,bf
SPIWrite 0588,02
SPIWrite 0589,21
SPIWrite 058a,01
SPIWrite 058b,21
SPIWrite 058c,8d
SPIWrite 058d,f8
SPIWrite 058e,04
SPIWrite 058f,30
SPIWrite 0590,09
```

```
SPIWrite 0591,18
SPIWrite 0592,49
SPIWrite 0593,1e
SPIWrite 0594,09
SPIWrite 0595,eb
SPIWrite 0596,02
SPIWrite 0597,00
SPIWrite 0598,90
SPIWrite 0599,f8
SPIWrite 059a,ed
SPIWrite 059b,70
SPIWrite 059c,8d
SPIWrite 059d,f8
SPIWrite 059e,05
SPIWrite 059f,10
SPIWrite 05a0,00
SPIWrite 05a1,2f
SPIWrite 05a2,0c
SPIWrite 05a3,bf
SPIWrite 05a4,01
SPIWrite 05a5,20
SPIWrite 05a6,02
SPIWrite 05a7,20
SPIWrite 05a8,07
SPIWrite 05a9,90
SPIWrite 05aa,0d
SPIWrite 05ab,f1
SPIWrite 05ac,03
SPIWrite 05ad,00
SPIWrite 05ae,03
SPIWrite 05af,90
SPIWrite 05b0,03
SPIWrite 05b1,98
SPIWrite 05b2,10
SPIWrite 05b3,f8
SPIWrite 05b4,01
SPIWrite 05b5,6f
SPIWrite 05b6,03
SPIWrite 05b7,90
SPIWrite 05b8,06
SPIWrite 05b9,eb
SPIWrite 05ba,09
SPIWrite 05bb,01
SPIWrite 05bc,91
SPIWrite 05bd,f8
SPIWrite 05be,6e
SPIWrite 05bf,00
SPIWrite 05c0,40
SPIWrite 05c1,1c
SPIWrite 05c2,c7
SPIWrite 05c3,b2
SPIWrite 05c4,00
SPIWrite 05c5,2f
SPIWrite 05c6,45
SPIWrite 05c7,d0
SPIWrite 05c8,7b
SPIWrite 05c9,48
SPIWrite 05ca,dd
SPIWrite 05cb,f8
SPIWrite 05cc,28
SPIWrite 05cd,80
SPIWrite 05ce,75
SPIWrite 05cf,4d
SPIWrite 05d0,e1
SPIWrite 05d1,31
SPIWrite 05d2,00
SPIWrite 05d3,24
SPIWrite 05d4,04
SPIWrite 05d5,91
```

```
SPIWrite 05d6,30
SPIWrite 05d7,18
SPIWrite 05d8,11
SPIWrite 05d9,30
SPIWrite 05da,a8
SPIWrite 05db,44
SPIWrite 05dc,05
SPIWrite 05dd,90
SPIWrite 05de,05
SPIWrite 05df,98
SPIWrite 05e0,04
SPIWrite 05e1,99
SPIWrite 05e2,03
SPIWrite 05e3,78
SPIWrite 05e4,98
SPIWrite 05e5,f8
SPIWrite 05e6,00
SPIWrite 05e7,50
SPIWrite 05e8,08
SPIWrite 05e9,78
SPIWrite 05ea,23
SPIWrite 05eb,b1
SPIWrite 05ec,72
SPIWrite 05ed,48
SPIWrite 05ee,04
SPIWrite 05ef,eb
SPIWrite 05f0,46
SPIWrite 05f1,01
SPIWrite 05f2,40
SPIWrite 05f3,18
SPIWrite 05f4,40
SPIWrite 05f5,7d
SPIWrite 05f6,0c
SPIWrite 05f7,99
SPIWrite 05f8,a9
SPIWrite 05f9,42
SPIWrite 05fa,27
SPIWrite 05fb,dd
SPIWrite 05fc,0b
SPIWrite 05fd,99
SPIWrite 05fe,81
SPIWrite 05ff,42
SPIWrite 0600,24
SPIWrite 0601,d1
SPIWrite 0602,6c
SPIWrite 0603,49
SPIWrite 0604,d1
SPIWrite 0605,f8
SPIWrite 0606,2c
SPIWrite 0607,c4
SPIWrite 0608,99
SPIWrite 0609,f8
SPIWrite 060a,cc
SPIWrite 060b,30
SPIWrite 060c,0b
SPIWrite 060d,9a
SPIWrite 060e,e0
SPIWrite 060f,00
SPIWrite 0610,00
SPIWrite 0611,eb
SPIWrite 0612,06
SPIWrite 0613,10
SPIWrite 0614,48
SPIWrite 0615,44
SPIWrite 0616,09
SPIWrite 0617,99
SPIWrite 0618,c0
SPIWrite 0619,68
SPIWrite 061a,e0
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```
SPIWrite 061b,47
SPIWrite 061c,64
SPIWrite 061d,49
SPIWrite 061e,4f
SPIWrite 061f,f4
SPIWrite 0620,7a
SPIWrite 0621,72
SPIWrite 0622,b0
SPIWrite 0623,fb
SPIWrite 0624,f2
SPIWrite 0625,f0
SPIWrite 0626,59
SPIWrite 0627,44
SPIWrite 0628,01
SPIWrite 0629,eb
SPIWrite 062a,45
SPIWrite 062b,01
SPIWrite 062c,a1
SPIWrite 062d,f8
SPIWrite 062e,23
SPIWrite 062f,00
SPIWrite 0630,08
SPIWrite 0631,98
SPIWrite 0632,51
SPIWrite 0633,46
SPIWrite 0634,ff
SPIWrite 0635,f7
SPIWrite 0636,44
SPIWrite 0637,ff
SPIWrite 0638,5d
SPIWrite 0639,49
SPIWrite 063a,98
SPIWrite 063b,f8
SPIWrite 063c,00
SPIWrite 063d,30
SPIWrite 063e,59
SPIWrite 063f,44
SPIWrite 0640,6d
SPIWrite 0641,18
SPIWrite 0642,85
SPIWrite 0643,f8
SPIWrite 0644,2b
SPIWrite 0645,00
SPIWrite 0646,59
SPIWrite 0647,1c
SPIWrite 0648,88
SPIWrite 0649,f8
SPIWrite 064a,00
SPIWrite 064b,10
SPIWrite 064c,7f
SPIWrite 064d,1e
SPIWrite 064e,04
SPIWrite 064f,f1
SPIWrite 0650,01
SPIWrite 0651,04
SPIWrite 0652,c4
SPIWrite 0653,d1
SPIWrite 0654,07
SPIWrite 0655,98
SPIWrite 0656,40
SPIWrite 0657,1e
SPIWrite 0658,07
SPIWrite 0659,90
SPIWrite 065a,a9
SPIWrite 065b,d1
SPIWrite 065c,06
SPIWrite 065d,98
SPIWrite 065e,40
SPIWrite 065f,1e
```

```
SPIWrite 0660,06
SPIWrite 0661,90
SPIWrite 0662,7f
SPIWrite 0663,f4
SPIWrite 0664,64
SPIWrite 0665,af
SPIWrite 0666,0a
SPIWrite 0667,f1
SPIWrite 0668,01
SPIWrite 0669,0a
SPIWrite 066a,ba
SPIWrite 066b,f1
SPIWrite 066c,03
SPIWrite 066d,0f
SPIWrite 066e,ff
SPIWrite 066f,f6
SPIWrite 0670,4f
SPIWrite 0671,af
SPIWrite 0672,0d
SPIWrite 0673,b0
SPIWrite 0674,bd
SPIWrite 0675,e8
SPIWrite 0676,f0
SPIWrite 0677,8f
SPIWrite 0678,2d
SPIWrite 0679,e9
SPIWrite 067a,f0
SPIWrite 067b,4f
SPIWrite 067c,81
SPIWrite 067d,46
SPIWrite 067e,ad
SPIWrite 067f,f1
SPIWrite 0680,24
SPIWrite 0681,0d
SPIWrite 0682,e8
SPIWrite 0683,f7
SPIWrite 0684,51
SPIWrite 0685,fc
SPIWrite 0686,48
SPIWrite 0687,4c
SPIWrite 0688,4a
SPIWrite 0689,4f
SPIWrite 068a,48
SPIWrite 068b,4a
SPIWrite 068c,05
SPIWrite 068d,90
SPIWrite 068e,04
SPIWrite 068f,eb
SPIWrite 0690,09
SPIWrite 0691,00
SPIWrite 0692,d7
SPIWrite 0693,f8
SPIWrite 0694,d8
SPIWrite 0695,31
SPIWrite 0696,b4
SPIWrite 0697,f8
SPIWrite 0698,9e
SPIWrite 0699,61
SPIWrite 069a,01
SPIWrite 069b,79
SPIWrite 069c,04
SPIWrite 069d,20
SPIWrite 069e,55
SPIWrite 069f,5c
SPIWrite 06a0,8d
SPIWrite 06a1,f8
SPIWrite 06a2,00
SPIWrite 06a3,00
SPIWrite 06a4,00
```

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  SPIWrite 06a5,21
  SPIWrite 06a6,48
  SPIWrite 06a7,46
  SPIWrite 06a8,6a
  SPIWrite 06a9,46
  SPIWrite 06aa,98
  SPIWrite 06ab,47
  SPIWrite 06ac,4f
  SPIWrite 06ad,f0
  SPIWrite 06ae,02
  SPIWrite 06af,0b
  SPIWrite 06b0,75
  SPIWrite 06b1,43
  SPIWrite 06b2,ad
  SPIWrite 06b3,f1
  SPIWrite 06b4,01
  SPIWrite 06b5,00
  SPIWrite 06b6,06
  SPIWrite 06b7,95
  SPIWrite 06b8,df
  SPIWrite 06b9,f8
  SPIWrite 06ba,f4
  SPIWrite 06bb,a0
  SPIWrite 06bc,01
  SPIWrite 06bd,90
  SPIWrite 06be,09
  SPIWrite 06bf,eb
  SPIWrite 06c0,04
  SPIWrite 06c1,00
  SPIWrite 06c2,02
  SPIWrite 06c3,90
  SPIWrite 06c4,01
  SPIWrite 06c5,98
  SPIWrite 06c6,10
  SPIWrite 06c7,f8
  SPIWrite 06c8,01
  SPIWrite 06c9,1f
  SPIWrite 06ca,04
  SPIWrite 06cb,29
  SPIWrite 06cc,01
  SPIWrite 06cd,90
  SPIWrite 06ce,5e
  SPIWrite 06cf,d0
  SPIWrite 06d0,38
  SPIWrite 06d1,48
  SPIWrite 06d2,d0
  SPIWrite 06d3,f8
  SPIWrite 06d4,f8
  SPIWrite 06d5,21
  SPIWrite 06d6,48
  SPIWrite 06d7,46
  SPIWrite 06d8,90
  SPIWrite 06d9,47
  SPIWrite 06da,01
  SPIWrite 06db,46
  SPIWrite 06dc,02
  SPIWrite 06dd,98
  SPIWrite 06de,4f
  SPIWrite 06df,f0
  SPIWrite 06e0,0d
  SPIWrite 06e1,08
  SPIWrite 06e2,01
  SPIWrite 06e3,eb
  SPIWrite 06e4,0a
  SPIWrite 06e5,03
  SPIWrite 06e6,08
  SPIWrite 06e7,fb
  SPIWrite 06e8,01
  SPIWrite 06e9,f8
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SPIWrite 06ea,08
SPIWrite 06eb,eb
SPIWrite 06ec,0a
SPIWrite 06ed,02
SPIWrite 06ee,9b
SPIWrite 06ef,7a
SPIWrite 06f0,90
SPIWrite 06f1,f8
SPIWrite 06f2,df
SPIWrite 06f3,00
SPIWrite 06f4,92
SPIWrite 06f5,f8
SPIWrite 06f6,22
SPIWrite 06f7,20
SPIWrite 06f8,07
SPIWrite 06f9,93
SPIWrite 06fa,40
SPIWrite 06fb,1c
SPIWrite 06fc,c7
SPIWrite 06fd,b2
SPIWrite 06fe,08
SPIWrite 06ff,92
SPIWrite 0700,00
SPIWrite 0701,2f
SPIWrite 0702,44
SPIWrite 0703,d0
SPIWrite 0704,02
SPIWrite 0705,9a
SPIWrite 0706,2c
SPIWrite 0707,48
SPIWrite 0708,26
SPIWrite 0709,4d
SPIWrite 070a,00
SPIWrite 070b,26
SPIWrite 070c,e5
SPIWrite 070d,32
SPIWrite 070e,48
SPIWrite 070f,44
SPIWrite 0710,6d
SPIWrite 0711,18
SPIWrite 0712,03
SPIWrite 0713,92
SPIWrite 0714,21
SPIWrite 0715,30
SPIWrite 0716,04
SPIWrite 0717,90
SPIWrite 0718,04
SPIWrite 0719,98
SPIWrite 071a,03
SPIWrite 071b,9a
SPIWrite 071c,03
SPIWrite 071d,78
SPIWrite 071e,2c
SPIWrite 071f,78
SPIWrite 0720,10
SPIWrite 0721,78
SPIWrite 0722,2b
SPIWrite 0723,b1
SPIWrite 0724,24
SPIWrite 0725,48
SPIWrite 0726,06
SPIWrite 0727,eb
SPIWrite 0728,89
SPIWrite 0729,01
SPIWrite 072a,40
SPIWrite 072b,18
SPIWrite 072c,90
SPIWrite 072d,f8
SPIWrite 072e,23
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SPIWrite 072f,00
SPIWrite 0730,08
SPIWrite 0731,99
SPIWrite 0732,a1
SPIWrite 0733,42
SPIWrite 0734,27
SPIWrite 0735,dd
SPIWrite 0736,07
SPIWrite 0737,99
SPIWrite 0738,81
SPIWrite 0739,42
SPIWrite 073a,24
SPIWrite 073b,d1
SPIWrite 073c,1d
SPIWrite 073d,4b
SPIWrite 073e,1a
SPIWrite 073f,48
SPIWrite 0740,d3
SPIWrite 0741,f8
SPIWrite 0742,2c
SPIWrite 0743,c4
SPIWrite 0744,07
SPIWrite 0745,9a
SPIWrite 0746,b1
SPIWrite 0747,00
SPIWrite 0748,01
SPIWrite 0749,eb
SPIWrite 074a,09
SPIWrite 074b,11
SPIWrite 074c,40
SPIWrite 074d,18
SPIWrite 074e,16
SPIWrite 074f,49
SPIWrite 0750,c0
SPIWrite 0751,6c
SPIWrite 0752,91
SPIWrite 0753,f8
SPIWrite 0754,ce
SPIWrite 0755,30
SPIWrite 0756,06
SPIWrite 0757,99
SPIWrite 0758,e0
SPIWrite 0759,47
SPIWrite 075a,08
SPIWrite 075b,eb
SPIWrite 075c,0a
SPIWrite 075d,01
SPIWrite 075e,4f
SPIWrite 075f,f4
SPIWrite 0760,7a
SPIWrite 0761,72
SPIWrite 0762,01
SPIWrite 0763,eb
SPIWrite 0764,44
SPIWrite 0765,01
SPIWrite 0766,b0
SPIWrite 0767,fb
SPIWrite 0768,f2
SPIWrite 0769,f0
SPIWrite 076a,a1
SPIWrite 076b,f8
SPIWrite 076c,23
SPIWrite 076d,00
SPIWrite 076e,00
SPIWrite 076f,21
SPIWrite 0770,48
SPIWrite 0771,46
SPIWrite 0772,ff
SPIWrite 0773,f7
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SPIWrite 0774,a5
SPIWrite 0775,fe
SPIWrite 0776,2b
SPIWrite 0777,78
SPIWrite 0778,08
SPIWrite 0779,eb
SPIWrite 077a,0a
SPIWrite 077b,01
SPIWrite 077c,64
SPIWrite 077d,18
SPIWrite 077e,84
SPIWrite 077f,f8
SPIWrite 0780,2b
SPIWrite 0781,00
SPIWrite 0782,59
SPIWrite 0783,1c
SPIWrite 0784,29
SPIWrite 0785,70
SPIWrite 0786,7f
SPIWrite 0787,1e
SPIWrite 0788,06
SPIWrite 0789,f1
SPIWrite 078a,01
SPIWrite 078b,06
SPIWrite 078c,c4
SPIWrite 078d,d1
SPIWrite 078e,bb
SPIWrite 078f,f1
SPIWrite 0790,01
SPIWrite 0791,0b
SPIWrite 0792,97
SPIWrite 0793,d1
SPIWrite 0794,05
SPIWrite 0795,98
SPIWrite 0796,09
SPIWrite 0797,b0
SPIWrite 0798,bd
SPIWrite 0799,e8
SPIWrite 079a,f0
SPIWrite 079b,8f
SPIWrite 079c,31
SPIWrite 079d,78
SPIWrite 079e,02
SPIWrite 079f,00
SPIWrite 07a0,ba
SPIWrite 07a1,01
SPIWrite 07a2,01
SPIWrite 07a3,20
SPIWrite 07a4,54
SPIWrite 07a5,22
SPIWrite 07a6,01
SPIWrite 07a7,20
SPIWrite 07a8,b4
SPIWrite 07a9,01
SPIWrite 07aa,01
SPIWrite 07ab,20
SPIWrite 07ac,ac
SPIWrite 07ad,78
SPIWrite 07ae,02
SPIWrite 07af,00
SPIWrite 07b0,98
SPIWrite 07b1,0e
SPIWrite 07b2,01
SPIWrite 07b3,20
SPIWrite 07b4,90
SPIWrite 07b5,d6
SPIWrite 07b6,00
SPIWrite 07b7,20
SPIWrite 07b8,a0
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SPIWrite 07b9,13
SPIWrite 07ba,01
SPIWrite 07bb,20
SPIWrite 07bc,2d
SPIWrite 07bd,e9
SPIWrite 07be,f8
SPIWrite 07bf,4f
SPIWrite 07c0,89
SPIWrite 07c1,46
SPIWrite 07c2,a5
SPIWrite 07c3,4a
SPIWrite 07c4,a5
SPIWrite 07c5,49
SPIWrite 07c6,80
SPIWrite 07c7,46
SPIWrite 07c8,4f
SPIWrite 07c9,ea
SPIWrite 07ca,68
SPIWrite 07cb,00
SPIWrite 07cc,a1
SPIWrite 07cd,4b
SPIWrite 07ce,12
SPIWrite 07cf,5c
SPIWrite 07d0,09
SPIWrite 07d1,88
SPIWrite 07d2,a4
SPIWrite 07d3,48
SPIWrite 07d4,9c
SPIWrite 07d5,5c
SPIWrite 07d6,00
SPIWrite 07d7,68
SPIWrite 07d8,a1
SPIWrite 07d9,4a
SPIWrite 07da,03
SPIWrite 07db,46
SPIWrite 07dc,4c
SPIWrite 07dd,43
SPIWrite 07de,02
SPIWrite 07df,eb
SPIWrite 07e0,c8
SPIWrite 07e1,02
SPIWrite 07e2,01
SPIWrite 07e3,20
SPIWrite 07e4,21
SPIWrite 07e5,46
SPIWrite 07e6,98
SPIWrite 07e7,47
SPIWrite 07e8,df
SPIWrite 07e9,f8
SPIWrite 07ea,7c
SPIWrite 07eb,c2
SPIWrite 07ec,4f
SPIWrite 07ed,ea
SPIWrite 07ee,08
SPIWrite 07ef,1a
SPIWrite 07f0,00
SPIWrite 07f1,25
SPIWrite 07f2,56
SPIWrite 07f3,46
SPIWrite 07f4,22
SPIWrite 07f5,46
SPIWrite 07f6,02
SPIWrite 07f7,24
SPIWrite 07f8,4f
SPIWrite 07f9,ea
SPIWrite 07fa,12
SPIWrite 07fb,1e
SPIWrite 07fc,0a
SPIWrite 07fd,eb
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SPIWrite 07fe,05
SPIWrite 07ff,03
SPIWrite 0800,06
SPIWrite 0801,eb
SPIWrite 0802,0c
SPIWrite 0803,00
SPIWrite 0804,02
SPIWrite 0805,27
SPIWrite 0806,63
SPIWrite 0807,44
SPIWrite 0808,90
SPIWrite 0809,30
SPIWrite 080a,03
SPIWrite 080b,f5
SPIWrite 080c,20
SPIWrite 080d,7b
SPIWrite 080e,50
SPIWrite 080f,f8
SPIWrite 0810,04
SPIWrite 0811,3b
SPIWrite 0812,19
SPIWrite 0813,01
SPIWrite 0814,7f
SPIWrite 0815,1e
SPIWrite 0816,b1
SPIWrite 0817,fb
SPIWrite 0818,f2
SPIWrite 0819,f1
SPIWrite 081a,0e
SPIWrite 081b,fb
SPIWrite 081c,11
SPIWrite 081d,31
SPIWrite 081e,4b
SPIWrite 081f,f8
SPIWrite 0018,00    //sys_calib_macro_memory=0x0;   Address(0x18[7:0])
SPIWrite 0018,20    //macro=0x1;    Address(0x18[7:5])
SPIRead 00f0

//Read  MACRO_READY=0x1;    Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,08    //MACRO_OPERAND_REG0=0x8000000;
Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00
SPIWrite 00a1,00
SPIWrite 00a0,00
SPIWrite 00a7,00    //MACRO_OPERAND_REG1=0x0;
Address(0xa4[7:0],0xa5[7:0],0xa6[7:0],0xa7[7:0],0xa8[7:0])
SPIWrite 00a6,00
SPIWrite 00a5,00
SPIWrite 00a4,00
SPIWrite 0193,78    //MACRO_OPCODE=0x78;    Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0

//Read  MACRO_DONE=0x1;     Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIRead 00f0

//Read  MACRO_ERROR=0x0;    Address(0xf0[7:3])

SPIRead 00f1

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```
2819   //Read  MACRO_ERROR_OPCODE=0x0;     Address(0xf1[7:0],0xf2[7:0])
2820
2821   SPIRead 00f0
2822
2823   //Read  MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])
2824
2825   SPIRead 00f0
2826
2827   //Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;     Address(0xf0[7:5])
2828
2829   SPIRead 00f0
2830
2831   //Read  MACRO_ERROR_IN_OPERAND=0x0;     Address(0xf0[7:6])
2832
2833   SPIRead 00f0
2834
2835   //Read  MACRO_ERROR_IN_EXECUTION=0x0;   Address(0xf0[7:7])
2836
2837   SPIRead 00f3
2838   SPIRead 00f2
2839
2840   //Read  MACRO_ERROR_EXTENDED_CODE=0x0;  Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
2841
2842   SPIRead 00f7
2843   SPIRead 00f6
2844   SPIRead 00f5
2845   SPIRead 00f4
2846
2847   //Read  MACRO_ERROR_EXTENDED_CODE_2=0x0;
       Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
2848
2849   SPIWrite 0144,00    //all_addr_high=0x0;    Address(0x144[7:2])
2850   SPIWrite 0018,00    //macro=0x0;    Address(0x18[7:5])
2851   SPIWrite 0018,01    //sys_calib_macro_memory=0x1;   Address(0x18[7:0])
2852   SPIWrite 0020,08
2853   SPIWrite 0021,1b
2854   SPIWrite 0022,f4
2855   SPIWrite 0023,d1
2856   SPIWrite 0024,64
2857   SPIWrite 0025,1e
2858   SPIWrite 0026,06
2859   SPIWrite 0027,f1
2860   SPIWrite 0028,08
2861   SPIWrite 0029,06
2862   SPIWrite 002a,05
2863   SPIWrite 002b,f1
2864   SPIWrite 002c,04
2865   SPIWrite 002d,05
2866   SPIWrite 002e,e5
2867   SPIWrite 002f,d1
2868   SPIWrite 0030,40
2869   SPIWrite 0031,46
2870   SPIWrite 0032,49
2871   SPIWrite 0033,46
2872   SPIWrite 0034,e2
2873   SPIWrite 0035,f7
2874   SPIWrite 0036,7c
2875   SPIWrite 0037,f9
2876   SPIWrite 0038,bd
2877   SPIWrite 0039,e8
2878   SPIWrite 003a,f8
2879   SPIWrite 003b,8f
2880   SPIWrite 003c,70
2881   SPIWrite 003d,b5
2882   SPIWrite 003e,02
2883   SPIWrite 003f,46
2884   SPIWrite 0040,d2
2885   SPIWrite 0041,f8
2886   SPIWrite 0042,a4
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  SPIWrite 0043,60
  SPIWrite 0044,d2
  SPIWrite 0045,f8
  SPIWrite 0046,44
  SPIWrite 0047,51
  SPIWrite 0048,d2
  SPIWrite 0049,f8
  SPIWrite 004a,04
  SPIWrite 004b,41
  SPIWrite 004c,08
  SPIWrite 004d,46
  SPIWrite 004e,02
  SPIWrite 004f,28
  SPIWrite 0050,0d
  SPIWrite 0051,db
  SPIWrite 0052,40
  SPIWrite 0053,1e
  SPIWrite 0054,01
  SPIWrite 0055,21
  SPIWrite 0056,02
  SPIWrite 0057,eb
  SPIWrite 0058,81
  SPIWrite 0059,03
  SPIWrite 005a,c3
  SPIWrite 005b,f8
  SPIWrite 005c,a4
  SPIWrite 005d,60
  SPIWrite 005e,40
  SPIWrite 005f,1e
  SPIWrite 0060,c3
  SPIWrite 0061,f8
  SPIWrite 0062,44
  SPIWrite 0063,51
  SPIWrite 0064,01
  SPIWrite 0065,f1
  SPIWrite 0066,01
  SPIWrite 0067,01
  SPIWrite 0068,c3
  SPIWrite 0069,f8
  SPIWrite 006a,04
  SPIWrite 006b,41
  SPIWrite 006c,f3
  SPIWrite 006d,d1
  SPIWrite 006e,70
  SPIWrite 006f,bd
  SPIWrite 0070,10
  SPIWrite 0071,b5
  SPIWrite 0072,04
  SPIWrite 0073,46
  SPIWrite 0074,7d
  SPIWrite 0075,48
  SPIWrite 0076,04
  SPIWrite 0077,70
  SPIWrite 0078,20
  SPIWrite 0079,46
  SPIWrite 007a,e2
  SPIWrite 007b,f7
  SPIWrite 007c,9d
  SPIWrite 007d,fc
  SPIWrite 007e,7c
  SPIWrite 007f,48
  SPIWrite 0080,50
  SPIWrite 0081,f8
  SPIWrite 0082,24
  SPIWrite 0083,00
  SPIWrite 0084,0f
  SPIWrite 0085,21
  SPIWrite 0086,ff
  SPIWrite 0087,f7
```

```
SPIWrite 0088,d9
SPIWrite 0089,ff
SPIWrite 008a,10
SPIWrite 008b,bd
SPIWrite 008c,70
SPIWrite 008d,b5
SPIWrite 008e,04
SPIWrite 008f,46
SPIWrite 0090,78
SPIWrite 0091,48
SPIWrite 0092,00
SPIWrite 0093,68
SPIWrite 0094,16
SPIWrite 0095,46
SPIWrite 0096,0d
SPIWrite 0097,46
SPIWrite 0098,80
SPIWrite 0099,47
SPIWrite 009a,01
SPIWrite 009b,28
SPIWrite 009c,31
SPIWrite 009d,46
SPIWrite 009e,3c
SPIWrite 009f,d1
SPIWrite 00a0,4f
SPIWrite 00a1,f0
SPIWrite 00a2,29
SPIWrite 00a3,42
SPIWrite 00a4,92
SPIWrite 00a5,f8
SPIWrite 00a6,77
SPIWrite 00a7,00
SPIWrite 00a8,40
SPIWrite 00a9,f0
SPIWrite 00aa,08
SPIWrite 00ab,00
SPIWrite 00ac,82
SPIWrite 00ad,f8
SPIWrite 00ae,77
SPIWrite 00af,00
SPIWrite 00b0,92
SPIWrite 00b1,f8
SPIWrite 00b2,82
SPIWrite 00b3,00
SPIWrite 00b4,00
SPIWrite 00b5,f0
SPIWrite 00b6,c3
SPIWrite 00b7,00
SPIWrite 00b8,0c
SPIWrite 00b9,30
SPIWrite 00ba,82
SPIWrite 00bb,f8
SPIWrite 00bc,82
SPIWrite 00bd,00
SPIWrite 00be,05
SPIWrite 00bf,eb
SPIWrite 00c0,04
SPIWrite 00c1,15
SPIWrite 00c2,82
SPIWrite 00c3,f8
SPIWrite 00c4,76
SPIWrite 00c5,50
SPIWrite 00c6,92
SPIWrite 00c7,f8
SPIWrite 00c8,77
SPIWrite 00c9,00
SPIWrite 00ca,01
SPIWrite 00cb,f0
SPIWrite 00cc,03
```

```
  SPIWrite 00cd,01
  SPIWrite 00ce,00
  SPIWrite 00cf,f0
  SPIWrite 00d0,fc
  SPIWrite 00d1,00
  SPIWrite 00d2,01
  SPIWrite 00d3,43
  SPIWrite 00d4,82
  SPIWrite 00d5,f8
  SPIWrite 00d6,77
  SPIWrite 00d7,10
  SPIWrite 00d8,92
  SPIWrite 00d9,f8
  SPIWrite 00da,77
  SPIWrite 00db,00
  SPIWrite 00dc,00
  SPIWrite 00dd,f0
  SPIWrite 00de,fb
  SPIWrite 00df,00
  SPIWrite 00e0,82
  SPIWrite 00e1,f8
  SPIWrite 00e2,77
  SPIWrite 00e3,00
  SPIWrite 00e4,92
  SPIWrite 00e5,f8
  SPIWrite 00e6,77
  SPIWrite 00e7,00
  SPIWrite 00e8,40
  SPIWrite 00e9,f0
  SPIWrite 00ea,04
  SPIWrite 00eb,00
  SPIWrite 00ec,82
  SPIWrite 00ed,f8
  SPIWrite 00ee,77
  SPIWrite 00ef,00
  SPIWrite 00f0,92
  SPIWrite 00f1,f8
  SPIWrite 00f2,77
  SPIWrite 00f3,00
  SPIWrite 00f4,00
  SPIWrite 00f5,f0
  SPIWrite 00f6,f7
  SPIWrite 00f7,00
  SPIWrite 00f8,82
  SPIWrite 00f9,f8
  SPIWrite 00fa,77
  SPIWrite 00fb,00
  SPIWrite 00fc,92
  SPIWrite 00fd,f8
  SPIWrite 00fe,82
  SPIWrite 00ff,00
  SPIWrite 0100,00
  SPIWrite 0101,f0
  SPIWrite 0102,c3
  SPIWrite 0103,00
  SPIWrite 0104,82
  SPIWrite 0105,f8
  SPIWrite 0106,82
  SPIWrite 0107,00
  SPIWrite 0108,00
  SPIWrite 0109,26
  SPIWrite 010a,82
  SPIWrite 010b,f8
  SPIWrite 010c,76
  SPIWrite 010d,60
  SPIWrite 010e,92
  SPIWrite 010f,f8
  SPIWrite 0110,77
  SPIWrite 0111,00
```

```
SPIWrite 0112,00
SPIWrite 0113,f0
SPIWrite 0114,fc
SPIWrite 0115,00
SPIWrite 0116,82
SPIWrite 0117,f8
SPIWrite 0118,77
SPIWrite 0119,00
SPIWrite 011a,57
SPIWrite 011b,48
SPIWrite 011c,d0
SPIWrite 011d,f8
SPIWrite 011e,18
SPIWrite 011f,04
SPIWrite 0120,80
SPIWrite 0121,47
SPIWrite 0122,70
SPIWrite 0123,bd
SPIWrite 0124,70
SPIWrite 0125,b5
SPIWrite 0126,51
SPIWrite 0127,4c
SPIWrite 0128,54
SPIWrite 0129,4b
SPIWrite 012a,25
SPIWrite 012b,78
SPIWrite 012c,03
SPIWrite 012d,eb
SPIWrite 012e,65
SPIWrite 012f,04
SPIWrite 0130,a6
SPIWrite 0131,79
SPIWrite 0132,5b
SPIWrite 0133,19
SPIWrite 0134,9c
SPIWrite 0135,7a
SPIWrite 0136,52
SPIWrite 0137,4d
SPIWrite 0138,73
SPIWrite 0139,00
SPIWrite 013a,03
SPIWrite 013b,eb
SPIWrite 013c,c6
SPIWrite 013d,03
SPIWrite 013e,e4
SPIWrite 013f,18
SPIWrite 0140,2b
SPIWrite 0141,5d
SPIWrite 0142,06
SPIWrite 0143,2b
SPIWrite 0144,06
SPIWrite 0145,da
SPIWrite 0146,8a
SPIWrite 0147,00
SPIWrite 0148,83
SPIWrite 0149,08
SPIWrite 014a,b2
SPIWrite 014b,fb
SPIWrite 014c,f0
SPIWrite 014d,f0
SPIWrite 014e,03
SPIWrite 014f,fb
SPIWrite 0150,10
SPIWrite 0151,10
SPIWrite 0152,70
SPIWrite 0153,bd
SPIWrite 0154,e2
SPIWrite 0155,f7
SPIWrite 0156,4f
```

```
SPIWrite 0157,ff
SPIWrite 0158,70
SPIWrite 0159,bd
SPIWrite 015a,2d
SPIWrite 015b,e9
SPIWrite 015c,f0
SPIWrite 015d,43
SPIWrite 015e,4f
SPIWrite 015f,f0
SPIWrite 0160,00
SPIWrite 0161,08
SPIWrite 0162,04
SPIWrite 0163,46
SPIWrite 0164,15
SPIWrite 0165,46
SPIWrite 0166,ad
SPIWrite 0167,f1
SPIWrite 0168,14
SPIWrite 0169,0d
SPIWrite 016a,81
SPIWrite 016b,f8
SPIWrite 016c,00
SPIWrite 016d,80
SPIWrite 016e,e2
SPIWrite 016f,f7
SPIWrite 0170,5f
SPIWrite 0171,ff
SPIWrite 0172,42
SPIWrite 0173,4a
SPIWrite 0174,50
SPIWrite 0175,78
SPIWrite 0176,01
SPIWrite 0177,21
SPIWrite 0178,01
SPIWrite 0179,fa
SPIWrite 017a,04
SPIWrite 017b,f3
SPIWrite 017c,03
SPIWrite 017d,42
SPIWrite 017e,65
SPIWrite 017f,d0
SPIWrite 0180,42
SPIWrite 0181,4b
SPIWrite 0182,40
SPIWrite 0183,4e
SPIWrite 0184,14
SPIWrite 0185,20
SPIWrite 0186,17
SPIWrite 0187,19
SPIWrite 0188,14
SPIWrite 0189,fb
SPIWrite 018a,00
SPIWrite 018b,f0
SPIWrite 018c,1b
SPIWrite 018d,58
SPIWrite 018e,38
SPIWrite 018f,7a
SPIWrite 0190,3d
SPIWrite 0191,4f
SPIWrite 0192,30
SPIWrite 0193,5c
SPIWrite 0194,b7
SPIWrite 0195,f8
SPIWrite 0196,9e
SPIWrite 0197,61
SPIWrite 0198,70
SPIWrite 0199,43
SPIWrite 019a,18
SPIWrite 019b,26
```

```
  SPIWrite 019c,14
  SPIWrite 019d,fb
  SPIWrite 019e,06
  SPIWrite 019f,2c
  SPIWrite 01a0,0c
  SPIWrite 01a1,eb
  SPIWrite 01a2,c5
  SPIWrite 01a3,0e
  SPIWrite 01a4,de
  SPIWrite 01a5,f8
  SPIWrite 01a6,d0
  SPIWrite 01a7,60
  SPIWrite 01a8,b2
  SPIWrite 01a9,00
  SPIWrite 01aa,b2
  SPIWrite 01ab,fb
  SPIWrite 01ac,f0
  SPIWrite 01ad,f9
  SPIWrite 01ae,82
  SPIWrite 01af,08
  SPIWrite 01b0,02
  SPIWrite 01b1,fb
  SPIWrite 01b2,19
  SPIWrite 01b3,66
  SPIWrite 01b4,00
  SPIWrite 01b5,96
  SPIWrite 01b6,de
  SPIWrite 01b7,f8
  SPIWrite 01b8,d4
  SPIWrite 01b9,60
  SPIWrite 01ba,4f
  SPIWrite 01bb,ea
  SPIWrite 01bc,86
  SPIWrite 01bd,0e
  SPIWrite 01be,be
  SPIWrite 01bf,fb
  SPIWrite 01c0,f0
  SPIWrite 01c1,fe
  SPIWrite 01c2,02
  SPIWrite 01c3,fb
  SPIWrite 01c4,1e
  SPIWrite 01c5,66
  SPIWrite 01c6,01
  SPIWrite 01c7,96
  SPIWrite 01c8,dc
  SPIWrite 01c9,f8
  SPIWrite 01ca,e0
  SPIWrite 01cb,60
  SPIWrite 01cc,4f
  SPIWrite 01cd,ea
  SPIWrite 01ce,86
  SPIWrite 01cf,0e
  SPIWrite 01d0,be
  SPIWrite 01d1,fb
  SPIWrite 01d2,f0
  SPIWrite 01d3,fe
  SPIWrite 01d4,02
  SPIWrite 01d5,fb
  SPIWrite 01d6,1e
  SPIWrite 01d7,66
  SPIWrite 01d8,02
  SPIWrite 01d9,96
  SPIWrite 01da,dc
  SPIWrite 01db,f8
  SPIWrite 01dc,e4
  SPIWrite 01dd,60
  SPIWrite 01de,3f
  SPIWrite 01df,19
  SPIWrite 01e0,4f
```

```
SPIWrite 01e1,ea
SPIWrite 01e2,86
SPIWrite 01e3,0c
SPIWrite 01e4,bc
SPIWrite 01e5,fb
SPIWrite 01e6,f0
SPIWrite 01e7,f0
SPIWrite 01e8,02
SPIWrite 01e9,fb
SPIWrite 01ea,10
SPIWrite 01eb,60
SPIWrite 01ec,03
SPIWrite 01ed,90
SPIWrite 01ee,97
SPIWrite 01ef,f8
SPIWrite 01f0,6c
SPIWrite 01f1,00
SPIWrite 01f2,0a
SPIWrite 01f3,46
SPIWrite 01f4,03
SPIWrite 01f5,28
SPIWrite 01f6,07
SPIWrite 01f7,d0
SPIWrite 01f8,0a
SPIWrite 01f9,28
SPIWrite 01fa,05
SPIWrite 01fb,d0
SPIWrite 01fc,0b
SPIWrite 01fd,28
SPIWrite 01fe,03
SPIWrite 01ff,d0
SPIWrite 0200,0c
SPIWrite 0201,28
SPIWrite 0202,1c
SPIWrite 0203,bf
SPIWrite 0204,0d
SPIWrite 0205,28
SPIWrite 0206,42
SPIWrite 0207,46
SPIWrite 0208,12
SPIWrite 0209,fb
SPIWrite 020a,05
SPIWrite 020b,f0
SPIWrite 020c,4f
SPIWrite 020d,f4
SPIWrite 020e,80
SPIWrite 020f,72
SPIWrite 0210,04
SPIWrite 0211,27
SPIWrite 0212,ec
SPIWrite 0213,46
SPIWrite 0214,02
SPIWrite 0215,eb
SPIWrite 0216,40
SPIWrite 0217,12
SPIWrite 0218,96
SPIWrite 0219,b2
SPIWrite 021a,40
SPIWrite 021b,46
SPIWrite 021c,5c
SPIWrite 021d,f8
SPIWrite 021e,04
SPIWrite 021f,2b
SPIWrite 0220,35
SPIWrite 0221,18
SPIWrite 0222,7f
SPIWrite 0223,1e
SPIWrite 0224,00
SPIWrite 0225,f1
```

```
  SPIWrite 0226,04
  SPIWrite 0227,00
  SPIWrite 0228,5a
  SPIWrite 0229,51
  SPIWrite 022a,f7
  SPIWrite 022b,d1
  SPIWrite 022c,18
  SPIWrite 022d,4a
  SPIWrite 022e,15
  SPIWrite 022f,20
  SPIWrite 0230,14
  SPIWrite 0231,fb
  SPIWrite 0232,00
  SPIWrite 0233,f0
  SPIWrite 0234,10
  SPIWrite 0235,5c
  SPIWrite 0236,06
  SPIWrite 0237,28
  SPIWrite 0238,03
  SPIWrite 0239,d0
  SPIWrite 023a,40
  SPIWrite 023b,08
  SPIWrite 023c,2c
  SPIWrite 023d,bf
  SPIWrite 023e,0f
  SPIWrite 023f,21
  SPIWrite 0240,07
  SPIWrite 0241,21
  SPIWrite 0242,14
  SPIWrite 0243,48
  SPIWrite 0244,50
  SPIWrite 0245,f8
  SPIWrite 0246,24
  SPIWrite 0247,00
  SPIWrite 0248,ff
  SPIWrite 0249,f7
  SPIWrite 024a,f8
  SPIWrite 024b,fe
  SPIWrite 024c,05
  SPIWrite 024d,b0
  SPIWrite 024e,bd
  SPIWrite 024f,e8
  SPIWrite 0250,f0
  SPIWrite 0251,83
  SPIWrite 0252,c0
  SPIWrite 0253,46
  SPIWrite 0254,3b
  SPIWrite 0255,78
  SPIWrite 0256,02
  SPIWrite 0257,00
  SPIWrite 0258,17
  SPIWrite 0259,01
  SPIWrite 025a,01
  SPIWrite 025b,20
  SPIWrite 025c,52
  SPIWrite 025d,03
  SPIWrite 025e,01
  SPIWrite 025f,20
  SPIWrite 0260,34
  SPIWrite 0261,fe
  SPIWrite 0262,00
  SPIWrite 0263,20
  SPIWrite 0264,bc
  SPIWrite 0265,dc
  SPIWrite 0266,00
  SPIWrite 0267,20
  SPIWrite 0268,d4
  SPIWrite 0269,fb
  SPIWrite 026a,00
```

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3439   SPIWrite 026b,20
3440   SPIWrite 026c,62
3441   SPIWrite 026d,22
3442   SPIWrite 026e,01
3443   SPIWrite 026f,20
3444   SPIWrite 0270,9c
3445   SPIWrite 0271,77
3446   SPIWrite 0272,02
3447   SPIWrite 0273,00
3448   SPIWrite 0274,a4
3449   SPIWrite 0275,da
3450   SPIWrite 0276,00
3451   SPIWrite 0277,20
3452   SPIWrite 0278,90
3453   SPIWrite 0279,d6
3454   SPIWrite 027a,00
3455   SPIWrite 027b,20
3456   SPIWrite 027c,18
3457   SPIWrite 027d,ff
3458   SPIWrite 027e,00
3459   SPIWrite 027f,20
3460   SPIWrite 0280,b8
3461   SPIWrite 0281,16
3462   SPIWrite 0282,01
3463   SPIWrite 0283,20
3464   SPIWrite 0284,ac
3465   SPIWrite 0285,78
3466   SPIWrite 0286,02
3467   SPIWrite 0287,00
3468   SPIWrite 0288,b4
3469   SPIWrite 0289,01
3470   SPIWrite 028a,01
3471   SPIWrite 028b,20
3472   SPIWrite 028c,d8
3473   SPIWrite 028d,74
3474   SPIWrite 028e,02
3475   SPIWrite 028f,00
3476   SPIWrite 0290,32
3477   SPIWrite 0291,d4
3478   SPIWrite 0292,00
3479   SPIWrite 0293,20
3480   SPIWrite 0294,90
3481   SPIWrite 0295,78
3482   SPIWrite 0296,02
3483   SPIWrite 0297,00
3484   SPIWrite 0298,70
3485   SPIWrite 0299,47
3486   SPIWrite 029a,f8
3487   SPIWrite 029b,b5
3488   SPIWrite 029c,78
3489   SPIWrite 029d,4c
3490   SPIWrite 029e,84
3491   SPIWrite 029f,46
3492   SPIWrite 02a0,e0
3493   SPIWrite 02a1,79
3494   SPIWrite 02a2,64
3495   SPIWrite 02a3,79
3496   SPIWrite 02a4,24
3497   SPIWrite 02a5,18
3498   SPIWrite 02a6,02
3499   SPIWrite 02a7,2c
3500   SPIWrite 02a8,3a
3501   SPIWrite 02a9,d1
3502   SPIWrite 02aa,57
3503   SPIWrite 02ab,78
3504   SPIWrite 02ac,37
3505   SPIWrite 02ad,f0
3506   SPIWrite 02ae,02
3507   SPIWrite 02af,07
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3508   SPIWrite 02b0,36
3509   SPIWrite 02b1,d1
3510   SPIWrite 02b2,76
3511   SPIWrite 02b3,4c
3512   SPIWrite 02b4,74
3513   SPIWrite 02b5,4a
3514   SPIWrite 02b6,03
3515   SPIWrite 02b7,27
3516   SPIWrite 02b8,0c
3517   SPIWrite 02b9,20
3518   SPIWrite 02ba,1c
3519   SPIWrite 02bb,fb
3520   SPIWrite 02bc,07
3521   SPIWrite 02bd,15
3522   SPIWrite 02be,1c
3523   SPIWrite 02bf,fb
3524   SPIWrite 02c0,00
3525   SPIWrite 02c1,f0
3526   SPIWrite 02c2,00
3527   SPIWrite 02c3,eb
3528   SPIWrite 02c4,81
3529   SPIWrite 02c5,00
3530   SPIWrite 02c6,67
3531   SPIWrite 02c7,5d
3532   SPIWrite 02c8,12
3533   SPIWrite 02c9,58
3534   SPIWrite 02ca,6e
3535   SPIWrite 02cb,48
3536   SPIWrite 02cc,92
3537   SPIWrite 02cd,f9
3538   SPIWrite 02ce,90
3539   SPIWrite 02cf,54
3540   SPIWrite 02d0,dc
3541   SPIWrite 02d1,26
3542   SPIWrite 02d2,4f
3543   SPIWrite 02d3,f4
3544   SPIWrite 02d4,25
3545   SPIWrite 02d5,7e
3546   SPIWrite 02d6,11
3547   SPIWrite 02d7,fb
3548   SPIWrite 02d8,06
3549   SPIWrite 02d9,f6
3550   SPIWrite 02da,1c
3551   SPIWrite 02db,fb
3552   SPIWrite 02dc,0e
3553   SPIWrite 02dd,66
3554   SPIWrite 02de,94
3555   SPIWrite 02df,46
3556   SPIWrite 02e0,80
3557   SPIWrite 02e1,19
3558   SPIWrite 02e2,90
3559   SPIWrite 02e3,f9
3560   SPIWrite 02e4,89
3561   SPIWrite 02e5,10
3562   SPIWrite 02e6,90
3563   SPIWrite 02e7,f9
3564   SPIWrite 02e8,87
3565   SPIWrite 02e9,40
3566   SPIWrite 02ea,90
3567   SPIWrite 02eb,f9
3568   SPIWrite 02ec,86
3569   SPIWrite 02ed,20
3570   SPIWrite 02ee,9c
3571   SPIWrite 02ef,f9
3572   SPIWrite 02f0,91
3573   SPIWrite 02f1,64
3574   SPIWrite 02f2,90
3575   SPIWrite 02f3,f9
3576   SPIWrite 02f4,88
```

```
  SPIWrite 02f5,00
  SPIWrite 02f6,4f
  SPIWrite 02f7,b9
  SPIWrite 02f8,86
  SPIWrite 02f9,42
  SPIWrite 02fa,0e
  SPIWrite 02fb,bf
  SPIWrite 02fc,a5
  SPIWrite 02fd,42
  SPIWrite 02fe,01
  SPIWrite 02ff,21
  SPIWrite 0300,19
  SPIWrite 0301,70
  SPIWrite 0302,8c
  SPIWrite 0303,f8
  SPIWrite 0304,90
  SPIWrite 0305,44
  SPIWrite 0306,8c
  SPIWrite 0307,f8
  SPIWrite 0308,91
  SPIWrite 0309,04
  SPIWrite 030a,f8
  SPIWrite 030b,bd
  SPIWrite 030c,95
  SPIWrite 030d,42
  SPIWrite 030e,0e
  SPIWrite 030f,bf
  SPIWrite 0310,8e
  SPIWrite 0311,42
  SPIWrite 0312,01
  SPIWrite 0313,20
  SPIWrite 0314,18
  SPIWrite 0315,70
  SPIWrite 0316,8c
  SPIWrite 0317,f8
  SPIWrite 0318,91
  SPIWrite 0319,14
  SPIWrite 031a,8c
  SPIWrite 031b,f8
  SPIWrite 031c,90
  SPIWrite 031d,24
  SPIWrite 031e,f8
  SPIWrite 031f,bd
  SPIWrite 0320,60
  SPIWrite 0321,46
  SPIWrite 0322,ec
  SPIWrite 0323,f7
  SPIWrite 0324,29
  SPIWrite 0325,fe
  SPIWrite 0326,f8
  SPIWrite 0327,bd
  SPIWrite 0328,2d
  SPIWrite 0329,e9
  SPIWrite 032a,fe
  SPIWrite 032b,4f
  SPIWrite 032c,0c
  SPIWrite 032d,9e
  SPIWrite 032e,82
  SPIWrite 032f,46
  SPIWrite 0330,89
  SPIWrite 0331,46
  SPIWrite 0332,14
  SPIWrite 0333,46
  SPIWrite 0334,0d
  SPIWrite 0335,9f
  SPIWrite 0336,00
  SPIWrite 0337,96
  SPIWrite 0338,1d
  SPIWrite 0339,46
```

```
SPIWrite 033a,01
SPIWrite 033b,97
SPIWrite 033c,ec
SPIWrite 033d,f7
SPIWrite 033e,4a
SPIWrite 033f,ff
SPIWrite 0340,df
SPIWrite 0341,f8
SPIWrite 0342,48
SPIWrite 0343,b1
SPIWrite 0344,20
SPIWrite 0345,88
SPIWrite 0346,20
SPIWrite 0347,b9
SPIWrite 0348,60
SPIWrite 0349,88
SPIWrite 034a,00
SPIWrite 034b,28
SPIWrite 034c,4f
SPIWrite 034d,d0
SPIWrite 034e,01
SPIWrite 034f,20
SPIWrite 0350,4e
SPIWrite 0351,e0
SPIWrite 0352,63
SPIWrite 0353,88
SPIWrite 0354,00
SPIWrite 0355,2b
SPIWrite 0356,4a
SPIWrite 0357,d0
SPIWrite 0358,ea
SPIWrite 0359,f7
SPIWrite 035a,77
SPIWrite 035b,ff
SPIWrite 035c,80
SPIWrite 035d,46
SPIWrite 035e,60
SPIWrite 035f,88
SPIWrite 0360,ea
SPIWrite 0361,f7
SPIWrite 0362,73
SPIWrite 0363,ff
SPIWrite 0364,69
SPIWrite 0365,79
SPIWrite 0366,00
SPIWrite 0367,eb
SPIWrite 0368,80
SPIWrite 0369,00
SPIWrite 036a,08
SPIWrite 036b,eb
SPIWrite 036c,88
SPIWrite 036d,02
SPIWrite 036e,c0
SPIWrite 036f,13
SPIWrite 0370,d2
SPIWrite 0371,13
SPIWrite 0372,01
SPIWrite 0373,29
SPIWrite 0374,44
SPIWrite 0375,b2
SPIWrite 0376,53
SPIWrite 0377,b2
SPIWrite 0378,3f
SPIWrite 0379,d1
SPIWrite 037a,42
SPIWrite 037b,48
SPIWrite 037c,dc
SPIWrite 037d,21
SPIWrite 037e,4f
```

```
SPIWrite 037f,f4
SPIWrite 0380,25
SPIWrite 0381,72
SPIWrite 0382,19
SPIWrite 0383,fb
SPIWrite 0384,01
SPIWrite 0385,f1
SPIWrite 0386,1a
SPIWrite 0387,fb
SPIWrite 0388,02
SPIWrite 0389,11
SPIWrite 038a,b2
SPIWrite 038b,78
SPIWrite 038c,40
SPIWrite 038d,18
SPIWrite 038e,71
SPIWrite 038f,78
SPIWrite 0390,b0
SPIWrite 0391,f9
SPIWrite 0392,5a
SPIWrite 0393,c0
SPIWrite 0394,b0
SPIWrite 0395,f9
SPIWrite 0396,5c
SPIWrite 0397,60
SPIWrite 0398,c2
SPIWrite 0399,f1
SPIWrite 039a,01
SPIWrite 039b,02
SPIWrite 039c,c1
SPIWrite 039d,f1
SPIWrite 039e,01
SPIWrite 039f,01
SPIWrite 03a0,11
SPIWrite 03a1,fb
SPIWrite 03a2,0c
SPIWrite 03a3,f0
SPIWrite 03a4,c0
SPIWrite 03a5,eb
SPIWrite 03a6,43
SPIWrite 03a7,10
SPIWrite 03a8,12
SPIWrite 03a9,fb
SPIWrite 03aa,06
SPIWrite 03ab,f1
SPIWrite 03ac,40
SPIWrite 03ad,11
SPIWrite 03ae,c1
SPIWrite 03af,eb
SPIWrite 03b0,44
SPIWrite 03b1,11
SPIWrite 03b2,a0
SPIWrite 03b3,eb
SPIWrite 03b4,61
SPIWrite 03b5,10
SPIWrite 03b6,41
SPIWrite 03b7,b2
SPIWrite 03b8,08
SPIWrite 03b9,46
SPIWrite 03ba,00
SPIWrite 03bb,28
SPIWrite 03bc,b8
SPIWrite 03bd,bf
SPIWrite 03be,40
SPIWrite 03bf,42
SPIWrite 03c0,c2
SPIWrite 03c1,b2
SPIWrite 03c2,00
SPIWrite 03c3,29
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3784   SPIWrite 03c4,4f
3785   SPIWrite 03c5,f0
3786   SPIWrite 03c6,00
3787   SPIWrite 03c7,00
3788   SPIWrite 03c8,d8
3789   SPIWrite 03c9,bf
3790   SPIWrite 03ca,01
3791   SPIWrite 03cb,20
3792   SPIWrite 03cc,a9
3793   SPIWrite 03cd,79
3794   SPIWrite 03ce,91
3795   SPIWrite 03cf,42
3796   SPIWrite 03d0,0e
3797   SPIWrite 03d1,da
3798   SPIWrite 03d2,2b
3799   SPIWrite 03d3,78
3800   SPIWrite 03d4,c9
3801   SPIWrite 03d5,18
3802   SPIWrite 03d6,91
3803   SPIWrite 03d7,42
3804   SPIWrite 03d8,0a
3805   SPIWrite 03d9,db
3806   SPIWrite 03da,03
3807   SPIWrite 03db,22
3808   SPIWrite 03dc,59
3809   SPIWrite 03dd,46
3810   SPIWrite 03de,1a
3811   SPIWrite 03df,fb
3812   SPIWrite 03e0,02
3813   SPIWrite 03e1,92
3814   SPIWrite 03e2,89
3815   SPIWrite 03e3,5c
3816   SPIWrite 03e4,81
3817   SPIWrite 03e5,42
3818   SPIWrite 03e6,1c
3819   SPIWrite 03e7,bf
3820   SPIWrite 03e8,01
3821   SPIWrite 03e9,21
3822   SPIWrite 03ea,79
3823   SPIWrite 03eb,70
3824   SPIWrite 03ec,00
3825   SPIWrite 03ed,e0
3826   SPIWrite 03ee,00
3827   SPIWrite 03ef,20
3828   SPIWrite 03f0,03
3829   SPIWrite 03f1,22
3830   SPIWrite 03f2,59
3831   SPIWrite 03f3,46
3832   SPIWrite 03f4,1a
3833   SPIWrite 03f5,fb
3834   SPIWrite 03f6,02
3835   SPIWrite 03f7,92
3836   SPIWrite 03f8,88
3837   SPIWrite 03f9,54
3838   SPIWrite 03fa,bd
3839   SPIWrite 03fb,e8
3840   SPIWrite 03fc,fe
3841   SPIWrite 03fd,8f
3842   SPIWrite 03fe,2d
3843   SPIWrite 03ff,e9
3844   SPIWrite 0400,fc
3845   SPIWrite 0401,47
3846   SPIWrite 0402,24
3847   SPIWrite 0403,48
3848   SPIWrite 0404,df
3849   SPIWrite 0405,f8
3850   SPIWrite 0406,88
3851   SPIWrite 0407,90
3852   SPIWrite 0408,c9
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SPIWrite 0409,f8
SPIWrite 040a,3c
SPIWrite 040b,01
SPIWrite 040c,ed
SPIWrite 040d,f7
SPIWrite 040e,7e
SPIWrite 040f,f8
SPIWrite 0410,00
SPIWrite 0411,24
SPIWrite 0412,22
SPIWrite 0413,4d
SPIWrite 0414,20
SPIWrite 0415,48
SPIWrite 0416,df
SPIWrite 0417,f8
SPIWrite 0418,8c
SPIWrite 0419,80
SPIWrite 041a,23
SPIWrite 041b,4f
SPIWrite 041c,df
SPIWrite 041d,f8
SPIWrite 041e,80
SPIWrite 041f,a0
SPIWrite 0420,19
SPIWrite 0421,4e
SPIWrite 0422,8d
SPIWrite 0423,f8
SPIWrite 0424,04
SPIWrite 0425,40
SPIWrite 0426,6d
SPIWrite 0427,1e
SPIWrite 0428,c9
SPIWrite 0429,f8
SPIWrite 042a,3c
SPIWrite 042b,01
SPIWrite 042c,15
SPIWrite 042d,f8
SPIWrite 042e,01
SPIWrite 042f,0f
SPIWrite 0430,01
SPIWrite 0431,28
SPIWrite 0432,20
SPIWrite 0433,d1
SPIWrite 0434,1a
SPIWrite 0435,f8
SPIWrite 0436,04
SPIWrite 0437,00
SPIWrite 0438,e8
SPIWrite 0439,b9
SPIWrite 043a,18
SPIWrite 043b,f8
SPIWrite 043c,14
SPIWrite 043d,10
SPIWrite 043e,60
SPIWrite 043f,00
SPIWrite 0440,00
SPIWrite 0441,eb
SPIWrite 0442,84
SPIWrite 0443,00
SPIWrite 0444,3b
SPIWrite 0445,18
SPIWrite 0446,9a
SPIWrite 0447,78
SPIWrite 0448,60
SPIWrite 0449,10
SPIWrite 044a,01
SPIWrite 044b,2a
SPIWrite 044c,0c
SPIWrite 044d,d0
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SPIWrite 044e,82
SPIWrite 044f,00
SPIWrite 0450,02
SPIWrite 0451,eb
SPIWrite 0452,c0
SPIWrite 0453,02
SPIWrite 0454,02
SPIWrite 0455,eb
SPIWrite 0456,81
SPIWrite 0457,02
SPIWrite 0458,b0
SPIWrite 0459,58
SPIWrite 045a,d0
SPIWrite 045b,f8
SPIWrite 045c,00
SPIWrite 045d,14
SPIWrite 045e,21
SPIWrite 045f,f4
SPIWrite 0460,80
SPIWrite 0461,71
SPIWrite 0462,c0
SPIWrite 0463,f8
SPIWrite 0464,00
SPIWrite 0465,14
SPIWrite 0466,06
SPIWrite 0467,e0
SPIWrite 0468,01
SPIWrite 0469,aa
SPIWrite 046a,00
SPIWrite 046b,92
SPIWrite 046c,d9
SPIWrite 046d,f8
SPIWrite 046e,3c
SPIWrite 046f,c1
SPIWrite 0470,da
SPIWrite 0471,78
SPIWrite 0472,1b
SPIWrite 0473,1d
SPIWrite 0474,e0
SPIWrite 0475,47
SPIWrite 0476,64
SPIWrite 0477,1c
SPIWrite 0478,04
SPIWrite 0479,2c
SPIWrite 047a,d7
SPIWrite 047b,db
SPIWrite 047c,bd
SPIWrite 047d,e8
SPIWrite 047e,fc
SPIWrite 047f,87
SPIWrite 0480,e6
SPIWrite 0481,1d
SPIWrite 0482,01
SPIWrite 0483,20
SPIWrite 0484,e0
SPIWrite 0485,ab
SPIWrite 0486,00
SPIWrite 0487,20
SPIWrite 0488,a8
SPIWrite 0489,75
SPIWrite 048a,02
SPIWrite 048b,00
SPIWrite 048c,4c
SPIWrite 048d,22
SPIWrite 048e,01
SPIWrite 048f,20
SPIWrite 0490,90
SPIWrite 0491,d6
SPIWrite 0492,00
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SPIWrite 0493,20
SPIWrite 0494,79
SPIWrite 0495,0a
SPIWrite 0496,03
SPIWrite 0497,00
SPIWrite 0498,c5
SPIWrite 0499,d6
SPIWrite 049a,01
SPIWrite 049b,00
SPIWrite 049c,f0
SPIWrite 049d,1e
SPIWrite 049e,01
SPIWrite 049f,20
SPIWrite 04a0,f4
SPIWrite 04a1,1e
SPIWrite 04a2,01
SPIWrite 04a3,20
SPIWrite 04a4,06
SPIWrite 04a5,d6
SPIWrite 04a6,00
SPIWrite 04a7,20
SPIWrite 04a8,6c
SPIWrite 04a9,1a
SPIWrite 04aa,01
SPIWrite 04ab,20
SPIWrite 04ac,70
SPIWrite 04ad,b5
SPIWrite 04ae,46
SPIWrite 04af,49
SPIWrite 04b0,44
SPIWrite 04b1,4c
SPIWrite 04b2,c4
SPIWrite 04b3,f8
SPIWrite 04b4,fc
SPIWrite 04b5,10
SPIWrite 04b6,45
SPIWrite 04b7,48
SPIWrite 04b8,c4
SPIWrite 04b9,f8
SPIWrite 04ba,c4
SPIWrite 04bb,00
SPIWrite 04bc,44
SPIWrite 04bd,49
SPIWrite 04be,c4
SPIWrite 04bf,f8
SPIWrite 04c0,c0
SPIWrite 04c1,10
SPIWrite 04c2,44
SPIWrite 04c3,48
SPIWrite 04c4,c4
SPIWrite 04c5,f8
SPIWrite 04c6,30
SPIWrite 04c7,01
SPIWrite 04c8,43
SPIWrite 04c9,49
SPIWrite 04ca,c4
SPIWrite 04cb,f8
SPIWrite 04cc,40
SPIWrite 04cd,11
SPIWrite 04ce,43
SPIWrite 04cf,48
SPIWrite 04d0,c4
SPIWrite 04d1,f8
SPIWrite 04d2,38
SPIWrite 04d3,01
SPIWrite 04d4,4a
SPIWrite 04d5,49
SPIWrite 04d6,c4
SPIWrite 04d7,f8
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4060   SPIWrite 04d8,a8
4061   SPIWrite 04d9,16
4062   SPIWrite 04da,4a
4063   SPIWrite 04db,48
4064   SPIWrite 04dc,c4
4065   SPIWrite 04dd,f8
4066   SPIWrite 04de,ac
4067   SPIWrite 04df,06
4068   SPIWrite 04e0,49
4069   SPIWrite 04e1,49
4070   SPIWrite 04e2,c4
4071   SPIWrite 04e3,f8
4072   SPIWrite 04e4,f4
4073   SPIWrite 04e5,15
4074   SPIWrite 04e6,49
4075   SPIWrite 04e7,48
4076   SPIWrite 04e8,a0
4077   SPIWrite 04e9,64
4078   SPIWrite 04ea,3f
4079   SPIWrite 04eb,48
4080   SPIWrite 04ec,28
4081   SPIWrite 04ed,23
4082   SPIWrite 04ee,40
4083   SPIWrite 04ef,f2
4084   SPIWrite 04f0,b7
4085   SPIWrite 04f1,55
4086   SPIWrite 04f2,03
4087   SPIWrite 04f3,80
4088   SPIWrite 04f4,46
4089   SPIWrite 04f5,4a
4090   SPIWrite 04f6,85
4091   SPIWrite 04f7,80
4092   SPIWrite 04f8,46
4093   SPIWrite 04f9,49
4094   SPIWrite 04fa,c4
4095   SPIWrite 04fb,f8
4096   SPIWrite 04fc,3c
4097   SPIWrite 04fd,26
4098   SPIWrite 04fe,41
4099   SPIWrite 04ff,f2
4100   SPIWrite 0500,88
4101   SPIWrite 0501,33
4102   SPIWrite 0502,c3
4103   SPIWrite 0503,60
4104   SPIWrite 0504,00
4105   SPIWrite 0505,26
4106   SPIWrite 0506,c4
4107   SPIWrite 0507,f8
4108   SPIWrite 0508,30
4109   SPIWrite 0509,16
4110   SPIWrite 050a,a6
4111   SPIWrite 050b,21
4112   SPIWrite 050c,41
4113   SPIWrite 050d,80
4114   SPIWrite 050e,3b
4115   SPIWrite 050f,49
4116   SPIWrite 0510,41
4117   SPIWrite 0511,4a
4118   SPIWrite 0512,0e
4119   SPIWrite 0513,70
4120   SPIWrite 0514,35
4121   SPIWrite 0515,49
4122   SPIWrite 0516,c4
4123   SPIWrite 0517,f8
4124   SPIWrite 0518,40
4125   SPIWrite 0519,26
4126   SPIWrite 051a,31
4127   SPIWrite 051b,4b
4128   SPIWrite 051c,81
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SPIWrite 051d,60
SPIWrite 051e,03
SPIWrite 051f,22
SPIWrite 0520,82
SPIWrite 0521,71
SPIWrite 0522,30
SPIWrite 0523,4a
SPIWrite 0524,1a
SPIWrite 0525,60
SPIWrite 0526,32
SPIWrite 0527,4a
SPIWrite 0528,32
SPIWrite 0529,4d
SPIWrite 052a,02
SPIWrite 052b,61
SPIWrite 052c,32
SPIWrite 052d,48
SPIWrite 052e,a8
SPIWrite 052f,65
SPIWrite 0530,3a
SPIWrite 0531,48
SPIWrite 0532,c4
SPIWrite 0533,f8
SPIWrite 0534,34
SPIWrite 0535,06
SPIWrite 0536,00
SPIWrite 0537,f0
SPIWrite 0538,77
SPIWrite 0539,fc
SPIWrite 053a,00
SPIWrite 053b,f0
SPIWrite 053c,06
SPIWrite 053d,f9
SPIWrite 053e,38
SPIWrite 053f,48
SPIWrite 0540,38
SPIWrite 0541,49
SPIWrite 0542,00
SPIWrite 0543,f0
SPIWrite 0544,a3
SPIWrite 0545,f8
SPIWrite 0546,39
SPIWrite 0547,48
SPIWrite 0548,3a
SPIWrite 0549,49
SPIWrite 054a,c4
SPIWrite 054b,f8
SPIWrite 054c,70
SPIWrite 054d,09
SPIWrite 054e,3a
SPIWrite 054f,48
SPIWrite 0550,c4
SPIWrite 0551,f8
SPIWrite 0552,4c
SPIWrite 0553,15
SPIWrite 0554,39
SPIWrite 0555,49
SPIWrite 0556,c4
SPIWrite 0557,f8
SPIWrite 0558,38
SPIWrite 0559,06
SPIWrite 055a,39
SPIWrite 055b,48
SPIWrite 055c,c4
SPIWrite 055d,f8
SPIWrite 055e,c4
SPIWrite 055f,14
SPIWrite 0560,38
SPIWrite 0561,49
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SPIWrite 0562,c4
SPIWrite 0563,f8
SPIWrite 0564,94
SPIWrite 0565,04
SPIWrite 0566,38
SPIWrite 0567,48
SPIWrite 0568,c4
SPIWrite 0569,f8
SPIWrite 056a,98
SPIWrite 056b,14
SPIWrite 056c,37
SPIWrite 056d,49
SPIWrite 056e,c4
SPIWrite 056f,f8
SPIWrite 0570,00
SPIWrite 0571,02
SPIWrite 0572,38
SPIWrite 0573,48
SPIWrite 0574,c4
SPIWrite 0575,f8
SPIWrite 0576,04
SPIWrite 0577,12
SPIWrite 0578,37
SPIWrite 0579,49
SPIWrite 057a,c4
SPIWrite 057b,f8
SPIWrite 057c,24
SPIWrite 057d,03
SPIWrite 057e,37
SPIWrite 057f,48
SPIWrite 0580,c4
SPIWrite 0581,f8
SPIWrite 0582,94
SPIWrite 0583,11
SPIWrite 0584,2a
SPIWrite 0585,49
SPIWrite 0586,38
SPIWrite 0587,4a
SPIWrite 0588,0e
SPIWrite 0589,70
SPIWrite 058a,36
SPIWrite 058b,49
SPIWrite 058c,c4
SPIWrite 058d,f8
SPIWrite 058e,c4
SPIWrite 058f,02
SPIWrite 0590,33
SPIWrite 0591,48
SPIWrite 0592,c4
SPIWrite 0593,f8
SPIWrite 0594,4c
SPIWrite 0595,24
SPIWrite 0596,02
SPIWrite 0597,22
SPIWrite 0598,02
SPIWrite 0599,70
SPIWrite 059a,01
SPIWrite 059b,20
SPIWrite 059c,08
SPIWrite 059d,80
SPIWrite 059e,33
SPIWrite 059f,49
SPIWrite 05a0,0e
SPIWrite 05a1,70
SPIWrite 05a2,34
SPIWrite 05a3,49
SPIWrite 05a4,88
SPIWrite 05a5,70
SPIWrite 05a6,4a
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4267   SPIWrite 05a7,70
4268   SPIWrite 05a8,14
4269   SPIWrite 05a9,20
4270   SPIWrite 05aa,c8
4271   SPIWrite 05ab,70
4272   SPIWrite 05ac,8e
4273   SPIWrite 05ad,20
4274   SPIWrite 05ae,88
4275   SPIWrite 05af,80
4276   SPIWrite 05b0,1d
4277   SPIWrite 05b1,48
4278   SPIWrite 05b2,c5
4279   SPIWrite 05b3,f8
4280   SPIWrite 05b4,34
4281   SPIWrite 05b5,02
4282   SPIWrite 05b6,26
4283   SPIWrite 05b7,48
4284   SPIWrite 05b8,c5
4285   SPIWrite 05b9,f8
4286   SPIWrite 05ba,f8
4287   SPIWrite 05bb,00
4288   SPIWrite 05bc,2c
4289   SPIWrite 05bd,48
4290   SPIWrite 05be,c4
4291   SPIWrite 05bf,f8
4292   SPIWrite 05c0,c8
4293   SPIWrite 05c1,04
4294   SPIWrite 05c2,70
4295   SPIWrite 05c3,bd
4296   SPIWrite 05c4,90
4297   SPIWrite 05c5,d6
4298   SPIWrite 05c6,00
4299   SPIWrite 05c7,20
4300   SPIWrite 05c8,bf
4301   SPIWrite 05c9,10
4302   SPIWrite 05ca,03
4303   SPIWrite 05cb,00
4304   SPIWrite 05cc,41
4305   SPIWrite 05cd,10
4306   SPIWrite 05ce,03
4307   SPIWrite 05cf,00
4308   SPIWrite 05d0,c1
4309   SPIWrite 05d1,0f
4310   SPIWrite 05d2,03
4311   SPIWrite 05d3,00
4312   SPIWrite 05d4,df
4313   SPIWrite 05d5,0b
4314   SPIWrite 05d6,03
4315   SPIWrite 05d7,00
4316   SPIWrite 05d8,7b
4317   SPIWrite 05d9,0a
4318   SPIWrite 05da,03
4319   SPIWrite 05db,00
4320   SPIWrite 05dc,09
4321   SPIWrite 05dd,0b
4322   SPIWrite 05de,03
4323   SPIWrite 05df,00
4324   SPIWrite 05e0,5c
4325   SPIWrite 05e1,22
4326   SPIWrite 05e2,01
4327   SPIWrite 05e3,20
4328   SPIWrite 05e4,00
4329   SPIWrite 05e5,00
4330   SPIWrite 05e6,02
4331   SPIWrite 05e7,ac
4332   SPIWrite 05e8,2c
4333   SPIWrite 05e9,22
4334   SPIWrite 05ea,01
4335   SPIWrite 05eb,20
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4336   SPIWrite 05ec,40
4337   SPIWrite 05ed,78
4338   SPIWrite 05ee,7d
4339   SPIWrite 05ef,01
4340   SPIWrite 05f0,48
4341   SPIWrite 05f1,e8
4342   SPIWrite 05f2,01
4343   SPIWrite 05f3,00
4344   SPIWrite 05f4,d4
4345   SPIWrite 05f5,f7
4346   SPIWrite 05f6,00
4347   SPIWrite 05f7,20
4348   SPIWrite 05f8,09
4349   SPIWrite 05f9,11
4350   SPIWrite 05fa,03
4351   SPIWrite 05fb,00
4352   SPIWrite 05fc,2b
4353   SPIWrite 05fd,22
4354   SPIWrite 05fe,01
4355   SPIWrite 05ff,20
4356   SPIWrite 0600,57
4357   SPIWrite 0601,14
4358   SPIWrite 0602,03
4359   SPIWrite 0603,00
4360   SPIWrite 0604,4b
4361   SPIWrite 0605,14
4362   SPIWrite 0606,03
4363   SPIWrite 0607,00
4364   SPIWrite 0608,71
4365   SPIWrite 0609,15
4366   SPIWrite 060a,03
4367   SPIWrite 060b,00
4368   SPIWrite 060c,4b
4369   SPIWrite 060d,13
4370   SPIWrite 060e,03
4371   SPIWrite 060f,00
4372   SPIWrite 0610,9d
4373   SPIWrite 0611,07
4374   SPIWrite 0612,03
4375   SPIWrite 0613,00
4376   SPIWrite 0614,51
4377   SPIWrite 0615,08
4378   SPIWrite 0616,03
4379   SPIWrite 0617,00
4380   SPIWrite 0618,05
4381   SPIWrite 0619,09
4382   SPIWrite 061a,03
4383   SPIWrite 061b,00
4384   SPIWrite 061c,3b
4385   SPIWrite 061d,09
4386   SPIWrite 061e,03
4387   SPIWrite 061f,00
4388   SPIWrite 0620,38
4389   SPIWrite 0621,17
4390   SPIWrite 0622,03
4391   SPIWrite 0623,00
4392   SPIWrite 0624,60
4393   SPIWrite 0625,17
4394   SPIWrite 0626,03
4395   SPIWrite 0627,00
4396   SPIWrite 0628,05
4397   SPIWrite 0629,12
4398   SPIWrite 062a,03
4399   SPIWrite 062b,00
4400   SPIWrite 062c,67
4401   SPIWrite 062d,0f
4402   SPIWrite 062e,03
4403   SPIWrite 062f,00
4404   SPIWrite 0630,63
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SPIWrite 0631,22
SPIWrite 0632,01
SPIWrite 0633,20
SPIWrite 0634,d5
SPIWrite 0635,14
SPIWrite 0636,03
SPIWrite 0637,00
SPIWrite 0638,f1
SPIWrite 0639,0e
SPIWrite 063a,03
SPIWrite 063b,00
SPIWrite 063c,f5
SPIWrite 063d,15
SPIWrite 063e,03
SPIWrite 063f,00
SPIWrite 0640,b7
SPIWrite 0641,04
SPIWrite 0642,03
SPIWrite 0643,00
SPIWrite 0644,59
SPIWrite 0645,06
SPIWrite 0646,03
SPIWrite 0647,00
SPIWrite 0648,a9
SPIWrite 0649,15
SPIWrite 064a,03
SPIWrite 064b,00
SPIWrite 064c,b7
SPIWrite 064d,15
SPIWrite 064e,03
SPIWrite 064f,00
SPIWrite 0650,1b
SPIWrite 0651,11
SPIWrite 0652,03
SPIWrite 0653,00
SPIWrite 0654,d9
SPIWrite 0655,15
SPIWrite 0656,03
SPIWrite 0657,00
SPIWrite 0658,31
SPIWrite 0659,15
SPIWrite 065a,03
SPIWrite 065b,00
SPIWrite 065c,a3
SPIWrite 065d,14
SPIWrite 065e,03
SPIWrite 065f,00
SPIWrite 0660,64
SPIWrite 0661,22
SPIWrite 0662,01
SPIWrite 0663,20
SPIWrite 0664,60
SPIWrite 0665,22
SPIWrite 0666,01
SPIWrite 0667,20
SPIWrite 0668,31
SPIWrite 0669,12
SPIWrite 066a,03
SPIWrite 066b,00
SPIWrite 066c,a1
SPIWrite 066d,13
SPIWrite 066e,01
SPIWrite 066f,20
SPIWrite 0670,f7
SPIWrite 0671,15
SPIWrite 0672,03
SPIWrite 0673,00
SPIWrite 0674,3c
SPIWrite 0675,d6
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4474   SPIWrite 0676,00
4475   SPIWrite 0677,20
4476   SPIWrite 0678,3a
4477   SPIWrite 0679,b1
4478   SPIWrite 067a,03
4479   SPIWrite 067b,46
4480   SPIWrite 067c,10
4481   SPIWrite 067d,46
4482   SPIWrite 067e,13
4483   SPIWrite 067f,f8
4484   SPIWrite 0680,01
4485   SPIWrite 0681,2b
4486   SPIWrite 0682,40
4487   SPIWrite 0683,1e
4488   SPIWrite 0684,01
4489   SPIWrite 0685,f8
4490   SPIWrite 0686,01
4491   SPIWrite 0687,2b
4492   SPIWrite 0688,f9
4493   SPIWrite 0689,d1
4494   SPIWrite 068a,70
4495   SPIWrite 068b,47
4496   SPIWrite 068c,38
4497   SPIWrite 068d,b5
4498   SPIWrite 068e,05
4499   SPIWrite 068f,46
4500   SPIWrite 0690,0c
4501   SPIWrite 0691,46
4502   SPIWrite 0692,28
4503   SPIWrite 0693,68
4504   SPIWrite 0694,21
4505   SPIWrite 0695,68
4506   SPIWrite 0696,0c
4507   SPIWrite 0697,22
4508   SPIWrite 0698,ff
4509   SPIWrite 0699,f7
4510   SPIWrite 069a,ee
4511   SPIWrite 069b,ff
4512   SPIWrite 069c,68
4513   SPIWrite 069d,68
4514   SPIWrite 069e,61
4515   SPIWrite 069f,68
4516   SPIWrite 06a0,05
4517   SPIWrite 06a1,22
4518   SPIWrite 06a2,ff
4519   SPIWrite 06a3,f7
4520   SPIWrite 06a4,e9
4521   SPIWrite 06a5,ff
4522   SPIWrite 06a6,a8
4523   SPIWrite 06a7,68
4524   SPIWrite 06a8,a1
4525   SPIWrite 06a9,68
4526   SPIWrite 06aa,18
4527   SPIWrite 06ab,22
4528   SPIWrite 06ac,ff
4529   SPIWrite 06ad,f7
4530   SPIWrite 06ae,e4
4531   SPIWrite 06af,ff
4532   SPIWrite 06b0,e8
4533   SPIWrite 06b1,68
4534   SPIWrite 06b2,e1
4535   SPIWrite 06b3,68
4536   SPIWrite 06b4,d2
4537   SPIWrite 06b5,22
4538   SPIWrite 06b6,ff
4539   SPIWrite 06b7,f7
4540   SPIWrite 06b8,df
4541   SPIWrite 06b9,ff
4542   SPIWrite 06ba,28
```

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4543   SPIWrite 06bb,69
4544   SPIWrite 06bc,21
4545   SPIWrite 06bd,69
4546   SPIWrite 06be,96
4547   SPIWrite 06bf,22
4548   SPIWrite 06c0,ff
4549   SPIWrite 06c1,f7
4550   SPIWrite 06c2,da
4551   SPIWrite 06c3,ff
4552   SPIWrite 06c4,38
4553   SPIWrite 06c5,bd
4554   SPIWrite 06c6,b0
4555   SPIWrite 06c7,b5
4556   SPIWrite 06c8,39
4557   SPIWrite 06c9,49
4558   SPIWrite 06ca,3a
4559   SPIWrite 06cb,4d
4560   SPIWrite 06cc,00
4561   SPIWrite 06cd,f0
4562   SPIWrite 06ce,01
4563   SPIWrite 06cf,02
4564   SPIWrite 06d0,04
4565   SPIWrite 06d1,27
4566   SPIWrite 06d2,12
4567   SPIWrite 06d3,04
4568   SPIWrite 06d4,08
4569   SPIWrite 06d5,70
4570   SPIWrite 06d6,55
4571   SPIWrite 06d7,f8
4572   SPIWrite 06d8,04
4573   SPIWrite 06d9,4b
4574   SPIWrite 06da,d4
4575   SPIWrite 06db,f8
4576   SPIWrite 06dc,80
4577   SPIWrite 06dd,1b
4578   SPIWrite 06de,21
4579   SPIWrite 06df,f4
4580   SPIWrite 06e0,80
4581   SPIWrite 06e1,31
4582   SPIWrite 06e2,11
4583   SPIWrite 06e3,43
4584   SPIWrite 06e4,c4
4585   SPIWrite 06e5,f8
4586   SPIWrite 06e6,80
4587   SPIWrite 06e7,1b
4588   SPIWrite 06e8,d4
4589   SPIWrite 06e9,f8
4590   SPIWrite 06ea,48
4591   SPIWrite 06eb,3b
4592   SPIWrite 06ec,7f
4593   SPIWrite 06ed,1e
4594   SPIWrite 06ee,80
4595   SPIWrite 06ef,ea
4596   SPIWrite 06f0,03
4597   SPIWrite 06f1,01
4598   SPIWrite 06f2,01
4599   SPIWrite 06f3,f0
4600   SPIWrite 06f4,01
4601   SPIWrite 06f5,01
4602   SPIWrite 06f6,81
4603   SPIWrite 06f7,ea
4604   SPIWrite 06f8,03
4605   SPIWrite 06f9,01
4606   SPIWrite 06fa,c4
4607   SPIWrite 06fb,f8
4608   SPIWrite 06fc,48
4609   SPIWrite 06fd,1b
4610   SPIWrite 06fe,ea
4611   SPIWrite 06ff,d1
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SPIWrite 0700,01
SPIWrite 0701,28
SPIWrite 0702,0c
SPIWrite 0703,bf
SPIWrite 0704,2c
SPIWrite 0705,48
SPIWrite 0706,2d
SPIWrite 0707,48
SPIWrite 0708,2d
SPIWrite 0709,49
SPIWrite 070a,ff
SPIWrite 070b,f7
SPIWrite 070c,bf
SPIWrite 070d,ff
SPIWrite 070e,b0
SPIWrite 070f,bd
SPIWrite 0710,8c
SPIWrite 0711,46
SPIWrite 0712,2c
SPIWrite 0713,49
SPIWrite 0714,f8
SPIWrite 0715,b5
SPIWrite 0716,09
SPIWrite 0717,5c
SPIWrite 0718,01
SPIWrite 0719,29
SPIWrite 071a,12
SPIWrite 071b,d1
SPIWrite 071c,2a
SPIWrite 071d,49
SPIWrite 071e,46
SPIWrite 071f,01
SPIWrite 0720,02
SPIWrite 0721,23
SPIWrite 0722,00
SPIWrite 0723,24
SPIWrite 0724,32
SPIWrite 0725,19
SPIWrite 0726,02
SPIWrite 0727,27
SPIWrite 0728,8a
SPIWrite 0729,18
SPIWrite 072a,b2
SPIWrite 072b,f9
SPIWrite 072c,00
SPIWrite 072d,50
SPIWrite 072e,7f
SPIWrite 072f,1e
SPIWrite 0730,4f
SPIWrite 0731,ea
SPIWrite 0732,45
SPIWrite 0733,05
SPIWrite 0734,22
SPIWrite 0735,f8
SPIWrite 0736,10
SPIWrite 0737,5b
SPIWrite 0738,f7
SPIWrite 0739,d1
SPIWrite 073a,5b
SPIWrite 073b,1e
SPIWrite 073c,04
SPIWrite 073d,f1
SPIWrite 073e,08
SPIWrite 073f,04
SPIWrite 0740,f0
SPIWrite 0741,d1
SPIWrite 0742,61
SPIWrite 0743,46
SPIWrite 0744,e1
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SPIWrite 0745,f7
SPIWrite 0746,f0
SPIWrite 0747,fe
SPIWrite 0748,f8
SPIWrite 0749,bd
SPIWrite 074a,98
SPIWrite 074b,b5
SPIWrite 074c,1f
SPIWrite 074d,4c
SPIWrite 074e,00
SPIWrite 074f,21
SPIWrite 0750,84
SPIWrite 0751,f8
SPIWrite 0752,24
SPIWrite 0753,10
SPIWrite 0754,1f
SPIWrite 0755,48
SPIWrite 0756,84
SPIWrite 0757,f8
SPIWrite 0758,25
SPIWrite 0759,10
SPIWrite 075a,03
SPIWrite 075b,22
SPIWrite 075c,84
SPIWrite 075d,f8
SPIWrite 075e,29
SPIWrite 075f,10
SPIWrite 0760,1b
SPIWrite 0761,4b
SPIWrite 0762,84
SPIWrite 0763,f8
SPIWrite 0764,2a
SPIWrite 0765,10
SPIWrite 0766,0a
SPIWrite 0767,21
SPIWrite 0768,40
SPIWrite 0769,1e
SPIWrite 076a,10
SPIWrite 076b,f8
SPIWrite 076c,01
SPIWrite 076d,4f
SPIWrite 076e,05
SPIWrite 076f,27
SPIWrite 0770,7f
SPIWrite 0771,1e
SPIWrite 0772,03
SPIWrite 0773,f8
SPIWrite 0774,01
SPIWrite 0775,4b
SPIWrite 0776,fb
SPIWrite 0777,d1
SPIWrite 0778,49
SPIWrite 0779,1e
SPIWrite 077a,f6
SPIWrite 077b,d1
SPIWrite 077c,52
SPIWrite 077d,1e
SPIWrite 077e,00
SPIWrite 077f,f1
SPIWrite 0780,01
SPIWrite 0781,00
SPIWrite 0782,f0
SPIWrite 0783,d1
SPIWrite 0784,98
SPIWrite 0785,bd
SPIWrite 0786,0a
SPIWrite 0787,4a
SPIWrite 0788,80
SPIWrite 0789,b5
```

```
SPIWrite 078a,12
SPIWrite 078b,78
SPIWrite 078c,01
SPIWrite 078d,2a
SPIWrite 078e,0c
SPIWrite 078f,d1
SPIWrite 0790,11
SPIWrite 0791,4b
SPIWrite 0792,42
SPIWrite 0793,10
SPIWrite 0794,9a
SPIWrite 0795,5c
SPIWrite 0796,92
SPIWrite 0797,1e
SPIWrite 0798,d7
SPIWrite 0799,b2
SPIWrite 079a,1f
SPIWrite 079b,b1
SPIWrite 079c,01
SPIWrite 079d,2f
SPIWrite 079e,04
SPIWrite 079f,d1
SPIWrite 07a0,05
SPIWrite 07a1,22
SPIWrite 07a2,00
SPIWrite 07a3,e0
SPIWrite 07a4,07
SPIWrite 07a5,22
SPIWrite 07a6,0d
SPIWrite 07a7,4b
SPIWrite 07a8,1a
SPIWrite 07a9,70
SPIWrite 07aa,d8
SPIWrite 07ab,f7
SPIWrite 07ac,bb
SPIWrite 07ad,fc
SPIWrite 07ae,80
SPIWrite 07af,bd
SPIWrite 07b0,63
SPIWrite 07b1,22
SPIWrite 07b2,01
SPIWrite 07b3,20
SPIWrite 07b4,bc
SPIWrite 07b5,77
SPIWrite 07b6,02
SPIWrite 07b7,00
SPIWrite 07b8,4c
SPIWrite 07b9,17
SPIWrite 07ba,03
SPIWrite 07bb,00
SPIWrite 07bc,60
SPIWrite 07bd,17
SPIWrite 07be,03
SPIWrite 07bf,00
SPIWrite 07c0,38
SPIWrite 07c1,17
SPIWrite 07c2,03
SPIWrite 07c3,00
SPIWrite 07c4,ac
SPIWrite 07c5,fe
SPIWrite 07c6,00
SPIWrite 07c7,20
SPIWrite 07c8,28
SPIWrite 07c9,fd
SPIWrite 07ca,00
SPIWrite 07cb,20
SPIWrite 07cc,4a
SPIWrite 07cd,0c
SPIWrite 07ce,01
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```
SPIWrite 07cf,20
SPIWrite 07d0,fb
SPIWrite 07d1,20
SPIWrite 07d2,01
SPIWrite 07d3,20
SPIWrite 07d4,17
SPIWrite 07d5,17
SPIWrite 07d6,03
SPIWrite 07d7,00
SPIWrite 07d8,a2
SPIWrite 07d9,01
SPIWrite 07da,01
SPIWrite 07db,20
SPIWrite 07dc,d4
SPIWrite 07dd,1e
SPIWrite 07de,01
SPIWrite 07df,20
SPIWrite 07e0,2d
SPIWrite 07e1,e9
SPIWrite 07e2,f0
SPIWrite 07e3,41
SPIWrite 07e4,04
SPIWrite 07e5,46
SPIWrite 07e6,4a
SPIWrite 07e7,48
SPIWrite 07e8,0d
SPIWrite 07e9,46
SPIWrite 07ea,a7
SPIWrite 07eb,00
SPIWrite 07ec,c1
SPIWrite 07ed,5d
SPIWrite 07ee,1e
SPIWrite 07ef,46
SPIWrite 07f0,8d
SPIWrite 07f1,42
SPIWrite 07f2,07
SPIWrite 07f3,44
SPIWrite 07f4,08
SPIWrite 07f5,d0
SPIWrite 07f6,b9
SPIWrite 07f7,78
SPIWrite 07f8,8d
SPIWrite 07f9,42
SPIWrite 07fa,18
SPIWrite 07fb,bf
SPIWrite 07fc,04
SPIWrite 07fd,27
SPIWrite 07fe,13
SPIWrite 07ff,d1
SPIWrite 0800,01
SPIWrite 0801,21
SPIWrite 0802,01
SPIWrite 0803,eb
SPIWrite 0804,44
SPIWrite 0805,01
SPIWrite 0806,00
SPIWrite 0807,e0
SPIWrite 0808,61
SPIWrite 0809,00
SPIWrite 080a,cf
SPIWrite 080b,b2
SPIWrite 080c,04
SPIWrite 080d,2f
SPIWrite 080e,0b
SPIWrite 080f,d0
SPIWrite 0810,40
SPIWrite 0811,49
SPIWrite 0812,00
SPIWrite 0813,eb
```

```
SPIWrite 0814,47
SPIWrite 0815,00
SPIWrite 0816,0a
SPIWrite 0817,5d
SPIWrite 0818,41
SPIWrite 0819,78
SPIWrite 081a,90
SPIWrite 081b,46
SPIWrite 081c,04
SPIWrite 081d,29
SPIWrite 081e,04
SPIWrite 081f,d0
SPIWrite 0018,00    //sys_calib_macro_memory=0x0;   Address(0x18[7:0])
SPIWrite 0018,20    //macro=0x1;    Address(0x18[7:5])
SPIRead 00f0

//Read  MACRO_READY=0x1;    Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,08    //MACRO_OPERAND_REG0=0x8000000;
Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00
SPIWrite 00a1,00
SPIWrite 00a0,00
SPIWrite 00a7,00    //MACRO_OPERAND_REG1=0x800;
Address(0xa4[7:0],0xa5[7:0],0xa6[7:0],0xa7[7:0],0xa8[7:0])
SPIWrite 00a6,00
SPIWrite 00a5,08
SPIWrite 00a4,00
SPIWrite 0193,78    //MACRO_OPCODE=0x78;    Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0

//Read  MACRO_DONE=0x1;     Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIRead 00f0

//Read  MACRO_ERROR=0x0;    Address(0xf0[7:3])

SPIRead 00f1

//Read  MACRO_ERROR_OPCODE=0x0;     Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0

//Read  MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0

//Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;     Address(0xf0[7:5])

SPIRead 00f0

//Read  MACRO_ERROR_IN_OPERAND=0x0;     Address(0xf0[7:6])

SPIRead 00f0

//Read  MACRO_ERROR_IN_EXECUTION=0x0;   Address(0xf0[7:7])

SPIRead 00f3
SPIRead 00f2

//Read  MACRO_ERROR_EXTENDED_CODE=0x0;  Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
```

```
4955
4956   SPIRead 00f7
4957   SPIRead 00f6
4958   SPIRead 00f5
4959   SPIRead 00f4
4960
4961   //Read  MACRO_ERROR_EXTENDED_CODE_2=0x0;
       Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
4962
4963   SPIWrite 0144,00    //all_addr_high=0x0;    Address(0x144[7:2])
4964   SPIWrite 0018,00    //macro=0x0;    Address(0x18[7:5])
4965   SPIWrite 0018,01    //sys_calib_macro_memory=0x1;   Address(0x18[7:0])
4966   SPIWrite 0020,20
4967   SPIWrite 0021,46
4968   SPIWrite 0022,de
4969   SPIWrite 0023,f7
4970   SPIWrite 0024,15
4971   SPIWrite 0025,fb
4972   SPIWrite 0026,00
4973   SPIWrite 0027,e0
4974   SPIWrite 0028,90
4975   SPIWrite 0029,46
4976   SPIWrite 002a,20
4977   SPIWrite 002b,46
4978   SPIWrite 002c,29
4979   SPIWrite 002d,46
4980   SPIWrite 002e,33
4981   SPIWrite 002f,46
4982   SPIWrite 0030,42
4983   SPIWrite 0031,46
4984   SPIWrite 0032,de
4985   SPIWrite 0033,f7
4986   SPIWrite 0034,0d
4987   SPIWrite 0035,fb
4988   SPIWrite 0036,04
4989   SPIWrite 0037,2f
4990   SPIWrite 0038,10
4991   SPIWrite 0039,d0
4992   SPIWrite 003a,38
4993   SPIWrite 003b,4b
4994   SPIWrite 003c,36
4995   SPIWrite 003d,49
4996   SPIWrite 003e,0c
4997   SPIWrite 003f,20
4998   SPIWrite 0040,14
4999   SPIWrite 0041,fb
5000   SPIWrite 0042,00
5001   SPIWrite 0043,f0
5002   SPIWrite 0044,00
5003   SPIWrite 0045,eb
5004   SPIWrite 0046,85
5005   SPIWrite 0047,02
5006   SPIWrite 0048,13
5007   SPIWrite 0049,f8
5008   SPIWrite 004a,17
5009   SPIWrite 004b,30
5010   SPIWrite 004c,8a
5011   SPIWrite 004d,58
5012   SPIWrite 004e,00
5013   SPIWrite 004f,eb
5014   SPIWrite 0050,83
5015   SPIWrite 0051,00
5016   SPIWrite 0052,92
5017   SPIWrite 0053,f8
5018   SPIWrite 0054,02
5019   SPIWrite 0055,26
5020   SPIWrite 0056,08
5021   SPIWrite 0057,58
5022   SPIWrite 0058,80
```

```
SPIWrite 0059,f8
SPIWrite 005a,02
SPIWrite 005b,26
SPIWrite 005c,bd
SPIWrite 005d,e8
SPIWrite 005e,f0
SPIWrite 005f,81
SPIWrite 0060,70
SPIWrite 0061,b5
SPIWrite 0062,05
SPIWrite 0063,46
SPIWrite 0064,0c
SPIWrite 0065,46
SPIWrite 0066,de
SPIWrite 0067,f7
SPIWrite 0068,a3
SPIWrite 0069,ff
SPIWrite 006a,2d
SPIWrite 006b,48
SPIWrite 006c,2a
SPIWrite 006d,4a
SPIWrite 006e,4f
SPIWrite 006f,f4
SPIWrite 0070,25
SPIWrite 0071,76
SPIWrite 0072,15
SPIWrite 0073,fb
SPIWrite 0074,06
SPIWrite 0075,f6
SPIWrite 0076,0c
SPIWrite 0077,21
SPIWrite 0078,dc
SPIWrite 0079,23
SPIWrite 007a,15
SPIWrite 007b,fb
SPIWrite 007c,01
SPIWrite 007d,f1
SPIWrite 007e,14
SPIWrite 007f,fb
SPIWrite 0080,03
SPIWrite 0081,63
SPIWrite 0082,01
SPIWrite 0083,eb
SPIWrite 0084,84
SPIWrite 0085,01
SPIWrite 0086,c0
SPIWrite 0087,18
SPIWrite 0088,54
SPIWrite 0089,58
SPIWrite 008a,90
SPIWrite 008b,f8
SPIWrite 008c,74
SPIWrite 008d,10
SPIWrite 008e,90
SPIWrite 008f,f8
SPIWrite 0090,42
SPIWrite 0091,20
SPIWrite 0092,d4
SPIWrite 0093,f8
SPIWrite 0094,3c
SPIWrite 0095,66
SPIWrite 0096,52
SPIWrite 0097,18
SPIWrite 0098,92
SPIWrite 0099,1e
SPIWrite 009a,06
SPIWrite 009b,21
SPIWrite 009c,d2
SPIWrite 009d,b2
```

```
  SPIWrite 009e,0d
  SPIWrite 009f,46
  SPIWrite 00a0,b2
  SPIWrite 00a1,fb
  SPIWrite 00a2,f1
  SPIWrite 00a3,f1
  SPIWrite 00a4,11
  SPIWrite 00a5,fb
  SPIWrite 00a6,05
  SPIWrite 00a7,f3
  SPIWrite 00a8,d2
  SPIWrite 00a9,1a
  SPIWrite 00aa,6f
  SPIWrite 00ab,f0
  SPIWrite 00ac,02
  SPIWrite 00ad,03
  SPIWrite 00ae,d2
  SPIWrite 00af,b2
  SPIWrite 00b0,9b
  SPIWrite 00b1,1a
  SPIWrite 00b2,63
  SPIWrite 00b3,f3
  SPIWrite 00b4,12
  SPIWrite 00b5,46
  SPIWrite 00b6,c4
  SPIWrite 00b7,f8
  SPIWrite 00b8,3c
  SPIWrite 00b9,66
  SPIWrite 00ba,90
  SPIWrite 00bb,f8
  SPIWrite 00bc,42
  SPIWrite 00bd,00
  SPIWrite 00be,d4
  SPIWrite 00bf,f8
  SPIWrite 00c0,3c
  SPIWrite 00c1,26
  SPIWrite 00c2,00
  SPIWrite 00c3,1d
  SPIWrite 00c4,90
  SPIWrite 00c5,fb
  SPIWrite 00c6,f5
  SPIWrite 00c7,f3
  SPIWrite 00c8,4f
  SPIWrite 00c9,f4
  SPIWrite 00ca,00
  SPIWrite 00cb,20
  SPIWrite 00cc,c9
  SPIWrite 00cd,1a
  SPIWrite 00ce,00
  SPIWrite 00cf,eb
  SPIWrite 00d0,c1
  SPIWrite 00d1,40
  SPIWrite 00d2,c0
  SPIWrite 00d3,0c
  SPIWrite 00d4,60
  SPIWrite 00d5,f3
  SPIWrite 00d6,d7
  SPIWrite 00d7,42
  SPIWrite 00d8,c4
  SPIWrite 00d9,f8
  SPIWrite 00da,3c
  SPIWrite 00db,26
  SPIWrite 00dc,70
  SPIWrite 00dd,bd
  SPIWrite 00de,38
  SPIWrite 00df,b5
  SPIWrite 00e0,0f
  SPIWrite 00e1,4a
  SPIWrite 00e2,10
```

```
SPIWrite 00e3,4c
SPIWrite 00e4,4f
SPIWrite 00e5,f4
SPIWrite 00e6,25
SPIWrite 00e7,75
SPIWrite 00e8,dc
SPIWrite 00e9,23
SPIWrite 00ea,10
SPIWrite 00eb,fb
SPIWrite 00ec,05
SPIWrite 00ed,f5
SPIWrite 00ee,b1
SPIWrite 00ef,32
SPIWrite 00f0,11
SPIWrite 00f1,fb
SPIWrite 00f2,03
SPIWrite 00f3,53
SPIWrite 00f4,d2
SPIWrite 00f5,5c
SPIWrite 00f6,94
SPIWrite 00f7,f9
SPIWrite 00f8,01
SPIWrite 00f9,50
SPIWrite 00fa,03
SPIWrite 00fb,2a
SPIWrite 00fc,03
SPIWrite 00fd,d0
SPIWrite 00fe,94
SPIWrite 00ff,f9
SPIWrite 0100,01
SPIWrite 0101,20
SPIWrite 0102,92
SPIWrite 0103,1f
SPIWrite 0104,62
SPIWrite 0105,70
SPIWrite 0106,df
SPIWrite 0107,f7
SPIWrite 0108,99
SPIWrite 0109,f9
SPIWrite 010a,65
SPIWrite 010b,70
SPIWrite 010c,38
SPIWrite 010d,bd
SPIWrite 010e,c0
SPIWrite 010f,46
SPIWrite 0110,fe
SPIWrite 0111,d5
SPIWrite 0112,00
SPIWrite 0113,20
SPIWrite 0114,b6
SPIWrite 0115,01
SPIWrite 0116,01
SPIWrite 0117,20
SPIWrite 0118,a8
SPIWrite 0119,75
SPIWrite 011a,02
SPIWrite 011b,00
SPIWrite 011c,06
SPIWrite 011d,d6
SPIWrite 011e,00
SPIWrite 011f,20
SPIWrite 0120,e0
SPIWrite 0121,ab
SPIWrite 0122,00
SPIWrite 0123,20
SPIWrite 0124,36
SPIWrite 0125,d6
SPIWrite 0126,00
SPIWrite 0127,20
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SPIWrite 0128,43
SPIWrite 0129,48
SPIWrite 012a,10
SPIWrite 012b,b5
SPIWrite 012c,00
SPIWrite 012d,78
SPIWrite 012e,0c
SPIWrite 012f,46
SPIWrite 0130,ff
SPIWrite 0131,f7
SPIWrite 0132,a7
SPIWrite 0133,f9
SPIWrite 0134,00
SPIWrite 0135,20
SPIWrite 0136,20
SPIWrite 0137,70
SPIWrite 0138,10
SPIWrite 0139,bd
SPIWrite 013a,3f
SPIWrite 013b,48
SPIWrite 013c,2d
SPIWrite 013d,e9
SPIWrite 013e,f0
SPIWrite 013f,41
SPIWrite 0140,05
SPIWrite 0141,78
SPIWrite 0142,3f
SPIWrite 0143,4f
SPIWrite 0144,3d
SPIWrite 0145,48
SPIWrite 0146,00
SPIWrite 0147,22
SPIWrite 0148,0c
SPIWrite 0149,46
SPIWrite 014a,2e
SPIWrite 014b,01
SPIWrite 014c,c7
SPIWrite 014d,eb
SPIWrite 014e,82
SPIWrite 014f,01
SPIWrite 0150,0b
SPIWrite 0151,68
SPIWrite 0152,02
SPIWrite 0153,f0
SPIWrite 0154,01
SPIWrite 0155,0c
SPIWrite 0156,42
SPIWrite 0157,f3
SPIWrite 0158,5d
SPIWrite 0159,01
SPIWrite 015a,52
SPIWrite 015b,1c
SPIWrite 015c,89
SPIWrite 015d,00
SPIWrite 015e,04
SPIWrite 015f,2a
SPIWrite 0160,01
SPIWrite 0161,eb
SPIWrite 0162,cc
SPIWrite 0163,01
SPIWrite 0164,31
SPIWrite 0165,44
SPIWrite 0166,01
SPIWrite 0167,44
SPIWrite 0168,cb
SPIWrite 0169,67
SPIWrite 016a,ef
SPIWrite 016b,db
SPIWrite 016c,df
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SPIWrite 016d,f8
SPIWrite 016e,d8
SPIWrite 016f,80
SPIWrite 0170,34
SPIWrite 0171,4f
SPIWrite 0172,90
SPIWrite 0173,f8
SPIWrite 0174,c2
SPIWrite 0175,20
SPIWrite 0176,d8
SPIWrite 0177,f8
SPIWrite 0178,50
SPIWrite 0179,37
SPIWrite 017a,39
SPIWrite 017b,46
SPIWrite 017c,98
SPIWrite 017d,47
SPIWrite 017e,33
SPIWrite 017f,4e
SPIWrite 0180,d8
SPIWrite 0181,f8
SPIWrite 0182,68
SPIWrite 0183,39
SPIWrite 0184,28
SPIWrite 0185,46
SPIWrite 0186,39
SPIWrite 0187,46
SPIWrite 0188,32
SPIWrite 0189,46
SPIWrite 018a,98
SPIWrite 018b,47
SPIWrite 018c,a8
SPIWrite 018d,19
SPIWrite 018e,00
SPIWrite 018f,f5
SPIWrite 0190,33
SPIWrite 0191,70
SPIWrite 0192,07
SPIWrite 0193,78
SPIWrite 0194,00
SPIWrite 0195,2f
SPIWrite 0196,31
SPIWrite 0197,d1
SPIWrite 0198,d8
SPIWrite 0199,f8
SPIWrite 019a,60
SPIWrite 019b,29
SPIWrite 019c,28
SPIWrite 019d,46
SPIWrite 019e,21
SPIWrite 019f,46
SPIWrite 01a0,90
SPIWrite 01a1,47
SPIWrite 01a2,20
SPIWrite 01a3,78
SPIWrite 01a4,00
SPIWrite 01a5,28
SPIWrite 01a6,3b
SPIWrite 01a7,d1
SPIWrite 01a8,d8
SPIWrite 01a9,f8
SPIWrite 01aa,70
SPIWrite 01ab,29
SPIWrite 01ac,28
SPIWrite 01ad,46
SPIWrite 01ae,21
SPIWrite 01af,46
SPIWrite 01b0,90
SPIWrite 01b1,47
```

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5368   SPIWrite 01b2,20
5369   SPIWrite 01b3,78
5370   SPIWrite 01b4,a0
5371   SPIWrite 01b5,bb
5372   SPIWrite 01b6,d8
5373   SPIWrite 01b7,f8
5374   SPIWrite 01b8,38
5375   SPIWrite 01b9,26
5376   SPIWrite 01ba,28
5377   SPIWrite 01bb,46
5378   SPIWrite 01bc,21
5379   SPIWrite 01bd,46
5380   SPIWrite 01be,90
5381   SPIWrite 01bf,47
5382   SPIWrite 01c0,20
5383   SPIWrite 01c1,78
5384   SPIWrite 01c2,68
5385   SPIWrite 01c3,bb
5386   SPIWrite 01c4,d8
5387   SPIWrite 01c5,f8
5388   SPIWrite 01c6,3c
5389   SPIWrite 01c7,26
5390   SPIWrite 01c8,28
5391   SPIWrite 01c9,46
5392   SPIWrite 01ca,21
5393   SPIWrite 01cb,46
5394   SPIWrite 01cc,90
5395   SPIWrite 01cd,47
5396   SPIWrite 01ce,20
5397   SPIWrite 01cf,78
5398   SPIWrite 01d0,30
5399   SPIWrite 01d1,bb
5400   SPIWrite 01d2,d8
5401   SPIWrite 01d3,f8
5402   SPIWrite 01d4,50
5403   SPIWrite 01d5,16
5404   SPIWrite 01d6,28
5405   SPIWrite 01d7,46
5406   SPIWrite 01d8,88
5407   SPIWrite 01d9,47
5408   SPIWrite 01da,d8
5409   SPIWrite 01db,f8
5410   SPIWrite 01dc,54
5411   SPIWrite 01dd,16
5412   SPIWrite 01de,28
5413   SPIWrite 01df,46
5414   SPIWrite 01e0,88
5415   SPIWrite 01e1,47
5416   SPIWrite 01e2,d8
5417   SPIWrite 01e3,f8
5418   SPIWrite 01e4,58
5419   SPIWrite 01e5,16
5420   SPIWrite 01e6,28
5421   SPIWrite 01e7,46
5422   SPIWrite 01e8,88
5423   SPIWrite 01e9,47
5424   SPIWrite 01ea,01
5425   SPIWrite 01eb,20
5426   SPIWrite 01ec,00
5427   SPIWrite 01ed,21
5428   SPIWrite 01ee,a8
5429   SPIWrite 01ef,40
5430   SPIWrite 01f0,0a
5431   SPIWrite 01f1,46
5432   SPIWrite 01f2,c0
5433   SPIWrite 01f3,b2
5434   SPIWrite 01f4,ff
5435   SPIWrite 01f5,f7
5436   SPIWrite 01f6,4a
```

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5437   SPIWrite 01f7,fb
5438   SPIWrite 01f8,bd
5439   SPIWrite 01f9,e8
5440   SPIWrite 01fa,f0
5441   SPIWrite 01fb,81
5442   SPIWrite 01fc,62
5443   SPIWrite 01fd,88
5444   SPIWrite 01fe,08
5445   SPIWrite 01ff,23
5446   SPIWrite 0200,01
5447   SPIWrite 0201,21
5448   SPIWrite 0202,66
5449   SPIWrite 0203,68
5450   SPIWrite 0204,23
5451   SPIWrite 0205,70
5452   SPIWrite 0206,42
5453   SPIWrite 0207,f4
5454   SPIWrite 0208,80
5455   SPIWrite 0209,42
5456   SPIWrite 020a,01
5457   SPIWrite 020b,fa
5458   SPIWrite 020c,05
5459   SPIWrite 020d,f3
5460   SPIWrite 020e,62
5461   SPIWrite 020f,80
5462   SPIWrite 0210,33
5463   SPIWrite 0211,43
5464   SPIWrite 0212,63
5465   SPIWrite 0213,60
5466   SPIWrite 0214,00
5467   SPIWrite 0215,78
5468   SPIWrite 0216,62
5469   SPIWrite 0217,68
5470   SPIWrite 0218,00
5471   SPIWrite 0219,1d
5472   SPIWrite 021a,81
5473   SPIWrite 021b,40
5474   SPIWrite 021c,11
5475   SPIWrite 021d,43
5476   SPIWrite 021e,61
5477   SPIWrite 021f,60
5478   SPIWrite 0220,bd
5479   SPIWrite 0221,e8
5480   SPIWrite 0222,f0
5481   SPIWrite 0223,81
5482   SPIWrite 0224,04
5483   SPIWrite 0225,48
5484   SPIWrite 0226,00
5485   SPIWrite 0227,78
5486   SPIWrite 0228,02
5487   SPIWrite 0229,28
5488   SPIWrite 022a,a4
5489   SPIWrite 022b,bf
5490   SPIWrite 022c,04
5491   SPIWrite 022d,20
5492   SPIWrite 022e,08
5493   SPIWrite 022f,70
5494   SPIWrite 0230,01
5495   SPIWrite 0231,da
5496   SPIWrite 0232,ff
5497   SPIWrite 0233,f7
5498   SPIWrite 0234,48
5499   SPIWrite 0235,be
5500   SPIWrite 0236,70
5501   SPIWrite 0237,47
5502   SPIWrite 0238,b4
5503   SPIWrite 0239,03
5504   SPIWrite 023a,00
5505   SPIWrite 023b,a2
```

```
SPIWrite 023c,b4
SPIWrite 023d,01
SPIWrite 023e,01
SPIWrite 023f,20
SPIWrite 0240,4b
SPIWrite 0241,fc
SPIWrite 0242,ff
SPIWrite 0243,5d
SPIWrite 0244,18
SPIWrite 0245,ff
SPIWrite 0246,00
SPIWrite 0247,20
SPIWrite 0248,90
SPIWrite 0249,d6
SPIWrite 024a,00
SPIWrite 024b,20
SPIWrite 024c,d4
SPIWrite 024d,fb
SPIWrite 024e,00
SPIWrite 024f,20
SPIWrite 0250,0a
SPIWrite 0251,46
SPIWrite 0252,2d
SPIWrite 0253,e9
SPIWrite 0254,f8
SPIWrite 0255,4f
SPIWrite 0256,01
SPIWrite 0257,46
SPIWrite 0258,4f
SPIWrite 0259,f0
SPIWrite 025a,aa
SPIWrite 025b,0a
SPIWrite 025c,00
SPIWrite 025d,20
SPIWrite 025e,a1
SPIWrite 025f,f1
SPIWrite 0260,aa
SPIWrite 0261,08
SPIWrite 0262,d3
SPIWrite 0263,46
SPIWrite 0264,04
SPIWrite 0265,46
SPIWrite 0266,00
SPIWrite 0267,92
SPIWrite 0268,08
SPIWrite 0269,f1
SPIWrite 026a,aa
SPIWrite 026b,08
SPIWrite 026c,98
SPIWrite 026d,f8
SPIWrite 026e,a6
SPIWrite 026f,20
SPIWrite 0270,04
SPIWrite 0271,2a
SPIWrite 0272,56
SPIWrite 0273,da
SPIWrite 0274,98
SPIWrite 0275,f8
SPIWrite 0276,04
SPIWrite 0277,70
SPIWrite 0278,00
SPIWrite 0279,2f
SPIWrite 027a,52
SPIWrite 027b,d0
SPIWrite 027c,7f
SPIWrite 027d,1e
SPIWrite 027e,7a
SPIWrite 027f,1c
SPIWrite 0280,5f
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5575   SPIWrite 0281,fa
5576   SPIWrite 0282,87
5577   SPIWrite 0283,f9
5578   SPIWrite 0284,d2
5579   SPIWrite 0285,b2
5580   SPIWrite 0286,06
5581   SPIWrite 0287,2a
5582   SPIWrite 0288,48
5583   SPIWrite 0289,da
5584   SPIWrite 028a,5b
5585   SPIWrite 028b,46
5586   SPIWrite 028c,03
5587   SPIWrite 028d,fb
5588   SPIWrite 028e,04
5589   SPIWrite 028f,13
5590   SPIWrite 0290,1d
5591   SPIWrite 0291,7c
5592   SPIWrite 0292,00
5593   SPIWrite 0293,23
5594   SPIWrite 0294,37
5595   SPIWrite 0295,e0
5596   SPIWrite 0296,c5
5597   SPIWrite 0297,18
5598   SPIWrite 0298,4d
5599   SPIWrite 0299,19
5600   SPIWrite 029a,ed
5601   SPIWrite 029b,7d
5602   SPIWrite 029c,09
5603   SPIWrite 029d,26
5604   SPIWrite 029e,19
5605   SPIWrite 029f,fb
5606   SPIWrite 02a0,06
5607   SPIWrite 02a1,f6
5608   SPIWrite 02a2,77
5609   SPIWrite 02a3,19
5610   SPIWrite 02a4,c7
5611   SPIWrite 02a5,19
5612   SPIWrite 02a6,cf
5613   SPIWrite 02a7,19
5614   SPIWrite 02a8,97
5615   SPIWrite 02a9,f9
5616   SPIWrite 02aa,22
5617   SPIWrite 02ab,e0
5618   SPIWrite 02ac,02
5619   SPIWrite 02ad,eb
5620   SPIWrite 02ae,c2
5621   SPIWrite 02af,0c
5622   SPIWrite 02b0,ae
5623   SPIWrite 02b1,19
5624   SPIWrite 02b2,86
5625   SPIWrite 02b3,19
5626   SPIWrite 02b4,47
5627   SPIWrite 02b5,19
5628   SPIWrite 02b6,8e
5629   SPIWrite 02b7,19
5630   SPIWrite 02b8,67
5631   SPIWrite 02b9,44
5632   SPIWrite 02ba,cf
5633   SPIWrite 02bb,19
5634   SPIWrite 02bc,87
5635   SPIWrite 02bd,f8
5636   SPIWrite 02be,22
5637   SPIWrite 02bf,e0
5638   SPIWrite 02c0,96
5639   SPIWrite 02c1,f9
5640   SPIWrite 02c2,58
5641   SPIWrite 02c3,70
5642   SPIWrite 02c4,46
5643   SPIWrite 02c5,19
```

```
5644   SPIWrite 02c6,0b
5645   SPIWrite 02c7,fb
5646   SPIWrite 02c8,04
5647   SPIWrite 02c9,f0
5648   SPIWrite 02ca,0c
5649   SPIWrite 02cb,eb
5650   SPIWrite 02cc,06
5651   SPIWrite 02cd,05
5652   SPIWrite 02ce,4e
5653   SPIWrite 02cf,19
5654   SPIWrite 02d0,0d
5655   SPIWrite 02d1,18
5656   SPIWrite 02d2,86
5657   SPIWrite 02d3,f8
5658   SPIWrite 02d4,58
5659   SPIWrite 02d5,70
5660   SPIWrite 02d6,ad
5661   SPIWrite 02d7,7d
5662   SPIWrite 02d8,5b
5663   SPIWrite 02d9,1c
5664   SPIWrite 02da,db
5665   SPIWrite 02db,b2
5666   SPIWrite 02dc,19
5667   SPIWrite 02dd,e0
5668   SPIWrite 02de,03
5669   SPIWrite 02df,25
5670   SPIWrite 02e0,19
5671   SPIWrite 02e1,fb
5672   SPIWrite 02e2,05
5673   SPIWrite 02e3,35
5674   SPIWrite 02e4,45
5675   SPIWrite 02e5,19
5676   SPIWrite 02e6,4d
5677   SPIWrite 02e7,19
5678   SPIWrite 02e8,95
5679   SPIWrite 02e9,f8
5680   SPIWrite 02ea,8e
5681   SPIWrite 02eb,70
5682   SPIWrite 02ec,02
5683   SPIWrite 02ed,eb
5684   SPIWrite 02ee,42
5685   SPIWrite 02ef,06
5686   SPIWrite 02f0,9d
5687   SPIWrite 02f1,19
5688   SPIWrite 02f2,45
5689   SPIWrite 02f3,19
5690   SPIWrite 02f4,0a
5691   SPIWrite 02f5,fb
5692   SPIWrite 02f6,04
5693   SPIWrite 02f7,f0
5694   SPIWrite 02f8,4e
5695   SPIWrite 02f9,19
5696   SPIWrite 02fa,0d
5697   SPIWrite 02fb,18
5698   SPIWrite 02fc,86
5699   SPIWrite 02fd,f8
5700   SPIWrite 02fe,8e
5701   SPIWrite 02ff,70
5702   SPIWrite 0300,2d
5703   SPIWrite 0301,7c
5704   SPIWrite 0302,5b
5705   SPIWrite 0303,1c
5706   SPIWrite 0304,db
5707   SPIWrite 0305,b2
5708   SPIWrite 0306,9d
5709   SPIWrite 0307,42
5710   SPIWrite 0308,e9
5711   SPIWrite 0309,dc
5712   SPIWrite 030a,0a
```

```
  SPIWrite 030b,fb
  SPIWrite 030c,04
  SPIWrite 030d,13
  SPIWrite 030e,9d
  SPIWrite 030f,7d
  SPIWrite 0310,00
  SPIWrite 0311,23
  SPIWrite 0312,9d
  SPIWrite 0313,42
  SPIWrite 0314,bf
  SPIWrite 0315,dc
  SPIWrite 0316,52
  SPIWrite 0317,1c
  SPIWrite 0318,06
  SPIWrite 0319,2a
  SPIWrite 031a,b6
  SPIWrite 031b,db
  SPIWrite 031c,06
  SPIWrite 031d,22
  SPIWrite 031e,88
  SPIWrite 031f,f8
  SPIWrite 0320,04
  SPIWrite 0321,20
  SPIWrite 0322,64
  SPIWrite 0323,1c
  SPIWrite 0324,aa
  SPIWrite 0325,30
  SPIWrite 0326,06
  SPIWrite 0327,2c
  SPIWrite 0328,9e
  SPIWrite 0329,db
  SPIWrite 032a,00
  SPIWrite 032b,9a
  SPIWrite 032c,08
  SPIWrite 032d,46
  SPIWrite 032e,11
  SPIWrite 032f,46
  SPIWrite 0330,e4
  SPIWrite 0331,f7
  SPIWrite 0332,48
  SPIWrite 0333,fa
  SPIWrite 0334,bd
  SPIWrite 0335,e8
  SPIWrite 0336,f8
  SPIWrite 0337,8f
  SPIWrite 0338,10
  SPIWrite 0339,b5
  SPIWrite 033a,30
  SPIWrite 033b,4a
  SPIWrite 033c,2e
  SPIWrite 033d,4c
  SPIWrite 033e,13
  SPIWrite 033f,78
  SPIWrite 0340,54
  SPIWrite 0341,f8
  SPIWrite 0342,20
  SPIWrite 0343,40
  SPIWrite 0344,84
  SPIWrite 0345,f8
  SPIWrite 0346,58
  SPIWrite 0347,3e
  SPIWrite 0348,06
  SPIWrite 0349,20
  SPIWrite 034a,c0
  SPIWrite 034b,f2
  SPIWrite 034c,00
  SPIWrite 034d,00
  SPIWrite 034e,03
  SPIWrite 034f,46
```

```
SPIWrite 0350,5b
SPIWrite 0351,1e
SPIWrite 0352,fd
SPIWrite 0353,d1
SPIWrite 0354,53
SPIWrite 0355,78
SPIWrite 0356,04
SPIWrite 0357,eb
SPIWrite 0358,83
SPIWrite 0359,03
SPIWrite 035a,c3
SPIWrite 035b,f8
SPIWrite 035c,c0
SPIWrite 035d,13
SPIWrite 035e,40
SPIWrite 035f,1e
SPIWrite 0360,fd
SPIWrite 0361,d1
SPIWrite 0362,50
SPIWrite 0363,78
SPIWrite 0364,84
SPIWrite 0365,f8
SPIWrite 0366,58
SPIWrite 0367,0e
SPIWrite 0368,10
SPIWrite 0369,bd
SPIWrite 036a,f8
SPIWrite 036b,b5
SPIWrite 036c,dd
SPIWrite 036d,f8
SPIWrite 036e,18
SPIWrite 036f,c0
SPIWrite 0370,07
SPIWrite 0371,46
SPIWrite 0372,14
SPIWrite 0373,46
SPIWrite 0374,1d
SPIWrite 0375,46
SPIWrite 0376,0e
SPIWrite 0377,46
SPIWrite 0378,cd
SPIWrite 0379,f8
SPIWrite 037a,00
SPIWrite 037b,c0
SPIWrite 037c,eb
SPIWrite 037d,f7
SPIWrite 037e,28
SPIWrite 037f,f8
SPIWrite 0380,55
SPIWrite 0381,ea
SPIWrite 0382,04
SPIWrite 0383,00
SPIWrite 0384,37
SPIWrite 0385,d1
SPIWrite 0386,1e
SPIWrite 0387,4b
SPIWrite 0388,1e
SPIWrite 0389,4a
SPIWrite 038a,03
SPIWrite 038b,eb
SPIWrite 038c,67
SPIWrite 038d,01
SPIWrite 038e,73
SPIWrite 038f,31
SPIWrite 0390,08
SPIWrite 0391,78
SPIWrite 0392,b3
SPIWrite 0393,f8
SPIWrite 0394,9e
```

```
  SPIWrite 0395,41
  SPIWrite 0396,12
  SPIWrite 0397,5c
  SPIWrite 0398,38
  SPIWrite 0399,46
  SPIWrite 039a,54
  SPIWrite 039b,43
  SPIWrite 039c,47
  SPIWrite 039d,b1
  SPIWrite 039e,01
  SPIWrite 039f,2f
  SPIWrite 03a0,08
  SPIWrite 03a1,bf
  SPIWrite 03a2,00
  SPIWrite 03a3,25
  SPIWrite 03a4,05
  SPIWrite 03a5,d0
  SPIWrite 03a6,02
  SPIWrite 03a7,2f
  SPIWrite 03a8,0c
  SPIWrite 03a9,bf
  SPIWrite 03aa,03
  SPIWrite 03ab,25
  SPIWrite 03ac,02
  SPIWrite 03ad,25
  SPIWrite 03ae,00
  SPIWrite 03af,e0
  SPIWrite 03b0,01
  SPIWrite 03b1,25
  SPIWrite 03b2,15
  SPIWrite 03b3,4a
  SPIWrite 03b4,d2
  SPIWrite 03b5,5d
  SPIWrite 03b6,01
  SPIWrite 03b7,2a
  SPIWrite 03b8,02
  SPIWrite 03b9,d0
  SPIWrite 03ba,91
  SPIWrite 03bb,f8
  SPIWrite 03bc,7e
  SPIWrite 03bd,30
  SPIWrite 03be,23
  SPIWrite 03bf,b1
  SPIWrite 03c0,79
  SPIWrite 03c1,08
  SPIWrite 03c2,02
  SPIWrite 03c3,d3
  SPIWrite 03c4,28
  SPIWrite 03c5,46
  SPIWrite 03c6,41
  SPIWrite 03c7,1c
  SPIWrite 03c8,cd
  SPIWrite 03c9,b2
  SPIWrite 03ca,d6
  SPIWrite 03cb,f8
  SPIWrite 03cc,01
  SPIWrite 03cd,10
  SPIWrite 03ce,27
  SPIWrite 03cf,09
  SPIWrite 03d0,0a
  SPIWrite 03d1,01
  SPIWrite 03d2,b2
  SPIWrite 03d3,fb
  SPIWrite 03d4,f4
  SPIWrite 03d5,f2
  SPIWrite 03d6,07
  SPIWrite 03d7,fb
  SPIWrite 03d8,12
  SPIWrite 03d9,11
```

```
  SPIWrite 03da,ff
  SPIWrite 03db,f7
  SPIWrite 03dc,ad
  SPIWrite 03dd,ff
  SPIWrite 03de,30
  SPIWrite 03df,78
  SPIWrite 03e0,48
  SPIWrite 03e1,b1
  SPIWrite 03e2,d6
  SPIWrite 03e3,f8
  SPIWrite 03e4,06
  SPIWrite 03e5,00
  SPIWrite 03e6,01
  SPIWrite 03e7,01
  SPIWrite 03e8,b1
  SPIWrite 03e9,fb
  SPIWrite 03ea,f4
  SPIWrite 03eb,f1
  SPIWrite 03ec,07
  SPIWrite 03ed,fb
  SPIWrite 03ee,11
  SPIWrite 03ef,01
  SPIWrite 03f0,28
  SPIWrite 03f1,46
  SPIWrite 03f2,ff
  SPIWrite 03f3,f7
  SPIWrite 03f4,a1
  SPIWrite 03f5,ff
  SPIWrite 03f6,f8
  SPIWrite 03f7,bd
  SPIWrite 03f8,bc
  SPIWrite 03f9,77
  SPIWrite 03fa,02
  SPIWrite 03fb,00
  SPIWrite 03fc,96
  SPIWrite 03fd,19
  SPIWrite 03fe,01
  SPIWrite 03ff,20
  SPIWrite 0400,b4
  SPIWrite 0401,01
  SPIWrite 0402,01
  SPIWrite 0403,20
  SPIWrite 0404,3b
  SPIWrite 0405,78
  SPIWrite 0406,02
  SPIWrite 0407,00
  SPIWrite 0408,98
  SPIWrite 0409,fe
  SPIWrite 040a,00
  SPIWrite 040b,20
  SPIWrite 040c,1d
  SPIWrite 040d,48
  SPIWrite 040e,b0
  SPIWrite 040f,b5
  SPIWrite 0410,00
  SPIWrite 0411,78
  SPIWrite 0412,48
  SPIWrite 0413,bb
  SPIWrite 0414,1c
  SPIWrite 0415,48
  SPIWrite 0416,00
  SPIWrite 0417,78
  SPIWrite 0418,30
  SPIWrite 0419,bb
  SPIWrite 041a,1d
  SPIWrite 041b,48
  SPIWrite 041c,1b
  SPIWrite 041d,4a
  SPIWrite 041e,02
```

```
SPIWrite 041f,21
SPIWrite 0420,0c
SPIWrite 0421,38
SPIWrite 0422,50
SPIWrite 0423,f8
SPIWrite 0424,0c
SPIWrite 0425,3f
SPIWrite 0426,93
SPIWrite 0427,f8
SPIWrite 0428,40
SPIWrite 0429,47
SPIWrite 042a,93
SPIWrite 042b,f8
SPIWrite 042c,41
SPIWrite 042d,77
SPIWrite 042e,0f
SPIWrite 042f,b9
SPIWrite 0430,83
SPIWrite 0431,f8
SPIWrite 0432,70
SPIWrite 0433,47
SPIWrite 0434,52
SPIWrite 0435,f8
SPIWrite 0436,08
SPIWrite 0437,4b
SPIWrite 0438,94
SPIWrite 0439,f8
SPIWrite 043a,80
SPIWrite 043b,5b
SPIWrite 043c,d4
SPIWrite 043d,f8
SPIWrite 043e,80
SPIWrite 043f,3b
SPIWrite 0440,49
SPIWrite 0441,1e
SPIWrite 0442,65
SPIWrite 0443,f3
SPIWrite 0444,4d
SPIWrite 0445,33
SPIWrite 0446,c4
SPIWrite 0447,f8
SPIWrite 0448,80
SPIWrite 0449,3b
SPIWrite 044a,ea
SPIWrite 044b,d1
SPIWrite 044c,11
SPIWrite 044d,4c
SPIWrite 044e,04
SPIWrite 044f,20
SPIWrite 0450,54
SPIWrite 0451,f8
SPIWrite 0452,04
SPIWrite 0453,3b
SPIWrite 0454,93
SPIWrite 0455,f8
SPIWrite 0456,71
SPIWrite 0457,27
SPIWrite 0458,93
SPIWrite 0459,f8
SPIWrite 045a,72
SPIWrite 045b,17
SPIWrite 045c,40
SPIWrite 045d,1e
SPIWrite 045e,01
SPIWrite 045f,ea
SPIWrite 0460,02
SPIWrite 0461,01
SPIWrite 0462,83
SPIWrite 0463,f8
```

```
  SPIWrite 0464,70
  SPIWrite 0465,17
  SPIWrite 0466,f3
  SPIWrite 0467,d1
  SPIWrite 0468,b0
  SPIWrite 0469,bd
  SPIWrite 046a,08
  SPIWrite 046b,b5
  SPIWrite 046c,d9
  SPIWrite 046d,f7
  SPIWrite 046e,f0
  SPIWrite 046f,fb
  SPIWrite 0470,ff
  SPIWrite 0471,f7
  SPIWrite 0472,cc
  SPIWrite 0473,ff
  SPIWrite 0474,08
  SPIWrite 0475,bd
  SPIWrite 0476,08
  SPIWrite 0477,b5
  SPIWrite 0478,d9
  SPIWrite 0479,f7
  SPIWrite 047a,9e
  SPIWrite 047b,fc
  SPIWrite 047c,ff
  SPIWrite 047d,f7
  SPIWrite 047e,c6
  SPIWrite 047f,ff
  SPIWrite 0480,08
  SPIWrite 0481,bd
  SPIWrite 0482,c0
  SPIWrite 0483,46
  SPIWrite 0484,c2
  SPIWrite 0485,19
  SPIWrite 0486,01
  SPIWrite 0487,20
  SPIWrite 0488,2b
  SPIWrite 0489,22
  SPIWrite 048a,01
  SPIWrite 048b,20
  SPIWrite 048c,bc
  SPIWrite 048d,77
  SPIWrite 048e,02
  SPIWrite 048f,00
  SPIWrite 0490,a8
  SPIWrite 0491,75
  SPIWrite 0492,02
  SPIWrite 0493,00
  SPIWrite 0494,9c
  SPIWrite 0495,77
  SPIWrite 0496,02
  SPIWrite 0497,00
  SPIWrite 0498,14
  SPIWrite 0499,49
  SPIWrite 049a,13
  SPIWrite 049b,48
  SPIWrite 049c,09
  SPIWrite 049d,68
  SPIWrite 049e,00
  SPIWrite 049f,88
  SPIWrite 04a0,00
  SPIWrite 04a1,22
  SPIWrite 04a2,48
  SPIWrite 04a3,43
  SPIWrite 04a4,c0
  SPIWrite 04a5,f3
  SPIWrite 04a6,40
  SPIWrite 04a7,11
  SPIWrite 04a8,01
```

```
  SPIWrite 04a9,eb
  SPIWrite 04aa,90
  SPIWrite 04ab,10
  SPIWrite 04ac,06
  SPIWrite 04ad,e0
  SPIWrite 04ae,13
  SPIWrite 04af,21
  SPIWrite 04b0,c0
  SPIWrite 04b1,f2
  SPIWrite 04b2,00
  SPIWrite 04b3,01
  SPIWrite 04b4,49
  SPIWrite 04b5,1e
  SPIWrite 04b6,fd
  SPIWrite 04b7,d1
  SPIWrite 04b8,00
  SPIWrite 04b9,bf
  SPIWrite 04ba,52
  SPIWrite 04bb,1c
  SPIWrite 04bc,90
  SPIWrite 04bd,42
  SPIWrite 04be,f6
  SPIWrite 04bf,d8
  SPIWrite 04c0,70
  SPIWrite 04c1,47
  SPIWrite 04c2,f8
  SPIWrite 04c3,b5
  SPIWrite 04c4,0a
  SPIWrite 04c5,4d
  SPIWrite 04c6,00
  SPIWrite 04c7,24
  SPIWrite 04c8,0e
  SPIWrite 04c9,46
  SPIWrite 04ca,07
  SPIWrite 04cb,46
  SPIWrite 04cc,07
  SPIWrite 04cd,e0
  SPIWrite 04ce,38
  SPIWrite 04cf,46
  SPIWrite 04d0,31
  SPIWrite 04d1,46
  SPIWrite 04d2,e6
  SPIWrite 04d3,f7
  SPIWrite 04d4,ad
  SPIWrite 04d5,fd
  SPIWrite 04d6,ff
  SPIWrite 04d7,f7
  SPIWrite 04d8,df
  SPIWrite 04d9,ff
  SPIWrite 04da,64
  SPIWrite 04db,1c
  SPIWrite 04dc,e4
  SPIWrite 04dd,b2
  SPIWrite 04de,28
  SPIWrite 04df,78
  SPIWrite 04e0,a0
  SPIWrite 04e1,42
  SPIWrite 04e2,f4
  SPIWrite 04e3,dc
  SPIWrite 04e4,f8
  SPIWrite 04e5,bd
  SPIWrite 04e6,c0
  SPIWrite 04e7,46
  SPIWrite 04e8,60
  SPIWrite 04e9,22
  SPIWrite 04ea,01
  SPIWrite 04eb,20
  SPIWrite 04ec,68
  SPIWrite 04ed,03
```

```
SPIWrite 04ee,01
SPIWrite 04ef,20
SPIWrite 04f0,64
SPIWrite 04f1,22
SPIWrite 04f2,01
SPIWrite 04f3,20
SPIWrite 04f4,2d
SPIWrite 04f5,e9
SPIWrite 04f6,fe
SPIWrite 04f7,4f
SPIWrite 04f8,00
SPIWrite 04f9,25
SPIWrite 04fa,9b
SPIWrite 04fb,46
SPIWrite 04fc,91
SPIWrite 04fd,46
SPIWrite 04fe,80
SPIWrite 04ff,46
SPIWrite 0500,0c
SPIWrite 0501,af
SPIWrite 0502,01
SPIWrite 0503,91
SPIWrite 0504,97
SPIWrite 0505,f8
SPIWrite 0506,00
SPIWrite 0507,a0
SPIWrite 0508,01
SPIWrite 0509,98
SPIWrite 050a,08
SPIWrite 050b,b9
SPIWrite 050c,5d
SPIWrite 050d,45
SPIWrite 050e,19
SPIWrite 050f,d1
SPIWrite 0510,05
SPIWrite 0511,eb
SPIWrite 0512,49
SPIWrite 0513,01
SPIWrite 0514,08
SPIWrite 0515,eb
SPIWrite 0516,c5
SPIWrite 0517,00
SPIWrite 0518,08
SPIWrite 0519,eb
SPIWrite 051a,c1
SPIWrite 051b,06
SPIWrite 051c,b0
SPIWrite 051d,f9
SPIWrite 051e,a4
SPIWrite 051f,7c
SPIWrite 0520,b6
SPIWrite 0521,f9
SPIWrite 0522,24
SPIWrite 0523,40
SPIWrite 0524,4a
SPIWrite 0525,46
SPIWrite 0526,2b
SPIWrite 0527,46
SPIWrite 0528,40
SPIWrite 0529,46
SPIWrite 052a,00
SPIWrite 052b,21
SPIWrite 052c,cd
SPIWrite 052d,f8
SPIWrite 052e,00
SPIWrite 052f,a0
SPIWrite 0530,d4
SPIWrite 0531,f7
SPIWrite 0532,ff
```

```
  SPIWrite 0533,fe
  SPIWrite 0534,e4
  SPIWrite 0535,1b
  SPIWrite 0536,6f
  SPIWrite 0537,f3
  SPIWrite 0538,df
  SPIWrite 0539,34
  SPIWrite 053a,84
  SPIWrite 053b,f4
  SPIWrite 053c,80
  SPIWrite 053d,44
  SPIWrite 053e,a4
  SPIWrite 053f,f5
  SPIWrite 0540,80
  SPIWrite 0541,44
  SPIWrite 0542,b4
  SPIWrite 0543,84
  SPIWrite 0544,6d
  SPIWrite 0545,1c
  SPIWrite 0546,02
  SPIWrite 0547,2d
  SPIWrite 0548,de
  SPIWrite 0549,db
  SPIWrite 054a,bd
  SPIWrite 054b,e8
  SPIWrite 054c,fe
  SPIWrite 054d,8f
  SPIWrite 054e,00
  SPIWrite 054f,00
  SPIWrite 0550,98
  SPIWrite 0551,b5
  SPIWrite 0552,e7
  SPIWrite 0553,f7
  SPIWrite 0554,93
  SPIWrite 0555,f8
  SPIWrite 0556,0c
  SPIWrite 0557,48
  SPIWrite 0558,0c
  SPIWrite 0559,4a
  SPIWrite 055a,00
  SPIWrite 055b,27
  SPIWrite 055c,4f
  SPIWrite 055d,f6
  SPIWrite 055e,df
  SPIWrite 055f,73
  SPIWrite 0560,40
  SPIWrite 0561,1e
  SPIWrite 0562,10
  SPIWrite 0563,f8
  SPIWrite 0564,01
  SPIWrite 0565,1f
  SPIWrite 0566,01
  SPIWrite 0567,29
  SPIWrite 0568,09
  SPIWrite 0569,d1
  SPIWrite 056a,00
  SPIWrite 056b,2f
  SPIWrite 056c,14
  SPIWrite 056d,bf
  SPIWrite 056e,02
  SPIWrite 056f,f1
  SPIWrite 0570,b8
  SPIWrite 0571,04
  SPIWrite 0572,14
  SPIWrite 0573,1c
  SPIWrite 0574,21
  SPIWrite 0575,88
  SPIWrite 0576,19
  SPIWrite 0577,40
```

```
  SPIWrite 0578,41
  SPIWrite 0579,f4
  SPIWrite 057a,00
  SPIWrite 057b,51
  SPIWrite 057c,21
  SPIWrite 057d,80
  SPIWrite 057e,7f
  SPIWrite 057f,1c
  SPIWrite 0580,02
  SPIWrite 0581,2f
  SPIWrite 0582,ee
  SPIWrite 0583,db
  SPIWrite 0584,98
  SPIWrite 0585,bd
  SPIWrite 0586,c0
  SPIWrite 0587,46
  SPIWrite 0588,9e
  SPIWrite 0589,13
  SPIWrite 058a,01
  SPIWrite 058b,20
  SPIWrite 058c,06
  SPIWrite 058d,07
  SPIWrite 058e,06
  SPIWrite 058f,a8
  SPIWrite 0590,0b
  SPIWrite 0591,49
  SPIWrite 0592,0c
  SPIWrite 0593,4b
  SPIWrite 0594,0c
  SPIWrite 0595,22
  SPIWrite 0596,10
  SPIWrite 0597,b5
  SPIWrite 0598,09
  SPIWrite 0599,18
  SPIWrite 059a,10
  SPIWrite 059b,fb
  SPIWrite 059c,02
  SPIWrite 059d,33
  SPIWrite 059e,91
  SPIWrite 059f,f8
  SPIWrite 05a0,b8
  SPIWrite 05a1,21
  SPIWrite 05a2,5c
  SPIWrite 05a3,68
  SPIWrite 05a4,c2
  SPIWrite 05a5,f1
  SPIWrite 05a6,01
  SPIWrite 05a7,02
  SPIWrite 05a8,84
  SPIWrite 05a9,f8
  SPIWrite 05aa,70
  SPIWrite 05ab,27
  SPIWrite 05ac,9a
  SPIWrite 05ad,68
  SPIWrite 05ae,91
  SPIWrite 05af,f8
  SPIWrite 05b0,b8
  SPIWrite 05b1,11
  SPIWrite 05b2,c1
  SPIWrite 05b3,f1
  SPIWrite 05b4,01
  SPIWrite 05b5,01
  SPIWrite 05b6,82
  SPIWrite 05b7,f8
  SPIWrite 05b8,70
  SPIWrite 05b9,17
  SPIWrite 05ba,dd
  SPIWrite 05bb,f7
  SPIWrite 05bc,44
```

```
SPIWrite 05bd,ff
SPIWrite 05be,10
SPIWrite 05bf,bd
SPIWrite 05c0,b4
SPIWrite 05c1,01
SPIWrite 05c2,01
SPIWrite 05c3,20
SPIWrite 05c4,a8
SPIWrite 05c5,75
SPIWrite 05c6,02
SPIWrite 05c7,00
SPIWrite 05c8,08
SPIWrite 05c9,b5
SPIWrite 05ca,eb
SPIWrite 05cb,f7
SPIWrite 05cc,e1
SPIWrite 05cd,ff
SPIWrite 05ce,4f
SPIWrite 05cf,f4
SPIWrite 05d0,11
SPIWrite 05d1,60
SPIWrite 05d2,00
SPIWrite 05d3,78
SPIWrite 05d4,08
SPIWrite 05d5,bd
SPIWrite 05d6,38
SPIWrite 05d7,b5
SPIWrite 05d8,04
SPIWrite 05d9,4d
SPIWrite 05da,05
SPIWrite 05db,4c
SPIWrite 05dc,05
SPIWrite 05dd,4b
SPIWrite 05de,2d
SPIWrite 05df,78
SPIWrite 05e0,24
SPIWrite 05e1,78
SPIWrite 05e2,1b
SPIWrite 05e3,78
SPIWrite 05e4,ec
SPIWrite 05e5,f7
SPIWrite 05e6,1c
SPIWrite 05e7,f8
SPIWrite 05e8,38
SPIWrite 05e9,bd
SPIWrite 05ea,c0
SPIWrite 05eb,46
SPIWrite 05ec,20
SPIWrite 05ed,00
SPIWrite 05ee,00
SPIWrite 05ef,64
SPIWrite 05f0,20
SPIWrite 05f1,00
SPIWrite 05f2,00
SPIWrite 05f3,54
SPIWrite 05f4,20
SPIWrite 05f5,00
SPIWrite 05f6,00
SPIWrite 05f7,74
SPIWrite 05f8,38
SPIWrite 05f9,b5
SPIWrite 05fa,05
SPIWrite 05fb,4d
SPIWrite 05fc,00
SPIWrite 05fd,24
SPIWrite 05fe,28
SPIWrite 05ff,68
SPIWrite 0600,01
SPIWrite 0601,46
```

```
  SPIWrite 0602,20
  SPIWrite 0603,46
  SPIWrite 0604,88
  SPIWrite 0605,47
  SPIWrite 0606,64
  SPIWrite 0607,1c
  SPIWrite 0608,04
  SPIWrite 0609,2c
  SPIWrite 060a,f8
  SPIWrite 060b,db
  SPIWrite 060c,38
  SPIWrite 060d,bd
  SPIWrite 060e,c0
  SPIWrite 060f,46
  SPIWrite 0610,ec
  SPIWrite 0611,de
  SPIWrite 0612,00
  SPIWrite 0613,20
  SPIWrite 0614,70
  SPIWrite 0615,47
  SPIWrite 0616,03
  SPIWrite 0617,48
  SPIWrite 0618,00
  SPIWrite 0619,78
  SPIWrite 061a,08
  SPIWrite 061b,b9
  SPIWrite 061c,ef
  SPIWrite 061d,f7
  SPIWrite 061e,e4
  SPIWrite 061f,bc
  SPIWrite 0620,70
  SPIWrite 0621,47
  SPIWrite 0622,c0
  SPIWrite 0623,46
  SPIWrite 0624,a1
  SPIWrite 0625,13
  SPIWrite 0626,01
  SPIWrite 0627,20
  SPIWrite 0628,03
  SPIWrite 0629,48
  SPIWrite 062a,08
  SPIWrite 062b,21
  SPIWrite 062c,41
  SPIWrite 062d,76
  SPIWrite 062e,09
  SPIWrite 062f,21
  SPIWrite 0630,c1
  SPIWrite 0631,76
  SPIWrite 0632,41
  SPIWrite 0633,77
  SPIWrite 0634,70
  SPIWrite 0635,47
  SPIWrite 0636,c0
  SPIWrite 0637,46
  SPIWrite 0638,88
  SPIWrite 0639,18
  SPIWrite 063a,01
  SPIWrite 063b,20
  SPIWrite 063c,00
  SPIWrite 063d,04
  SPIWrite 063e,07
  SPIWrite 063f,07
  SPIWrite 0640,00
  SPIWrite 0641,00
  SPIWrite 0642,03
  SPIWrite 0643,07
  SPIWrite 0644,00
  SPIWrite 0645,00
  SPIWrite 0646,00
```

```
SPIWrite 0647,07
SPIWrite 0648,00
SPIWrite 0649,05
SPIWrite 064a,05
SPIWrite 064b,07
SPIWrite 064c,07
SPIWrite 064d,00
SPIWrite 064e,0a
SPIWrite 064f,0c
SPIWrite 0650,0a
SPIWrite 0651,16
SPIWrite 0652,14
SPIWrite 0653,16
SPIWrite 0654,14
SPIWrite 0655,00
SPIWrite 0656,16
SPIWrite 0657,00
SPIWrite 0658,16
SPIWrite 0659,16
SPIWrite 065a,14
SPIWrite 065b,16
SPIWrite 065c,14
SPIWrite 065d,00
SPIWrite 065e,00
SPIWrite 065f,00
SPIWrite 0660,00
SPIWrite 0661,16
SPIWrite 0662,14
SPIWrite 0663,16
SPIWrite 0664,14
SPIWrite 0665,00
SPIWrite 0666,15
SPIWrite 0667,00
SPIWrite 0668,00
SPIWrite 0669,00
SPIWrite 066a,00
SPIWrite 066b,00
SPIWrite 066c,00
SPIWrite 066d,01
SPIWrite 066e,02
SPIWrite 066f,01
SPIWrite 0670,10
SPIWrite 0671,0a
SPIWrite 0672,10
SPIWrite 0673,00
SPIWrite 0674,00
SPIWrite 0675,00
SPIWrite 0676,00
SPIWrite 0677,00
SPIWrite 0678,00
SPIWrite 0679,00
SPIWrite 067a,00
SPIWrite 067b,06
SPIWrite 067c,02
SPIWrite 067d,01
SPIWrite 067e,10
SPIWrite 067f,0a
SPIWrite 0680,10
SPIWrite 0681,00
SPIWrite 0682,07
SPIWrite 0683,00
SPIWrite 0684,01
SPIWrite 0685,00
SPIWrite 0686,0a
SPIWrite 0687,00
SPIWrite 0688,00
SPIWrite 0689,16
SPIWrite 068a,00
SPIWrite 068b,00
```

```
  SPIWrite 068c,00
  SPIWrite 068d,0a
  SPIWrite 068e,00
  SPIWrite 068f,00
  SPIWrite 0690,01
  SPIWrite 0691,10
  SPIWrite 0692,01
  SPIWrite 0693,10
  SPIWrite 0694,0a
  SPIWrite 0695,00
  SPIWrite 0696,00
  SPIWrite 0697,07
  SPIWrite 0698,10
  SPIWrite 0699,01
  SPIWrite 069a,0f
  SPIWrite 069b,0a
  SPIWrite 069c,00
  SPIWrite 069d,00
  SPIWrite 069e,00
  SPIWrite 069f,00
  SPIWrite 06a0,08
  SPIWrite 06a1,00
  SPIWrite 06a2,00
  SPIWrite 06a3,00
  SPIWrite 06a4,00
  SPIWrite 06a5,01
  SPIWrite 06a6,10
  SPIWrite 06a7,0a
  SPIWrite 06a8,00
  SPIWrite 06a9,00
  SPIWrite 06aa,00
  SPIWrite 06ab,00
  SPIWrite 06ac,00
  SPIWrite 06ad,02
  SPIWrite 06ae,00
  SPIWrite 06af,00
  SPIWrite 06b0,00
  SPIWrite 06b1,00
  SPIWrite 06b2,00
  SPIWrite 06b3,00
  SPIWrite 06b4,00
  SPIWrite 06b5,00
  SPIWrite 06b6,00
  SPIWrite 06b7,00
  SPIWrite 06b8,00
  SPIWrite 06b9,00
  SPIWrite 06ba,00
  SPIWrite 06bb,00
  SPIWrite 06bc,00
  SPIWrite 06bd,00
  SPIWrite 06be,00
  SPIWrite 06bf,00
  SPIWrite 06c0,00
  SPIWrite 06c1,00
  SPIWrite 06c2,11
  SPIWrite 06c3,00
  SPIWrite 06c4,00
  SPIWrite 06c5,00
  SPIWrite 06c6,00
  SPIWrite 06c7,00
  SPIWrite 06c8,01
  SPIWrite 06c9,16
  SPIWrite 06ca,01
  SPIWrite 06cb,10
  SPIWrite 06cc,0a
  SPIWrite 06cd,10
  SPIWrite 06ce,00
  SPIWrite 06cf,01
  SPIWrite 06d0,03
```

```
  SPIWrite 06d1,01
  SPIWrite 06d2,10
  SPIWrite 06d3,0a
  SPIWrite 06d4,10
  SPIWrite 06d5,00
  SPIWrite 06d6,00
  SPIWrite 06d7,12
  SPIWrite 06d8,01
  SPIWrite 06d9,10
  SPIWrite 06da,0a
  SPIWrite 06db,00
  SPIWrite 06dc,00
  SPIWrite 06dd,00
  SPIWrite 06de,11
  SPIWrite 06df,01
  SPIWrite 06e0,10
  SPIWrite 06e1,0a
  SPIWrite 06e2,00
  SPIWrite 06e3,00
  SPIWrite 06e4,01
  SPIWrite 06e5,10
  SPIWrite 06e6,01
  SPIWrite 06e7,0e
  SPIWrite 06e8,0a
  SPIWrite 06e9,00
  SPIWrite 06ea,00
  SPIWrite 06eb,01
  SPIWrite 06ec,0f
  SPIWrite 06ed,0a
  SPIWrite 06ee,00
  SPIWrite 06ef,00
  SPIWrite 06f0,00
  SPIWrite 06f1,00
  SPIWrite 06f2,00
  SPIWrite 06f3,00
  SPIWrite 06f4,00
  SPIWrite 06f5,00
  SPIWrite 06f6,00
  SPIWrite 06f7,00
  SPIWrite 06f8,00
  SPIWrite 06f9,00
  SPIWrite 06fa,00
  SPIWrite 06fb,00
  SPIWrite 06fc,00
  SPIWrite 06fd,00
  SPIWrite 06fe,00
  SPIWrite 06ff,00
  SPIWrite 0700,00
  SPIWrite 0701,00
  SPIWrite 0702,00
  SPIWrite 0703,00
  SPIWrite 0704,00
  SPIWrite 0705,00
  SPIWrite 0706,00
  SPIWrite 0707,00
  SPIWrite 0708,03
  SPIWrite 0709,00
  SPIWrite 070a,00
  SPIWrite 070b,00
  SPIWrite 070c,00
  SPIWrite 070d,00
  SPIWrite 070e,00
  SPIWrite 070f,00
  SPIWrite 0710,00
  SPIWrite 0711,00
  SPIWrite 0712,00
  SPIWrite 0713,00
  SPIWrite 0714,00
  SPIWrite 0715,07
```

```
  SPIWrite 0716,00
  SPIWrite 0717,00
  SPIWrite 0718,00
  SPIWrite 0719,00
  SPIWrite 071a,00
  SPIWrite 071b,00
  SPIWrite 071c,01
  SPIWrite 071d,03
  SPIWrite 071e,01
  SPIWrite 071f,10
  SPIWrite 0720,0a
  SPIWrite 0721,10
  SPIWrite 0722,00
  SPIWrite 0723,09
  SPIWrite 0724,02
  SPIWrite 0725,01
  SPIWrite 0726,10
  SPIWrite 0727,0a
  SPIWrite 0728,10
  SPIWrite 0729,00
  SPIWrite 072a,07
  SPIWrite 072b,00
  SPIWrite 072c,01
  SPIWrite 072d,00
  SPIWrite 072e,0a
  SPIWrite 072f,00
  SPIWrite 0730,00
  SPIWrite 0731,01
  SPIWrite 0732,10
  SPIWrite 0733,0a
  SPIWrite 0734,10
  SPIWrite 0735,0a
  SPIWrite 0736,00
  SPIWrite 0737,00
  SPIWrite 0738,00
  SPIWrite 0739,00
  SPIWrite 073a,00
  SPIWrite 073b,00
  SPIWrite 073c,00
  SPIWrite 073d,02
  SPIWrite 073e,00
  SPIWrite 073f,02
  SPIWrite 0740,06
  SPIWrite 0741,00
  SPIWrite 0742,00
  SPIWrite 0743,00
  SPIWrite 0744,00
  SPIWrite 0745,00
  SPIWrite 0746,00
  SPIWrite 0747,00
  SPIWrite 0748,00
  SPIWrite 0749,02
  SPIWrite 074a,06
  SPIWrite 074b,00
  SPIWrite 074c,00
  SPIWrite 074d,00
  SPIWrite 074e,00
  SPIWrite 074f,00
  SPIWrite 0750,00
  SPIWrite 0751,00
  SPIWrite 0752,00
  SPIWrite 0753,00
  SPIWrite 0754,06
  SPIWrite 0755,00
  SPIWrite 0756,00
  SPIWrite 0757,00
  SPIWrite 0758,7c
  SPIWrite 0759,1c
  SPIWrite 075a,01
```

```
SPIWrite 075b,20
SPIWrite 075c,d1
SPIWrite 075d,1e
SPIWrite 075e,01
SPIWrite 075f,20
SPIWrite 0760,84
SPIWrite 0761,1a
SPIWrite 0762,01
SPIWrite 0763,20
SPIWrite 0764,26
SPIWrite 0765,07
SPIWrite 0766,01
SPIWrite 0767,20
SPIWrite 0768,4a
SPIWrite 0769,0c
SPIWrite 076a,01
SPIWrite 076b,20
SPIWrite 076c,1c
SPIWrite 076d,16
SPIWrite 076e,03
SPIWrite 076f,00
SPIWrite 0770,28
SPIWrite 0771,16
SPIWrite 0772,03
SPIWrite 0773,00
SPIWrite 0774,2d
SPIWrite 0775,16
SPIWrite 0776,03
SPIWrite 0777,00
SPIWrite 0778,45
SPIWrite 0779,16
SPIWrite 077a,03
SPIWrite 077b,00
SPIWrite 077c,fb
SPIWrite 077d,20
SPIWrite 077e,01
SPIWrite 077f,20
SPIWrite 0780,00
SPIWrite 0781,20
SPIWrite 0782,01
SPIWrite 0783,20
SPIWrite 0784,0c
SPIWrite 0785,20
SPIWrite 0786,01
SPIWrite 0787,20
SPIWrite 0788,11
SPIWrite 0789,20
SPIWrite 078a,01
SPIWrite 078b,20
SPIWrite 078c,29
SPIWrite 078d,20
SPIWrite 078e,01
SPIWrite 078f,20
SPIWrite 0790,93
SPIWrite 0791,21
SPIWrite 0792,01
SPIWrite 0793,20
SPIWrite 0794,00
SPIWrite 0018,00    //sys_calib_macro_memory=0x0;   Address(0x18[7:0])
SPIWrite 0018,20    //macro=0x1;    Address(0x18[7:5])
SPIRead 00f0

//Read  MACRO_READY=0x1;    Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,07    //MACRO_OPERAND_REG0=0x7750000;
Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
```

```
SPIWrite 00a2,75
SPIWrite 00a1,00
SPIWrite 00a0,00
SPIWrite 00a7,00    //MACRO_OPERAND_REG1=0x1000;
Address(0xa4[7:0],0xa5[7:0],0xa6[7:0],0xa7[7:0],0xa8[7:0])
SPIWrite 00a6,00
SPIWrite 00a5,10
SPIWrite 00a4,00
SPIWrite 0193,78    //MACRO_OPCODE=0x78;    Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0

//Read  MACRO_DONE=0x1;     Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIRead 00f0

//Read  MACRO_ERROR=0x0;    Address(0xf0[7:3])

SPIRead 00f1

//Read  MACRO_ERROR_OPCODE=0x0;     Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0

//Read  MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0

//Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;     Address(0xf0[7:5])

SPIRead 00f0

//Read  MACRO_ERROR_IN_OPERAND=0x0;     Address(0xf0[7:6])

SPIRead 00f0

//Read  MACRO_ERROR_IN_EXECUTION=0x0;   Address(0xf0[7:7])

SPIRead 00f3
SPIRead 00f2

//Read  MACRO_ERROR_EXTENDED_CODE=0x0;  Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7
SPIRead 00f6
SPIRead 00f5
SPIRead 00f4

//Read  MACRO_ERROR_EXTENDED_CODE_2=0x0;
Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0

//Read  MACRO_READY=0x1;    Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00    //MACRO_OPERAND_REG0=0x1;
Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00
SPIWrite 00a1,00
SPIWrite 00a0,01
SPIWrite 0193,78    //MACRO_OPCODE=0x78;    Address(0x193[7:0],0x194[7:0])

```

```
WAIT 0.001
SPIRead 00f0

//Read  MACRO_DONE=0x1;     Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIRead 00f0

//Read  MACRO_ERROR=0x0;    Address(0xf0[7:3])

SPIRead 00f1

//Read  MACRO_ERROR_OPCODE=0x0;     Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0

//Read  MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0

//Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;     Address(0xf0[7:5])

SPIRead 00f0

//Read  MACRO_ERROR_IN_OPERAND=0x0;     Address(0xf0[7:6])

SPIRead 00f0

//Read  MACRO_ERROR_IN_EXECUTION=0x0;   Address(0xf0[7:7])

SPIRead 00f3
SPIRead 00f2

//Read  MACRO_ERROR_EXTENDED_CODE=0x0;  Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7
SPIRead 00f6
SPIRead 00f5
SPIRead 00f4

//Read  MACRO_ERROR_EXTENDED_CODE_2=0x0;
Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0

//Read  MACRO_READY=0x1;    Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00    //MACRO_OPERAND_REG0=0x3;
Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00
SPIWrite 00a1,00
SPIWrite 00a0,03
SPIWrite 0193,01    //MACRO_OPCODE=0x1;     Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0

//Read  MACRO_DONE=0x1;     Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIRead 00f0

```

```
7018   //Read  MACRO_ERROR=0x0;    Address(0xf0[7:3])
7019
7020   SPIRead 00f1
7021
7022   //Read  MACRO_ERROR_OPCODE=0x0;     Address(0xf1[7:0],0xf2[7:0])
7023
7024   SPIRead 00f0
7025
7026   //Read  MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])
7027
7028   SPIRead 00f0
7029
7030   //Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;     Address(0xf0[7:5])
7031
7032   SPIRead 00f0
7033
7034   //Read  MACRO_ERROR_IN_OPERAND=0x0;     Address(0xf0[7:6])
7035
7036   SPIRead 00f0
7037
7038   //Read  MACRO_ERROR_IN_EXECUTION=0x0;   Address(0xf0[7:7])
7039
7040   SPIRead 00f3
7041   SPIRead 00f2
7042
7043   //Read  MACRO_ERROR_EXTENDED_CODE=0x0;  Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
7044
7045   SPIRead 00f7
7046   SPIRead 00f6
7047   SPIRead 00f5
7048   SPIRead 00f4
7049
7050   //Read  MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
7051
7052   SPIRead 00fb
7053   SPIRead 00fa
7054   SPIRead 00f9
7055   SPIRead 00f8
7056
7057   //Read  MACRO_RESULT_REG0=0x14010200;
      Address(0xf8[7:0],0xf9[7:0],0xfa[7:0],0xfb[7:0],0xfc[7:0])
7058
7059   SPIRead 00ff
7060   SPIRead 00fe
7061   SPIRead 00fd
7062   SPIRead 00fc
7063
7064   //Read  MACRO_RESULT_REG1=0x8e;
      Address(0xfc[7:0],0xfd[7:0],0xfe[7:0],0xff[7:0],0x100[7:0])
7065
7066   SPIWrite 0018,00    //macro=0x0;    Address(0x18[7:5])
7067
7068   //STEP: pllEfuse/step0
7069
7070   //START: Enabling Temp Sense
7071
7072   SPIWrite 0015,02    //ana_4t4r=0x1;     Address(0x15[7:1])
7073   SPIWrite 00c0,80    //EN_CLK_TEMP_SENSE=0x1;    Address(0xc0[7:7])
7074   SPIWrite 0015,00    //ana_4t4r=0x0;     Address(0x15[7:1])
7075   SPIWrite 0015,40    //digtop=0x1;   Address(0x15[7:6])
7076   SPIWrite 02a3,00    //temp_sense1_cfg0=0x7e;
      Address(0x2a0[7:0],0x2a1[7:0],0x2a2[7:0],0x2a3[7:0],0x2a4[7:0])
7077   SPIWrite 02a2,00
7078   SPIWrite 02a1,00
7079   SPIWrite 02a0,7e
7080   SPIWrite 02a7,01    //temp_sense1_cfg1=0x1000000;
      Address(0x2a4[7:0],0x2a5[7:0],0x2a6[7:0],0x2a7[7:0],0x2a8[7:0])
7081   SPIWrite 02a6,00
```

```
SPIWrite 02a5,00
SPIWrite 02a4,00

//END: Enabling Temp Sense


//START: Loading PLL EFuse trims

SPIWrite 0015,00    //digtop=0x0;   Address(0x15[7:6])
SPIWrite 0018,20    //macro=0x1;    Address(0x18[7:5])
SPIRead 00f0

//Read  MACRO_READY=0x1;    Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00    //MACRO_OPERAND_REG0=0x21f;
Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00
SPIWrite 00a1,02
SPIWrite 00a0,1f
SPIWrite 0193,33    //MACRO_OPCODE=0x33;    Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0

//Read  MACRO_DONE=0x1;     Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIRead 00f0

//Read  MACRO_ERROR=0x0;    Address(0xf0[7:3])

SPIRead 00f1

//Read  MACRO_ERROR_OPCODE=0x0;     Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0

//Read  MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0

//Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;     Address(0xf0[7:5])

SPIRead 00f0

//Read  MACRO_ERROR_IN_OPERAND=0x0;     Address(0xf0[7:6])

SPIRead 00f0

//Read  MACRO_ERROR_IN_EXECUTION=0x0;   Address(0xf0[7:7])

SPIRead 00f3
SPIRead 00f2

//Read  MACRO_ERROR_EXTENDED_CODE=0x0;  Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7
SPIRead 00f6
SPIRead 00f5
SPIRead 00f4

//Read  MACRO_ERROR_EXTENDED_CODE_2=0x0;
Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

```

```
SPIRead 00f0

//Read  MACRO_READY=0x1;    Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00    //MACRO_OPERAND_REG0=0x10f;
Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00
SPIWrite 00a1,01
SPIWrite 00a0,0f
SPIWrite 0193,34    //MACRO_OPCODE=0x34;    Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0

//Read  MACRO_DONE=0x1;     Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIRead 00f0

//Read  MACRO_ERROR=0x0;    Address(0xf0[7:3])

SPIRead 00f1

//Read  MACRO_ERROR_OPCODE=0x0;     Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0

//Read  MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0

//Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;     Address(0xf0[7:5])

SPIRead 00f0

//Read  MACRO_ERROR_IN_OPERAND=0x0;     Address(0xf0[7:6])

SPIRead 00f0

//Read  MACRO_ERROR_IN_EXECUTION=0x0;   Address(0xf0[7:7])

SPIRead 00f3
SPIRead 00f2

//Read  MACRO_ERROR_EXTENDED_CODE=0x0;  Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7
SPIRead 00f6
SPIRead 00f5
SPIRead 00f4

//Read  MACRO_ERROR_EXTENDED_CODE_2=0x0;
Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0

//Read  MACRO_READY=0x1;    Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00    //MACRO_OPERAND_REG0=0x1;
Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00
```

```
SPIWrite 00a1,00
SPIWrite 00a0,01
SPIWrite 0193,72    //MACRO_OPCODE=0x72;    Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0

//Read  MACRO_DONE=0x1;     Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIRead 00f0

//Read  MACRO_ERROR=0x0;    Address(0xf0[7:3])

SPIRead 00f1

//Read  MACRO_ERROR_OPCODE=0x0;     Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0

//Read  MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0

//Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;     Address(0xf0[7:5])

SPIRead 00f0

//Read  MACRO_ERROR_IN_OPERAND=0x0;     Address(0xf0[7:6])

SPIRead 00f0

//Read  MACRO_ERROR_IN_EXECUTION=0x0;   Address(0xf0[7:7])

SPIRead 00f3
SPIRead 00f2

//Read  MACRO_ERROR_EXTENDED_CODE=0x0;  Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7
SPIRead 00f6
SPIRead 00f5
SPIRead 00f4

//Read  MACRO_ERROR_EXTENDED_CODE_2=0x0;
Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0

//Read  MACRO_READY=0x1;    Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00    //MACRO_OPERAND_REG0=0xe0100;
Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,0e
SPIWrite 00a1,01
SPIWrite 00a0,00
SPIWrite 0193,71    //MACRO_OPCODE=0x71;    Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0

//Read  MACRO_DONE=0x1;     Address(0xf0[7:2])


```

```
SPIPoll 00f0,2,2,4

SPIRead 00f0

//Read  MACRO_ERROR=0x0;    Address(0xf0[7:3])

SPIRead 00f1

//Read  MACRO_ERROR_OPCODE=0x0;     Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0

//Read  MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0

//Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;     Address(0xf0[7:5])

SPIRead 00f0

//Read  MACRO_ERROR_IN_OPERAND=0x0;     Address(0xf0[7:6])

SPIRead 00f0

//Read  MACRO_ERROR_IN_EXECUTION=0x0;   Address(0xf0[7:7])

SPIRead 00f3
SPIRead 00f2

//Read  MACRO_ERROR_EXTENDED_CODE=0x0;  Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7
SPIRead 00f6
SPIRead 00f5
SPIRead 00f4

//Read  MACRO_ERROR_EXTENDED_CODE_2=0x0;
Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])


//END: Done Loading PLL EFuse trims

SPIRead 00f0

//Read  MACRO_READY=0x1;    Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00    //MACRO_OPERAND_REG0=0x10101;
Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,01
SPIWrite 00a1,01
SPIWrite 00a0,01
SPIWrite 0193,73    //MACRO_OPCODE=0x73;    Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0

//Read  MACRO_DONE=0x1;     Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIRead 00f0

//Read  MACRO_ERROR=0x0;    Address(0xf0[7:3])

SPIRead 00f1
```

```
7349
7350   //Read  MACRO_ERROR_OPCODE=0x0;     Address(0xf1[7:0],0xf2[7:0])
7351
7352   SPIRead 00f0
7353
7354   //Read  MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])
7355
7356   SPIRead 00f0
7357
7358   //Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;     Address(0xf0[7:5])
7359
7360   SPIRead 00f0
7361
7362   //Read  MACRO_ERROR_IN_OPERAND=0x0;     Address(0xf0[7:6])
7363
7364   SPIRead 00f0
7365
7366   //Read  MACRO_ERROR_IN_EXECUTION=0x0;   Address(0xf0[7:7])
7367
7368   SPIRead 00f3
7369   SPIRead 00f2
7370
7371   //Read  MACRO_ERROR_EXTENDED_CODE=0x0;  Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
7372
7373   SPIRead 00f7
7374   SPIRead 00f6
7375   SPIRead 00f5
7376   SPIRead 00f4
7377
7378   //Read  MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
7379
7380   SPIWrite 0018,00    //macro=0x0;    Address(0x18[7:5])
7381   SPIWrite 0012,01    //rxdig=0x1;    Address(0x12[7:0])
7382   SPIWrite 0761,0a    //cfg_fmix_hbw_pmode=0x0;   Address(0x761[7:4])
7383   SPIWrite 0012,02    //rxdig=0x2;    Address(0x12[7:0])
7384   SPIWrite 0761,0a    //cfg_fmix_hbw_pmode=0x0;   Address(0x761[7:4])
7385   SPIWrite 0012,04    //rxdig=0x4;    Address(0x12[7:0])
7386   SPIWrite 0761,0a    //cfg_fmix_hbw_pmode=0x0;   Address(0x761[7:4])
7387   SPIWrite 0012,08    //rxdig=0x8;    Address(0x12[7:0])
7388   SPIWrite 0761,0a    //cfg_fmix_hbw_pmode=0x0;   Address(0x761[7:4])
7389   SPIWrite 0012,00    //rxdig=0x0;    Address(0x12[7:0])
7390
7391   //STEP: pllConfig/step0
7392
7393   //START: Configuring PLL
7394
7395   SPIWrite 0015,08    //rx=0x2;   Address(0x15[7:2])
7396   SPIWrite 0043,00    //po_to_rx_2r_rxab_config_6=0x0;
      Address(0x40[7:0],0x41[7:0],0x42[7:0],0x43[7:0],0x44[7:0])
7397   SPIWrite 0042,00
7398   SPIWrite 0041,00
7399   SPIWrite 0040,00
7400   SPIWrite 0015,00    //rx=0x0;   Address(0x15[7:2])
7401   SPIWrite 0015,02    //ana_4t4r=0x1;     Address(0x15[7:1])
7402   SPIWrite 00c1,60    //DIS_DIGCLK=0x3;   Address(0xc1[7:5])
7403
7404   //START: Requesting/releasing SPI Access to PLL Pages
7405
7406   SPIWrite 0015,00    //ana_4t4r=0x0;     Address(0x15[7:1])
7407   SPIWrite 0015,40    //digtop=0x1;   Address(0x15[7:6])
7408   SPIWrite 0170,01    //pll_reg_spi_req_a=0x1;    Address(0x170[7:0])
7409   SPIWrite 0540,00    //pll_reg_spi_req_b1=0x0;   Address(0x540[7:0])
7410
7411   SPIPoll 0171,0,0,01
7412   SPIRead 0171
7413
7414   //Read  pll_reg_spi_a_ack=0x1(Meaning: );;  Address(0x171[7:0])
7415
```

```
7416
7417   //END: Requesting/releasing SPI Access to PLL Pages
7418
7419   SPIWrite 0015,00    //digtop=0x0;   Address(0x15[7:6])
7420   SPIWrite 0015,01    //pll=0x1;  Address(0x15[7:0])
7421   SPIWrite 003f,08    //EN_CP=0x1;    Address(0x3f[7:3])
7422   SPIWrite 0028,01    //EN_BIAS=0x1;  Address(0x28[7:0])
7423   SPIWrite 0035,10    //EN_LDO_ANA=0x1;   Address(0x35[7:4])
7424   SPIWrite 0036,40    //EN_LDO_RF=0x1;    Address(0x36[7:6])
7425   SPIWrite 0038,08    //EN_LDO_TXFB=0x1;  Address(0x38[7:3])
7426   SPIWrite 0039,20    //EN_LDO_RX=0x1;    Address(0x39[7:5])
7427   SPIWrite 003b,08    //EN_LDO_REFD2S=0x1;    Address(0x3b[7:3])
7428   SPIWrite 0046,60    //EN_VCO=0x1;   Address(0x46[7:5])
7429   SPIWrite 0046,60    //EN_VCO_PKDET=0x1;     Address(0x46[7:6])
7430   SPIWrite 0043,18    //EN_VCTRL_ADC=0x1;     Address(0x43[7:4])
7431   SPIWrite 0043,18    //EN_VREF_CAL=0x1;  Address(0x43[7:3])
7432   SPIWrite 004c,00    //CTL_VCO_BUF_ATT=0x0;  Address(0x4c[7:0])
7433   SPIWrite 003c,e0    //EN_REFDIV_DIV=0x1;    Address(0x3c[7:5])
7434   SPIWrite 0015,00    //pll=0x0;  Address(0x15[7:0])
7435   SPIWrite 0015,02    //ana_4t4r=0x1;     Address(0x15[7:1])
7436   SPIWrite 010c,00    //EN_REFDIV_DMP=0x0;    Address(0x10c[7:0])
7437   SPIWrite 0015,00    //ana_4t4r=0x0;     Address(0x15[7:1])
7438   SPIWrite 0015,01    //pll=0x1;  Address(0x15[7:0])
7439   SPIWrite 003c,60    //EN_REFDIV_DMP=0x0;    Address(0x3c[7:7])
7440   SPIWrite 003c,20    //EN_REFDIV_SYNC=0x0;   Address(0x3c[7:6])
7441   SPIWrite 003d,00    //CTL_REFDIV_EDGE_SEL=0x0;  Address(0x3d[7:0])
7442   SPIWrite 0015,00    //pll=0x0;  Address(0x15[7:0])
7443   SPIWrite 0015,02    //ana_4t4r=0x1;     Address(0x15[7:1])
7444   SPIWrite 010d,01    //CTL_REFDIV_DIV=0x1;   Address(0x10d[7:0])
7445   SPIWrite 0015,00    //ana_4t4r=0x0;     Address(0x15[7:1])
7446   SPIWrite 0015,01    //pll=0x1;  Address(0x15[7:0])
7447   SPIWrite 0056,43    //CTL_SYNC_SYSREF_CLK_MUX=0x1;  Address(0x56[7:6])
7448   SPIWrite 0056,c3    //CTL_SYNC_SYSREF_MUX=0x1;  Address(0x56[7:7])
7449   SPIWrite 0056,c3    //CTL_SYNC_LCM_MUX=0x0;     Address(0x56[7:3])
7450   SPIWrite 0056,f3    //CTL_SYNC_LCMDIV=0x3;  Address(0x56[7:4])
7451   SPIWrite 0057,02    //CTL_SYNC_SYSREF_OUT_MUX=0x1;  Address(0x57[7:1])
7452   SPIWrite 0015,00    //pll=0x0;  Address(0x15[7:0])
7453   SPIWrite 0015,80    //timing_controller=0x1;    Address(0x15[7:7])
7454   SPIWrite 07f5,01    //count_len_sysref=0x17f;   Address(0x7f4[7:0],0x7f5[7:0],0x7f6[7:0])
7455   SPIWrite 07f4,7f
7456   SPIWrite 0015,00    //timing_controller=0x0;    Address(0x15[7:7])
7457   SPIWrite 0015,01    //pll=0x1;  Address(0x15[7:0])
7458   SPIWrite 006d,01    //LCMGEN_DIV=0x17f;     Address(0x6c[7:0],0x6d[7:0],0x6e[7:0])
7459   SPIWrite 006c,7f
7460   SPIWrite 0062,00    //NO_OF_SYSREFS_REFDIV=0x0;     Address(0x62[7:4])
7461   SPIWrite 0015,00    //pll=0x0;  Address(0x15[7:0])
7462   SPIWrite 0015,02    //ana_4t4r=0x1;     Address(0x15[7:1])
7463   SPIWrite 010f,18    //CTL_FBDIV_DIV=0x18;   Address(0x10f[7:0])
7464   SPIWrite 010e,00    //CTL_FBDIV_DIVBY2=0x0;     Address(0x10e[7:0])
7465   SPIWrite 0015,00    //ana_4t4r=0x0;     Address(0x15[7:1])
7466   SPIWrite 0015,01    //pll=0x1;  Address(0x15[7:0])
7467   SPIWrite 0050,fe    //EN_OUTDIV_MUX_TX=0x3;     Address(0x50[7:1])
7468   SPIWrite 0050,fe    //EN_OUTDIV_MUX_RX=0x3;     Address(0x50[7:3])
7469   SPIWrite 0050,fe    //EN_OUTDIV_MUX_FB=0x3;     Address(0x50[7:5])
7470   SPIWrite 0015,00    //pll=0x0;  Address(0x15[7:0])
7471   SPIWrite 0015,02    //ana_4t4r=0x1;     Address(0x15[7:1])
7472   SPIWrite 0110,01    //CTL_OUTDIV_MUX_TX=0x1;    Address(0x110[7:0])
7473   SPIWrite 0015,00    //ana_4t4r=0x0;     Address(0x15[7:1])
7474   SPIWrite 0015,01    //pll=0x1;  Address(0x15[7:0])
7475   SPIWrite 0051,3f    //EN_OUTDIV_DIV_TX=0x1;     Address(0x51[7:1])
7476   SPIWrite 0015,00    //pll=0x0;  Address(0x15[7:0])
7477   SPIWrite 0015,02    //ana_4t4r=0x1;     Address(0x15[7:1])
7478   SPIWrite 0111,01    //CTL_OUTDIV_DIV_TX=0x1;    Address(0x111[7:0])
7479   SPIWrite 0015,00    //ana_4t4r=0x0;     Address(0x15[7:1])
7480   SPIWrite 0015,01    //pll=0x1;  Address(0x15[7:0])
7481   SPIWrite 007f,00    //MASK_EN_OUTDIV_MAIN_CLK_TX=0x0;   Address(0x7f[7:6])
7482   SPIWrite 0015,00    //pll=0x0;  Address(0x15[7:0])
7483   SPIWrite 0015,02    //ana_4t4r=0x1;     Address(0x15[7:1])
7484   SPIWrite 0112,01    //CTL_OUTDIV_MUX_RX=0x1;    Address(0x112[7:0])
```

```
SPIWrite 0015,00    //ana_4t4r=0x0;     Address(0x15[7:1])
SPIWrite 0015,01    //pll=0x1;  Address(0x15[7:0])
SPIWrite 0051,3f    //EN_OUTDIV_DIV_RX=0x1;     Address(0x51[7:2])
SPIWrite 0015,00    //pll=0x0;  Address(0x15[7:0])
SPIWrite 0015,02    //ana_4t4r=0x1;     Address(0x15[7:1])
SPIWrite 0113,03    //CTL_OUTDIV_DIV_RX=0x3;    Address(0x113[7:0])
SPIWrite 0015,00    //ana_4t4r=0x0;     Address(0x15[7:1])
SPIWrite 0015,01    //pll=0x1;  Address(0x15[7:0])
SPIWrite 007f,00    //MASK_EN_OUTDIV_MAIN_CLK_RX=0x0;   Address(0x7f[7:7])
SPIWrite 0015,00    //pll=0x0;  Address(0x15[7:0])
SPIWrite 0015,02    //ana_4t4r=0x1;     Address(0x15[7:1])
SPIWrite 0114,01    //CTL_OUTDIV_MUX_FB=0x1;    Address(0x114[7:0])
SPIWrite 0015,00    //ana_4t4r=0x0;     Address(0x15[7:1])
SPIWrite 0015,01    //pll=0x1;  Address(0x15[7:0])
SPIWrite 0051,3f    //EN_OUTDIV_DIV_FB=0x1;     Address(0x51[7:3])
SPIWrite 0015,00    //pll=0x0;  Address(0x15[7:0])
SPIWrite 0015,02    //ana_4t4r=0x1;     Address(0x15[7:1])
SPIWrite 0115,01    //CTL_OUTDIV_DIV_FB=0x1;    Address(0x115[7:0])
SPIWrite 0015,00    //ana_4t4r=0x0;     Address(0x15[7:1])
SPIWrite 0015,01    //pll=0x1;  Address(0x15[7:0])
SPIWrite 0051,2f    //EN_OUTDIV_MUX3_TX_JESD=0x0;   Address(0x51[7:4])
SPIWrite 0063,01    //NO_OF_SYSREFS_OUTDIV=0x1;     Address(0x63[7:0])
SPIWrite 0072,02    //SYSREF_PULSE_CNT_DIG=0x2;     Address(0x72[7:0],0x73[7:0])
SPIWrite 006f,05    //SYSREF_PULSE_CNT_TX=0x5;  Address(0x6f[7:0],0x70[7:0])
SPIWrite 0070,02    //SYSREF_PULSE_CNT_RX=0x2;  Address(0x70[7:0],0x71[7:0])
SPIWrite 0071,02    //SYSREF_PULSE_CNT_FB=0x2;  Address(0x71[7:0],0x72[7:0])
SPIWrite 006d,01    //LCMGEN_DIV=0x17f;     Address(0x6c[7:0],0x6d[7:0],0x6e[7:0])
SPIWrite 006c,7f
SPIWrite 007c,04    //SYSREF_WIDTH=0x4;     Address(0x7c[7:0])
SPIWrite 0055,ff    //EN_SYNC_LCM_MUX=0x1;  Address(0x55[7:0])
SPIWrite 0055,ff    //EN_SYNC_SYSREF_CLK_MUX=0x1;   Address(0x55[7:7])
SPIWrite 0055,ff    //EN_SYNC_LCMDIV_CLKBUFF=0x1;   Address(0x55[7:1])
SPIWrite 0055,ff    //EN_SYNC_LCMDIV_STG=0xf;   Address(0x55[7:2])
SPIWrite 0055,ff    //EN_SYNC_LCMDIV_MUX=0x1;   Address(0x55[7:6])
SPIWrite 0059,01    //EN_SYNC_SYSREF_TO_OUTDIV_HANDOFF_CLK_MUX=0x1;
    Address(0x59[7:0])
SPIWrite 0058,00    //CTL_SYNC_SYSREF_TO_OUTDIV_HANDOFF_CLK_MUX=0x0;
    Address(0x58[7:7])
SPIWrite 0059,01    //EN_SYNC_SYSREF_MODE3=0x0;     Address(0x59[7:2])
SPIWrite 0059,01    //DIS_SYNC_SYSREF_MODE12=0x0;   Address(0x59[7:3])
SPIWrite 005c,00    //EN_DIV_STG_SERDES=0x0;    Address(0x5c[7:3])
SPIWrite 005d,04    //SEL_CLK_SERDES=0x2;   Address(0x5d[7:1])
SPIWrite 005d,0c    //SEL_REF_CLK_SERDES=0x1;   Address(0x5d[7:3])
SPIWrite 003d,01    //CTL_REFDIV_EDGE_SEL=0x1;  Address(0x3d[7:0])
SPIWrite 0053,03    //ESR_1P2_TXFB_CLKTOP=0x3;  Address(0x53[7:0])
SPIWrite 003e,0c    //ESR_1P8_CP=0x3;   Address(0x3e[7:2])
SPIWrite 0065,6a    //ESR_1P8_ANA_PLLTOP_LSB=0x1;   Address(0x65[7:6])
SPIWrite 004e,01    //ESR_1P8_ANA_PLLTOP_MSB=0x1;   Address(0x4e[7:0])
SPIWrite 0052,00    //ESR_1P2_RX_CLKTOP=0x0;    Address(0x52[7:5])
SPIWrite 0065,62    //ESR_1P2_RX_PLLTOP=0x0;    Address(0x65[7:2])
SPIWrite 0052,00    //ESR_1P2_TXFB_CML_MSB=0x0;     Address(0x52[7:0])
SPIWrite 0052,00    //ESR_1P2_TXFB_CML_LSB=0x0;     Address(0x52[7:4])
SPIWrite 0053,03    //ESR_1P8_BIAS_CLKTOP=0x0;  Address(0x53[7:2])
SPIWrite 005e,00    //ESR_1P8_BIAS_CLKTOP2=0x0;     Address(0x5e[7:1])
SPIWrite 0052,00    //ESR_1P2_VCO_CLKTOP_MSB=0x0;   Address(0x52[7:3])
SPIWrite 0052,00    //ESR_1P2_VCO_CLKTOP_LSB=0x0;   Address(0x52[7:7])
SPIWrite 003e,0c    //ESR_1P2_TXFB_PLLTOP=0x0;  Address(0x3e[7:4],0x3f[7:1])
SPIWrite 003f,08
SPIWrite 0065,60    //ESR_1P2_VCO_PLLTOP=0x0;   Address(0x65[7:0])
SPIWrite 0087,00    //ESR_1P2_VCOTOP=0x0;   Address(0x87[7:5])
SPIWrite 005e,00    //ESR_1P8_VCO_CLKTOP=0x0;   Address(0x5e[7:3])
SPIWrite 0087,00    //ESR_1P8_VCOTOP=0x0;   Address(0x87[7:1])
SPIWrite 0087,00    //ESR_PLL_LDOOUT=0x0;   Address(0x87[7:3])
SPIWrite 003e,0c    //ESR_1P2_CP=0x0;   Address(0x3e[7:0])
SPIWrite 0051,2f    //ESR_1P2_DIG_MISCTOP=0x0;  Address(0x51[7:6])
SPIWrite 0052,00    //ESR_1P2_REF_MISCTOP=0x0;  Address(0x52[7:1])
SPIWrite 0065,40    //ESR_1P2_ANA_PLLTOP=0x0;   Address(0x65[7:4])
SPIWrite 0084,10    //CTL_LDOVCO_VREF=0x1;  Address(0x84[7:4])
SPIWrite 0084,90    //CTL_LDOVCO_FBRES=0x2;     Address(0x84[7:6])
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SPIWrite 0069,47    //LOCK_DETECT_DELTA2_PROG=0x47;     Address(0x69[7:0],0x6a[7:0])
SPIWrite 0045,20    //CTL_VREF_CAL_EXT2INT=0x1;     Address(0x45[7:5])
SPIWrite 0032,00    //CTL_VCO_300U=0x0;     Address(0x32[7:2])
SPIWrite 0049,38    //CTL_VCO_IB_VAR_SLOPE=0x7;     Address(0x49[7:3])
SPIWrite 0049,3d    //CTL_VCO_IB_VAR=0x5;   Address(0x49[7:0])
SPIWrite 004a,00    //CTL_VCO_IB_GM_SLOPE=0x0;  Address(0x4a[7:3])
SPIWrite 004b,00    //CTL_VCO_IB_TAIL_SLOPE=0x0;    Address(0x4b[7:4])
SPIWrite 004d,c0    //CTL_VCO_VAR_BIAS=0x0;     Address(0x4d[7:0])
SPIWrite 004a,04    //CTL_VCO_IB_GM=0x4;    Address(0x4a[7:0])
SPIWrite 004b,0f    //CTL_VCO_IB_TAIL=0xf;  Address(0x4b[7:0])
SPIWrite 004b,3f    //CTL_VCO_IB_TAIL_SLOPE=0x3;    Address(0x4b[7:4])
SPIWrite 0051,2f    //CTL_VCO_IB_TAIL_SLOPE_SIGN=0x1;   Address(0x51[7:0])
SPIWrite 0040,40    //CTL_CP_CURR=0x2;  Address(0x40[7:5])
SPIWrite 0041,00    //CTL_CP_BIAS=0x0;  Address(0x41[7:1])
SPIWrite 0043,f8    //CTL_LPF_R=0x7;    Address(0x43[7:5])
SPIWrite 0075,08    //CAL_BYPASS=0x1;   Address(0x75[7:3])
SPIWrite 0075,0e    //VCO_SEL_IN=0x6;   Address(0x75[7:0])
SPIWrite 0045,24    //CTL_VREF_CAL_SLOPE=0x4;   Address(0x45[7:0])
SPIWrite 0031,40    //CTL_LPF_50U_0=0x1;    Address(0x31[7:6])
SPIWrite 0046,63    //CTL_VCTRL_ADC_VL_LVL=0x3;     Address(0x46[7:0])
SPIWrite 0045,24    //CTL_VCTRL_ADC_VH_LVL=0x0;     Address(0x45[7:6])
SPIWrite 0064,07    //M_IN_PROG=0x7;    Address(0x64[7:0])
SPIWrite 0073,20    //EN_SYNC_SYSREF_BUFF=0x1;  Address(0x73[7:5])
SPIWrite 0056,f1    //EN_SYNC_SYSREF_OUT_MUX=0x0;   Address(0x56[7:1])
SPIWrite 0058,00    //CTL_SYNC_LCMDIV_SYSREF_PULSE=0x0;     Address(0x58[7:2])
SPIWrite 0062,00    //NO_OF_SYSREFS_REFDIV=0x0;     Address(0x62[7:4])
SPIWrite 0066,00    //EN_CAL=0x0;   Address(0x66[7:0])
SPIWrite 0066,01    //EN_CAL=0x1;   Address(0x66[7:0])

WAIT 0.005
SPIWrite 0066,03    //EN_LOCK_DETECT=0x1;   Address(0x66[7:1])

WAIT 0.005
SPIWrite 0063,41    //CLR_FLAG_LOCK_LOST=0x1;   Address(0x63[7:6])
SPIWrite 0063,01    //CLR_FLAG_LOCK_LOST=0x0;   Address(0x63[7:6])

WAIT 0.005
SPIRead 0066

//Read  LOCK_OUT_STICKY=0x1;    Address(0x66[7:5])

SPIRead 0066

//Read  LOCK_LOST_STICKY=0x0;   Address(0x66[7:6])

SPIRead 0066

//Read  LOCK=0x1;   Address(0x66[7:4])

SPIRead 0066

//Read  LOCK_LOST_STICKY=0x0;   Address(0x66[7:6])

SPIWrite 0066,31    //EN_LOCK_DETECT=0x0;   Address(0x66[7:1])
SPIWrite 0063,81    //CLR_FLAG_LOCK_OUT=0x1;    Address(0x63[7:7])
SPIWrite 0063,c1    //CLR_FLAG_LOCK_LOST=0x1;   Address(0x63[7:6])
SPIWrite 0063,c2    //NO_OF_SYSREFS_OUTDIV=0x2;     Address(0x63[7:0])

//START: Sending Sysref to device

SPIWrite 0015,00    //pll=0x0;  Address(0x15[7:0])
SPIWrite 0015,80    //timing_controller=0x1;    Address(0x15[7:7])
SPIWrite 085b,00    //spare_reg_port=0x0;
Address(0x858[7:0],0x859[7:0],0x85a[7:0],0x85b[7:0],0x85c[7:0])
SPIWrite 085a,00
SPIWrite 0859,00
SPIWrite 0858,00
SPIWrite 085b,00    //spare_reg_port=0x101;
Address(0x858[7:0],0x859[7:0],0x85a[7:0],0x85b[7:0],0x85c[7:0])
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SPIWrite 085a,00
SPIWrite 0859,01
SPIWrite 0858,01
SPIWrite 085b,00    //spare_reg_port=0x0;
Address(0x858[7:0],0x859[7:0],0x85a[7:0],0x85b[7:0],0x85c[7:0])
SPIWrite 085a,00
SPIWrite 0859,00
SPIWrite 0858,00
SPIWrite 0015,00    //timing_controller=0x0;    Address(0x15[7:7])
SPIWrite 0015,01    //pll=0x1;  Address(0x15[7:0])
SPIWrite 006a,00    //LCMGEN_SYNC_ENA=0x0;  Address(0x6a[7:1])
SPIWrite 006e,00    //LCMGEN_USE_SPI_SYSREF=0x0;    Address(0x6e[7:0])
SPIWrite 006a,00    //LCMGEN_SYNC_ENA=0x0;  Address(0x6a[7:1])
SPIWrite 006a,02    //LCMGEN_SYNC_ENA=0x1;  Address(0x6a[7:1])
SPIWrite 0015,00    //pll=0x0;  Address(0x15[7:0])

//STEP: pllConfig/step1

//External-Action: Give Sysref Here.


WAIT 0.001

//END: Sending Sysref to device

SPIWrite 0015,01    //pll=0x1;  Address(0x15[7:0])
SPIWrite 0063,c0    //NO_OF_SYSREFS_OUTDIV=0x0;     Address(0x63[7:0])
SPIWrite 0015,00    //pll=0x0;  Address(0x15[7:0])
SPIWrite 0015,02    //ana_4t4r=0x1;     Address(0x15[7:1])
SPIWrite 00c1,00    //DIS_DIGCLK=0x0;   Address(0xc1[7:5])
SPIWrite 0015,00    //ana_4t4r=0x0;     Address(0x15[7:1])
SPIWrite 0015,01    //pll=0x1;  Address(0x15[7:0])
SPIWrite 0063,40    //CLR_FLAG_LOCK_OUT=0x0;    Address(0x63[7:7])
SPIWrite 0063,00    //CLR_FLAG_LOCK_LOST=0x0;   Address(0x63[7:6])
SPIWrite 0066,33    //EN_LOCK_DETECT=0x1;   Address(0x66[7:1])

//START: Requesting/releasing SPI Access to PLL Pages

SPIWrite 0015,00    //pll=0x0;  Address(0x15[7:0])
SPIWrite 0015,40    //digtop=0x1;   Address(0x15[7:6])
SPIWrite 0170,00    //pll_reg_spi_req_a=0x0;    Address(0x170[7:0])
SPIWrite 0540,00    //pll_reg_spi_req_b1=0x0;   Address(0x540[7:0])

WAIT 0.2

//END: Requesting/releasing SPI Access to PLL Pages

SPIWrite 0015,00    //digtop=0x0;   Address(0x15[7:6])
SPIWrite 0015,80    //timing_controller=0x1;    Address(0x15[7:7])
SPIWrite 010d,03    //config_rise_xx_A_4=0x31f;
Address(0x10c[7:0],0x10d[7:0],0x10e[7:0])
SPIWrite 010c,1f
SPIWrite 01ad,03    //config_rise_xx_A_4=0x31f;
Address(0x1ac[7:0],0x1ad[7:0],0x1ae[7:0])
SPIWrite 01ac,1f
SPIWrite 024d,03    //config_rise_xx_A_4=0x31f;
Address(0x24c[7:0],0x24d[7:0],0x24e[7:0])
SPIWrite 024c,1f
SPIWrite 02ed,03    //config_rise_xx_A_4=0x31f;
Address(0x2ec[7:0],0x2ed[7:0],0x2ee[7:0])
SPIWrite 02ec,1f
SPIWrite 0421,01    //config_rise_xx_A_41=0x190;
Address(0x420[7:0],0x421[7:0],0x422[7:0])
SPIWrite 0420,90
SPIWrite 04d9,01    //config_rise_xx_A_41=0x190;
Address(0x4d8[7:0],0x4d9[7:0],0x4da[7:0])
SPIWrite 04d8,90
SPIWrite 0591,01    //config_rise_xx_A_41=0x190;
Address(0x590[7:0],0x591[7:0],0x592[7:0])
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SPIWrite 0590,90
SPIWrite 0649,01    //config_rise_xx_A_41=0x190;
Address(0x648[7:0],0x649[7:0],0x64a[7:0])
SPIWrite 0648,90
SPIWrite 0701,01    //config_rise_xx_A_41=0x190;
Address(0x700[7:0],0x701[7:0],0x702[7:0])
SPIWrite 0700,90
SPIWrite 07b9,01    //config_rise_xx_A_41=0x190;
Address(0x7b8[7:0],0x7b9[7:0],0x7ba[7:0])
SPIWrite 07b8,90

//END: Configuring PLL

SPIWrite 0015,00    //timing_controller=0x0;    Address(0x15[7:7])

//STEP: pllConfig/step2
SPIWrite 0018,40    //cm4_internal=0x1;     Address(0x18[7:6])
SPIWrite 0086,01    //cfg_dithered_mode_en=0x1;     Address(0x86[7:0])
SPIWrite 0082,10    //cfg_divide_factor=0x10;   Address(0x82[7:0])
SPIWrite 0083,01    //cfg_divide_factor_odd=0x1;    Address(0x83[7:0])
SPIWrite 0084,00    //cfg_divide_factor_load_enable=0x0;    Address(0x84[7:0])
SPIWrite 0084,01    //cfg_divide_factor_load_enable=0x1;    Address(0x84[7:0])
SPIWrite 0084,00    //cfg_divide_factor_load_enable=0x0;    Address(0x84[7:0])
SPIWrite 0018,00    //cm4_internal=0x0;     Address(0x18[7:6])
SPIWrite 0018,20    //macro=0x1;    Address(0x18[7:5])
SPIRead 00f0

//Read  MACRO_READY=0x1;    Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 0193,12    //MACRO_OPCODE=0x12;    Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0

//Read  MACRO_DONE=0x1;     Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIRead 00f0

//Read  MACRO_ERROR=0x0;    Address(0xf0[7:3])

SPIRead 00f1

//Read  MACRO_ERROR_OPCODE=0x0;     Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0

//Read  MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0

//Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;     Address(0xf0[7:5])

SPIRead 00f0

//Read  MACRO_ERROR_IN_OPERAND=0x0;     Address(0xf0[7:6])

SPIRead 00f0

//Read  MACRO_ERROR_IN_EXECUTION=0x0;   Address(0xf0[7:7])

SPIRead 00f3
SPIRead 00f2

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7746   //Read  MACRO_ERROR_EXTENDED_CODE=0x0;  Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
7747
7748   SPIRead 00f7
7749   SPIRead 00f6
7750   SPIRead 00f5
7751   SPIRead 00f4
7752
7753   //Read  MACRO_ERROR_EXTENDED_CODE_2=0x0;
       Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
7754
7755   SPIWrite 0018,00    //macro=0x0;    Address(0x18[7:5])
7756
7757   //STEP: serdesConfig/step0
7758
7759   //START: Enabling access to SERDES
7760
7761   SPIWrite 0016,10    //jesd_subchip=0x1;     Address(0x16[7:4])
7762   SPIWrite 00c0,02    //apb_clk_disable=0x0;  Address(0xc0[7:0])
7763   SPIWrite 00c0,00    //apb_clk_dithered_mode_en=0x0;     Address(0xc0[7:1])
7764   SPIWrite 00c4,01    //apb_clk_from_cm4_clk_en=0x1;  Address(0xc4[7:0])
7765   SPIWrite 0020,12    //serdesab_apb_page_addr_index=0x2;     Address(0x20[7:0])
7766   SPIWrite 0021,12    //serdescd_apb_page_addr_index=0x2;     Address(0x21[7:0])
7767   SPIWrite 0020,12    //serdesab_apb_mode_16b=0x1;    Address(0x20[7:4])
7768   SPIWrite 0021,12    //serdescd_apb_mode_16b=0x1;    Address(0x21[7:4])
7769   SPIWrite 0020,12    //serdesab_apb_pin_intf_en=0x0;     Address(0x20[7:2])
7770   SPIWrite 0021,12    //serdescd_apb_pin_intf_en=0x0;     Address(0x21[7:2])
7771   SPIWrite 00c0,40    //apb_clk_sysref_sel=0x1;   Address(0xc0[7:6])
7772   SPIWrite 00c0,40    //apb_clk_sysref_val=0x0;   Address(0xc0[7:7])
7773   SPIWrite 00c0,c0    //apb_clk_sysref_val=0x1;   Address(0xc0[7:7])
7774   SPIWrite 00c0,40    //apb_clk_sysref_val=0x0;   Address(0xc0[7:7])
7775   SPIWrite 0016,00    //jesd_subchip=0x0;     Address(0x16[7:4])
7776   SPIWrite 0016,20    //serdes_jesd=0x1;  Address(0x16[7:5])
7777   SPIWrite 7007,00    //BUS_WIDTH_LANE3=0x0;  Address(0x9803[7:3])
7778   SPIWrite 7006,00
7779   SPIWrite 7007,00    //BUS_WIDTH_LANE2=0x0;  Address(0x9803[7:2])
7780   SPIWrite 7006,00
7781   SPIWrite 7007,00    //BUS_WIDTH_LANE1=0x0;  Address(0x9803[7:1])
7782   SPIWrite 7006,00
7783   SPIWrite 7007,00    //BUS_WIDTH_LANE0=0x0;  Address(0x9803[7:0])
7784   SPIWrite 7006,00
7785   SPIWrite 0016,40    //serdes_jesd=0x2;  Address(0x16[7:5])
7786   SPIWrite 7007,00    //BUS_WIDTH_LANE3=0x0;  Address(0x9803[7:3])
7787   SPIWrite 7006,00
7788   SPIWrite 7007,00    //BUS_WIDTH_LANE2=0x0;  Address(0x9803[7:2])
7789   SPIWrite 7006,00
7790   SPIWrite 7007,00    //BUS_WIDTH_LANE1=0x0;  Address(0x9803[7:1])
7791   SPIWrite 7006,00
7792   SPIWrite 7007,00    //BUS_WIDTH_LANE0=0x0;  Address(0x9803[7:0])
7793   SPIWrite 7006,00
7794
7795   //END: Done enabling access to SERDES
7796
7797
7798   //START: Setting Serdes Reference Clock Divs
7799
7800   SPIWrite 0016,00    //serdes_jesd=0x0;  Address(0x16[7:5])
7801   SPIWrite 0015,02    //ana_4t4r=0x1;     Address(0x15[7:1])
7802   SPIWrite 0107,00    //po_common_digtop_spare_0=0x801;
       Address(0x104[7:0],0x105[7:0],0x106[7:0],0x107[7:0],0x108[7:0])
7803   SPIWrite 0106,00
7804   SPIWrite 0105,08
7805   SPIWrite 0104,01
7806
7807   //END: Setting Serdes Reference Clock Divs
7808
7809   SPIWrite 0015,00    //ana_4t4r=0x0;     Address(0x15[7:1])
7810
7811   //STEP: serdesConfig/step1
7812
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7813  //START: Resetting Serdes
7814
7815  SPIWrite 0016,20    //serdes_jesd=0x1;  Address(0x16[7:5])
7816  SPIWrite 701b,08    //DOMAIN_RESET=0x888;   Address(0x980d[3:0],0x980e[7:0])
7817  SPIWrite 701a,88
7818  SPIWrite 701b,00    //DOMAIN_RESET=0x0;     Address(0x980d[3:0],0x980e[7:0])
7819  SPIWrite 701a,00
7820
7821  WAIT 0.1
7822  SPIWrite 701b,07    //DOMAIN_RESET=0x777;   Address(0x980d[3:0],0x980e[7:0])
7823  SPIWrite 701a,77
7824  SPIWrite 701b,00    //DOMAIN_RESET=0x0;     Address(0x980d[3:0],0x980e[7:0])
7825  SPIWrite 701a,00
7826
7827  WAIT 0.1
7828
7829  //END: Done resetting Serdes
7830
7831
7832  //START: Resetting Serdes
7833
7834  SPIWrite 0016,40    //serdes_jesd=0x2;  Address(0x16[7:5])
7835  SPIWrite 701b,08    //DOMAIN_RESET=0x888;   Address(0x980d[3:0],0x980e[7:0])
7836  SPIWrite 701a,88
7837  SPIWrite 701b,00    //DOMAIN_RESET=0x0;     Address(0x980d[3:0],0x980e[7:0])
7838  SPIWrite 701a,00
7839
7840  WAIT 0.1
7841  SPIWrite 701b,07    //DOMAIN_RESET=0x777;   Address(0x980d[3:0],0x980e[7:0])
7842  SPIWrite 701a,77
7843  SPIWrite 701b,00    //DOMAIN_RESET=0x0;     Address(0x980d[3:0],0x980e[7:0])
7844  SPIWrite 701a,00
7845
7846  WAIT 0.1
7847
7848  //END: Done resetting Serdes
7849
7850  SPIWrite 0016,00    //serdes_jesd=0x0;  Address(0x16[7:5])
7851
7852  //STEP: serdesConfig/step2
7853
7854  //START: Configuring the SERDES
7855
7856  SPIWrite 0016,10    //jesd_subchip=0x1;     Address(0x16[7:4])
7857  SPIWrite 00c1,02    //apb_clk_div_factor=0x2;   Address(0xc1[7:0])
7858  SPIWrite 00c0,40    //apb_clk_disable=0x0;  Address(0xc0[7:0])
7859  SPIWrite 0020,12    //serdesab_apb_page_addr_index=0x2;     Address(0x20[7:0])
7860  SPIWrite 0021,12    //serdescd_apb_page_addr_index=0x2;     Address(0x21[7:0])
7861  SPIWrite 0016,00    //jesd_subchip=0x0;     Address(0x16[7:4])
7862  SPIWrite 0016,60    //serdes_jesd=0x3;  Address(0x16[7:5])
7863  SPIWrite 7029,ff
7864  SPIWrite 7028,f0
7865  SPIWrite 701b,0a
7866  SPIWrite 701a,aa
7867  SPIWrite 701b,00
7868  SPIWrite 701a,00
7869  SPIWrite 7007,00
7870  SPIWrite 7006,00
7871  SPIWrite 0016,20    //serdes_jesd=0x1;  Address(0x16[7:5])
7872  SPIWrite 49f1,92
7873  SPIWrite 49f0,40
7874  SPIWrite 49f3,ea
7875  SPIWrite 49f2,80
7876  SPIWrite 49e3,f0
7877  SPIWrite 49e2,00
7878  SPIWrite 49b5,47
7879  SPIWrite 49b4,47
7880  SPIWrite 49ff,fd
7881  SPIWrite 49fe,b0
```

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  SPIWrite 49ed,1d
  SPIWrite 49ec,c0
  SPIWrite 49e7,52
  SPIWrite 49e6,26
  SPIWrite 49e5,6e
  SPIWrite 49e4,b6
  SPIWrite 49df,a8
  SPIWrite 49de,28
  SPIWrite 49eb,63
  SPIWrite 49ea,98
  SPIWrite 49e9,b2
  SPIWrite 49e8,44
  SPIWrite 49fd,63
  SPIWrite 49fc,98
  SPIWrite 49fb,b2
  SPIWrite 49fa,48
  SPIWrite 49f9,4a
  SPIWrite 49f8,44
  SPIWrite 49f7,79
  SPIWrite 49f6,b6
  SPIWrite 49d9,6c
  SPIWrite 49d8,06
  SPIWrite 4201,10
  SPIWrite 4200,6b
  SPIWrite 4203,64
  SPIWrite 4202,80
  SPIWrite 4205,62
  SPIWrite 4204,00
  SPIWrite 4207,7b
  SPIWrite 4206,33
  SPIWrite 4209,70
  SPIWrite 4208,0a
  SPIWrite 420b,bd
  SPIWrite 420a,68
  SPIWrite 420d,76
  SPIWrite 420c,2d
  SPIWrite 420f,66
  SPIWrite 420e,ab
  SPIWrite 4211,d0
  SPIWrite 4210,08
  SPIWrite 4213,00
  SPIWrite 4212,18
  SPIWrite 4215,66
  SPIWrite 4214,2c
  SPIWrite 4217,3d
  SPIWrite 4216,15
  SPIWrite 4219,00
  SPIWrite 4218,80
  SPIWrite 421b,00
  SPIWrite 421a,02
  SPIWrite 421d,34
  SPIWrite 421c,00
  SPIWrite 421f,00
  SPIWrite 421e,00
  SPIWrite 4221,10
  SPIWrite 4220,1a
  SPIWrite 4239,03
  SPIWrite 4238,40
  SPIWrite 423b,00
  SPIWrite 423a,60
  SPIWrite 423d,00
  SPIWrite 423c,00
  SPIWrite 423f,00
  SPIWrite 423e,80
  SPIWrite 4277,00
  SPIWrite 4276,00
  SPIWrite 4279,00
  SPIWrite 4278,00
  SPIWrite 427b,00
```

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SPIWrite 427a,00
SPIWrite 427d,00
SPIWrite 427c,00
SPIWrite 4283,9f
SPIWrite 4282,df
SPIWrite 4285,b3
SPIWrite 4284,c0
SPIWrite 428f,24
SPIWrite 428e,a2
SPIWrite 4291,cc
SPIWrite 4290,34
SPIWrite 4293,e3
SPIWrite 4292,d7
SPIWrite 4295,74
SPIWrite 4294,60
SPIWrite 4297,06
SPIWrite 4296,db
SPIWrite 4341,03
SPIWrite 4340,01
SPIWrite 43e7,00
SPIWrite 43e6,80
SPIWrite 43e9,fc
SPIWrite 43e8,00
SPIWrite 43eb,9f
SPIWrite 43ea,fe
SPIWrite 43ed,00
SPIWrite 43ec,60
SPIWrite 43ef,10
SPIWrite 43ee,00
SPIWrite 43f1,68
SPIWrite 43f0,64
SPIWrite 43f3,92
SPIWrite 43f2,30
SPIWrite 43f5,00
SPIWrite 43f4,00
SPIWrite 43f7,6d
SPIWrite 43f6,87
SPIWrite 43f9,db
SPIWrite 43f8,6c
SPIWrite 43fb,42
SPIWrite 43fa,6e
SPIWrite 43fd,62
SPIWrite 43fc,7c
SPIWrite 43ff,88
SPIWrite 43fe,c8
SPIWrite 4001,10
SPIWrite 4000,6b
SPIWrite 4003,64
SPIWrite 4002,80
SPIWrite 4005,62
SPIWrite 4004,00
SPIWrite 4007,7b
SPIWrite 4006,33
SPIWrite 4009,70
SPIWrite 4008,0a
SPIWrite 400b,bd
SPIWrite 400a,68
SPIWrite 400d,76
SPIWrite 400c,2d
SPIWrite 400f,66
SPIWrite 400e,ab
SPIWrite 4011,d0
SPIWrite 4010,08
SPIWrite 4013,00
SPIWrite 4012,18
SPIWrite 4015,66
SPIWrite 4014,2c
SPIWrite 4017,3d
SPIWrite 4016,15
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  SPIWrite 4019,00
  SPIWrite 4018,80
  SPIWrite 401b,00
  SPIWrite 401a,02
  SPIWrite 401d,34
  SPIWrite 401c,00
  SPIWrite 401f,00
  SPIWrite 401e,00
  SPIWrite 4021,10
  SPIWrite 4020,1a
  SPIWrite 4039,03
  SPIWrite 4038,40
  SPIWrite 403b,00
  SPIWrite 403a,60
  SPIWrite 403d,00
  SPIWrite 403c,00
  SPIWrite 403f,00
  SPIWrite 403e,80
  SPIWrite 4077,00
  SPIWrite 4076,00
  SPIWrite 4079,00
  SPIWrite 4078,00
  SPIWrite 407b,00
  SPIWrite 407a,00
  SPIWrite 407d,00
  SPIWrite 407c,00
  SPIWrite 4083,9f
  SPIWrite 4082,df
  SPIWrite 4085,b3
  SPIWrite 4084,c0
  SPIWrite 408f,24
  SPIWrite 408e,a2
  SPIWrite 4091,cc
  SPIWrite 4090,34
  SPIWrite 4093,e3
  SPIWrite 4092,d7
  SPIWrite 4095,74
  SPIWrite 4094,60
  SPIWrite 4097,06
  SPIWrite 4096,db
  SPIWrite 4141,03
  SPIWrite 4140,01
  SPIWrite 41e7,00
  SPIWrite 41e6,80
  SPIWrite 41e9,fc
  SPIWrite 41e8,00
  SPIWrite 41eb,9f
  SPIWrite 41ea,fe
  SPIWrite 41ed,00
  SPIWrite 41ec,00
  SPIWrite 41ef,10
  SPIWrite 41ee,00
  SPIWrite 41f1,68
  SPIWrite 41f0,64
  SPIWrite 41f3,92
  SPIWrite 41f2,30
  SPIWrite 41f5,00
  SPIWrite 41f4,00
  SPIWrite 41f7,6d
  SPIWrite 41f6,87
  SPIWrite 41f9,db
  SPIWrite 41f8,6c
  SPIWrite 41fb,42
  SPIWrite 41fa,6e
  SPIWrite 41fd,62
  SPIWrite 41fc,7c
  SPIWrite 41ff,88
  SPIWrite 41fe,c8
  SPIWrite 4401,10
```

```
  SPIWrite 4400,6b
  SPIWrite 4403,64
  SPIWrite 4402,80
  SPIWrite 4405,62
  SPIWrite 4404,00
  SPIWrite 4407,7b
  SPIWrite 4406,33
  SPIWrite 4409,70
  SPIWrite 4408,0a
  SPIWrite 440b,bd
  SPIWrite 440a,68
  SPIWrite 440d,76
  SPIWrite 440c,2d
  SPIWrite 440f,66
  SPIWrite 440e,ab
  SPIWrite 4411,d0
  SPIWrite 4410,08
  SPIWrite 4413,00
  SPIWrite 4412,18
  SPIWrite 4415,66
  SPIWrite 4414,2c
  SPIWrite 4417,3d
  SPIWrite 4416,15
  SPIWrite 4419,00
  SPIWrite 4418,80
  SPIWrite 441b,00
  SPIWrite 441a,02
  SPIWrite 441d,34
  SPIWrite 441c,00
  SPIWrite 441f,00
  SPIWrite 441e,00
  SPIWrite 4421,10
  SPIWrite 4420,1a
  SPIWrite 4439,03
  SPIWrite 4438,40
  SPIWrite 443b,00
  SPIWrite 443a,60
  SPIWrite 443d,00
  SPIWrite 443c,00
  SPIWrite 443f,00
  SPIWrite 443e,80
  SPIWrite 4477,00
  SPIWrite 4476,00
  SPIWrite 4479,00
  SPIWrite 4478,00
  SPIWrite 447b,00
  SPIWrite 447a,00
  SPIWrite 447d,00
  SPIWrite 447c,00
  SPIWrite 4483,9f
  SPIWrite 4482,df
  SPIWrite 4485,b3
  SPIWrite 4484,c0
  SPIWrite 448f,24
  SPIWrite 448e,a2
  SPIWrite 4491,cc
  SPIWrite 4490,34
  SPIWrite 4493,e3
  SPIWrite 4492,d7
  SPIWrite 4495,74
  SPIWrite 4494,60
  SPIWrite 4497,06
  SPIWrite 4496,db
  SPIWrite 4541,03
  SPIWrite 4540,01
  SPIWrite 45e7,00
  SPIWrite 45e6,80
  SPIWrite 45e9,fc
  SPIWrite 45e8,00
```

```
SPIWrite 45eb,9f
SPIWrite 45ea,fe
SPIWrite 45ed,00
SPIWrite 45ec,00
SPIWrite 45ef,10
SPIWrite 45ee,00
SPIWrite 45f1,68
SPIWrite 45f0,64
SPIWrite 45f3,92
SPIWrite 45f2,30
SPIWrite 45f5,00
SPIWrite 45f4,00
SPIWrite 45f7,6d
SPIWrite 45f6,87
SPIWrite 45f9,db
SPIWrite 45f8,6c
SPIWrite 45fb,42
SPIWrite 45fa,6e
SPIWrite 45fd,62
SPIWrite 45fc,7c
SPIWrite 45ff,88
SPIWrite 45fe,c8
SPIWrite 4601,10
SPIWrite 4600,6b
SPIWrite 4603,64
SPIWrite 4602,80
SPIWrite 4605,62
SPIWrite 4604,00
SPIWrite 4607,7b
SPIWrite 4606,33
SPIWrite 4609,70
SPIWrite 4608,0a
SPIWrite 460b,bd
SPIWrite 460a,68
SPIWrite 460d,76
SPIWrite 460c,2d
SPIWrite 460f,66
SPIWrite 460e,ab
SPIWrite 4611,d0
SPIWrite 4610,08
SPIWrite 4613,00
SPIWrite 4612,18
SPIWrite 4615,66
SPIWrite 4614,2c
SPIWrite 4617,3d
SPIWrite 4616,15
SPIWrite 4619,00
SPIWrite 4618,80
SPIWrite 461b,00
SPIWrite 461a,02
SPIWrite 461d,34
SPIWrite 461c,00
SPIWrite 461f,00
SPIWrite 461e,00
SPIWrite 4621,10
SPIWrite 4620,1a
SPIWrite 4639,03
SPIWrite 4638,40
SPIWrite 463b,00
SPIWrite 463a,60
SPIWrite 463d,00
SPIWrite 463c,00
SPIWrite 463f,00
SPIWrite 463e,80
SPIWrite 4677,00
SPIWrite 4676,00
SPIWrite 4679,00
SPIWrite 4678,00
SPIWrite 467b,00
```

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SPIWrite 467a,00
SPIWrite 467d,00
SPIWrite 467c,00
SPIWrite 4683,9f
SPIWrite 4682,df
SPIWrite 4685,b3
SPIWrite 4684,c0
SPIWrite 468f,24
SPIWrite 468e,a2
SPIWrite 4691,cc
SPIWrite 4690,34
SPIWrite 4693,e3
SPIWrite 4692,d7
SPIWrite 4695,74
SPIWrite 4694,60
SPIWrite 4697,06
SPIWrite 4696,db
SPIWrite 4741,03
SPIWrite 4740,01
SPIWrite 47e7,00
SPIWrite 47e6,80
SPIWrite 47e9,fc
SPIWrite 47e8,00
SPIWrite 47eb,9f
SPIWrite 47ea,fe
SPIWrite 47ed,00
SPIWrite 47ec,00
SPIWrite 47ef,10
SPIWrite 47ee,00
SPIWrite 47f1,68
SPIWrite 47f0,64
SPIWrite 47f3,92
SPIWrite 47f2,30
SPIWrite 47f5,00
SPIWrite 47f4,00
SPIWrite 47f7,6d
SPIWrite 47f6,87
SPIWrite 47f9,db
SPIWrite 47f8,6c
SPIWrite 47fb,42
SPIWrite 47fa,6e
SPIWrite 47fd,62
SPIWrite 47fc,7c
SPIWrite 47ff,88
SPIWrite 47fe,c8
SPIWrite 0016,40    //serdes_jesd=0x2;  Address(0x16[7:5])
SPIWrite 49f1,82
SPIWrite 49f0,40
SPIWrite 49f3,e2
SPIWrite 49f2,80
SPIWrite 49e3,b0
SPIWrite 49e2,00
SPIWrite 49b5,47
SPIWrite 49b4,47
SPIWrite 49ff,ed
SPIWrite 49fe,b0
SPIWrite 49ed,0d
SPIWrite 49ec,c0
SPIWrite 49e7,52
SPIWrite 49e6,26
SPIWrite 49e5,6e
SPIWrite 49e4,b6
SPIWrite 49df,a8
SPIWrite 49de,28
SPIWrite 49eb,63
SPIWrite 49ea,18
SPIWrite 49e9,b2
SPIWrite 49e8,44
SPIWrite 49fd,63
```

```
  SPIWrite 49fc,18
  SPIWrite 49fb,b2
  SPIWrite 49fa,48
  SPIWrite 49f9,4a
  SPIWrite 49f8,44
  SPIWrite 49f7,79
  SPIWrite 49f6,b6
  SPIWrite 49d9,6c
  SPIWrite 49d8,06
  SPIWrite 4601,10
  SPIWrite 4600,6b
  SPIWrite 4603,64
  SPIWrite 4602,80
  SPIWrite 4605,62
  SPIWrite 4604,00
  SPIWrite 4607,7b
  SPIWrite 4606,33
  SPIWrite 4609,70
  SPIWrite 4608,0a
  SPIWrite 460b,bd
  SPIWrite 460a,68
  SPIWrite 460d,76
  SPIWrite 460c,2d
  SPIWrite 460f,66
  SPIWrite 460e,ab
  SPIWrite 4611,d0
  SPIWrite 4610,08
  SPIWrite 4613,00
  SPIWrite 4612,18
  SPIWrite 4615,66
  SPIWrite 4614,2c
  SPIWrite 4617,3d
  SPIWrite 4616,15
  SPIWrite 4619,00
  SPIWrite 4618,80
  SPIWrite 461b,00
  SPIWrite 461a,02
  SPIWrite 461d,34
  SPIWrite 461c,00
  SPIWrite 461f,00
  SPIWrite 461e,00
  SPIWrite 4621,10
  SPIWrite 4620,1a
  SPIWrite 4639,03
  SPIWrite 4638,40
  SPIWrite 463b,00
  SPIWrite 463a,60
  SPIWrite 463d,00
  SPIWrite 463c,00
  SPIWrite 463f,00
  SPIWrite 463e,80
  SPIWrite 4677,00
  SPIWrite 4676,00
  SPIWrite 4679,00
  SPIWrite 4678,00
  SPIWrite 467b,00
  SPIWrite 467a,00
  SPIWrite 467d,00
  SPIWrite 467c,00
  SPIWrite 4683,9f
  SPIWrite 4682,df
  SPIWrite 4685,b3
  SPIWrite 4684,c0
  SPIWrite 468f,24
  SPIWrite 468e,a2
  SPIWrite 4691,cc
  SPIWrite 4690,34
  SPIWrite 4693,e3
  SPIWrite 4692,d7
```

```
  SPIWrite 4695,74
  SPIWrite 4694,60
  SPIWrite 4697,06
  SPIWrite 4696,db
  SPIWrite 4741,03
  SPIWrite 4740,01
  SPIWrite 47e7,00
  SPIWrite 47e6,80
  SPIWrite 47e9,fc
  SPIWrite 47e8,00
  SPIWrite 47eb,1f
  SPIWrite 47ea,fe
  SPIWrite 47ed,00
  SPIWrite 47ec,00
  SPIWrite 47ef,10
  SPIWrite 47ee,00
  SPIWrite 47f1,68
  SPIWrite 47f0,64
  SPIWrite 47f3,92
  SPIWrite 47f2,30
  SPIWrite 47f5,00
  SPIWrite 47f4,00
  SPIWrite 47f7,6d
  SPIWrite 47f6,83
  SPIWrite 47f9,db
  SPIWrite 47f8,6c
  SPIWrite 47fb,42
  SPIWrite 47fa,6e
  SPIWrite 47fd,62
  SPIWrite 47fc,78
  SPIWrite 47ff,08
  SPIWrite 47fe,c8
  SPIWrite 4401,10
  SPIWrite 4400,6b
  SPIWrite 4403,64
  SPIWrite 4402,80
  SPIWrite 4405,62
  SPIWrite 4404,00
  SPIWrite 4407,7b
  SPIWrite 4406,33
  SPIWrite 4409,70
  SPIWrite 4408,0a
  SPIWrite 440b,bd
  SPIWrite 440a,68
  SPIWrite 440d,76
  SPIWrite 440c,2d
  SPIWrite 440f,66
  SPIWrite 440e,ab
  SPIWrite 4411,d0
  SPIWrite 4410,08
  SPIWrite 4413,00
  SPIWrite 4412,18
  SPIWrite 4415,66
  SPIWrite 4414,2c
  SPIWrite 4417,3d
  SPIWrite 4416,15
  SPIWrite 4419,00
  SPIWrite 4418,80
  SPIWrite 441b,00
  SPIWrite 441a,02
  SPIWrite 441d,34
  SPIWrite 441c,00
  SPIWrite 441f,00
  SPIWrite 441e,00
  SPIWrite 4421,10
  SPIWrite 4420,1a
  SPIWrite 4439,03
  SPIWrite 4438,40
  SPIWrite 443b,00
```

```
8434   SPIWrite 443a,60
8435   SPIWrite 443d,00
8436   SPIWrite 443c,00
8437   SPIWrite 443f,00
8438   SPIWrite 443e,80
8439   SPIWrite 4477,00
8440   SPIWrite 4476,00
8441   SPIWrite 4479,00
8442   SPIWrite 4478,00
8443   SPIWrite 447b,00
8444   SPIWrite 447a,00
8445   SPIWrite 447d,00
8446   SPIWrite 447c,00
8447   SPIWrite 4483,9f
8448   SPIWrite 4482,df
8449   SPIWrite 4485,b3
8450   SPIWrite 4484,c0
8451   SPIWrite 448f,24
8452   SPIWrite 448e,a2
8453   SPIWrite 4491,cc
8454   SPIWrite 4490,34
8455   SPIWrite 4493,e3
8456   SPIWrite 4492,d7
8457   SPIWrite 4495,74
8458   SPIWrite 4494,60
8459   SPIWrite 4497,06
8460   SPIWrite 4496,db
8461   SPIWrite 4541,03
8462   SPIWrite 4540,01
8463   SPIWrite 45e7,00
8464   SPIWrite 45e6,80
8465   SPIWrite 45e9,fc
8466   SPIWrite 45e8,00
8467   SPIWrite 45eb,1f
8468   SPIWrite 45ea,fe
8469   SPIWrite 45ed,00
8470   SPIWrite 45ec,00
8471   SPIWrite 45ef,10
8472   SPIWrite 45ee,00
8473   SPIWrite 45f1,68
8474   SPIWrite 45f0,64
8475   SPIWrite 45f3,92
8476   SPIWrite 45f2,30
8477   SPIWrite 45f5,00
8478   SPIWrite 45f4,00
8479   SPIWrite 45f7,6d
8480   SPIWrite 45f6,83
8481   SPIWrite 45f9,db
8482   SPIWrite 45f8,6c
8483   SPIWrite 45fb,42
8484   SPIWrite 45fa,6e
8485   SPIWrite 45fd,62
8486   SPIWrite 45fc,78
8487   SPIWrite 45ff,08
8488   SPIWrite 45fe,c8
8489   SPIWrite 4001,10
8490   SPIWrite 4000,6b
8491   SPIWrite 4003,64
8492   SPIWrite 4002,80
8493   SPIWrite 4005,62
8494   SPIWrite 4004,00
8495   SPIWrite 4007,7b
8496   SPIWrite 4006,33
8497   SPIWrite 4009,70
8498   SPIWrite 4008,0a
8499   SPIWrite 400b,bd
8500   SPIWrite 400a,68
8501   SPIWrite 400d,76
8502   SPIWrite 400c,2d
```

```
  SPIWrite 400f,66
  SPIWrite 400e,ab
  SPIWrite 4011,d0
  SPIWrite 4010,08
  SPIWrite 4013,00
  SPIWrite 4012,18
  SPIWrite 4015,66
  SPIWrite 4014,2c
  SPIWrite 4017,3d
  SPIWrite 4016,15
  SPIWrite 4019,00
  SPIWrite 4018,80
  SPIWrite 401b,00
  SPIWrite 401a,02
  SPIWrite 401d,34
  SPIWrite 401c,00
  SPIWrite 401f,00
  SPIWrite 401e,00
  SPIWrite 4021,10
  SPIWrite 4020,1a
  SPIWrite 4039,03
  SPIWrite 4038,40
  SPIWrite 403b,00
  SPIWrite 403a,60
  SPIWrite 403d,00
  SPIWrite 403c,00
  SPIWrite 403f,00
  SPIWrite 403e,80
  SPIWrite 4077,00
  SPIWrite 4076,00
  SPIWrite 4079,00
  SPIWrite 4078,00
  SPIWrite 407b,00
  SPIWrite 407a,00
  SPIWrite 407d,00
  SPIWrite 407c,00
  SPIWrite 4083,9f
  SPIWrite 4082,df
  SPIWrite 4085,b3
  SPIWrite 4084,c0
  SPIWrite 408f,24
  SPIWrite 408e,a2
  SPIWrite 4091,cc
  SPIWrite 4090,34
  SPIWrite 4093,e3
  SPIWrite 4092,d7
  SPIWrite 4095,74
  SPIWrite 4094,60
  SPIWrite 4097,06
  SPIWrite 4096,db
  SPIWrite 4141,03
  SPIWrite 4140,01
  SPIWrite 41e7,00
  SPIWrite 41e6,80
  SPIWrite 41e9,fc
  SPIWrite 41e8,00
  SPIWrite 41eb,1f
  SPIWrite 41ea,fe
  SPIWrite 41ed,00
  SPIWrite 41ec,00
  SPIWrite 41ef,10
  SPIWrite 41ee,00
  SPIWrite 41f1,68
  SPIWrite 41f0,64
  SPIWrite 41f3,92
  SPIWrite 41f2,30
  SPIWrite 41f5,00
  SPIWrite 41f4,00
  SPIWrite 41f7,6d
```

```
  SPIWrite 41f6,83
  SPIWrite 41f9,db
  SPIWrite 41f8,6c
  SPIWrite 41fb,42
  SPIWrite 41fa,6e
  SPIWrite 41fd,62
  SPIWrite 41fc,78
  SPIWrite 41ff,08
  SPIWrite 41fe,c8
  SPIWrite 4201,10
  SPIWrite 4200,6b
  SPIWrite 4203,64
  SPIWrite 4202,80
  SPIWrite 4205,62
  SPIWrite 4204,00
  SPIWrite 4207,7b
  SPIWrite 4206,33
  SPIWrite 4209,70
  SPIWrite 4208,0a
  SPIWrite 420b,bd
  SPIWrite 420a,68
  SPIWrite 420d,76
  SPIWrite 420c,2d
  SPIWrite 420f,66
  SPIWrite 420e,ab
  SPIWrite 4211,d0
  SPIWrite 4210,08
  SPIWrite 4213,00
  SPIWrite 4212,18
  SPIWrite 4215,66
  SPIWrite 4214,2c
  SPIWrite 4217,3d
  SPIWrite 4216,15
  SPIWrite 4219,00
  SPIWrite 4218,80
  SPIWrite 421b,00
  SPIWrite 421a,02
  SPIWrite 421d,34
  SPIWrite 421c,00
  SPIWrite 421f,00
  SPIWrite 421e,00
  SPIWrite 4221,10
  SPIWrite 4220,1a
  SPIWrite 4239,03
  SPIWrite 4238,40
  SPIWrite 423b,00
  SPIWrite 423a,60
  SPIWrite 423d,00
  SPIWrite 423c,00
  SPIWrite 423f,00
  SPIWrite 423e,80
  SPIWrite 4277,00
  SPIWrite 4276,00
  SPIWrite 4279,00
  SPIWrite 4278,00
  SPIWrite 427b,00
  SPIWrite 427a,00
  SPIWrite 427d,00
  SPIWrite 427c,00
  SPIWrite 4283,9f
  SPIWrite 4282,df
  SPIWrite 4285,b3
  SPIWrite 4284,c0
  SPIWrite 428f,24
  SPIWrite 428e,a2
  SPIWrite 4291,cc
  SPIWrite 4290,34
  SPIWrite 4293,e3
  SPIWrite 4292,d7
```

```
SPIWrite 4295,74
SPIWrite 4294,60
SPIWrite 4297,06
SPIWrite 4296,db
SPIWrite 4341,03
SPIWrite 4340,01
SPIWrite 43e7,00
SPIWrite 43e6,80
SPIWrite 43e9,fc
SPIWrite 43e8,00
SPIWrite 43eb,1f
SPIWrite 43ea,fe
SPIWrite 43ed,00
SPIWrite 43ec,60
SPIWrite 43ef,10
SPIWrite 43ee,00
SPIWrite 43f1,68
SPIWrite 43f0,64
SPIWrite 43f3,92
SPIWrite 43f2,30
SPIWrite 43f5,00
SPIWrite 43f4,00
SPIWrite 43f7,6d
SPIWrite 43f6,83
SPIWrite 43f9,db
SPIWrite 43f8,6c
SPIWrite 43fb,42
SPIWrite 43fa,6e
SPIWrite 43fd,62
SPIWrite 43fc,78
SPIWrite 43ff,08
SPIWrite 43fe,c8
SPIWrite 0016,60    //serdes_jesd=0x3;  Address(0x16[7:5])
SPIWrite 7007,00    //BUS_WIDTH_LANE0=0x0;  Address(0x9803[7:0])
SPIWrite 7006,00
SPIWrite 7007,00    //BUS_WIDTH_LANE1=0x0;  Address(0x9803[7:1])
SPIWrite 7006,00
SPIWrite 7007,00    //BUS_WIDTH_LANE2=0x0;  Address(0x9803[7:2])
SPIWrite 7006,00
SPIWrite 7007,00    //BUS_WIDTH_LANE3=0x0;  Address(0x9803[7:3])
SPIWrite 7006,00
SPIWrite 0016,00    //serdes_jesd=0x0;  Address(0x16[7:5])

//END: Done configuring the SERDES


//STEP: serdesConfig/step3

//START: Loading Serdes Firmware.

SPIWrite 0018,20    //macro=0x1;    Address(0x18[7:5])
SPIRead 00f0

//Read  MACRO_READY=0x1;    Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00    //MACRO_OPERAND_REG0=0x10300;
Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,01
SPIWrite 00a1,03
SPIWrite 00a0,00
SPIWrite 0193,79    //MACRO_OPCODE=0x79;    Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0

//Read  MACRO_DONE=0x1;     Address(0xf0[7:2])
```

```
8709
8710
8711   SPIPoll 00f0,2,2,4
8712
8713   SPIRead 00f0
8714
8715   //Read  MACRO_ERROR=0x0;    Address(0xf0[7:3])
8716
8717   SPIRead 00f1
8718
8719   //Read  MACRO_ERROR_OPCODE=0x0;     Address(0xf1[7:0],0xf2[7:0])
8720
8721   SPIRead 00f0
8722
8723   //Read  MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])
8724
8725   SPIRead 00f0
8726
8727   //Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;     Address(0xf0[7:5])
8728
8729   SPIRead 00f0
8730
8731   //Read  MACRO_ERROR_IN_OPERAND=0x0;     Address(0xf0[7:6])
8732
8733   SPIRead 00f0
8734
8735   //Read  MACRO_ERROR_IN_EXECUTION=0x0;   Address(0xf0[7:7])
8736
8737   SPIRead 00f3
8738   SPIRead 00f2
8739
8740   //Read  MACRO_ERROR_EXTENDED_CODE=0x0;  Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
8741
8742   SPIRead 00f7
8743   SPIRead 00f6
8744   SPIRead 00f5
8745   SPIRead 00f4
8746
8747   //Read  MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
8748
8749   SPIRead 00f0
8750
8751   //Read  MACRO_READY=0x1;    Address(0xf0[7:0])
8752
8753
8754   SPIPoll 00f0,0,0,1
8755
8756   SPIWrite 00a3,00    //MACRO_OPERAND_REG0=0x10301;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
8757   SPIWrite 00a2,01
8758   SPIWrite 00a1,03
8759   SPIWrite 00a0,01
8760   SPIWrite 0193,79    //MACRO_OPCODE=0x79;    Address(0x193[7:0],0x194[7:0])
8761
8762   WAIT 0.001
8763   SPIRead 00f0
8764
8765   //Read  MACRO_DONE=0x1;     Address(0xf0[7:2])
8766
8767
8768   SPIPoll 00f0,2,2,4
8769
8770   SPIRead 00f0
8771
8772   //Read  MACRO_ERROR=0x0;    Address(0xf0[7:3])
8773
8774   SPIRead 00f1
8775
```

```
8776  //Read  MACRO_ERROR_OPCODE=0x0;     Address(0xf1[7:0],0xf2[7:0])
8777
8778  SPIRead 00f0
8779
8780  //Read  MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])
8781
8782  SPIRead 00f0
8783
8784  //Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;     Address(0xf0[7:5])
8785
8786  SPIRead 00f0
8787
8788  //Read  MACRO_ERROR_IN_OPERAND=0x0;     Address(0xf0[7:6])
8789
8790  SPIRead 00f0
8791
8792  //Read  MACRO_ERROR_IN_EXECUTION=0x0;   Address(0xf0[7:7])
8793
8794  SPIRead 00f3
8795  SPIRead 00f2
8796
8797  //Read  MACRO_ERROR_EXTENDED_CODE=0x0;  Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
8798
8799  SPIRead 00f7
8800  SPIRead 00f6
8801  SPIRead 00f5
8802  SPIRead 00f4
8803
8804  //Read  MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
8805
8806  SPIWrite 0018,00    //macro=0x0;    Address(0x18[7:5])
8807  SPIWrite 0016,60    //serdes_jesd=0x3;  Address(0x16[7:5])
8808  SPIWrite 702d,00
8809  SPIWrite 702c,05
8810  SPIWrite 7025,00
8811  SPIWrite 7024,08
8812  SPIWrite 702b,e0
8813  SPIWrite 702a,20
8814
8815  WAIT 0.01
8816  SPIWrite 702d,00
8817  SPIWrite 702c,02
8818  SPIWrite 7025,00
8819  SPIWrite 7024,50
8820  SPIWrite 702b,e0
8821  SPIWrite 702a,20
8822
8823  WAIT 0.01
8824  SPIWrite 701b,07    //DOMAIN_RESET=0x777;   Address(0x980d[3:0],0x980e[7:0])
8825  SPIWrite 701a,77
8826  SPIWrite 701b,00    //DOMAIN_RESET=0x0;     Address(0x980d[3:0],0x980e[7:0])
8827  SPIWrite 701a,00
8828
8829  WAIT 5
8830  SPIWrite 0016,00    //serdes_jesd=0x0;  Address(0x16[7:5])
8831
8832  //END: Done loading Serdes Firmware.
8833
8834
8835  //STEP: topConfig/step0
8836
8837  //START: Setting Top Control Modes
8838
8839  SPIWrite 0015,80    //timing_controller=0x1;    Address(0x15[7:7])
8840  SPIWrite 0081,00    //fdd_mode=0x0;     Address(0x81[7:0])
8841  SPIWrite 0080,01    //mode_2t2r=0x1;    Address(0x80[7:0])
8842  SPIWrite 008c,01    //use_per_ch_txab_tdd=0x1;  Address(0x8c[7:0])
8843  SPIWrite 008d,01    //use_per_ch_txcd_tdd=0x1;  Address(0x8d[7:0])
```

```
SPIWrite 00a0,01    //use_per_ch_rxab_tdd=0x1;  Address(0xa0[7:0])
SPIWrite 00a1,01    //use_per_ch_rxcd_tdd=0x1;  Address(0xa1[7:0])
SPIWrite 0015,00    //timing_controller=0x0;    Address(0x15[7:7])
SPIWrite 0015,02    //ana_4t4r=0x1;     Address(0x15[7:1])
SPIWrite 0129,00    //tx_dac_div2=0x0;  Address(0x129[7:0])
SPIWrite 012a,00    //rx_adc_div2=0x0;  Address(0x12a[7:0])
SPIWrite 012b,00    //fb_adc_div2=0x0;  Address(0x12b[7:0])
SPIWrite 00dc,00    //clk_out_sel_tx_ab=0x0;    Address(0xdc[7:0])
SPIWrite 00df,00    //clk_out_sel_tx_cd=0x0;    Address(0xdf[7:0])
SPIWrite 00c4,00    //clk_out_sel_fb_ab=0x0;    Address(0xc4[7:0])
SPIWrite 00c7,00    //clk_out_sel_fb_cd=0x0;    Address(0xc7[7:0])
SPIWrite 00cc,00    //clk_out_sel_rx_ab=0x0;    Address(0xcc[7:0])
SPIWrite 00cf,00    //clk_out_sel_rx_cd=0x0;    Address(0xcf[7:0])
SPIWrite 0015,00    //ana_4t4r=0x0;     Address(0x15[7:1])
SPIWrite 0015,80    //timing_controller=0x1;    Address(0x15[7:7])
SPIWrite 0399,00    //config_rise_xx_A_7=0x0;   Address(0x398[7:0],0x399[7:0],0x39a[7:0])
SPIWrite 0398,00
SPIWrite 039b,00    //config_fall_xx_A_7=0xe1;  Address(0x39a[7:0],0x39b[7:0],0x39c[7:0])
SPIWrite 039a,e1
SPIWrite 0451,00    //config_rise_xx_A_7=0x0;   Address(0x450[7:0],0x451[7:0],0x452[7:0])
SPIWrite 0450,00
SPIWrite 0453,00    //config_fall_xx_A_7=0xe1;  Address(0x452[7:0],0x453[7:0],0x454[7:0])
SPIWrite 0452,e1
SPIWrite 0509,00    //config_rise_xx_A_7=0x0;   Address(0x508[7:0],0x509[7:0],0x50a[7:0])
SPIWrite 0508,00
SPIWrite 050b,00    //config_fall_xx_A_7=0xe1;  Address(0x50a[7:0],0x50b[7:0],0x50c[7:0])
SPIWrite 050a,e1
SPIWrite 05c1,00    //config_rise_xx_A_7=0x0;   Address(0x5c0[7:0],0x5c1[7:0],0x5c2[7:0])
SPIWrite 05c0,00
SPIWrite 05c3,00    //config_fall_xx_A_7=0xe1;  Address(0x5c2[7:0],0x5c3[7:0],0x5c4[7:0])
SPIWrite 05c2,e1
SPIWrite 0679,00    //config_rise_xx_A_7=0x0;   Address(0x678[7:0],0x679[7:0],0x67a[7:0])
SPIWrite 0678,00
SPIWrite 067b,00    //config_fall_xx_A_7=0xe1;  Address(0x67a[7:0],0x67b[7:0],0x67c[7:0])
SPIWrite 067a,e1
SPIWrite 0731,00    //config_rise_xx_A_7=0x0;   Address(0x730[7:0],0x731[7:0],0x732[7:0])
SPIWrite 0730,00
SPIWrite 0733,00    //config_fall_xx_A_7=0xe1;  Address(0x732[7:0],0x733[7:0],0x734[7:0])
SPIWrite 0732,e1

//END: Setting Top Control Modes

SPIWrite 0015,00    //timing_controller=0x0;    Address(0x15[7:7])
SPIWrite 0015,40    //digtop=0x1;   Address(0x15[7:6])
SPIWrite 0180,00    //spi_ids_dsa_ab=0x0;   Address(0x180[7:0])
SPIWrite 0181,00    //spi_ids_dsa_cd=0x0;   Address(0x181[7:0])
SPIWrite 0015,00    //digtop=0x0;   Address(0x15[7:6])

//STEP: topConfig/step1
SPIWrite 0013,40    //dsa_page1=0x1;    Address(0x13[7:6])
SPIWrite 054e,00    //tm_gate_clk=0x0;  Address(0x54e[7:0])
SPIWrite 0013,80    //dsa_page1=0x2;    Address(0x13[7:6])
SPIWrite 054e,00    //tm_gate_clk=0x0;  Address(0x54e[7:0])
SPIWrite 0013,c0    //dsa_page1=0x3;    Address(0x13[7:6])
SPIWrite 0444,03
SPIWrite 0445,00
SPIWrite 0446,00
SPIWrite 0447,00
SPIWrite 0448,0b
SPIWrite 0449,84
SPIWrite 044a,00
SPIWrite 044b,00
SPIWrite 044c,1f
SPIWrite 044d,08
SPIWrite 044e,01
SPIWrite 044f,00
SPIWrite 0450,33
SPIWrite 0451,8c
SPIWrite 0452,01
```

```
SPIWrite 0453,00
SPIWrite 0454,47
SPIWrite 0455,90
SPIWrite 0456,02
SPIWrite 0457,00
SPIWrite 0458,5b
SPIWrite 0459,14
SPIWrite 045a,03
SPIWrite 045b,01
SPIWrite 045c,6f
SPIWrite 045d,18
SPIWrite 045e,04
SPIWrite 045f,01
SPIWrite 0460,83
SPIWrite 0461,9c
SPIWrite 0462,04
SPIWrite 0463,01
SPIWrite 0464,9b
SPIWrite 0465,a0
SPIWrite 0466,05
SPIWrite 0467,02
SPIWrite 0468,b3
SPIWrite 0469,a4
SPIWrite 046a,06
SPIWrite 046b,02
SPIWrite 046c,c7
SPIWrite 046d,a8
SPIWrite 046e,07
SPIWrite 046f,03
SPIWrite 0470,df
SPIWrite 0471,ac
SPIWrite 0472,08
SPIWrite 0473,03
SPIWrite 0474,f7
SPIWrite 0475,b0
SPIWrite 0476,09
SPIWrite 0477,04
SPIWrite 0478,17
SPIWrite 0479,b5
SPIWrite 047a,0a
SPIWrite 047b,04
SPIWrite 047c,37
SPIWrite 047d,b9
SPIWrite 047e,0b
SPIWrite 047f,04
SPIWrite 0480,4f
SPIWrite 0481,bd
SPIWrite 0482,0c
SPIWrite 0483,05
SPIWrite 0484,6b
SPIWrite 0485,c1
SPIWrite 0486,0d
SPIWrite 0487,07
SPIWrite 0488,87
SPIWrite 0489,c5
SPIWrite 048a,0e
SPIWrite 048b,07
SPIWrite 048c,9f
SPIWrite 048d,c9
SPIWrite 048e,0f
SPIWrite 048f,07
SPIWrite 0490,a7
SPIWrite 0491,49
SPIWrite 0492,10
SPIWrite 0493,07
SPIWrite 0494,bb
SPIWrite 0495,4d
SPIWrite 0496,11
SPIWrite 0497,08
```

```
  SPIWrite 0498,d3
  SPIWrite 0499,51
  SPIWrite 049a,12
  SPIWrite 049b,09
  SPIWrite 049c,eb
  SPIWrite 049d,55
  SPIWrite 049e,13
  SPIWrite 049f,0a
  SPIWrite 04a0,0b
  SPIWrite 04a1,da
  SPIWrite 04a2,14
  SPIWrite 04a3,0b
  SPIWrite 04a4,23
  SPIWrite 04a5,de
  SPIWrite 04a6,15
  SPIWrite 04a7,0c
  SPIWrite 04a8,3b
  SPIWrite 04a9,e2
  SPIWrite 04aa,16
  SPIWrite 04ab,0e
  SPIWrite 04ac,4f
  SPIWrite 04ad,66
  SPIWrite 04ae,17
  SPIWrite 04af,0e
  SPIWrite 04b0,63
  SPIWrite 04b1,ea
  SPIWrite 04b2,17
  SPIWrite 04b3,11
  SPIWrite 04b4,77
  SPIWrite 04b5,6e
  SPIWrite 04b6,18
  SPIWrite 04b7,11
  SPIWrite 04b8,8b
  SPIWrite 04b9,f2
  SPIWrite 04ba,18
  SPIWrite 04bb,13
  SPIWrite 04bc,9f
  SPIWrite 04bd,72
  SPIWrite 04be,19
  SPIWrite 04bf,15
  SPIWrite 04c0,b3
  SPIWrite 04c1,f6
  SPIWrite 04c2,19
  SPIWrite 04c3,16
  SPIWrite 04c4,c3
  SPIWrite 04c5,76
  SPIWrite 04c6,1a
  SPIWrite 04c7,18
  SPIWrite 04c8,d7
  SPIWrite 04c9,f6
  SPIWrite 04ca,1a
  SPIWrite 04cb,19
  SPIWrite 04cc,eb
  SPIWrite 04cd,76
  SPIWrite 04ce,1b
  SPIWrite 04cf,1b
  SPIWrite 04d0,ff
  SPIWrite 04d1,f6
  SPIWrite 04d2,1b
  SPIWrite 04d3,1d
  SPIWrite 04d4,13
  SPIWrite 04d5,77
  SPIWrite 04d6,1c
  SPIWrite 04d7,1f
  SPIWrite 04d8,23
  SPIWrite 04d9,f7
  SPIWrite 04da,1c
  SPIWrite 04db,1f
  SPIWrite 04dc,33
```

```
SPIWrite 04dd,77
SPIWrite 04de,1d
SPIWrite 04df,1f
SPIWrite 04e0,3f
SPIWrite 04e1,f7
SPIWrite 04e2,1d
SPIWrite 04e3,1f
SPIWrite 04e4,4b
SPIWrite 04e5,77
SPIWrite 04e6,1e
SPIWrite 04e7,1f
SPIWrite 04e8,57
SPIWrite 04e9,f7
SPIWrite 04ea,1e
SPIWrite 04eb,1f
SPIWrite 04ec,5f
SPIWrite 04ed,77
SPIWrite 04ee,1f
SPIWrite 04ef,1f
SPIWrite 04f0,67
SPIWrite 04f1,f7
SPIWrite 04f2,1f
SPIWrite 04f3,1f
SPIWrite 04f4,73
SPIWrite 04f5,f7
SPIWrite 04f6,1f
SPIWrite 04f7,1f
SPIWrite 04f8,7b
SPIWrite 04f9,f7
SPIWrite 04fa,1f
SPIWrite 04fb,1f
SPIWrite 04fc,87
SPIWrite 04fd,f7
SPIWrite 04fe,1f
SPIWrite 04ff,1f
SPIWrite 0500,8f
SPIWrite 0501,f7
SPIWrite 0502,1f
SPIWrite 0503,1f
SPIWrite 0504,97
SPIWrite 0505,f7
SPIWrite 0506,1f
SPIWrite 0507,1f
SPIWrite 0508,9b
SPIWrite 0509,f7
SPIWrite 050a,1f
SPIWrite 050b,1f
SPIWrite 0744,03
SPIWrite 0745,00
SPIWrite 0746,00
SPIWrite 0747,00
SPIWrite 0748,0b
SPIWrite 0749,84
SPIWrite 074a,00
SPIWrite 074b,00
SPIWrite 074c,1f
SPIWrite 074d,08
SPIWrite 074e,01
SPIWrite 074f,00
SPIWrite 0750,33
SPIWrite 0751,8c
SPIWrite 0752,01
SPIWrite 0753,00
SPIWrite 0754,47
SPIWrite 0755,90
SPIWrite 0756,02
SPIWrite 0757,00
SPIWrite 0758,5b
SPIWrite 0759,14
```

```
SPIWrite 075a,03
SPIWrite 075b,01
SPIWrite 075c,6f
SPIWrite 075d,18
SPIWrite 075e,04
SPIWrite 075f,01
SPIWrite 0760,83
SPIWrite 0761,9c
SPIWrite 0762,04
SPIWrite 0763,01
SPIWrite 0764,9b
SPIWrite 0765,a0
SPIWrite 0766,05
SPIWrite 0767,02
SPIWrite 0768,b3
SPIWrite 0769,a4
SPIWrite 076a,06
SPIWrite 076b,02
SPIWrite 076c,c7
SPIWrite 076d,a8
SPIWrite 076e,07
SPIWrite 076f,03
SPIWrite 0770,df
SPIWrite 0771,ac
SPIWrite 0772,08
SPIWrite 0773,03
SPIWrite 0774,f7
SPIWrite 0775,b0
SPIWrite 0776,09
SPIWrite 0777,04
SPIWrite 0778,17
SPIWrite 0779,b5
SPIWrite 077a,0a
SPIWrite 077b,04
SPIWrite 077c,37
SPIWrite 077d,b9
SPIWrite 077e,0b
SPIWrite 077f,04
SPIWrite 0780,4f
SPIWrite 0781,bd
SPIWrite 0782,0c
SPIWrite 0783,05
SPIWrite 0784,6b
SPIWrite 0785,c1
SPIWrite 0786,0d
SPIWrite 0787,07
SPIWrite 0788,87
SPIWrite 0789,c5
SPIWrite 078a,0e
SPIWrite 078b,07
SPIWrite 078c,9f
SPIWrite 078d,c9
SPIWrite 078e,0f
SPIWrite 078f,07
SPIWrite 0790,a7
SPIWrite 0791,49
SPIWrite 0792,10
SPIWrite 0793,07
SPIWrite 0794,bb
SPIWrite 0795,4d
SPIWrite 0796,11
SPIWrite 0797,08
SPIWrite 0798,d3
SPIWrite 0799,51
SPIWrite 079a,12
SPIWrite 079b,09
SPIWrite 079c,eb
SPIWrite 079d,55
SPIWrite 079e,13
```

```
  SPIWrite 079f,0a
  SPIWrite 07a0,0b
  SPIWrite 07a1,da
  SPIWrite 07a2,14
  SPIWrite 07a3,0b
  SPIWrite 07a4,23
  SPIWrite 07a5,de
  SPIWrite 07a6,15
  SPIWrite 07a7,0c
  SPIWrite 07a8,3b
  SPIWrite 07a9,e2
  SPIWrite 07aa,16
  SPIWrite 07ab,0e
  SPIWrite 07ac,4f
  SPIWrite 07ad,66
  SPIWrite 07ae,17
  SPIWrite 07af,0e
  SPIWrite 07b0,63
  SPIWrite 07b1,ea
  SPIWrite 07b2,17
  SPIWrite 07b3,11
  SPIWrite 07b4,77
  SPIWrite 07b5,6e
  SPIWrite 07b6,18
  SPIWrite 07b7,11
  SPIWrite 07b8,8b
  SPIWrite 07b9,f2
  SPIWrite 07ba,18
  SPIWrite 07bb,13
  SPIWrite 07bc,9f
  SPIWrite 07bd,72
  SPIWrite 07be,19
  SPIWrite 07bf,15
  SPIWrite 07c0,b3
  SPIWrite 07c1,f6
  SPIWrite 07c2,19
  SPIWrite 07c3,16
  SPIWrite 07c4,c3
  SPIWrite 07c5,76
  SPIWrite 07c6,1a
  SPIWrite 07c7,18
  SPIWrite 07c8,d7
  SPIWrite 07c9,f6
  SPIWrite 07ca,1a
  SPIWrite 07cb,19
  SPIWrite 07cc,eb
  SPIWrite 07cd,76
  SPIWrite 07ce,1b
  SPIWrite 07cf,1b
  SPIWrite 07d0,ff
  SPIWrite 07d1,f6
  SPIWrite 07d2,1b
  SPIWrite 07d3,1d
  SPIWrite 07d4,13
  SPIWrite 07d5,77
  SPIWrite 07d6,1c
  SPIWrite 07d7,1f
  SPIWrite 07d8,23
  SPIWrite 07d9,f7
  SPIWrite 07da,1c
  SPIWrite 07db,1f
  SPIWrite 07dc,33
  SPIWrite 07dd,77
  SPIWrite 07de,1d
  SPIWrite 07df,1f
  SPIWrite 07e0,3f
  SPIWrite 07e1,f7
  SPIWrite 07e2,1d
  SPIWrite 07e3,1f
```

```
  SPIWrite 07e4,4b
  SPIWrite 07e5,77
  SPIWrite 07e6,1e
  SPIWrite 07e7,1f
  SPIWrite 07e8,57
  SPIWrite 07e9,f7
  SPIWrite 07ea,1e
  SPIWrite 07eb,1f
  SPIWrite 07ec,5f
  SPIWrite 07ed,77
  SPIWrite 07ee,1f
  SPIWrite 07ef,1f
  SPIWrite 07f0,67
  SPIWrite 07f1,f7
  SPIWrite 07f2,1f
  SPIWrite 07f3,1f
  SPIWrite 07f4,73
  SPIWrite 07f5,f7
  SPIWrite 07f6,1f
  SPIWrite 07f7,1f
  SPIWrite 07f8,7b
  SPIWrite 07f9,f7
  SPIWrite 07fa,1f
  SPIWrite 07fb,1f
  SPIWrite 07fc,87
  SPIWrite 07fd,f7
  SPIWrite 07fe,1f
  SPIWrite 07ff,1f
  SPIWrite 0800,8f
  SPIWrite 0801,f7
  SPIWrite 0802,1f
  SPIWrite 0803,1f
  SPIWrite 0804,97
  SPIWrite 0805,f7
  SPIWrite 0806,1f
  SPIWrite 0807,1f
  SPIWrite 0808,9b
  SPIWrite 0809,f7
  SPIWrite 080a,1f
  SPIWrite 080b,1f
  SPIWrite 0844,03
  SPIWrite 0845,00
  SPIWrite 0846,00
  SPIWrite 0847,00
  SPIWrite 0848,0b
  SPIWrite 0849,84
  SPIWrite 084a,00
  SPIWrite 084b,00
  SPIWrite 084c,1f
  SPIWrite 084d,08
  SPIWrite 084e,01
  SPIWrite 084f,00
  SPIWrite 0850,33
  SPIWrite 0851,8c
  SPIWrite 0852,01
  SPIWrite 0853,00
  SPIWrite 0854,47
  SPIWrite 0855,90
  SPIWrite 0856,02
  SPIWrite 0857,00
  SPIWrite 0858,5b
  SPIWrite 0859,14
  SPIWrite 085a,03
  SPIWrite 085b,01
  SPIWrite 085c,6f
  SPIWrite 085d,18
  SPIWrite 085e,04
  SPIWrite 085f,01
  SPIWrite 0860,83
```

```
SPIWrite 0861,9c
SPIWrite 0862,04
SPIWrite 0863,01
SPIWrite 0864,9b
SPIWrite 0865,a0
SPIWrite 0866,05
SPIWrite 0867,02
SPIWrite 0868,b3
SPIWrite 0869,a4
SPIWrite 086a,06
SPIWrite 086b,02
SPIWrite 086c,c7
SPIWrite 086d,a8
SPIWrite 086e,07
SPIWrite 086f,03
SPIWrite 0870,df
SPIWrite 0871,ac
SPIWrite 0872,08
SPIWrite 0873,03
SPIWrite 0874,f7
SPIWrite 0875,b0
SPIWrite 0876,09
SPIWrite 0877,04
SPIWrite 0878,17
SPIWrite 0879,b5
SPIWrite 087a,0a
SPIWrite 087b,04
SPIWrite 087c,37
SPIWrite 087d,b9
SPIWrite 087e,0b
SPIWrite 087f,04
SPIWrite 0880,4f
SPIWrite 0881,bd
SPIWrite 0882,0c
SPIWrite 0883,05
SPIWrite 0884,6b
SPIWrite 0885,c1
SPIWrite 0886,0d
SPIWrite 0887,07
SPIWrite 0888,87
SPIWrite 0889,c5
SPIWrite 088a,0e
SPIWrite 088b,07
SPIWrite 088c,9f
SPIWrite 088d,c9
SPIWrite 088e,0f
SPIWrite 088f,07
SPIWrite 0890,a7
SPIWrite 0891,49
SPIWrite 0892,10
SPIWrite 0893,07
SPIWrite 0894,bb
SPIWrite 0895,4d
SPIWrite 0896,11
SPIWrite 0897,08
SPIWrite 0898,d3
SPIWrite 0899,51
SPIWrite 089a,12
SPIWrite 089b,09
SPIWrite 089c,eb
SPIWrite 089d,55
SPIWrite 089e,13
SPIWrite 089f,0a
SPIWrite 08a0,0b
SPIWrite 08a1,da
SPIWrite 08a2,14
SPIWrite 08a3,0b
SPIWrite 08a4,23
SPIWrite 08a5,de
```

```
  SPIWrite 08a6,15
  SPIWrite 08a7,0c
  SPIWrite 08a8,3b
  SPIWrite 08a9,e2
  SPIWrite 08aa,16
  SPIWrite 08ab,0e
  SPIWrite 08ac,4f
  SPIWrite 08ad,66
  SPIWrite 08ae,17
  SPIWrite 08af,0e
  SPIWrite 08b0,63
  SPIWrite 08b1,ea
  SPIWrite 08b2,17
  SPIWrite 08b3,11
  SPIWrite 08b4,77
  SPIWrite 08b5,6e
  SPIWrite 08b6,18
  SPIWrite 08b7,11
  SPIWrite 08b8,8b
  SPIWrite 08b9,f2
  SPIWrite 08ba,18
  SPIWrite 08bb,13
  SPIWrite 08bc,9f
  SPIWrite 08bd,72
  SPIWrite 08be,19
  SPIWrite 08bf,15
  SPIWrite 08c0,b3
  SPIWrite 08c1,f6
  SPIWrite 08c2,19
  SPIWrite 08c3,16
  SPIWrite 08c4,c3
  SPIWrite 08c5,76
  SPIWrite 08c6,1a
  SPIWrite 08c7,18
  SPIWrite 08c8,d7
  SPIWrite 08c9,f6
  SPIWrite 08ca,1a
  SPIWrite 08cb,19
  SPIWrite 08cc,eb
  SPIWrite 08cd,76
  SPIWrite 08ce,1b
  SPIWrite 08cf,1b
  SPIWrite 08d0,ff
  SPIWrite 08d1,f6
  SPIWrite 08d2,1b
  SPIWrite 08d3,1d
  SPIWrite 08d4,13
  SPIWrite 08d5,77
  SPIWrite 08d6,1c
  SPIWrite 08d7,1f
  SPIWrite 08d8,23
  SPIWrite 08d9,f7
  SPIWrite 08da,1c
  SPIWrite 08db,1f
  SPIWrite 08dc,33
  SPIWrite 08dd,77
  SPIWrite 08de,1d
  SPIWrite 08df,1f
  SPIWrite 08e0,3f
  SPIWrite 08e1,f7
  SPIWrite 08e2,1d
  SPIWrite 08e3,1f
  SPIWrite 08e4,4b
  SPIWrite 08e5,77
  SPIWrite 08e6,1e
  SPIWrite 08e7,1f
  SPIWrite 08e8,57
  SPIWrite 08e9,f7
  SPIWrite 08ea,1e
```

```
SPIWrite 08eb,1f
SPIWrite 08ec,5f
SPIWrite 08ed,77
SPIWrite 08ee,1f
SPIWrite 08ef,1f
SPIWrite 08f0,67
SPIWrite 08f1,f7
SPIWrite 08f2,1f
SPIWrite 08f3,1f
SPIWrite 08f4,73
SPIWrite 08f5,f7
SPIWrite 08f6,1f
SPIWrite 08f7,1f
SPIWrite 08f8,7b
SPIWrite 08f9,f7
SPIWrite 08fa,1f
SPIWrite 08fb,1f
SPIWrite 08fc,87
SPIWrite 08fd,f7
SPIWrite 08fe,1f
SPIWrite 08ff,1f
SPIWrite 0900,8f
SPIWrite 0901,f7
SPIWrite 0902,1f
SPIWrite 0903,1f
SPIWrite 0904,97
SPIWrite 0905,f7
SPIWrite 0906,1f
SPIWrite 0907,1f
SPIWrite 0908,9b
SPIWrite 0909,f7
SPIWrite 090a,1f
SPIWrite 090b,1f
SPIWrite 00d1,06    //dig_gain_range=0x6;   Address(0xd1[7:0])
SPIWrite 0124,01    //spi_agc_dsa_A=0x1;    Address(0x124[7:0])
SPIWrite 0124,00    //spi_agc_dsa_A=0x0;    Address(0x124[7:0])
SPIWrite 0174,01    //spi_agc_dsa_B=0x1;    Address(0x174[7:0])
SPIWrite 0174,00    //spi_agc_dsa_B=0x0;    Address(0x174[7:0])
SPIWrite 0013,00    //dsa_page1=0x0;    Address(0x13[7:6])
SPIWrite 0013,10    //dsa_page0=0x1;    Address(0x13[7:4])
SPIWrite 006c,01    //spi_agc_dsa_fb=0x1;   Address(0x6c[7:0])
SPIWrite 006c,00    //spi_agc_dsa_fb=0x0;   Address(0x6c[7:0])
SPIWrite 0013,00    //dsa_page0=0x0;    Address(0x13[7:4])
SPIWrite 0013,80    //dsa_page1=0x2;    Address(0x13[7:6])
SPIWrite 00d1,06    //dig_gain_range=0x6;   Address(0xd1[7:0])
SPIWrite 0124,01    //spi_agc_dsa_A=0x1;    Address(0x124[7:0])
SPIWrite 0124,00    //spi_agc_dsa_A=0x0;    Address(0x124[7:0])
SPIWrite 0174,01    //spi_agc_dsa_B=0x1;    Address(0x174[7:0])
SPIWrite 0174,00    //spi_agc_dsa_B=0x0;    Address(0x174[7:0])
SPIWrite 0013,00    //dsa_page1=0x0;    Address(0x13[7:6])
SPIWrite 0013,20    //dsa_page0=0x2;    Address(0x13[7:4])
SPIWrite 006c,01    //spi_agc_dsa_fb=0x1;   Address(0x6c[7:0])
SPIWrite 006c,00    //spi_agc_dsa_fb=0x0;   Address(0x6c[7:0])
SPIWrite 0013,00    //dsa_page0=0x0;    Address(0x13[7:4])
SPIWrite 0015,40    //digtop=0x1;   Address(0x15[7:6])
SPIWrite 0940,00    //disable_pkdet_regs_ab=0x0;    Address(0x940[7:0])
SPIWrite 0941,00    //disable_pkdet_regs_cd=0x0;    Address(0x941[7:0])
SPIWrite 0015,00    //digtop=0x0;   Address(0x15[7:6])
SPIWrite 0013,c0    //dsa_page1=0x3;    Address(0x13[7:6])
SPIWrite 00d1,03    //dig_gain_range=0x3;   Address(0xd1[7:0])
SPIWrite 0545,06    //tm_rel_index_step=0x6;    Address(0x545[7:0])
SPIWrite 054a,06    //tm_rel_cust_diff=0x6;     Address(0x54a[7:0])
SPIWrite 05a4,2c    //tm_pkdet_index_limit=0x2c;    Address(0x5a4[7:0])
SPIWrite 05a5,18    //tm_pkdet_index_add=0x18;  Address(0x5a5[7:0])
SPIWrite 0577,00    //tm_rel_en_exit_decay=0x0;     Address(0x577[7:0])
SPIWrite 056f,01    //tm_rel_en_exit_count=0x1;     Address(0x56f[7:0])
SPIWrite 05a1,00    //tm_rel_use_cust_pkdet=0x0;    Address(0x5a1[7:0])
SPIWrite 0013,00    //dsa_page1=0x0;    Address(0x13[7:6])
```

```
//STEP: topConfig/step2
SPIWrite 0013,10    //dsa_page0=0x1;    Address(0x13[7:4])
SPIWrite 00d0,18    //txa_dsa_dig0_gain=0x18;   Address(0xd0[7:0],0xd1[7:0])
SPIWrite 00d4,18    //txb_dsa_dig0_gain=0x18;   Address(0xd4[7:0],0xd5[7:0])
SPIWrite 0013,20    //dsa_page0=0x2;    Address(0x13[7:4])
SPIWrite 00d0,18    //txa_dsa_dig0_gain=0x18;   Address(0xd0[7:0],0xd1[7:0])
SPIWrite 00d4,18    //txb_dsa_dig0_gain=0x18;   Address(0xd4[7:0],0xd5[7:0])
SPIWrite 0013,00    //dsa_page0=0x0;    Address(0x13[7:4])
SPIWrite 0013,c0    //dsa_page1=0x3;    Address(0x13[7:6])
SPIWrite 0a37,40
SPIWrite 0a3f,40
SPIWrite 0a4f,40
SPIWrite 0a5f,40
SPIWrite 0a77,40
SPIWrite 0a7f,40
SPIWrite 0a97,40
SPIWrite 0a9f,40
SPIWrite 0aa7,40
SPIWrite 0aaf,40
SPIWrite 0c37,40
SPIWrite 0c3f,40
SPIWrite 0c4f,40
SPIWrite 0c5f,40
SPIWrite 0c77,40
SPIWrite 0c7f,40
SPIWrite 0c97,40
SPIWrite 0c9f,40
SPIWrite 0ca7,40
SPIWrite 0caf,40
SPIWrite 0013,00    //dsa_page1=0x0;    Address(0x13[7:6])

//STEP: sysConfig/step0

//START: Configuring RRF Mode to TOP MCU

SPIWrite 0018,20    //macro=0x1;    Address(0x18[7:5])
SPIRead 00f0

//Read  MACRO_READY=0x1;    Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00    //MACRO_OPERAND_REG0=0x3;
Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00
SPIWrite 00a1,00
SPIWrite 00a0,03
SPIWrite 0193,22    //MACRO_OPCODE=0x22;    Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0

//Read  MACRO_DONE=0x1;     Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIRead 00f0

//Read  MACRO_ERROR=0x0;    Address(0xf0[7:3])

SPIRead 00f1

//Read  MACRO_ERROR_OPCODE=0x0;     Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0

//Read  MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])
```

```
9602
9603   SPIRead 00f0
9604
9605   //Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;     Address(0xf0[7:5])
9606
9607   SPIRead 00f0
9608
9609   //Read  MACRO_ERROR_IN_OPERAND=0x0;     Address(0xf0[7:6])
9610
9611   SPIRead 00f0
9612
9613   //Read  MACRO_ERROR_IN_EXECUTION=0x0;   Address(0xf0[7:7])
9614
9615   SPIRead 00f3
9616   SPIRead 00f2
9617
9618   //Read  MACRO_ERROR_EXTENDED_CODE=0x0;  Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
9619
9620   SPIRead 00f7
9621   SPIRead 00f6
9622   SPIRead 00f5
9623   SPIRead 00f4
9624
9625   //Read  MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
9626
9627   SPIRead 00f0
9628
9629   //Read  MACRO_READY=0x1;    Address(0xf0[7:0])
9630
9631
9632   SPIPoll 00f0,0,0,1
9633
9634   SPIWrite 00a3,00    //MACRO_OPERAND_REG0=0xf010f;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
9635   SPIWrite 00a2,0f
9636   SPIWrite 00a1,01
9637   SPIWrite 00a0,0f
9638   SPIWrite 0193,21    //MACRO_OPCODE=0x21;    Address(0x193[7:0],0x194[7:0])
9639
9640   WAIT 0.001
9641   SPIRead 00f0
9642
9643   //Read  MACRO_DONE=0x1;     Address(0xf0[7:2])
9644
9645
9646   SPIPoll 00f0,2,2,4
9647
9648   SPIRead 00f0
9649
9650   //Read  MACRO_ERROR=0x0;    Address(0xf0[7:3])
9651
9652   SPIRead 00f1
9653
9654   //Read  MACRO_ERROR_OPCODE=0x0;     Address(0xf1[7:0],0xf2[7:0])
9655
9656   SPIRead 00f0
9657
9658   //Read  MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])
9659
9660   SPIRead 00f0
9661
9662   //Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;     Address(0xf0[7:5])
9663
9664   SPIRead 00f0
9665
9666   //Read  MACRO_ERROR_IN_OPERAND=0x0;     Address(0xf0[7:6])
9667
9668   SPIRead 00f0
```

```
9669
9670   //Read  MACRO_ERROR_IN_EXECUTION=0x0;   Address(0xf0[7:7])
9671
9672   SPIRead 00f3
9673   SPIRead 00f2
9674
9675   //Read  MACRO_ERROR_EXTENDED_CODE=0x0;  Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
9676
9677   SPIRead 00f7
9678   SPIRead 00f6
9679   SPIRead 00f5
9680   SPIRead 00f4
9681
9682   //Read  MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
9683
9684   SPIRead 00f0
9685
9686   //Read  MACRO_READY=0x1;    Address(0xf0[7:0])
9687
9688
9689   SPIPoll 00f0,0,0,1
9690
9691   SPIWrite 00a3,00    //MACRO_OPERAND_REG0=0x0;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
9692   SPIWrite 00a2,00
9693   SPIWrite 00a1,00
9694   SPIWrite 00a0,00
9695   SPIWrite 0193,2f    //MACRO_OPCODE=0x2f;    Address(0x193[7:0],0x194[7:0])
9696
9697   WAIT 0.001
9698   SPIRead 00f0
9699
9700   //Read  MACRO_DONE=0x1;     Address(0xf0[7:2])
9701
9702
9703   SPIPoll 00f0,2,2,4
9704
9705   SPIRead 00f0
9706
9707   //Read  MACRO_ERROR=0x0;    Address(0xf0[7:3])
9708
9709   SPIRead 00f1
9710
9711   //Read  MACRO_ERROR_OPCODE=0x0;     Address(0xf1[7:0],0xf2[7:0])
9712
9713   SPIRead 00f0
9714
9715   //Read  MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])
9716
9717   SPIRead 00f0
9718
9719   //Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;     Address(0xf0[7:5])
9720
9721   SPIRead 00f0
9722
9723   //Read  MACRO_ERROR_IN_OPERAND=0x0;     Address(0xf0[7:6])
9724
9725   SPIRead 00f0
9726
9727   //Read  MACRO_ERROR_IN_EXECUTION=0x0;   Address(0xf0[7:7])
9728
9729   SPIRead 00f3
9730   SPIRead 00f2
9731
9732   //Read  MACRO_ERROR_EXTENDED_CODE=0x0;  Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
9733
9734   SPIRead 00f7
9735   SPIRead 00f6
```

```
9736   SPIRead 00f5
9737   SPIRead 00f4
9738
9739   //Read  MACRO_ERROR_EXTENDED_CODE_2=0x0;
       Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
9740
9741
9742   //END: Configuring RRF Mode to TOP MCU
9743
9744   SPIWrite 0018,00    //macro=0x0;    Address(0x18[7:5])
9745
9746   //STEP: sysConfig/step1
9747
9748   //START: Configuring RX Chain Parameters to TOP MCU
9749
9750   SPIWrite 0018,20    //macro=0x1;    Address(0x18[7:5])
9751   SPIRead 00f0
9752
9753   //Read  MACRO_READY=0x1;    Address(0xf0[7:0])
9754
9755
9756   SPIPoll 00f0,0,0,1
9757
9758   SPIWrite 00a3,00    //MACRO_OPERAND_REG0=0x703;
       Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
9759   SPIWrite 00a2,00
9760   SPIWrite 00a1,07
9761   SPIWrite 00a0,03
9762   SPIWrite 0193,2c    //MACRO_OPCODE=0x2c;    Address(0x193[7:0],0x194[7:0])
9763
9764   WAIT 0.001
9765   SPIRead 00f0
9766
9767   //Read  MACRO_DONE=0x1;     Address(0xf0[7:2])
9768
9769
9770   SPIPoll 00f0,2,2,4
9771
9772   SPIRead 00f0
9773
9774   //Read  MACRO_ERROR=0x0;    Address(0xf0[7:3])
9775
9776   SPIRead 00f1
9777
9778   //Read  MACRO_ERROR_OPCODE=0x0;     Address(0xf1[7:0],0xf2[7:0])
9779
9780   SPIRead 00f0
9781
9782   //Read  MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])
9783
9784   SPIRead 00f0
9785
9786   //Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;     Address(0xf0[7:5])
9787
9788   SPIRead 00f0
9789
9790   //Read  MACRO_ERROR_IN_OPERAND=0x0;     Address(0xf0[7:6])
9791
9792   SPIRead 00f0
9793
9794   //Read  MACRO_ERROR_IN_EXECUTION=0x0;   Address(0xf0[7:7])
9795
9796   SPIRead 00f3
9797   SPIRead 00f2
9798
9799   //Read  MACRO_ERROR_EXTENDED_CODE=0x0;  Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
9800
9801   SPIRead 00f7
9802   SPIRead 00f6
```

```
SPIRead 00f5
SPIRead 00f4

//Read  MACRO_ERROR_EXTENDED_CODE_2=0x0;
Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0

//Read  MACRO_READY=0x1;    Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00    //MACRO_OPERAND_REG0=0x301;
Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00
SPIWrite 00a1,03
SPIWrite 00a0,01
SPIWrite 0193,29    //MACRO_OPCODE=0x29;    Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0

//Read  MACRO_DONE=0x1;     Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIRead 00f0

//Read  MACRO_ERROR=0x0;    Address(0xf0[7:3])

SPIRead 00f1

//Read  MACRO_ERROR_OPCODE=0x0;     Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0

//Read  MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0

//Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;     Address(0xf0[7:5])

SPIRead 00f0

//Read  MACRO_ERROR_IN_OPERAND=0x0;     Address(0xf0[7:6])

SPIRead 00f0

//Read  MACRO_ERROR_IN_EXECUTION=0x0;   Address(0xf0[7:7])

SPIRead 00f3
SPIRead 00f2

//Read  MACRO_ERROR_EXTENDED_CODE=0x0;  Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7
SPIRead 00f6
SPIRead 00f5
SPIRead 00f4

//Read  MACRO_ERROR_EXTENDED_CODE_2=0x0;
Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0

//Read  MACRO_READY=0x1;    Address(0xf0[7:0])

```

```
9869
9870   SPIPoll 00f0,0,0,1
9871
9872   SPIWrite 00a3,00    //MACRO_OPERAND_REG0=0x101;
       Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
9873   SPIWrite 00a2,00
9874   SPIWrite 00a1,01
9875   SPIWrite 00a0,01
9876   SPIWrite 0193,23    //MACRO_OPCODE=0x23;    Address(0x193[7:0],0x194[7:0])
9877
9878   WAIT 0.001
9879   SPIRead 00f0
9880
9881   //Read  MACRO_DONE=0x1;     Address(0xf0[7:2])
9882
9883
9884   SPIPoll 00f0,2,2,4
9885
9886   SPIRead 00f0
9887
9888   //Read  MACRO_ERROR=0x0;    Address(0xf0[7:3])
9889
9890   SPIRead 00f1
9891
9892   //Read  MACRO_ERROR_OPCODE=0x0;     Address(0xf1[7:0],0xf2[7:0])
9893
9894   SPIRead 00f0
9895
9896   //Read  MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])
9897
9898   SPIRead 00f0
9899
9900   //Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;     Address(0xf0[7:5])
9901
9902   SPIRead 00f0
9903
9904   //Read  MACRO_ERROR_IN_OPERAND=0x0;     Address(0xf0[7:6])
9905
9906   SPIRead 00f0
9907
9908   //Read  MACRO_ERROR_IN_EXECUTION=0x0;   Address(0xf0[7:7])
9909
9910   SPIRead 00f3
9911   SPIRead 00f2
9912
9913   //Read  MACRO_ERROR_EXTENDED_CODE=0x0;  Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
9914
9915   SPIRead 00f7
9916   SPIRead 00f6
9917   SPIRead 00f5
9918   SPIRead 00f4
9919
9920   //Read  MACRO_ERROR_EXTENDED_CODE_2=0x0;
       Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
9921
9922   SPIRead 00f0
9923
9924   //Read  MACRO_READY=0x1;    Address(0xf0[7:0])
9925
9926
9927   SPIPoll 00f0,0,0,1
9928
9929   SPIWrite 00a3,77    //MACRO_OPERAND_REG0=0x77400001;
       Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
9930   SPIWrite 00a2,40
9931   SPIWrite 00a1,00
9932   SPIWrite 00a0,01
9933   SPIWrite 00a7,ac    //MACRO_OPERAND_REG1=0xac40001b;
       Address(0xa4[7:0],0xa5[7:0],0xa6[7:0],0xa7[7:0],0xa8[7:0])
```

```
SPIWrite 00a6,40
SPIWrite 00a5,00
SPIWrite 00a4,1b
SPIWrite 00ab,77    //MACRO_OPERAND_REG2=0x77400027;
Address(0xa8[7:0],0xa9[7:0],0xaa[7:0],0xab[7:0],0xac[7:0])
SPIWrite 00aa,40
SPIWrite 00a9,00
SPIWrite 00a8,27
SPIWrite 00af,ac    //MACRO_OPERAND_REG3=0xac40001b;
Address(0xac[7:0],0xad[7:0],0xae[7:0],0xaf[7:0],0xb0[7:0])
SPIWrite 00ae,40
SPIWrite 00ad,00
SPIWrite 00ac,1b
SPIWrite 00b3,00    //MACRO_OPERAND_REG4=0x27;
Address(0xb0[7:0],0xb1[7:0],0xb2[7:0],0xb3[7:0],0xb4[7:0])
SPIWrite 00b2,00
SPIWrite 00b1,00
SPIWrite 00b0,27
SPIWrite 0193,31    //MACRO_OPCODE=0x31;    Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0

//Read  MACRO_DONE=0x1;     Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIRead 00f0

//Read  MACRO_ERROR=0x0;    Address(0xf0[7:3])

SPIRead 00f1

//Read  MACRO_ERROR_OPCODE=0x0;     Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0

//Read  MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0

//Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;     Address(0xf0[7:5])

SPIRead 00f0

//Read  MACRO_ERROR_IN_OPERAND=0x0;     Address(0xf0[7:6])

SPIRead 00f0

//Read  MACRO_ERROR_IN_EXECUTION=0x0;   Address(0xf0[7:7])

SPIRead 00f3
SPIRead 00f2

//Read  MACRO_ERROR_EXTENDED_CODE=0x0;  Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7
SPIRead 00f6
SPIRead 00f5
SPIRead 00f4

//Read  MACRO_ERROR_EXTENDED_CODE_2=0x0;
Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0

//Read  MACRO_READY=0x1;    Address(0xf0[7:0])

```

```
 9999
10000   SPIPoll 00f0,0,0,1
10001
10002   SPIWrite 00a3,00    //MACRO_OPERAND_REG0=0x302;
        Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
10003   SPIWrite 00a2,00
10004   SPIWrite 00a1,03
10005   SPIWrite 00a0,02
10006   SPIWrite 0193,29    //MACRO_OPCODE=0x29;    Address(0x193[7:0],0x194[7:0])
10007
10008   WAIT 0.001
10009   SPIRead 00f0
10010
10011   //Read  MACRO_DONE=0x1;     Address(0xf0[7:2])
10012
10013
10014   SPIPoll 00f0,2,2,4
10015
10016   SPIRead 00f0
10017
10018   //Read  MACRO_ERROR=0x0;    Address(0xf0[7:3])
10019
10020   SPIRead 00f1
10021
10022   //Read  MACRO_ERROR_OPCODE=0x0;     Address(0xf1[7:0],0xf2[7:0])
10023
10024   SPIRead 00f0
10025
10026   //Read  MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])
10027
10028   SPIRead 00f0
10029
10030   //Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;     Address(0xf0[7:5])
10031
10032   SPIRead 00f0
10033
10034   //Read  MACRO_ERROR_IN_OPERAND=0x0;     Address(0xf0[7:6])
10035
10036   SPIRead 00f0
10037
10038   //Read  MACRO_ERROR_IN_EXECUTION=0x0;   Address(0xf0[7:7])
10039
10040   SPIRead 00f3
10041   SPIRead 00f2
10042
10043   //Read  MACRO_ERROR_EXTENDED_CODE=0x0;  Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
10044
10045   SPIRead 00f7
10046   SPIRead 00f6
10047   SPIRead 00f5
10048   SPIRead 00f4
10049
10050   //Read  MACRO_ERROR_EXTENDED_CODE_2=0x0;
        Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
10051
10052   SPIRead 00f0
10053
10054   //Read  MACRO_READY=0x1;    Address(0xf0[7:0])
10055
10056
10057   SPIPoll 00f0,0,0,1
10058
10059   SPIWrite 00a3,00    //MACRO_OPERAND_REG0=0x102;
        Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
10060   SPIWrite 00a2,00
10061   SPIWrite 00a1,01
10062   SPIWrite 00a0,02
10063   SPIWrite 0193,23    //MACRO_OPCODE=0x23;    Address(0x193[7:0],0x194[7:0])
10064
```

```
10065   WAIT 0.001
10066   SPIRead 00f0
10067
10068   //Read  MACRO_DONE=0x1;     Address(0xf0[7:2])
10069
10070
10071   SPIPoll 00f0,2,2,4
10072
10073   SPIRead 00f0
10074
10075   //Read  MACRO_ERROR=0x0;    Address(0xf0[7:3])
10076
10077   SPIRead 00f1
10078
10079   //Read  MACRO_ERROR_OPCODE=0x0;     Address(0xf1[7:0],0xf2[7:0])
10080
10081   SPIRead 00f0
10082
10083   //Read  MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])
10084
10085   SPIRead 00f0
10086
10087   //Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;     Address(0xf0[7:5])
10088
10089   SPIRead 00f0
10090
10091   //Read  MACRO_ERROR_IN_OPERAND=0x0;     Address(0xf0[7:6])
10092
10093   SPIRead 00f0
10094
10095   //Read  MACRO_ERROR_IN_EXECUTION=0x0;   Address(0xf0[7:7])
10096
10097   SPIRead 00f3
10098   SPIRead 00f2
10099
10100   //Read  MACRO_ERROR_EXTENDED_CODE=0x0;  Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
10101
10102   SPIRead 00f7
10103   SPIRead 00f6
10104   SPIRead 00f5
10105   SPIRead 00f4
10106
10107   //Read  MACRO_ERROR_EXTENDED_CODE_2=0x0;
       Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
10108
10109   SPIRead 00f0
10110
10111   //Read  MACRO_READY=0x1;    Address(0xf0[7:0])
10112
10113
10114   SPIPoll 00f0,0,0,1
10115
10116   SPIWrite 00a3,77    //MACRO_OPERAND_REG0=0x77400002;
       Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
10117   SPIWrite 00a2,40
10118   SPIWrite 00a1,00
10119   SPIWrite 00a0,02
10120   SPIWrite 00a7,ac    //MACRO_OPERAND_REG1=0xac40001b;
       Address(0xa4[7:0],0xa5[7:0],0xa6[7:0],0xa7[7:0],0xa8[7:0])
10121   SPIWrite 00a6,40
10122   SPIWrite 00a5,00
10123   SPIWrite 00a4,1b
10124   SPIWrite 00ab,77    //MACRO_OPERAND_REG2=0x77400027;
       Address(0xa8[7:0],0xa9[7:0],0xaa[7:0],0xab[7:0],0xac[7:0])
10125   SPIWrite 00aa,40
10126   SPIWrite 00a9,00
10127   SPIWrite 00a8,27
10128   SPIWrite 00af,ac    //MACRO_OPERAND_REG3=0xac40001b;
       Address(0xac[7:0],0xad[7:0],0xae[7:0],0xaf[7:0],0xb0[7:0])
```

```
SPIWrite 00ae,40
SPIWrite 00ad,00
SPIWrite 00ac,1b
SPIWrite 00b3,00    //MACRO_OPERAND_REG4=0x27;
Address(0xb0[7:0],0xb1[7:0],0xb2[7:0],0xb3[7:0],0xb4[7:0])
SPIWrite 00b2,00
SPIWrite 00b1,00
SPIWrite 00b0,27
SPIWrite 0193,31    //MACRO_OPCODE=0x31;    Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0

//Read  MACRO_DONE=0x1;     Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIRead 00f0

//Read  MACRO_ERROR=0x0;    Address(0xf0[7:3])

SPIRead 00f1

//Read  MACRO_ERROR_OPCODE=0x0;     Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0

//Read  MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0

//Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;     Address(0xf0[7:5])

SPIRead 00f0

//Read  MACRO_ERROR_IN_OPERAND=0x0;     Address(0xf0[7:6])

SPIRead 00f0

//Read  MACRO_ERROR_IN_EXECUTION=0x0;   Address(0xf0[7:7])

SPIRead 00f3
SPIRead 00f2

//Read  MACRO_ERROR_EXTENDED_CODE=0x0;  Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7
SPIRead 00f6
SPIRead 00f5
SPIRead 00f4

//Read  MACRO_ERROR_EXTENDED_CODE_2=0x0;
Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0

//Read  MACRO_READY=0x1;    Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00    //MACRO_OPERAND_REG0=0x304;
Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00
SPIWrite 00a1,03
SPIWrite 00a0,04
SPIWrite 0193,29    //MACRO_OPCODE=0x29;    Address(0x193[7:0],0x194[7:0])

```

```
10195   WAIT 0.001
10196   SPIRead 00f0
10197
10198   //Read  MACRO_DONE=0x1;     Address(0xf0[7:2])
10199
10200
10201   SPIPoll 00f0,2,2,4
10202
10203   SPIRead 00f0
10204
10205   //Read  MACRO_ERROR=0x0;    Address(0xf0[7:3])
10206
10207   SPIRead 00f1
10208
10209   //Read  MACRO_ERROR_OPCODE=0x0;     Address(0xf1[7:0],0xf2[7:0])
10210
10211   SPIRead 00f0
10212
10213   //Read  MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])
10214
10215   SPIRead 00f0
10216
10217   //Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;     Address(0xf0[7:5])
10218
10219   SPIRead 00f0
10220
10221   //Read  MACRO_ERROR_IN_OPERAND=0x0;     Address(0xf0[7:6])
10222
10223   SPIRead 00f0
10224
10225   //Read  MACRO_ERROR_IN_EXECUTION=0x0;   Address(0xf0[7:7])
10226
10227   SPIRead 00f3
10228   SPIRead 00f2
10229
10230   //Read  MACRO_ERROR_EXTENDED_CODE=0x0;  Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
10231
10232   SPIRead 00f7
10233   SPIRead 00f6
10234   SPIRead 00f5
10235   SPIRead 00f4
10236
10237   //Read  MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
10238
10239   SPIRead 00f0
10240
10241   //Read  MACRO_READY=0x1;    Address(0xf0[7:0])
10242
10243
10244   SPIPoll 00f0,0,0,1
10245
10246   SPIWrite 00a3,00    //MACRO_OPERAND_REG0=0x104;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
10247   SPIWrite 00a2,00
10248   SPIWrite 00a1,01
10249   SPIWrite 00a0,04
10250   SPIWrite 0193,23    //MACRO_OPCODE=0x23;    Address(0x193[7:0],0x194[7:0])
10251
10252   WAIT 0.001
10253   SPIRead 00f0
10254
10255   //Read  MACRO_DONE=0x1;     Address(0xf0[7:2])
10256
10257
10258   SPIPoll 00f0,2,2,4
10259
10260   SPIRead 00f0
10261
```

```
10262   //Read  MACRO_ERROR=0x0;    Address(0xf0[7:3])
10263
10264   SPIRead 00f1
10265
10266   //Read  MACRO_ERROR_OPCODE=0x0;     Address(0xf1[7:0],0xf2[7:0])
10267
10268   SPIRead 00f0
10269
10270   //Read  MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])
10271
10272   SPIRead 00f0
10273
10274   //Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;     Address(0xf0[7:5])
10275
10276   SPIRead 00f0
10277
10278   //Read  MACRO_ERROR_IN_OPERAND=0x0;     Address(0xf0[7:6])
10279
10280   SPIRead 00f0
10281
10282   //Read  MACRO_ERROR_IN_EXECUTION=0x0;   Address(0xf0[7:7])
10283
10284   SPIRead 00f3
10285   SPIRead 00f2
10286
10287   //Read  MACRO_ERROR_EXTENDED_CODE=0x0;  Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
10288
10289   SPIRead 00f7
10290   SPIRead 00f6
10291   SPIRead 00f5
10292   SPIRead 00f4
10293
10294   //Read  MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
10295
10296   SPIRead 00f0
10297
10298   //Read  MACRO_READY=0x1;    Address(0xf0[7:0])
10299
10300
10301   SPIPoll 00f0,0,0,1
10302
10303   SPIWrite 00a3,77    //MACRO_OPERAND_REG0=0x77400004;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
10304   SPIWrite 00a2,40
10305   SPIWrite 00a1,00
10306   SPIWrite 00a0,04
10307   SPIWrite 00a7,ac    //MACRO_OPERAND_REG1=0xac40001b;
      Address(0xa4[7:0],0xa5[7:0],0xa6[7:0],0xa7[7:0],0xa8[7:0])
10308   SPIWrite 00a6,40
10309   SPIWrite 00a5,00
10310   SPIWrite 00a4,1b
10311   SPIWrite 00ab,77    //MACRO_OPERAND_REG2=0x77400027;
      Address(0xa8[7:0],0xa9[7:0],0xaa[7:0],0xab[7:0],0xac[7:0])
10312   SPIWrite 00aa,40
10313   SPIWrite 00a9,00
10314   SPIWrite 00a8,27
10315   SPIWrite 00af,ac    //MACRO_OPERAND_REG3=0xac40001b;
      Address(0xac[7:0],0xad[7:0],0xae[7:0],0xaf[7:0],0xb0[7:0])
10316   SPIWrite 00ae,40
10317   SPIWrite 00ad,00
10318   SPIWrite 00ac,1b
10319   SPIWrite 00b3,00    //MACRO_OPERAND_REG4=0x27;
      Address(0xb0[7:0],0xb1[7:0],0xb2[7:0],0xb3[7:0],0xb4[7:0])
10320   SPIWrite 00b2,00
10321   SPIWrite 00b1,00
10322   SPIWrite 00b0,27
10323   SPIWrite 0193,31    //MACRO_OPCODE=0x31;    Address(0x193[7:0],0x194[7:0])
10324
```

```
10325   WAIT 0.001
10326   SPIRead 00f0
10327
10328   //Read  MACRO_DONE=0x1;     Address(0xf0[7:2])
10329
10330
10331   SPIPoll 00f0,2,2,4
10332
10333   SPIRead 00f0
10334
10335   //Read  MACRO_ERROR=0x0;    Address(0xf0[7:3])
10336
10337   SPIRead 00f1
10338
10339   //Read  MACRO_ERROR_OPCODE=0x0;     Address(0xf1[7:0],0xf2[7:0])
10340
10341   SPIRead 00f0
10342
10343   //Read  MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])
10344
10345   SPIRead 00f0
10346
10347   //Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;     Address(0xf0[7:5])
10348
10349   SPIRead 00f0
10350
10351   //Read  MACRO_ERROR_IN_OPERAND=0x0;     Address(0xf0[7:6])
10352
10353   SPIRead 00f0
10354
10355   //Read  MACRO_ERROR_IN_EXECUTION=0x0;   Address(0xf0[7:7])
10356
10357   SPIRead 00f3
10358   SPIRead 00f2
10359
10360   //Read  MACRO_ERROR_EXTENDED_CODE=0x0;  Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
10361
10362   SPIRead 00f7
10363   SPIRead 00f6
10364   SPIRead 00f5
10365   SPIRead 00f4
10366
10367   //Read  MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
10368
10369   SPIRead 00f0
10370
10371   //Read  MACRO_READY=0x1;    Address(0xf0[7:0])
10372
10373
10374   SPIPoll 00f0,0,0,1
10375
10376   SPIWrite 00a3,00    //MACRO_OPERAND_REG0=0x308;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
10377   SPIWrite 00a2,00
10378   SPIWrite 00a1,03
10379   SPIWrite 00a0,08
10380   SPIWrite 0193,29    //MACRO_OPCODE=0x29;    Address(0x193[7:0],0x194[7:0])
10381
10382   WAIT 0.001
10383   SPIRead 00f0
10384
10385   //Read  MACRO_DONE=0x1;     Address(0xf0[7:2])
10386
10387
10388   SPIPoll 00f0,2,2,4
10389
10390   SPIRead 00f0
10391
```

```
10392   //Read  MACRO_ERROR=0x0;    Address(0xf0[7:3])
10393
10394   SPIRead 00f1
10395
10396   //Read  MACRO_ERROR_OPCODE=0x0;     Address(0xf1[7:0],0xf2[7:0])
10397
10398   SPIRead 00f0
10399
10400   //Read  MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])
10401
10402   SPIRead 00f0
10403
10404   //Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;     Address(0xf0[7:5])
10405
10406   SPIRead 00f0
10407
10408   //Read  MACRO_ERROR_IN_OPERAND=0x0;     Address(0xf0[7:6])
10409
10410   SPIRead 00f0
10411
10412   //Read  MACRO_ERROR_IN_EXECUTION=0x0;   Address(0xf0[7:7])
10413
10414   SPIRead 00f3
10415   SPIRead 00f2
10416
10417   //Read  MACRO_ERROR_EXTENDED_CODE=0x0;  Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
10418
10419   SPIRead 00f7
10420   SPIRead 00f6
10421   SPIRead 00f5
10422   SPIRead 00f4
10423
10424   //Read  MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
10425
10426   SPIRead 00f0
10427
10428   //Read  MACRO_READY=0x1;    Address(0xf0[7:0])
10429
10430
10431   SPIPoll 00f0,0,0,1
10432
10433   SPIWrite 00a3,00    //MACRO_OPERAND_REG0=0x108;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
10434   SPIWrite 00a2,00
10435   SPIWrite 00a1,01
10436   SPIWrite 00a0,08
10437   SPIWrite 0193,23    //MACRO_OPCODE=0x23;    Address(0x193[7:0],0x194[7:0])
10438
10439   WAIT 0.001
10440   SPIRead 00f0
10441
10442   //Read  MACRO_DONE=0x1;     Address(0xf0[7:2])
10443
10444
10445   SPIPoll 00f0,2,2,4
10446
10447   SPIRead 00f0
10448
10449   //Read  MACRO_ERROR=0x0;    Address(0xf0[7:3])
10450
10451   SPIRead 00f1
10452
10453   //Read  MACRO_ERROR_OPCODE=0x0;     Address(0xf1[7:0],0xf2[7:0])
10454
10455   SPIRead 00f0
10456
10457   //Read  MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])
10458
```

```
10459   SPIRead 00f0
10460
10461   //Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;     Address(0xf0[7:5])
10462
10463   SPIRead 00f0
10464
10465   //Read  MACRO_ERROR_IN_OPERAND=0x0;     Address(0xf0[7:6])
10466
10467   SPIRead 00f0
10468
10469   //Read  MACRO_ERROR_IN_EXECUTION=0x0;   Address(0xf0[7:7])
10470
10471   SPIRead 00f3
10472   SPIRead 00f2
10473
10474   //Read  MACRO_ERROR_EXTENDED_CODE=0x0;  Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
10475
10476   SPIRead 00f7
10477   SPIRead 00f6
10478   SPIRead 00f5
10479   SPIRead 00f4
10480
10481   //Read  MACRO_ERROR_EXTENDED_CODE_2=0x0;
       Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
10482
10483   SPIRead 00f0
10484
10485   //Read  MACRO_READY=0x1;    Address(0xf0[7:0])
10486
10487
10488   SPIPoll 00f0,0,0,1
10489
10490   SPIWrite 00a3,77    //MACRO_OPERAND_REG0=0x77400008;
       Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
10491   SPIWrite 00a2,40
10492   SPIWrite 00a1,00
10493   SPIWrite 00a0,08
10494   SPIWrite 00a7,ac    //MACRO_OPERAND_REG1=0xac40001b;
       Address(0xa4[7:0],0xa5[7:0],0xa6[7:0],0xa7[7:0],0xa8[7:0])
10495   SPIWrite 00a6,40
10496   SPIWrite 00a5,00
10497   SPIWrite 00a4,1b
10498   SPIWrite 00ab,77    //MACRO_OPERAND_REG2=0x77400027;
       Address(0xa8[7:0],0xa9[7:0],0xaa[7:0],0xab[7:0],0xac[7:0])
10499   SPIWrite 00aa,40
10500   SPIWrite 00a9,00
10501   SPIWrite 00a8,27
10502   SPIWrite 00af,ac    //MACRO_OPERAND_REG3=0xac40001b;
       Address(0xac[7:0],0xad[7:0],0xae[7:0],0xaf[7:0],0xb0[7:0])
10503   SPIWrite 00ae,40
10504   SPIWrite 00ad,00
10505   SPIWrite 00ac,1b
10506   SPIWrite 00b3,00    //MACRO_OPERAND_REG4=0x27;
       Address(0xb0[7:0],0xb1[7:0],0xb2[7:0],0xb3[7:0],0xb4[7:0])
10507   SPIWrite 00b2,00
10508   SPIWrite 00b1,00
10509   SPIWrite 00b0,27
10510   SPIWrite 0193,31    //MACRO_OPCODE=0x31;    Address(0x193[7:0],0x194[7:0])
10511
10512   WAIT 0.001
10513   SPIRead 00f0
10514
10515   //Read  MACRO_DONE=0x1;     Address(0xf0[7:2])
10516
10517
10518   SPIPoll 00f0,2,2,4
10519
10520   SPIRead 00f0
10521
```

```
10522   //Read  MACRO_ERROR=0x0;    Address(0xf0[7:3])
10523
10524   SPIRead 00f1
10525
10526   //Read  MACRO_ERROR_OPCODE=0x0;     Address(0xf1[7:0],0xf2[7:0])
10527
10528   SPIRead 00f0
10529
10530   //Read  MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])
10531
10532   SPIRead 00f0
10533
10534   //Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;     Address(0xf0[7:5])
10535
10536   SPIRead 00f0
10537
10538   //Read  MACRO_ERROR_IN_OPERAND=0x0;     Address(0xf0[7:6])
10539
10540   SPIRead 00f0
10541
10542   //Read  MACRO_ERROR_IN_EXECUTION=0x0;   Address(0xf0[7:7])
10543
10544   SPIRead 00f3
10545   SPIRead 00f2
10546
10547   //Read  MACRO_ERROR_EXTENDED_CODE=0x0;  Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
10548
10549   SPIRead 00f7
10550   SPIRead 00f6
10551   SPIRead 00f5
10552   SPIRead 00f4
10553
10554   //Read  MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
10555
10556
10557   //END: Configuring RX Chain Parameters to TOP MCU
10558
10559   SPIWrite 0018,00    //macro=0x0;    Address(0x18[7:5])
10560
10561   //STEP: sysConfig/step2
10562
10563   //START: Configuring FB Chain Parameters to TOP MCU
10564
10565   SPIWrite 0018,20    //macro=0x1;    Address(0x18[7:5])
10566   SPIRead 00f0
10567
10568   //Read  MACRO_READY=0x1;    Address(0xf0[7:0])
10569
10570
10571   SPIPoll 00f0,0,0,1
10572
10573   SPIWrite 00a3,00    //MACRO_OPERAND_REG0=0x701;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
10574   SPIWrite 00a2,00
10575   SPIWrite 00a1,07
10576   SPIWrite 00a0,01
10577   SPIWrite 0193,2d    //MACRO_OPCODE=0x2d;    Address(0x193[7:0],0x194[7:0])
10578
10579   WAIT 0.001
10580   SPIRead 00f0
10581
10582   //Read  MACRO_DONE=0x1;     Address(0xf0[7:2])
10583
10584
10585   SPIPoll 00f0,2,2,4
10586
10587   SPIRead 00f0
10588
```

```
10589   //Read  MACRO_ERROR=0x0;    Address(0xf0[7:3])
10590
10591   SPIRead 00f1
10592
10593   //Read  MACRO_ERROR_OPCODE=0x0;     Address(0xf1[7:0],0xf2[7:0])
10594
10595   SPIRead 00f0
10596
10597   //Read  MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])
10598
10599   SPIRead 00f0
10600
10601   //Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;     Address(0xf0[7:5])
10602
10603   SPIRead 00f0
10604
10605   //Read  MACRO_ERROR_IN_OPERAND=0x0;     Address(0xf0[7:6])
10606
10607   SPIRead 00f0
10608
10609   //Read  MACRO_ERROR_IN_EXECUTION=0x0;   Address(0xf0[7:7])
10610
10611   SPIRead 00f3
10612   SPIRead 00f2
10613
10614   //Read  MACRO_ERROR_EXTENDED_CODE=0x0;  Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
10615
10616   SPIRead 00f7
10617   SPIRead 00f6
10618   SPIRead 00f5
10619   SPIRead 00f4
10620
10621   //Read  MACRO_ERROR_EXTENDED_CODE_2=0x0;
       Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
10622
10623   SPIRead 00f0
10624
10625   //Read  MACRO_READY=0x1;    Address(0xf0[7:0])
10626
10627
10628   SPIPoll 00f0,0,0,1
10629
10630   SPIWrite 00a3,00    //MACRO_OPERAND_REG0=0x501;
       Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
10631   SPIWrite 00a2,00
10632   SPIWrite 00a1,05
10633   SPIWrite 00a0,01
10634   SPIWrite 0193,2a    //MACRO_OPCODE=0x2a;    Address(0x193[7:0],0x194[7:0])
10635
10636   WAIT 0.001
10637   SPIRead 00f0
10638
10639   //Read  MACRO_DONE=0x1;     Address(0xf0[7:2])
10640
10641
10642   SPIPoll 00f0,2,2,4
10643
10644   SPIRead 00f0
10645
10646   //Read  MACRO_ERROR=0x0;    Address(0xf0[7:3])
10647
10648   SPIRead 00f1
10649
10650   //Read  MACRO_ERROR_OPCODE=0x0;     Address(0xf1[7:0],0xf2[7:0])
10651
10652   SPIRead 00f0
10653
10654   //Read  MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])
10655
```

```
10656   SPIRead 00f0
10657
10658   //Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;     Address(0xf0[7:5])
10659
10660   SPIRead 00f0
10661
10662   //Read  MACRO_ERROR_IN_OPERAND=0x0;     Address(0xf0[7:6])
10663
10664   SPIRead 00f0
10665
10666   //Read  MACRO_ERROR_IN_EXECUTION=0x0;   Address(0xf0[7:7])
10667
10668   SPIRead 00f3
10669   SPIRead 00f2
10670
10671   //Read  MACRO_ERROR_EXTENDED_CODE=0x0;  Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
10672
10673   SPIRead 00f7
10674   SPIRead 00f6
10675   SPIRead 00f5
10676   SPIRead 00f4
10677
10678   //Read  MACRO_ERROR_EXTENDED_CODE_2=0x0;
       Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
10679
10680   SPIRead 00f0
10681
10682   //Read  MACRO_READY=0x1;    Address(0xf0[7:0])
10683
10684
10685   SPIPoll 00f0,0,0,1
10686
10687   SPIWrite 00a3,77    //MACRO_OPERAND_REG0=0x77400001;
       Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
10688   SPIWrite 00a2,40
10689   SPIWrite 00a1,00
10690   SPIWrite 00a0,01
10691   SPIWrite 00a7,00    //MACRO_OPERAND_REG1=0x1b;
       Address(0xa4[7:0],0xa5[7:0],0xa6[7:0],0xa7[7:0],0xa8[7:0])
10692   SPIWrite 00a6,00
10693   SPIWrite 00a5,00
10694   SPIWrite 00a4,1b
10695   SPIWrite 0193,32    //MACRO_OPCODE=0x32;    Address(0x193[7:0],0x194[7:0])
10696
10697   WAIT 0.001
10698   SPIRead 00f0
10699
10700   //Read  MACRO_DONE=0x1;     Address(0xf0[7:2])
10701
10702
10703   SPIPoll 00f0,2,2,4
10704
10705   SPIRead 00f0
10706
10707   //Read  MACRO_ERROR=0x0;    Address(0xf0[7:3])
10708
10709   SPIRead 00f1
10710
10711   //Read  MACRO_ERROR_OPCODE=0x0;     Address(0xf1[7:0],0xf2[7:0])
10712
10713   SPIRead 00f0
10714
10715   //Read  MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])
10716
10717   SPIRead 00f0
10718
10719   //Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;     Address(0xf0[7:5])
10720
10721   SPIRead 00f0
```

```
10722
10723   //Read  MACRO_ERROR_IN_OPERAND=0x0;     Address(0xf0[7:6])
10724
10725   SPIRead 00f0
10726
10727   //Read  MACRO_ERROR_IN_EXECUTION=0x0;   Address(0xf0[7:7])
10728
10729   SPIRead 00f3
10730   SPIRead 00f2
10731
10732   //Read  MACRO_ERROR_EXTENDED_CODE=0x0;  Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
10733
10734   SPIRead 00f7
10735   SPIRead 00f6
10736   SPIRead 00f5
10737   SPIRead 00f4
10738
10739   //Read  MACRO_ERROR_EXTENDED_CODE_2=0x0;
       Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
10740
10741   SPIRead 00f0
10742
10743   //Read  MACRO_READY=0x1;    Address(0xf0[7:0])
10744
10745
10746   SPIPoll 00f0,0,0,1
10747
10748   SPIWrite 00a3,00    //MACRO_OPERAND_REG0=0x502;
       Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
10749   SPIWrite 00a2,00
10750   SPIWrite 00a1,05
10751   SPIWrite 00a0,02
10752   SPIWrite 0193,2a    //MACRO_OPCODE=0x2a;    Address(0x193[7:0],0x194[7:0])
10753
10754   WAIT 0.001
10755   SPIRead 00f0
10756
10757   //Read  MACRO_DONE=0x1;     Address(0xf0[7:2])
10758
10759
10760   SPIPoll 00f0,2,2,4
10761
10762   SPIRead 00f0
10763
10764   //Read  MACRO_ERROR=0x0;    Address(0xf0[7:3])
10765
10766   SPIRead 00f1
10767
10768   //Read  MACRO_ERROR_OPCODE=0x0;     Address(0xf1[7:0],0xf2[7:0])
10769
10770   SPIRead 00f0
10771
10772   //Read  MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])
10773
10774   SPIRead 00f0
10775
10776   //Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;     Address(0xf0[7:5])
10777
10778   SPIRead 00f0
10779
10780   //Read  MACRO_ERROR_IN_OPERAND=0x0;     Address(0xf0[7:6])
10781
10782   SPIRead 00f0
10783
10784   //Read  MACRO_ERROR_IN_EXECUTION=0x0;   Address(0xf0[7:7])
10785
10786   SPIRead 00f3
10787   SPIRead 00f2
10788
```

```
10789   //Read  MACRO_ERROR_EXTENDED_CODE=0x0;  Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
10790
10791   SPIRead 00f7
10792   SPIRead 00f6
10793   SPIRead 00f5
10794   SPIRead 00f4
10795
10796   //Read  MACRO_ERROR_EXTENDED_CODE_2=0x0;
        Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
10797
10798   SPIRead 00f0
10799
10800   //Read  MACRO_READY=0x1;    Address(0xf0[7:0])
10801
10802
10803   SPIPoll 00f0,0,0,1
10804
10805   SPIWrite 00a3,77    //MACRO_OPERAND_REG0=0x77400002;
        Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
10806   SPIWrite 00a2,40
10807   SPIWrite 00a1,00
10808   SPIWrite 00a0,02
10809   SPIWrite 00a7,00    //MACRO_OPERAND_REG1=0x1b;
        Address(0xa4[7:0],0xa5[7:0],0xa6[7:0],0xa7[7:0],0xa8[7:0])
10810   SPIWrite 00a6,00
10811   SPIWrite 00a5,00
10812   SPIWrite 00a4,1b
10813   SPIWrite 0193,32    //MACRO_OPCODE=0x32;    Address(0x193[7:0],0x194[7:0])
10814
10815   WAIT 0.001
10816   SPIRead 00f0
10817
10818   //Read  MACRO_DONE=0x1;     Address(0xf0[7:2])
10819
10820
10821   SPIPoll 00f0,2,2,4
10822
10823   SPIRead 00f0
10824
10825   //Read  MACRO_ERROR=0x0;    Address(0xf0[7:3])
10826
10827   SPIRead 00f1
10828
10829   //Read  MACRO_ERROR_OPCODE=0x0;     Address(0xf1[7:0],0xf2[7:0])
10830
10831   SPIRead 00f0
10832
10833   //Read  MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])
10834
10835   SPIRead 00f0
10836
10837   //Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;     Address(0xf0[7:5])
10838
10839   SPIRead 00f0
10840
10841   //Read  MACRO_ERROR_IN_OPERAND=0x0;     Address(0xf0[7:6])
10842
10843   SPIRead 00f0
10844
10845   //Read  MACRO_ERROR_IN_EXECUTION=0x0;   Address(0xf0[7:7])
10846
10847   SPIRead 00f3
10848   SPIRead 00f2
10849
10850   //Read  MACRO_ERROR_EXTENDED_CODE=0x0;  Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
10851
10852   SPIRead 00f7
10853   SPIRead 00f6
10854   SPIRead 00f5
```

```
SPIRead 00f4

//Read  MACRO_ERROR_EXTENDED_CODE_2=0x0;
Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])


//END: Configuring FB Chain Parameters to TOP MCU

SPIWrite 0018,00    //macro=0x0;    Address(0x18[7:5])

//STEP: sysConfig/step3

//START: Configuring TX Chain Parameters to TOP MCU

SPIWrite 0018,20    //macro=0x1;    Address(0x18[7:5])
SPIRead 00f0

//Read  MACRO_READY=0x1;    Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00    //MACRO_OPERAND_REG0=0x0;
Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00
SPIWrite 00a1,00
SPIWrite 00a0,00
SPIWrite 0193,8d    //MACRO_OPCODE=0x8d;    Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0

//Read  MACRO_DONE=0x1;     Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIRead 00f0

//Read  MACRO_ERROR=0x0;    Address(0xf0[7:3])

SPIRead 00f1

//Read  MACRO_ERROR_OPCODE=0x0;     Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0

//Read  MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0

//Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;     Address(0xf0[7:5])

SPIRead 00f0

//Read  MACRO_ERROR_IN_OPERAND=0x0;     Address(0xf0[7:6])

SPIRead 00f0

//Read  MACRO_ERROR_IN_EXECUTION=0x0;   Address(0xf0[7:7])

SPIRead 00f3
SPIRead 00f2

//Read  MACRO_ERROR_EXTENDED_CODE=0x0;  Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7
SPIRead 00f6
SPIRead 00f5
```

```
SPIRead 00f4

//Read  MACRO_ERROR_EXTENDED_CODE_2=0x0;
Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0

//Read  MACRO_READY=0x1;    Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00    //MACRO_OPERAND_REG0=0xc03;
Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00
SPIWrite 00a1,0c
SPIWrite 00a0,03
SPIWrite 0193,2e    //MACRO_OPCODE=0x2e;    Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0

//Read  MACRO_DONE=0x1;     Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIRead 00f0

//Read  MACRO_ERROR=0x0;    Address(0xf0[7:3])

SPIRead 00f1

//Read  MACRO_ERROR_OPCODE=0x0;     Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0

//Read  MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0

//Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;     Address(0xf0[7:5])

SPIRead 00f0

//Read  MACRO_ERROR_IN_OPERAND=0x0;     Address(0xf0[7:6])

SPIRead 00f0

//Read  MACRO_ERROR_IN_EXECUTION=0x0;   Address(0xf0[7:7])

SPIRead 00f3
SPIRead 00f2

//Read  MACRO_ERROR_EXTENDED_CODE=0x0;  Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7
SPIRead 00f6
SPIRead 00f5
SPIRead 00f4

//Read  MACRO_ERROR_EXTENDED_CODE_2=0x0;
Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0

//Read  MACRO_READY=0x1;    Address(0xf0[7:0])


```

```
SPIPoll 00f0,0,0,1

SPIWrite 00a3,00    //MACRO_OPERAND_REG0=0x50f;
Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00
SPIWrite 00a1,05
SPIWrite 00a0,0f
SPIWrite 0193,2b    //MACRO_OPCODE=0x2b;    Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0

//Read  MACRO_DONE=0x1;     Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIRead 00f0

//Read  MACRO_ERROR=0x0;    Address(0xf0[7:3])

SPIRead 00f1

//Read  MACRO_ERROR_OPCODE=0x0;     Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0

//Read  MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0

//Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;     Address(0xf0[7:5])

SPIRead 00f0

//Read  MACRO_ERROR_IN_OPERAND=0x0;     Address(0xf0[7:6])

SPIRead 00f0

//Read  MACRO_ERROR_IN_EXECUTION=0x0;   Address(0xf0[7:7])

SPIRead 00f3
SPIRead 00f2

//Read  MACRO_ERROR_EXTENDED_CODE=0x0;  Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7
SPIRead 00f6
SPIRead 00f5
SPIRead 00f4

//Read  MACRO_ERROR_EXTENDED_CODE_2=0x0;
Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0

//Read  MACRO_READY=0x1;    Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00    //MACRO_OPERAND_REG0=0x1f0;
Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00
SPIWrite 00a1,01
SPIWrite 00a0,f0
SPIWrite 0193,23    //MACRO_OPCODE=0x23;    Address(0x193[7:0],0x194[7:0])

WAIT 0.001
```

```
11054   SPIRead 00f0
11055
11056   //Read  MACRO_DONE=0x1;     Address(0xf0[7:2])
11057
11058
11059   SPIPoll 00f0,2,2,4
11060
11061   SPIRead 00f0
11062
11063   //Read  MACRO_ERROR=0x0;    Address(0xf0[7:3])
11064
11065   SPIRead 00f1
11066
11067   //Read  MACRO_ERROR_OPCODE=0x0;     Address(0xf1[7:0],0xf2[7:0])
11068
11069   SPIRead 00f0
11070
11071   //Read  MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])
11072
11073   SPIRead 00f0
11074
11075   //Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;     Address(0xf0[7:5])
11076
11077   SPIRead 00f0
11078
11079   //Read  MACRO_ERROR_IN_OPERAND=0x0;     Address(0xf0[7:6])
11080
11081   SPIRead 00f0
11082
11083   //Read  MACRO_ERROR_IN_EXECUTION=0x0;   Address(0xf0[7:7])
11084
11085   SPIRead 00f3
11086   SPIRead 00f2
11087
11088   //Read  MACRO_ERROR_EXTENDED_CODE=0x0;  Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
11089
11090   SPIRead 00f7
11091   SPIRead 00f6
11092   SPIRead 00f5
11093   SPIRead 00f4
11094
11095   //Read  MACRO_ERROR_EXTENDED_CODE_2=0x0;
       Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
11096
11097   SPIRead 00f0
11098
11099   //Read  MACRO_READY=0x1;    Address(0xf0[7:0])
11100
11101
11102   SPIPoll 00f0,0,0,1
11103
11104   SPIWrite 00a3,77    //MACRO_OPERAND_REG0=0x7740000f;
       Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
11105   SPIWrite 00a2,40
11106   SPIWrite 00a1,00
11107   SPIWrite 00a0,0f
11108   SPIWrite 00a7,ac    //MACRO_OPERAND_REG1=0xac40001b;
       Address(0xa4[7:0],0xa5[7:0],0xa6[7:0],0xa7[7:0],0xa8[7:0])
11109   SPIWrite 00a6,40
11110   SPIWrite 00a5,00
11111   SPIWrite 00a4,1b
11112   SPIWrite 00ab,77    //MACRO_OPERAND_REG2=0x77400027;
       Address(0xa8[7:0],0xa9[7:0],0xaa[7:0],0xab[7:0],0xac[7:0])
11113   SPIWrite 00aa,40
11114   SPIWrite 00a9,00
11115   SPIWrite 00a8,27
11116   SPIWrite 00af,ac    //MACRO_OPERAND_REG3=0xac40001b;
       Address(0xac[7:0],0xad[7:0],0xae[7:0],0xaf[7:0],0xb0[7:0])
11117   SPIWrite 00ae,40
```

```
SPIWrite 00ad,00
SPIWrite 00ac,1b
SPIWrite 00b3,00    //MACRO_OPERAND_REG4=0x27;
Address(0xb0[7:0],0xb1[7:0],0xb2[7:0],0xb3[7:0],0xb4[7:0])
SPIWrite 00b2,00
SPIWrite 00b1,00
SPIWrite 00b0,27
SPIWrite 0193,30    //MACRO_OPCODE=0x30;    Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0

//Read  MACRO_DONE=0x1;     Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIRead 00f0

//Read  MACRO_ERROR=0x0;    Address(0xf0[7:3])

SPIRead 00f1

//Read  MACRO_ERROR_OPCODE=0x0;     Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0

//Read  MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0

//Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;     Address(0xf0[7:5])

SPIRead 00f0

//Read  MACRO_ERROR_IN_OPERAND=0x0;     Address(0xf0[7:6])

SPIRead 00f0

//Read  MACRO_ERROR_IN_EXECUTION=0x0;   Address(0xf0[7:7])

SPIRead 00f3
SPIRead 00f2

//Read  MACRO_ERROR_EXTENDED_CODE=0x0;  Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7
SPIRead 00f6
SPIRead 00f5
SPIRead 00f4

//Read  MACRO_ERROR_EXTENDED_CODE_2=0x0;
Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])


//END: Configuring TX Chain Parameters to TOP MCU

SPIWrite 0018,00    //macro=0x0;    Address(0x18[7:5])

//STEP: configTune/step0

//START: Configuring Digital Chain

SPIWrite 0018,20    //macro=0x1;    Address(0x18[7:5])
SPIRead 00f0

//Read  MACRO_READY=0x1;    Address(0xf0[7:0])


```

```
SPIPoll 00f0,0,0,1

SPIWrite 00a3,00    //MACRO_OPERAND_REG0=0xf1f;
Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00
SPIWrite 00a1,0f
SPIWrite 00a0,1f
SPIWrite 0193,36    //MACRO_OPCODE=0x36;    Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0

//Read  MACRO_DONE=0x1;     Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIRead 00f0

//Read  MACRO_ERROR=0x0;    Address(0xf0[7:3])

SPIRead 00f1

//Read  MACRO_ERROR_OPCODE=0x0;     Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0

//Read  MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0

//Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;     Address(0xf0[7:5])

SPIRead 00f0

//Read  MACRO_ERROR_IN_OPERAND=0x0;     Address(0xf0[7:6])

SPIRead 00f0

//Read  MACRO_ERROR_IN_EXECUTION=0x0;   Address(0xf0[7:7])

SPIRead 00f3
SPIRead 00f2

//Read  MACRO_ERROR_EXTENDED_CODE=0x0;  Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7
SPIRead 00f6
SPIRead 00f5
SPIRead 00f4

//Read  MACRO_ERROR_EXTENDED_CODE_2=0x0;
Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])


//END: Configuring Digital Chain

SPIWrite 0018,00    //macro=0x0;    Address(0x18[7:5])

//STEP: configTune/step1

//START: Setting FIFO Pointers

SPIWrite 0012,01    //rxdig=0x1;    Address(0x12[7:0])
SPIWrite 0060,46    //async_fifo_ptr_offset_p0=0x6;     Address(0x60[7:0])
SPIWrite 0060,66    //async_fifo_ptr_offset_p1=0x6;     Address(0x60[7:4])
SPIWrite 0061,46    //async_fifo_ptr_offset_p2=0x6;     Address(0x61[7:0])
SPIWrite 0061,66    //async_fifo_ptr_offset_p3=0x6;     Address(0x61[7:4])
SPIWrite 0012,02    //rxdig=0x2;    Address(0x12[7:0])
```

```
11252   SPIWrite 0060,46    //async_fifo_ptr_offset_p0=0x6;     Address(0x60[7:0])
11253   SPIWrite 0060,66    //async_fifo_ptr_offset_p1=0x6;     Address(0x60[7:4])
11254   SPIWrite 0061,46    //async_fifo_ptr_offset_p2=0x6;     Address(0x61[7:0])
11255   SPIWrite 0061,66    //async_fifo_ptr_offset_p3=0x6;     Address(0x61[7:4])
11256   SPIWrite 0012,04    //rxdig=0x4;    Address(0x12[7:0])
11257   SPIWrite 0060,46    //async_fifo_ptr_offset_p0=0x6;     Address(0x60[7:0])
11258   SPIWrite 0060,66    //async_fifo_ptr_offset_p1=0x6;     Address(0x60[7:4])
11259   SPIWrite 0061,46    //async_fifo_ptr_offset_p2=0x6;     Address(0x61[7:0])
11260   SPIWrite 0061,66    //async_fifo_ptr_offset_p3=0x6;     Address(0x61[7:4])
11261   SPIWrite 0012,08    //rxdig=0x8;    Address(0x12[7:0])
11262   SPIWrite 0060,46    //async_fifo_ptr_offset_p0=0x6;     Address(0x60[7:0])
11263   SPIWrite 0060,66    //async_fifo_ptr_offset_p1=0x6;     Address(0x60[7:4])
11264   SPIWrite 0061,46    //async_fifo_ptr_offset_p2=0x6;     Address(0x61[7:0])
11265   SPIWrite 0061,66    //async_fifo_ptr_offset_p3=0x6;     Address(0x61[7:4])
11266   SPIWrite 0012,00    //rxdig=0x0;    Address(0x12[7:0])
11267   SPIWrite 0012,10    //fbdig=0x1;    Address(0x12[7:4])
11268   SPIWrite 0060,46    //async_fifo_ptr_offset_p0=0x6;     Address(0x60[7:0])
11269   SPIWrite 0060,66    //async_fifo_ptr_offset_p1=0x6;     Address(0x60[7:4])
11270   SPIWrite 0061,46    //async_fifo_ptr_offset_p2=0x6;     Address(0x61[7:0])
11271   SPIWrite 0061,66    //async_fifo_ptr_offset_p3=0x6;     Address(0x61[7:4])
11272   SPIWrite 0012,20    //fbdig=0x2;    Address(0x12[7:4])
11273   SPIWrite 0060,46    //async_fifo_ptr_offset_p0=0x6;     Address(0x60[7:0])
11274   SPIWrite 0060,66    //async_fifo_ptr_offset_p1=0x6;     Address(0x60[7:4])
11275   SPIWrite 0061,46    //async_fifo_ptr_offset_p2=0x6;     Address(0x61[7:0])
11276   SPIWrite 0061,66    //async_fifo_ptr_offset_p3=0x6;     Address(0x61[7:4])
11277   SPIWrite 0012,00    //fbdig=0x0;    Address(0x12[7:4])
11278   SPIWrite 0019,10    //txdig=0x1;    Address(0x19[7:4])
11279   SPIWrite 0062,06    //cfg_rd_ptr_out_async_fifo=0x6;    Address(0x62[7:0])
11280   SPIWrite 0019,20    //txdig=0x2;    Address(0x19[7:4])
11281   SPIWrite 0062,06    //cfg_rd_ptr_out_async_fifo=0x6;    Address(0x62[7:0])
11282   SPIWrite 0019,40    //txdig=0x4;    Address(0x19[7:4])
11283   SPIWrite 0062,06    //cfg_rd_ptr_out_async_fifo=0x6;    Address(0x62[7:0])
11284   SPIWrite 0019,80    //txdig=0x8;    Address(0x19[7:4])
11285   SPIWrite 0062,06    //cfg_rd_ptr_out_async_fifo=0x6;    Address(0x62[7:0])
11286   SPIWrite 0019,10    //txdig=0x1;    Address(0x19[7:4])
11287   SPIWrite 0060,00    //cfg_wr_ptr_async_fifo_offset_val=0x0;     Address(0x60[7:0])
11288   SPIWrite 0019,20    //txdig=0x2;    Address(0x19[7:4])
11289   SPIWrite 0060,00    //cfg_wr_ptr_async_fifo_offset_val=0x0;     Address(0x60[7:0])
11290   SPIWrite 0019,40    //txdig=0x4;    Address(0x19[7:4])
11291   SPIWrite 0060,00    //cfg_wr_ptr_async_fifo_offset_val=0x0;     Address(0x60[7:0])
11292   SPIWrite 0019,80    //txdig=0x8;    Address(0x19[7:4])
11293   SPIWrite 0060,00    //cfg_wr_ptr_async_fifo_offset_val=0x0;     Address(0x60[7:0])
11294   SPIWrite 0019,00    //txdig=0x0;    Address(0x19[7:4])
11295   SPIWrite 0016,10    //jesd_subchip=0x1;     Address(0x16[7:4])
11296   SPIWrite 0030,8c    //rxa_afifo_offset=0xc;     Address(0x30[7:0])
11297   SPIWrite 0030,cc    //rxb_afifo_offset=0xc;     Address(0x30[7:4])
11298   SPIWrite 0031,8c    //rxc_afifo_offset=0xc;     Address(0x31[7:0])
11299   SPIWrite 0031,cc    //rxd_afifo_offset=0xc;     Address(0x31[7:4])
11300   SPIWrite 0032,80    //fba_afifo_offset=0x0;     Address(0x32[7:0])
11301   SPIWrite 0032,00    //fbc_afifo_offset=0x0;     Address(0x32[7:4])
11302
11303   //END: Setting FIFO Pointers
11304
11305   SPIWrite 0016,00    //jesd_subchip=0x0;     Address(0x16[7:4])
11306   SPIWrite 0018,20    //macro=0x1;    Address(0x18[7:5])
11307   SPIRead 00f0
11308
11309   //Read  MACRO_READY=0x1;    Address(0xf0[7:0])
11310
11311
11312   SPIPoll 00f0,0,0,1
11313
11314   SPIWrite 0193,3d    //MACRO_OPCODE=0x3d;    Address(0x193[7:0],0x194[7:0])
11315
11316   WAIT 0.001
11317   SPIRead 00f0
11318
11319   //Read  MACRO_DONE=0x1;     Address(0xf0[7:2])
11320
```

```
11321
11322   SPIPoll 00f0,2,2,4
11323
11324   SPIRead 00f0
11325
11326   //Read  MACRO_ERROR=0x0;    Address(0xf0[7:3])
11327
11328   SPIRead 00f1
11329
11330   //Read  MACRO_ERROR_OPCODE=0x0;     Address(0xf1[7:0],0xf2[7:0])
11331
11332   SPIRead 00f0
11333
11334   //Read  MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])
11335
11336   SPIRead 00f0
11337
11338   //Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;     Address(0xf0[7:5])
11339
11340   SPIRead 00f0
11341
11342   //Read  MACRO_ERROR_IN_OPERAND=0x0;     Address(0xf0[7:6])
11343
11344   SPIRead 00f0
11345
11346   //Read  MACRO_ERROR_IN_EXECUTION=0x0;   Address(0xf0[7:7])
11347
11348   SPIRead 00f3
11349   SPIRead 00f2
11350
11351   //Read  MACRO_ERROR_EXTENDED_CODE=0x0;  Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
11352
11353   SPIRead 00f7
11354   SPIRead 00f6
11355   SPIRead 00f5
11356   SPIRead 00f4
11357
11358   //Read  MACRO_ERROR_EXTENDED_CODE_2=0x0;
       Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
11359
11360   SPIWrite 0018,00    //macro=0x0;    Address(0x18[7:5])
11361
11362   //STEP: analogWrites/step0
11363   SPIWrite 0011,3f    //ec_ana=0x3f;  Address(0x11[7:0])
11364   SPIWrite 0075,00    //NCTRL_CTRL=0x6;   Address(0x75[7:7],0x76[7:0])
11365   SPIWrite 0076,03
11366   SPIWrite 0071,04    //TRIM_VR_LATPP=0x2;    Address(0x71[7:1])
11367   SPIWrite 0071,14    //PK_MEASURE_CC=0x1;    Address(0x71[7:4])
11368   SPIWrite 0084,80    //INV_PF_CTRL=0xe;  Address(0x84[7:6],0x85[7:0])
11369   SPIWrite 0085,03
11370   SPIWrite 0011,00    //ec_ana=0x0;   Address(0x11[7:0])
11371   SPIWrite 0018,20    //macro=0x1;    Address(0x18[7:5])
11372   SPIRead 00f0
11373
11374   //Read  MACRO_READY=0x1;    Address(0xf0[7:0])
11375
11376
11377   SPIPoll 00f0,0,0,1
11378
11379   SPIWrite 00a3,00    //MACRO_OPERAND_REG0=0x124;
       Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
11380   SPIWrite 00a2,00
11381   SPIWrite 00a1,01
11382   SPIWrite 00a0,24
11383   SPIWrite 0193,72    //MACRO_OPCODE=0x72;    Address(0x193[7:0],0x194[7:0])
11384
11385   WAIT 0.001
11386   SPIRead 00f0
11387
```

```
11388   //Read  MACRO_DONE=0x1;     Address(0xf0[7:2])
11389
11390
11391   SPIPoll 00f0,2,2,4
11392
11393   SPIRead 00f0
11394
11395   //Read  MACRO_ERROR=0x0;    Address(0xf0[7:3])
11396
11397   SPIRead 00f1
11398
11399   //Read  MACRO_ERROR_OPCODE=0x0;     Address(0xf1[7:0],0xf2[7:0])
11400
11401   SPIRead 00f0
11402
11403   //Read  MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])
11404
11405   SPIRead 00f0
11406
11407   //Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;     Address(0xf0[7:5])
11408
11409   SPIRead 00f0
11410
11411   //Read  MACRO_ERROR_IN_OPERAND=0x0;     Address(0xf0[7:6])
11412
11413   SPIRead 00f0
11414
11415   //Read  MACRO_ERROR_IN_EXECUTION=0x0;   Address(0xf0[7:7])
11416
11417   SPIRead 00f3
11418   SPIRead 00f2
11419
11420   //Read  MACRO_ERROR_EXTENDED_CODE=0x0;  Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
11421
11422   SPIRead 00f7
11423   SPIRead 00f6
11424   SPIRead 00f5
11425   SPIRead 00f4
11426
11427   //Read  MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
11428
11429   SPIRead 00f0
11430
11431   //Read  MACRO_READY=0x1;    Address(0xf0[7:0])
11432
11433
11434   SPIPoll 00f0,0,0,1
11435
11436   SPIWrite 00a3,01    //MACRO_OPERAND_REG0=0x1000600;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
11437   SPIWrite 00a2,00
11438   SPIWrite 00a1,06
11439   SPIWrite 00a0,00
11440   SPIWrite 00a7,05    //MACRO_OPERAND_REG1=0x5040302;
      Address(0xa4[7:0],0xa5[7:0],0xa6[7:0],0xa7[7:0],0xa8[7:0])
11441   SPIWrite 00a6,04
11442   SPIWrite 00a5,03
11443   SPIWrite 00a4,02
11444   SPIWrite 0193,71    //MACRO_OPCODE=0x71;    Address(0x193[7:0],0x194[7:0])
11445
11446   WAIT 0.001
11447   SPIRead 00f0
11448
11449   //Read  MACRO_DONE=0x1;     Address(0xf0[7:2])
11450
11451
11452   SPIPoll 00f0,2,2,4
11453
```

```
11454   SPIRead 00f0
11455
11456   //Read  MACRO_ERROR=0x0;    Address(0xf0[7:3])
11457
11458   SPIRead 00f1
11459
11460   //Read  MACRO_ERROR_OPCODE=0x0;     Address(0xf1[7:0],0xf2[7:0])
11461
11462   SPIRead 00f0
11463
11464   //Read  MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])
11465
11466   SPIRead 00f0
11467
11468   //Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;     Address(0xf0[7:5])
11469
11470   SPIRead 00f0
11471
11472   //Read  MACRO_ERROR_IN_OPERAND=0x0;     Address(0xf0[7:6])
11473
11474   SPIRead 00f0
11475
11476   //Read  MACRO_ERROR_IN_EXECUTION=0x0;   Address(0xf0[7:7])
11477
11478   SPIRead 00f3
11479   SPIRead 00f2
11480
11481   //Read  MACRO_ERROR_EXTENDED_CODE=0x0;  Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
11482
11483   SPIRead 00f7
11484   SPIRead 00f6
11485   SPIRead 00f5
11486   SPIRead 00f4
11487
11488   //Read  MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
11489
11490   SPIWrite 0018,00    //macro=0x0;    Address(0x18[7:5])
11491   SPIWrite 0011,3f    //ec_ana=0x3f;  Address(0x11[7:0])
11492   SPIWrite 0060,01    //TM_DLL_RESET=0x1;     Address(0x60[7:0])
11493   SPIWrite 0060,00    //TM_DLL_RESET=0x0;     Address(0x60[7:0])
11494   SPIWrite 0011,00    //ec_ana=0x0;   Address(0x11[7:0])
11495
11496   //STEP: analogWrites/step1
11497
11498   //START: Removing TDD Pin Overrides.
11499
11500   SPIWrite 0015,80    //timing_controller=0x1;    Address(0x15[7:7])
11501   SPIWrite 00ed,00    //reg_for_rxtdd=0x0;    Address(0xed[7:0])
11502   SPIWrite 00f5,00    //reg_for_fbtdd=0x0;    Address(0xf5[7:0])
11503   SPIWrite 00e5,0f    //reg_for_txtdd=0xf;    Address(0xe5[7:0])
11504
11505   //END: Removing TDD Pin Overrides.
11506
11507
11508   //START: DAC Analog Writes
11509
11510   SPIWrite 0015,00    //timing_controller=0x0;    Address(0x15[7:7])
11511   SPIWrite 0013,0f    //txdh=0xf;     Address(0x13[7:0])
11512   SPIWrite 015a,20    //po_ppa_corr_pdn=0x1;  Address(0x15a[7:5])
11513   SPIWrite 01bd,00    //po_ana_spare8=0x1;    Address(0x1bc[7:0],0x1bd[7:0],0x1be[7:0])
11514   SPIWrite 01bc,01
11515   SPIWrite 015a,22    //po_ppa_pdn=0x1;   Address(0x15a[7:1])
11516   SPIWrite 0070,27    //dsa_dac_decode1_th1=0x27;     Address(0x70[7:0])
11517   SPIWrite 0071,27    //dsa_dac_decode1_th2=0x27;     Address(0x71[7:0])
11518   SPIWrite 0072,27    //dsa_dac_decode1_th3=0x27;     Address(0x72[7:0])
11519   SPIWrite 0074,27    //dsa_dac_decode2_th1=0x27;     Address(0x74[7:0])
11520   SPIWrite 0075,27    //dsa_dac_decode2_th2=0x27;     Address(0x75[7:0])
11521   SPIWrite 0076,27    //dsa_dac_decode2_th3=0x27;     Address(0x76[7:0])
```

```
SPIWrite 0078,27    //dsa_dac_decode3_th1=0x27;     Address(0x78[7:0])
SPIWrite 0079,27    //dsa_dac_decode3_th2=0x27;     Address(0x79[7:0])
SPIWrite 007a,27    //dsa_dac_decode3_th3=0x27;     Address(0x7a[7:0])
SPIWrite 015a,26    //po_caldac_ldo_pdn=0x1;    Address(0x15a[7:2])
SPIWrite 015a,26    //po_caldac_ldo_pdn=0x1;    Address(0x15a[7:2])
SPIWrite 0025,00    //twos_complement_mode=0x0;     Address(0x25[7:0])
SPIWrite 015a,27    //po_cg_pdn=0x1;    Address(0x15a[7:0])
SPIWrite 0168,01    //po_dac1_common_resetz=0x1;    Address(0x168[7:0])
SPIWrite 017c,01    //po_dac2_common_resetz=0x1;    Address(0x17c[7:0])
SPIWrite 01b1,00    //po_ana_spare5=0x10;   Address(0x1b0[7:0],0x1b1[7:0],0x1b2[7:0])
SPIWrite 01b0,10
SPIWrite 0158,01    //po_caldac1_pdn=0x1;   Address(0x158[7:0])
SPIWrite 0159,01    //po_caldac2_pdn=0x1;   Address(0x159[7:0])
SPIWrite 0177,00    //po_dac1_enc_tm_lv=0x800000001;
Address(0x174[7:0],0x175[7:0],0x176[7:0],0x177[7:0],0x178[7:0],0x178[7:0])
SPIWrite 0176,00
SPIWrite 0175,00
SPIWrite 0174,01
SPIWrite 0178,08
SPIWrite 018b,00    //po_dac2_enc_tm_lv=0x800000001;
Address(0x188[7:0],0x189[7:0],0x18a[7:0],0x18b[7:0],0x18c[7:0],0x18c[7:0])
SPIWrite 018a,00
SPIWrite 0189,00
SPIWrite 0188,01
SPIWrite 018c,08
SPIWrite 011a,00    //po_dac1_tm=0x0;   Address(0x118[4:0],0x119[4:0],0x11a[7:0])
SPIWrite 0119,00
SPIWrite 0118,00
SPIWrite 0126,00    //po_dac2_tm=0x0;   Address(0x124[4:0],0x125[4:0],0x126[7:0])
SPIWrite 0125,00
SPIWrite 0124,00
SPIWrite 01c5,3d    //po_ana_spare10=0x3de0;    Address(0x1c4[7:0],0x1c5[7:0],0x1c6[7:0])
SPIWrite 01c4,e0
SPIWrite 0133,00    //po_ppa_tm=0x1fe0;
Address(0x130[7:0],0x131[7:0],0x132[7:0],0x133[7:0],0x134[7:0],0x134[6:0],0x135[7:0])
SPIWrite 0132,00
SPIWrite 0131,1f
SPIWrite 0130,e0
SPIWrite 0135,00
SPIWrite 0134,00
SPIWrite 0029,00    //dh_lsb_xor_enc=0x0;   Address(0x29[7:0])
SPIWrite 018e,01    //po_en_lsb_xor=0x1;    Address(0x18e[7:0])
SPIWrite 0112,00    //po_cml_tm=0x0;    Address(0x110[2:0],0x111[2:0],0x112[7:0])
SPIWrite 0111,00
SPIWrite 0110,00
SPIWrite 0151,0e    //po_mix_delay_prog=0xed3;  Address(0x150[7:0],0x151[7:0],0x152[7:0])
SPIWrite 0150,d3
SPIWrite 01ad,00    //po_ana_spare4=0xff;   Address(0x1ac[7:0],0x1ad[7:0],0x1ae[7:0])
SPIWrite 01ac,ff
SPIWrite 0162,00    //po_dac1_clk_prog=0x0;     Address(0x162[7:0])
SPIWrite 0163,00    //po_dac2_clk_prog=0x0;     Address(0x163[7:0])
SPIWrite 0013,00    //txdh=0x0;     Address(0x13[7:0])

//START: Requesting/releasing SPI Access to PLL Pages

SPIWrite 0015,40    //digtop=0x1;   Address(0x15[7:6])
SPIWrite 0170,01    //pll_reg_spi_req_a=0x1;    Address(0x170[7:0])
SPIWrite 0540,00    //pll_reg_spi_req_b1=0x0;   Address(0x540[7:0])

SPIPoll 0171,0,0,01
SPIRead 0171

//Read  pll_reg_spi_a_ack=0x1(Meaning: );;  Address(0x171[7:0])


//END: Requesting/releasing SPI Access to PLL Pages

SPIWrite 0015,00    //digtop=0x0;   Address(0x15[7:6])
SPIWrite 0014,ff    //txcalib=0xff;     Address(0x14[7:0],0x15[7:0])
```

```
SPIWrite 0119,00    //caldac_spare=0x1;     Address(0x118[7:0],0x119[7:0],0x11a[7:0])
SPIWrite 0118,01

WAIT 0.1
SPIWrite 0119,00    //caldac_spare=0x0;     Address(0x118[7:0],0x119[7:0],0x11a[7:0])
SPIWrite 0118,00

//START: Requesting/releasing SPI Access to PLL Pages

SPIWrite 0014,00    //txcalib=0x0;  Address(0x14[7:0],0x15[7:0])
SPIWrite 0015,40    //digtop=0x1;   Address(0x15[7:6])
SPIWrite 0170,00    //pll_reg_spi_req_a=0x0;    Address(0x170[7:0])
SPIWrite 0540,00    //pll_reg_spi_req_b1=0x0;   Address(0x540[7:0])

WAIT 0.2

//END: Requesting/releasing SPI Access to PLL Pages

SPIWrite 0015,00    //digtop=0x0;   Address(0x15[7:6])
SPIWrite 0019,f0    //txdig=0xf;    Address(0x19[7:4])
SPIWrite 07d3,01    //EnDacDataRandomization=0x1;   Address(0x7d3[7:0])
SPIWrite 0019,00    //txdig=0x0;    Address(0x19[7:4])
SPIWrite 0019,f0    //txdig=0xf;    Address(0x19[7:4])
SPIWrite 0320,00    //dither_freq_shift_ctrl0=0x0;  Address(0x320[7:0])
SPIWrite 0019,00    //txdig=0x0;    Address(0x19[7:4])
SPIWrite 0013,01    //txdh=0x1;     Address(0x13[7:0])
SPIWrite 0107,f0    //po_cg_tm=0xf0000040;
Address(0x104[7:0],0x105[7:0],0x106[7:0],0x107[7:0],0x108[7:0],0x108[3:0],0x109[3:0],0x10
a[7:0])
SPIWrite 0106,00
SPIWrite 0105,00
SPIWrite 0104,40
SPIWrite 010a,00
SPIWrite 0109,00
SPIWrite 0108,00
SPIWrite 0013,02    //txdh=0x2;     Address(0x13[7:0])
SPIWrite 0107,f0    //po_cg_tm=0xf0000040;
Address(0x104[7:0],0x105[7:0],0x106[7:0],0x107[7:0],0x108[7:0],0x108[3:0],0x109[3:0],0x10
a[7:0])
SPIWrite 0106,00
SPIWrite 0105,00
SPIWrite 0104,40
SPIWrite 010a,00
SPIWrite 0109,00
SPIWrite 0108,00
SPIWrite 0013,04    //txdh=0x4;     Address(0x13[7:0])
SPIWrite 0107,f0    //po_cg_tm=0xf0000040;
Address(0x104[7:0],0x105[7:0],0x106[7:0],0x107[7:0],0x108[7:0],0x108[3:0],0x109[3:0],0x10
a[7:0])
SPIWrite 0106,00
SPIWrite 0105,00
SPIWrite 0104,40
SPIWrite 010a,00
SPIWrite 0109,00
SPIWrite 0108,00
SPIWrite 0013,08    //txdh=0x8;     Address(0x13[7:0])
SPIWrite 0107,f0    //po_cg_tm=0xf0000040;
Address(0x104[7:0],0x105[7:0],0x106[7:0],0x107[7:0],0x108[7:0],0x108[3:0],0x109[3:0],0x10
a[7:0])
SPIWrite 0106,00
SPIWrite 0105,00
SPIWrite 0104,40
SPIWrite 010a,00
SPIWrite 0109,00
SPIWrite 0108,00
SPIWrite 0013,0f    //txdh=0xf;     Address(0x13[7:0])
SPIWrite 0024,00    //data_handoff_mode=0x0;    Address(0x24[7:0])
SPIWrite 0013,00    //txdh=0x0;     Address(0x13[7:0])
SPIWrite 0019,f0    //txdig=0xf;    Address(0x19[7:4])
```

```
11649   SPIWrite 030c,01    //nyq_sel=0x1;  Address(0x30c[7:0])
11650   SPIWrite 0019,00    //txdig=0x0;    Address(0x19[7:4])
11651   SPIWrite 0013,0f    //txdh=0xf;     Address(0x13[7:0])
11652   SPIWrite 011a,00    //po_dac1_tm=0x2000;    Address(0x118[4:0],0x119[4:0],0x11a[7:0])
11653   SPIWrite 0119,20
11654   SPIWrite 0118,00
11655   SPIWrite 0126,00    //po_dac2_tm=0x2000;    Address(0x124[4:0],0x125[4:0],0x126[7:0])
11656   SPIWrite 0125,20
11657   SPIWrite 0124,00
11658   SPIWrite 015a,25    //po_ppa_pdn=0x0;   Address(0x15a[7:1])
11659   SPIWrite 0013,00    //txdh=0x0;     Address(0x13[7:0])
11660   SPIWrite 0015,80    //timing_controller=0x1;    Address(0x15[7:7])
11661   SPIWrite 00fd,01    //config_rise_xx_A_0=0x180;
       Address(0xfc[7:0],0xfd[7:0],0xfe[7:0])
11662   SPIWrite 00fc,80
11663   SPIWrite 0101,01    //config_rise_xx_A_1=0x180;
       Address(0x100[7:0],0x101[7:0],0x102[7:0])
11664   SPIWrite 0100,80
11665   SPIWrite 019d,01    //config_rise_xx_A_0=0x180;
       Address(0x19c[7:0],0x19d[7:0],0x19e[7:0])
11666   SPIWrite 019c,80
11667   SPIWrite 01a1,01    //config_rise_xx_A_1=0x180;
       Address(0x1a0[7:0],0x1a1[7:0],0x1a2[7:0])
11668   SPIWrite 01a0,80
11669   SPIWrite 023d,01    //config_rise_xx_A_0=0x180;
       Address(0x23c[7:0],0x23d[7:0],0x23e[7:0])
11670   SPIWrite 023c,80
11671   SPIWrite 0241,01    //config_rise_xx_A_1=0x180;
       Address(0x240[7:0],0x241[7:0],0x242[7:0])
11672   SPIWrite 0240,80
11673   SPIWrite 02dd,01    //config_rise_xx_A_0=0x180;
       Address(0x2dc[7:0],0x2dd[7:0],0x2de[7:0])
11674   SPIWrite 02dc,80
11675   SPIWrite 02e1,01    //config_rise_xx_A_1=0x180;
       Address(0x2e0[7:0],0x2e1[7:0],0x2e2[7:0])
11676   SPIWrite 02e0,80
11677   SPIWrite 0135,0c    //config_rise_xx_A_14=0xc00;
       Address(0x134[7:0],0x135[7:0],0x136[7:0])
11678   SPIWrite 0134,00
11679   SPIWrite 01d5,0c    //config_rise_xx_A_14=0xc00;
       Address(0x1d4[7:0],0x1d5[7:0],0x1d6[7:0])
11680   SPIWrite 01d4,00
11681   SPIWrite 0275,0c    //config_rise_xx_A_14=0xc00;
       Address(0x274[7:0],0x275[7:0],0x276[7:0])
11682   SPIWrite 0274,00
11683   SPIWrite 0315,0c    //config_rise_xx_A_14=0xc00;
       Address(0x314[7:0],0x315[7:0],0x316[7:0])
11684   SPIWrite 0314,00
11685   SPIWrite 0015,00    //timing_controller=0x0;    Address(0x15[7:7])
11686   SPIWrite 0013,0f    //txdh=0xf;     Address(0x13[7:0])
11687   SPIWrite 0167,02    //po_mask_tdd=0x2000000;
       Address(0x164[3:0],0x165[3:0],0x166[3:0],0x167[7:0])
11688   SPIWrite 0166,00
11689   SPIWrite 0165,00
11690   SPIWrite 0164,00
11691   SPIWrite 01b1,00    //po_ana_spare5=0x30;   Address(0x1b0[7:0],0x1b1[7:0],0x1b2[7:0])
11692   SPIWrite 01b0,30
11693   SPIWrite 0112,01    //po_cml_tm=0x10000;    Address(0x110[2:0],0x111[2:0],0x112[7:0])
11694   SPIWrite 0111,00
11695   SPIWrite 0110,00
11696   SPIWrite 0013,00    //txdh=0x0;     Address(0x13[7:0])
11697
11698   //END: DAC Analog Writes
11699
11700   SPIWrite 0018,20    //macro=0x1;    Address(0x18[7:5])
11701   SPIRead 00f0
11702
11703   //Read  MACRO_READY=0x1;    Address(0xf0[7:0])
11704
```

```
11705
11706   SPIPoll 00f0,0,0,1
11707
11708   SPIWrite 00a3,0a    //MACRO_OPERAND_REG0=0xa040414;
        Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
11709   SPIWrite 00a2,04
11710   SPIWrite 00a1,04
11711   SPIWrite 00a0,14
11712   SPIWrite 00a7,1f    //MACRO_OPERAND_REG1=0x1f010100;
        Address(0xa4[7:0],0xa5[7:0],0xa6[7:0],0xa7[7:0],0xa8[7:0])
11713   SPIWrite 00a6,01
11714   SPIWrite 00a5,01
11715   SPIWrite 00a4,00
11716   SPIWrite 00ab,03    //MACRO_OPERAND_REG2=0x303041f;
        Address(0xa8[7:0],0xa9[7:0],0xaa[7:0],0xab[7:0],0xac[7:0])
11717   SPIWrite 00aa,03
11718   SPIWrite 00a9,04
11719   SPIWrite 00a8,1f
11720   SPIWrite 00af,00    //MACRO_OPERAND_REG3=0x101;
        Address(0xac[7:0],0xad[7:0],0xae[7:0],0xaf[7:0],0xb0[7:0])
11721   SPIWrite 00ae,00
11722   SPIWrite 00ad,01
11723   SPIWrite 00ac,01
11724   SPIWrite 0193,88    //MACRO_OPCODE=0x88;    Address(0x193[7:0],0x194[7:0])
11725
11726   WAIT 0.001
11727   SPIRead 00f0
11728
11729   //Read  MACRO_DONE=0x1;     Address(0xf0[7:2])
11730
11731
11732   SPIPoll 00f0,2,2,4
11733
11734   SPIRead 00f0
11735
11736   //Read  MACRO_ERROR=0x0;    Address(0xf0[7:3])
11737
11738   SPIRead 00f1
11739
11740   //Read  MACRO_ERROR_OPCODE=0x0;     Address(0xf1[7:0],0xf2[7:0])
11741
11742   SPIRead 00f0
11743
11744   //Read  MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])
11745
11746   SPIRead 00f0
11747
11748   //Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;     Address(0xf0[7:5])
11749
11750   SPIRead 00f0
11751
11752   //Read  MACRO_ERROR_IN_OPERAND=0x0;     Address(0xf0[7:6])
11753
11754   SPIRead 00f0
11755
11756   //Read  MACRO_ERROR_IN_EXECUTION=0x0;   Address(0xf0[7:7])
11757
11758   SPIRead 00f3
11759   SPIRead 00f2
11760
11761   //Read  MACRO_ERROR_EXTENDED_CODE=0x0;  Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
11762
11763   SPIRead 00f7
11764   SPIRead 00f6
11765   SPIRead 00f5
11766   SPIRead 00f4
11767
11768   //Read  MACRO_ERROR_EXTENDED_CODE_2=0x0;
        Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
```

```
11769
11770   SPIRead 00f0
11771
11772   //Read  MACRO_READY=0x1;    Address(0xf0[7:0])
11773
11774
11775   SPIPoll 00f0,0,0,1
11776
11777   SPIWrite 00a3,00    //MACRO_OPERAND_REG0=0x0;
        Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
11778   SPIWrite 00a2,00
11779   SPIWrite 00a1,00
11780   SPIWrite 00a0,00
11781   SPIWrite 0193,90    //MACRO_OPCODE=0x90;    Address(0x193[7:0],0x194[7:0])
11782
11783   WAIT 0.001
11784   SPIRead 00f0
11785
11786   //Read  MACRO_DONE=0x1;     Address(0xf0[7:2])
11787
11788
11789   SPIPoll 00f0,2,2,4
11790
11791   SPIRead 00f0
11792
11793   //Read  MACRO_ERROR=0x0;    Address(0xf0[7:3])
11794
11795   SPIRead 00f1
11796
11797   //Read  MACRO_ERROR_OPCODE=0x0;     Address(0xf1[7:0],0xf2[7:0])
11798
11799   SPIRead 00f0
11800
11801   //Read  MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])
11802
11803   SPIRead 00f0
11804
11805   //Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;     Address(0xf0[7:5])
11806
11807   SPIRead 00f0
11808
11809   //Read  MACRO_ERROR_IN_OPERAND=0x0;     Address(0xf0[7:6])
11810
11811   SPIRead 00f0
11812
11813   //Read  MACRO_ERROR_IN_EXECUTION=0x0;   Address(0xf0[7:7])
11814
11815   SPIRead 00f3
11816   SPIRead 00f2
11817
11818   //Read  MACRO_ERROR_EXTENDED_CODE=0x0;  Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
11819
11820   SPIRead 00f7
11821   SPIRead 00f6
11822   SPIRead 00f5
11823   SPIRead 00f4
11824
11825   //Read  MACRO_ERROR_EXTENDED_CODE_2=0x0;
        Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
11826
11827   SPIWrite 0144,08    //all_addr_high=0x2;    Address(0x144[7:2])
11828   SPIWrite 0018,00    //macro=0x0;    Address(0x18[7:5])
11829   SPIWrite 0018,08    //cm4top_dram=0x1;  Address(0x18[7:3])
11830   SPIWrite 1f96,00
11831   SPIWrite 0018,00    //cm4top_dram=0x0;  Address(0x18[7:3])
11832   SPIWrite 0018,20    //macro=0x1;    Address(0x18[7:5])
11833   SPIRead 00f0
11834
11835   //Read  MACRO_READY=0x1;    Address(0xf0[7:0])
```

```
11836
11837
11838   SPIPoll 00f0,0,0,1
11839
11840   SPIWrite 00a3,00    //MACRO_OPERAND_REG0=0x1;
        Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
11841   SPIWrite 00a2,00
11842   SPIWrite 00a1,00
11843   SPIWrite 00a0,01
11844   SPIWrite 0193,90    //MACRO_OPCODE=0x90;    Address(0x193[7:0],0x194[7:0])
11845
11846   WAIT 0.001
11847   SPIRead 00f0
11848
11849   //Read  MACRO_DONE=0x1;     Address(0xf0[7:2])
11850
11851
11852   SPIPoll 00f0,2,2,4
11853
11854   SPIRead 00f0
11855
11856   //Read  MACRO_ERROR=0x0;    Address(0xf0[7:3])
11857
11858   SPIRead 00f1
11859
11860   //Read  MACRO_ERROR_OPCODE=0x0;     Address(0xf1[7:0],0xf2[7:0])
11861
11862   SPIRead 00f0
11863
11864   //Read  MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])
11865
11866   SPIRead 00f0
11867
11868   //Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;     Address(0xf0[7:5])
11869
11870   SPIRead 00f0
11871
11872   //Read  MACRO_ERROR_IN_OPERAND=0x0;     Address(0xf0[7:6])
11873
11874   SPIRead 00f0
11875
11876   //Read  MACRO_ERROR_IN_EXECUTION=0x0;   Address(0xf0[7:7])
11877
11878   SPIRead 00f3
11879   SPIRead 00f2
11880
11881   //Read  MACRO_ERROR_EXTENDED_CODE=0x0;  Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
11882
11883   SPIRead 00f7
11884   SPIRead 00f6
11885   SPIRead 00f5
11886   SPIRead 00f4
11887
11888   //Read  MACRO_ERROR_EXTENDED_CODE_2=0x0;
        Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
11889
11890
11891   //START: Configuring AUX ADC
11892
11893   SPIWrite 0018,00    //macro=0x0;    Address(0x18[7:5])
11894   SPIWrite 0015,02    //ana_4t4r=0x1;     Address(0x15[7:1])
11895   SPIWrite 00c0,c0    //EN_CLK_SAR=0x1;   Address(0xc0[7:6])
11896   SPIWrite 0015,00    //ana_4t4r=0x0;     Address(0x15[7:1])
11897   SPIWrite 0015,40    //digtop=0x1;   Address(0x15[7:6])
11898   SPIWrite 0500,01    //auxadc_powerup=0x1;   Address(0x500[7:0])
11899   SPIWrite 0500,01    //auxadc_en_conv=0x0;   Address(0x500[7:1])
11900   SPIWrite 0500,09    //auxadc_soft_reset=0x1;    Address(0x500[7:3])
11901   SPIWrite 0506,01    //auxadc_sar_bit_mode=0x1;  Address(0x506[7:0])
11902   SPIWrite 0502,00    //auxadc_INP_MUX=0x0;   Address(0x502[7:5])
```

```
11903   SPIWrite 0502,00    //auxadc_INM_MUX=0x0;   Address(0x502[7:2])
11904   SPIWrite 0501,08    //auxadc_clk_div=0x1;   Address(0x501[7:3])
11905   SPIWrite 0501,0a    //auxadc_duty_cycle_clk=0x2;    Address(0x501[7:0])
11906   SPIWrite 0508,00    //auxadc_offset_estim_phase_en=0x0;     Address(0x508[7:5])
11907   SPIWrite 0505,a0    //auxadc_sar_averaging=0x5;     Address(0x505[7:5])
11908   SPIWrite 0505,a1    //auxadc_sar_logic_niter=0x1;   Address(0x505[7:0])
11909   SPIWrite 0506,05    //auxadc_inp_buf_chop=0x2;  Address(0x506[7:1])
11910   SPIWrite 0506,15    //auxadc_incm_buf_chop=0x2;     Address(0x506[7:3])
11911   SPIWrite 0506,15    //auxadc_inp_buf_mux_ctrl=0x0;  Address(0x506[7:5])
11912   SPIWrite 0505,a1    //auxadc_sar_logic_state_start=0x0;     Address(0x505[7:2])
11913   SPIWrite 0508,00    //auxadc_offset_data_out=0x0;   Address(0x508[7:6])
11914   SPIWrite 0508,00    //auxadc_offsetvalue_force_en=0x0;  Address(0x508[7:4])
11915   SPIWrite 0503,00    //auxadc_inp_res_term_imeas=0x0;    Address(0x503[7:6])
11916   SPIWrite 0502,00    //auxadc_preamp_curr_prog=0x0;  Address(0x502[7:0])
11917
11918   WAIT 0.01
11919   SPIWrite 0500,01    //auxadc_soft_reset=0x0;    Address(0x500[7:3])
11920
11921   WAIT 0.01
11922   SPIWrite 0500,03    //auxadc_en_conv=0x1;   Address(0x500[7:1])
11923
11924   //END: Configuring AUX ADC
11925
11926   SPIWrite 0015,00    //digtop=0x0;   Address(0x15[7:6])
11927
11928   //STEP: analogWrites/step2
11929
11930   //START: Removing TDD Pin Overrides.
11931
11932   SPIWrite 0015,80    //timing_controller=0x1;    Address(0x15[7:7])
11933   SPIWrite 00ed,0f    //reg_for_rxtdd=0xf;    Address(0xed[7:0])
11934   SPIWrite 00f5,00    //reg_for_fbtdd=0x0;    Address(0xf5[7:0])
11935   SPIWrite 00e5,00    //reg_for_txtdd=0x0;    Address(0xe5[7:0])
11936
11937   //END: Removing TDD Pin Overrides.
11938
11939   SPIWrite 0015,00    //timing_controller=0x0;    Address(0x15[7:7])
11940   SPIWrite 0018,20    //macro=0x1;    Address(0x18[7:5])
11941   SPIRead 00f0
11942
11943   //Read  MACRO_READY=0x1;    Address(0xf0[7:0])
11944
11945
11946   SPIPoll 00f0,0,0,1
11947
11948   SPIWrite 00a3,00    //MACRO_OPERAND_REG0=0x36;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
11949   SPIWrite 00a2,00
11950   SPIWrite 00a1,00
11951   SPIWrite 00a0,36
11952   SPIWrite 0193,16    //MACRO_OPCODE=0x16;    Address(0x193[7:0],0x194[7:0])
11953
11954   WAIT 0.2
11955   SPIRead 00f0
11956
11957   //Read  MACRO_DONE=0x0;     Address(0xf0[7:2])
11958
11959   SPIRead 00f0
11960
11961   //Read  MACRO_DONE=0x0;     Address(0xf0[7:2])
11962
11963   SPIRead 00f0
11964
11965   //Read  MACRO_DONE=0x1;     Address(0xf0[7:2])
11966
11967
11968   SPIPoll 00f0,2,2,4
11969
11970   SPIRead 00f0
```

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11971
11972   //Read  MACRO_ERROR=0x0;    Address(0xf0[7:3])
11973
11974   SPIRead 00f1
11975
11976   //Read  MACRO_ERROR_OPCODE=0x0;     Address(0xf1[7:0],0xf2[7:0])
11977
11978   SPIRead 00f0
11979
11980   //Read  MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])
11981
11982   SPIRead 00f0
11983
11984   //Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;     Address(0xf0[7:5])
11985
11986   SPIRead 00f0
11987
11988   //Read  MACRO_ERROR_IN_OPERAND=0x0;     Address(0xf0[7:6])
11989
11990   SPIRead 00f0
11991
11992   //Read  MACRO_ERROR_IN_EXECUTION=0x0;   Address(0xf0[7:7])
11993
11994   SPIRead 00f3
11995   SPIRead 00f2
11996
11997   //Read  MACRO_ERROR_EXTENDED_CODE=0x0;  Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
11998
11999   SPIRead 00f7
12000   SPIRead 00f6
12001   SPIRead 00f5
12002   SPIRead 00f4
12003
12004   //Read  MACRO_ERROR_EXTENDED_CODE_2=0x0;
       Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
12005
12006   SPIWrite 0018,00    //macro=0x0;    Address(0x18[7:5])
12007   SPIWrite 0011,3f    //ec_ana=0x3f;  Address(0x11[7:0])
12008   SPIWrite 0063,80    //SYNC_DIVBY2_LATCHEDGE_FLIPZ=0x1;  Address(0x63[7:7])
12009   SPIWrite 0067,10    //VREF_PK_DET=0x1;  Address(0x67[7:4])
12010   SPIWrite 0077,0c    //PCTRL_CTRL=0x6;   Address(0x77[7:1])
12011   SPIWrite 0076,53    //INVNEG_NF_CTRL=0x5;   Address(0x76[7:4])
12012   SPIWrite 0082,80    //POS_REF_CTRL=0x2;     Address(0x82[7:6])
12013   SPIWrite 0082,a0    //VREF_CTRL=0x4;    Address(0x82[7:3])
12014   SPIWrite 0081,30    //NEG_REF_CTRL=0x3;     Address(0x81[7:4])
12015   SPIWrite 0086,c0    //INV_NF_CTRL=0xe;  Address(0x86[7:5],0x87[7:0])
12016   SPIWrite 0087,01
12017   SPIWrite 0084,85    //INVNEG_PF_CTRL=0x5;   Address(0x84[7:0])
12018   SPIWrite 0087,05    //TRIM_VF_LATP2=0x2;    Address(0x87[7:1])
12019   SPIWrite 00f9,00    //INTR_80N_NL_DITH_DAC_LARGE=0xc;   Address(0xf9[7:7],0xfa[7:0])
12020   SPIWrite 00fa,06
12021   SPIWrite 00e8,80    //CONST_200N_D2S_0=0x4;     Address(0xe8[7:5])
12022   SPIWrite 014e,01    //PRG_V1P4_REG_SP=0x1;  Address(0x14e[7:0])
12023   SPIWrite 014d,1c    //PRG_V0P4_REG_SP=0x7;  Address(0x14d[7:2])
12024   SPIWrite 014c,20    //PRG_FLREG_1V=0x4;     Address(0x14c[7:3])
12025   SPIWrite 0138,18    //TM_ANA_DITH_FL=0x3;   Address(0x138[7:3])
12026   SPIWrite 013e,40    //DIS_CM_SW_1P8V=0x1;   Address(0x13e[7:6])
12027   SPIWrite 004a,60    //ITRIM_CORRREFM_BE=0x6;    Address(0x4a[7:4])
12028   SPIWrite 0049,80    //ITRIM_CORRREFP_BE=0x6;    Address(0x49[7:6],0x4a[7:0])
12029   SPIWrite 004a,61
12030   SPIWrite 00c2,c0    //ITRIM_CORRREFM_FE=0x6;    Address(0xc2[7:5])
12031   SPIWrite 00c1,60    //ITRIM_CORRREFP_FE=0x6;    Address(0xc1[7:4])
12032   SPIWrite 00b6,0c    //DEL_1V=0x3;   Address(0xb6[7:2])
12033   SPIWrite 004f,0c    //DEL_1V=0x3;   Address(0x4f[7:2])
12034   SPIWrite 012e,80    //RES_SER_SEL_REL_1P8=0x7;  Address(0x12e[7:7],0x12f[7:0])
12035   SPIWrite 012f,03
12036   SPIWrite 012e,f0    //RES_SER_SEL_CUST_1P8=0x7;     Address(0x12e[7:4])
12037   SPIWrite 012f,03    //RES_BIAS_SEL_1P8=0x0;     Address(0x12f[7:2])
12038   SPIWrite 0011,00    //ec_ana=0x0;   Address(0x11[7:0])
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12039   SPIWrite 0010,3f    //ec_dig=0x3f;  Address(0x10[7:0])
12040   SPIWrite 00c1,5a    //nl_ana_dith_val=0x5a;     Address(0xc1[7:0])
12041   SPIWrite 0078,60    //s2_therm_ms_loop_en=0x0;  Address(0x78[7:7])
12042   SPIWrite 00c0,17    //nl_therm_ms_loop_en=0x0;  Address(0xc0[7:3])
12043   SPIWrite 00d5,00    //s1_g_pattern_del=0x0;     Address(0xd5[7:0])
12044   SPIWrite 00d5,08    //s1_m_pattern_del=0x2;     Address(0xd5[7:2])
12045   SPIWrite 0150,30    //dir_pu=0x0;   Address(0x150[7:3])
12046   SPIWrite 00f8,51    //calib_seq_avg=0xa8c0c5051;
        Address(0xf8[7:0],0xf9[7:0],0xf9[7:0],0xfa[7:0],0xfa[7:0],0xfb[7:0],0xfb[7:0],0xfc[7:0],0
        xfc[7:0],0xfd[7:0])
12047   SPIWrite 00f9,50
12048   SPIWrite 00fa,0c
12049   SPIWrite 00fb,8c
12050   SPIWrite 00fc,0a
12051   SPIWrite 0168,02    //freeze_pu=0x1;    Address(0x168[7:1])
12052   SPIWrite 00ef,08    //s1_ad_pu_unfreeze_loops=0x0;  Address(0xef[7:6])
12053   SPIWrite 0178,71    //dir_corr=0x1;     Address(0x178[7:4])
12054   SPIWrite 0075,b5    //s1_sat_del_en=0x1;    Address(0x75[7:4])
12055   SPIWrite 0168,06    //reset=0x1;    Address(0x168[7:2])
12056   SPIWrite 0168,02    //reset=0x0;    Address(0x168[7:2])
12057   SPIWrite 0169,bb    //avg_bg=0xb;   Address(0x169[7:0])
12058   SPIWrite 0074,7a    //s1_metastab_table_dis=0x0;    Address(0x74[7:7])
12059   SPIWrite 013c,fe    //dir_lower=0x6bfffe;
        Address(0x13c[7:0],0x13d[7:0],0x13d[7:0],0x13e[7:0],0x13e[7:0],0x13f[7:0])
12060   SPIWrite 013d,ff
12061   SPIWrite 013e,6b
12062   SPIWrite 0124,fe    //dir_bg=0x6bfffe;
        Address(0x124[7:0],0x125[7:0],0x125[7:0],0x126[7:0],0x126[7:0],0x127[7:0])
12063   SPIWrite 0125,ff
12064   SPIWrite 0126,6b
12065   SPIWrite 0129,24    //zone_sel_pu=0x4;  Address(0x129[7:0])
12066   SPIWrite 0130,76    //border_checks=0x1;    Address(0x130[7:2])
12067   SPIWrite 0130,7e    //cycle_zone=0x1;   Address(0x130[7:3])
12068   SPIWrite 0010,2f    //ec_dig=0x2f;  Address(0x10[7:0])
12069   SPIWrite 0044,01    //freeze_all_loops=0x1;     Address(0x44[7:0])
12070   SPIWrite 003c,01    //ec_reset=0x1;     Address(0x3c[7:0])
12071
12072   WAIT 0.001
12073   SPIWrite 003c,00    //ec_reset=0x0;     Address(0x3c[7:0])
12074   SPIWrite 0044,00    //freeze_all_loops=0x0;     Address(0x44[7:0])
12075   SPIWrite 00e8,00    //calib_start=0x0;  Address(0xe8[7:0])
12076   SPIWrite 00e8,01    //calib_start=0x1;  Address(0xe8[7:0])
12077   SPIWrite 0010,00    //ec_dig=0x0;   Address(0x10[7:0])
12078   SPIWrite 0015,04    //rx=0x1;   Address(0x15[7:2])
12079   SPIWrite 0063,00    //po_common_to_2r_rx_spare_0=0x40000;
        Address(0x60[7:0],0x61[7:0],0x62[7:0],0x63[7:0],0x64[7:0])
12080   SPIWrite 0062,04
12081   SPIWrite 0061,00
12082   SPIWrite 0060,00
12083   SPIWrite 0038,b0
12084   SPIWrite 0028,04
12085   SPIWrite 0015,08    //rx=0x2;   Address(0x15[7:2])
12086   SPIWrite 0063,00    //po_common_to_2r_rx_spare_0=0x40000;
        Address(0x60[7:0],0x61[7:0],0x62[7:0],0x63[7:0],0x64[7:0])
12087   SPIWrite 0062,04
12088   SPIWrite 0061,00
12089   SPIWrite 0060,00
12090   SPIWrite 0038,b0
12091   SPIWrite 0028,04
12092   SPIWrite 0015,00    //rx=0x0;   Address(0x15[7:2])
12093   SPIWrite 0015,02    //ana_4t4r=0x1;     Address(0x15[7:1])
12094   SPIWrite 006b,00    //po_common_to_pll_spare_1=0x8;
        Address(0x68[7:0],0x69[7:0],0x6a[7:0],0x6b[7:0],0x6c[7:0])
12095   SPIWrite 006a,00
12096   SPIWrite 0069,00
12097   SPIWrite 0068,08
12098   SPIWrite 0067,00    //po_common_to_pll_spare_0=0x4000;
        Address(0x64[7:0],0x65[7:0],0x66[7:0],0x67[7:0],0x68[7:0])
12099   SPIWrite 0066,00
```

```
SPIWrite 0065,40
SPIWrite 0064,00
SPIWrite 0015,00    //ana_4t4r=0x0;     Address(0x15[7:1])
SPIWrite 0012,0f    //rxdig=0xf;    Address(0x12[7:0])
SPIWrite 20f4,32    //DSAGainRange0=0x32;   Address(0x20f4[7:0])
SPIWrite 20f5,32    //DSAGainRange1=0x32;   Address(0x20f5[7:0])
SPIWrite 20f6,32    //DSAGainRange2=0x32;   Address(0x20f6[7:0])
SPIWrite 20f7,32    //DSAGainRange3=0x32;   Address(0x20f7[7:0])
SPIWrite 20f8,32    //DSAGainRange4=0x32;   Address(0x20f8[7:0])
SPIWrite 20f9,32    //DSAGainRange5=0x32;   Address(0x20f9[7:0])
SPIWrite 0012,00    //rxdig=0x0;    Address(0x12[7:0])
SPIWrite 0012,30    //fbdig=0x3;    Address(0x12[7:4])
SPIWrite 20f4,32    //DSAGainRange0=0x32;   Address(0x20f4[7:0])
SPIWrite 20f5,32    //DSAGainRange1=0x32;   Address(0x20f5[7:0])
SPIWrite 20f6,32    //DSAGainRange2=0x32;   Address(0x20f6[7:0])
SPIWrite 20f7,32    //DSAGainRange3=0x32;   Address(0x20f7[7:0])
SPIWrite 20f8,32    //DSAGainRange4=0x32;   Address(0x20f8[7:0])
SPIWrite 20f9,32    //DSAGainRange5=0x32;   Address(0x20f9[7:0])
SPIWrite 0012,00    //fbdig=0x0;    Address(0x12[7:4])

//STEP: analogWrites/step3

//START: Removing TDD Pin Overrides.

SPIWrite 0015,80    //timing_controller=0x1;    Address(0x15[7:7])
SPIWrite 00ed,00    //reg_for_rxtdd=0x0;    Address(0xed[7:0])
SPIWrite 00f5,03    //reg_for_fbtdd=0x3;    Address(0xf5[7:0])
SPIWrite 00e5,00    //reg_for_txtdd=0x0;    Address(0xe5[7:0])

//END: Removing TDD Pin Overrides.

SPIWrite 0015,00    //timing_controller=0x0;    Address(0x15[7:7])
SPIWrite 0018,20    //macro=0x1;    Address(0x18[7:5])
SPIRead 00f0

//Read  MACRO_READY=0x1;    Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00    //MACRO_OPERAND_REG0=0x1;
Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00
SPIWrite 00a1,00
SPIWrite 00a0,01
SPIWrite 0193,16    //MACRO_OPCODE=0x16;    Address(0x193[7:0],0x194[7:0])

WAIT 0.2
SPIRead 00f0

//Read  MACRO_DONE=0x0;     Address(0xf0[7:2])

SPIRead 00f0

//Read  MACRO_DONE=0x0;     Address(0xf0[7:2])

SPIRead 00f0

//Read  MACRO_DONE=0x1;     Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIRead 00f0

//Read  MACRO_ERROR=0x0;    Address(0xf0[7:3])

SPIRead 00f1

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```
12168   //Read  MACRO_ERROR_OPCODE=0x0;     Address(0xf1[7:0],0xf2[7:0])
12169
12170   SPIRead 00f0
12171
12172   //Read  MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])
12173
12174   SPIRead 00f0
12175
12176   //Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;     Address(0xf0[7:5])
12177
12178   SPIRead 00f0
12179
12180   //Read  MACRO_ERROR_IN_OPERAND=0x0;     Address(0xf0[7:6])
12181
12182   SPIRead 00f0
12183
12184   //Read  MACRO_ERROR_IN_EXECUTION=0x0;   Address(0xf0[7:7])
12185
12186   SPIRead 00f3
12187   SPIRead 00f2
12188
12189   //Read  MACRO_ERROR_EXTENDED_CODE=0x0;  Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
12190
12191   SPIRead 00f7
12192   SPIRead 00f6
12193   SPIRead 00f5
12194   SPIRead 00f4
12195
12196   //Read  MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
12197
12198   SPIWrite 0018,00    //macro=0x0;    Address(0x18[7:5])
12199   SPIWrite 0010,10    //ec_dig=0x10;  Address(0x10[7:0])
12200   SPIWrite 0044,01    //freeze_all_loops=0x1;     Address(0x44[7:0])
12201   SPIWrite 003c,01    //ec_reset=0x1;     Address(0x3c[7:0])
12202   SPIWrite 003c,00    //ec_reset=0x0;     Address(0x3c[7:0])
12203   SPIWrite 0044,00    //freeze_all_loops=0x0;     Address(0x44[7:0])
12204   SPIWrite 00e8,00    //calib_start=0x0;  Address(0xe8[7:0])
12205   SPIWrite 00e8,01    //calib_start=0x1;  Address(0xe8[7:0])
12206   SPIWrite 0010,00    //ec_dig=0x0;   Address(0x10[7:0])
12207
12208   //STEP: analogWrites/step4
12209
12210   //START: PLL Ana Trims
12211
12212
12213   //START: Requesting/releasing SPI Access to PLL Pages
12214
12215   SPIWrite 0015,40    //digtop=0x1;   Address(0x15[7:6])
12216   SPIWrite 0170,01    //pll_reg_spi_req_a=0x1;    Address(0x170[7:0])
12217   SPIWrite 0540,00    //pll_reg_spi_req_b1=0x0;   Address(0x540[7:0])
12218
12219   SPIPoll 0171,0,0,01
12220   SPIRead 0171
12221
12222   //Read  pll_reg_spi_a_ack=0x1(Meaning: );;  Address(0x171[7:0])
12223
12224
12225   //END: Requesting/releasing SPI Access to PLL Pages
12226
12227   SPIWrite 0015,00    //digtop=0x0;   Address(0x15[7:6])
12228   SPIWrite 0015,01    //pll=0x1;  Address(0x15[7:0])
12229   SPIWrite 005e,01    //ENCLK_CSETAMP=0x1;    Address(0x5e[7:0])
12230   SPIWrite 005d,ec    //TRIM_CSETAMP_CUR=0x7;     Address(0x5d[7:5])
12231
12232   //START: Requesting/releasing SPI Access to PLL Pages
12233
12234   SPIWrite 0015,00    //pll=0x0;  Address(0x15[7:0])
12235   SPIWrite 0015,40    //digtop=0x1;   Address(0x15[7:6])
```

```
12236   SPIWrite 0170,00    //pll_reg_spi_req_a=0x0;    Address(0x170[7:0])
12237   SPIWrite 0540,00    //pll_reg_spi_req_b1=0x0;   Address(0x540[7:0])
12238
12239   WAIT 0.2
12240
12241   //END: Requesting/releasing SPI Access to PLL Pages
12242
12243   SPIWrite 050f,00    //auxadc_cfg3=0xc0000;
        Address(0x50c[7:0],0x50d[7:0],0x50e[7:0],0x50f[7:0],0x510[7:0])
12244   SPIWrite 050e,0c
12245   SPIWrite 050d,00
12246   SPIWrite 050c,00
12247   SPIWrite 0015,00    //digtop=0x0;   Address(0x15[7:6])
12248   SPIWrite 0015,02    //ana_4t4r=0x1;     Address(0x15[7:1])
12249   SPIWrite 00bb,00    //po_txc_interface_control=0x0;
        Address(0xb8[7:0],0xb9[7:0],0xba[7:0],0xbb[7:0],0xbc[7:0])
12250   SPIWrite 00ba,00
12251   SPIWrite 00b9,00
12252   SPIWrite 00b8,00
12253   SPIWrite 00bb,00    //po_txc_interface_control=0x8000;
        Address(0xb8[7:0],0xb9[7:0],0xba[7:0],0xbb[7:0],0xbc[7:0])
12254   SPIWrite 00ba,00
12255   SPIWrite 00b9,80
12256   SPIWrite 00b8,00
12257   SPIWrite 00bb,00    //po_txc_interface_control=0x0;
        Address(0xb8[7:0],0xb9[7:0],0xba[7:0],0xbb[7:0],0xbc[7:0])
12258   SPIWrite 00ba,00
12259   SPIWrite 00b9,00
12260   SPIWrite 00b8,00
12261
12262   WAIT 0.1
12263
12264   //END: PLL Ana Trims
12265
12266   SPIWrite 0015,00    //ana_4t4r=0x0;     Address(0x15[7:1])
12267
12268   //STEP: jesdConfig/step0
12269
12270   //START: Configuring JESD Muxes and Pointers
12271
12272
12273   //START: Configuring JESD TX Lane Mux
12274
12275   SPIWrite 0016,10    //jesd_subchip=0x1;     Address(0x16[7:4])
12276   SPIWrite 0048,10    //txoctetpath0_sel=0x0;     Address(0x48[7:0])
12277   SPIWrite 0048,20    //txoctetpath1_sel=0x2;     Address(0x48[7:4])
12278   SPIWrite 0049,31    //txoctetpath2_sel=0x1;     Address(0x49[7:0])
12279   SPIWrite 0049,31    //txoctetpath3_sel=0x3;     Address(0x49[7:4])
12280   SPIWrite 004a,54    //txoctetpath4_sel=0x4;     Address(0x4a[7:0])
12281   SPIWrite 004a,54    //txoctetpath5_sel=0x5;     Address(0x4a[7:4])
12282   SPIWrite 004b,76    //txoctetpath6_sel=0x6;     Address(0x4b[7:0])
12283   SPIWrite 004b,76    //txoctetpath7_sel=0x7;     Address(0x4b[7:4])
12284   SPIWrite 004c,10    //txoctetpath0_clk_sel=0x0;     Address(0x4c[7:0])
12285   SPIWrite 004c,20    //txoctetpath1_clk_sel=0x2;     Address(0x4c[7:4])
12286   SPIWrite 004d,31    //txoctetpath2_clk_sel=0x1;     Address(0x4d[7:0])
12287   SPIWrite 004d,31    //txoctetpath3_clk_sel=0x3;     Address(0x4d[7:4])
12288   SPIWrite 004e,54    //txoctetpath4_clk_sel=0x4;     Address(0x4e[7:0])
12289   SPIWrite 004e,54    //txoctetpath5_clk_sel=0x5;     Address(0x4e[7:4])
12290   SPIWrite 004f,76    //txoctetpath6_clk_sel=0x6;     Address(0x4f[7:0])
12291   SPIWrite 004f,76    //txoctetpath7_clk_sel=0x7;     Address(0x4f[7:4])
12292
12293   //END: Configuring JESD TX Lane Mux
12294
12295
12296   //START: Configuring JESD RX Lane Mux
12297
12298   SPIWrite 0068,11    //rxoctetpath0_sel=0x1;     Address(0x68[7:0])
12299   SPIWrite 0068,31    //rxoctetpath1_sel=0x3;     Address(0x68[7:4])
12300   SPIWrite 0069,35    //rxoctetpath2_sel=0x5;     Address(0x69[7:0])
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SPIWrite 0069,65    //rxoctetpath3_sel=0x6;     Address(0x69[7:4])
SPIWrite 006a,50    //rxoctetpath4_sel=0x0;     Address(0x6a[7:0])
SPIWrite 006a,20    //rxoctetpath5_sel=0x2;     Address(0x6a[7:4])
SPIWrite 006b,74    //rxoctetpath6_sel=0x4;     Address(0x6b[7:0])
SPIWrite 006b,74    //rxoctetpath7_sel=0x7;     Address(0x6b[7:4])
SPIWrite 006c,14    //rxoctetpath0_clk_sel=0x4;     Address(0x6c[7:0])
SPIWrite 006c,04    //rxoctetpath1_clk_sel=0x0;     Address(0x6c[7:4])
SPIWrite 006d,35    //rxoctetpath2_clk_sel=0x5;     Address(0x6d[7:0])
SPIWrite 006d,15    //rxoctetpath3_clk_sel=0x1;     Address(0x6d[7:4])
SPIWrite 006e,56    //rxoctetpath4_clk_sel=0x6;     Address(0x6e[7:0])
SPIWrite 006e,26    //rxoctetpath5_clk_sel=0x2;     Address(0x6e[7:4])
SPIWrite 006f,73    //rxoctetpath6_clk_sel=0x3;     Address(0x6f[7:0])
SPIWrite 006f,73    //rxoctetpath7_clk_sel=0x7;     Address(0x6f[7:4])

//END: Configuring JESD RX Lane Mux


//START: Configuring the DDC-JESD Data Muxes

SPIWrite 0034,00    //mux_sel_rxa_b1_i_for_2r1f_ab=0x0;     Address(0x34[7:0])
SPIWrite 0034,00    //mux_sel_rxa_b1_q_for_2r1f_ab=0x0;     Address(0x34[7:4])
SPIWrite 0035,22    //mux_sel_rxa_b2_i_for_2r1f_ab=0x2;     Address(0x35[7:0])
SPIWrite 0035,22    //mux_sel_rxa_b2_q_for_2r1f_ab=0x2;     Address(0x35[7:4])
SPIWrite 0036,44    //mux_sel_rxb_b1_i_for_2r1f_ab=0x4;     Address(0x36[7:0])
SPIWrite 0036,44    //mux_sel_rxb_b1_q_for_2r1f_ab=0x4;     Address(0x36[7:4])
SPIWrite 0037,66    //mux_sel_rxb_b2_i_for_2r1f_ab=0x6;     Address(0x37[7:0])
SPIWrite 0037,66    //mux_sel_rxb_b2_q_for_2r1f_ab=0x6;     Address(0x37[7:4])
SPIWrite 0038,40    //mux_sel_rxc_b1_i_for_2r1f_ab=0x0;     Address(0x38[7:0])
SPIWrite 0038,00    //mux_sel_rxc_b1_q_for_2r1f_ab=0x0;     Address(0x38[7:4])
SPIWrite 0039,52    //mux_sel_rxc_b2_i_for_2r1f_ab=0x2;     Address(0x39[7:0])
SPIWrite 0039,22    //mux_sel_rxc_b2_q_for_2r1f_ab=0x2;     Address(0x39[7:4])
SPIWrite 003a,64    //mux_sel_rxd_b1_i_for_2r1f_ab=0x4;     Address(0x3a[7:0])
SPIWrite 003a,44    //mux_sel_rxd_b1_q_for_2r1f_ab=0x4;     Address(0x3a[7:4])
SPIWrite 003b,76    //mux_sel_rxd_b2_i_for_2r1f_ab=0x6;     Address(0x3b[7:0])
SPIWrite 003b,66    //mux_sel_rxd_b2_q_for_2r1f_ab=0x6;     Address(0x3b[7:4])
SPIWrite 0040,00    //mux_sel_rxc_b1_i_for_2r1f_cd=0x0;     Address(0x40[7:0])
SPIWrite 0040,00    //mux_sel_rxc_b1_q_for_2r1f_cd=0x0;     Address(0x40[7:4])
SPIWrite 0041,22    //mux_sel_rxc_b2_i_for_2r1f_cd=0x2;     Address(0x41[7:0])
SPIWrite 0041,22    //mux_sel_rxc_b2_q_for_2r1f_cd=0x2;     Address(0x41[7:4])
SPIWrite 0042,24    //mux_sel_rxd_b1_i_for_2r1f_cd=0x4;     Address(0x42[7:0])
SPIWrite 0042,44    //mux_sel_rxd_b1_q_for_2r1f_cd=0x4;     Address(0x42[7:4])
SPIWrite 0043,36    //mux_sel_rxd_b2_i_for_2r1f_cd=0x6;     Address(0x43[7:0])
SPIWrite 0043,66    //mux_sel_rxd_b2_q_for_2r1f_cd=0x6;     Address(0x43[7:4])
SPIWrite 0044,50    //mux_sel_fba_i0_for_2r1f_ab=0x0;   Address(0x44[7:0])
SPIWrite 0044,50    //mux_sel_fba_q0_for_2r1f_ab=0x0;   Address(0x44[7:2])
SPIWrite 0044,50    //mux_sel_fba_i1_for_2r1f_ab=0x1;   Address(0x44[7:4])
SPIWrite 0044,50    //mux_sel_fba_q1_for_2r1f_ab=0x1;   Address(0x44[7:6])
SPIWrite 0045,fa    //mux_sel_fbc_i0_for_2r1f_ab=0x2;   Address(0x45[7:0])
SPIWrite 0045,fa    //mux_sel_fbc_q0_for_2r1f_ab=0x2;   Address(0x45[7:2])
SPIWrite 0045,fa    //mux_sel_fbc_i1_for_2r1f_ab=0x3;   Address(0x45[7:4])
SPIWrite 0045,fa    //mux_sel_fbc_q1_for_2r1f_ab=0x3;   Address(0x45[7:6])
SPIWrite 0046,fa    //mux_sel_fba_i0_for_2r1f_cd=0x2;   Address(0x46[7:0])
SPIWrite 0046,fa    //mux_sel_fba_q0_for_2r1f_cd=0x2;   Address(0x46[7:2])
SPIWrite 0046,fa    //mux_sel_fba_i1_for_2r1f_cd=0x3;   Address(0x46[7:4])
SPIWrite 0046,fa    //mux_sel_fba_q1_for_2r1f_cd=0x3;   Address(0x46[7:6])
SPIWrite 0047,50    //mux_sel_fbc_i0_for_2r1f_cd=0x0;   Address(0x47[7:0])
SPIWrite 0047,50    //mux_sel_fbc_q0_for_2r1f_cd=0x0;   Address(0x47[7:2])
SPIWrite 0047,50    //mux_sel_fbc_i1_for_2r1f_cd=0x1;   Address(0x47[7:4])
SPIWrite 0047,50    //mux_sel_fbc_q1_for_2r1f_cd=0x1;   Address(0x47[7:6])

//END: Configuring the DDC-JESD Data Muxes


//START: Configuring the JESD-DUC Data Muxes

SPIWrite 00cc,00    //mux_sel_for_txa_b0_i=0x0;     Address(0xcc[7:0])
SPIWrite 00cc,00    //mux_sel_for_txa_b0_q=0x0;     Address(0xcc[7:4])
SPIWrite 00cd,11    //mux_sel_for_txa_b1_i=0x1;     Address(0xcd[7:0])
SPIWrite 00cd,11    //mux_sel_for_txa_b1_q=0x1;     Address(0xcd[7:4])
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12370   SPIWrite 00ce,22    //mux_sel_for_txb_b0_i=0x2;     Address(0xce[7:0])
12371   SPIWrite 00ce,22    //mux_sel_for_txb_b0_q=0x2;     Address(0xce[7:4])
12372   SPIWrite 00cf,33    //mux_sel_for_txb_b1_i=0x3;     Address(0xcf[7:0])
12373   SPIWrite 00cf,33    //mux_sel_for_txb_b1_q=0x3;     Address(0xcf[7:4])
12374   SPIWrite 00d0,48    //mux_sel_for_txc_b0_i=0x8;     Address(0xd0[7:0])
12375   SPIWrite 00d0,88    //mux_sel_for_txc_b0_q=0x8;     Address(0xd0[7:4])
12376   SPIWrite 00d1,59    //mux_sel_for_txc_b1_i=0x9;     Address(0xd1[7:0])
12377   SPIWrite 00d1,99    //mux_sel_for_txc_b1_q=0x9;     Address(0xd1[7:4])
12378   SPIWrite 00d2,6a    //mux_sel_for_txd_b0_i=0xa;     Address(0xd2[7:0])
12379   SPIWrite 00d2,aa    //mux_sel_for_txd_b0_q=0xa;     Address(0xd2[7:4])
12380   SPIWrite 00d3,7b    //mux_sel_for_txd_b1_i=0xb;     Address(0xd3[7:0])
12381   SPIWrite 00d3,bb    //mux_sel_for_txd_b1_q=0xb;     Address(0xd3[7:4])
12382   SPIWrite 0060,10    //mux_sel_for_txa_ctrl=0x0;     Address(0x60[7:0])
12383   SPIWrite 0060,10    //mux_sel_for_txb_ctrl=0x1;     Address(0x60[7:4])
12384   SPIWrite 0061,34    //mux_sel_for_txc_ctrl=0x4;     Address(0x61[7:0])
12385   SPIWrite 0061,54    //mux_sel_for_txd_ctrl=0x5;     Address(0x61[7:4])
12386
12387   //END: Configuring the JESD-DUC Data Muxes
12388
12389
12390   //START: Configuring JESD TX Sync Mux
12391
12392   SPIWrite 0054,00    //adc_jesd_sync_n0_mux_sel=0x0;     Address(0x54[7:0])
12393   SPIWrite 0054,00    //adc_jesd_sync_n1_mux_sel=0x0;     Address(0x54[7:4])
12394   SPIWrite 0055,30    //adc_jesd_sync_n2_mux_sel=0x0;     Address(0x55[7:0])
12395   SPIWrite 0055,00    //adc_jesd_sync_n3_mux_sel=0x0;     Address(0x55[7:4])
12396   SPIWrite 0056,50    //adc_jesd_sync_n4_mux_sel=0x0;     Address(0x56[7:0])
12397   SPIWrite 0056,00    //adc_jesd_sync_n5_mux_sel=0x0;     Address(0x56[7:4])
12398
12399   //END: Configuring JESD TX Sync Mux
12400
12401
12402   //START: Configuring JESD RX Sync Mux
12403
12404   SPIWrite 00ca,e4    //dac_jesd_sync_n0_mux_sel=0x0;     Address(0xca[7:0])
12405   SPIWrite 00ca,e0    //dac_jesd_sync_n1_mux_sel=0x0;     Address(0xca[7:2])
12406   SPIWrite 00ca,c0    //dac_jesd_sync_n2_mux_sel=0x0;     Address(0xca[7:4])
12407   SPIWrite 00ca,00    //dac_jesd_sync_n3_mux_sel=0x0;     Address(0xca[7:6])
12408
12409   //END: Configuring JESD RX Sync Mux
12410
12411   SPIWrite 009c,03    //rx_clk_dithered_mode_en=0x1;  Address(0x9c[7:1])
12412   SPIWrite 009e,03    //fb_clk_dithered_mode_en=0x1;  Address(0x9e[7:1])
12413   SPIWrite 009c,03    //rx_clk_disable=0x1;   Address(0x9c[7:0])
12414   SPIWrite 00a0,02    //tx_clk_disable=0x0;   Address(0xa0[7:0])
12415   SPIWrite 00a0,00    //tx_clk_dithered_mode_en=0x0;  Address(0xa0[7:1])
12416
12417   //END: Configuring JESD Muxes and Pointers
12418
12419
12420   //START: Setting JESD SyncB Pin Mode
12421
12422
12423   //END: Setting JESD SyncB Pin Mode
12424
12425   SPIWrite 0016,00    //jesd_subchip=0x0;     Address(0x16[7:4])
12426
12427   //STEP: jesdConfig/step1
12428
12429   //START: Configuring ADC JESD TX
12430
12431   SPIWrite 0016,01    //adc_jesd=0x1;     Address(0x16[7:0])
12432   SPIWrite 006d,07    //link0_init_state=0x1;     Address(0x6d[7:0])
12433   SPIWrite 006d,07    //link1_init_state=0x1;     Address(0x6d[7:1])
12434   SPIWrite 006d,07    //link2_init_state=0x1;     Address(0x6d[7:2])
12435   SPIWrite 006f,02    //init_state_gearbox_spi_ovr=0x1;   Address(0x6f[7:1])
12436   SPIWrite 006c,0f    //lane0_gearbox_init_state=0x1;     Address(0x6c[7:0])
12437   SPIWrite 006c,0f    //lane1_gearbox_init_state=0x1;     Address(0x6c[7:1])
12438   SPIWrite 006c,0f    //lane2_gearbox_init_state=0x1;     Address(0x6c[7:2])
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12439   SPIWrite 006c,0f    //lane3_gearbox_init_state=0x1;     Address(0x6c[7:3])
12440   SPIWrite 006c,0e    //lane0_gearbox_init_state=0x0;     Address(0x6c[7:0])
12441   SPIWrite 006c,0c    //lane1_gearbox_init_state=0x0;     Address(0x6c[7:1])
12442   SPIWrite 006c,08    //lane2_gearbox_init_state=0x0;     Address(0x6c[7:2])
12443   SPIWrite 006c,00    //lane3_gearbox_init_state=0x0;     Address(0x6c[7:3])
12444   SPIWrite 006e,0f    //lane0_serdes_fifo_init_state=0x1;     Address(0x6e[7:0])
12445   SPIWrite 006e,0f    //lane1_serdes_fifo_init_state=0x1;     Address(0x6e[7:1])
12446   SPIWrite 006e,0f    //lane2_serdes_fifo_init_state=0x1;     Address(0x6e[7:2])
12447   SPIWrite 006e,0f    //lane3_serdes_fifo_init_state=0x1;     Address(0x6e[7:3])
12448   SPIWrite 005c,1f    //rx_root_clk_dither_en=0x1;    Address(0x5c[7:0])
12449   SPIWrite 005c,1f    //fb_root_clk_dither_en=0x1;    Address(0x5c[7:1])
12450   SPIWrite 005c,1b    //ddc_rd_clk_dither_en=0x0;     Address(0x5c[7:2])
12451   SPIWrite 005c,13    //jesd_clk_dither_en=0x0;   Address(0x5c[7:3])
12452   SPIWrite 005c,03    //jesd_clk_div2_dither_en=0x0;  Address(0x5c[7:4])
12453   SPIWrite 0021,01    //jesd_system_mode=0x1;     Address(0x21[7:0])
12454   SPIWrite 005d,01    //rx_adc_clk_sysref_mux=0x1;    Address(0x5d[7:0])
12455   SPIWrite 005d,01    //fb_adc_clk_sysref_mux=0x0;    Address(0x5d[7:1])
12456   SPIWrite 0024,0f    //jesd_clear_data=0xf;  Address(0x24[7:0])
12457   SPIWrite 0069,8c    //serdes_fifo_read_dly_lane0=0xc;   Address(0x69[7:0])
12458   SPIWrite 0069,cc    //serdes_fifo_read_dly_lane1=0xc;   Address(0x69[7:4])
12459   SPIWrite 006a,8c    //serdes_fifo_read_dly_lane2=0xc;   Address(0x6a[7:0])
12460   SPIWrite 006a,cc    //serdes_fifo_read_dly_lane3=0xc;   Address(0x6a[7:4])
12461   SPIWrite 0040,01    //rx1_root_clk_div_m=0x1;   Address(0x40[7:0])
12462   SPIWrite 0041,00    //rx1_root_clk_div_n_m1=0x0;    Address(0x41[7:0])
12463   SPIWrite 0046,01    //ddc_rd_clk_rx1_div_m=0x1;     Address(0x46[7:0])
12464   SPIWrite 0047,03    //ddc_rd_clk_rx1_div_n_m1=0x3;  Address(0x47[7:0])
12465   SPIWrite 004c,01    //jesd_clk_rx1_div_m=0x1;   Address(0x4c[7:0])
12466   SPIWrite 004d,00    //jesd_clk_rx1_div_n_m1=0x0;    Address(0x4d[7:0])
12467   SPIWrite 0034,14    //rx1_jesd_mode=0x14;   Address(0x34[7:0])
12468   SPIWrite 0084,00    //link0_k_m1=0x0;   Address(0x84[7:0],0x85[7:0])
12469   SPIWrite 0079,00    //link0_ila_k_m1=0x0;   Address(0x79[7:0],0x7a[7:0])
12470   SPIWrite 0042,01    //rx2_root_clk_div_m=0x1;   Address(0x42[7:0])
12471   SPIWrite 0043,00    //rx2_root_clk_div_n_m1=0x0;    Address(0x43[7:0])
12472   SPIWrite 0048,01    //ddc_rd_clk_rx2_div_m=0x1;     Address(0x48[7:0])
12473   SPIWrite 0049,03    //ddc_rd_clk_rx2_div_n_m1=0x3;  Address(0x49[7:0])
12474   SPIWrite 004e,01    //jesd_clk_rx2_div_m=0x1;   Address(0x4e[7:0])
12475   SPIWrite 004f,00    //jesd_clk_rx2_div_n_m1=0x0;    Address(0x4f[7:0])
12476   SPIWrite 0035,14    //rx2_jesd_mode=0x14;   Address(0x35[7:0])
12477   SPIWrite 009c,00    //link1_k_m1=0x0;   Address(0x9c[7:0],0x9d[7:0])
12478   SPIWrite 0091,00    //link1_ila_k_m1=0x0;   Address(0x91[7:0],0x92[7:0])
12479   SPIWrite 0044,01    //fb_root_clk_div_m=0x1;    Address(0x44[7:0])
12480   SPIWrite 0045,00    //fb_root_clk_div_n_m1=0x0;     Address(0x45[7:0])
12481   SPIWrite 004a,01    //ddc_rd_clk_fb_div_m=0x1;  Address(0x4a[7:0])
12482   SPIWrite 004b,03    //ddc_rd_clk_fb_div_n_m1=0x3;   Address(0x4b[7:0])
12483   SPIWrite 0050,01    //jesd_clk_fb_div_m=0x1;    Address(0x50[7:0])
12484   SPIWrite 0051,00    //jesd_clk_fb_div_n_m1=0x0;     Address(0x51[7:0])
12485   SPIWrite 0036,0b    //fb_jesd_mode=0xb;     Address(0x36[7:0])
12486   SPIWrite 00b4,00    //link2_k_m1=0x0;   Address(0xb4[7:0],0xb5[7:0])
12487   SPIWrite 00a9,00    //link2_ila_k_m1=0x0;   Address(0xa9[7:0],0xaa[7:0])
12488   SPIWrite 0020,02    //jesd_std_sel=0x2;     Address(0x20[7:0])
12489   SPIWrite 0077,01    //link0_scr=0x0;    Address(0x77[7:7])
12490   SPIWrite 008f,01    //link1_scr=0x0;    Address(0x8f[7:7])
12491   SPIWrite 00a7,01    //link2_scr=0x0;    Address(0xa7[7:7])
12492   SPIWrite 0023,05    //lane_ena=0x5;     Address(0x23[7:0])
12493   SPIWrite 003c,02    //sel_rx1_jesd_mode_1s_2s_ovr=0x1;  Address(0x3c[7:1])
12494   SPIWrite 003c,02    //sel_rx1_jesd_mode_1s_2s_val=0x0;  Address(0x3c[7:0])
12495   SPIWrite 003c,0a    //sel_rx2_jesd_mode_1s_2s_ovr=0x1;  Address(0x3c[7:3])
12496   SPIWrite 003c,0a    //sel_rx2_jesd_mode_1s_2s_val=0x0;  Address(0x3c[7:2])
12497   SPIWrite 003c,2a    //sel_fb_jesd_mode_1s_2s_ovr=0x1;   Address(0x3c[7:5])
12498   SPIWrite 003c,3a    //sel_fb_jesd_mode_1s_2s_val=0x1;   Address(0x3c[7:4])
12499   SPIWrite 0083,01    //link0_jesd_ila_config_override=0x1;   Address(0x83[7:0])
12500   SPIWrite 009b,01    //link1_jesd_ila_config_override=0x1;   Address(0x9b[7:0])
12501   SPIWrite 0078,0f    //link0_ila_f_m1=0xf;   Address(0x78[7:0],0x79[7:0])
12502   SPIWrite 0090,0f    //link1_ila_f_m1=0xf;   Address(0x90[7:0],0x91[7:0])
12503   SPIWrite 00a8,07    //link2_ila_f_m1=0x7;   Address(0xa8[7:0],0xa9[7:0])
12504   SPIWrite 007a,07    //link0_ila_m_m1=0x7;   Address(0x7a[7:0],0x7b[7:0])
12505   SPIWrite 0092,07    //link1_ila_m_m1=0x7;   Address(0x92[7:0],0x93[7:0])
12506   SPIWrite 00aa,01    //link2_ila_m_m1=0x1;   Address(0xaa[7:0],0xab[7:0])
12507   SPIWrite 0077,03    //link0_ila_l_m1=0x3;   Address(0x77[7:0])
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SPIWrite 008f,03    //link1_ila_l_m1=0x3;   Address(0x8f[7:0])
SPIWrite 00a7,01    //link2_ila_l_m1=0x1;   Address(0xa7[7:0])
SPIWrite 007b,0f    //link0_ila_n_m1=0xf;   Address(0x7b[7:0])
SPIWrite 0093,0f    //link1_ila_n_m1=0xf;   Address(0x93[7:0])
SPIWrite 00ab,0f    //link2_ila_n_m1=0xf;   Address(0xab[7:0])
SPIWrite 00bc,00    //lid0=0x0;     Address(0xbc[7:0])
SPIWrite 00bd,01    //lid1=0x1;     Address(0xbd[7:0])
SPIWrite 00be,02    //lid2=0x2;     Address(0xbe[7:0])
SPIWrite 00bf,03    //lid3=0x3;     Address(0xbf[7:0])
SPIWrite 00e4,42    //msf_rx1_offset_default_mode0=0x2;     Address(0xe4[7:0])
SPIWrite 00e4,22    //msf_rx1_offset_default_mode1=0x2;     Address(0xe4[7:4])
SPIWrite 00e5,83    //msf_rx1_offset_default_mode2=0x3;     Address(0xe5[7:0])
SPIWrite 00e5,43    //msf_rx1_offset_default_mode3=0x4;     Address(0xe5[7:4])
SPIWrite 00e6,42    //msf_rx2_offset_default_mode0=0x2;     Address(0xe6[7:0])
SPIWrite 00e6,22    //msf_rx2_offset_default_mode1=0x2;     Address(0xe6[7:4])
SPIWrite 00e7,83    //msf_rx2_offset_default_mode2=0x3;     Address(0xe7[7:0])
SPIWrite 00e7,43    //msf_rx2_offset_default_mode3=0x4;     Address(0xe7[7:4])
SPIWrite 00e8,42    //msf_fb_offset_default_mode0=0x2;  Address(0xe8[7:0])
SPIWrite 00e8,22    //msf_fb_offset_default_mode1=0x2;  Address(0xe8[7:4])
SPIWrite 00e9,83    //msf_fb_offset_default_mode2=0x3;  Address(0xe9[7:0])
SPIWrite 00e9,43    //msf_fb_offset_default_mode3=0x4;  Address(0xe9[7:4])
SPIWrite 0037,06    //rx1_ctrlmode_12b_trunc_en=0x0;    Address(0x37[7:0])
SPIWrite 0037,04    //rx2_ctrlmode_12b_trunc_en=0x0;    Address(0x37[7:1])
SPIWrite 0037,00    //fb_ctrlmode_12b_trunc_en=0x0;     Address(0x37[7:2])

//END: Done Configuring ADC JESD TX


//START: Configuring ADC JESD TX

SPIWrite 0016,02    //adc_jesd=0x2;     Address(0x16[7:0])
SPIWrite 006d,07    //link0_init_state=0x1;     Address(0x6d[7:0])
SPIWrite 006d,07    //link1_init_state=0x1;     Address(0x6d[7:1])
SPIWrite 006d,07    //link2_init_state=0x1;     Address(0x6d[7:2])
SPIWrite 006f,02    //init_state_gearbox_spi_ovr=0x1;   Address(0x6f[7:1])
SPIWrite 006c,0f    //lane0_gearbox_init_state=0x1;     Address(0x6c[7:0])
SPIWrite 006c,0f    //lane1_gearbox_init_state=0x1;     Address(0x6c[7:1])
SPIWrite 006c,0f    //lane2_gearbox_init_state=0x1;     Address(0x6c[7:2])
SPIWrite 006c,0f    //lane3_gearbox_init_state=0x1;     Address(0x6c[7:3])
SPIWrite 006c,0e    //lane0_gearbox_init_state=0x0;     Address(0x6c[7:0])
SPIWrite 006c,0c    //lane1_gearbox_init_state=0x0;     Address(0x6c[7:1])
SPIWrite 006c,08    //lane2_gearbox_init_state=0x0;     Address(0x6c[7:2])
SPIWrite 006c,00    //lane3_gearbox_init_state=0x0;     Address(0x6c[7:3])
SPIWrite 006e,0f    //lane0_serdes_fifo_init_state=0x1;     Address(0x6e[7:0])
SPIWrite 006e,0f    //lane1_serdes_fifo_init_state=0x1;     Address(0x6e[7:1])
SPIWrite 006e,0f    //lane2_serdes_fifo_init_state=0x1;     Address(0x6e[7:2])
SPIWrite 006e,0f    //lane3_serdes_fifo_init_state=0x1;     Address(0x6e[7:3])
SPIWrite 005c,1f    //rx_root_clk_dither_en=0x1;    Address(0x5c[7:0])
SPIWrite 005c,1f    //fb_root_clk_dither_en=0x1;    Address(0x5c[7:1])
SPIWrite 005c,1b    //ddc_rd_clk_dither_en=0x0;     Address(0x5c[7:2])
SPIWrite 005c,13    //jesd_clk_dither_en=0x0;   Address(0x5c[7:3])
SPIWrite 005c,03    //jesd_clk_div2_dither_en=0x0;  Address(0x5c[7:4])
SPIWrite 0021,01    //jesd_system_mode=0x1;     Address(0x21[7:0])
SPIWrite 005d,01    //rx_adc_clk_sysref_mux=0x1;    Address(0x5d[7:0])
SPIWrite 005d,01    //fb_adc_clk_sysref_mux=0x0;    Address(0x5d[7:1])
SPIWrite 0024,0f    //jesd_clear_data=0xf;  Address(0x24[7:0])
SPIWrite 0069,8c    //serdes_fifo_read_dly_lane0=0xc;   Address(0x69[7:0])
SPIWrite 0069,cc    //serdes_fifo_read_dly_lane1=0xc;   Address(0x69[7:4])
SPIWrite 006a,8c    //serdes_fifo_read_dly_lane2=0xc;   Address(0x6a[7:0])
SPIWrite 006a,cc    //serdes_fifo_read_dly_lane3=0xc;   Address(0x6a[7:4])
SPIWrite 0040,01    //rx1_root_clk_div_m=0x1;   Address(0x40[7:0])
SPIWrite 0041,00    //rx1_root_clk_div_n_m1=0x0;    Address(0x41[7:0])
SPIWrite 0046,01    //ddc_rd_clk_rx1_div_m=0x1;     Address(0x46[7:0])
SPIWrite 0047,03    //ddc_rd_clk_rx1_div_n_m1=0x3;  Address(0x47[7:0])
SPIWrite 004c,01    //jesd_clk_rx1_div_m=0x1;   Address(0x4c[7:0])
SPIWrite 004d,00    //jesd_clk_rx1_div_n_m1=0x0;    Address(0x4d[7:0])
SPIWrite 0034,14    //rx1_jesd_mode=0x14;   Address(0x34[7:0])
SPIWrite 0084,00    //link0_k_m1=0x0;   Address(0x84[7:0],0x85[7:0])
SPIWrite 0079,00    //link0_ila_k_m1=0x0;   Address(0x79[7:0],0x7a[7:0])
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12577   SPIWrite 0042,01    //rx2_root_clk_div_m=0x1;   Address(0x42[7:0])
12578   SPIWrite 0043,00    //rx2_root_clk_div_n_m1=0x0;    Address(0x43[7:0])
12579   SPIWrite 0048,01    //ddc_rd_clk_rx2_div_m=0x1;     Address(0x48[7:0])
12580   SPIWrite 0049,03    //ddc_rd_clk_rx2_div_n_m1=0x3;  Address(0x49[7:0])
12581   SPIWrite 004e,01    //jesd_clk_rx2_div_m=0x1;   Address(0x4e[7:0])
12582   SPIWrite 004f,00    //jesd_clk_rx2_div_n_m1=0x0;    Address(0x4f[7:0])
12583   SPIWrite 0035,14    //rx2_jesd_mode=0x14;   Address(0x35[7:0])
12584   SPIWrite 009c,00    //link1_k_m1=0x0;   Address(0x9c[7:0],0x9d[7:0])
12585   SPIWrite 0091,00    //link1_ila_k_m1=0x0;   Address(0x91[7:0],0x92[7:0])
12586   SPIWrite 0044,01    //fb_root_clk_div_m=0x1;    Address(0x44[7:0])
12587   SPIWrite 0045,00    //fb_root_clk_div_n_m1=0x0;     Address(0x45[7:0])
12588   SPIWrite 004a,01    //ddc_rd_clk_fb_div_m=0x1;  Address(0x4a[7:0])
12589   SPIWrite 004b,03    //ddc_rd_clk_fb_div_n_m1=0x3;   Address(0x4b[7:0])
12590   SPIWrite 0050,01    //jesd_clk_fb_div_m=0x1;    Address(0x50[7:0])
12591   SPIWrite 0051,00    //jesd_clk_fb_div_n_m1=0x0;     Address(0x51[7:0])
12592   SPIWrite 0036,0b    //fb_jesd_mode=0xb;     Address(0x36[7:0])
12593   SPIWrite 00b4,00    //link2_k_m1=0x0;   Address(0xb4[7:0],0xb5[7:0])
12594   SPIWrite 00a9,00    //link2_ila_k_m1=0x0;   Address(0xa9[7:0],0xaa[7:0])
12595   SPIWrite 0020,02    //jesd_std_sel=0x2;     Address(0x20[7:0])
12596   SPIWrite 0077,01    //link0_scr=0x0;    Address(0x77[7:7])
12597   SPIWrite 008f,01    //link1_scr=0x0;    Address(0x8f[7:7])
12598   SPIWrite 00a7,01    //link2_scr=0x0;    Address(0xa7[7:7])
12599   SPIWrite 0023,00    //lane_ena=0x0;     Address(0x23[7:0])
12600   SPIWrite 003c,02    //sel_rx1_jesd_mode_1s_2s_ovr=0x1;  Address(0x3c[7:1])
12601   SPIWrite 003c,02    //sel_rx1_jesd_mode_1s_2s_val=0x0;  Address(0x3c[7:0])
12602   SPIWrite 003c,0a    //sel_rx2_jesd_mode_1s_2s_ovr=0x1;  Address(0x3c[7:3])
12603   SPIWrite 003c,0a    //sel_rx2_jesd_mode_1s_2s_val=0x0;  Address(0x3c[7:2])
12604   SPIWrite 003c,2a    //sel_fb_jesd_mode_1s_2s_ovr=0x1;   Address(0x3c[7:5])
12605   SPIWrite 003c,3a    //sel_fb_jesd_mode_1s_2s_val=0x1;   Address(0x3c[7:4])
12606   SPIWrite 0083,01    //link0_jesd_ila_config_override=0x1;   Address(0x83[7:0])
12607   SPIWrite 009b,01    //link1_jesd_ila_config_override=0x1;   Address(0x9b[7:0])
12608   SPIWrite 0078,0f    //link0_ila_f_m1=0xf;   Address(0x78[7:0],0x79[7:0])
12609   SPIWrite 0090,0f    //link1_ila_f_m1=0xf;   Address(0x90[7:0],0x91[7:0])
12610   SPIWrite 00a8,07    //link2_ila_f_m1=0x7;   Address(0xa8[7:0],0xa9[7:0])
12611   SPIWrite 007a,07    //link0_ila_m_m1=0x7;   Address(0x7a[7:0],0x7b[7:0])
12612   SPIWrite 0092,07    //link1_ila_m_m1=0x7;   Address(0x92[7:0],0x93[7:0])
12613   SPIWrite 00aa,01    //link2_ila_m_m1=0x1;   Address(0xaa[7:0],0xab[7:0])
12614   SPIWrite 0077,03    //link0_ila_l_m1=0x3;   Address(0x77[7:0])
12615   SPIWrite 008f,03    //link1_ila_l_m1=0x3;   Address(0x8f[7:0])
12616   SPIWrite 00a7,01    //link2_ila_l_m1=0x1;   Address(0xa7[7:0])
12617   SPIWrite 007b,0f    //link0_ila_n_m1=0xf;   Address(0x7b[7:0])
12618   SPIWrite 0093,0f    //link1_ila_n_m1=0xf;   Address(0x93[7:0])
12619   SPIWrite 00ab,0f    //link2_ila_n_m1=0xf;   Address(0xab[7:0])
12620   SPIWrite 00bc,04    //lid0=0x4;     Address(0xbc[7:0])
12621   SPIWrite 00bd,05    //lid1=0x5;     Address(0xbd[7:0])
12622   SPIWrite 00be,06    //lid2=0x6;     Address(0xbe[7:0])
12623   SPIWrite 00bf,07    //lid3=0x7;     Address(0xbf[7:0])
12624   SPIWrite 00e4,42    //msf_rx1_offset_default_mode0=0x2;     Address(0xe4[7:0])
12625   SPIWrite 00e4,22    //msf_rx1_offset_default_mode1=0x2;     Address(0xe4[7:4])
12626   SPIWrite 00e5,83    //msf_rx1_offset_default_mode2=0x3;     Address(0xe5[7:0])
12627   SPIWrite 00e5,43    //msf_rx1_offset_default_mode3=0x4;     Address(0xe5[7:4])
12628   SPIWrite 00e6,42    //msf_rx2_offset_default_mode0=0x2;     Address(0xe6[7:0])
12629   SPIWrite 00e6,22    //msf_rx2_offset_default_mode1=0x2;     Address(0xe6[7:4])
12630   SPIWrite 00e7,83    //msf_rx2_offset_default_mode2=0x3;     Address(0xe7[7:0])
12631   SPIWrite 00e7,43    //msf_rx2_offset_default_mode3=0x4;     Address(0xe7[7:4])
12632   SPIWrite 00e8,42    //msf_fb_offset_default_mode0=0x2;  Address(0xe8[7:0])
12633   SPIWrite 00e8,22    //msf_fb_offset_default_mode1=0x2;  Address(0xe8[7:4])
12634   SPIWrite 00e9,83    //msf_fb_offset_default_mode2=0x3;  Address(0xe9[7:0])
12635   SPIWrite 00e9,43    //msf_fb_offset_default_mode3=0x4;  Address(0xe9[7:4])
12636   SPIWrite 0037,06    //rx1_ctrlmode_12b_trunc_en=0x0;    Address(0x37[7:0])
12637   SPIWrite 0037,04    //rx2_ctrlmode_12b_trunc_en=0x0;    Address(0x37[7:1])
12638   SPIWrite 0037,00    //fb_ctrlmode_12b_trunc_en=0x0;     Address(0x37[7:2])
12639
12640   //END: Done Configuring ADC JESD TX
12641
12642   SPIWrite 0016,00    //adc_jesd=0x0;     Address(0x16[7:0])
12643
12644   //STEP: jesdConfig/step2
12645
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12646   //START: Configuring DAC JESD RX
12647
12648   SPIWrite 0016,04    //dac_jesd=0x1;     Address(0x16[7:2])
12649   SPIWrite 006c,00    //link0_k_m1=0x0;   Address(0x6c[7:0],0x6d[7:0])
12650   SPIWrite 006d,00    //link1_k_m1=0x0;   Address(0x6d[7:0],0x6e[7:0])
12651   SPIWrite 0057,00    //link1_ila_k_m1=0x0;   Address(0x57[7:0],0x58[7:0])
12652   SPIWrite 0049,00    //link0_ila_k_m1=0x0;   Address(0x49[7:0],0x4a[7:0])
12653   SPIWrite 0069,00    //link0_rbd_m1=0x3;     Address(0x68[7:0],0x69[7:0],0x6a[7:0])
12654   SPIWrite 0068,03
12655   SPIWrite 006b,00    //link1_rbd_m1=0x3;     Address(0x6a[7:0],0x6b[7:0],0x6c[7:0])
12656   SPIWrite 006a,03
12657   SPIWrite 0024,5e    //gearbox_init_state_ovr=0x1;   Address(0x24[7:6])
12658   SPIWrite 0025,ff    //gearbox_init_state_lane0_val=0x1;     Address(0x25[7:0])
12659   SPIWrite 0025,ff    //gearbox_init_state_lane1_val=0x1;     Address(0x25[7:1])
12660   SPIWrite 0025,ff    //gearbox_init_state_lane2_val=0x1;     Address(0x25[7:2])
12661   SPIWrite 0025,ff    //gearbox_init_state_lane3_val=0x1;     Address(0x25[7:3])
12662   SPIWrite 0025,fe    //gearbox_init_state_lane0_val=0x0;     Address(0x25[7:0])
12663   SPIWrite 0025,fc    //gearbox_init_state_lane1_val=0x0;     Address(0x25[7:1])
12664   SPIWrite 0025,f8    //gearbox_init_state_lane2_val=0x0;     Address(0x25[7:2])
12665   SPIWrite 0025,f0    //gearbox_init_state_lane3_val=0x0;     Address(0x25[7:3])
12666   SPIWrite 0020,03    //link0_init_state=0x1;     Address(0x20[7:0])
12667   SPIWrite 0020,03    //link1_init_state=0x1;     Address(0x20[7:1])
12668   SPIWrite 0064,ff    //jesd_clear_data=0xf;  Address(0x64[7:4])
12669   SPIWrite 0040,04    //link0_comma_align_lock_reset_disable=0x1;     Address(0x40[7:2])
12670   SPIWrite 0040,0c    //link1_comma_align_lock_reset_disable=0x1;     Address(0x40[7:3])
12671   SPIWrite 00ac,04    //link0_emb_align_lock_reset_disable=0x1;   Address(0xac[7:2])
12672   SPIWrite 00ac,0c    //link1_emb_align_lock_reset_disable=0x1;   Address(0xac[7:3])
12673   SPIWrite 002c,01    //root_clk_tx1_div_m=0x1;   Address(0x2c[7:0])
12674   SPIWrite 002d,00    //root_clk_tx1_div_n_m1=0x0;    Address(0x2d[7:0])
12675   SPIWrite 002e,01    //root_clk_tx2_div_m=0x1;   Address(0x2e[7:0])
12676   SPIWrite 002f,00    //root_clk_tx2_div_n_m1=0x0;    Address(0x2f[7:0])
12677   SPIWrite 0030,01    //duc_clk_tx1_div_m=0x1;    Address(0x30[7:0])
12678   SPIWrite 0031,01    //duc_clk_tx1_div_n_m1=0x1;     Address(0x31[7:0])
12679   SPIWrite 0032,01    //duc_clk_tx2_div_m=0x1;    Address(0x32[7:0])
12680   SPIWrite 0033,01    //duc_clk_tx2_div_n_m1=0x1;     Address(0x33[7:0])
12681   SPIWrite 0034,01    //jesd_clk_tx1_div_m=0x1;   Address(0x34[7:0])
12682   SPIWrite 0035,00    //jesd_clk_tx1_div_n_m1=0x0;    Address(0x35[7:0])
12683   SPIWrite 0036,01    //jesd_clk_tx2_div_m=0x1;   Address(0x36[7:0])
12684   SPIWrite 0037,00    //jesd_clk_tx2_div_n_m1=0x0;    Address(0x37[7:0])
12685   SPIWrite 0022,41    //link0_jesd_mode=0x1;  Address(0x22[7:0])
12686   SPIWrite 0023,41    //link1_jesd_mode=0x1;  Address(0x23[7:0])
12687   SPIWrite 0022,41    //link0_jesd_sample_mode=0x1;   Address(0x22[7:6])
12688   SPIWrite 0023,41    //link1_jesd_sample_mode=0x1;   Address(0x23[7:6])
12689   SPIWrite 0038,1f    //tx_root_clk_div_dither_en=0x1;    Address(0x38[7:0])
12690   SPIWrite 0038,1d    //duc_clk_io_div_dither_en=0x0;     Address(0x38[7:1])
12691   SPIWrite 0038,19    //duc_clk_div_dither_en=0x0;    Address(0x38[7:2])
12692   SPIWrite 0038,11    //jesd_clk_div_dither_en=0x0;   Address(0x38[7:3])
12693   SPIWrite 0038,01    //jesd_clk_div2_div_dither_en=0x0;  Address(0x38[7:4])
12694   SPIWrite 0026,00    //num_links=0x0;    Address(0x26[7:2])
12695   SPIWrite 0042,7f    //comma_align_valid_thresh=0x7f;    Address(0x42[7:0])
12696   SPIWrite 00ad,86    //emb_align_valid_thresh=0x6;   Address(0xad[7:0])
12697   SPIWrite 0078,00    //link0_sync_request_ena=0x0;   Address(0x78[7:0],0x79[7:0])
12698   SPIWrite 0079,00    //link1_sync_request_ena=0x0;   Address(0x79[7:0],0x7a[7:0])
12699   SPIWrite 007a,00    //link0_error_ena=0x0;  Address(0x7a[7:0],0x7b[7:0])
12700   SPIWrite 007b,00    //link1_error_ena=0x0;  Address(0x7b[7:0],0x7c[7:0])
12701   SPIWrite 0103,00    //alarms_clear=0xe1e1e1e1000000bf;
      Address(0x100[7:0],0x101[7:0],0x102[7:0],0x103[7:0],0x104[7:0],0x104[7:0],0x105[7:0],0x10
      6[7:0],0x107[7:0],0x108[7:0])
12702   SPIWrite 0102,00
12703   SPIWrite 0101,00
12704   SPIWrite 0100,bf
12705   SPIWrite 0107,e1
12706   SPIWrite 0106,e1
12707   SPIWrite 0105,e1
12708   SPIWrite 0104,e1
12709   SPIWrite 00fb,00    //alarms_mask=0xe1e1e1e1000000bf;
      Address(0xf8[7:0],0xf9[7:0],0xfa[7:0],0xfb[7:0],0xfc[7:0],0xfc[7:0],0xfd[7:0],0xfe[7:0],0
      xff[7:0],0x100[7:0])
12710   SPIWrite 00fa,00
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12711   SPIWrite 00f9,00
12712   SPIWrite 00f8,bf
12713   SPIWrite 00ff,e1
12714   SPIWrite 00fe,e1
12715   SPIWrite 00fd,e1
12716   SPIWrite 00fc,e1
12717   SPIWrite 0113,00    //alarms_to_pap_clear=0xe1e1e1e1000000bf;
        Address(0x110[7:0],0x111[7:0],0x112[7:0],0x113[7:0],0x114[7:0],0x114[7:0],0x115[7:0],0x11
        6[7:0],0x117[7:0],0x118[7:0])
12718   SPIWrite 0112,00
12719   SPIWrite 0111,00
12720   SPIWrite 0110,bf
12721   SPIWrite 0117,e1
12722   SPIWrite 0116,e1
12723   SPIWrite 0115,e1
12724   SPIWrite 0114,e1
12725   SPIWrite 010b,00    //alarms_to_pap_mask=0xe1e1e1e1000000bf;
        Address(0x108[7:0],0x109[7:0],0x10a[7:0],0x10b[7:0],0x10c[7:0],0x10c[7:0],0x10d[7:0],0x10
        e[7:0],0x10f[7:0],0x110[7:0])
12726   SPIWrite 010a,00
12727   SPIWrite 0109,00
12728   SPIWrite 0108,bf
12729   SPIWrite 010f,e1
12730   SPIWrite 010e,e1
12731   SPIWrite 010d,e1
12732   SPIWrite 010c,e1
12733   SPIWrite 0024,5c    //alarm_zeros_jesd_data_ena=0x0;    Address(0x24[7:1])
12734   SPIWrite 003c,82    //serdes_fifo_offset_lane0=0x2;     Address(0x3c[7:0])
12735   SPIWrite 003c,22    //serdes_fifo_offset_lane1=0x2;     Address(0x3c[7:4])
12736   SPIWrite 003d,82    //serdes_fifo_offset_lane2=0x2;     Address(0x3d[7:0])
12737   SPIWrite 003d,22    //serdes_fifo_offset_lane3=0x2;     Address(0x3d[7:4])
12738   SPIWrite 0026,02    //jesd_std_sel=0x2;     Address(0x26[7:0])
12739   SPIWrite 0047,01    //link0_scr=0x0;    Address(0x47[7:7])
12740   SPIWrite 0055,01    //link1_scr=0x0;    Address(0x55[7:7])
12741   SPIWrite 0064,f1    //lane_ena=0x1;     Address(0x64[7:0])
12742   SPIWrite 0081,f1    //rbd_buf_overflow_err_cnt_thresh=0xf;  Address(0x81[7:4])
12743   SPIWrite 0083,1f    //dec_8b10b_code_err_cnt_thresh=0xf;    Address(0x83[7:0])
12744   SPIWrite 0083,ff    //dec_8b10b_disp_err_cnt_thresh=0xf;    Address(0x83[7:4])
12745   SPIWrite 0081,ff    //link_config_err_cnt_thresh=0xf;   Address(0x81[7:0])
12746   SPIWrite 0080,1f    //multiframe_align_err_cnt_thresh=0xf;  Address(0x80[7:0])
12747   SPIWrite 0080,ff    //frame_align_err_cnt_thresh=0xf;   Address(0x80[7:4])
12748   SPIWrite 00a8,02    //code_err_disable=0x1;     Address(0xa8[7:1])
12749   SPIWrite 0024,58    //zero_invalid_data=0x0;    Address(0x24[7:2])
12750   SPIWrite 0024,50    //fifo_error_zeros_data_ena=0x0;    Address(0x24[7:3])
12751
12752   //END: Done Configuring DAC JESD RX
12753
12754
12755   //START: Configuring DAC JESD RX
12756
12757   SPIWrite 0016,08    //dac_jesd=0x2;     Address(0x16[7:2])
12758   SPIWrite 006c,00    //link0_k_m1=0x0;   Address(0x6c[7:0],0x6d[7:0])
12759   SPIWrite 006d,00    //link1_k_m1=0x0;   Address(0x6d[7:0],0x6e[7:0])
12760   SPIWrite 0057,00    //link1_ila_k_m1=0x0;   Address(0x57[7:0],0x58[7:0])
12761   SPIWrite 0049,00    //link0_ila_k_m1=0x0;   Address(0x49[7:0],0x4a[7:0])
12762   SPIWrite 0069,00    //link0_rbd_m1=0x3;     Address(0x68[7:0],0x69[7:0],0x6a[7:0])
12763   SPIWrite 0068,03
12764   SPIWrite 006b,00    //link1_rbd_m1=0x3;     Address(0x6a[7:0],0x6b[7:0],0x6c[7:0])
12765   SPIWrite 006a,03
12766   SPIWrite 0024,5e    //gearbox_init_state_ovr=0x1;   Address(0x24[7:6])
12767   SPIWrite 0025,ff    //gearbox_init_state_lane0_val=0x1;     Address(0x25[7:0])
12768   SPIWrite 0025,ff    //gearbox_init_state_lane1_val=0x1;     Address(0x25[7:1])
12769   SPIWrite 0025,ff    //gearbox_init_state_lane2_val=0x1;     Address(0x25[7:2])
12770   SPIWrite 0025,ff    //gearbox_init_state_lane3_val=0x1;     Address(0x25[7:3])
12771   SPIWrite 0025,fe    //gearbox_init_state_lane0_val=0x0;     Address(0x25[7:0])
12772   SPIWrite 0025,fc    //gearbox_init_state_lane1_val=0x0;     Address(0x25[7:1])
12773   SPIWrite 0025,f8    //gearbox_init_state_lane2_val=0x0;     Address(0x25[7:2])
12774   SPIWrite 0025,f0    //gearbox_init_state_lane3_val=0x0;     Address(0x25[7:3])
12775   SPIWrite 0020,03    //link0_init_state=0x1;     Address(0x20[7:0])
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12776   SPIWrite 0020,03    //link1_init_state=0x1;     Address(0x20[7:1])
12777   SPIWrite 0064,ff    //jesd_clear_data=0xf;  Address(0x64[7:4])
12778   SPIWrite 0040,04    //link0_comma_align_lock_reset_disable=0x1;     Address(0x40[7:2])
12779   SPIWrite 0040,0c    //link1_comma_align_lock_reset_disable=0x1;     Address(0x40[7:3])
12780   SPIWrite 00ac,04    //link0_emb_align_lock_reset_disable=0x1;   Address(0xac[7:2])
12781   SPIWrite 00ac,0c    //link1_emb_align_lock_reset_disable=0x1;   Address(0xac[7:3])
12782   SPIWrite 002c,01    //root_clk_tx1_div_m=0x1;   Address(0x2c[7:0])
12783   SPIWrite 002d,00    //root_clk_tx1_div_n_m1=0x0;    Address(0x2d[7:0])
12784   SPIWrite 002e,01    //root_clk_tx2_div_m=0x1;   Address(0x2e[7:0])
12785   SPIWrite 002f,00    //root_clk_tx2_div_n_m1=0x0;    Address(0x2f[7:0])
12786   SPIWrite 0030,01    //duc_clk_tx1_div_m=0x1;    Address(0x30[7:0])
12787   SPIWrite 0031,01    //duc_clk_tx1_div_n_m1=0x1;     Address(0x31[7:0])
12788   SPIWrite 0032,01    //duc_clk_tx2_div_m=0x1;    Address(0x32[7:0])
12789   SPIWrite 0033,01    //duc_clk_tx2_div_n_m1=0x1;     Address(0x33[7:0])
12790   SPIWrite 0034,01    //jesd_clk_tx1_div_m=0x1;   Address(0x34[7:0])
12791   SPIWrite 0035,00    //jesd_clk_tx1_div_n_m1=0x0;    Address(0x35[7:0])
12792   SPIWrite 0036,01    //jesd_clk_tx2_div_m=0x1;   Address(0x36[7:0])
12793   SPIWrite 0037,00    //jesd_clk_tx2_div_n_m1=0x0;    Address(0x37[7:0])
12794   SPIWrite 0022,41    //link0_jesd_mode=0x1;  Address(0x22[7:0])
12795   SPIWrite 0023,41    //link1_jesd_mode=0x1;  Address(0x23[7:0])
12796   SPIWrite 0022,41    //link0_jesd_sample_mode=0x1;   Address(0x22[7:6])
12797   SPIWrite 0023,41    //link1_jesd_sample_mode=0x1;   Address(0x23[7:6])
12798   SPIWrite 0038,1f    //tx_root_clk_div_dither_en=0x1;    Address(0x38[7:0])
12799   SPIWrite 0038,1d    //duc_clk_io_div_dither_en=0x0;     Address(0x38[7:1])
12800   SPIWrite 0038,19    //duc_clk_div_dither_en=0x0;    Address(0x38[7:2])
12801   SPIWrite 0038,11    //jesd_clk_div_dither_en=0x0;   Address(0x38[7:3])
12802   SPIWrite 0038,01    //jesd_clk_div2_div_dither_en=0x0;  Address(0x38[7:4])
12803   SPIWrite 0026,00    //num_links=0x0;    Address(0x26[7:2])
12804   SPIWrite 0042,7f    //comma_align_valid_thresh=0x7f;    Address(0x42[7:0])
12805   SPIWrite 00ad,86    //emb_align_valid_thresh=0x6;   Address(0xad[7:0])
12806   SPIWrite 0078,00    //link0_sync_request_ena=0x0;   Address(0x78[7:0],0x79[7:0])
12807   SPIWrite 0079,00    //link1_sync_request_ena=0x0;   Address(0x79[7:0],0x7a[7:0])
12808   SPIWrite 007a,00    //link0_error_ena=0x0;  Address(0x7a[7:0],0x7b[7:0])
12809   SPIWrite 007b,00    //link1_error_ena=0x0;  Address(0x7b[7:0],0x7c[7:0])
12810   SPIWrite 0103,00    //alarms_clear=0xe1e1e1e1000000bf;
      Address(0x100[7:0],0x101[7:0],0x102[7:0],0x103[7:0],0x104[7:0],0x104[7:0],0x105[7:0],0x10
      6[7:0],0x107[7:0],0x108[7:0])
12811   SPIWrite 0102,00
12812   SPIWrite 0101,00
12813   SPIWrite 0100,bf
12814   SPIWrite 0107,e1
12815   SPIWrite 0106,e1
12816   SPIWrite 0105,e1
12817   SPIWrite 0104,e1
12818   SPIWrite 00fb,00    //alarms_mask=0xe1e1e1e1000000bf;
      Address(0xf8[7:0],0xf9[7:0],0xfa[7:0],0xfb[7:0],0xfc[7:0],0xfc[7:0],0xfd[7:0],0xfe[7:0],0
      xff[7:0],0x100[7:0])
12819   SPIWrite 00fa,00
12820   SPIWrite 00f9,00
12821   SPIWrite 00f8,bf
12822   SPIWrite 00ff,e1
12823   SPIWrite 00fe,e1
12824   SPIWrite 00fd,e1
12825   SPIWrite 00fc,e1
12826   SPIWrite 0113,00    //alarms_to_pap_clear=0xe1e1e1e1000000bf;
      Address(0x110[7:0],0x111[7:0],0x112[7:0],0x113[7:0],0x114[7:0],0x114[7:0],0x115[7:0],0x11
      6[7:0],0x117[7:0],0x118[7:0])
12827   SPIWrite 0112,00
12828   SPIWrite 0111,00
12829   SPIWrite 0110,bf
12830   SPIWrite 0117,e1
12831   SPIWrite 0116,e1
12832   SPIWrite 0115,e1
12833   SPIWrite 0114,e1
12834   SPIWrite 010b,00    //alarms_to_pap_mask=0xe1e1e1e1000000bf;
      Address(0x108[7:0],0x109[7:0],0x10a[7:0],0x10b[7:0],0x10c[7:0],0x10c[7:0],0x10d[7:0],0x10
      e[7:0],0x10f[7:0],0x110[7:0])
12835   SPIWrite 010a,00
12836   SPIWrite 0109,00
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SPIWrite 0108,bf
SPIWrite 010f,e1
SPIWrite 010e,e1
SPIWrite 010d,e1
SPIWrite 010c,e1
SPIWrite 0024,5c    //alarm_zeros_jesd_data_ena=0x0;    Address(0x24[7:1])
SPIWrite 003c,82    //serdes_fifo_offset_lane0=0x2;     Address(0x3c[7:0])
SPIWrite 003c,22    //serdes_fifo_offset_lane1=0x2;     Address(0x3c[7:4])
SPIWrite 003d,82    //serdes_fifo_offset_lane2=0x2;     Address(0x3d[7:0])
SPIWrite 003d,22    //serdes_fifo_offset_lane3=0x2;     Address(0x3d[7:4])
SPIWrite 0026,02    //jesd_std_sel=0x2;     Address(0x26[7:0])
SPIWrite 0047,01    //link0_scr=0x0;    Address(0x47[7:7])
SPIWrite 0055,01    //link1_scr=0x0;    Address(0x55[7:7])
SPIWrite 0064,f1    //lane_ena=0x1;     Address(0x64[7:0])
SPIWrite 0081,f1    //rbd_buf_overflow_err_cnt_thresh=0xf;  Address(0x81[7:4])
SPIWrite 0083,1f    //dec_8b10b_code_err_cnt_thresh=0xf;    Address(0x83[7:0])
SPIWrite 0083,ff    //dec_8b10b_disp_err_cnt_thresh=0xf;    Address(0x83[7:4])
SPIWrite 0081,ff    //link_config_err_cnt_thresh=0xf;   Address(0x81[7:0])
SPIWrite 0080,1f    //multiframe_align_err_cnt_thresh=0xf;  Address(0x80[7:0])
SPIWrite 0080,ff    //frame_align_err_cnt_thresh=0xf;   Address(0x80[7:4])
SPIWrite 00a8,02    //code_err_disable=0x1;     Address(0xa8[7:1])
SPIWrite 0024,58    //zero_invalid_data=0x0;    Address(0x24[7:2])
SPIWrite 0024,50    //fifo_error_zeros_data_ena=0x0;    Address(0x24[7:3])

//END: Done Configuring DAC JESD RX

SPIWrite 0016,00    //dac_jesd=0x0;     Address(0x16[7:2])

//STEP: jesdConfig/step3
SPIWrite 0016,10    //jesd_subchip=0x1;     Address(0x16[7:4])
SPIWrite 007c,c3    //lp_rx_on_a_sel_2r1f_ab_mask=0x3;  Address(0x7c[7:0])
SPIWrite 007c,c3    //lp_rx_on_b_sel_2r1f_ab_mask=0xc;  Address(0x7c[7:4])
SPIWrite 007d,03    //lp_rx_on_c_sel_2r1f_ab_mask=0x3;  Address(0x7d[7:0])
SPIWrite 007d,c3    //lp_rx_on_d_sel_2r1f_ab_mask=0xc;  Address(0x7d[7:4])
SPIWrite 007e,09    //lp_fb_on_a_sel_2r1f_ab_mask=0x1;  Address(0x7e[7:0])
SPIWrite 007e,09    //lp_fb_on_c_sel_2r1f_ab_mask=0x2;  Address(0x7e[7:2])
SPIWrite 0016,00    //jesd_subchip=0x0;     Address(0x16[7:4])
SPIWrite 0016,01    //adc_jesd=0x1;     Address(0x16[7:0])
SPIWrite 0120,00    //ctrl_rx1_msf_sig_invalid=0x0;     Address(0x120[7:0])
SPIWrite 0120,00    //ctrl_rx2_msf_sig_invalid=0x0;     Address(0x120[7:2])
SPIWrite 0120,30    //ctrl_rx3_rx4_msf_sig_invalid=0x3;     Address(0x120[7:4])
SPIWrite 0121,00    //ctrl_fb1_msf_sig_invalid=0x0;     Address(0x121[7:0])
SPIWrite 0121,00    //ctrl_fb2_msf_sig_invalid=0x0;     Address(0x121[7:2])
SPIWrite 0016,00    //adc_jesd=0x0;     Address(0x16[7:0])
SPIWrite 0016,10    //jesd_subchip=0x1;     Address(0x16[7:4])
SPIWrite 0029,02    //dual_2t2r1f_mode_ab=0x0;  Address(0x29[7:0])
SPIWrite 0029,00    //dual_2t2r1f_mode_cd=0x0;  Address(0x29[7:1])
SPIWrite 0081,03    //lp_rx_on_c_sel_2r1f_cd_mask=0x3;  Address(0x81[7:0])
SPIWrite 0081,c3    //lp_rx_on_d_sel_2r1f_cd_mask=0xc;  Address(0x81[7:4])
SPIWrite 0082,04    //lp_fb_on_c_sel_2r1f_cd_mask=0x1;  Address(0x82[7:2])
SPIWrite 0082,06    //lp_fb_on_a_sel_2r1f_cd_mask=0x2;  Address(0x82[7:0])
SPIWrite 0016,00    //jesd_subchip=0x0;     Address(0x16[7:4])
SPIWrite 0016,02    //adc_jesd=0x2;     Address(0x16[7:0])
SPIWrite 0120,00    //ctrl_rx1_msf_sig_invalid=0x0;     Address(0x120[7:0])
SPIWrite 0120,00    //ctrl_rx2_msf_sig_invalid=0x0;     Address(0x120[7:2])
SPIWrite 0120,30    //ctrl_rx3_rx4_msf_sig_invalid=0x3;     Address(0x120[7:4])
SPIWrite 0121,00    //ctrl_fb1_msf_sig_invalid=0x0;     Address(0x121[7:0])
SPIWrite 0121,00    //ctrl_fb2_msf_sig_invalid=0x0;     Address(0x121[7:2])
SPIWrite 0016,00    //adc_jesd=0x0;     Address(0x16[7:0])
SPIWrite 0016,10    //jesd_subchip=0x1;     Address(0x16[7:4])
SPIWrite 0029,00    //dual_2t2r1f_mode_ab=0x0;  Address(0x29[7:0])
SPIWrite 0029,00    //dual_2t2r1f_mode_cd=0x0;  Address(0x29[7:1])
SPIWrite 0016,00    //jesd_subchip=0x0;     Address(0x16[7:4])

//STEP: agcConfig/step0
SPIWrite 0013,40    //dsa_page1=0x1;    Address(0x13[7:6])
SPIWrite 00d0,03    //gain_ctrl=0x3;    Address(0xd0[7:0])
SPIWrite 0013,80    //dsa_page1=0x2;    Address(0x13[7:6])
SPIWrite 00d0,03    //gain_ctrl=0x3;    Address(0xd0[7:0])
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SPIWrite 0013,00    //dsa_page1=0x0;    Address(0x13[7:6])
SPIWrite 0012,01    //rxdig=0x1;    Address(0x12[7:0])
SPIWrite 0773,01    //cfg_agc_pdn=0x1;  Address(0x773[7:0])
SPIWrite 0773,01    //cfg_agc_pdn=0x1;  Address(0x773[7:0])
SPIWrite 0012,08    //rxdig=0x8;    Address(0x12[7:0])
SPIWrite 0773,01    //cfg_agc_pdn=0x1;  Address(0x773[7:0])
SPIWrite 0773,01    //cfg_agc_pdn=0x1;  Address(0x773[7:0])
SPIWrite 0012,00    //rxdig=0x0;    Address(0x12[7:0])

//STEP: miscConfig/step0

//START: Configuring Interrupt Pins

SPIWrite 0015,40    //digtop=0x1;   Address(0x15[7:6])
SPIWrite 0101,02    //alarm_mask_lsb_for_alarm0=0x23f;
Address(0x100[7:0],0x101[7:0],0x102[7:0])
SPIWrite 0100,3f
SPIWrite 0103,00    //alarm_mask_msb_for_alarm0=0x0;
Address(0x102[7:0],0x103[7:0],0x104[7:0])
SPIWrite 0102,00
SPIWrite 0105,02    //alarm_mask_lsb_for_alarm1=0x23f;
Address(0x104[7:0],0x105[7:0],0x106[7:0])
SPIWrite 0104,3f
SPIWrite 0107,00    //alarm_mask_msb_for_alarm1=0x0;
Address(0x106[7:0],0x107[7:0],0x108[7:0])
SPIWrite 0106,00

//END: Done configuring Interrupt Pins


//START: Power Saving Options

SPIWrite 0931,02    //misc_spi_force_ctrl_gbl_pdn_fbana_cd=0x1;     Address(0x931[7:1])
SPIWrite 0015,00    //digtop=0x0;   Address(0x15[7:6])
SPIWrite 0011,3f    //ec_ana=0x3f;  Address(0x11[7:0])
SPIWrite 00ce,20    //PDN_NL_BUF=0x1;   Address(0xce[7:5])
SPIWrite 00cb,04    //PDN_NL_DITH=0x1;  Address(0xcb[7:2])
SPIWrite 00ca,20    //PDN_NL_SAMP=0x1;  Address(0xca[7:5])
SPIWrite 00ce,30    //PDN_NL_BE=0x1;    Address(0xce[7:4])
SPIWrite 00c3,40    //OVR_PDN_NL_BE_WO_CLK=0x1;     Address(0xc3[7:6])
SPIWrite 00c0,01    //PDN_NL_BE_WO_CLK_SPI=0x1;     Address(0xc0[7:0])
SPIWrite 00b9,40    //OVR_PDN_NL_DITH_WO_CLK=0x1;   Address(0xb9[7:6])
SPIWrite 00b9,50    //PDN_NL_DITH_WO_CLK_SPI=0x1;   Address(0xb9[7:4])
SPIWrite 00b9,70    //OVR_PDN_NL_SAMP_WO_CLK=0x1;   Address(0xb9[7:5])
SPIWrite 00b9,78    //PDN_NL_SAMP_WO_CLK_SPI=0x1;   Address(0xb9[7:3])
SPIWrite 0011,00    //ec_ana=0x0;   Address(0x11[7:0])
SPIWrite 0010,3f    //ec_dig=0x3f;  Address(0x10[7:0])
SPIWrite 00b0,30    //gate_all_clocks=0x1;  Address(0xb0[7:5])
SPIWrite 00b4,30    //gate_all_clocks=0x1;  Address(0xb4[7:5])
SPIWrite 0010,00    //ec_dig=0x0;   Address(0x10[7:0])
SPIWrite 0019,01    //NL_reg0=0x1;  Address(0x19[7:0])
SPIWrite 039c,01    //cfg_ref_adc_pdn_rxa=0x1;  Address(0x39c[7:0])
SPIWrite 039d,01    //cfg_ref_adc_pdn_rxb=0x1;  Address(0x39d[7:0])
SPIWrite 039e,01    //cfg_ref_adc_pdn_rxc=0x1;  Address(0x39e[7:0])
SPIWrite 039f,01    //cfg_ref_adc_pdn_rxd=0x1;  Address(0x39f[7:0])
SPIWrite 03a0,01    //cfg_ref_adc_pdn_fba=0x1;  Address(0x3a0[7:0])
SPIWrite 03a1,01    //cfg_ref_adc_pdn_fbc=0x1;  Address(0x3a1[7:0])

//END: Power Saving Options

SPIWrite 0019,00    //NL_reg0=0x0;  Address(0x19[7:0])

//STEP: miscConfig/step1
SPIWrite 0013,40    //dsa_page1=0x1;    Address(0x13[7:6])
SPIWrite 0124,00    //spi_agc_dsa_A=0x0;    Address(0x124[7:0])
SPIWrite 0174,00    //spi_agc_dsa_B=0x0;    Address(0x174[7:0])
SPIWrite 0013,80    //dsa_page1=0x2;    Address(0x13[7:6])
SPIWrite 0124,00    //spi_agc_dsa_A=0x0;    Address(0x124[7:0])
SPIWrite 0174,00    //spi_agc_dsa_B=0x0;    Address(0x174[7:0])
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12971   SPIWrite 0013,00    //dsa_page1=0x0;    Address(0x13[7:6])
12972   SPIWrite 0013,10    //dsa_page0=0x1;    Address(0x13[7:4])
12973   SPIWrite 00c8,00    //txa_dsa_index=0x0;    Address(0xc8[7:0])
12974   SPIWrite 00cc,00    //txb_dsa_index=0x0;    Address(0xcc[7:0])
12975   SPIWrite 0013,20    //dsa_page0=0x2;    Address(0x13[7:4])
12976   SPIWrite 00c8,00    //txa_dsa_index=0x0;    Address(0xc8[7:0])
12977   SPIWrite 00cc,00    //txb_dsa_index=0x0;    Address(0xcc[7:0])
12978   SPIWrite 0013,10    //dsa_page0=0x1;    Address(0x13[7:4])
12979   SPIWrite 006c,00    //spi_agc_dsa_fb=0x0;   Address(0x6c[7:0])
12980   SPIWrite 0013,20    //dsa_page0=0x2;    Address(0x13[7:4])
12981   SPIWrite 006c,00    //spi_agc_dsa_fb=0x0;   Address(0x6c[7:0])
12982   SPIWrite 0013,00    //dsa_page0=0x0;    Address(0x13[7:4])
12983
12984   //STEP: gpioConfig/step0
12985   SPIWrite 0015,10    //io_wrap=0x1;  Address(0x15[7:4])
12986   SPIWrite 04c0,05    //preferred_input_sel_gpio_48=0x1;  Address(0x4c0[7:2])
12987   SPIWrite 04c0,05    //buf_dir_ctrl_gpio_48=0x1;     Address(0x4c0[7:0])
12988   SPIWrite 08a1,00    //ovr_sel_intpi_adc_sync_n_ab_0=0x0;    Address(0x8a1[7:1])
12989   SPIWrite 04bc,21    //preferred_output_sel_gpio_47=0x1;     Address(0x4bc[7:5])
12990   SPIWrite 04bc,22    //buf_dir_ctrl_gpio_47=0x2;     Address(0x4bc[7:0])
12991   SPIWrite 10c5,00    //ovr_sel_intpo_dac_sync_n_ab_0=0x0;    Address(0x10c5[7:1])
12992   SPIWrite 0438,05    //preferred_input_sel_gpio_14=0x1;  Address(0x438[7:2])
12993   SPIWrite 0438,05    //buf_dir_ctrl_gpio_14=0x1;     Address(0x438[7:0])
12994   SPIWrite 0899,00    //ovr_sel_intpi_spib1_cs_n=0x0;     Address(0x899[7:1])
12995   SPIWrite 0420,01    //preferred_input_sel_gpio_8=0x0;   Address(0x420[7:2])
12996   SPIWrite 0420,01    //buf_dir_ctrl_gpio_8=0x1;  Address(0x420[7:0])
12997   SPIWrite 08c9,00    //ovr_sel_intpi_tdd_en_fbab=0x0;    Address(0x8c9[7:1])
12998   SPIWrite 08ca,09    //crossbar_sel_intpi_tdd_en_fbab=0x9;
        Address(0x8ca[7:0],0x8cb[7:0])
12999   SPIWrite 0420,01    //preferred_input_sel_gpio_8=0x0;   Address(0x420[7:2])
13000   SPIWrite 0420,01    //buf_dir_ctrl_gpio_8=0x1;  Address(0x420[7:0])
13001   SPIWrite 08cd,00    //ovr_sel_intpi_tdd_en_fbcd=0x0;    Address(0x8cd[7:1])
13002   SPIWrite 08ce,09    //crossbar_sel_intpi_tdd_en_fbcd=0x9;
        Address(0x8ce[7:0],0x8cf[7:0])
13003   SPIWrite 0430,05    //preferred_input_sel_gpio_12=0x1;  Address(0x430[7:2])
13004   SPIWrite 0430,05    //buf_dir_ctrl_gpio_12=0x1;     Address(0x430[7:0])
13005   SPIWrite 0701,00    //ovr_sel_intbipi_spib1_sdi=0x0;    Address(0x701[7:1])
13006   SPIWrite 0514,21    //preferred_output_sel_gpio_69=0x1;     Address(0x514[7:5])
13007   SPIWrite 0514,22    //buf_dir_ctrl_gpio_69=0x2;     Address(0x514[7:0])
13008   SPIWrite 10f5,00    //ovr_sel_intpo_dac_sync_n_cd_1=0x0;    Address(0x10f5[7:1])
13009   SPIWrite 04e4,05    //preferred_input_sel_gpio_57=0x1;  Address(0x4e4[7:2])
13010   SPIWrite 04e4,05    //buf_dir_ctrl_gpio_57=0x1;     Address(0x4e4[7:0])
13011   SPIWrite 08a5,00    //ovr_sel_intpi_adc_sync_n_ab_1=0x0;    Address(0x8a5[7:1])
13012   SPIWrite 04c4,21    //preferred_output_sel_gpio_49=0x1;     Address(0x4c4[7:5])
13013   SPIWrite 04c4,22    //buf_dir_ctrl_gpio_49=0x2;     Address(0x4c4[7:0])
13014   SPIWrite 10c9,00    //ovr_sel_intpo_dac_sync_n_ab_1=0x0;    Address(0x10c9[7:1])
13015   SPIWrite 0510,01    //preferred_input_sel_gpio_68=0x0;  Address(0x510[7:2])
13016   SPIWrite 0510,01    //buf_dir_ctrl_gpio_68=0x1;     Address(0x510[7:0])
13017   SPIWrite 08ad,00    //ovr_sel_intpi_adc_sync_n_cd_0=0x0;    Address(0x8ad[7:1])
13018   SPIWrite 08ae,3e    //crossbar_sel_intpi_adc_sync_n_cd_0=0x3e;
        Address(0x8ae[7:0],0x8af[7:0])
13019   SPIWrite 050c,21    //preferred_output_sel_gpio_67=0x1;     Address(0x50c[7:5])
13020   SPIWrite 050c,22    //buf_dir_ctrl_gpio_67=0x2;     Address(0x50c[7:0])
13021   SPIWrite 10f1,00    //ovr_sel_intpo_dac_sync_n_cd_0=0x0;    Address(0x10f1[7:1])
13022   SPIWrite 040c,01    //preferred_input_sel_gpio_3=0x0;   Address(0x40c[7:2])
13023   SPIWrite 040c,01    //buf_dir_ctrl_gpio_3=0x1;  Address(0x40c[7:0])
13024   SPIWrite 08b9,00    //ovr_sel_intpi_tdd_en_txa=0x0;     Address(0x8b9[7:1])
13025   SPIWrite 08ba,04    //crossbar_sel_intpi_tdd_en_txa=0x4;
        Address(0x8ba[7:0],0x8bb[7:0])
13026   SPIWrite 040c,01    //preferred_input_sel_gpio_3=0x0;   Address(0x40c[7:2])
13027   SPIWrite 040c,01    //buf_dir_ctrl_gpio_3=0x1;  Address(0x40c[7:0])
13028   SPIWrite 08bd,00    //ovr_sel_intpi_tdd_en_txb=0x0;     Address(0x8bd[7:1])
13029   SPIWrite 08be,04    //crossbar_sel_intpi_tdd_en_txb=0x4;
        Address(0x8be[7:0],0x8bf[7:0])
13030   SPIWrite 040c,01    //preferred_input_sel_gpio_3=0x0;   Address(0x40c[7:2])
13031   SPIWrite 040c,01    //buf_dir_ctrl_gpio_3=0x1;  Address(0x40c[7:0])
13032   SPIWrite 08c1,00    //ovr_sel_intpi_tdd_en_txc=0x0;     Address(0x8c1[7:1])
13033   SPIWrite 08c2,04    //crossbar_sel_intpi_tdd_en_txc=0x4;
        Address(0x8c2[7:0],0x8c3[7:0])
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13034   SPIWrite 040c,01    //preferred_input_sel_gpio_3=0x0;   Address(0x40c[7:2])
13035   SPIWrite 040c,01    //buf_dir_ctrl_gpio_3=0x1;  Address(0x40c[7:0])
13036   SPIWrite 08c5,00    //ovr_sel_intpi_tdd_en_txd=0x0;     Address(0x8c5[7:1])
13037   SPIWrite 08c6,04    //crossbar_sel_intpi_tdd_en_txd=0x4;
        Address(0x8c6[7:0],0x8c7[7:0])
13038   SPIWrite 0454,05    //preferred_input_sel_gpio_21=0x1;  Address(0x454[7:2])
13039   SPIWrite 0454,05    //buf_dir_ctrl_gpio_21=0x1;     Address(0x454[7:0])
13040   SPIWrite 0905,00    //ovr_sel_intpi_global_pdn=0x0;     Address(0x905[7:1])
13041   SPIWrite 0444,05    //preferred_input_sel_gpio_17=0x1;  Address(0x444[7:2])
13042   SPIWrite 0444,05    //buf_dir_ctrl_gpio_17=0x1;     Address(0x444[7:0])
13043   SPIWrite 089d,00    //ovr_sel_intpi_spib1_clk=0x0;  Address(0x89d[7:1])
13044   SPIWrite 04cc,01    //preferred_input_sel_gpio_51=0x0;  Address(0x4cc[7:2])
13045   SPIWrite 04cc,01    //buf_dir_ctrl_gpio_51=0x1;     Address(0x4cc[7:0])
13046   SPIWrite 09d5,00    //ovr_sel_intpi_tdd_en_rxa=0x0;     Address(0x9d5[7:1])
13047   SPIWrite 09d6,2d    //crossbar_sel_intpi_tdd_en_rxa=0x2d;
        Address(0x9d6[7:0],0x9d7[7:0])
13048   SPIWrite 04cc,01    //preferred_input_sel_gpio_51=0x0;  Address(0x4cc[7:2])
13049   SPIWrite 04cc,01    //buf_dir_ctrl_gpio_51=0x1;     Address(0x4cc[7:0])
13050   SPIWrite 09d9,00    //ovr_sel_intpi_tdd_en_rxb=0x0;     Address(0x9d9[7:1])
13051   SPIWrite 09da,2d    //crossbar_sel_intpi_tdd_en_rxb=0x2d;
        Address(0x9da[7:0],0x9db[7:0])
13052   SPIWrite 04cc,01    //preferred_input_sel_gpio_51=0x0;  Address(0x4cc[7:2])
13053   SPIWrite 04cc,01    //buf_dir_ctrl_gpio_51=0x1;     Address(0x4cc[7:0])
13054   SPIWrite 09dd,00    //ovr_sel_intpi_tdd_en_rxc=0x0;     Address(0x9dd[7:1])
13055   SPIWrite 09de,2d    //crossbar_sel_intpi_tdd_en_rxc=0x2d;
        Address(0x9de[7:0],0x9df[7:0])
13056   SPIWrite 04cc,01    //preferred_input_sel_gpio_51=0x0;  Address(0x4cc[7:2])
13057   SPIWrite 04cc,01    //buf_dir_ctrl_gpio_51=0x1;     Address(0x4cc[7:0])
13058   SPIWrite 09e1,00    //ovr_sel_intpi_tdd_en_rxd=0x0;     Address(0x9e1[7:1])
13059   SPIWrite 09e2,2d    //crossbar_sel_intpi_tdd_en_rxd=0x2d;
        Address(0x9e2[7:0],0x9e3[7:0])
13060   SPIWrite 042c,21    //preferred_output_sel_gpio_11=0x1;     Address(0x42c[7:5])
13061   SPIWrite 042c,22    //buf_dir_ctrl_gpio_11=0x2;     Address(0x42c[7:0])
13062   SPIWrite 1005,00    //ovr_sel_intpo_spib1_sdo=0x0;  Address(0x1005[7:1])
13063   SPIWrite 0534,05    //preferred_input_sel_gpio_77=0x1;  Address(0x534[7:2])
13064   SPIWrite 0534,05    //buf_dir_ctrl_gpio_77=0x1;     Address(0x534[7:0])
13065   SPIWrite 08b1,00    //ovr_sel_intpi_adc_sync_n_cd_1=0x0;    Address(0x8b1[7:1])
13066   SPIWrite 0015,00    //io_wrap=0x0;  Address(0x15[7:4])
13067
13068   //STEP: sysrefJesdLinkup/step0
13069   SPIWrite 0016,03    //adc_jesd=0x3;     Address(0x16[7:0])
13070   SPIWrite 006d,06    //link0_init_state=0x0;     Address(0x6d[7:0])
13071   SPIWrite 006d,02    //link2_init_state=0x0;     Address(0x6d[7:2])
13072   SPIWrite 006d,00    //link1_init_state=0x0;     Address(0x6d[7:1])
13073   SPIWrite 006e,0e    //lane0_serdes_fifo_init_state=0x0;     Address(0x6e[7:0])
13074   SPIWrite 006e,0c    //lane1_serdes_fifo_init_state=0x0;     Address(0x6e[7:1])
13075   SPIWrite 006e,08    //lane2_serdes_fifo_init_state=0x0;     Address(0x6e[7:2])
13076   SPIWrite 006e,00    //lane3_serdes_fifo_init_state=0x0;     Address(0x6e[7:3])
13077   SPIWrite 0016,00    //adc_jesd=0x0;     Address(0x16[7:0])
13078   SPIWrite 0016,0c    //dac_jesd=0x3;     Address(0x16[7:2])
13079   SPIWrite 0020,02    //link0_init_state=0x0;     Address(0x20[7:0])
13080   SPIWrite 0020,00    //link1_init_state=0x0;     Address(0x20[7:1])
13081   SPIWrite 0016,00    //dac_jesd=0x0;     Address(0x16[7:2])
13082
13083   //STEP: sysrefJesdLinkup/step1
13084
13085   //START: Clearing Sysref Flags
13086
13087   SPIWrite 0016,03    //adc_jesd=0x3;     Address(0x16[7:0])
13088   SPIWrite 0124,08    //clear_jesd_clk_rx1_p0=0x1;    Address(0x124[7:3])
13089   SPIWrite 0128,08    //clear_jesd_sysref_rx1_p0=0x1;     Address(0x128[7:3])
13090   SPIWrite 0124,00    //clear_jesd_clk_rx1_p0=0x0;    Address(0x124[7:3])
13091   SPIWrite 0128,00    //clear_jesd_sysref_rx1_p0=0x0;     Address(0x128[7:3])
13092   SPIWrite 0016,00    //adc_jesd=0x0;     Address(0x16[7:0])
13093   SPIWrite 0016,04    //dac_jesd=0x1;     Address(0x16[7:2])
13094   SPIWrite 00eb,f0    //clear_jesd_sysref_flag=0xf;   Address(0xeb[7:4])
13095   SPIWrite 00eb,ff    //clear_jesd_clk_flag=0xf;  Address(0xeb[7:0])
13096   SPIWrite 00eb,0f    //clear_jesd_sysref_flag=0x0;   Address(0xeb[7:4])
13097   SPIWrite 00eb,00    //clear_jesd_clk_flag=0x0;  Address(0xeb[7:0])
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13098   SPIWrite 0016,00    //dac_jesd=0x0;     Address(0x16[7:2])
13099   SPIWrite 0015,02    //ana_4t4r=0x1;     Address(0x15[7:1])
13100   SPIWrite 00dc,10    //sys_ind_clr_tx_ab=0x1;    Address(0xdc[7:4])
13101   SPIWrite 00df,10    //sys_ind_clr_tx_cd=0x1;    Address(0xdf[7:4])
13102   SPIWrite 0100,10    //sys_ind_clr_digtop=0x1;   Address(0x100[7:4])
13103   SPIWrite 00c4,10    //sys_ind_clr_fb_ab=0x1;    Address(0xc4[7:4])
13104   SPIWrite 00c7,10    //sys_ind_clr_fb_cd=0x1;    Address(0xc7[7:4])
13105   SPIWrite 00cc,10    //sys_ind_clr_rx_ab=0x1;    Address(0xcc[7:4])
13106   SPIWrite 00cf,10    //sys_ind_clr_rx_cd=0x1;    Address(0xcf[7:4])
13107   SPIWrite 00d8,10    //sys_ind_clr_jesd_dac=0x1;     Address(0xd8[7:4])
13108   SPIWrite 00d4,10    //sys_ind_clr_jesd_adc=0x1;     Address(0xd4[7:4])
13109   SPIWrite 00dc,00    //sys_ind_clr_tx_ab=0x0;    Address(0xdc[7:4])
13110   SPIWrite 00df,00    //sys_ind_clr_tx_cd=0x0;    Address(0xdf[7:4])
13111   SPIWrite 0100,00    //sys_ind_clr_digtop=0x0;   Address(0x100[7:4])
13112   SPIWrite 00c4,00    //sys_ind_clr_fb_ab=0x0;    Address(0xc4[7:4])
13113   SPIWrite 00c7,00    //sys_ind_clr_fb_cd=0x0;    Address(0xc7[7:4])
13114   SPIWrite 00cc,00    //sys_ind_clr_rx_ab=0x0;    Address(0xcc[7:4])
13115   SPIWrite 00cf,00    //sys_ind_clr_rx_cd=0x0;    Address(0xcf[7:4])
13116   SPIWrite 00d8,00    //sys_ind_clr_jesd_dac=0x0;     Address(0xd8[7:4])
13117   SPIWrite 00d4,00    //sys_ind_clr_jesd_adc=0x0;     Address(0xd4[7:4])
13118
13119   //END: Done clearing Sysref Flags
13120
13121   SPIWrite 0015,00    //ana_4t4r=0x0;     Address(0x15[7:1])
13122
13123   //STEP: sysrefJesdLinkup/step2
13124
13125   //START: Sending Sysref to device
13126
13127
13128   //START: Requesting/releasing SPI Access to PLL Pages
13129
13130   SPIWrite 0015,40    //digtop=0x1;   Address(0x15[7:6])
13131   SPIWrite 0170,01    //pll_reg_spi_req_a=0x1;    Address(0x170[7:0])
13132   SPIWrite 0540,00    //pll_reg_spi_req_b1=0x0;   Address(0x540[7:0])
13133
13134   SPIPoll 0171,0,0,01
13135   SPIRead 0171
13136
13137   //Read  pll_reg_spi_a_ack=0x1(Meaning: );;  Address(0x171[7:0])
13138
13139
13140   //END: Requesting/releasing SPI Access to PLL Pages
13141
13142   SPIWrite 0015,00    //digtop=0x0;   Address(0x15[7:6])
13143   SPIWrite 0015,80    //timing_controller=0x1;    Address(0x15[7:7])
13144   SPIWrite 085b,00    //spare_reg_port=0x0;
      Address(0x858[7:0],0x859[7:0],0x85a[7:0],0x85b[7:0],0x85c[7:0])
13145   SPIWrite 085a,00
13146   SPIWrite 0859,00
13147   SPIWrite 0858,00
13148   SPIWrite 085b,00    //spare_reg_port=0x101;
      Address(0x858[7:0],0x859[7:0],0x85a[7:0],0x85b[7:0],0x85c[7:0])
13149   SPIWrite 085a,00
13150   SPIWrite 0859,01
13151   SPIWrite 0858,01
13152   SPIWrite 085b,00    //spare_reg_port=0x0;
      Address(0x858[7:0],0x859[7:0],0x85a[7:0],0x85b[7:0],0x85c[7:0])
13153   SPIWrite 085a,00
13154   SPIWrite 0859,00
13155   SPIWrite 0858,00
13156   SPIWrite 0015,00    //timing_controller=0x0;    Address(0x15[7:7])
13157   SPIWrite 0015,01    //pll=0x1;  Address(0x15[7:0])
13158   SPIWrite 006a,00    //LCMGEN_SYNC_ENA=0x0;  Address(0x6a[7:1])
13159   SPIWrite 006e,00    //LCMGEN_USE_SPI_SYSREF=0x0;    Address(0x6e[7:0])
13160   SPIWrite 006a,00    //LCMGEN_SYNC_ENA=0x0;  Address(0x6a[7:1])
13161   SPIWrite 006a,02    //LCMGEN_SYNC_ENA=0x1;  Address(0x6a[7:1])
13162   SPIWrite 0015,00    //pll=0x0;  Address(0x15[7:0])
13163
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13164   //STEP: sysrefJesdLinkup/step3
13165
13166   //External-Action: Give Sysref Here.
13167
13168
13169   WAIT 0.001
13170
13171   //START: Requesting/releasing SPI Access to PLL Pages
13172
13173   SPIWrite 0015,40    //digtop=0x1;   Address(0x15[7:6])
13174   SPIWrite 0170,00    //pll_reg_spi_req_a=0x0;    Address(0x170[7:0])
13175   SPIWrite 0540,00    //pll_reg_spi_req_b1=0x0;   Address(0x540[7:0])
13176
13177   WAIT 0.2
13178
13179   //END: Requesting/releasing SPI Access to PLL Pages
13180
13181
13182   //END: Sending Sysref to device
13183
13184   SPIWrite 0015,00    //digtop=0x0;   Address(0x15[7:6])
13185
13186   //STEP: sysrefJesdLinkup/step4
13187
13188   //START: Checking Sysref Flags
13189
13190   SPIWrite 0016,01    //adc_jesd=0x1;     Address(0x16[7:0])
13191   SPIRead 012c
13192
13193   //Read  monitor_jesd_clk_rx1_p0=0x1;    Address(0x12c[7:3])
13194
13195   SPIRead 0130
13196
13197   //Read  monitor_jesd_sysref_rx1_p0=0x1;     Address(0x130[7:3])
13198
13199
13200   //END: Done checking Sysref Flags
13201
13202   SPIWrite 0016,00    //adc_jesd=0x0;     Address(0x16[7:0])
13203
13204   //STEP: sysrefJesdLinkup/step5
13205   SPIWrite 0016,03    //adc_jesd=0x3;     Address(0x16[7:0])
13206   SPIWrite 0024,00    //jesd_clear_data=0x0;  Address(0x24[7:0])
13207   SPIWrite 00f0,0f    //alarms_serdes_fifo_errors_clear=0xf;  Address(0xf0[7:0])
13208   SPIWrite 00f0,00    //alarms_serdes_fifo_errors_clear=0x0;  Address(0xf0[7:0])
13209   SPIWrite 0016,00    //adc_jesd=0x0;     Address(0x16[7:0])
13210   SPIWrite 0016,0c    //dac_jesd=0x3;     Address(0x16[7:2])
13211   SPIWrite 0064,01    //jesd_clear_data=0x0;  Address(0x64[7:4])
13212   SPIWrite 0128,01    //clear_all_alarms=0x1;     Address(0x128[7:0])
13213   SPIWrite 0128,00    //clear_all_alarms=0x0;     Address(0x128[7:0])
13214   SPIWrite 0128,04    //clear_all_alarms_to_pap=0x1;  Address(0x128[7:2])
13215   SPIWrite 0128,00    //clear_all_alarms_to_pap=0x0;  Address(0x128[7:2])
13216   SPIWrite 0016,00    //dac_jesd=0x0;     Address(0x16[7:2])
13217   SPIWrite 0015,00    //digtop=0x0;   Address(0x15[7:6])
13218
13219   //STEP: postLinkUp/step0
13220
13221   //START: Writing Post Link up SERDES writes
13222
13223   SPIWrite 0016,60    //serdes_jesd=0x3;  Address(0x16[7:5])
13224   SPIWrite 0016,20    //serdes_jesd=0x1;  Address(0x16[7:5])
13225   SPIWrite 0016,60    //serdes_jesd=0x3;  Address(0x16[7:5])
13226   SPIWrite 41fb,02
13227   SPIWrite 41fa,6e
13228   SPIWrite 43fb,02
13229   SPIWrite 43fa,6e
13230   SPIWrite 45fb,02
13231   SPIWrite 45fa,6e
13232   SPIWrite 47fb,02
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13233   SPIWrite 47fa,6e
13234
13235   //END: Done writing Post Link up SERDES writes
13236
13237   SPIWrite 0016,00    //serdes_jesd=0x0;  Address(0x16[7:5])
13238
13239   //STEP: postLinkUp/step1
13240
13241   //START: Removing TDD Pin Overrides.
13242
13243   SPIWrite 0015,80    //timing_controller=0x1;    Address(0x15[7:7])
13244   SPIWrite 00ed,00    //reg_for_rxtdd=0x0;    Address(0xed[7:0])
13245   SPIWrite 00f5,00    //reg_for_fbtdd=0x0;    Address(0xf5[7:0])
13246   SPIWrite 00e5,0f    //reg_for_txtdd=0xf;    Address(0xe5[7:0])
13247
13248   //END: Removing TDD Pin Overrides.
13249
13250   SPIWrite 0015,00    //timing_controller=0x0;    Address(0x15[7:7])
13251   SPIWrite 0018,20    //macro=0x1;    Address(0x18[7:5])
13252   SPIRead 00f0
13253
13254   //Read  MACRO_READY=0x1;    Address(0xf0[7:0])
13255
13256
13257   SPIPoll 00f0,0,0,1
13258
13259   SPIWrite 00a3,00    //MACRO_OPERAND_REG0=0x10f;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
13260   SPIWrite 00a2,00
13261   SPIWrite 00a1,01
13262   SPIWrite 00a0,0f
13263   SPIWrite 00a7,00    //MACRO_OPERAND_REG1=0x1;
      Address(0xa4[7:0],0xa5[7:0],0xa6[7:0],0xa7[7:0],0xa8[7:0])
13264   SPIWrite 00a6,00
13265   SPIWrite 00a5,00
13266   SPIWrite 00a4,01
13267   SPIWrite 0193,52    //MACRO_OPCODE=0x52;    Address(0x193[7:0],0x194[7:0])
13268
13269   WAIT 0.001
13270   SPIRead 00f0
13271
13272   //Read  MACRO_DONE=0x1;     Address(0xf0[7:2])
13273
13274
13275   SPIPoll 00f0,2,2,4
13276
13277   SPIRead 00f0
13278
13279   //Read  MACRO_ERROR=0x0;    Address(0xf0[7:3])
13280
13281   SPIRead 00f1
13282
13283   //Read  MACRO_ERROR_OPCODE=0x0;     Address(0xf1[7:0],0xf2[7:0])
13284
13285   SPIRead 00f0
13286
13287   //Read  MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])
13288
13289   SPIRead 00f0
13290
13291   //Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;     Address(0xf0[7:5])
13292
13293   SPIRead 00f0
13294
13295   //Read  MACRO_ERROR_IN_OPERAND=0x0;     Address(0xf0[7:6])
13296
13297   SPIRead 00f0
13298
13299   //Read  MACRO_ERROR_IN_EXECUTION=0x0;   Address(0xf0[7:7])
```

```
13300
13301   SPIRead 00f3
13302   SPIRead 00f2
13303
13304   //Read  MACRO_ERROR_EXTENDED_CODE=0x0;  Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
13305
13306   SPIRead 00f7
13307   SPIRead 00f6
13308   SPIRead 00f5
13309   SPIRead 00f4
13310
13311   //Read  MACRO_ERROR_EXTENDED_CODE_2=0x0;
       Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
13312
13313   SPIRead 00f0
13314
13315   //Read  MACRO_READY=0x1;    Address(0xf0[7:0])
13316
13317
13318   SPIPoll 00f0,0,0,1
13319
13320   SPIWrite 00a3,00    //MACRO_OPERAND_REG0=0x30f;
       Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
13321   SPIWrite 00a2,00
13322   SPIWrite 00a1,03
13323   SPIWrite 00a0,0f
13324   SPIWrite 0193,53    //MACRO_OPCODE=0x53;    Address(0x193[7:0],0x194[7:0])
13325
13326   WAIT 0.001
13327   SPIRead 00f0
13328
13329   //Read  MACRO_DONE=0x1;     Address(0xf0[7:2])
13330
13331
13332   SPIPoll 00f0,2,2,4
13333
13334   SPIRead 00f0
13335
13336   //Read  MACRO_ERROR=0x0;    Address(0xf0[7:3])
13337
13338   SPIRead 00f1
13339
13340   //Read  MACRO_ERROR_OPCODE=0x0;     Address(0xf1[7:0],0xf2[7:0])
13341
13342   SPIRead 00f0
13343
13344   //Read  MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])
13345
13346   SPIRead 00f0
13347
13348   //Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;     Address(0xf0[7:5])
13349
13350   SPIRead 00f0
13351
13352   //Read  MACRO_ERROR_IN_OPERAND=0x0;     Address(0xf0[7:6])
13353
13354   SPIRead 00f0
13355
13356   //Read  MACRO_ERROR_IN_EXECUTION=0x0;   Address(0xf0[7:7])
13357
13358   SPIRead 00f3
13359   SPIRead 00f2
13360
13361   //Read  MACRO_ERROR_EXTENDED_CODE=0x0;  Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
13362
13363   SPIRead 00f7
13364   SPIRead 00f6
13365   SPIRead 00f5
13366   SPIRead 00f4
```

```
13367
13368   //Read  MACRO_ERROR_EXTENDED_CODE_2=0x0;
        Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
13369
13370   SPIRead 00f0
13371
13372   //Read  MACRO_READY=0x1;    Address(0xf0[7:0])
13373
13374
13375   SPIPoll 00f0,0,0,1
13376
13377   SPIWrite 00a3,00    //MACRO_OPERAND_REG0=0x0;
        Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
13378   SPIWrite 00a2,00
13379   SPIWrite 00a1,00
13380   SPIWrite 00a0,00
13381   SPIWrite 0193,90    //MACRO_OPCODE=0x90;    Address(0x193[7:0],0x194[7:0])
13382
13383   WAIT 0.001
13384   SPIRead 00f0
13385
13386   //Read  MACRO_DONE=0x1;     Address(0xf0[7:2])
13387
13388
13389   SPIPoll 00f0,2,2,4
13390
13391   SPIRead 00f0
13392
13393   //Read  MACRO_ERROR=0x0;    Address(0xf0[7:3])
13394
13395   SPIRead 00f1
13396
13397   //Read  MACRO_ERROR_OPCODE=0x0;     Address(0xf1[7:0],0xf2[7:0])
13398
13399   SPIRead 00f0
13400
13401   //Read  MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])
13402
13403   SPIRead 00f0
13404
13405   //Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;     Address(0xf0[7:5])
13406
13407   SPIRead 00f0
13408
13409   //Read  MACRO_ERROR_IN_OPERAND=0x0;     Address(0xf0[7:6])
13410
13411   SPIRead 00f0
13412
13413   //Read  MACRO_ERROR_IN_EXECUTION=0x0;   Address(0xf0[7:7])
13414
13415   SPIRead 00f3
13416   SPIRead 00f2
13417
13418   //Read  MACRO_ERROR_EXTENDED_CODE=0x0;  Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
13419
13420   SPIRead 00f7
13421   SPIRead 00f6
13422   SPIRead 00f5
13423   SPIRead 00f4
13424
13425   //Read  MACRO_ERROR_EXTENDED_CODE_2=0x0;
        Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
13426
13427   SPIWrite 0144,08    //all_addr_high=0x2;    Address(0x144[7:2])
13428   SPIWrite 0018,00    //macro=0x0;    Address(0x18[7:5])
13429   SPIWrite 0018,08    //cm4top_dram=0x1;  Address(0x18[7:3])
13430   SPIWrite 1f8f,64
13431   SPIWrite 0018,00    //cm4top_dram=0x0;  Address(0x18[7:3])
13432   SPIWrite 0018,20    //macro=0x1;    Address(0x18[7:5])
```

```
13433   SPIRead 00f0
13434
13435   //Read  MACRO_READY=0x1;    Address(0xf0[7:0])
13436
13437
13438   SPIPoll 00f0,0,0,1
13439
13440   SPIWrite 00a3,00    //MACRO_OPERAND_REG0=0x1;
        Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
13441   SPIWrite 00a2,00
13442   SPIWrite 00a1,00
13443   SPIWrite 00a0,01
13444   SPIWrite 0193,90    //MACRO_OPCODE=0x90;    Address(0x193[7:0],0x194[7:0])
13445
13446   WAIT 0.001
13447   SPIRead 00f0
13448
13449   //Read  MACRO_DONE=0x1;     Address(0xf0[7:2])
13450
13451
13452   SPIPoll 00f0,2,2,4
13453
13454   SPIRead 00f0
13455
13456   //Read  MACRO_ERROR=0x0;    Address(0xf0[7:3])
13457
13458   SPIRead 00f1
13459
13460   //Read  MACRO_ERROR_OPCODE=0x0;     Address(0xf1[7:0],0xf2[7:0])
13461
13462   SPIRead 00f0
13463
13464   //Read  MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])
13465
13466   SPIRead 00f0
13467
13468   //Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;     Address(0xf0[7:5])
13469
13470   SPIRead 00f0
13471
13472   //Read  MACRO_ERROR_IN_OPERAND=0x0;     Address(0xf0[7:6])
13473
13474   SPIRead 00f0
13475
13476   //Read  MACRO_ERROR_IN_EXECUTION=0x0;   Address(0xf0[7:7])
13477
13478   SPIRead 00f3
13479   SPIRead 00f2
13480
13481   //Read  MACRO_ERROR_EXTENDED_CODE=0x0;  Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
13482
13483   SPIRead 00f7
13484   SPIRead 00f6
13485   SPIRead 00f5
13486   SPIRead 00f4
13487
13488   //Read  MACRO_ERROR_EXTENDED_CODE_2=0x0;
        Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
13489
13490   SPIRead 00f0
13491
13492   //Read  MACRO_READY=0x1;    Address(0xf0[7:0])
13493
13494
13495   SPIPoll 00f0,0,0,1
13496
13497   SPIWrite 00a3,01    //MACRO_OPERAND_REG0=0x101010f;
        Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
13498   SPIWrite 00a2,01
```

```
13499   SPIWrite 00a1,01
13500   SPIWrite 00a0,0f
13501   SPIWrite 0193,9f    //MACRO_OPCODE=0x9f;    Address(0x193[7:0],0x194[7:0])
13502
13503   WAIT 0.001
13504   SPIRead 00f0
13505
13506   //Read  MACRO_DONE=0x1;     Address(0xf0[7:2])
13507
13508
13509   SPIPoll 00f0,2,2,4
13510
13511   SPIRead 00f0
13512
13513   //Read  MACRO_ERROR=0x0;    Address(0xf0[7:3])
13514
13515   SPIRead 00f1
13516
13517   //Read  MACRO_ERROR_OPCODE=0x0;     Address(0xf1[7:0],0xf2[7:0])
13518
13519   SPIRead 00f0
13520
13521   //Read  MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])
13522
13523   SPIRead 00f0
13524
13525   //Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;     Address(0xf0[7:5])
13526
13527   SPIRead 00f0
13528
13529   //Read  MACRO_ERROR_IN_OPERAND=0x0;     Address(0xf0[7:6])
13530
13531   SPIRead 00f0
13532
13533   //Read  MACRO_ERROR_IN_EXECUTION=0x0;   Address(0xf0[7:7])
13534
13535   SPIRead 00f3
13536   SPIRead 00f2
13537
13538   //Read  MACRO_ERROR_EXTENDED_CODE=0x0;  Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
13539
13540   SPIRead 00f7
13541   SPIRead 00f6
13542   SPIRead 00f5
13543   SPIRead 00f4
13544
13545   //Read  MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
13546
13547   SPIRead 00f0
13548
13549   //Read  MACRO_READY=0x1;    Address(0xf0[7:0])
13550
13551
13552   SPIPoll 00f0,0,0,1
13553
13554   SPIWrite 00a3,00    //MACRO_OPERAND_REG0=0xb010f;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
13555   SPIWrite 00a2,0b
13556   SPIWrite 00a1,01
13557   SPIWrite 00a0,0f
13558   SPIWrite 0193,49    //MACRO_OPCODE=0x49;    Address(0x193[7:0],0x194[7:0])
13559
13560   WAIT 0.001
13561   SPIRead 00f0
13562
13563   //Read  MACRO_DONE=0x1;     Address(0xf0[7:2])
13564
13565
```

```
13566   SPIPoll 00f0,2,2,4
13567
13568   SPIRead 00f0
13569
13570   //Read  MACRO_ERROR=0x0;    Address(0xf0[7:3])
13571
13572   SPIRead 00f1
13573
13574   //Read  MACRO_ERROR_OPCODE=0x0;     Address(0xf1[7:0],0xf2[7:0])
13575
13576   SPIRead 00f0
13577
13578   //Read  MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])
13579
13580   SPIRead 00f0
13581
13582   //Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;     Address(0xf0[7:5])
13583
13584   SPIRead 00f0
13585
13586   //Read  MACRO_ERROR_IN_OPERAND=0x0;     Address(0xf0[7:6])
13587
13588   SPIRead 00f0
13589
13590   //Read  MACRO_ERROR_IN_EXECUTION=0x0;   Address(0xf0[7:7])
13591
13592   SPIRead 00f3
13593   SPIRead 00f2
13594
13595   //Read  MACRO_ERROR_EXTENDED_CODE=0x0;  Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
13596
13597   SPIRead 00f7
13598   SPIRead 00f6
13599   SPIRead 00f5
13600   SPIRead 00f4
13601
13602   //Read  MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
13603
13604   SPIRead 00f0
13605
13606   //Read  MACRO_READY=0x1;    Address(0xf0[7:0])
13607
13608
13609   SPIPoll 00f0,0,0,1
13610
13611   SPIWrite 00a3,00    //MACRO_OPERAND_REG0=0x1010f;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
13612   SPIWrite 00a2,01
13613   SPIWrite 00a1,01
13614   SPIWrite 00a0,0f
13615   SPIWrite 0193,4b    //MACRO_OPCODE=0x4b;    Address(0x193[7:0],0x194[7:0])
13616
13617   WAIT 0.001
13618   SPIRead 00f0
13619
13620   //Read  MACRO_DONE=0x1;     Address(0xf0[7:2])
13621
13622
13623   SPIPoll 00f0,2,2,4
13624
13625   SPIRead 00f0
13626
13627   //Read  MACRO_ERROR=0x0;    Address(0xf0[7:3])
13628
13629   SPIRead 00f1
13630
13631   //Read  MACRO_ERROR_OPCODE=0x0;     Address(0xf1[7:0],0xf2[7:0])
13632
```

```
13633   SPIRead 00f0
13634
13635   //Read  MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])
13636
13637   SPIRead 00f0
13638
13639   //Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;     Address(0xf0[7:5])
13640
13641   SPIRead 00f0
13642
13643   //Read  MACRO_ERROR_IN_OPERAND=0x0;     Address(0xf0[7:6])
13644
13645   SPIRead 00f0
13646
13647   //Read  MACRO_ERROR_IN_EXECUTION=0x0;   Address(0xf0[7:7])
13648
13649   SPIRead 00f3
13650   SPIRead 00f2
13651
13652   //Read  MACRO_ERROR_EXTENDED_CODE=0x0;  Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
13653
13654   SPIRead 00f7
13655   SPIRead 00f6
13656   SPIRead 00f5
13657   SPIRead 00f4
13658
13659   //Read  MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
13660
13661   SPIRead 00f0
13662
13663   //Read  MACRO_READY=0x1;    Address(0xf0[7:0])
13664
13665
13666   SPIPoll 00f0,0,0,1
13667
13668   SPIWrite 00a3,01    //MACRO_OPERAND_REG0=0x10100ff;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
13669   SPIWrite 00a2,01
13670   SPIWrite 00a1,00
13671   SPIWrite 00a0,ff
13672   SPIWrite 00a7,00    //MACRO_OPERAND_REG1=0x0;
      Address(0xa4[7:0],0xa5[7:0],0xa6[7:0],0xa7[7:0],0xa8[7:0])
13673   SPIWrite 00a6,00
13674   SPIWrite 00a5,00
13675   SPIWrite 00a4,00
13676   SPIWrite 0193,13    //MACRO_OPCODE=0x13;    Address(0x193[7:0],0x194[7:0])
13677
13678   WAIT 0.001
13679   SPIRead 00f0
13680
13681   //Read  MACRO_DONE=0x0;     Address(0xf0[7:2])
13682
13683   SPIRead 00f0
13684
13685   //Read  MACRO_DONE=0x0;     Address(0xf0[7:2])
13686
13687   SPIRead 00f0
13688
13689   //Read  MACRO_DONE=0x0;     Address(0xf0[7:2])
13690
13691   SPIRead 00f0
13692
13693   //Read  MACRO_DONE=0x0;     Address(0xf0[7:2])
13694
13695   SPIRead 00f0
13696
13697   //Read  MACRO_DONE=0x0;     Address(0xf0[7:2])
13698
```

```
13699   SPIRead 00f0
13700
13701   //Read  MACRO_DONE=0x0;     Address(0xf0[7:2])
13702
13703   SPIRead 00f0
13704
13705   //Read  MACRO_DONE=0x0;     Address(0xf0[7:2])
13706
13707   SPIRead 00f0
13708
13709   //Read  MACRO_DONE=0x0;     Address(0xf0[7:2])
13710
13711   SPIRead 00f0
13712
13713   //Read  MACRO_DONE=0x0;     Address(0xf0[7:2])
13714
13715   SPIRead 00f0
13716
13717   //Read  MACRO_DONE=0x0;     Address(0xf0[7:2])
13718
13719   SPIRead 00f0
13720
13721   //Read  MACRO_DONE=0x0;     Address(0xf0[7:2])
13722
13723   SPIRead 00f0
13724
13725   //Read  MACRO_DONE=0x1;     Address(0xf0[7:2])
13726
13727
13728   SPIPoll 00f0,2,2,4
13729
13730   SPIRead 00f0
13731
13732   //Read  MACRO_ERROR=0x0;    Address(0xf0[7:3])
13733
13734   SPIRead 00f1
13735
13736   //Read  MACRO_ERROR_OPCODE=0x0;     Address(0xf1[7:0],0xf2[7:0])
13737
13738   SPIRead 00f0
13739
13740   //Read  MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])
13741
13742   SPIRead 00f0
13743
13744   //Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;     Address(0xf0[7:5])
13745
13746   SPIRead 00f0
13747
13748   //Read  MACRO_ERROR_IN_OPERAND=0x0;     Address(0xf0[7:6])
13749
13750   SPIRead 00f0
13751
13752   //Read  MACRO_ERROR_IN_EXECUTION=0x0;   Address(0xf0[7:7])
13753
13754   SPIRead 00f3
13755   SPIRead 00f2
13756
13757   //Read  MACRO_ERROR_EXTENDED_CODE=0x0;  Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
13758
13759   SPIRead 00f7
13760   SPIRead 00f6
13761   SPIRead 00f5
13762   SPIRead 00f4
13763
13764   //Read  MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
13765
13766   SPIWrite 0018,00    //macro=0x0;    Address(0x18[7:5])
```

```
13767   SPIWrite 0012,01    //rxdig=0x1;    Address(0x12[7:0])
13768   SPIWrite 14c4,00    //dc_corr_fw_pause=0x0;     Address(0x14c4[7:0])
13769   SPIWrite 0012,02    //rxdig=0x2;    Address(0x12[7:0])
13770   SPIWrite 14c4,00    //dc_corr_fw_pause=0x0;     Address(0x14c4[7:0])
13771   SPIWrite 0012,04    //rxdig=0x4;    Address(0x12[7:0])
13772   SPIWrite 14c4,00    //dc_corr_fw_pause=0x0;     Address(0x14c4[7:0])
13773   SPIWrite 0012,08    //rxdig=0x8;    Address(0x12[7:0])
13774   SPIWrite 14c4,00    //dc_corr_fw_pause=0x0;     Address(0x14c4[7:0])
13775   SPIWrite 0012,00    //rxdig=0x0;    Address(0x12[7:0])
13776   SPIWrite 0012,10    //fbdig=0x1;    Address(0x12[7:4])
13777   SPIWrite 14c4,00    //dc_corr_fw_pause=0x0;     Address(0x14c4[7:0])
13778   SPIWrite 0012,20    //fbdig=0x2;    Address(0x12[7:4])
13779   SPIWrite 14c4,00    //dc_corr_fw_pause=0x0;     Address(0x14c4[7:0])
13780
13781   //START: Removing TDD Pin Overrides.
13782
13783   SPIWrite 0012,00    //fbdig=0x0;    Address(0x12[7:4])
13784   SPIWrite 0015,80    //timing_controller=0x1;    Address(0x15[7:7])
13785   SPIWrite 00ed,00    //reg_for_rxtdd=0x0;    Address(0xed[7:0])
13786   SPIWrite 00f5,03    //reg_for_fbtdd=0x3;    Address(0xf5[7:0])
13787   SPIWrite 00e5,00    //reg_for_txtdd=0x0;    Address(0xe5[7:0])
13788
13789   //END: Removing TDD Pin Overrides.
13790
13791
13792   //START: Removing TDD Pin Overrides.
13793
13794   SPIWrite 00ed,0f    //reg_for_rxtdd=0xf;    Address(0xed[7:0])
13795   SPIWrite 00f5,00    //reg_for_fbtdd=0x0;    Address(0xf5[7:0])
13796   SPIWrite 00e5,00    //reg_for_txtdd=0x0;    Address(0xe5[7:0])
13797
13798   //END: Removing TDD Pin Overrides.
13799
13800
13801   //START: Removing TDD Pin Overrides.
13802
13803   SPIWrite 00ec,00    //use_reg_for_rxtdd=0x0;    Address(0xec[7:0])
13804   SPIWrite 00f4,00    //use_reg_for_fbtdd=0x0;    Address(0xf4[7:0])
13805   SPIWrite 00e4,00    //use_reg_for_txtdd=0x0;    Address(0xe4[7:0])
13806
13807   //END: Removing TDD Pin Overrides.
13808
13809   SPIWrite 0015,00    //timing_controller=0x0;    Address(0x15[7:7])
13810   SPIWrite 0018,20    //macro=0x1;    Address(0x18[7:5])
13811   SPIRead 00f0
13812
13813   //Read  MACRO_READY=0x1;    Address(0xf0[7:0])
13814
13815
13816   SPIPoll 00f0,0,0,1
13817
13818   SPIWrite 00a3,00    //MACRO_OPERAND_REG0=0x0;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
13819   SPIWrite 00a2,00
13820   SPIWrite 00a1,00
13821   SPIWrite 00a0,00
13822   SPIWrite 0193,15    //MACRO_OPCODE=0x15;    Address(0x193[7:0],0x194[7:0])
13823
13824   WAIT 0.001
13825   SPIRead 00f0
13826
13827   //Read  MACRO_DONE=0x1;     Address(0xf0[7:2])
13828
13829
13830   SPIPoll 00f0,2,2,4
13831
13832   SPIRead 00f0
13833
13834   //Read  MACRO_ERROR=0x0;    Address(0xf0[7:3])
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13835
13836   SPIRead 00f1
13837
13838   //Read  MACRO_ERROR_OPCODE=0x0;     Address(0xf1[7:0],0xf2[7:0])
13839
13840   SPIRead 00f0
13841
13842   //Read  MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])
13843
13844   SPIRead 00f0
13845
13846   //Read  MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;     Address(0xf0[7:5])
13847
13848   SPIRead 00f0
13849
13850   //Read  MACRO_ERROR_IN_OPERAND=0x0;     Address(0xf0[7:6])
13851
13852   SPIRead 00f0
13853
13854   //Read  MACRO_ERROR_IN_EXECUTION=0x0;   Address(0xf0[7:7])
13855
13856   SPIRead 00f3
13857   SPIRead 00f2
13858
13859   //Read  MACRO_ERROR_EXTENDED_CODE=0x0;  Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
13860
13861   SPIRead 00f7
13862   SPIRead 00f6
13863   SPIRead 00f5
13864   SPIRead 00f4
13865
13866   //Read  MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
13867
13868   SPIWrite 0018,00    //macro=0x0;    Address(0x18[7:5])
13869
13870   //STEP: postLinkUp/step2
13871   SPIWrite 0016,03    //adc_jesd=0x3;     Address(0x16[7:0])
13872   SPIWrite 0024,00    //jesd_clear_data=0x0;  Address(0x24[7:0])
13873   SPIWrite 00f0,0f    //alarms_serdes_fifo_errors_clear=0xf;  Address(0xf0[7:0])
13874   SPIWrite 00f0,00    //alarms_serdes_fifo_errors_clear=0x0;  Address(0xf0[7:0])
13875   SPIWrite 0016,00    //adc_jesd=0x0;     Address(0x16[7:0])
13876   SPIWrite 0016,0c    //dac_jesd=0x3;     Address(0x16[7:2])
13877   SPIWrite 0064,01    //jesd_clear_data=0x0;  Address(0x64[7:4])
13878   SPIWrite 0128,01    //clear_all_alarms=0x1;     Address(0x128[7:0])
13879   SPIWrite 0128,00    //clear_all_alarms=0x0;     Address(0x128[7:0])
13880   SPIWrite 0128,04    //clear_all_alarms_to_pap=0x1;  Address(0x128[7:2])
13881   SPIWrite 0128,00    //clear_all_alarms_to_pap=0x0;  Address(0x128[7:2])
13882   SPIWrite 0016,00    //dac_jesd=0x0;     Address(0x16[7:2])
13883   SPIWrite 0019,30    //txdig=0x3;    Address(0x19[7:4])
13884   SPIWrite 0a40,0f    //HBF59OvrClr=0xf;  Address(0xa40[7:0])
13885   SPIWrite 0a41,0f    //HBF23HROvrClr=0xf;    Address(0xa41[7:0])
13886   SPIWrite 0a44,0f    //mixerOvrClr=0xf;  Address(0xa44[7:0])
13887   SPIWrite 0a45,0f    //isincOvrClr=0xf;  Address(0xa45[7:0])
13888   SPIWrite 0a46,0f    //dacDitherOvrClr=0xf;  Address(0xa46[7:0])
13889   SPIWrite 0a40,00    //HBF59OvrClr=0x0;  Address(0xa40[7:0])
13890   SPIWrite 0a41,00    //HBF23HROvrClr=0x0;    Address(0xa41[7:0])
13891   SPIWrite 0a44,00    //mixerOvrClr=0x0;  Address(0xa44[7:0])
13892   SPIWrite 0a45,00    //isincOvrClr=0x0;  Address(0xa45[7:0])
13893   SPIWrite 0a46,00    //dacDitherOvrClr=0x0;  Address(0xa46[7:0])
13894   SPIWrite 054d,07    //txa_pap_alarm_clr=0x7ff;  Address(0x54c[2:0],0x54d[7:0])
13895   SPIWrite 054c,ff
13896   SPIWrite 0580,07    //pap_det_alarm_clr=0x7;    Address(0x580[7:0])
13897   SPIWrite 0589,07    //ip_pap_det_alarm_clr=0x7;     Address(0x589[7:0])
13898   SPIWrite 06b4,01    //pap_hw_alarm_act_alc_clr=0x1;     Address(0x6b4[7:0])
13899   SPIWrite 06b4,03    //pap_hw_alarm_act_lmt_clr=0x1;     Address(0x6b4[7:1])
13900   SPIWrite 054d,00    //txa_pap_alarm_clr=0x0;    Address(0x54c[2:0],0x54d[7:0])
13901   SPIWrite 054c,00
13902   SPIWrite 0580,00    //pap_det_alarm_clr=0x0;    Address(0x580[7:0])
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```
SPIWrite 0589,00    //ip_pap_det_alarm_clr=0x0;     Address(0x589[7:0])
SPIWrite 06b4,02    //pap_hw_alarm_act_alc_clr=0x0;     Address(0x6b4[7:0])
SPIWrite 06b4,00    //pap_hw_alarm_act_lmt_clr=0x0;     Address(0x6b4[7:1])
SPIWrite 052c,1f    //pap_alarm_clr=0x1f;   Address(0x52c[7:0])
SPIWrite 052c,00    //pap_alarm_clr=0x0;    Address(0x52c[7:0])
SPIWrite 0019,00    //txdig=0x0;    Address(0x19[7:4])

//STEP: dlJesdLinkupCheck/step0

//START: Reading the JESD RX states to check if link is established


WAIT 0.001
SPIWrite 0016,04    //dac_jesd=0x1;     Address(0x16[7:2])
SPIRead 011b
SPIRead 011a
SPIRead 0119
SPIRead 0118
SPIRead 011f
SPIRead 011e
SPIRead 011d
SPIRead 011c

//Read  alarms=0x0;
Address(0x118[7:0],0x119[7:0],0x11a[7:0],0x11b[7:0],0x11c[7:0],0x11c[7:0],0x11d[7:0],0x11
e[7:0],0x11f[7:0],0x120[7:0])

SPIRead 00ee

//Read  comma_align_lock_flag=0x1;  Address(0xee[7:0])

SPIRead 00a2

//Read  jesd_cs_state=0x2;  Address(0xa2[7:0],0xa3[7:0])

SPIRead 00a6

//Read  jesd_buf_state=0x3;     Address(0xa6[7:0],0xa7[7:0])


//END: Done reading the JESD RX states to check if link is established


//START: Reading the JESD RX states to check if link is established


WAIT 0.001
SPIWrite 0016,08    //dac_jesd=0x2;     Address(0x16[7:2])
SPIRead 011b
SPIRead 011a
SPIRead 0119
SPIRead 0118
SPIRead 011f
SPIRead 011e
SPIRead 011d
SPIRead 011c

//Read  alarms=0x200000000;
Address(0x118[7:0],0x119[7:0],0x11a[7:0],0x11b[7:0],0x11c[7:0],0x11c[7:0],0x11d[7:0],0x11
e[7:0],0x11f[7:0],0x120[7:0])

SPIRead 00ee

//Read  comma_align_lock_flag=0x1;  Address(0xee[7:0])

SPIRead 00a2

//Read  jesd_cs_state=0x2;  Address(0xa2[7:0],0xa3[7:0])

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```
13968   SPIRead 00a6
13969
13970   //Read  jesd_buf_state=0x3;     Address(0xa6[7:0],0xa7[7:0])
13971
13972
13973   //END: Done reading the JESD RX states to check if link is established
13974
13975   SPIWrite 0016,00    //dac_jesd=0x0;     Address(0x16[7:2])
13976
13977   //END: Device Config Complete
13978
13979
```