Interfacing op amps to high-speed DACs, Part 2: Current-sourcing DACs

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Introduction

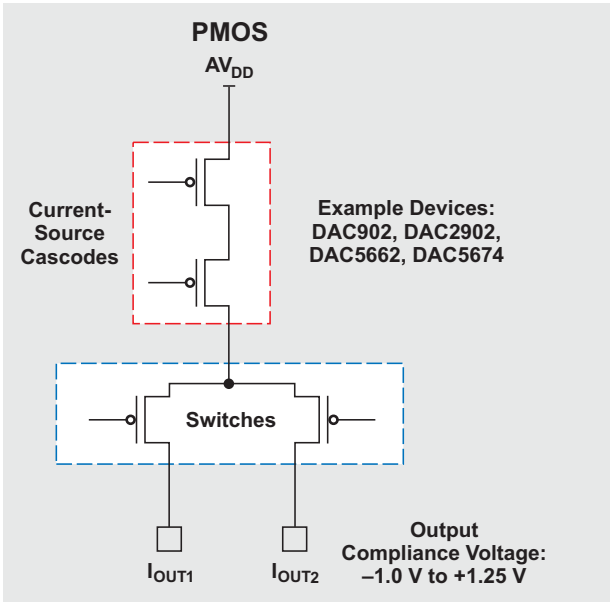
Most high-speed DACs are current-steering DACs that are designed with complementary outputs that either source or sink current. Part 1 (see Reference 1) of this three-part article series discussed the interface between a current-sinking DAC and an op amp. This article, Part 2, discusses the interface between a current-sourcing DAC and an op amp. This interface allows the designer to use the full compliance voltage range of the DAC. Part 3, which will appear in a future issue of the *Analog Applications Journal*, will discuss interfacing a current-sourcing DAC and an op amp by using the more popular configuration that simply terminates to ground. This article series focuses on using high-speed DACs in end equipment that requires DC coupling, like signal generators with frequency bandwidths of up to 100 MHz and a single-ended output. In these cases, high-speed op amps can provide a good solution for converting the complementary-current output from a high-speed DAC to a voltage that can drive the signal output.

It is assumed that the reader is familiar with the operation of complementary-current-steering DACs. If further information is needed, please see Reference 1 for an overview. The design approach for Part 2 is the same as for Part 1, except that a current-sourcing DAC was used to derive the design equations instead of the current-sinking DAC used in Part 1. Because of this, about half of the equations are the same and about half are modified.

Architecture and compliance voltage of current-sourcing DACs

Figure 11 shows a simplified example of a PMOS current source and lists a few devices that use it. The compliance voltage shown is the voltage range at the DAC outputs within which a device will perform as specified. Higher voltages tend to shut down the outputs, and lower voltages have the potential to cause breakdown. Both of these should be avoided to provide the best performance and long term-reliability.

Figure 11. Simplified PMOS current source



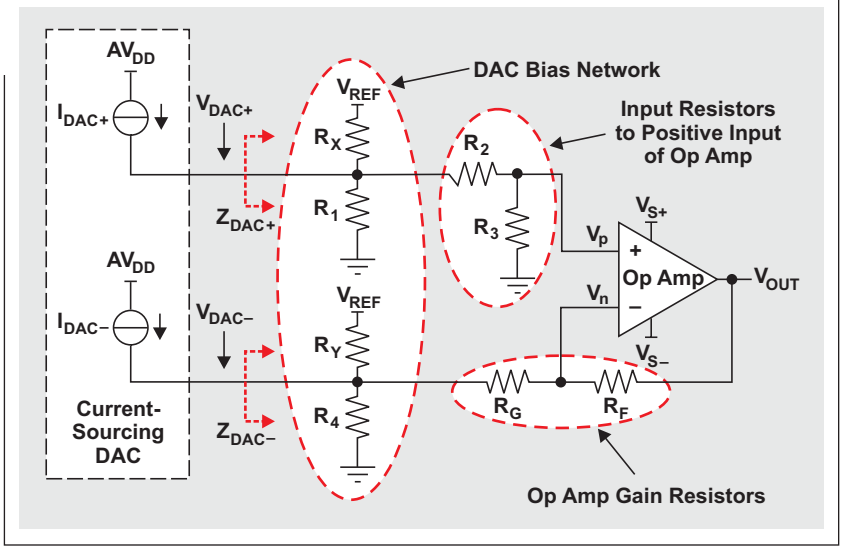
Generally the output is terminated via some impedance to ground. This impedance supplies a current path needed for the array, and the voltage drop across the same impedance can be used as a voltage output. The impedance can be constructed in various ways; it can be a simple resistor divider, a transformer-coupled impedance, or an active circuit like an op amp. This article focuses on the interface to an op amp.

Op amp interface

A proposed op amp interface is shown in Figure 12. This circuit will provide biasing of the DAC outputs, convert the DAC currents to voltages, and provide a single-ended output voltage. The op amp is the active amplifier element for the circuit and is configured as a difference amplifier.

- I_{DAC+} and I_{DAC-} are the current outputs from the DAC.
- R_2 and R_3 are input resistors to the positive input of the op amp.
- R_G and R_F are the main gain-setting resistors for the op amp.
- R_X, R_1, R_Y, and R_4 provide bias and impedance termination for the DAC outputs.
- V_{DAC+} and V_{DAC-} are the voltages at the outputs of the DAC.
- V_p and V_n are the input terminals of the op amp.
- V_{S+} and V_{S-} are the power supplies to the op amp.

Figure 12. Proposed circuit for an op amp interface



Proper component selection will provide the impedance required to maintain voltage compliance with maximum amplitude and balance for the best performance. The analysis of this circuit follows from Part 1 with only minor changes due to the change in polarity of the DAC current (sourcing versus sinking) and the change in compliance voltage range around ground instead of AV_{DD}. The circuit in Figure 12 enables the designer to use the maximum compliance voltage range of the DAC.

The motivation for this interface design is to balance the input voltages to the difference-amplifier circuit to suppress second-order harmonics, and little impact is expected on third-order harmonics. Also, because it allows higher voltage swings at the DAC output than simple termination to ground, the gain of the op amp will be lower given the same output-voltage requirement.

Analysis of positive side

Figure 13 shows the analysis circuit for the positive side. The node equation at the V_{DAC+} output is the same as in Part 1 but with a change in the polarity of I_{DAC+}:

$$\frac{V_{DAC+} - V_{REF}}{R_X} + \frac{V_{DAC+}}{R_1} + \frac{V_{DAC+}}{R_2 + R_3} - I_{DAC+} = 0 \quad \textbf{(20)}$$

The equation for the DAC output impedance stays the same:

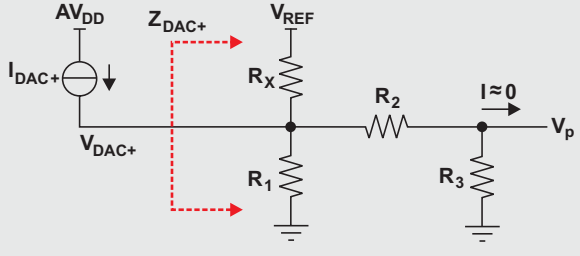
$$Z_{DAC+} = R_X \parallel R_1 \parallel (R_2 + R_3) \quad \textbf{(21)}$$

To solve Equations 20 and 21, which are simultaneous equations with more variables than equations, the designer must choose or identify values based on other design criteria. The following assumptions are made in this article:

1. The DAC output current, I_{DAC+}, and the voltage swing, V_{DAC+}, are defined by the designer to set a target value for Z_{DAC+}.
2. An existing circuit voltage or other known voltage is used for V_{REF}.
3. In a difference amplifier, R_3/R_2 needs to equal R_F/R_G to balance the gain of the amplifier.*
4. The equations will be solved for the condition where the DAC current on the positive side is zero (I_{DAC+} = 0 mA). This in turn will set the DAC voltage on the positive side to its minimum value, $V_{DAC+} = V_{DAC+(min)}$. Note that this value is different from that of the current-sinking DAC in Part 1, where setting I_{DAC+} = 0 mA led to $V_{DAC+} = V_{DAC+(max)}$.

*Note that in a voltage-feedback op amp, it is desirable to make the impedance at V_p equal to that at V_n in order to cancel voltage offset caused by the input bias current. In a current-feedback op amp, the input bias currents are not correlated; so it is acceptable not to balance these impedances, but it may be desirable to minimize them.

Figure 13. Positive side of analysis circuit



With these constraints, algebra and simultaneous-equation techniques can be applied to Equations 20 and 21 to solve for $1/R_1$:

$$\frac{1}{R_1} = \frac{1}{Z_{DAC+}\left(1+\frac{1}{\frac{V_{REF}}{V_{DAC+(min)}}-1}\right)} - \frac{1}{R_2+R_3} \quad (22)$$

The known value for R_1 can be substituted into Equation 21, which can then be rearranged to find $1/R_X$. The result is exactly the same as in Part 1:

$$\frac{1}{R_X} = \frac{1}{Z_{DAC+}} - \frac{1}{R_1} - \frac{1}{R_2+R_3} \quad (23)$$

Analysis of negative side

Figure 14 shows the analysis circuit for the negative side. The node equation at the V_{DAC-} output is the same as in Part 1 except for the DAC current's change in polarity:

$$\frac{V_{DAC-}-V_{REF}}{R_Y} + \frac{V_{DAC-}}{R_4} + \frac{V_{DAC-}-V_n}{R_G+R_3} - I_{DAC-} = 0 \quad (24)$$

The equation for the DAC output impedance stays the same:

$$Z_{DAC-} = \frac{V_{DAC-}}{I_{DAC-}} \quad (25)$$

With substitution and rearrangement,

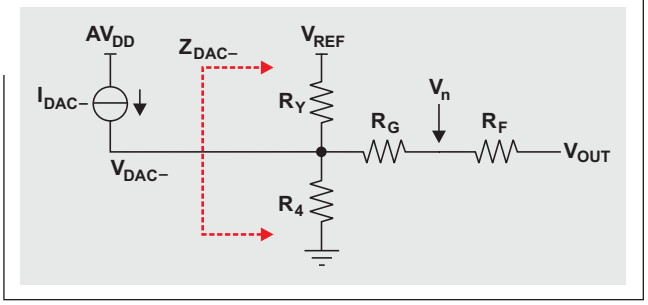
$$V_p = V_{DAC+} \times \frac{R_3}{R_2+R_3},$$

and $V_n = \alpha V_p$ can be used to rewrite Equation 25 as

$$\frac{1}{Z_{DAC-}} = \frac{1}{1-\frac{Z_{DAC+}\times\alpha\left(\frac{R_3}{R_2+R_3}\right)}{R_G}} \times \left(\frac{1}{R_Y}+\frac{1}{R_4}+\frac{1}{R_G}\right). \quad (26)$$

Using the same substitutions and general design constraints used on the positive side to drive values for Z_{DAC-}, V_{REF}, and R_G, simultaneous-equation techniques can be applied to Equations 24 and 26 to solve for $1/R_4$ (Equation 27 below). Note that the equations are solved for the condition where the DAC current on the negative side is zero: $I_{DAC-} = 0$ mA. This sets the DAC voltage on the negative side to its minimum value, $V_{DAC-} = V_{DAC-(min)}$, and sets the DAC voltage on the positive side to its maximum value, $V_{DAC+} = V_{DAC+(max)}$. The value of $1/R_4$ can then be used to find $1/R_Y$:

Figure 14. Negative side of analysis circuit



$$\frac{1}{R_Y} = \frac{1-\frac{Z_{DAC+}\times\alpha\left(\frac{R_3}{R_2+R_3}\right)}{R_G}}{Z_{DAC-}} - \left(\frac{1}{R_4}+\frac{1}{R_G}\right) \quad (28)$$

Note that α, the multiplication factor from V_p to V_n, in essence expresses the difference between the input pins. In a voltage-feedback amplifier, α is set by the loop gain of the amplifier. In a current-feedback amplifier, α is the gain of the input buffer between the inputs. All that aside, α is typically close enough to 1 that it can simply be removed from the calculation.

Calculating output voltage

Superposition can be used to write equations for the separate terms referred to V_{OUT}. These equations are the same as those in Part 1. The difference is that now the DAC only sources current, which is by convention positive current flow, making the direction of the op amp's output-voltage swing match that of the DAC. In other words, when the DAC is sourcing current on the positive side, the output of the op amp tends to swing positive, and when the DAC is sourcing current on the negative side, the output of the op amp tends to swing negative. This means that in the following equations, I_{DAC+} and I_{DAC-} are always positive or zero.

$$\frac{1}{R_4} = \frac{\frac{1-\frac{Z_{DAC+}\times\alpha\left(\frac{R_3}{R_2+R_3}\right)}{R_G}}{Z_{DAC-}} + \left[\frac{V_{DAC+(max)}\times\alpha\left(\frac{R_3}{R_2+R_3}\right)-V_{DAC-(min)}}{V_{REF}-V_{DAC-(min)}}-1\right]\left(\frac{1}{R_G}\right)}{\frac{V_{DAC-(min)}}{V_{REF}-V_{DAC-(min)}}+1} \quad (27)$$

The output-referred DC bias from the positive side is

$$V_{OUT\_V_{p(DC)}} = \left(1 + \frac{R_F}{R_G + R_Y \parallel R_4}\right) \times \left[V_{REF} \times \frac{R_1 R_3}{R_1(R_2 + R_3) + R_X(R_1 + R_2 + R_3)}\right].$$

The output-referred DAC signal from the positive side is

$$V_{OUT\_V_{p(DAC)}} = \left(1 + \frac{R_F}{R_G + R_Y \parallel R_4}\right) \times \left[I_{DAC+} \times \frac{R_X R_1 R_3}{R_X R_1 + (R_1 + R_X)(R_2 + R_3)}\right].$$

The output-referred DC bias from the negative side is

$$V_{OUT\_V_{n(DC)}} = -\left(V_{REF} \times \frac{R_4}{R_Y + R_4} \times \frac{R_F}{R_G + R_Y \parallel R_4}\right).$$

The output-referred DAC signal from the negative side is

$$V_{OUT\_V_{n(DAC)}} = -\left(I_{DAC-} \times \frac{R_Y R_4 R_F}{R_Y R_4 + R_G R_4 + R_Y R_G}\right).$$

Adding these four equations provides an expression for V_{OUT}:

$$V_{OUT} = V_{OUT\_V_{p(DC)}} + V_{OUT\_V_{p(DAC)}} + V_{OUT\_V_{n(DC)}} + V_{OUT\_V_{n(DAC)}} \quad \textbf{(29)}$$

If it is assumed that $I_{DAC} = I_{DAC+} - I_{DAC-}$, $Z = Z_{DAC+} = Z_{DAC-}$, and $R_F/R_G = R_3/R_2$, the DC component of the DAC outputs will cancel and the AC signal's gain equation from the DAC output current to the voltage output of the op amp can be simplified and written as

$$\frac{V_{OUT}}{I_{DAC}} = 2Z \times \frac{R_F}{R_G}. \quad \textbf{(30)}$$

Design example and simulation

For an example of how to proceed with the design, assume that the PMOS DAC noted earlier, with a compliance voltage ranging from –1.0 V to +1.25 V, is being used. Also assume that the full compliance voltage range will be used to maximize the DAC output voltage, which in turn will minimize the gain required from the op amp and will require V_{REF} to be a negative voltage. The DAC full-scale output is set to 20 mA. To get a 5-V_{PP}, DC-coupled single-ended output signal, the circuit shown in Figure 12 can be used. Since a ±5-V power supply is being used for the op amp, it is convenient to make V_{REF} = –5 V. Given that $I_{DAC\pm}$ = 20 mA and $V_{DAC\pm}$ = 2.25 V_{PP}, the target impedance, $Z_{DAC\pm}$, can be calculated to equal 112.5 Ω.

With the starting design constraints given earlier, the Texas Instruments THS3095 current-feedback op amp is selected as the amplifier, where $R_3 = R_F$ = 750 Ω. The gain from $V_{DAC\pm}$ to the output is given by the resistor ratios $R_F/R_G = R_3/R_2$, so R_G can be calculated as

$$R_G = R_2 = R_F \times \frac{V_{DAC\pm}}{V_{OUT}} = 750\ \Omega \times \frac{2(2.25\ V)}{5\ V} = 675\ \Omega.$$

The nearest standard 1% value, 681 Ω, should be used.

Equations 22, 23, 27, and 28 can be used to find, respectively, R_1, R_X, R_4, and R_Y:

$$R_1 = \frac{1}{\frac{1}{Z_{DAC+}\left(1+\frac{1}{\frac{V_{REF}}{V_{DAC+(min)}}-1}\right)}-\frac{1}{R_2+R_3}} = \frac{1}{\frac{1}{112.50\ \Omega\left(1+\frac{1}{\frac{-5\ V}{-1\ V}-1}\right)}-\frac{1}{681\ \Omega+750\ \Omega}} = 155.95\ \Omega$$

$$R_X = \frac{1}{\frac{1}{Z_{DAC+}}-\frac{1}{R_1}-\frac{1}{R_2+R_3}} = \frac{1}{\frac{1}{112.5\ \Omega}-\frac{1}{155.95\ \Omega}-\frac{1}{681\ \Omega+750\ \Omega}} = 562.5\ \Omega$$

$$R_4 = \frac{\frac{V_{DAC-(min)}}{V_{REF}-V_{DAC-(min)}}+1}{\frac{1-\frac{Z_{DAC+}\times\alpha\left(\frac{R_3}{R_2+R_3}\right)}{R_G}}{Z_{DAC-}}+\left[\frac{V_{DAC+(max)}\times\alpha\left(\frac{R_3}{R_2+R_3}\right)-V_{DAC-(min)}}{V_{REF}-V_{DAC-(min)}}-1\right]\left(\frac{1}{R_G}\right)}$$

$$= \frac{\frac{-1\ V}{-5\ V+1\ V}+1}{\frac{1-\frac{112.5\ \Omega\times1\times\frac{750\ \Omega}{681\ \Omega+750\ \Omega}}{681\ \Omega}}{112.5\ \Omega}+\left(\frac{1.25\ V\times1\times\frac{750\ \Omega}{681\ \Omega+750\ \Omega}+1\ V}{-5\ V+1\ V}-1\right)\left(\frac{1}{681\ \Omega}\right)} = 206.84\ \Omega$$

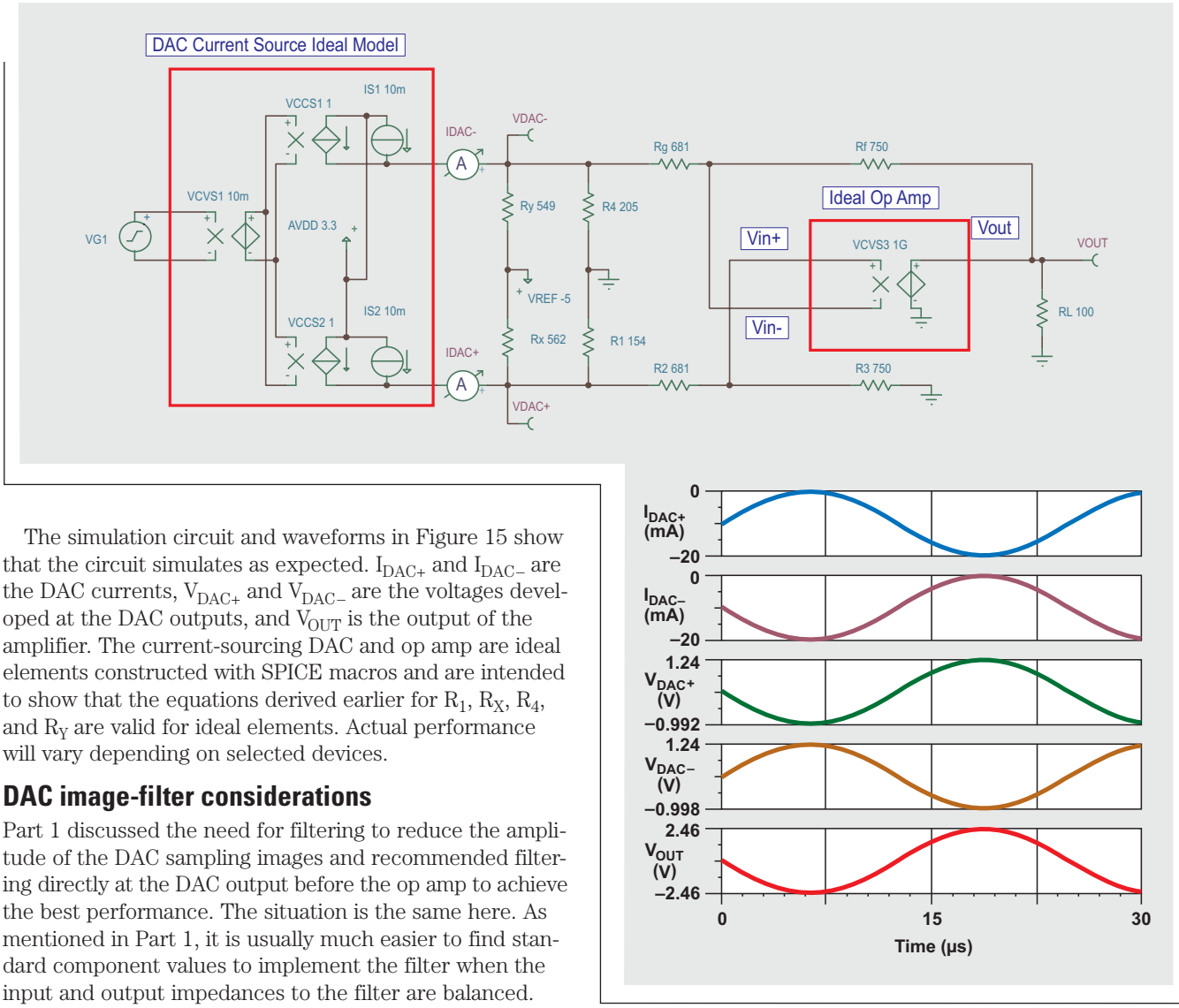
$$R_Y = \frac{1}{\frac{1-\frac{Z_{DAC+}\times\alpha\left(\frac{R_3}{R_2+R_3}\right)}{R_G}}{Z_{DAC-}}-\left(\frac{1}{R_4}+\frac{1}{R_G}\right)} = \frac{1}{\frac{1-\frac{112.5\ \Omega\times1\times\frac{750\ \Omega}{681\ \Omega+750\ \Omega}}{681\ \Omega}}{112.5\ \Omega}-\left(\frac{1}{206.84\ \Omega}+\frac{1}{681\ \Omega}\right)} = 550.58\ \Omega$$

The nearest standard 1% values should be used: R_1 = 154 Ω, R_X = 562 Ω, R_4 = 205 Ω, and R_Y = 549 Ω.

These equations are easily solved when set up in a spreadsheet. To see an example Excel® worksheet, go to http://www.ti.com/lit/zip/slyt360 and click Open to view the WinZip® directory online (or click Save to download the WinZip file for offline use). Then open the file DAC_Source_to_Op_Amp_Wksht.xls and select the "DAC Source to Op Amp, No Filter" worksheet tab.

SPICE simulation is a great way to validate the design. To see a TINA-TI™ simulation of the circuit in this example, go to http://www.ti.com/lit/zip/slyt360 and click Open to view the WinZip directory online (or click Save to download the WinZip file for offline use). If you have the TINA-TI software installed, you can open the file DAC_Source_to_Op_Amp_No_Filter.TSC to view the example. To download and install the free TINA-TI software, visit www.ti.com/tina-ti and click the Download button.

Figure 15. Simulation of current-sourcing DAC interfaced to op amp



The simulation circuit and waveforms in Figure 15 show that the circuit simulates as expected. I_{DAC+} and I_{DAC-} are the DAC currents, V_{DAC+} and V_{DAC-} are the voltages developed at the DAC outputs, and V_{OUT} is the output of the amplifier. The current-sourcing DAC and op amp are ideal elements constructed with SPICE macros and are intended to show that the equations derived earlier for R_1, R_X, R_4, and R_Y are valid for ideal elements. Actual performance will vary depending on selected devices.

DAC image-filter considerations

Part 1 discussed the need for filtering to reduce the amplitude of the DAC sampling images and recommended filtering directly at the DAC output before the op amp to achieve the best performance. The situation is the same here. As mentioned in Part 1, it is usually much easier to find standard component values to implement the filter when the input and output impedances to the filter are balanced.

Figure 16. Inserting DAC image filter

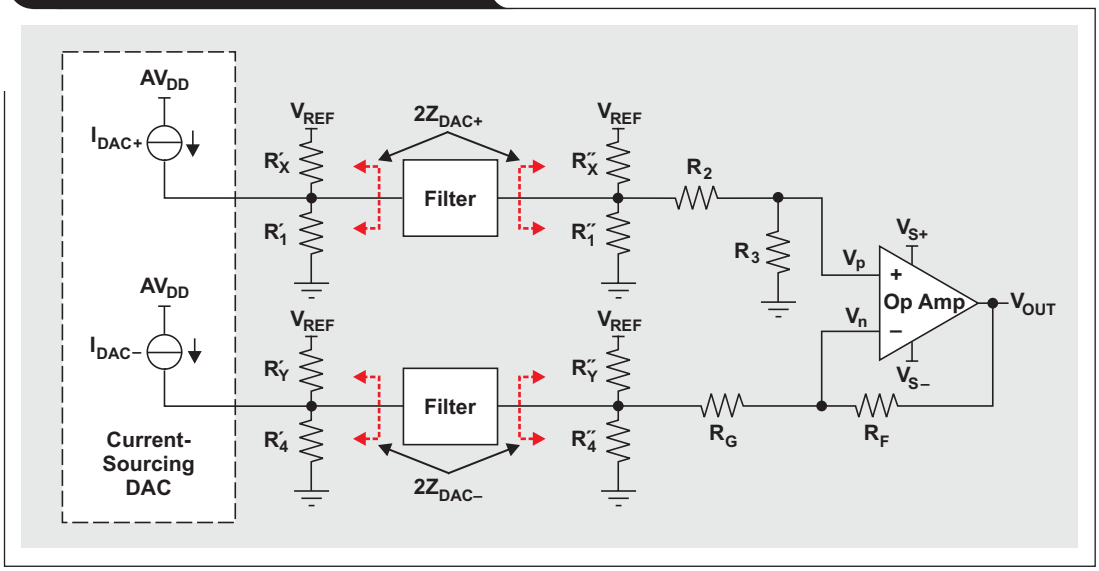


Figure 16 shows the proposed circuit implementation where R_1, R_X, R_4, and R_Y have been replaced with prime and double-prime components on either side of the filter, so that

$R_1 = R'_1 \parallel R''_1$,
$R_X = R'_X \parallel R''_X$,
$R_4 = R'_4 \parallel R''_4$, and
$R_Y = R'_Y \parallel R''_Y$.

At the same time, the impedance seen on each terminal of the filter is $2 \times Z_{DAC\pm}$. By use of algebra, the following equations can be derived:

$$\frac{1}{R'_1} = \frac{1}{2Z_{DAC+}\left(1+\frac{1}{\frac{V_{REF}}{V_{DAC+(min)}}-1}\right)} \quad (31)$$

$$\frac{1}{R''_1} = \frac{1}{2Z_{DAC+}\left(1+\frac{1}{\frac{V_{REF}}{V_{DAC+(min)}}-1}\right)} - \frac{1}{R_2+R_3} \quad (32)$$

$$\frac{1}{R'_X} = \frac{1}{2Z_{DAC+}} - \frac{1}{R'_1} \quad (33)$$

$$\frac{1}{R''_X} = \frac{1}{2Z_{DAC+}} - \frac{1}{R''_1} - \frac{1}{R_2+R_3} \quad (34)$$

$$\frac{1}{R'_4} = \frac{\left[1-\frac{Z_{DAC+}\times\alpha\left(\frac{R_3}{R_2+R_3}\right)}{\frac{R_G}{2Z_{DAC-}}}\right]}{\frac{V_{DAC-(min)}}{V_{REF}-V_{DAC-(min)}}+1} \quad (35)$$

$$\frac{1}{R''_4} = \frac{1-\frac{Z_{DAC+}\times\alpha\left(\frac{R_3}{R_2+R_3}\right)}{\frac{R_G}{2Z_{DAC-}}} + \left[\frac{V_{DAC+(max)}\times\alpha\left(\frac{R_3}{R_2+R_3}\right)-V_{DAC-(min)}}{V_{REF}-V_{DAC-(min)}}-1\right]\left(\frac{1}{R_G}\right)}{\frac{V_{DAC-(min)}}{V_{REF}-V_{DAC-(min)}}+1} \quad (36)$$

$$\frac{1}{R'_Y} = \frac{1 - \frac{Z_{DAC+} \times \alpha\left(\frac{R_3}{R_2 + R_3}\right)}{R_G}}{2Z_{DAC-}} - \frac{1}{R'_4} \quad \textbf{(37)}$$

$$\frac{1}{R''_Y} = \frac{1 - \frac{Z_{DAC+} \times \alpha\left(\frac{R_3}{R_2 + R_3}\right)}{R_G}}{2Z_{DAC-}} - \left(\frac{1}{R''_4} + \frac{1}{R_G}\right) \quad \textbf{(38)}$$

These equations are easily solved when set up in a spreadsheet. To see an example Excel worksheet, go to http://www.ti.com/lit/zip/slyt360 and click Open to view the WinZip directory online (or click Save to download the WinZip file for offline use). Then open the file DAC_Source_to_Op_Amp_Wksht.xls and select the "DAC Source to Op Amp, Filtered" worksheet tab.

The performance is similar to that shown in the SPICE simulation for Part 1 (Reference 1). Please refer to that simulation to see the effects of balancing and matching the filter impedance versus using a filter with unmatched impedance.

Conclusion

This article has shown a circuit implementation using a single-stage op amp to convert complementary-current outputs from a current-sourcing DAC to a single-ended voltage. Equations were derived and a methodology presented for proper selection of component values to set the DAC's output-voltage compliance while maintaining balanced input signals to the op amp for best overall performance. Filter-design considerations were also included to explain proper insertion when filtering before the amplifier is desired.

Reference

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Document Title	**TI Lit. #**
1. Jim Karki, "Interfacing Op Amps to High-Speed DACs, Part 1: Current-Sinking DACs," *Analog Applications Journal* (3Q 2009)	slyt342

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