

# DAC38RF89 Test

TI Information– Selective Disclosure

# DAC38RF89 bypass DUC Test

## Test Setup:

Fdac = 5000Msps internal PLL

NCO not used

Int 2X

IF = 50 tones from 100MHz to 1.2GHz

LMF = 821

## DAC38RFxx EVM GUI

Click on “Not in RESET” then click on “DAC in RESET”. Click on “LOAD DEFAULT”  
Enter parameters, then click on “CONFIGURE DAC”.  
If using the DAC PLL, click on “PLL AUTO TUNE”.

**DAC38RFxx EVM GUI v2p0**

File Debug Settings Help

Quick Start **DAC38RF8x** LMK04828 **Low Level V** Reconnect?

Die Temp (Celsius)  
0  
Update

**DAC38RF89** SELECT DEVICE

DAC RESETB Pin  
Not in RESET LOAD DEFAULT

Quick Start Procedure  
-Reset the DAC. Toggle the RESET pin.  
-Load Default Register Settings.

**DAC MODE**

DAC Clock Frequency (MHz)  
5000

# of DACs  
Dual DAC

# of IQ pairs per DAC  
real input

# of serdes lanes per DAC  
4 Lanes

Desired Interpolation  
2x

CONFIGURE DAC

**On-chip PLL**

PLL Enable ☒

M 10 x4 Ref Freq (MHz)  
N 1 x 125

SMA J4 CLK (MHz)  
625

Valid PLL Frequency  
Current Serdes Lane Rate = 12500.00MHz  
Maximum sample rate for Dual DAC, real input, 4 Lanes, 2x interpolation is 5000  
Serdes Configured to Full Rate  
Serdes clock predivider = 4  
Serdes PLL Vrange = 0  
Serdes PLL Multiplier = 10  
HSDCPRO ini file: DAC38RF8x\_LMF\_821

PLL AUTO TUNE

-For External clock mode, enter the external clock frequency and select the desired no. of DACs, no. of IQ pairs, no. of serdes lanes and the interpolation.  
-Click on CONFIGURE DAC button to configure the DAC for the mode selected

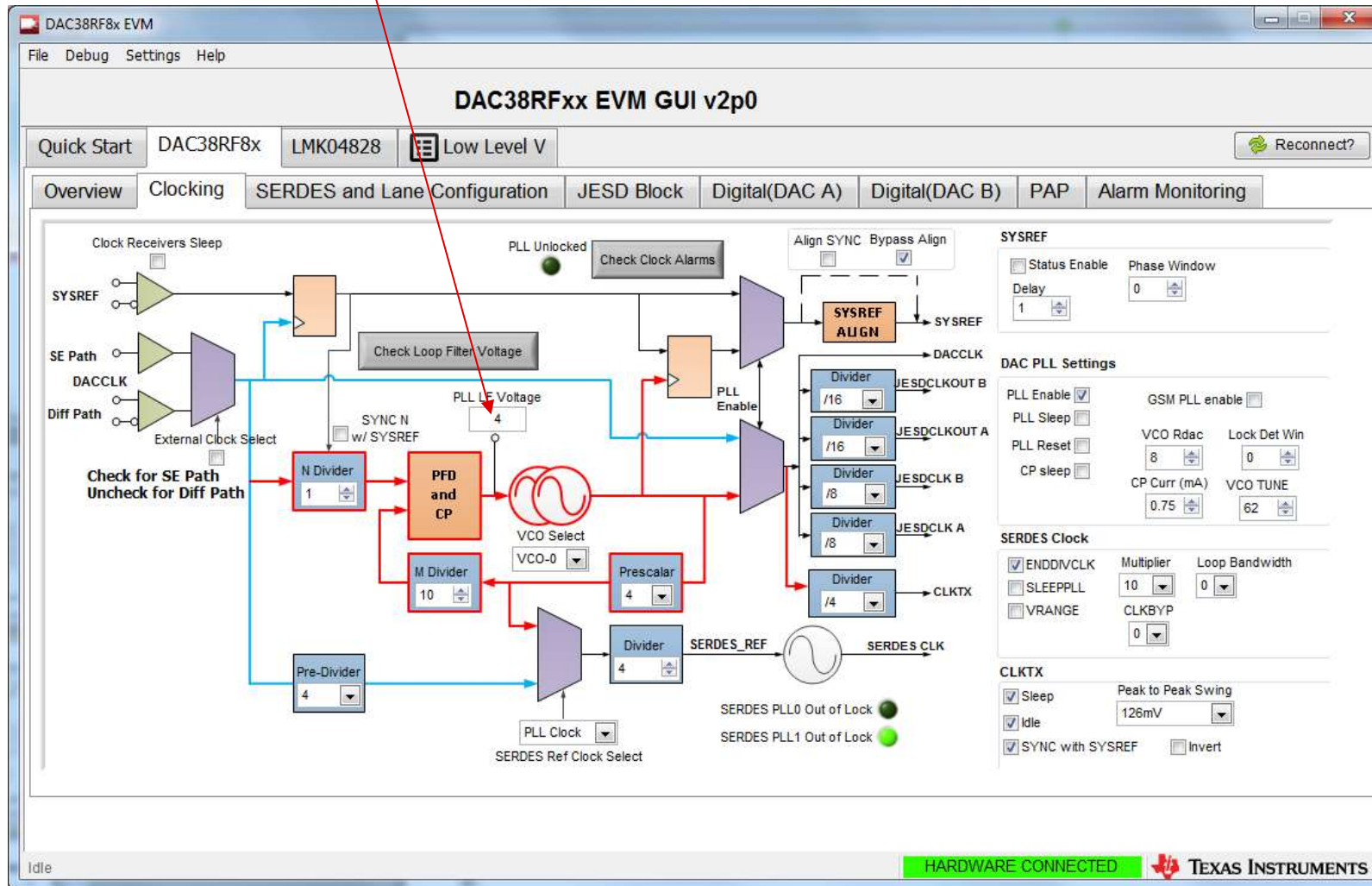
-For onchip PLL mode, check the PLL Enable box and specify the Reference frequency, M and N divider values.  
-Select the desired mode of the DAC and click on the Configure DAC button.  
-Click on the PLL AUTO TUNE button to automatically set the PLL loop filter voltage

Reset DAC  
JESD Core & SYSREF TRIGGER

-Reset the DAC JESD Core and trigger sysref

Idle HARDWARE CONNECTED TEXAS INSTRUMENTS

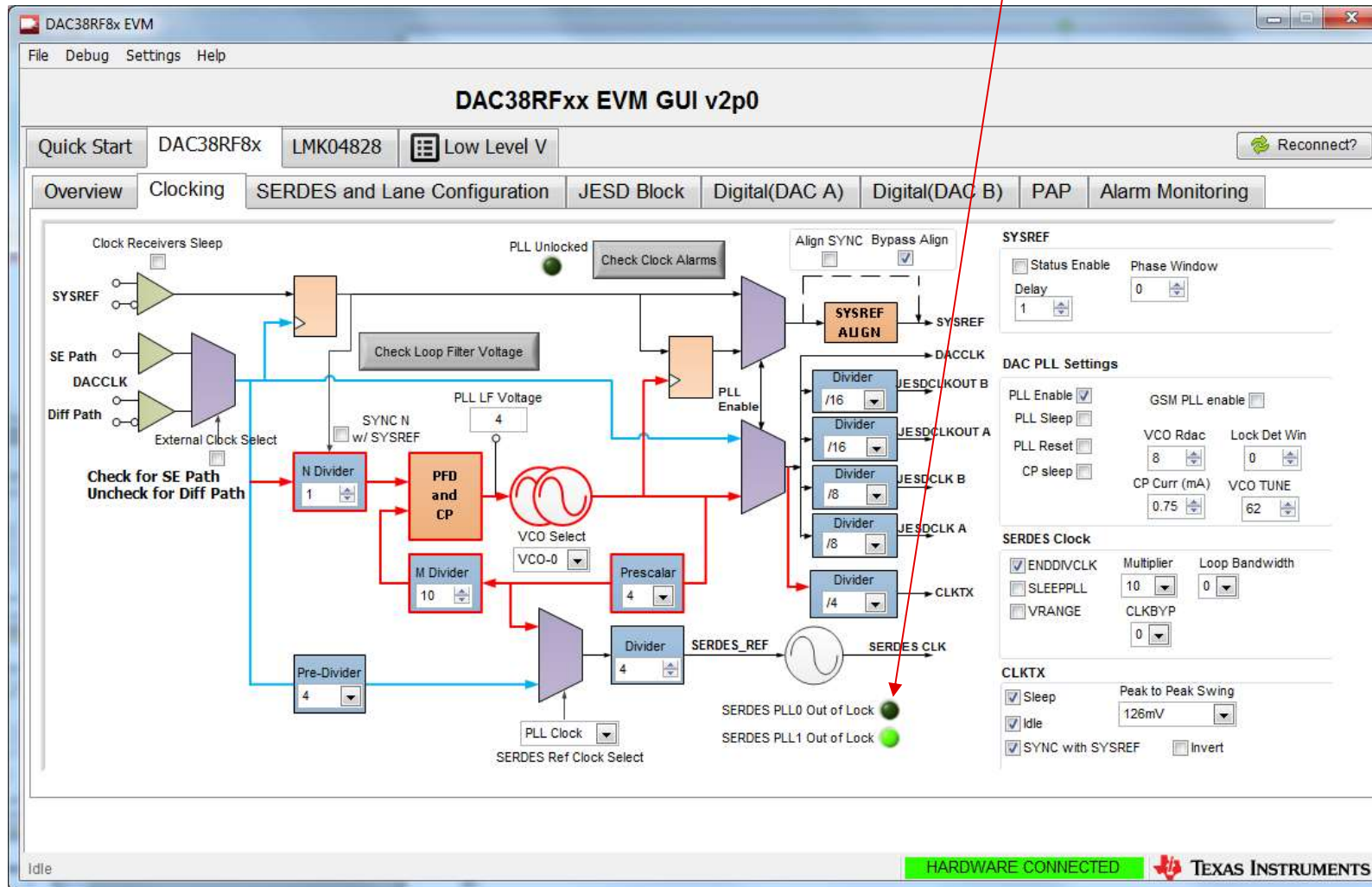
**Clocking Settings. Click on “Check Loop Filter Voltage” and verify the PLL LF Voltage is between 3-5.**



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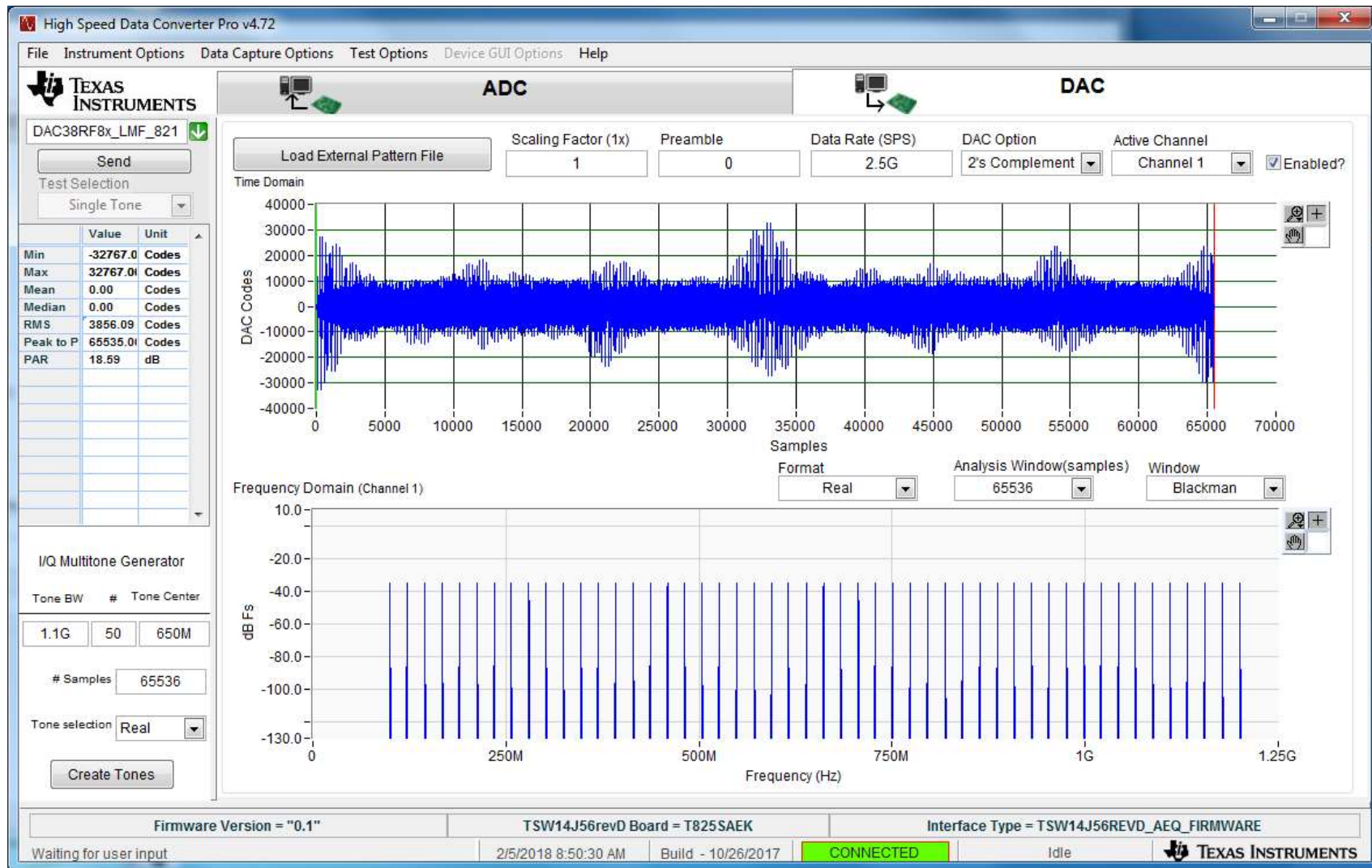
4

Verify the SERDES PLL0 is not Out of Lock by clicking here. This indicator shall turn off (not green) if SERDES PLL is locked.





**TSW14J56 Settings. Load HSDC Pro as shown below. Click on “Create Tones”, then “Send”**



Go back to the DAC38RFxx EVM GUI and click on “Reset DAC JESD Core & SYSREF TRIGGER”

DAC38RFxx EVM GUI v2p0

Quick Start | DAC38RF8x | LMK04828 | Low Level V | Reconnect?

Die Temp (Celsius): 0 | Update

DAC38RF89 | SELECT DEVICE

DAC RESETB Pin: Not in RESET | LOAD DEFAULT

Quick Start Procedure:  
-Reset the DAC. Toggle the RESET pin.  
-Load Default Register Settings.

DAC MODE:  
DAC Clock Frequency (MHz): 5000  
# of DACs: Dual DAC  
# of IQ pairs per DAC: real input  
# of serdes lanes per DAC: 4 Lanes  
Desired Interpolation: 2x  
CONFIGURE DAC

On-chip PLL:  
PLL Enable: ☒  
M: 10 x4  
N: 1  
Ref Freq (MHz): 125  
SMA J4 CLK (MHz): 625  
PLL AUTO TUNE

Valid PLL Frequency  
Current Serdes Lane Rate = 12500.00MHz  
Maximum sample rate for Dual DAC, real input, 4 Lanes, 2x interpolation is 5000  
Serdes Configured to Full Rate  
Serdes clock predivider = 4  
Serdes PLL Vrange = 0  
Serdes PLL Multiplier = 10  
HSDCPRO ini file: DAC38RF8x\_LMF\_821

Reset DAC JESD Core & SYSREF TRIGGER

-Reset the DAC JESD Core and trigger sysref

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# DAC output at SMA J6

