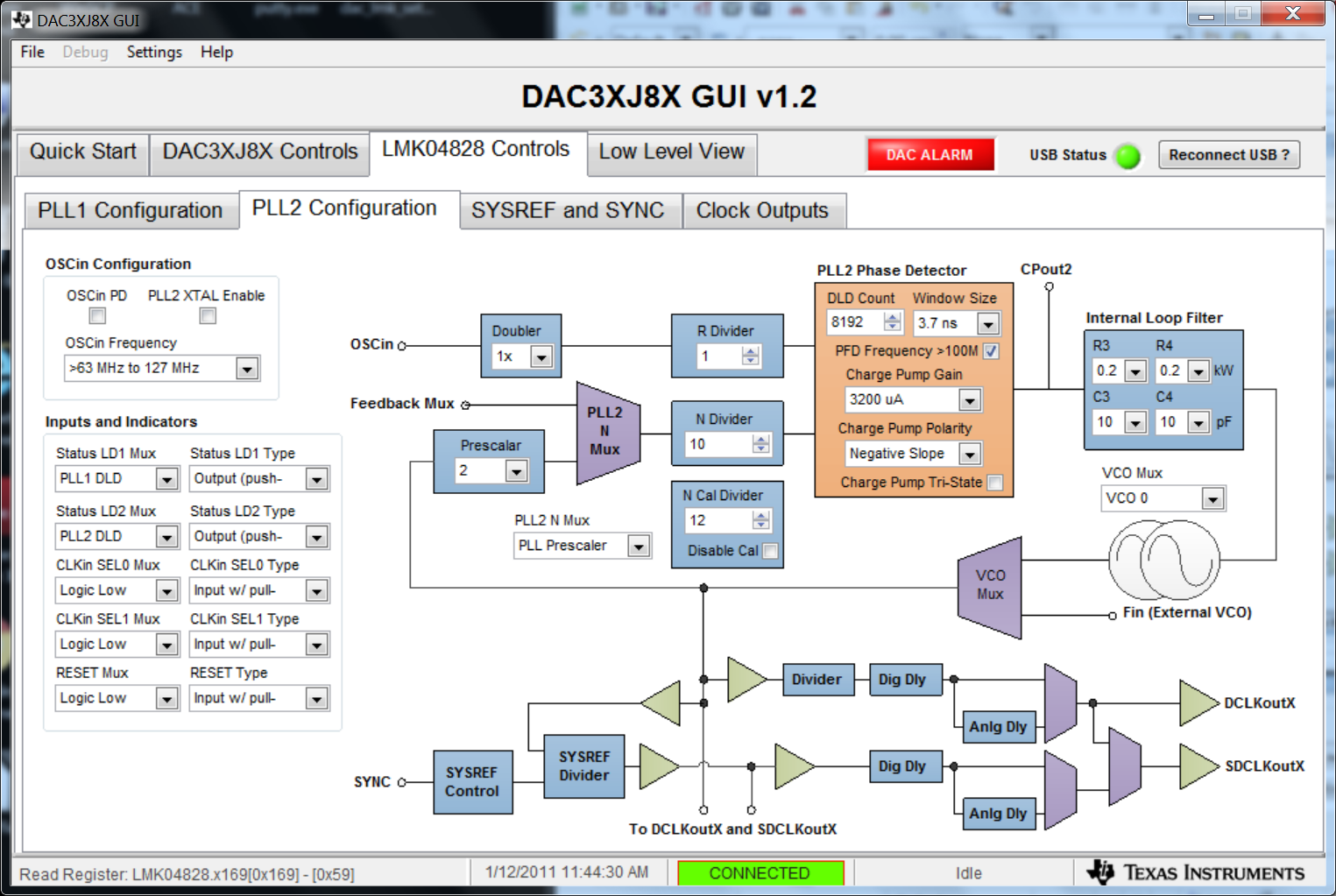
Dear sirs,

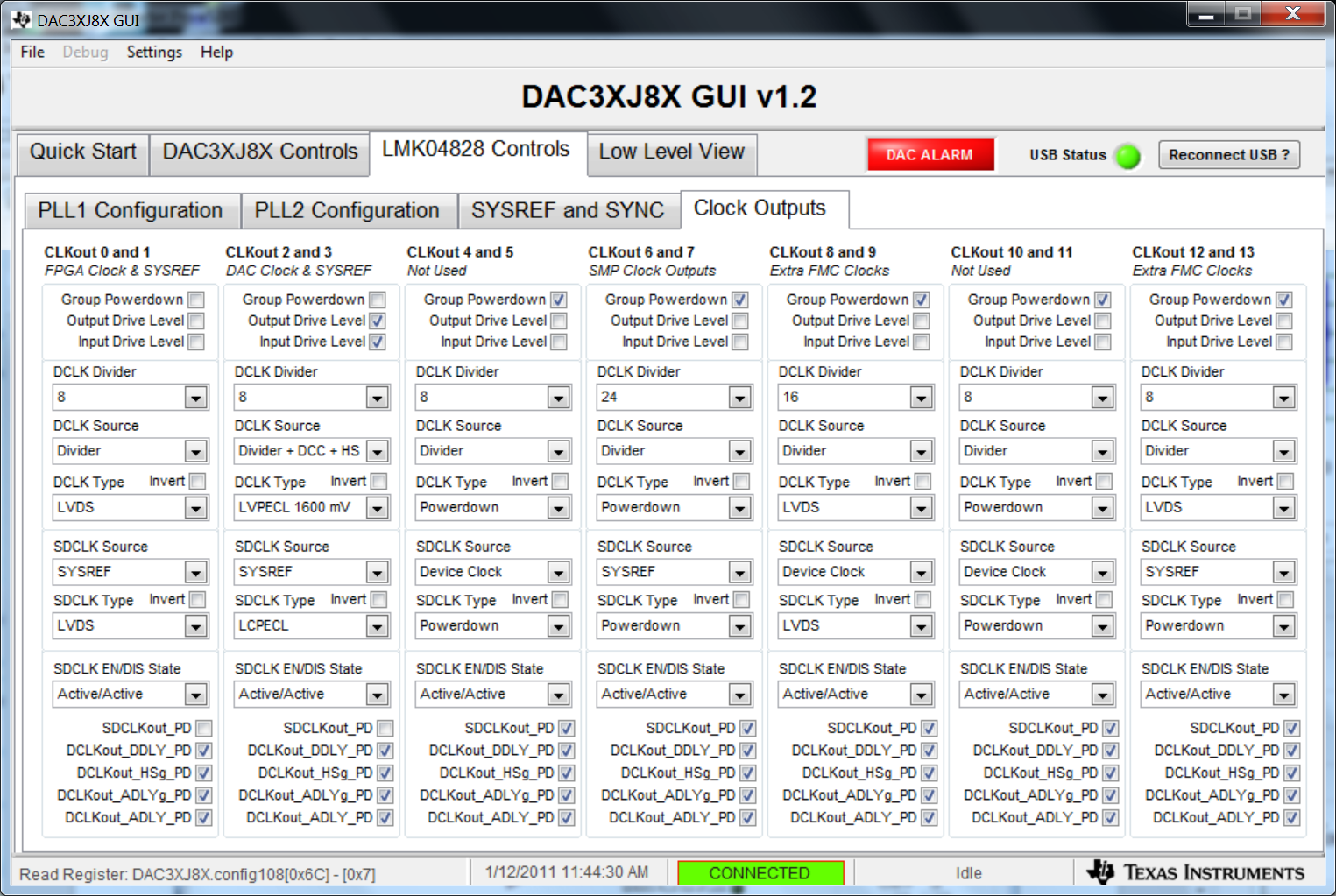
I wonder, is it possible to set the DAC3XJ8XEVM as follows?

LMK04828, PLL1 bypassed and PLL2 receives the OSCin with the following set as in the picture. The signal delivered to the PLL is 122.88 MHz coming from J17 after implement the configuration option of *Clock Generator using External Reference* (R177, C206, and C121 should be uninstalled and R185, R186, and C92 should be installed).

The VCO frequency designed to 122.88 \* 20 = 2457.6 MHz that is using VCO0 (2370 to 2630 MHz) unfortunately the VCO frequency is not stable and locked.



CLKout0 and 2 are tuned to VCO0 /8 = 307.2 MHz and CLKout1 and 3 provides in accordance the SYSREF.



The DAC operated using it's internal PLL.

VCO Freq = 307.2 \* 2 \* 7 = 4300.8 MHz that is, using L-band VCO (3.7 – 4.66 GHz). As a result the DACCLK (DAC Output Rate) = 4300.8 /2 = 2150.4 MHz

