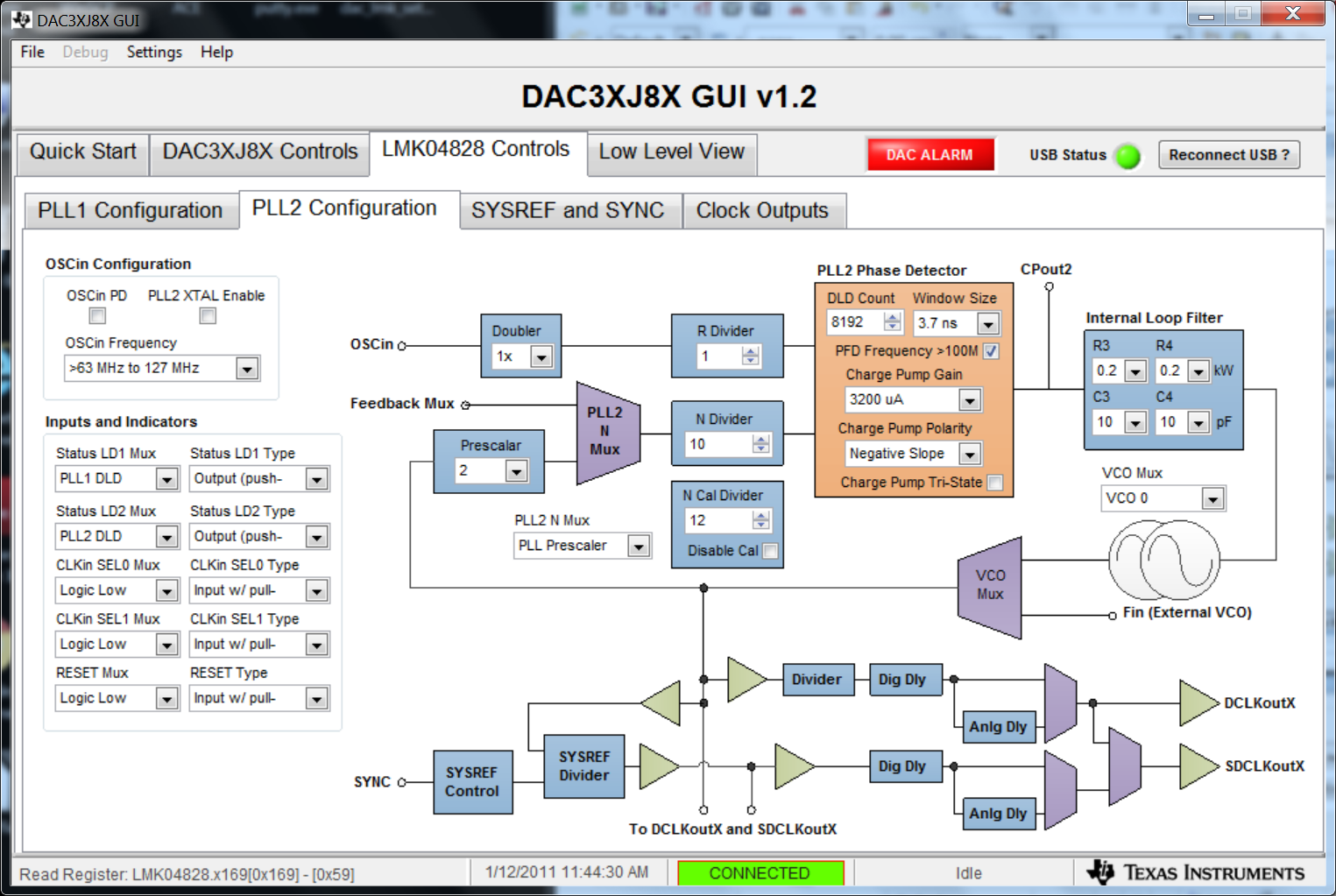
Dear Jim

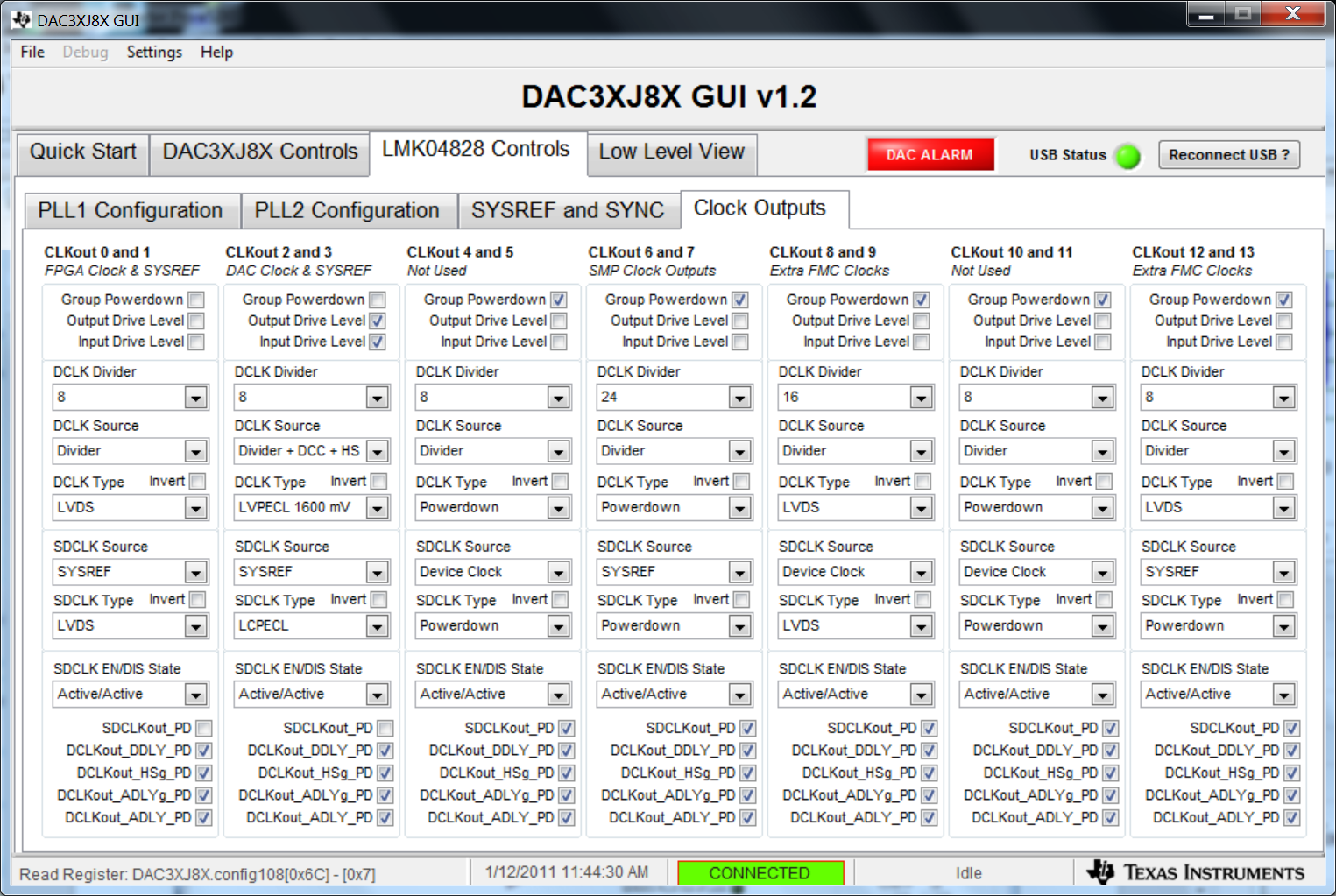
With your recommendation, I tried to set the GUI for the DAC as follows:

LMK04828, PLL1 bypassed and PLL2 receives the **OSCin** with the following set as in the picture. The signal delivered to the PLL is 134.4 MHz coming from J17 (after implement the configuration option of *Clock Generator using External Reference* that is R177, C206, and C121 should be uninstalled and R185, R186, and C92 should be installed).

The VCO frequency designed to 134.4 \* 24 = 3225.6 MHz that is using VCO1 (2945 to 3255 MHz) using PLL2 Prescaler =2 and PLL2 N Divider =12. I believe that the Charge pump Tri-State should be left unmarked and I tried to lower the Charge Pump Gain to 100uA but unfortunately the VCO frequency was not stable and with a lot of noise.

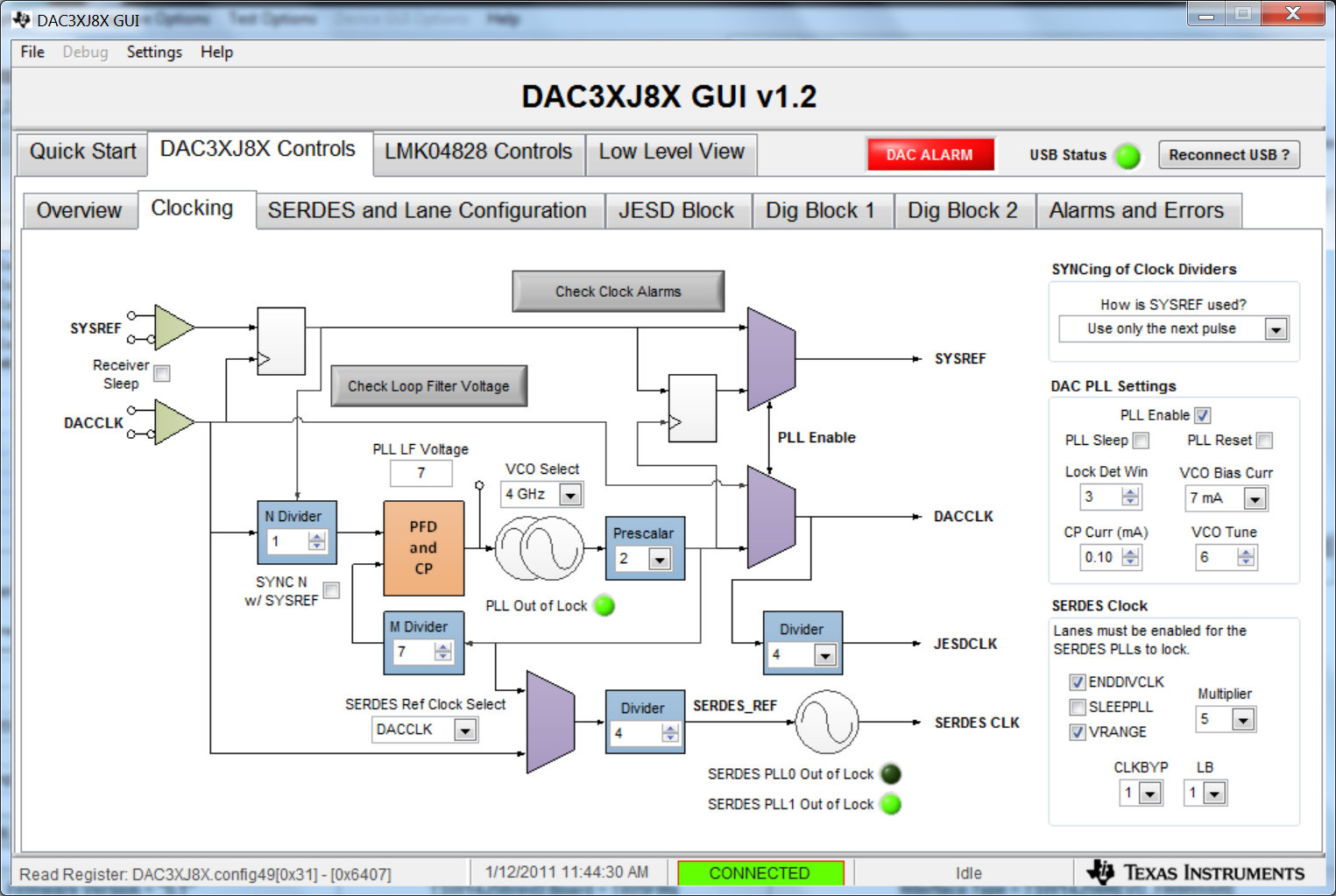


CLKout0 tuned to VCO1 /12 = 268.8 MHz , CLKout2 tuned to VCO1 /6 = 537.6 MHz and CLKout1 and 3 provides in accordance the SYSREF. (DCLKout0 Divider =12 and DCLKout2 Divider =6)



**The DAC operated using it's internal PLL:**

VCO Freq = 537.6 \* M\_Divider \* DAC\_VCO\_Prescaler / N\_Divider = 537.6 \* 8 \*2 / 2 = 4300.8 MHz , using L-band VCO (3.7 – 4.66 GHz). As a result the DACCLK (DAC Output Rate) = 4300.8 /2 = 2150.4 MHz . **The PLL OUT OF Lock is lit !!!!** (The PLL Enable check box is checked)



The LMF = 222 , the serdes rate is 10.752Gbps.