T-51-09-16

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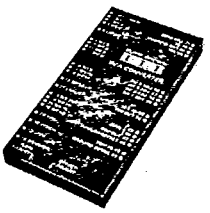
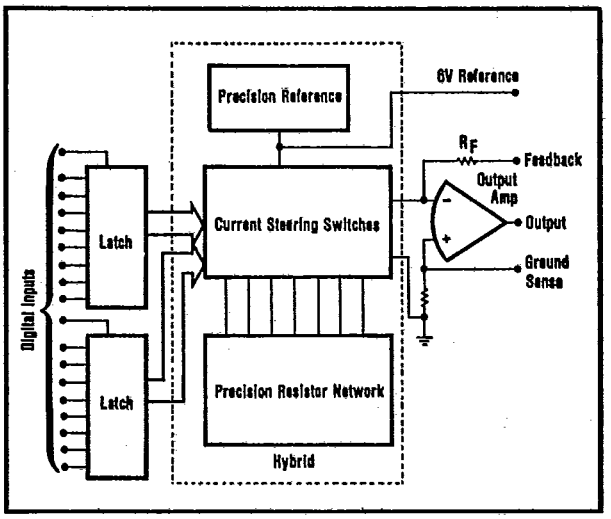


DAC73
DAC736

High Resolution
16-BIT DIGITAL-TO-ANALOG CONVERTER

FEATURES

- 16-BIT RESOLUTION
- ±1/2LSB MAXIMUM NONLINEARITY
- LOW DRIFT
- CURRENT OR VOLTAGE OUTPUT
- INTERNAL GAIN, OFFSET, AND LINEARITY ADJUSTMENT
- LATCHED INPUTS (DAC73)
- LOW COST



DESCRIPTION

The DAC73 is a 16-bit modular high performance digital-to-analog converter in a 2" x 4" x 0.4" (50.8mm x 101.6mm x 10.2mm) package. The low drift and ultra-high linearity of the DAC73 provide voltage or current output signals that are accurate to ±0.00075% of full scale input range at 25°C ambient.

The critical components including the current steering switches, the temperature-compensated zener reference, and the precision laser-trimmed bit resistor network are contained in a single ceramic hybrid package.

The feedback and reference resistors are laid out for maximum stability with low current density and ±10ppm/°C maximum temperature coefficient with ±1ppm/°C tracking. This insures very-low superposition errors and low temperature coefficient of gain.

The inputs are TTL-compatible CMOS and contain level triggered latches in an 8-bit format for microprocessor data bus compatibility. No external components are required to achieve full 16-bit accuracy. Gain and offset potentiometers are also included in the DAC73.

The DAC736 has electrical specifications identical to the DAC73, but it is pin-compatible with the AD1136. The input latches, bit adjust pins, ground sense pin, and internal offset adjust pot are not included.

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PDS-419A

Printed in U.S.A. August, 1982

SPECIFICATIONS

T-51-09-16

ELECTRICAL

T_A = +25°C and rated power supplies unless otherwise noted.

MODEL	DAC73J/DAC736J MIN	DAC73J/DAC736J TYP	DAC73J/DAC736J MAX	DAC73K/DAC736K MIN	DAC73K/DAC736K TYP	DAC73K/DAC736K MAX	UNITS
INPUT							
DIGITAL INPUT							
Resolution - CSB, COB			16			16	Bits
Logic Levels (TTL-Compatible CMOS)							
Logical "1" (at +1.0µA)	+3.5		+5.5	+3.5		+5.5	VDC
Logical "0" (at -0.5mA)	-0.5		+1.5	-0.5		+1.5	VDC
TRANSFER CHARACTERISTICS							
ACCURACY							
Linearity Error at 25°C			±0.0015			±0.00075	% of FSR(1)
Gain Error,(2) Voltage CSB		±0.005	±0.02		±0.005	±0.02	%
COB		±0.01	±0.05		±0.01	±0.05	%
Current		±0.05	±0.25		±0.05	±0.25	%
Offset Error,(2) Voltage, Unipolar			±0.8			±0.8	mV
Bipolar			±10			±10	mV
Current, Unipolar			±1			±1	µA
Bipolar			±5			±5	µA
Monotonicity Temp. Range 16 Bits for K, 15 Bits for J		±15		~+5		+35	°C
DRIFT (Over specified temp. range)							
Total Drift (Includes gain, offset, and linearity drift)							
CSB		±9.5	±24		±9.5	±24	ppm of FSR/°C
COB		±9	±22		±9	±22	ppm of FSR/°C
Total Error over Temp. Range(3)							
Voltage, Unipolar 0°C to 70°C		±0.043	±0.108		±0.043	±0.108	% of FSR
Bipolar		±0.040	±0.099		±0.040	±0.099	% of FSR
Voltage, Unipolar 15°C to 35°C		±0.010	±0.024		±0.010	±0.024	% of FSR
Bipolar		±0.009	±0.022		±0.009	±0.022	% of FSR
Gain (Exclusive of reference drift)		±4	±10		±4	±10	ppm/°C
Offset (Exclusive of reference drift)							
Unipolar		±0.5	±2		±0.5	±2	ppm of FSR/°C
Bipolar		±2	±5		±2	±5	ppm of FSR/°C
Differential Linearity over Temperature		±1	±2		±1	±2	ppm of FSR/°C
Linearity Error over Temperature		±1	±2		±1	±2	ppm of FSR/°C
SETTLING TIME							
Voltage (to ±0.00075% of FSR)							
Output: 20V Step			50			50	µsec
1LSB Step(4)		6	10		6	10	µsec
Slew Rate		18			18		V/µsec
Current (to ±0.00075% of FSR)							
Output: 2mA Step		6			6		µsec
COB Switching Transient Magnitude		600			600		mV
COB Switching Transient Energy		0.45			0.45		V-µsec
OUTPUT							
ANALOG OUTPUT							
Voltage Output							
Ranges - CSB		0 to +5			0 to +5		V
		0 to +10			0 to +10		V
COB		±2.5, ±5, ±10			±2.5, ±5, ±10		V
Output Current - Unipolar			+4			+4	mA
Bipolar			±2			±2	mA
Output Impedance (DC)		0.03	0.05		0.03	0.05	Ω
Short Circuit Duration		Indefinite to Common			Indefinite to Common		
Current Output							
Ranges - CSB		0 to -2			0 to -2		mA
COB		±1			±1		mA
Output Impedance - Unipolar		15			15		kΩ
Bipolar		4.4			4.4		kΩ
Compliance		-1.5 to +10			-1.5 to +10		V
INTERNAL REFERENCE VOLTAGE	5.990	6.000	6.010	5.990	6.000	6.010	V
Maximum External Current(5)			+4			+4	mA
Temp. Coeff.		±4	±10		±4	±10	ppm/°C
OUTPUT NOISE							
Current, COB							
0.1Hz to 10Hz		1			1		nA, p-p
10Hz to 100kHz		4			4		nA, rms
Voltage, COB, ±10V Range							
0.1Hz to 10Hz		10			10		µV, p-p
10Hz to 100kHz		70			70		µV, rms

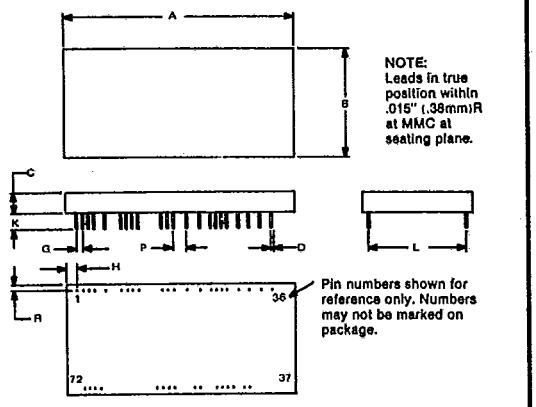
ELECTRICAL (CONT)

MODEL	DAC73J/DAC736J MIN	DAC73J/DAC736J TYP	DAC73J/DAC736J MAX	DAC73K/DAC736K MIN	DAC73K/DAC736K TYP	DAC73K/DAC736K MAX	UNITS
STABILITY, LONG TERM							
Gain (Exclusive of reference)		±30			±30		ppm/10³hr
Offset COB (Exclusive of reference)		±30			±30		ppm of FSR/ 10³hr
CSB		±5			±5		ppm of FSR/ 10³hr
Linearity		±0.25			±0.25		LSB/10³hr
Reference		±10			±10	±20	ppm/10³hr
POWER SUPPLY SENSITIVITY							
Unipolar Offset							
±15VDC		±0.0001			±0.0001		% of FSR/% Vs
+5VDC		±0.0001			±0.0001		% of FSR/% Vs
Bipolar Offset							
±15VDC		±0.0004			±0.0004		% of FSR/% Vs
+5VDC		±0.0001			±0.0001		% of FSR/% Vs
Gain							
±15VDC		±0.001			±0.001		% of FSR/% Vs
+5VDC		±0.0005			±0.0005		% of FSR/% Vs
POWER SUPPLY REQUIREMENTS							
Rated Voltage		±15, +5			±15, +5		VDC
Range	±14.5, +4.75	±15, +5	±15.5, +5.25	±14.5, +4.75	±15, +5	±15.5, +5.25	VDC
Supply Drain, ±15VDC (no load)		+35, -45	+50, -60		+35, -45	+50, -60	mA
+5VDC (logic supply)		9			9		mA
TEMPERATURE RANGE							
Specification	0		+70	0		+70	°C
Storage	-55		+100	-55		+100	°C
PRICES							
1-24		242/220			286/260		$
25-99		218/198			257/234		
100-249		193/175			228/206		

NOTES:
1. FSR means Full Scale Range and is 20V for ±10V range, 10V for ±5V range, etc.
2. Adjustable to zero with internal trim potentiometer (offset adjustment external on DAC736).
3. With gain and offset errors adjusted to zero at +25°C.
4. LSB is for 16-bit resolution.
5. Maximum with no degradation of specifications.

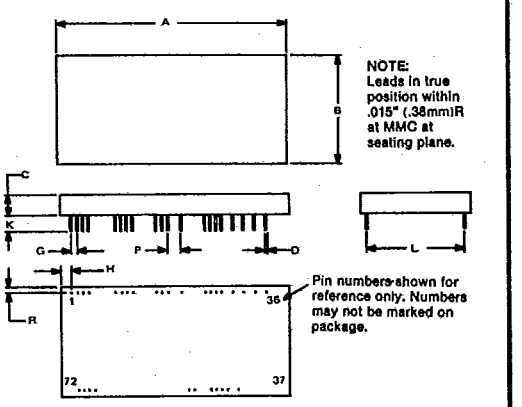
MECHANICAL

DAC73



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	3.950	4.010	100.33	101.85
B	1.950	2.010	49.53	51.05
C	.350	.410	8.89	10.41
D	.019	.021	0.48	0.53
G	.100 BASIC		2.54 BASIC	
H	.150	.250	3.81	6.35
K	.250	.350	6.35	8.89
L	1.800 BASIC		45.72 BASIC	
P	.200 BASIC		5.08 BASIC	
R	0.50	.150	1.27	3.81

DAC736



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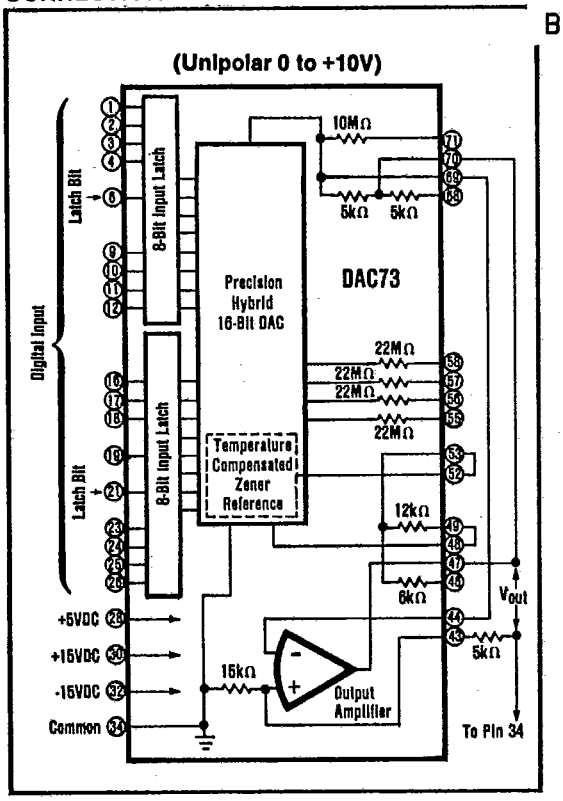
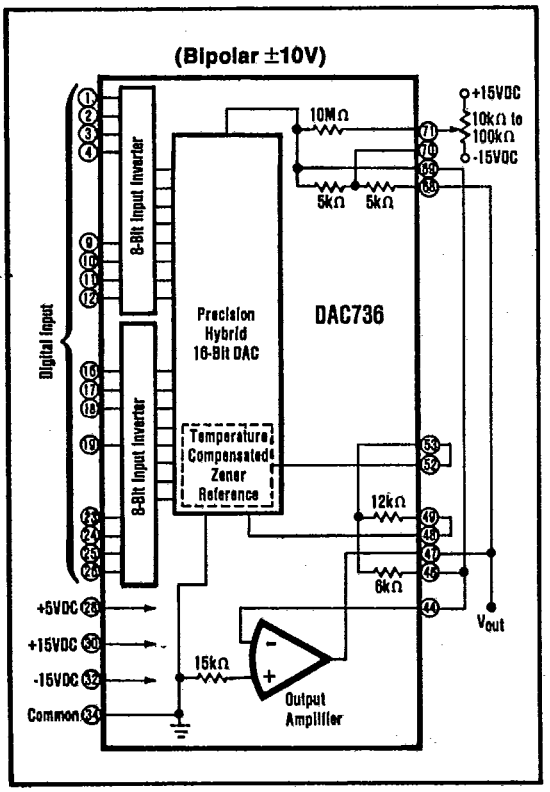
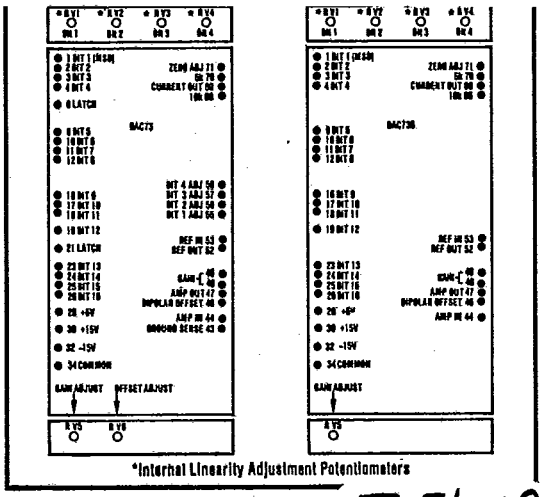
D	.019	.021	0.48	0.53
G	.100 BASIC		2.54 BASIC	
H	.150	.250	3.81	6.35
K	.250	.350	6.35	8.89
L	1.800 BASIC		45.72 BASIC	
P	.200 BASIC		5.08 BASIC	
R	0.50	.150	1.27	3.81

CONNECTION DIAGRAMS





PIN ASSIGNMENTS



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DISCUSSION OF SPECIFICATIONS

DIGITAL INPUT CODES

The DAC73/736 accepts complementary digital input codes in CSB or COB format. The COB model may be connected by the user for either complementary offset binary (COB) or complementary two's complement (CTC) codes (see Table I).

TABLE I. Digital Input Codes.

CSB, COB MODELS	DIGITAL INPUT CODES MSB LSB	CSB Compl. Straight Binary	COB Compl. Offset Binary	CTC* Compl. Two's Complement
All bits ON	0000...000	+Full Scale	+Full Scale	-1LSB
Mid Scale	0111...111	+1/2 Full Scale	Zero	-Full Scale
All Bits OFF	1111...111	Zero	-Full Scale	Zero
	1000...000	Mid Scale-1LSB	-1LSB	+Full Scale

*Invert the MSB of the COB code with an external inverter to obtain CTC code.

INPUTS

Each bit input of the DAC73 consists of a buffered CMOS D type latch (see Figure 1). Bits 1 (MSB) through 8 are latched by a low level on pin 6. Bits 9 through 16 (LSB) are latched by a low level on pin 21. The latch inputs may be left open for transparent transfer of data.

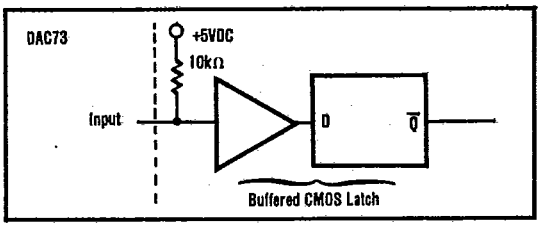

FIGURE 1. DAC73 Input.

The DAC736 inputs are CMOS inverters with 10kΩ pull-up resistors (see Figure 2).

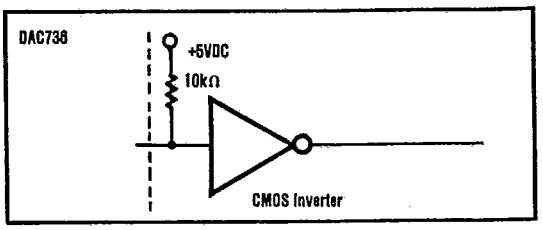

FIGURE 2. DAC736 Input.

The DAC73 and DAC736 can be driven directly by open collector or totem pole TTL logic.

ACCURACY

Linearity

This specification describes one of the truest measures of D/A converter accuracy. As defined it means that the analog output will not vary by more than ±0.00075% max (CSB, COB) from a straight line drawn through the end points (all bits ON and all bits OFF) at +25°C (see Figure 3).

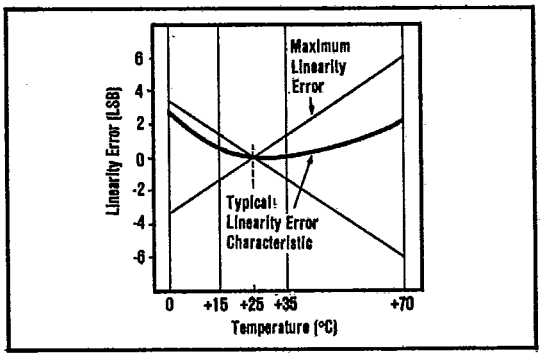

FIGURE 3. Nonlinearity vs Temperature.

Differential Linearity

Differential linearity error of a D/A converter is the deviation from an ideal 1LSB voltage change from one adjacent output state to the next. A differential linearity error specification of ±1/2LSB means than the output voltage step sizes can be anywhere from 1/2LSB to 3/2LSB when the input changes from one adjacent input stage to the next.

Monotonicity

Monotonicity over a ±5°C range for the DAC73 and DAC736 is guaranteed when ambient linearity is calibrated. This insures that the analog output will increase or remain the same for increasing 16-bit input digital codes.

DRIFT

Gain Drift is a measure of the change in the full scale range output over temperature expressed in LSB's per °C (see Figure 4). Gain Drift is established by: 1) testing the end point differences for each DAC73 model at +25°C and the appropriate specification temperature extremes; 2) calculating the gain error with respect to the +25°C value; and 3) dividing by the temperature change. This is expressed in ppm/°C.

Offset Drift is a measure of the actual change in output with all "1"s on the input over the specified temperature range.

The maximum change in offset is referenced to the offset at +25°C and is divided by the temperature range. This drift is expressed in parts per million of full scale range per °C (ppm of FSR/°C).

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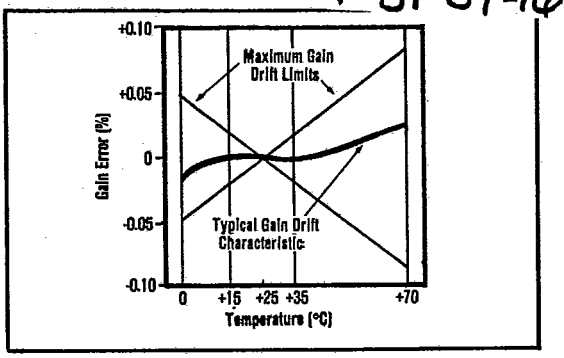

FIGURE 4. Gain Drift Error (%) vs Temperature.

SETTLING TIME

Settling time for each DAC73/736 model is the total time (including slew time) required for the output to settle within an error band around its final value after a change in input (see Figure 5).

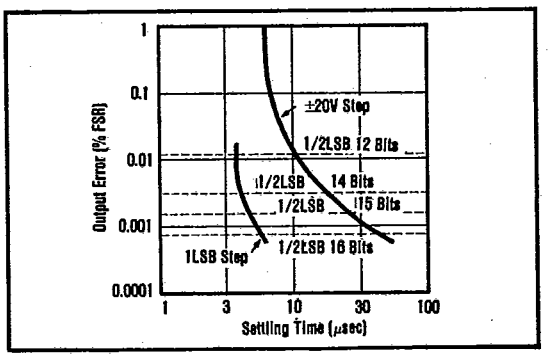

FIGURE 5. Full Scale Range Settling Time vs Accuracy.

Settling times are specified to ±0.00075% of FSR; one for maximum full scale range changes of 20V and one for a 1LSB change. The 1LSB change is measured at the major carry (0111...11 to 1000...00), the point at which the worst case settling time occurs.

COMPLIANCE

Compliance voltage is the maximum voltage swing allowed on the current output while maintaining

specified accuracy. The maximum compliance voltage is -1.5V to +10V.

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a power supply change on the D/A converter output. It is defined as a percent of FSR per percent of change in either the positive, negative, or logic supplies about the nominal power supply voltages (see Figure 6).

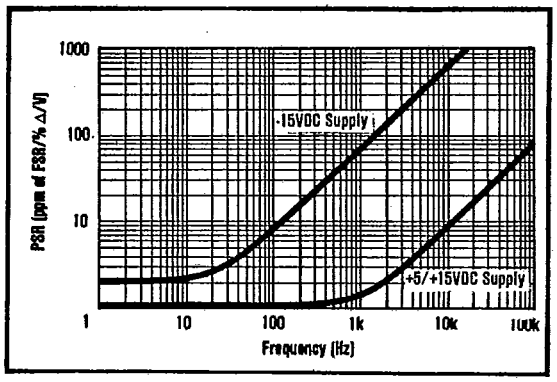

FIGURE 6. Power Supply Rejection vs Power Supply Ripple Frequency.

REFERENCE SUPPLY

All models are supplied with an internal +6V reference voltage supply. This reference voltage (pin 52) has a tolerance of ±0.05% and is connected internally for specified operation. The zener is selected for a Gain Drift of typically ±4ppm/°C and is burned-in for a total of 48 hours for guaranteed reliability. This reference may also be used externally but the current drain is limited to 4mA and constant load conditions.

INSTALLATION AND OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

For optimum performance and noise rejection the DAC73/736 decoupling capacitors are included internally. Refer to Figure 13 for correct grounding connections.

OFFSET AND GAIN ADJUSTMENT

Before taking measurements or making adjustments, the DAC73/736 should be warmed up for at least 25 minutes. The DAC73 has internal gain and offset potentiometers that are connected to an internal regulated supply. In most applications no external adjustment will be required.

External offset and gain adjustment of the DAC736, or DAC73 if the application requires, maybe accomplished as shown in Figures 7 and 8. These external circuits could be used in an application using both unipolar and bipolar modes. Refer to Figures 9 and 10 for relationship of offset and gain adjustments to unipolar and bipolar D/A converters. The internal potentiometers could be used to null the unipolar gain and offset, and the external null could be switched in by relays to null bipolar gain and offset. An alternate offset adjustment is shown on the DAC736 connection diagram.

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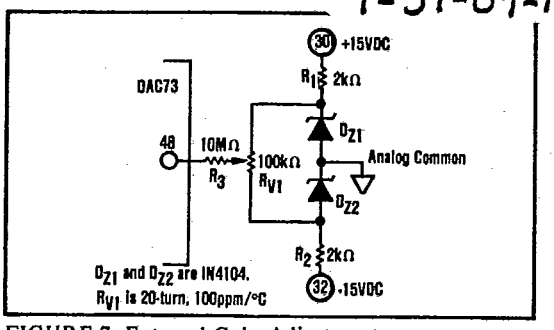

FIGURE 7. External Gain Adjustment.

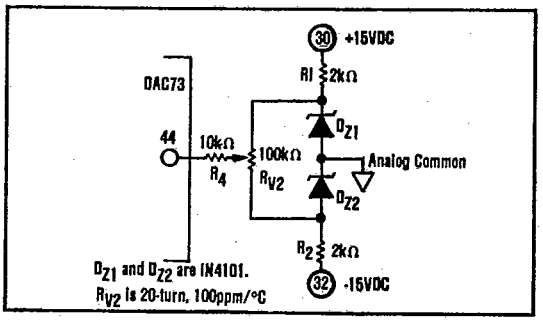

FIGURE 8. External Offset Adjustment.

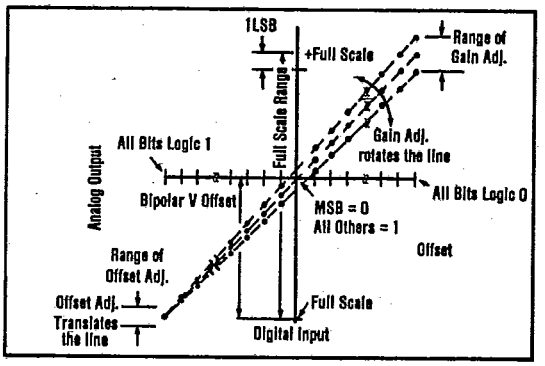

FIGURE 9. Relationship of Offset and Gain Adjustments for a Bipolar D/A Converter.

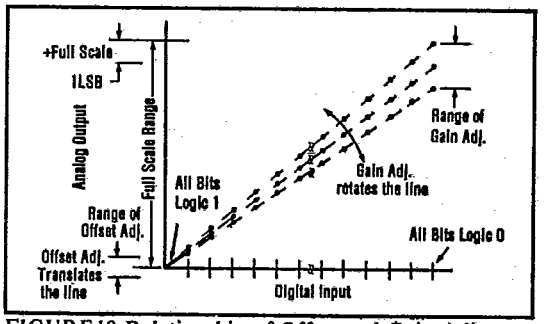

FIGURE 10. Relationship of Offset and Gain Adjustments for a Unipolar D/A Converter.

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OUTPUT RANGE CONNECTIONS

Internal scaling resistors in the DAC73/736 provide a wide range of output voltage range connections. These internal resistors may be connected to provide three bipolar output voltage ranges of ±10V, ±5V, or ±2.5V or two unipolar voltage ranges of 0 to +5V or 0 to +10V. Since the internal scaling resistors are an integral part of the DAC73/736, gain and offset drift are minimized by their use. Connections for DAC73/736 are shown in Table II. Figure 11 is a connection diagram.

TABLE II. Output Range Connections.

Output Range	Digital Input Codes	Connect Pin 47 to	Connect Pin 46 to	Connect Pin 44 to	Connect Pin 68 to
±10V	COB	68	44	69	47
±5V	COB	70	44	69	NC
±2.5V	COB	70	44	69	69
0 to +10V	CSB	70	NC	69	NC
0 to +5V	CSB	70	NC	69	69

In all cases pins 52 and 53 and pins 48 and 49 should be shorted together with low resistance/capacitance connections.

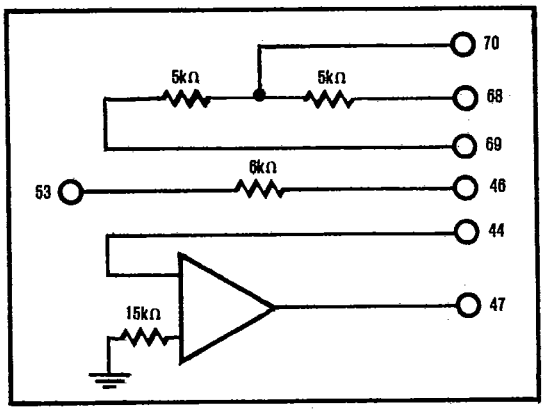

FIGURE 11. Output Amplifier Voltage Range Scaling Circuit.

LINEARITY ADJUSTMENT

Internal

If it becomes necessary to adjust the linearity of the DAC73 or DAC736 after an extended time period or for operation under temperature extremes, the 4MSB's may be user-adjusted. For optimum operation the unit should be calibrated in its operating environment. Calibration is performed by a differential linearity adjustment at the first four major carries. This method of calibration is possible since the DAC73 and DAC736 have almost no superposition error. The calibration procedure including gain, offset, and linearity adjustment is outlined in Table III. Steps 1 and 10 may be omitted for linearity adjustment only.

External (DAC73 only)

The linearity adjustment of the first 4MSB's of the DAC73 may be accomplished externally either with potentiometers or with D/A converters. Using a DAC to adjust linearity will allow computer controlled accuracy adjustments of the DAC thus giving the capability of maintaining 16-bit accuracy over all environmental variations. Gain and offset may also be adjusted in this manner.

Eight-bit bipolar voltage output DAC's can be used for all of the adjustments. Each circuit is shown in Figure 12.

INSTALLATION CONSIDERATIONS

To maintain the extremely-high accuracy of the DAC73 and DAC736 when installed in a system environment, careful attention must be paid to grounding and to connection resistances. Figures 13 and 14 are examples of correct connection configurations to yield maximum accuracy. The effects of various wiring and contact resistances R_1, R_2, R_3, and R_4 are reduced or eliminated as follows.

R_1 appears in series with the feedback resistance and therefore introduces only a gain error that can be nulled during calibration.

R_2 is inside the output amplifier feedback loop and its effect will be reduced by the loop gain.

In Figure 13 for the DAC736, R_3 is in series with the load

TABLE III. Calibration Procedure.

STEP	HEX INPUT CODE	ADJUST POTENTIOMETER(1)	DVM READING		DESCRIPTION
			UNIPOLAR MODE	±10 VOLT BIPOLAR MODE	
1	FFFF	R_{V6}(2)	0.0V	-10.0000V	Null Offset
2	F000	N/A	V_4	V_4	Read Output Voltage
3	EFFF	R_{V4}	$V_4 + 153\mu V$	$V_4 + 305\mu V$	Adjust R_{V4} until DVM reads $V_4 + 1LSB$
4	E000	N/A	V_3	V_3	Read Output Voltage
5	DFFF	R_{V3}	$V_3 + 153\mu V$	$V_3 + 305\mu V$	Adjust R_{V3} until DVM reads $V_3 + 1LSB$
6	C000	N/A	V_2	V_2	Read Output Voltage
7	BFFF	R_{V2}	$V_2 + 153\mu V$	$V_2 + 305\mu V$	Adjust R_{V2} until DVM reads $V_2 + 1LSB$
8	8000	N/A	V_1	V_1	Read Output Voltage
9	7FFF	R_{V1}	$V_1 + 153\mu V$	$V_1 + 305\mu V$	Adjust R_{V1} until DVM reads $V_1 + 1LSB$
10	0000	R_{V5}	+9.999847V	+9.999695V	Adjust Gain

NOTES: 1. For potentiometer location see Pin Assignments. 2. External offset adjustment on DAC736.

resistor and will cause an error in the voltage across R_L. One-half LSB error would result at full load for $R_3 = 0.02\Omega$. Therefore, if possible, sense the output voltage to include R_3.

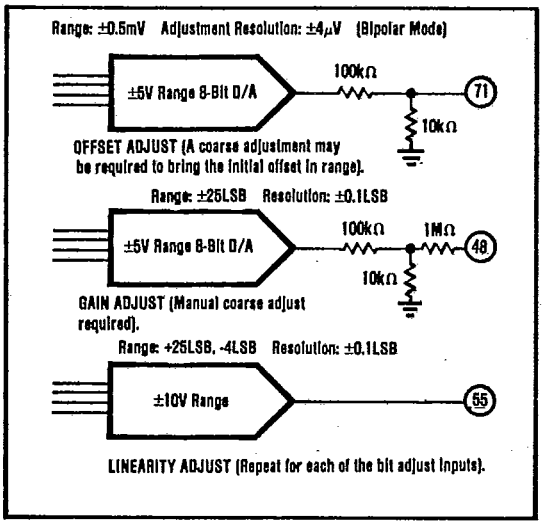

FIGURE 12. External Accuracy Adjustment.

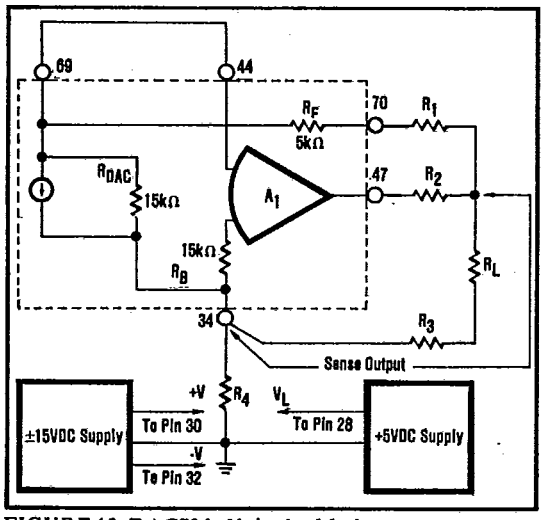

FIGURE 13. DAC736 - Unipolar Mode.

Figure 14 illustrates the optimum connection made possible by the ground sense pin on the DAC73. In the configuration shown $R'_F = R_F$ and $R'_B \parallel R_B = R_{DAC} \parallel R_{BPO}$. This causes any signal developed across R_3 to be rejected as a common-mode input, and R_3 will not affect the voltage across R_L. This configuration will also reject noise present on the system common.

R_4 is negligible in both circuits when ground connections are made as shown.

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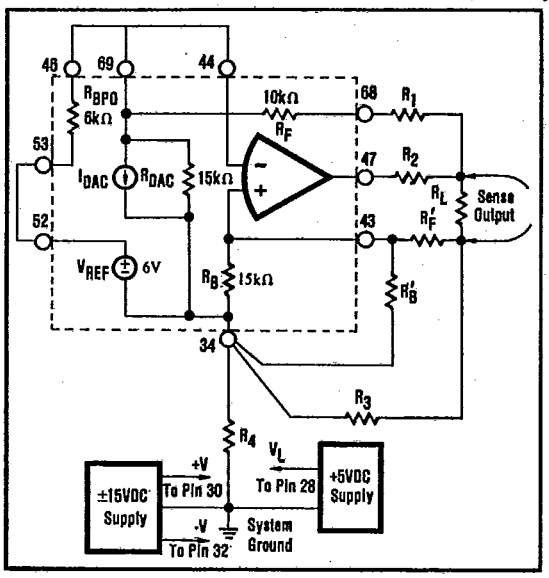

FIGURE 14. DAC73 - ±10V Bipolar Mode.

The DAC73/736 and the wiring to their connectors should be located to provide optimum isolation from sources of RFI and EMI. The key word in elimination of RF radiation or pickup is loop area. Therefore, signal leads and their return conductors should be kept close together. This reduces the external magnetic field along with any radiation. Also, if a signal lead and its return conductor are wired close together they present a small flux-capture cross section for any external field.