Measure on outputs chan B and C. The time between both signals is 1.4 usec



Programming the DAC80004 repetitive. The all channels are written repeatedly.

|  |  |  |
| --- | --- | --- |
| Channel  | Data 1 (hex) | Data 2 (hex) |
| A | a000 | a000 |
| B | 29a4 | bc2f |
| C | 29a4 | bc2f |
| D | 0000 | 0000 |

The last command 8 and channel F is used to enable SDO.

For debugging this time slot the channel selection, data, command and r\_wrn can be programmed.

The data in the pictures is sampled with a period with 6.25 nsec

Time between 32 edge of data channel B and channel C is 1256.25 nsec



Chan B Command 0

Chan C Command 2

Chan A Command 0

Chan D Command 0

Chan F Command 8

Repetitive read back of channel B C with command 0



Program Chan B

Command 0

Data bc2f

Read Chan B Command 0

Serial shift data Chan B

Read back data Chan B

Programmed data is read back OK

Repetitive read back of channel C with command 0



 Program Chan C Command 2

Data bc2f

Program Chan B

Command 0

Data bc2f

Serial shift data Chan C

Read back data Chan C

Repetitive read back of command 6 to check all LDAC register bits are 0

During data-in shift of reading of the LDAC register bits D03-D00 are set to “1010”

Returned read back bits D03-D00 are “0000”



 Read

 Command 6

Data “1010”

Read back data reg 6

Timing measurements

Qdac Clk period : 37 nsec

Blue: Data

Red: Clk

Yellow : Sync\_n

|  |  |
| --- | --- |
| A screenshot of a cell phone  Description automatically generated | A close up of a map  Description automatically generatedSync high period : 56.6 nsec |
| A close up of a map  Description automatically generatedTime falling edge clk to rising edge sync\_n : 18.2 nsec | A close up of a map  Description automatically generatedFalling edge sync\_n to falling edge clk : 18.2 nsec |
| A close up of a map  Description automatically generatedSetup time and level data ‘0’  | A close up of a map  Description automatically generatedsetup time and level data ‘1’ |