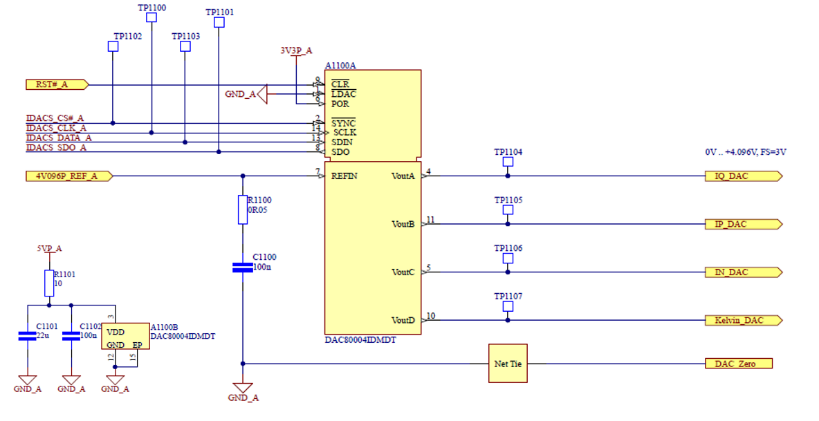
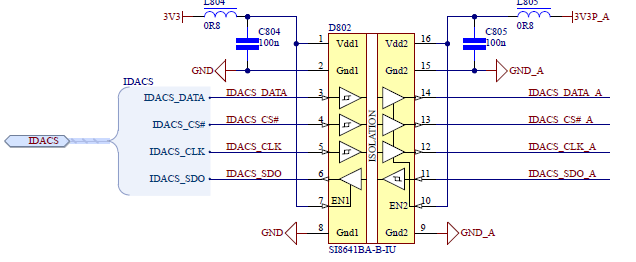
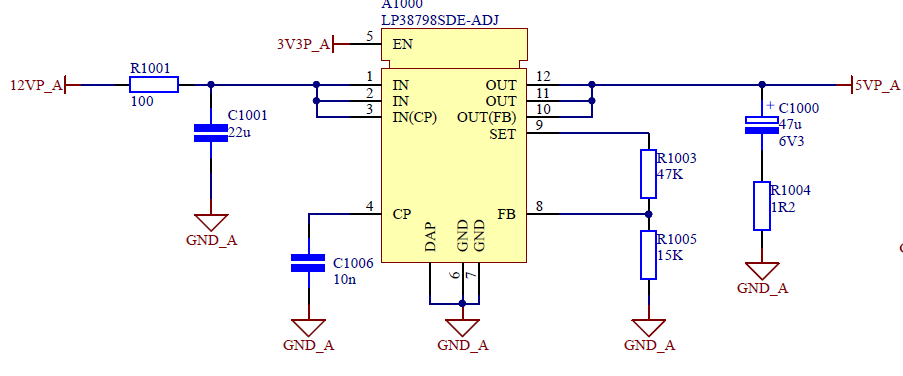
Schematic





FPGA side

NOTE: the DAC POR is now connected to the 5VP\_A with a modification on the PCB



The 12VP\_A and 3V3P\_A are supplies from one external supply and switched on simultaneously

A screenshot of a cell phone

Description automatically generated

Blue: Initialization complete @ IO pin

Red: Clk @ IO pin

Yellow : 5VP\_A

Green: Lock from PLL @ IO pin

NOTE: the grounding of the probes was not optimal