DAC38RF89 Test

TI Information– Selective Disclosure

DAC38RF89 bypass DUC Test

Test Setup:

Fdac = 5000Msps internal PLL

NCO not used

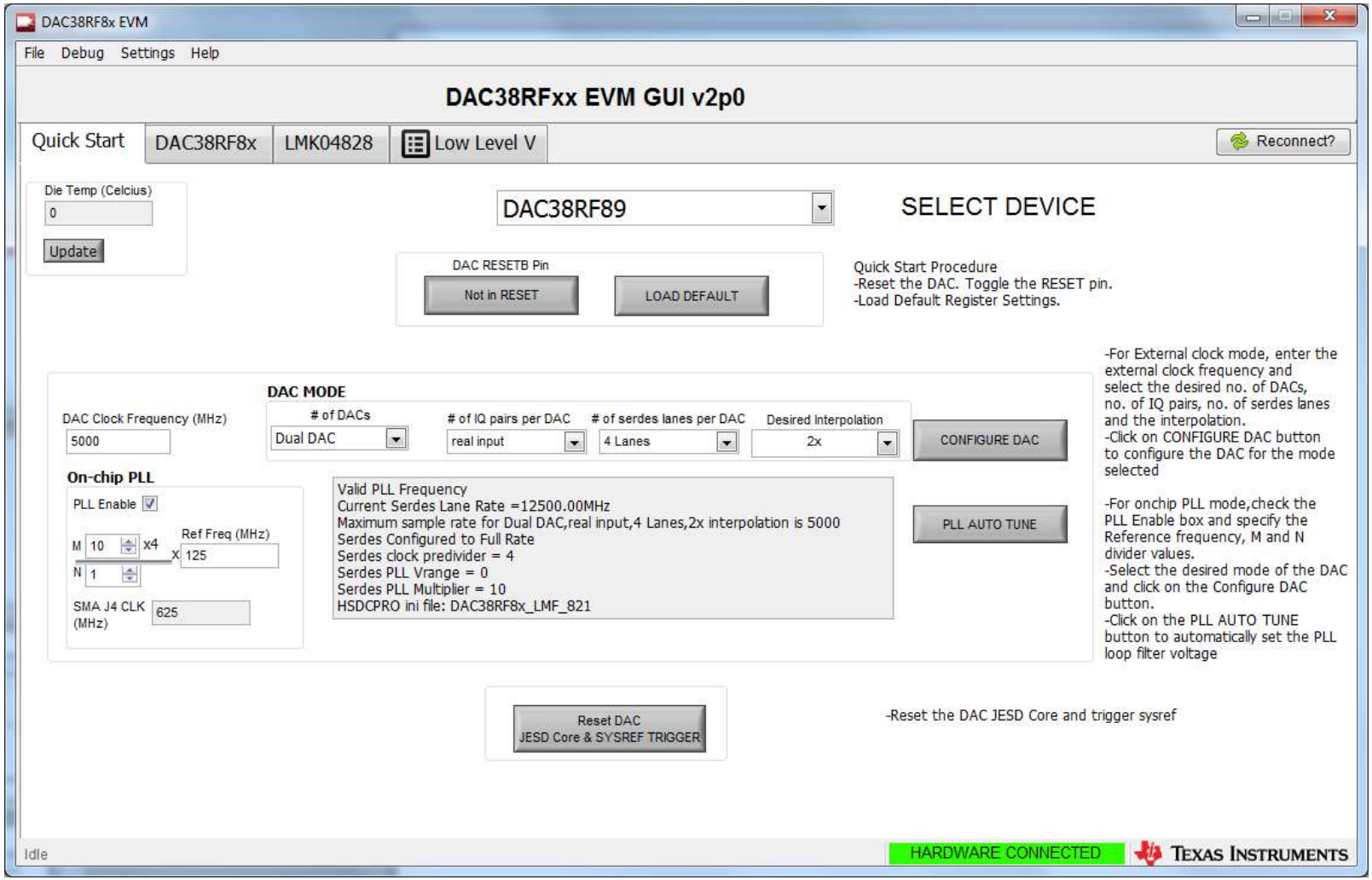
Int 2X

IF = 50 tones from 100MHz to 1.2GHz

LMF = 821

TI Information– Selective Disclosure

DAC38RFxx EVM GUI
Click on “Not in RESET” then click on “DAC in RESET”. Click on “LOAD DEFAULT”
Enter parameters, then click on “CONFIGURE DAC.
If using the DAC PLL, click on “PLL AUTO TUNE”.



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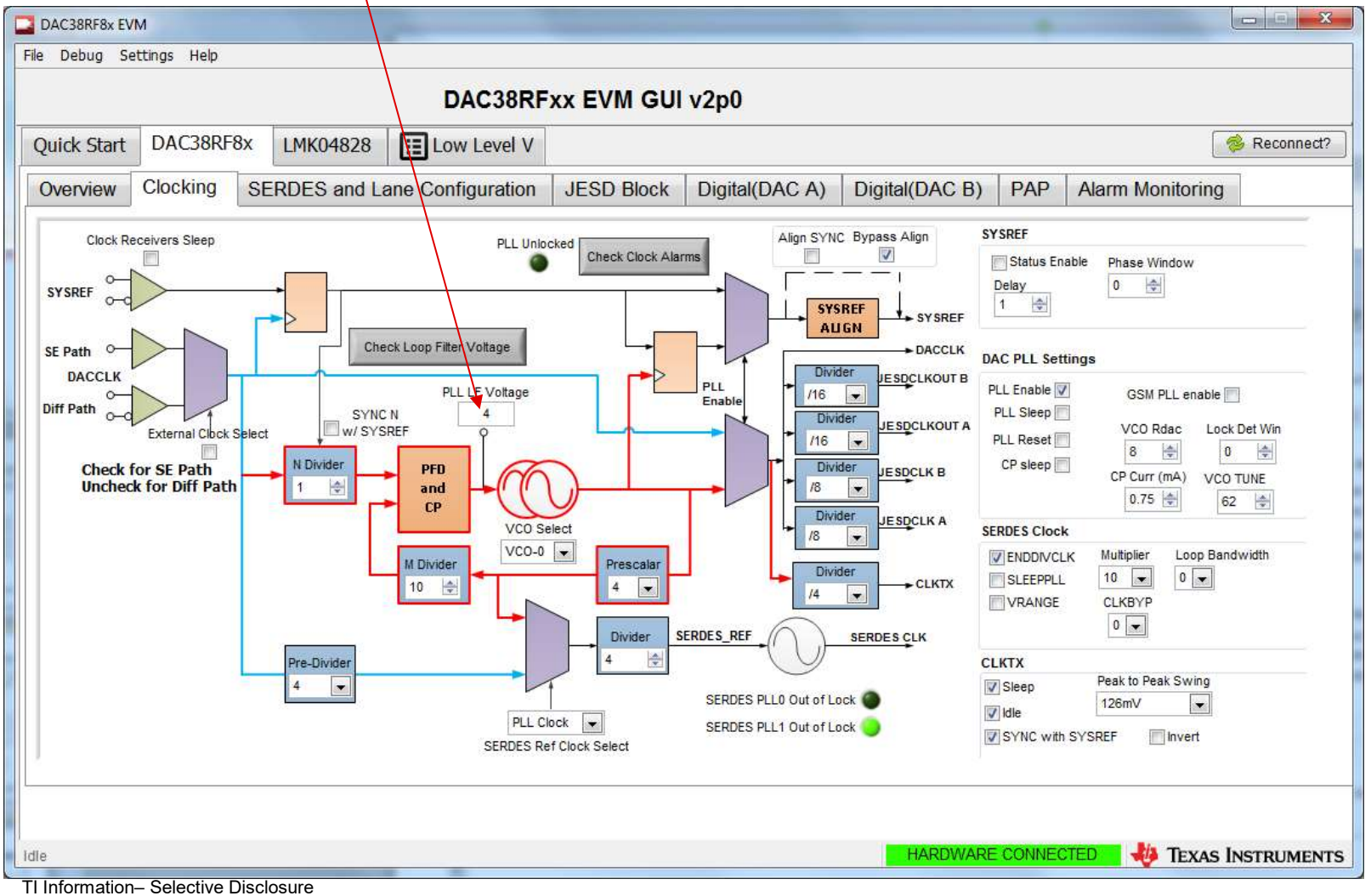
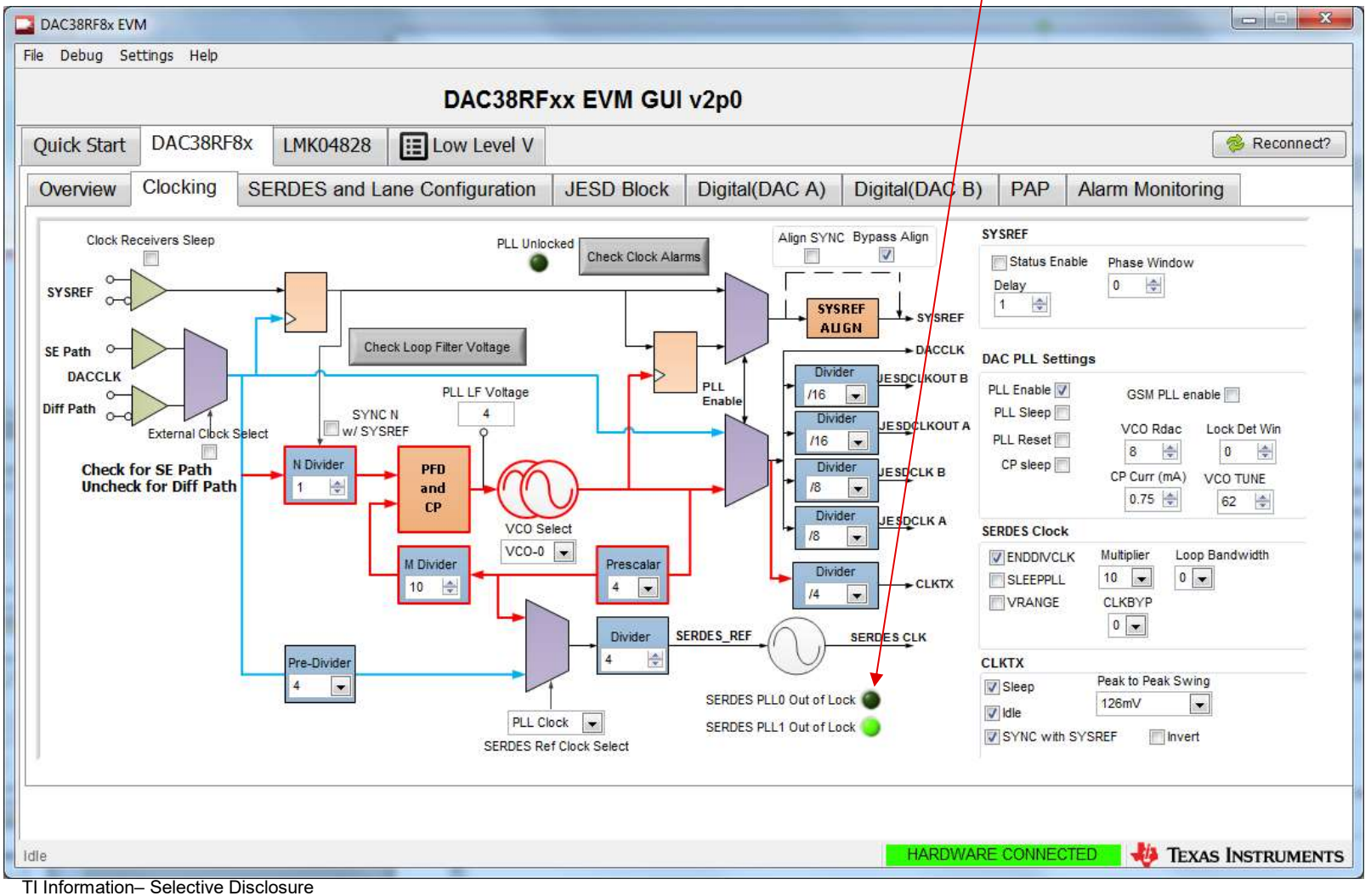
Clocking Settings. Click on “Check Loop Filter Voltage” and verify the PLL LF Voltage is between 3-5.



Verify the SERDES PLL0 is not Out of Lock by clicking here. This indicator shall turn off (not green) if SERDES PLL is locked.



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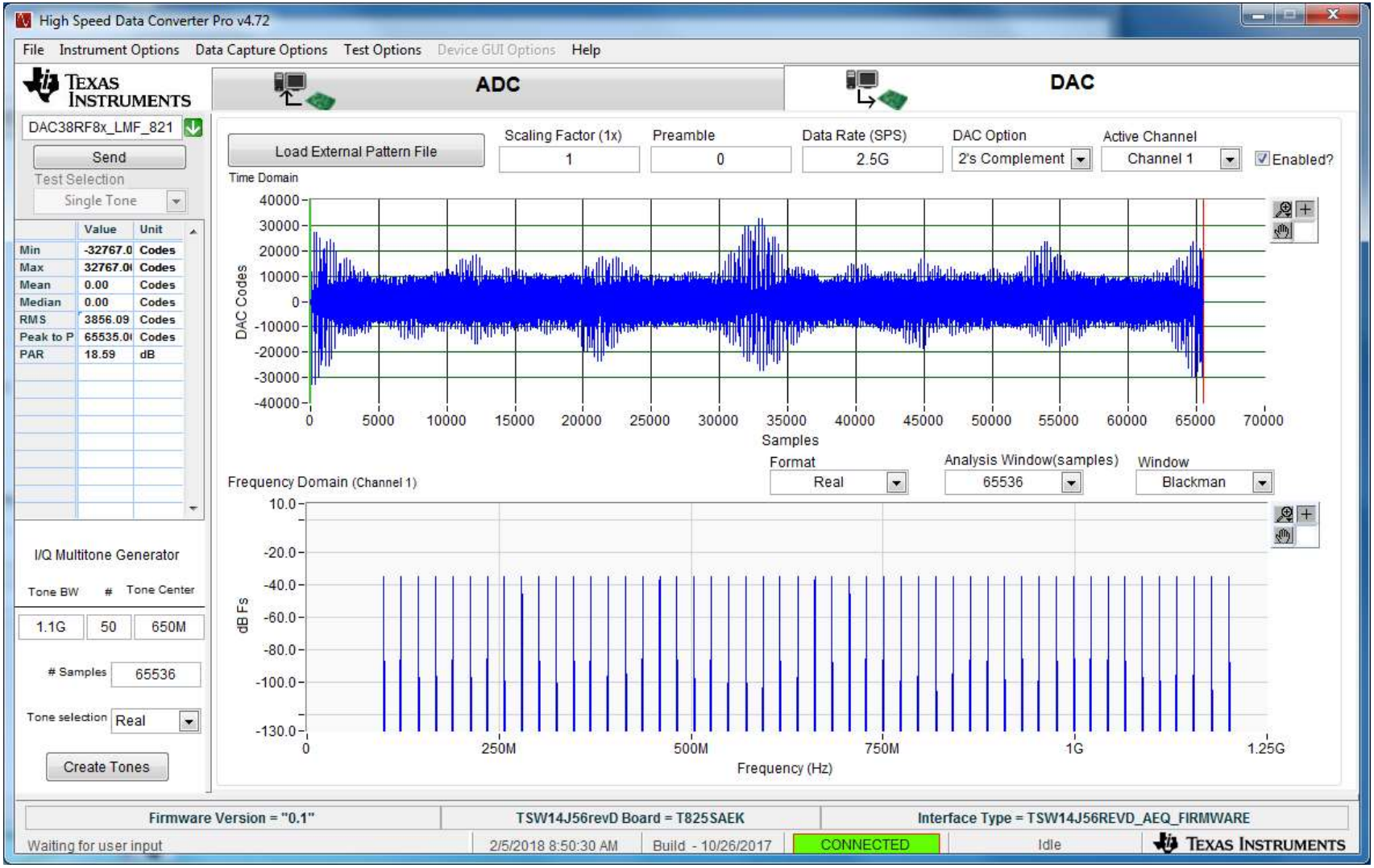
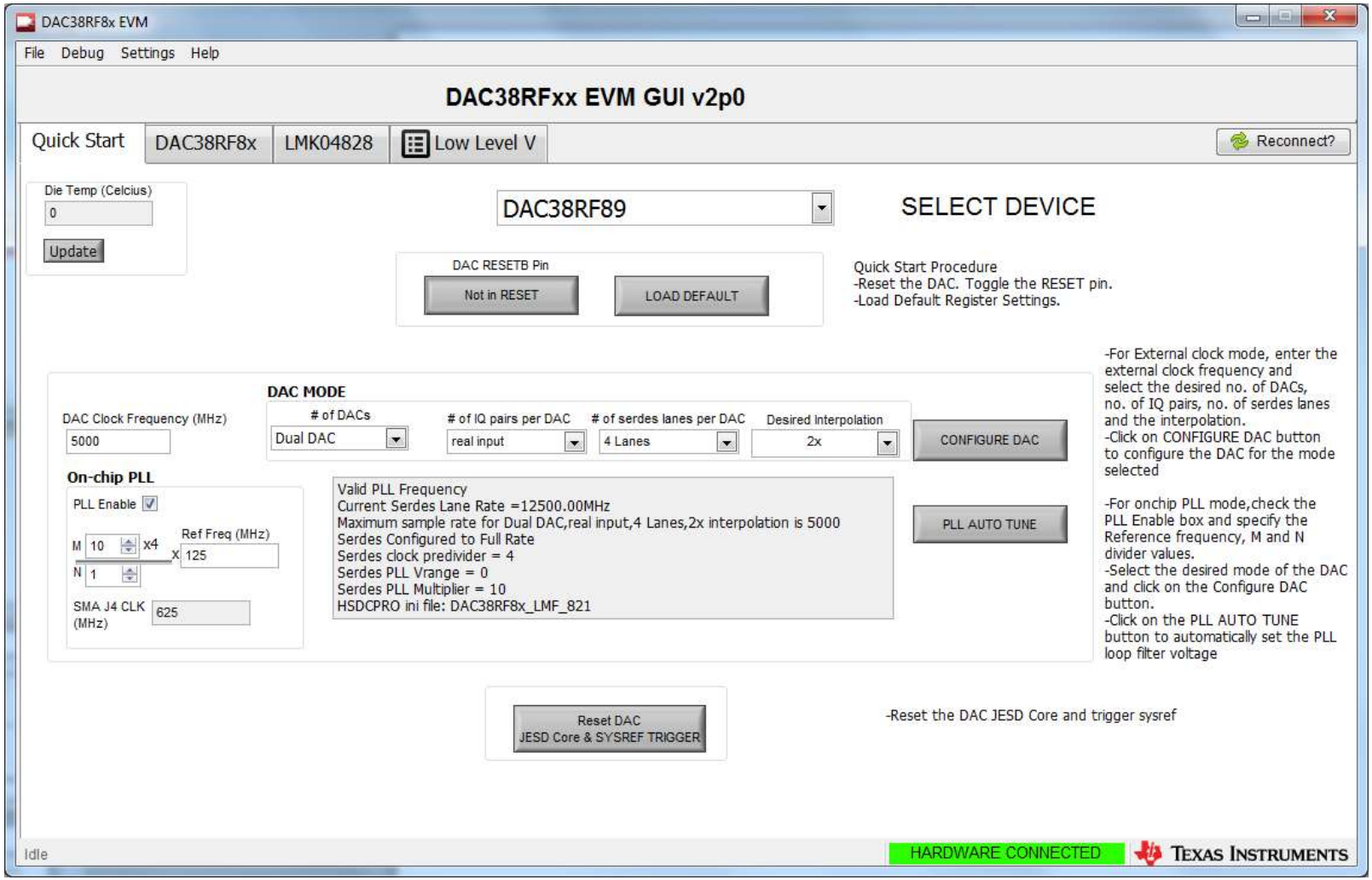
TSW14J56 Settings. Load HSDC Pro as shown below. Click on “Create Tones”, then “Send”



Go back to the DAC38RFxx EVM GUI and click on “Reset DAC JESD Core & SYSREF TRIGGER”



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DAC output at SMA J6