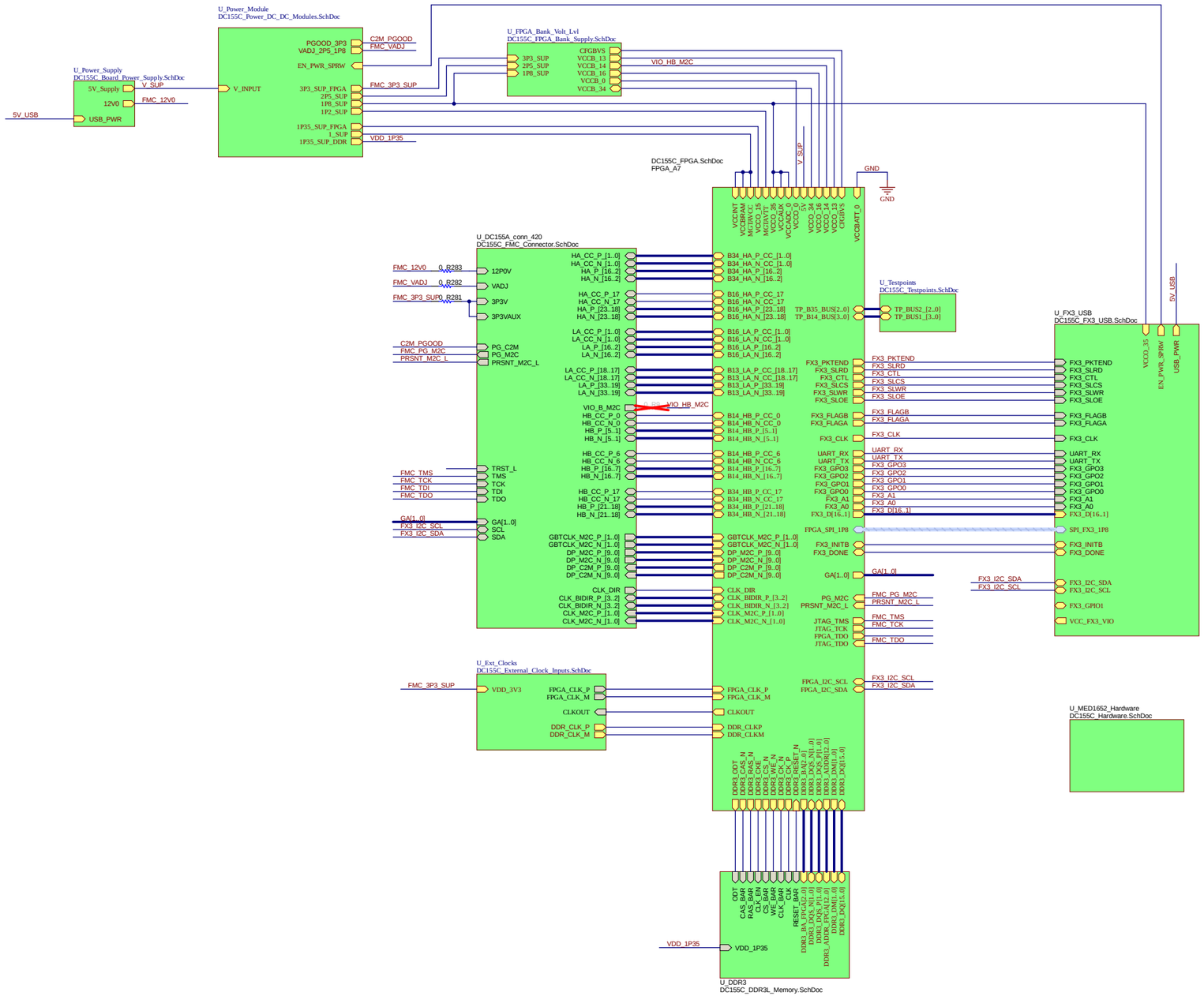
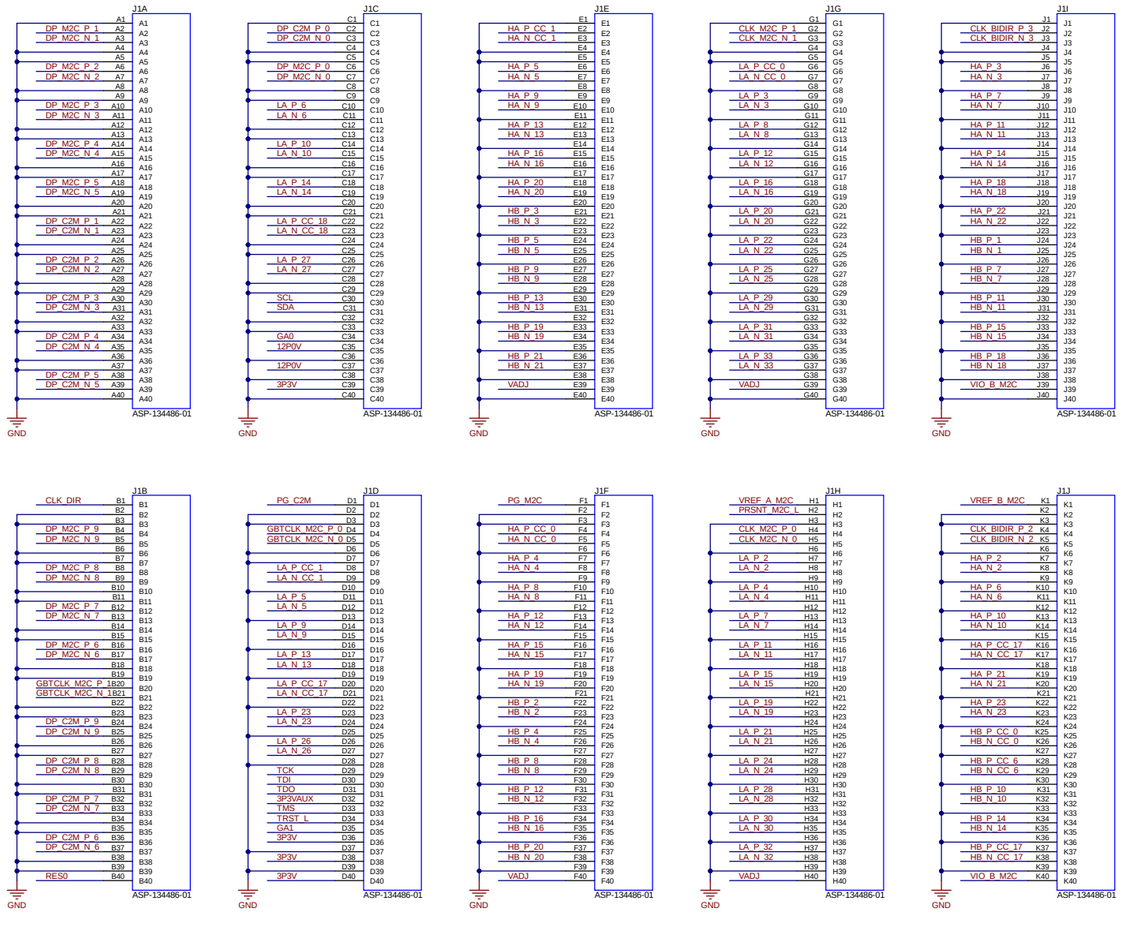
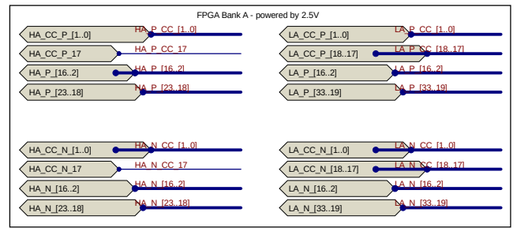
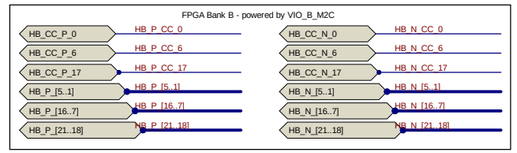
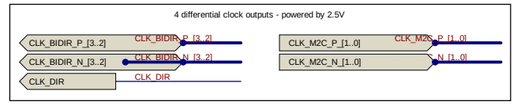


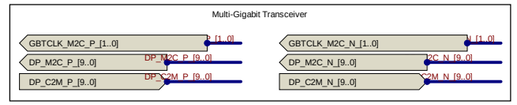
Orderable: TSWDC155BEVM		Designed for: Public Release	Mod. Date: 3/3/2023
TID #: N/A		Project Title: DC155C	
Number: DC155C	Rev: 1P0	Sheet Title: Top_Level	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 1 of 18
Drawn By: TI		File: DC155C_Top_Level.SchDoc	Size: C
Engineer: Rahul Kulkarni		Contact: http://www.ti.com/support	

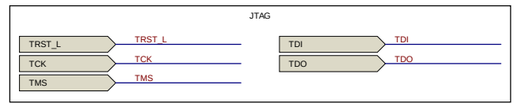


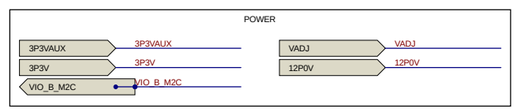


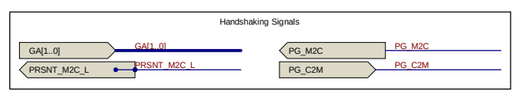












Connector includes:

- 16 LVDS pairs + 2 DCLK + 1FCLK for DUT1
  - DOUTP/M1_n, DCLKP/M1,3, FCLKP/M1
- 16 LVDS pairs + 2 DCLK + 1FCLK for DUT2
  - DOUTP/M2_n, DCLKP/M2,4, FCLKP/M2
- LVDS SPI Lines
  - 4 Data pairs-> S_DATAP/M_1/2/3/4
  - 2 Clock pair -> S_CLKP/M_1/2
  - 2 SEN pair -> S_SENP/M_1/2
- 6 LVDS high speed clock pairs (from FPGA)
  - CLKP/M_n
- 4 LVDS sync pairs (from FPGA)
  - SYNCP/M_n

- 6 CMOS SPI signals (SC -> SPI CMOS)
  - SC_DATA_n, SC_SCLK_n, SC_SEN_n, SC_SDOUT_n
- 36 general purpose IOs -> GPIOx

- SPI Buses from FX3
  - I2C from FX3
  - SPI bus (FX3_COM bus with 6 SEN's)

-Power lines for DUT
  - 5 Power lines from the Sullins Connecter
  - 1.8, 2.5 & 3.3V FPGA supplies.
- FX3 VIO for reading IDs

- Clocks from LMK
  - 5 DCLK lines
  - 6 SDCLK lines
  - Option for 2 more DCLK lines
  - 100M CLK

- JESD high speed lines
  - 4 GTP RX/TX lines
  - 2 MGT_REFCLK lines
  - MGT Ref signal

- Option to use FPGA's on-chip ADC if necessary

- 200M crystal clock input for the DUT board.

Connector includes:

- HA : 21 pairs + 3 clock pairs - powered by 2.5V
- LA: 30 pairs + 4 clock pairs - powered by 2.5V
- HB: 18 pairs + 3 clock pairs - powered by VIO_B_M2C

- GTP: 10 + 10 GTP + 2 REFCLKs

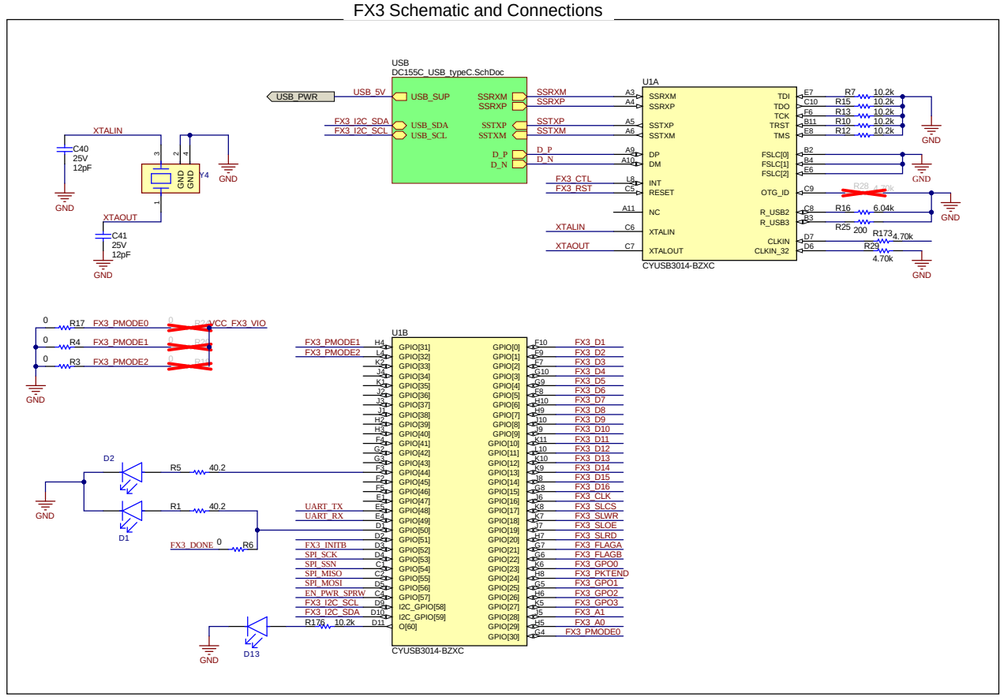
VREFA and VREFB for signalling levels of Bank A (HA/LA) are unused.

- I2C from FX3

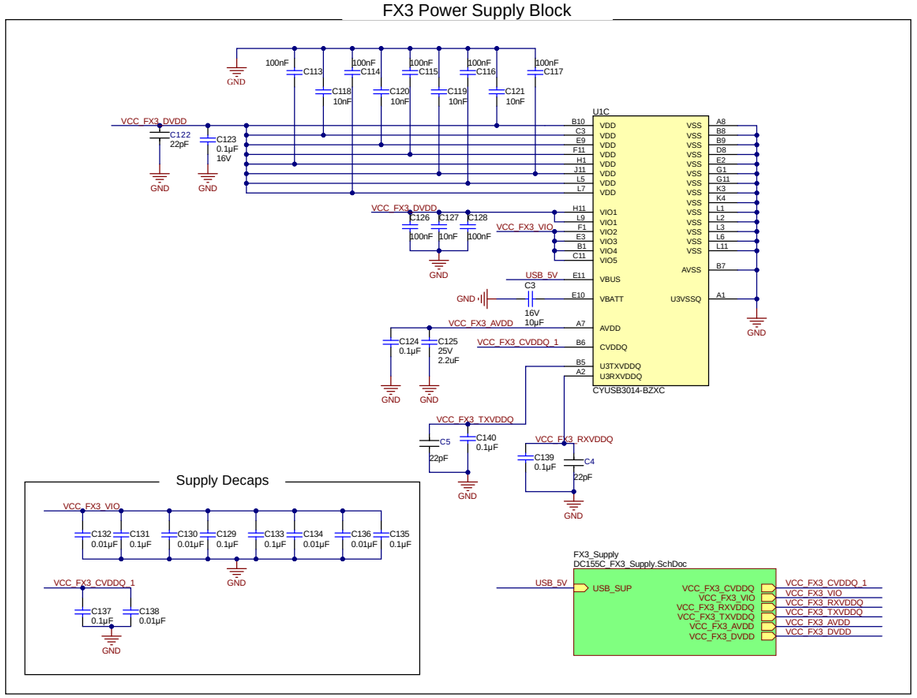
Orderable: TSWDC155BEVM		Designed for: Public Release	Mod. Date: 3/2/2023
TID #: N/A		Project Title: DC155C	
Number: DC155C	Rev: 1P0	Sheet Title: Conn_420	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 2 of 18
Drawn By: TI		File: DC155C_FMC_Connector.SchDoc	Size: C
Engineer: Rahul Kulkarni		Contact: http://www.ti.com/support	

Texas Instruments http://www.ti.com

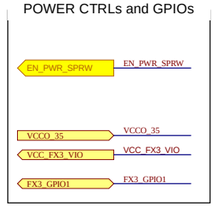
FX3 Schematic and Connections



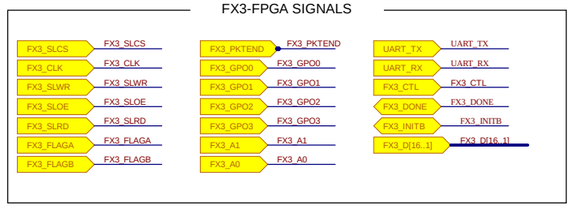
FX3 Power Supply Block



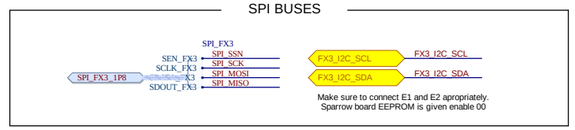
POWER CTRLs and GPIOs



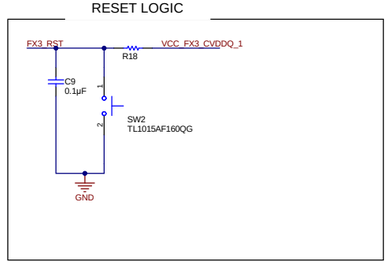
FX3-FPGA SIGNALS



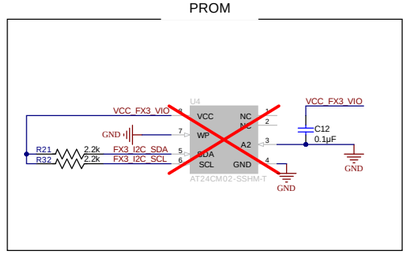
SPI BUSES



RESET LOGIC



PROM



Orderable: TSWDC155BEVM		Designed for: Public Release	Mod. Date: 3/2/2023
TID #: N/A		Project Title: DC155C	
Number: DC155C	Rev: 1P0	Sheet Title: FX3_USB	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 4 of 18
Drawn By: TI		File: DC155C_FX3_USB.SchDoc	Size: C
Engineer: Rahul Kulkarni		Contact: http://www.ti.com/support	

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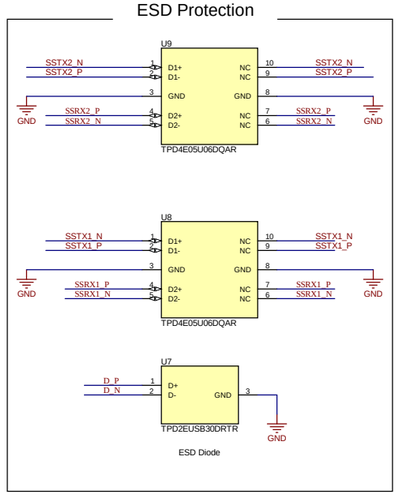
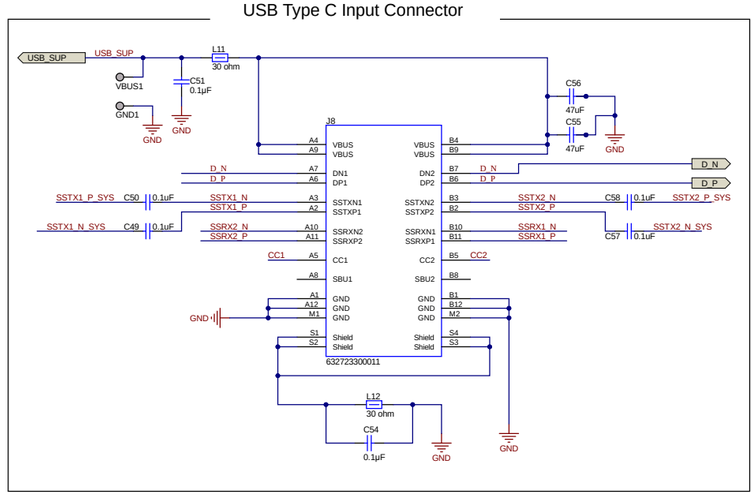
http://www.ti.com

USB_typeC.SchDoc

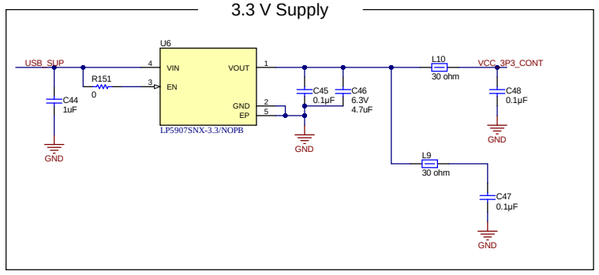
ESD Protection



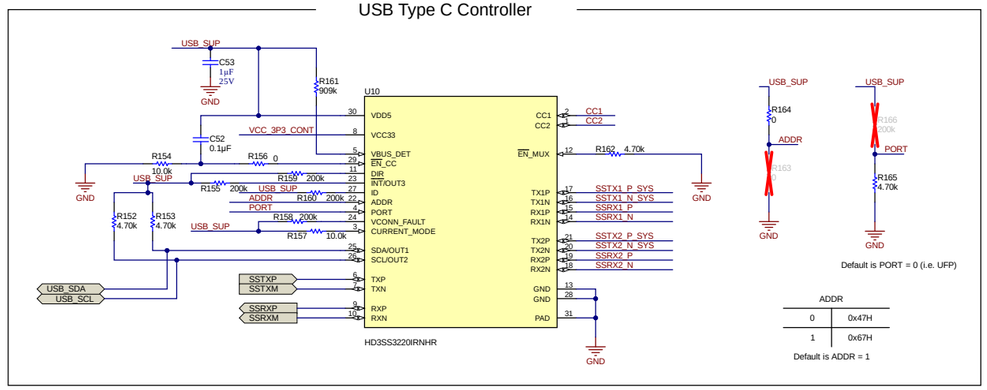
USB Type C Input Connector



3.3 V Supply



USB Type C Controller



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TID #: N/A		Project Title: DC155C	
Number: DC155C	Rev: 1P0	Sheet Title: USB_TypeC	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 5 of 18
Drawn By: TI		File: DC155C_USB_typeC.SchDoc	Size: C
Engineer: Rahul Kulkarni		Contact: http://www.ti.com/support	

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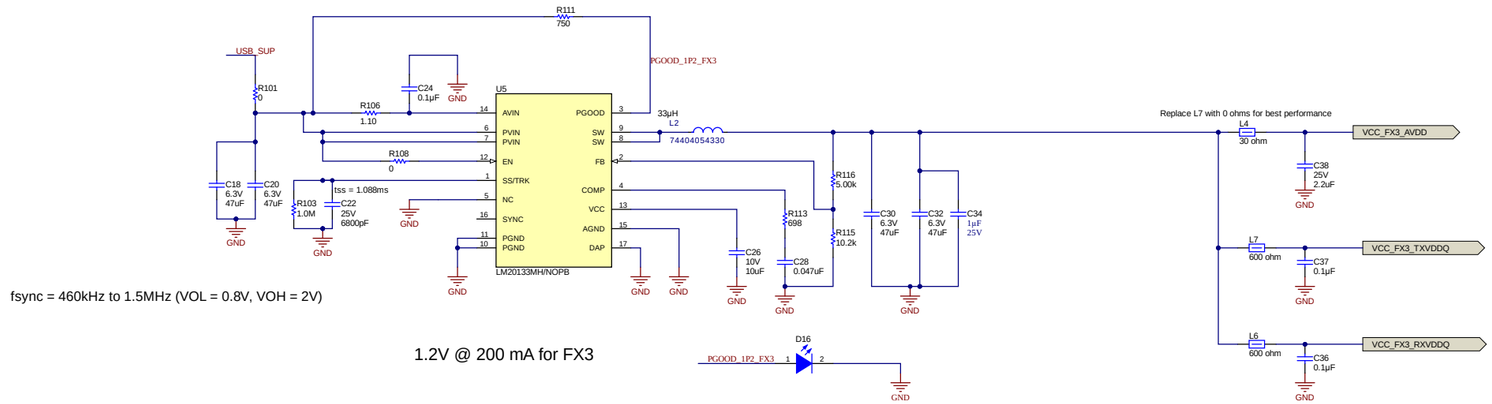
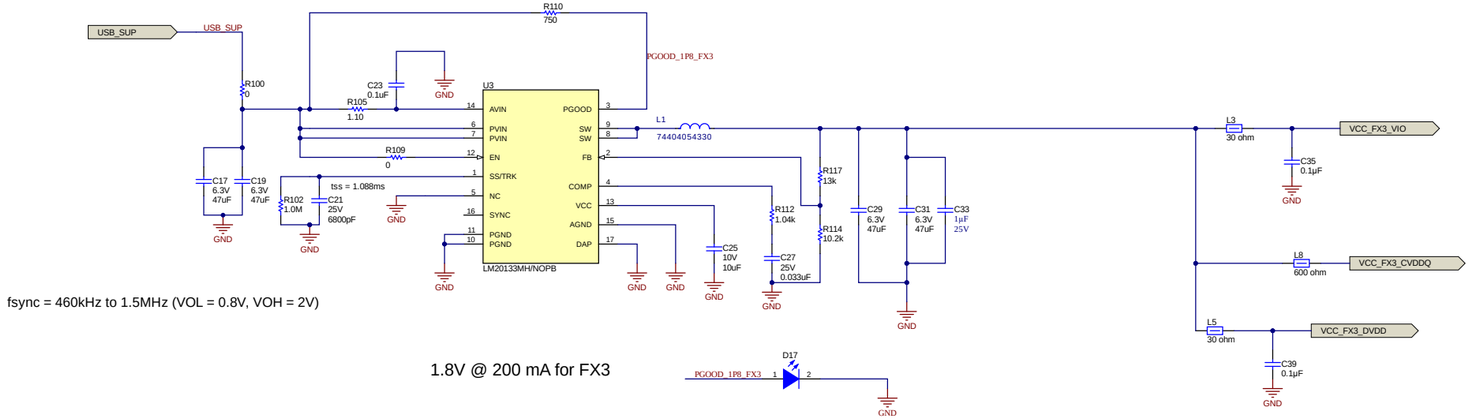
http://www.ti.com

FX3_Sup.SchDoc





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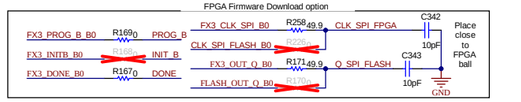
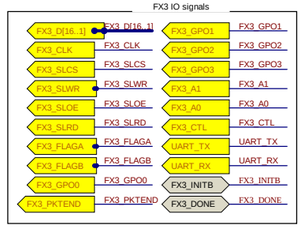
TID #: N/A		Project Title: DC155C	
Number: DC155C	Rev: 1P0	Sheet Title: FX3_Sup	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 6 of 18
Drawn By: TI		File: DC155C_FX3_Supply.SchDoc	Size: C
Engineer: Rahul Kulkarni		Contact: http://www.ti.com/support	http://www.ti.com

FPGA.SchDoc

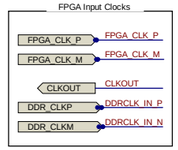
FPGA Firmware Download option

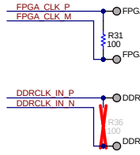


FX3 IO signals

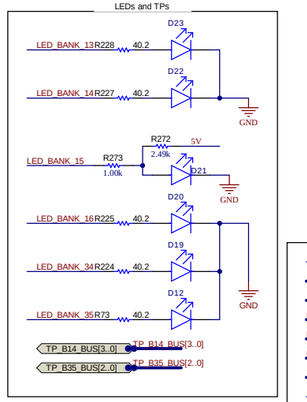


FPGA Input Clocks

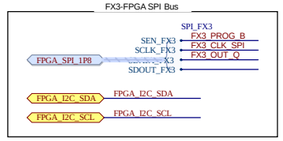




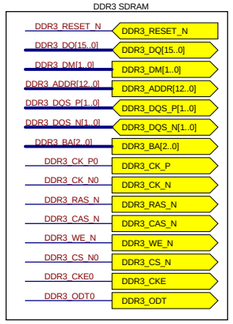
LEDs and TPs



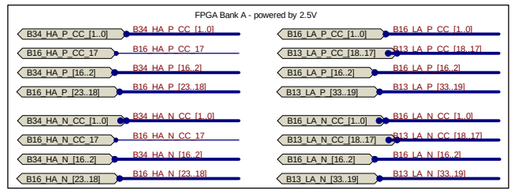
FX3-FPGA SPI Bus



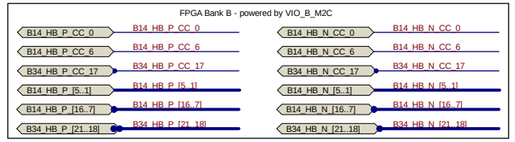
DDR3 SDRAM



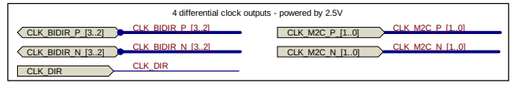
FPGA Bank A - powered by 2.5V



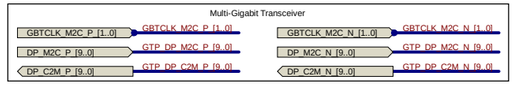
FPGA Bank B - powered by VIO_B_M2C



4 differential clock outputs - powered by 2.5V

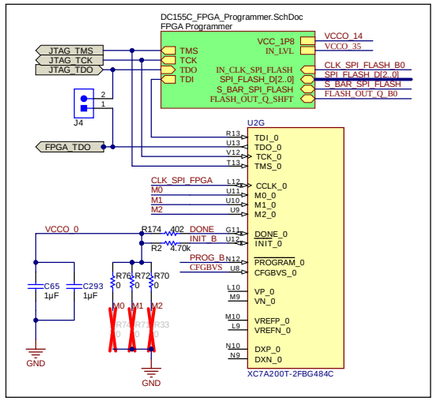


Multi-Gigabit Transceiver

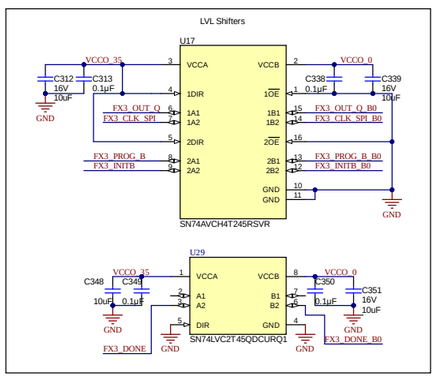


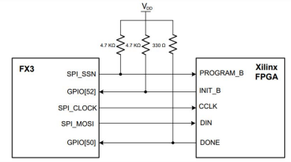
DC155C_FPGA_Programmer.SchDoc

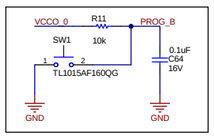
FPGA Programmer



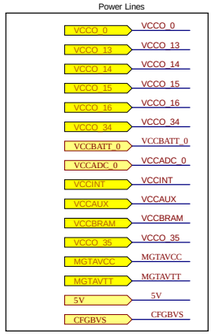
LVL Shifters



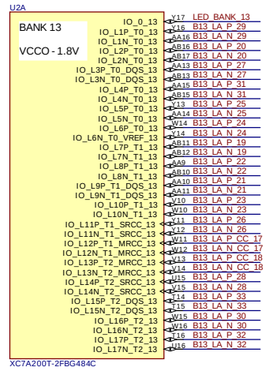




Power Lines



U2A



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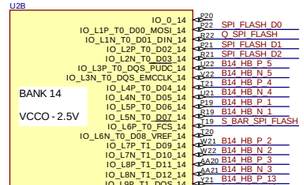

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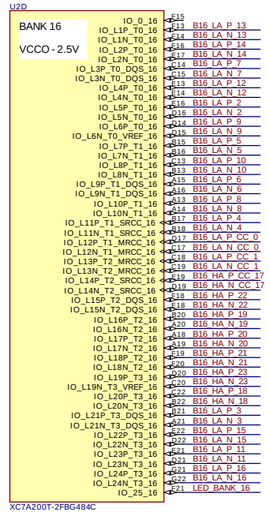
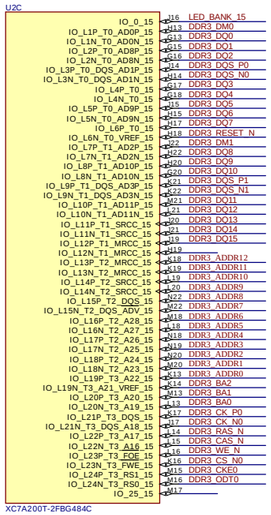


U2C



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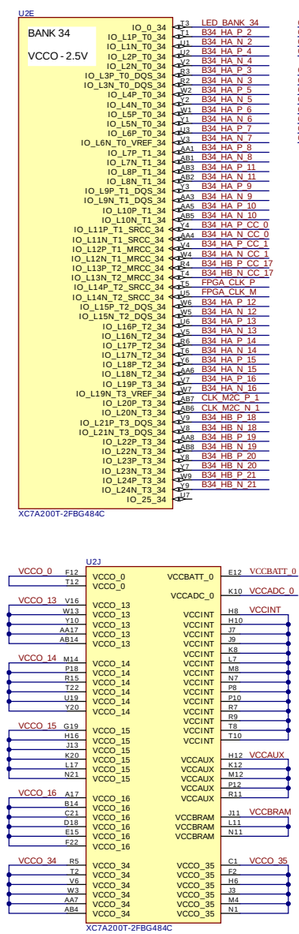
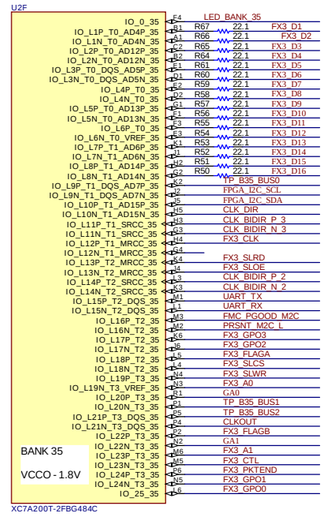


U2J

U2F



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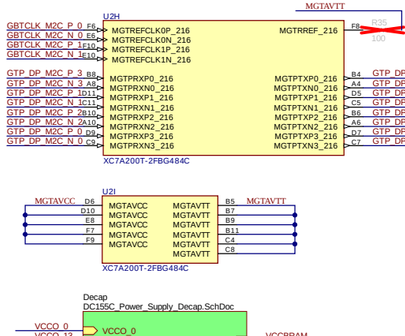

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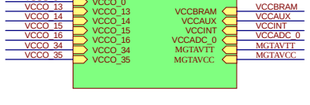
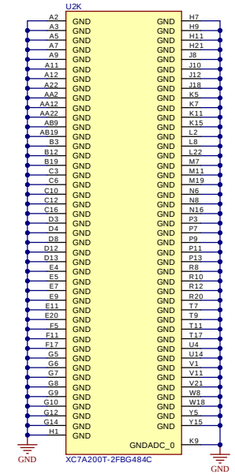


Decap

DC155C_Power_Supply_Decap.SchDoc

U2K



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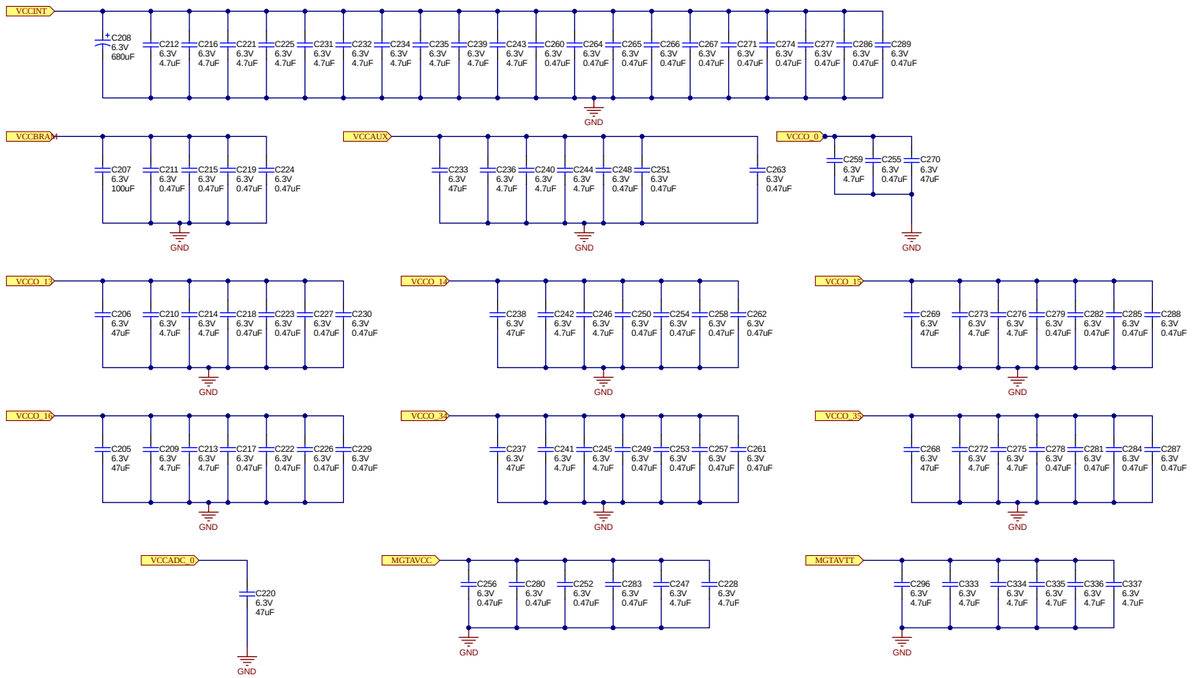
TID #: N/A	Project Title: DC155C		
Number: DC155C Rev: 1P0	Sheet Title: FPGA		
SVN Rev: Not in version control	Assembly Variant: 001	Sheet: 7 of 18	
Drawn By: TI	File: DC155C_FPGA.SchDoc	Size: C	
Engineer: Rahul Kulkarni	Contact: http://www.ti.com/support		

SupplyDecap.SchDoc



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Drawn By: TI		File: DC155C_Power_Supply_Decap.SchDoc	Size: C
Engineer: Rahul Kulkarni		Contact: http://www.ti.com/support	

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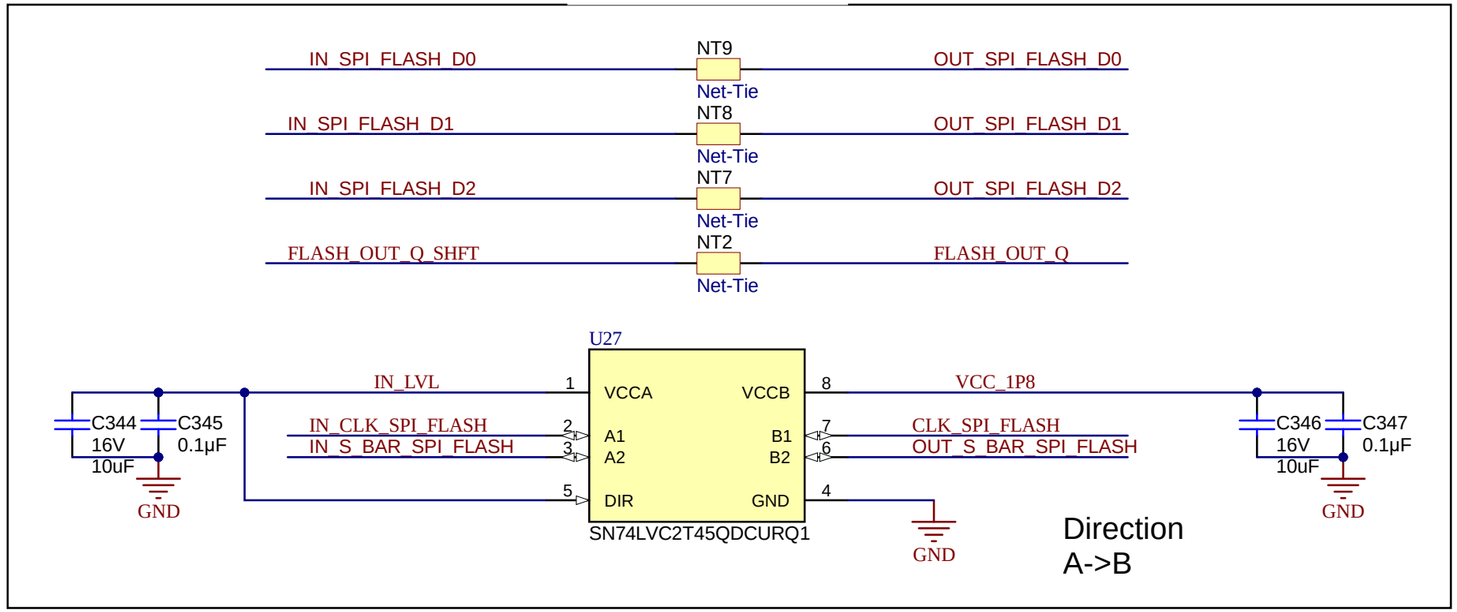
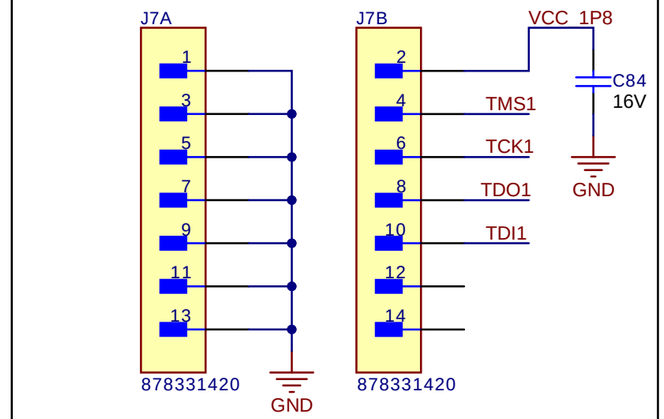
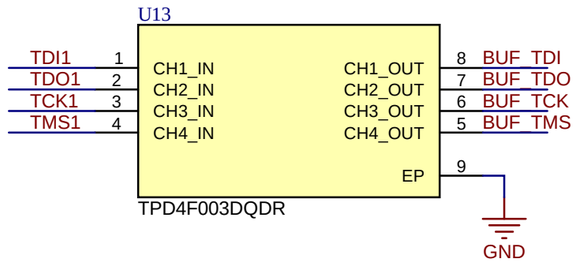
LVL Shifters

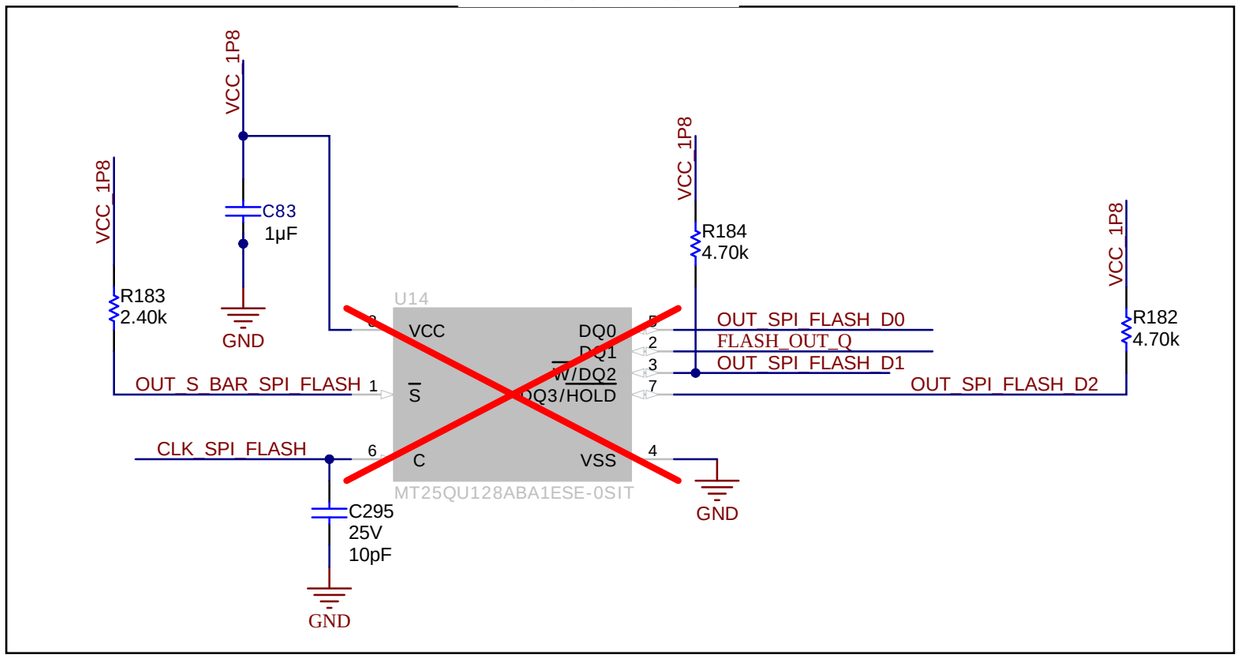


JTAG Connecter

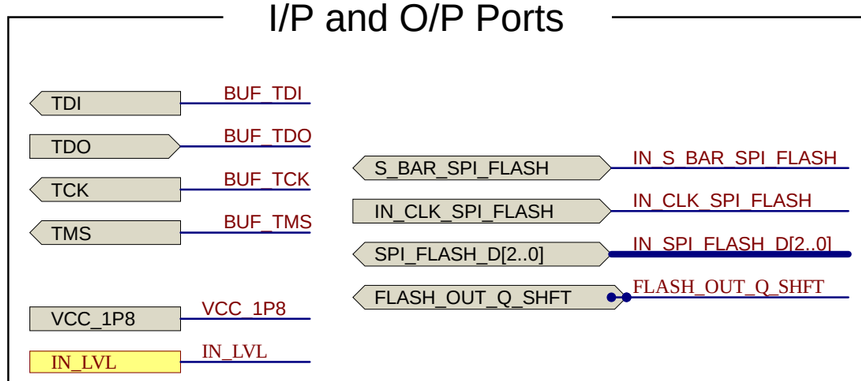




SPI Flash



I/P and O/P Ports



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TID #: N/A		Project Title: DC155C	
Number: DC155C	Rev: 1P0	Sheet Title: FPGA_Programmer	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 9 of 18
Drawn By: TI		File: DC155C_FPGA_Programmer.SchDoc	Size: A4
Engineer: Rahul Kulkarni		Contact: http://www.ti.com/support	

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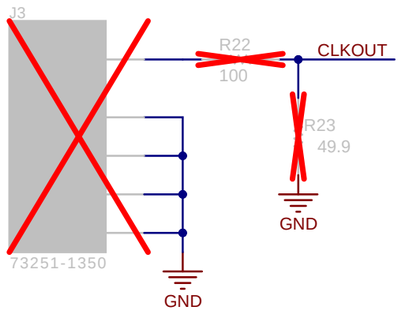
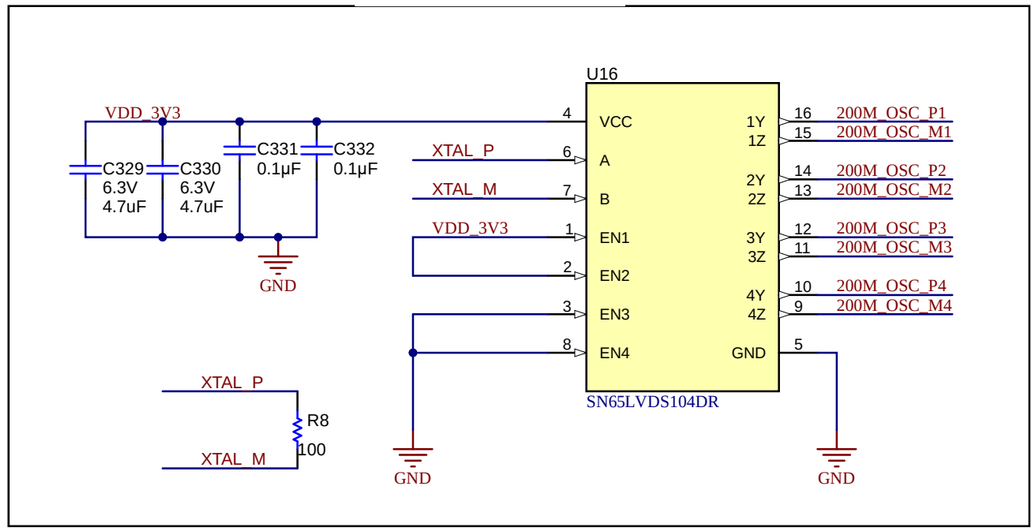
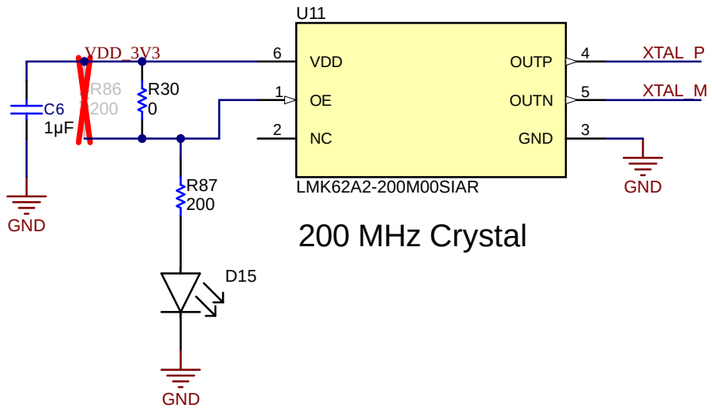
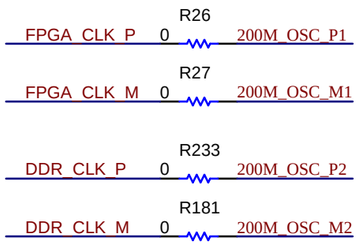
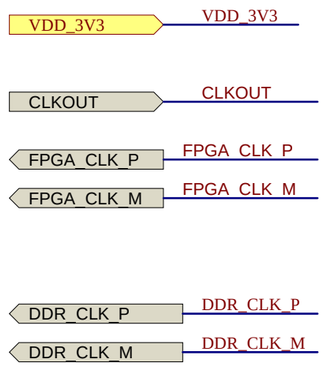


Clock Buffer









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TID #: N/A		Project Title: DC155C	
Number: DC155C	Rev: 1P0	Sheet Title: Ext_Clocks	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 10 of 18
Drawn By: TI		File: DC155C_External_Clock_Inputs.SchDoc	Size: Letter
Engineer: Rahul Kulkarni		Contact: http://www.ti.com/support	

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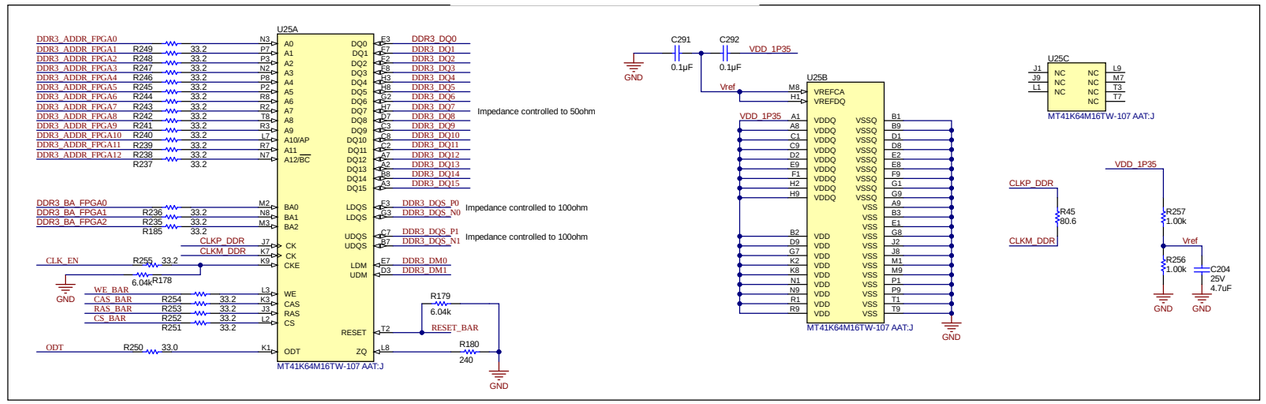
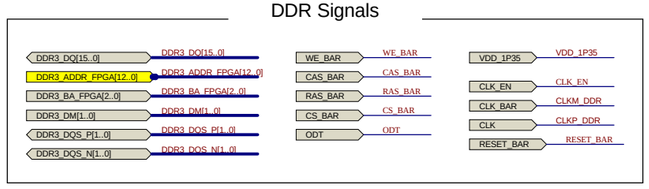
DDR3.SchDoc

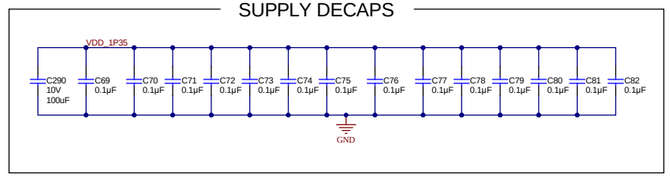
DDR3 Schematic and Connections



DDR Signals



SUPPLY DECAPS



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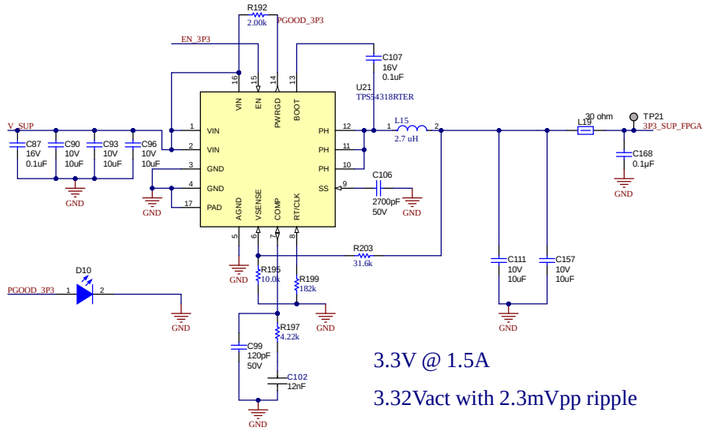
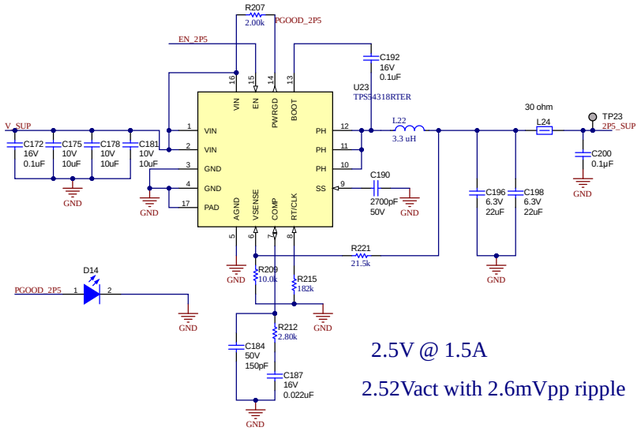
TID #: N/A		Project Title: DC155C	
Number: DC155C	Rev: 1P0	Sheet Title: DDR3	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 11 of 18
Drawn By: Ti		File: DC155C_DDR3L_Memory.SchDoc	Size: C
Engineer: Rahul Kulkarni		Contact: http://www.ti.com/support	http://www.ti.com

Power_Module.SchDoc



3.3V @ 1.5A

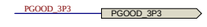
3.32Vact with 2.3mVpp ripple

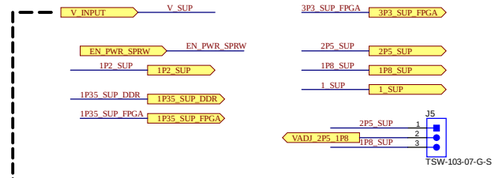


2.5V @ 1.5A

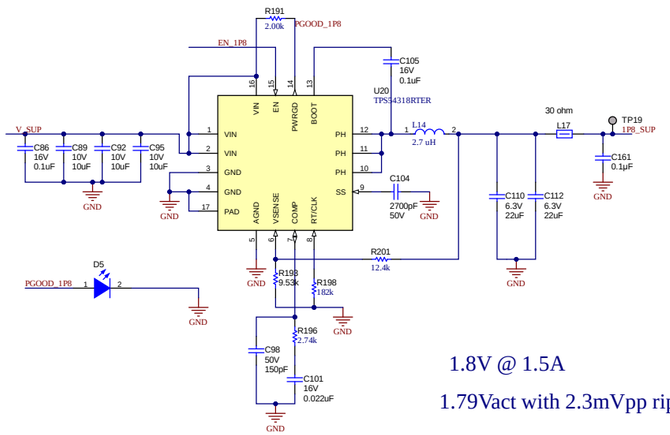
2.52Vact with 2.6mVpp ripple

PORTS



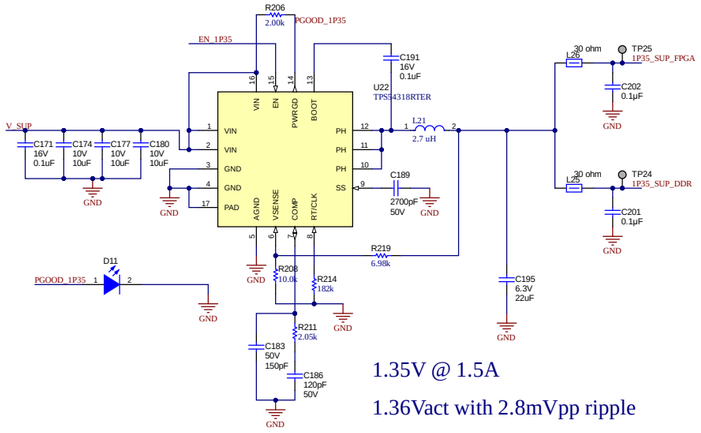


Input Supply Range : 4.8-5.2V



1.8V @ 1.5A

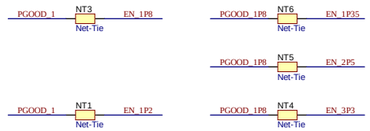
1.79Vact with 2.3mVpp ripple

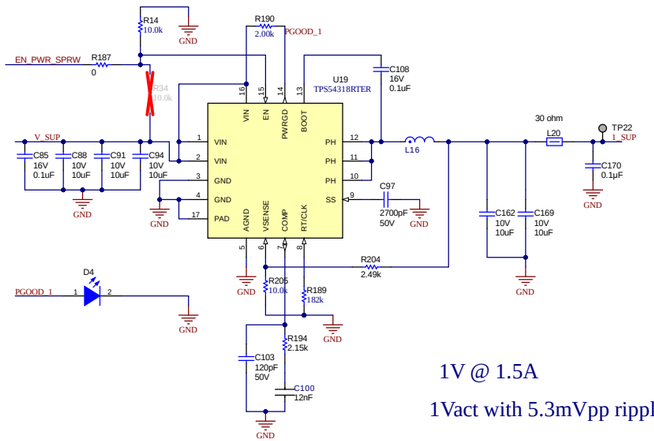


1.35V @ 1.5A

1.36Vact with 2.8mVpp ripple

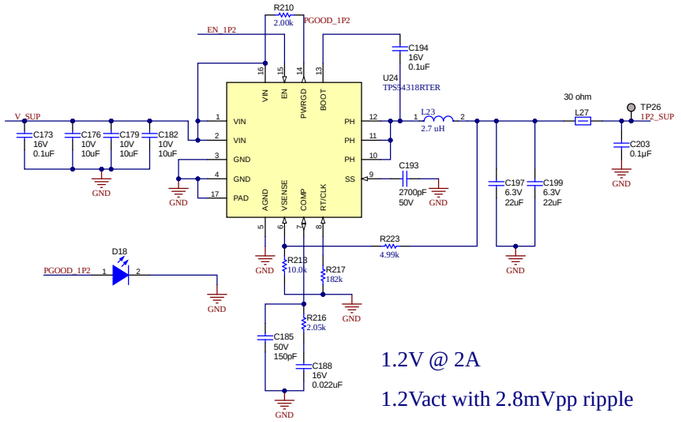
POWER SEQUENCING





1V @ 1.5A

1Vact with 5.3mVpp ripple



1.2V @ 2A

1.2Vact with 2.8mVpp ripple

NOTES

FPGA_INT -> 1_SUP

FPGA_BRAM -> 1_SUP

FPGA_AUX -> 1P8_SUP

FPGA_VCCO -> 1P35_SUP, 2P5_SUP & 3P3_SUP

FPGA_MGTAVCC -> 1_SUP

FPGA_MGTAVTT -> 1P2_SUP

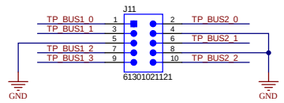
FPGA_ADC_SUP -> 1P8_SUP

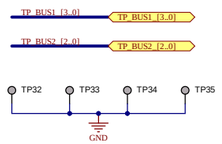
SEQUENCING

FPGA_INT
FPGA_BRAM
FPGA_MGTAVCC
FPGA_ADC_REF
--> FPGA_AUX, FPGA_ADC_SUP --> FPGA_VCCO

Orderable: TSWDC155BEVM		Designed for: Public Release	Mod. Date: 3/2/2023
TID #: N/A		Project Title: DC155C	
Number: DC155C	Rev: 1P0	Sheet Title: Power_Module	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 12 of 18
Drawn By: TI		File: DC155C_Power_DC_DC_Modules.SchDoc	Size: C
Engineer: Rahul Kulkarni		Contact: http://www.ti.com/support	http://www.ti.com

TestPoints.SchDoc





Orderable: TSWDC155BEVM		Designed for: Public Release	Mod. Date: 3/2/2023
TID #: N/A		Project Title: DC155C	
Number: DC155C	Rev: 1P0	Sheet Title: Test Points	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 14 of 18
Drawn By: TI		File: DC155C_Testpoints.SchDoc	Size: C
Engineer: Rahul Kulkarni		Contact: http://www.ti.com/support	

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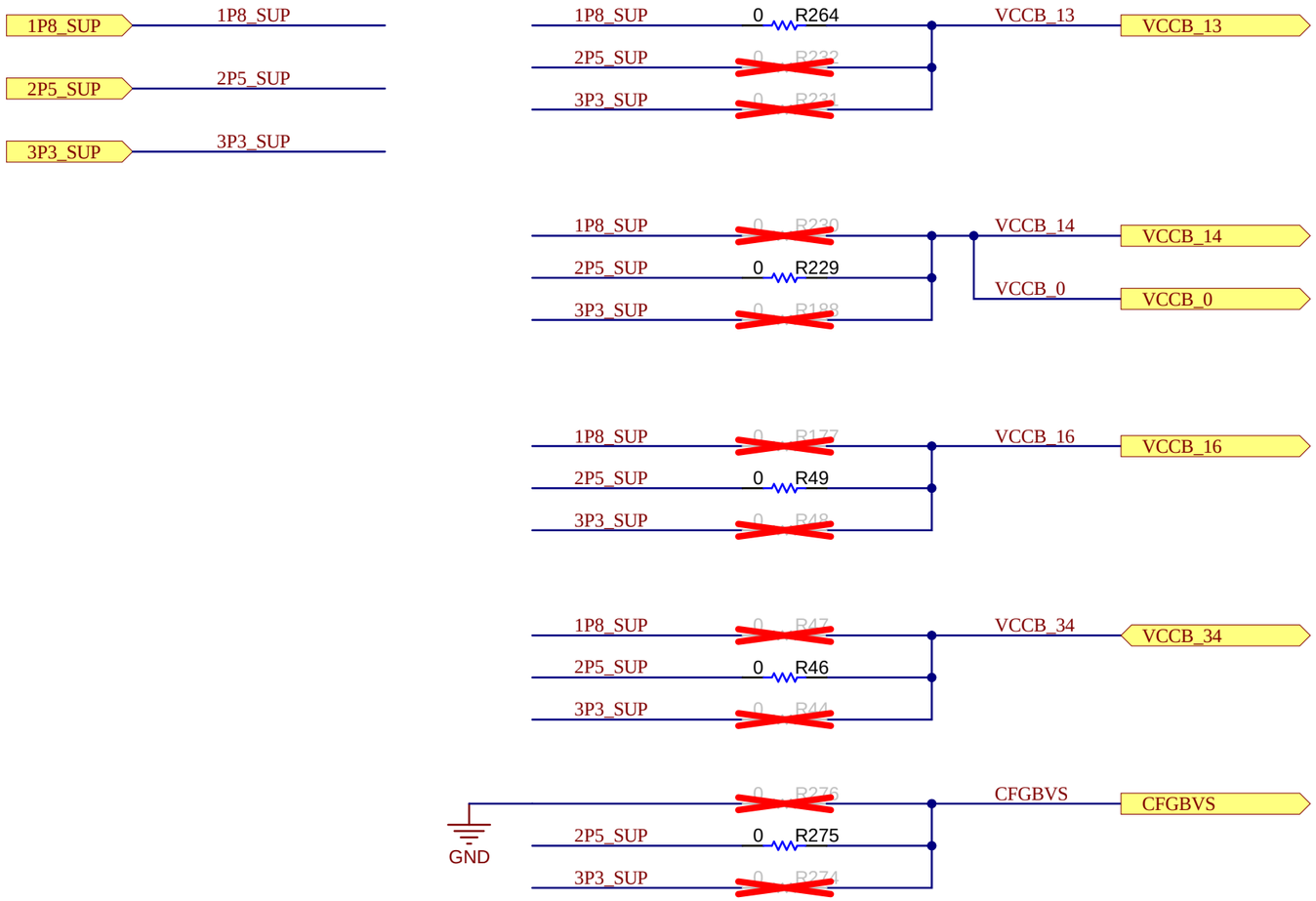

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TID #: N/A		Project Title: DC155C	
Number: DC155C	Rev: 1P0	Sheet Title: FPGA_Bank_Volt_Lvl	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 15 of 18
Drawn By: TI		File: DC155C_FPGA_Bank_Supply.SchDoc	Size: A4
Engineer: Rahul Kulkarni		Contact: http://www.ti.com/support	

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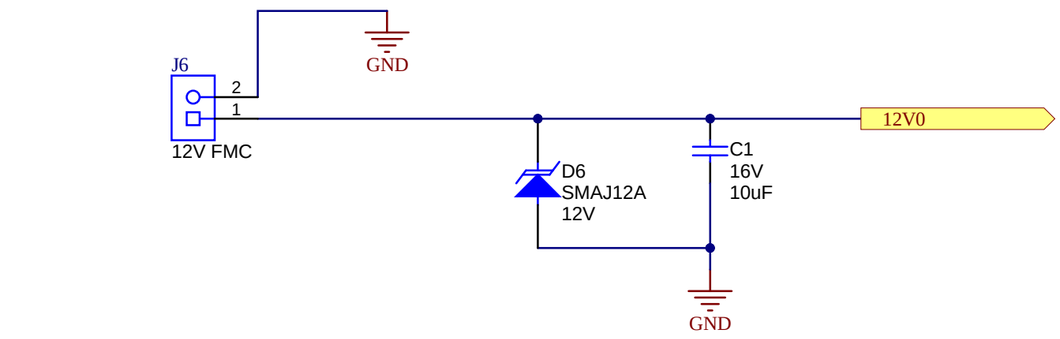

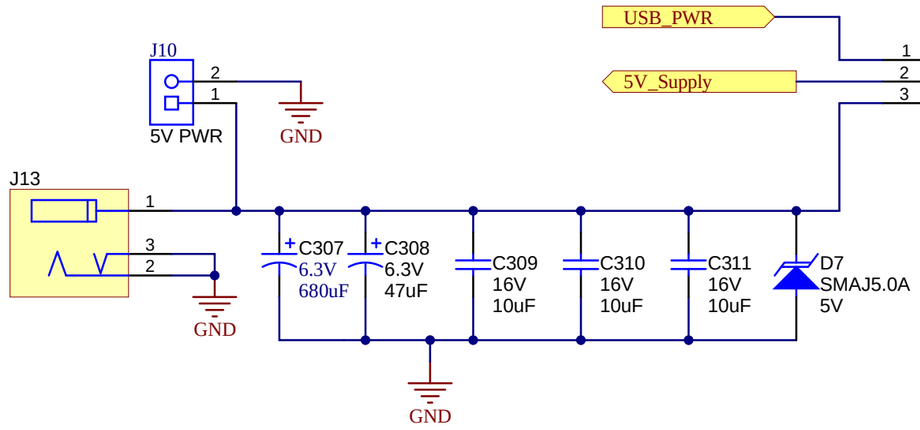

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TID #: N/A		Project Title: DC155C	
Number: DC155C	Rev: 1P0	Sheet Title: Power_Supply	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 17 of 18
Drawn By: TI		File: DC155C_Board_Power_Supply.SchDoc	Size: A4
Engineer: Rahul Kulkarni		Contact: http://www.ti.com/support	

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H1
RM3X8MM 2701

H2
RM3X8MM 2701

H3
RM3X8MM 2701

H4
RM3X8MM 2701

H5
1893

H6
1893

H7
1893

H8
1893

FID1 FID2 FID3 FID4 FID5 FID6

PCB Number: DC155C
PCB Rev: 1P0

PCB
LOGO
Texas Instruments

CE Mark

PCB
LOGO
FCC disclaimer

PCB
LOGO
WEEE logo

SH-J1
881545-2

SH-J2
881545-2

LOGO6

CAUTION HOT SURFACE

ZZ1
Label Assembly Note
This Assembly Note is for PCB labels only

Orderable: TSWDC155BEVM	Designed for: Public Release	Mod. Date: 3/2/2023
TID #: N/A	Project Title: DC155C	
Number: DC155C Rev: 1P0	Sheet Title: Hard Ware	
SVN Rev: Not in version control	Assembly Variant: 001	Sheet: 18 of 18
Drawn By: TI	File: DC155C_Hardware.SchDoc	Size: B
Engineer: Rahul Kulkarni	Contact: http://www.ti.com/support	

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