Schematic Review

1. The DDC needs to have a voltage reference of +4.096V. Please use REF3040 as recommended in the datasheet with the appropriate buffering. The REF3025 used is a fix voltage reference of +2.5V and is not the correct voltage reference.
2. There should be placeholders in different locations for several AGND to DGND shorts connection in the design, either with zero ohms resistor or a ferrite bead, for fine tuning and noise optimization. Please refer to datasheet Figure 36 for reference and guide.
3. There is probably no need to have 10uF on every IC on the design.
4. The buffers (74LVC245AD) are probably not needed if the CPLD controller is placed close to the DDC. A place holder for the buffer can be added if there is a concern. The buffer can be bypassed if it proves that the buffer is not needed. This will save the BOM cost.
5. If there is a jumper option to connect the output of one DDC (DOUT1) as the input for a neighboring DDC (DIN0), then it may be useful to have the option to connect DIN0 to ground (in case it is not connected to DOUT1).
6. The PD diodes connection to the DDC channel inputs can be optimized in the schematic and layout to minimize cross trace and to reduce the number of PCB layers.
7. In the most sensitive gain settings, the parasitic capacitance of the input traces matters, so, if shielding is used (which may be needed on that environment to reduce interference) then a thicker board can be used and the ground layers can be placed further from the signal layers.
8. Typically, the photodiode (PD) cathodes must be connected to ground. So there is no need to place any capacitors to GND on the PD cathodes unless the plan is to apply a negative voltage to the PD cathodes. In such a configuration, check with TI for further support.

Layout Review

1. Option to have the chassis either connected to AGND or DGND with short jumper or have it totally isolated.
2. It is good to have no overlap of digital and analog at all layers.
3. Increase the number of short jumpers between AGND and DGND. Distribute them throughout the board to be able to optimize the design with the right short position later.
4. Make sure the electronics is shielded from direct and scatter x-rays.