**Download and Extract the Design files**

1. Download and extract the design files from the following link:

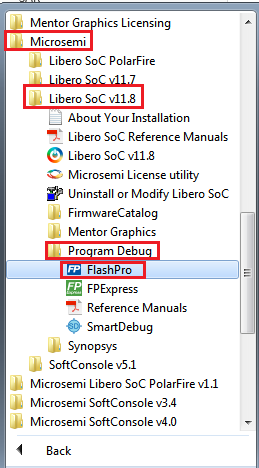
<ftp://ftp.actel.com/outgoing/RTG4_ADC12DJ3200.rar>

1. Extract this file to a local drive.

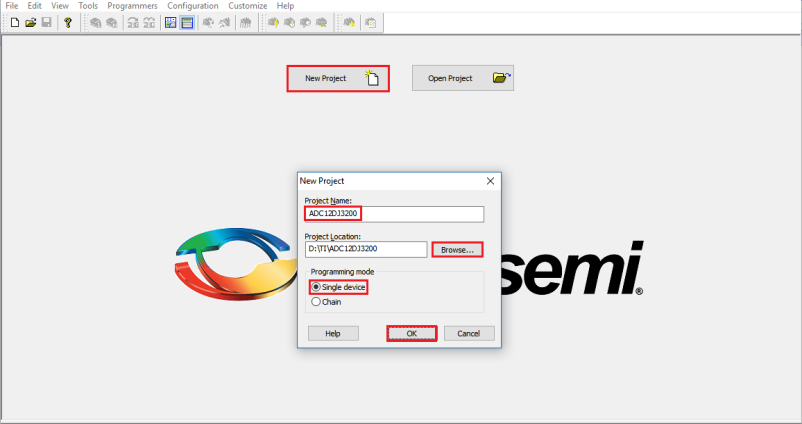
**Programing using Flash pro Software**

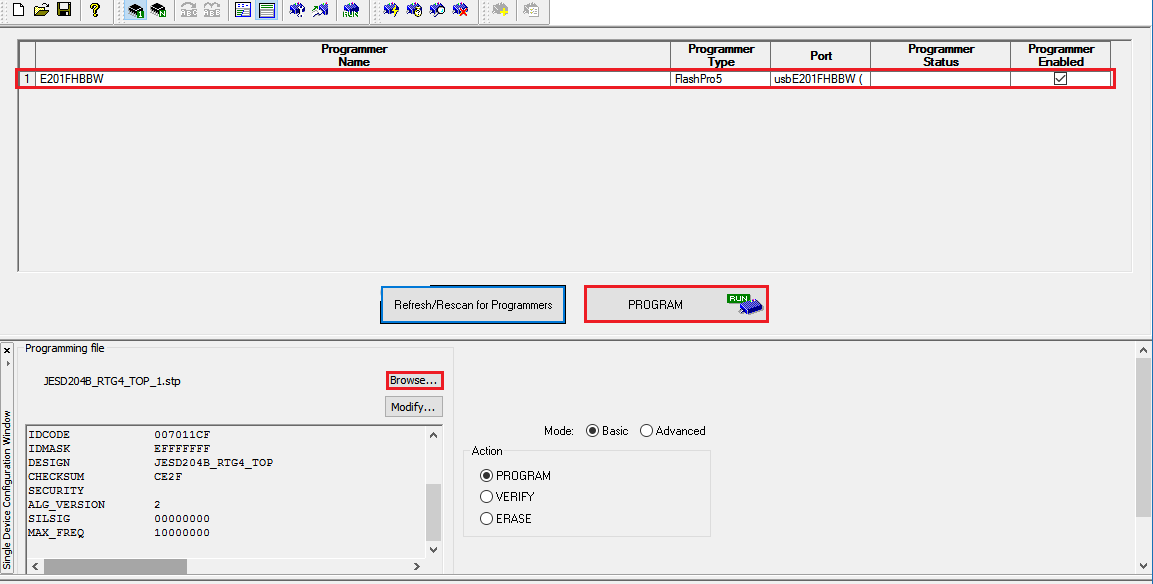
1. Launch the FlashPro software.

Go to Start > Programs > Microsemi > Libero SoC v11.8 > Program Debug >FlashPro

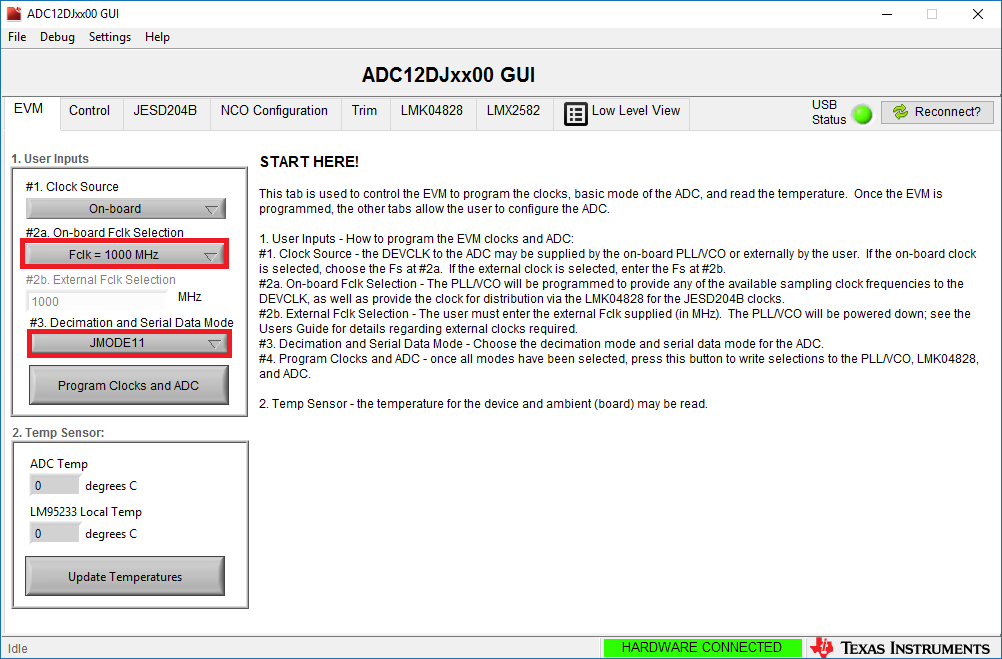
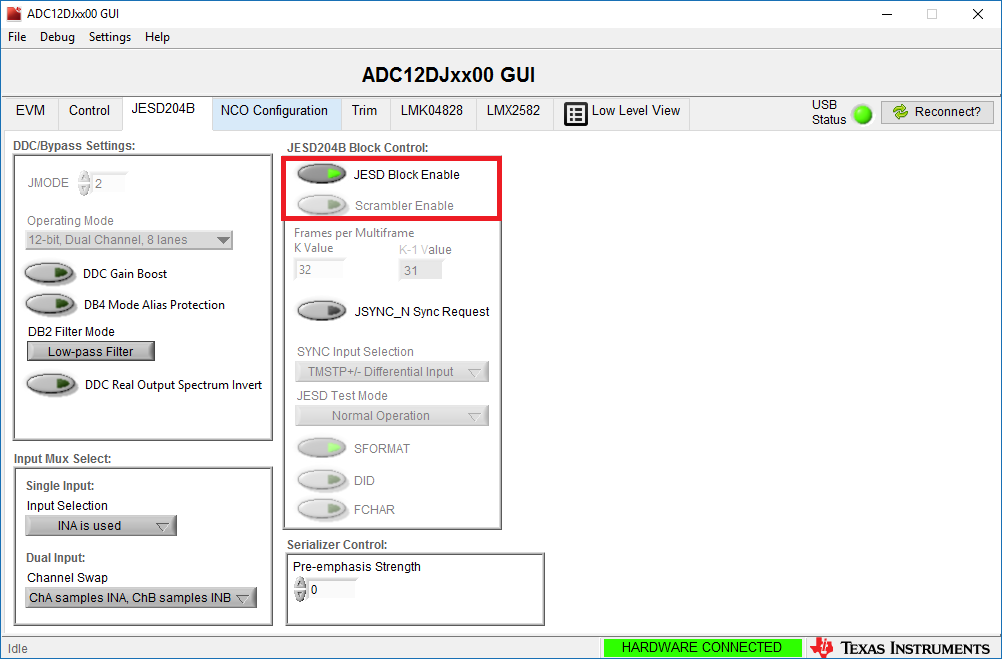
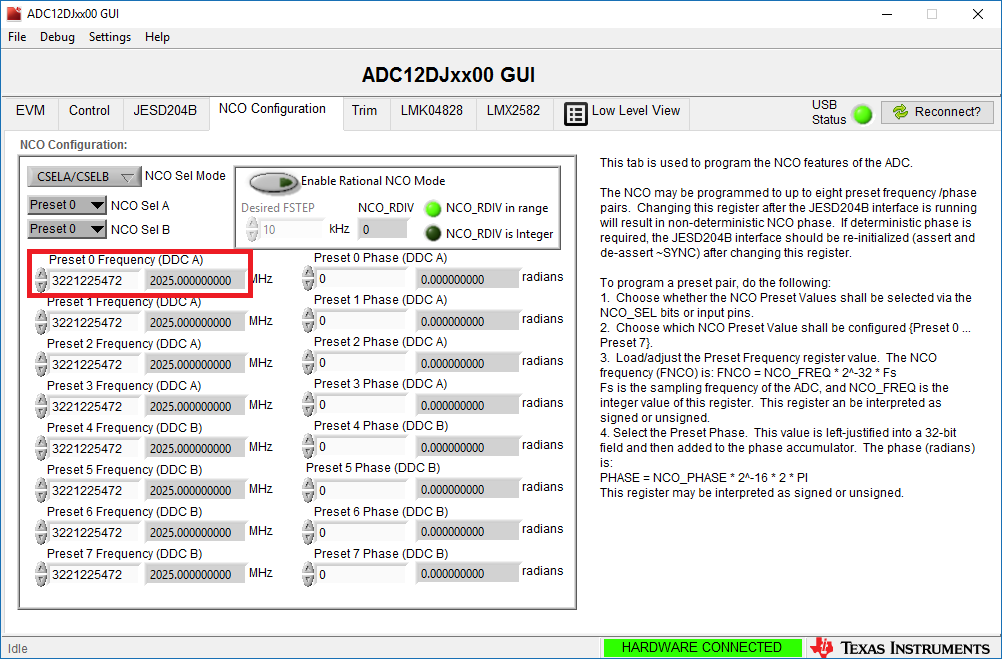
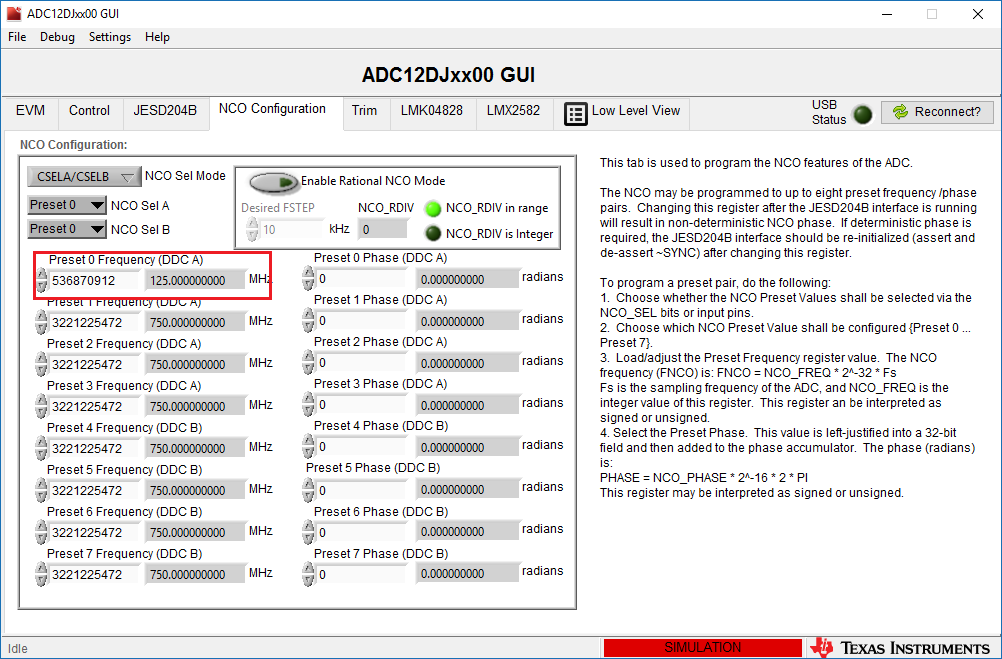
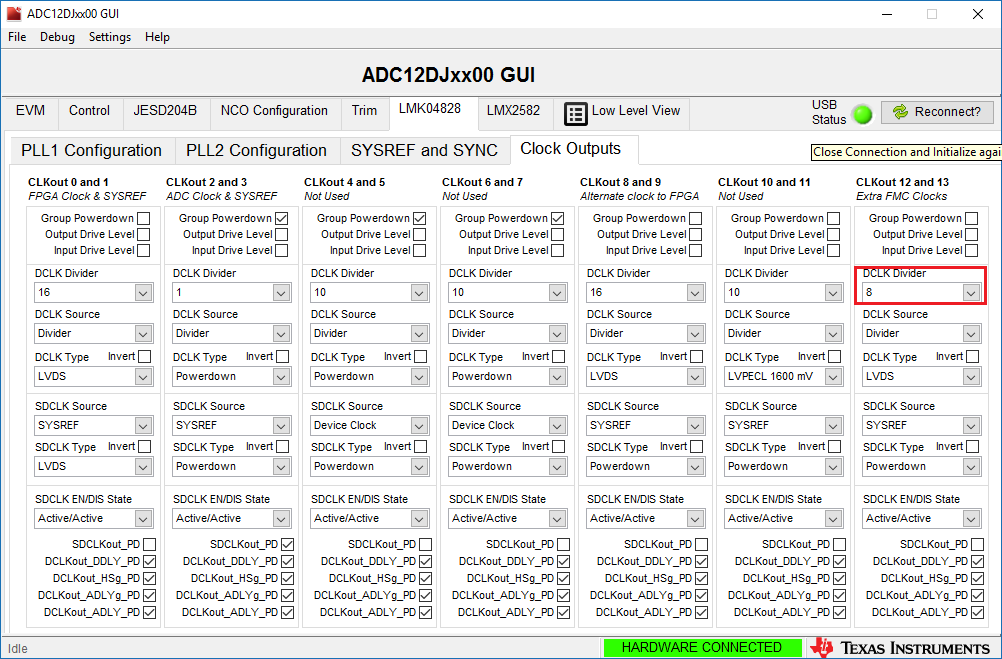


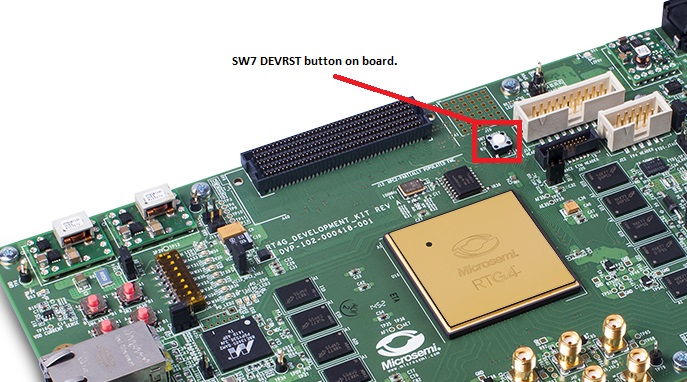
1. Click New Project, In the New Project window, enter the project name.
2. Click Browse and navigate to the location where the project is required to be saved.
3. Select Single device as the Programming mode.
4. Click OK to save the project.



1. Click Configure Device. (? Don’t see this step in video ?)
2. Click Browse, navigate to ***RTG4\_ADC12DJ3200\Programing\_file\JESD204B\_RTG4.stp***
3. Click run program action button to program the RTG4 FPGA.

**Configuring ADC12DJ3200**

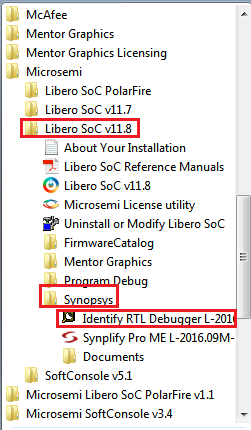
1. Open ADC12DJ3200 GUI
2. Configure this GUI as shown in the following Figures.
3. ****Configuring Clock and Data mode. (click Program Clocks and ADC after selecting 1000M and JMODE11)
4. ****Configuring JESD204B. (Matt’s comments – turn off JESD block enable, turn off scrambler, than turn back on JESD block enable) (this step is not shown in the video)
5. ****Configuring NCO
6. **** Configuring LMK0428
7. Reset the board once programing and ADC configuration is completed by pressing SW7 DEVRST button on board.

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**Debugging using Identify**

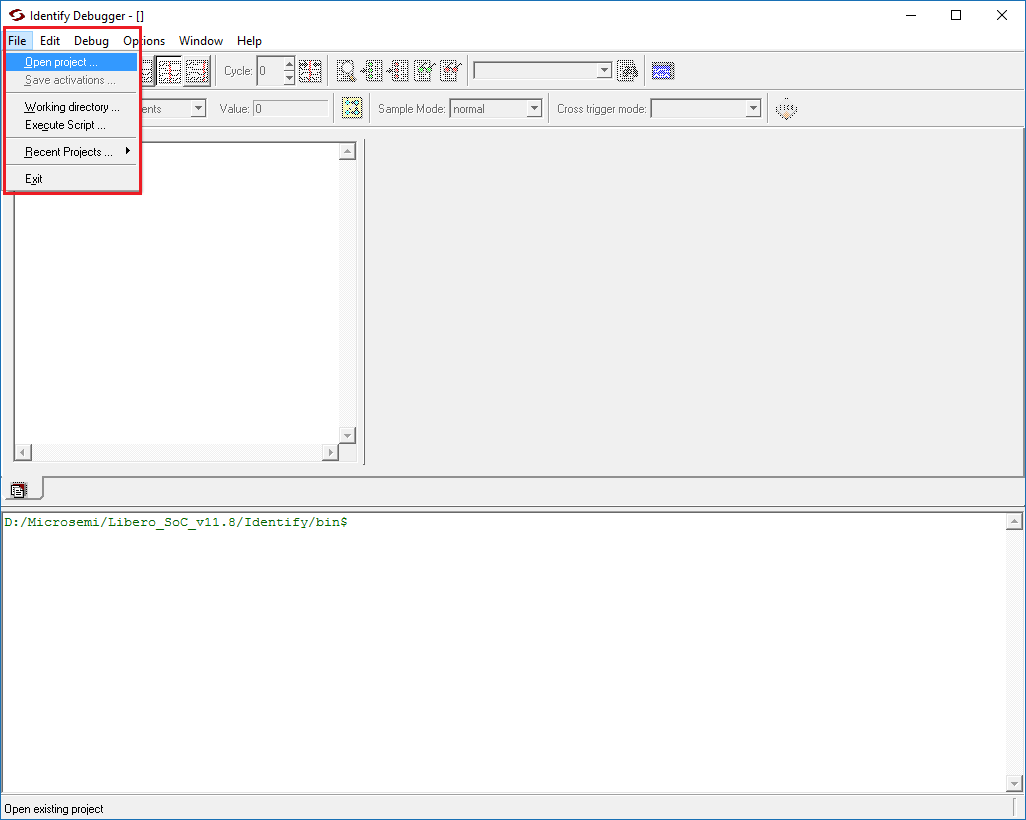
1. Open Identify pro software.

Go to Start > Programs > Microsemi >Synopsys>Identify RTL debugger

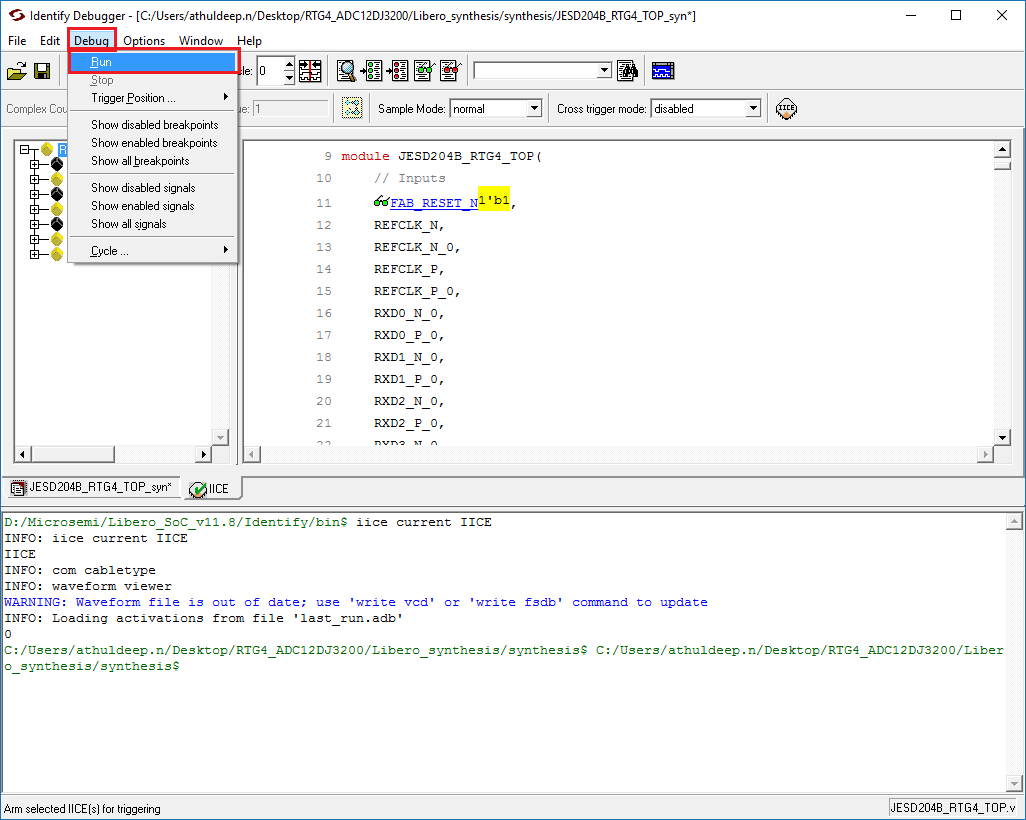


1. Open the identify project, navigate to

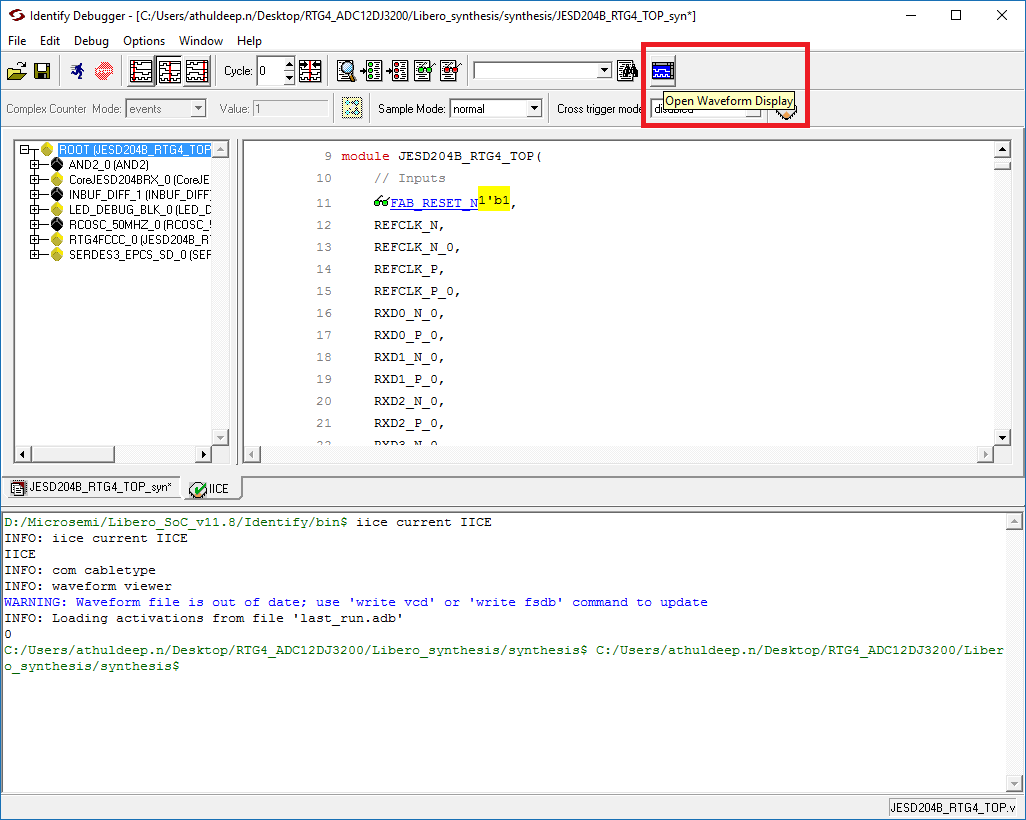
***RTG4\_ADC12DJ3200\Libero\_synthesis\synthesis\JESD204B\_RTG4\_TOP\_syn.prj*** as shown in Figure.



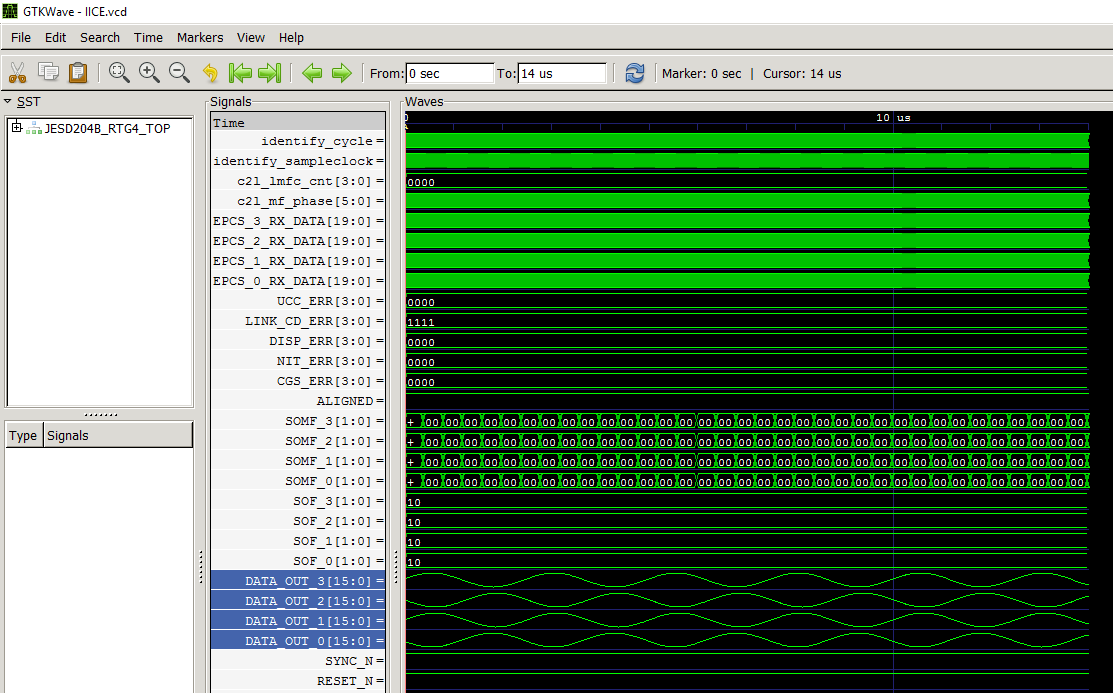
1. Click Debug button and select Run as shown in figure to start capturing samples. (Matt’s comments – you have to hit Stop before you can look at data)



1. Click Open waveform Display button to see the captured data as shown in figure.



1. Following figure shows the final captured samples**. (Matt’s comments – select the DATA\_OUT, right click and ???...... see video)**

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**Useful links:**

* RTG4: <https://www.microsemi.com/products/fpga-soc/radtolerant-fpgas/rtg4#documents>
* Identify: <https://www.microsemi.com/products/fpga-soc/design-resources/programming/identify-me-downloads#documents>
* Libero: https://www.microsemi.com/products/fpga-soc/design-resources/design-software/libero-soc