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Research on a high-precision and high-resolution seismic wave signal acquisition system

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Abstract-In oil and gas exploration, high-resolution seismic acquisition is an important research content of seismic exploration methods. In order to improve the accuracy and high resolution of the seismic wave acquisition system, a seismic wave signal acquisition system based on the 32-bit high-resolution analog-to-digital converter ADS1282 is designed in cooperation with a high-anti-interference and high-resolution piezoelectric geophone, Improve the resolution of seismic wave signal acquisition from the two aspects of seismic wave pickup and analog-to-digital conversion. The system chooses the high-performance, ultra-low power consumption Microcontroller MSP430F149 as the control core of the acquisition system, which effectively reduces system power consumption. System debugging results show that the collected data of ADS1282 is stable to 24 bits, and the consistency is good.

1. Introduction

Seismic wave exploration is one of the most commonly used methods for oil and gas energy exploration. The pickup and acquisition of seismic wave data directly affects the accuracy of oil and gas energy exploration. At present, the existing oil and gas exploration has turned to deeper and thinner reservoirs. How to improve the resolution and accuracy of seismic wave exploration has always been an important research direction for scholars. Commonly used seismic wave detection is a moving coil velocity detector that uses electromagnetic principles and a 24-bit resolution analog-to-digital converter, which is susceptible to interference from external magnetic fields, and has low data fidelity and low resolution.

In order to improve the resolution and accuracy of the seismic wave acquisition system to meet the requirements of oil and gas exploration at this stage, this paper designs a high-sensitivity seismic wave signal with a piezoelectric accelerometer and a 32-bit resolution Σ - \triangle analog-to-digital converter. The acquisition system, and the system is integrated with the detector, shortens the transmission path to the analog signal, and reduces the interference of external noise on the low-frequency seismic analog signal. The system uses the ultra-low power consumption microcontroller MSP430F149 as the main control to reduce the power consumption of the system and meet the requirements of the seismic wave detection environment for system power consumption.

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2. Mechanism of piezoelectric accelerometer

The piezoelectric accelerometer reflects the ground vibration signal through the change of the charge amount of the upper and lower plates of the piezoelectric stack^[1]. A schematic diagram of the working structure of a piezoelectric accelerometer is shown in Figure 1. It is composed of a mechanical casing, a piezoelectric ceramic laminate, and a mass. When a seismic wave signal is received, the output charge is:

$$\mathbf{Q} = \mathbf{d}_{33} M a \tag{1}$$

The d33 is the strain coefficient of piezoelectric ceramics, M is the mass of the mass, and a is the vibration acceleration. It can be seen that Q is proportional to d33 and M, and acceleration can be obtained by measuring the amount of charge.

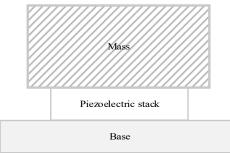


Figure 1 Schematic diagram of the working structure of a piezoelectric accelerometer

Compared with the performance of the traditional seismic wave detection device, the laminated structure of the piezoelectric ceramic sheet greatly improves the sensitivity of the detector signal. The internal structure of the piezoelectric acceleration detector is a direct rigid connection without springs and coils, and there is no Relative displacement and deformation, so the piezoelectric acceleration detector has better signal fidelity, and there is no false frequency and harmonic distortion components[2-3]. Select the digital detector I/O System Four of the American I/O company and the piezoelectric acceleration detector, and the piezoelectric as the American I/O company Digital detector, the figure b shows a piezoelectric acceleration detector.

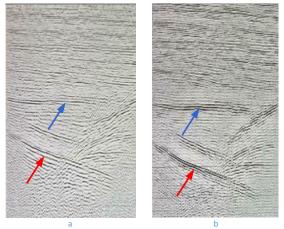


Figure 2 The effect diagram of the performance comparison of the detector

Comparing the line density at the red arrow in the above figure, the b figure is obviously richer. At the same time, the blue arrow indicates the area, and the fault in figure b is obvious. Therefore, it can be inferred that the signal information detected by the piezoelectric acceleration detector is richer, and the advantages of resolution and signal-to-noise ratio are more obvious.

3. High-sensitivity seismic wave signal acquisition system hardware design

In order to realize the acquisition of seismic wave signals, the system uses the microcontroller MSP430F149 chip as the main control of the system. The high-sensitivity seismic wave signal system circuit is mainly composed of piezoelectric acceleration detector, MSP430F149 main control module, ADC conversion module, storage module, trigger circuit, communication interface, analog power supply and digital power supply [4], the overall structure of the system is shown in Figure 3 Show.

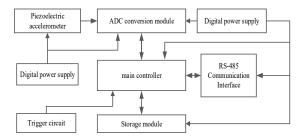


Figure 3 The overall structure of the system

The seismic wave signal of the ground vibration is picked up by the piezoelectric acceleration detector, the mechanical signal of the vibration is converted into an electrical signal, and the signal is amplified and filtered. The ADC analog-to-digital converter converts the analog seismic wave signal into a digital signal for processing, storage and transmission by the subsequent circuit. The system uses an external memory to store digital signals, and transmits data through the communication interface circuit when data communication is required. In order to improve the signal ratio of the system and reduce the interference of switching power supply noise to the analog signal, the digital and analog power supplies are used to supply power separately.

3.1. MSP430F149 microcontroller peripheral circuit

The MSP430F149 microcontroller is a 16-bit controller with ultra-low power consumption[5-6], which meets the system's requirements for low power consumption. The signal acquisition system takes the microcontroller MSP430F149 as the core, which controls the peripheral functional circuits to coordinate operations and realize data acquisition. The main controller communicates with the ADC module through the SPI interface, reads the data converted by the ADC, further digitally processes the data, and stores and uploads the data through the communication interface. The peripheral circuit of the MSP430F149 chip used by the system is shown in Figure 4.

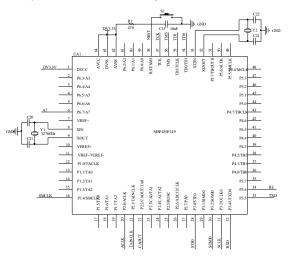


Figure 4 MSP430F149 peripheral circuit diagram

3.2. ADS1282 peripheral circuit

ADS1282 converts seismic wave signal into digital quantity. In order to improve the quality of the signal, the input signal of ADS1282 is adjusted to filter the high-frequency common-mode interference in the line and the differential mode noise between the lines. The input signal is limited through the overcurrent and over-voltage protection circuit, and it is input to the differential input end of ADS1282. R4 and R5 in the circuit form a current loop to obtain differential voltage signals.Resistance R3, R6 and capacitance C22 and C24 constitute a low pass filter to filter out the high frequency common mode interference noise in the circuit. Resistance R3, R7 and capacitor C23 constitute differential mode filter. Capacitance value of C23 capacitor is more than 10 times of C22 and C24, effectively solving common mode errors caused by mismatch of C22 and C24.Schottky diode D1, D2, D3 and D4 are used in the circuit to limit the input signal to prevent the damage of ADS1282 chip caused by too high or too low input signal [5].The front-end processing circuit of ADS1282 is shown in Figure 5.

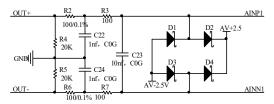


Figure 5 ADS1282 front-end processing circuit

The reference voltage is an important part of the analog-to-digital conversion chip, and the accuracy of the reference voltage directly affects the accuracy of the analog-to-digital conversion. The system uses REF02 voltage chip, the input voltage range is 7V-40V, and the output high-precision reference voltage +5V, the error accuracy reaches 0.3% (MAX). The ADS1282 reference voltage circuit diagram is shown in Figure 6.

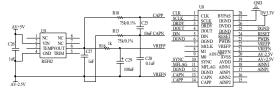


Figure 6 ADS1282 reference voltage circuit diagram

3.3. ADS1282 analog-to-digital converter and MSP430F149 main controller interface circuit

MSP430F149 is an ultra-low-power 16-bit processor produced by Texas Instruments, with 5 low-power modes to choose from. The power supply voltage range is low, between 1.8V and 3.6V, and the current consumption is only 280uA under the condition of 2.2V and 1MHZ clock frequency in the active mode; the current consumption in the general standby mode is 1.6uA; the current consumption in the offline mode is only There is 0.1uA [8-9], which is widely used in conditions that require harsh power consumption. MSP430F149 has two general-purpose serial synchronous or asynchronous communication microcontroller configurations, one is used for communication with PC for debugging, the other is used for data transmission with ADS1282. The system transmits the data converted by ADS1282 to the controller through the SPI1 channel, and the controller simply processes the data and stores it and sends it to the acquisition station through the RS485 bus. The circuit diagram of the controller part requires an external clock circuit and a reset circuit.

The controller communicates with the ADS1282 analog-to-digital conversion chip through the SPI interface, which is implemented by three-wire SCLK, MOSI, and MISO. During communication, data is read into ADS1282 on the rising edge of SCLK, and data is output on the falling edge of SCLK. An external 4.096MHz active crystal oscillator is used to provide the master clock for the ADS1282 chip, and the SCLK frequency requirement range of the SPI bus is fclk/16 ~ fclk/2. During communication, the microcontroller provides the clock to implement operations such as the configuration of the

ADS1282's internal registers and data readout. In order to remove the interference from the digital noise on the port, a 47Ω buffer resistor is inserted between the interfaces to reduce the interference, and the resistor is placed close to the signal sending end when wiring. The port wiring is shown in Figure 7.

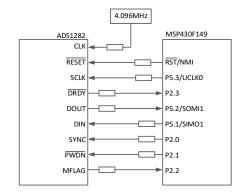


Figure 7 ADS1282 and MSP430F149 wiring diagram

4. Software design

The ADS1282 analog-to-digital conversion chip connects with an external active crystal oscillator, the main clock frequency is fclk = 4.096MHz, and the SPI bus clock is required to be in the range of fclk/16 ~ fclk/2. The microcontroller MSP430F149 is connected to an 8MHz crystal oscillator to provide an external clock. Because the microcontroller provides a serial clock during communication, in order to make the SCLK of the SPI bus meet the demand, the main clock must be divided. The software design must first configure the SPI protocol, such as SPI mode, baud rate,number of data bits, and number of stop bits to ensure the correctness of data transmission. The serial interface must be reset before using serial communication to prevent the power-on sequence from affecting SPI communication. When reading or writing registers, turn off the data continuous mode first. ADS1282 has eleven registers with address 00-0A. Table 1 shows the registers CONFIG0 and CONFIG1 that are generally used in ADS1282 configuration.

| Address | Register | Reset | BIT7 | BIT6 | BIT5 | BIT4 | BIT3 | BIT2 | BIT1 | BIT0 |
|---------|----------|-------|------|------|------|------|------|------|--------|--------|
| 01h | CONFIG0 | 52 | SYNC | 1 | DR2 | DR1 | DR0 | PHS | FILTR1 | FILTR0 |
| 02h | CONFIG1 | 08 | 0 | MUX2 | MUX1 | MUX0 | СНОР | PGA2 | PGA1 | PGA0 |

 Table 1
 DS1282 parameter configuration register

When configuring the register, write the register reset instruction 0X11 first, and then write the configuration parameters into the two registers. After the configuration is completed, open the data continuous reading mode. The system ADS1282 is configured in pulse synchronization mode, the conversion rate is 4000SPS, the FIR+SIN digital filter mode is adopted, the working mode is normal mode, the input channel selects channel 1, the programmable gain amplifier multiple is 1, so the parameter of CONFIG0 is 0X62, The configuration parameter of CONFIG1 is 0X18. The program flow chart is shown as in Figure 8.

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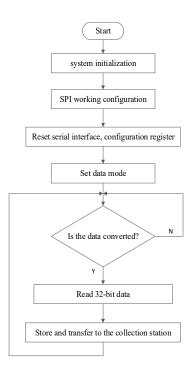


Figure 8 Program flow chart

5. System testing and verification

After completing the hardware and software design of the high-sensitivity seismic wave signal acquisition system, the acquisition capability of the system is tested. Through the input signal of the given acquisition system, the error between the output signal quantity of the acquisition system and the given input signal quantity is compared to calculate the acquisition accuracy of the system. The signal input adopts a precision voltage source as the input of the system's voltage stabilization source, and respectively take signals of different amplitudes, and compare and detect the output digital signals. Table 2 below shows the signal detection error and accuracy.

| Table 2 Signal detection error and accuracy | | | | | | |
|--|-------------------|----------------------|--------------|-----------|--|--|
| Serial num | Input voltage (V) | Test value (V) | Error (V) | Precision | | |
| 1 | 0.200574 | 0.200581 | 0.000007 | 0.00349% | | |
| 2 | 0.400283 | 0.400292 | 0.000009 | 0.002248% | | |
| 3 | 0.500348 | 0.500349 | 0.000001 | 0.0002% | | |
| 4 | 0.600326 | 0.600325 | 0.000001 | 0.000167% | | |
| 5 | 0.700273 | 0.700284 | 0.000011 | 0.001571% | | |
| 6 | 0.800325 | 0.800333 | 0.000008 | 0.001% | | |
| 7 | 0.900249 | 0.900254 | 0.000005 | 0.000555% | | |
| 8 | 1.000503 | 1.000509 | 0.000006 | 0.0006% | | |
| 9 | 1.200578 | 1.200579 | 0.000001 | 0.000083% | | |
| 10 | 1.400427 | 1.400431 | 0.000004 | 0.000286% | | |
| 11 | 1.600336 | 1.60033 | 0.000006 | 0.000375% | | |
| 12 | 1.800344 | 1.800346 | 0.000002 | 0.000111% | | |

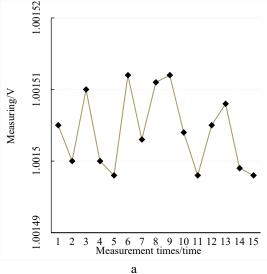
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|--------|--------------|-------------------------------------|
|--------|--------------|-------------------------------------|

| 13 | 2.000253 | 2.000246 | 0.000007 | 0.00035% |
|----|----------|----------|----------|-----------|
| 14 | 2.200372 | 2.200379 | 0.000007 | 0.000318% |
| 15 | 2.400581 | 2.400585 | 0.000004 | 0.000167% |

It can be seen from Table 2 that the acquisition accuracy of the system is better, and the accuracy can reach within 0.004%. In order to test the stability of the data collected by the system, three measurement data were recorded for five groups of input signals. When comparing the same input signal, the number of stable and non-flickering digits in the 32-bit data volume of the acquisition system was recorded. Table 3 shows the test of the number of stable bits of the collected signal.

| Serial num | Input voltage (V) | The first measurement (0X) | The second measurement (0X) | The third measurement (0X) | Stable digits |
|---------------|----------------------|-------------------------------|--------------------------------|-------------------------------|------------------|
| 1 | 0.500348 | 199E1931 | 199E1950 | 199E19CC | 24bit |
| 2 | 0.800325 | 28F9E162 | 28F9E1B8 | 28F9E130 | 24bit |
| 3 | 1.200578 | 3D782B3D | 3D782BF9 | 3D782B49 | 24bit |
| 4 | 1.800344 | 5C2D9C68 | 5C2D9C79 | 5C2D9C22 | 25bit |
| 5 | 2.400581 | 7AE8DD17 | 7AE8DDEF | 7AE8DD69 | 24bit |

It can be seen from the five sets of measurement data in the above table that the signal data detected by the system is basically stable at 24 bits. Detect the same input value signal multiple times through the acquisition board, record the data, and compare the deviation of the multiple measured data. The left picture of Fig 10 shows the data distribution of the voltage signal of the input signal 1.001503v detected by the acquisition board 15 times. The right figure draws the error distribution range diagram by calculating the absolute value of the error between the collected data and the input signal. It can be clearly observed that the absolute value of the acquisition error of the acquisition board is less than 0.01mV.



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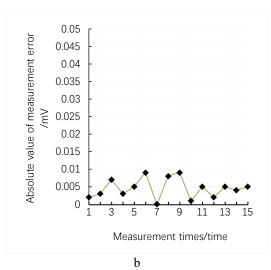


Figure 9 Data distribution and error range diagram

6. Conclusion

This article mainly introduces the high-sensitivity seismic wave signal acquisition system from the mechanism of piezoelectric accelerometer, acquisition system hardware and software. This system adopts the combination of piezoelectric accelerometer and ADS1282, using the advantages of piezoelectric accelerometer with high sensitivity and high anti-interference and ADS1282's highly integrated 32-bit resolution performance to collect single-channel seismic signals.

The system collects the signal generated by the seismic source through the piezoelectric accelerometer, after processing by the front-end circuit, the analog-to-digital conversion, the microcontroller integrates, stores and sends the converted data to the collection station, which achieves the system design requirements and has high precision The advantages of high resolution, low power consumption and simple structure. Through experimental tests, the system's acquisition accuracy can reach 0.004%, the data output digits can reach 24 stable, and the acquisition error range is within 0.01mV. The development of this seismic wave acquisition system provides a new acquisition system with high resolution, ultra-low power consumption and simple structure for exploration operations.

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