AFE79xx Quad-Channel RF Transceiver With Feedback Path

1 Features

- Quad RF sampling 12-GSPS transmit DACs
- Quad RF sampling 3-GSPS receive ADCs
- Dual RF sampling 3-GSPS feedback ADCs (AFE792x only)
- Maximum RF signal bandwidth:
  - TX/FB: 1200 MHz (AFE7920/88) or 400 MHz (AFE7921/89)
  - RX: 600 MHz (AFE7920/88) or 400 MHz (AFE7921/89)
- Digital Step Attenuators (DSA):
  - TX: 40 dB range, 1-dB analog and 0.125-dB digital steps
  - RX: 25 dB range, 0.5-dB steps
  - FB: 25 dB range, 0.5-dB steps
- Single or dual-band DUC/DDCs (AFE7920/88 only) for TX and RX
- Dual NCOs for fast frequency switching
- Supports TDD operation with fast switching between TX and RX
- Internal PLL/VCO to generate DAC/ADC clocks
- Optional external CLK at DAC or ADC rate
- SerDes data interface:
  - JESD204B and JESD204C compliant
  - 8 SerDes transceivers up to 29.5 Gbps
  - 8b/10b and 64b/66b encoding
  - 12-bit, 16-bit, 24-bit, and 32-bit resolution
  - Subclass 1 multi-device synchronization
- Package: 17-mm × 17-mm FCBGA, 0.8-mm pitch

2 Applications

- Macro remote radio unit (RRU)
- Active antenna system mMIMO (AAS)
- Small cell base station
- Repeater
- Distributed Antenna Systems (DAS)

3 Description

The AFE79xx is a family of high performance, wide bandwidth multi-channel transceivers, integrating four RF sampling transmitter chains, four RF sampling receiver chains, and up to two RF sampling digitizing auxiliary chains (feedback paths). The high dynamic range of the transmitter and receiver chains allows the device to generate and receive 3G, 4G, and 5G signals from wireless base stations, while the wide bandwidth capability of the AFE79xx devices is designed for multi-band 4G and 5G base stations.

Each receiver chain includes a 25-dB range DSA (Digital Step Attenuator), followed by a 3-GSPS ADC (analog-to-digital converter). Each receiver channel has an analog peak power detector and various digital power detectors to assist an external or internal autonomous automatic gain controller, and RF overload detectors for device reliability protection. The single or dual digital down converters (DDC) provide up to 600 MHz of combined signal BW. In TDD mode, the receiver channel can be configured to dynamically switch between the traffic receiver (TDD RX) and wideband feedback receiver (TDD FB), with the capability of re-using the same analog input for both purposes.

Each transmitter chain includes a single or dual digital up converters (DUCs) supporting up to 1200-MHz combined signal bandwidth. The output of the DUCs drives a 12-GSPS DAC (digital to analog converter) with a mixed mode output option to enhance 2nd or 3rd Nyquist operation. The DAC output includes a variable gain amplifier (TX DSA) with 40-dB range and 1-dB analog and 0.125-dB digital steps.

The feedback path includes an 25-dB range DSA driving a 3-GSPS RF sampling ADC, followed by a DDC with up to 1200-MHz bandwidth.

Device Information[1]

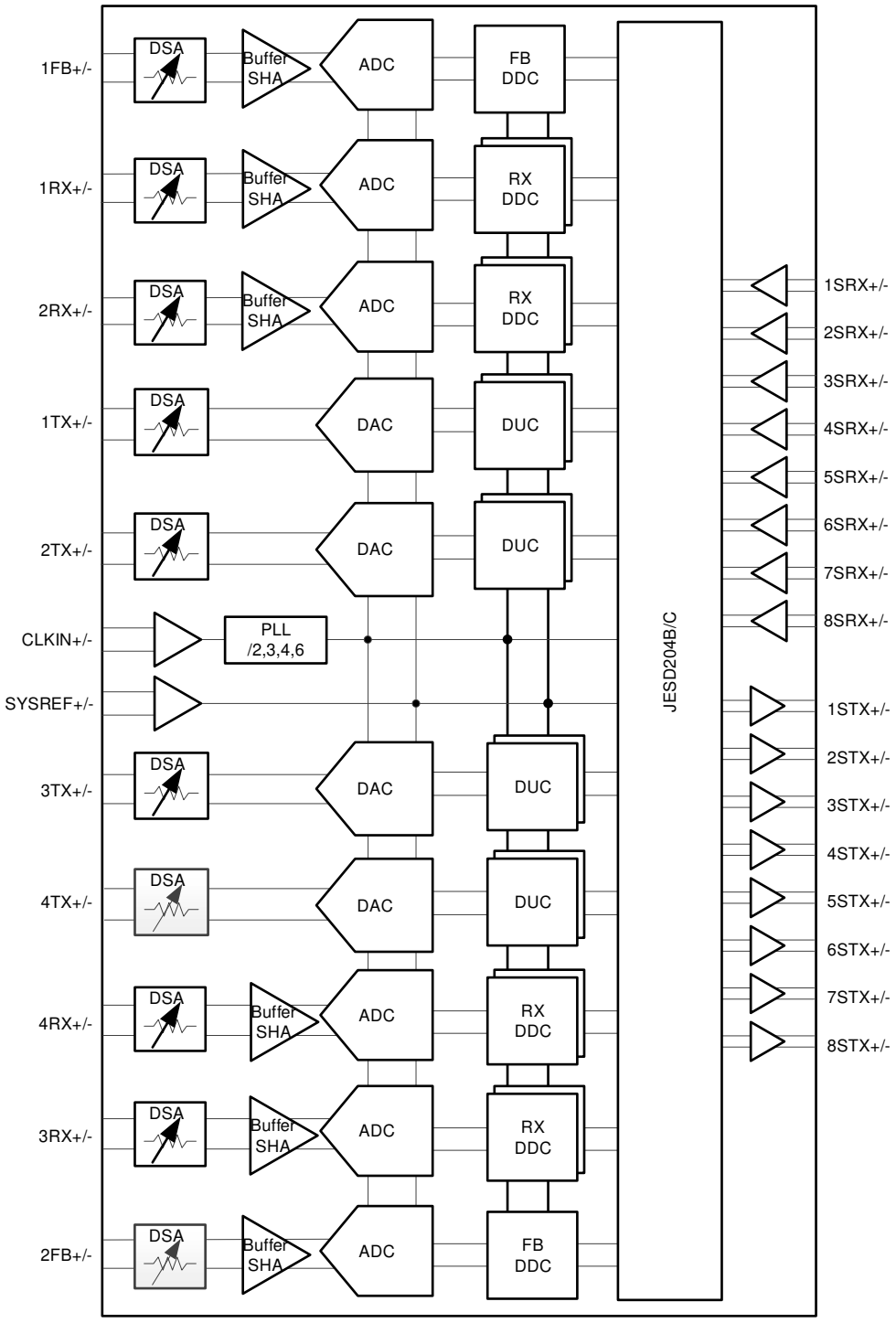
PART NUMBER	PACKAGE	BODY SIZE
AFE7989	FC-BGA	17.00 mm × 17.00 mm
AFE7920	FC-BGA	17.00 mm × 17.00 mm
AFE7988	FC-BGA	17.00 mm × 17.00 mm
AFE7921[2]	FC-BGA	17.00 mm × 17.00 mm

(1) For more information, see *Mechanical, Packaging, and Orderable Information*.

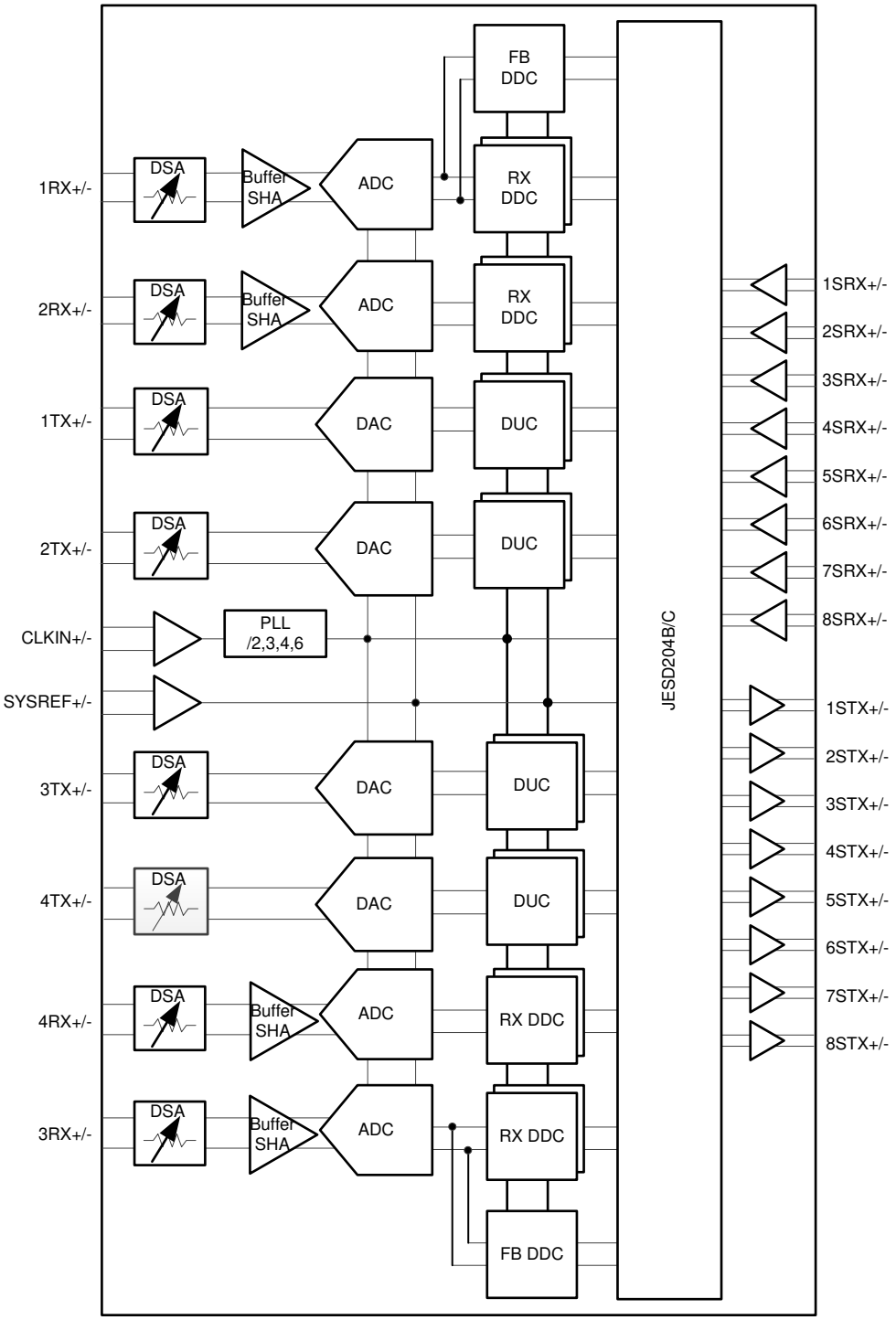
(2) Advanced Information

4 Functional Block Diagram

4.1 AFE7920/21 Functional Block Diagram



4.2 AFE7988/89 Functional Block Diagram



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5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (February 2020) to Revision B **Page**

- Changed AFE7988 device status from advanced information to production data ... 1
- Changed $R_{\theta JA}$ from 16.2 to 15.7 ... 16
- Changed $R_{\theta JC(top)}$ from 0.42 to 0.51 ... 16
- Changed $R_{\theta JB}$ from 4.85 to 4.82 ... 16
- Changed Ψ_{JT} from 0.12 to 0.08 ... 16
- Changed Ψ_{JB} from 4.6 to 4.8 ... 16
- Changed the max full scale power at 2600MHz from 2.9dBm to 4.0dBm ... 17
- Changed the max full scale power at 3500MHz from 1.7dBm to 3.9dBm ... 17
- Added ± sign in front of TX DSA step gain and phase accuracy. ... 17
- Added uncalibrated TX DSA step accuracy. ... 17
- Added in-band SFDR with f_{out}=850MHz with f_{DAC}=5898.24MSPS ... 18
- Added in-band SFDR with f_{out}=1800MHz with f_{DAC}=5898.24MSPS ... 18
- Added in-band SFDR with f_{out}=260MHz with f_{DAC}=8847.36MSPS ... 18
- Added in-band SFDR with f_{out}=3500MHz with f_{DAC}=8847.36MSPS ... 18
- Added ± sign in front of RX DSA step gain and phase accuracy. ... 23
- Changed RX IMD3 at 4.9GHz from -71.8 dBFS to -75.9 dBFS. ... 24
- Changed RX SFDR with A_{IN} = -13dBFS and f_{IN} = 3610 MHz from 87dBFS to 90dBFS ... 24
- Changed RX HDn, n>3, with A_{IN} = -13dBFS and f_{IN} = 3610MHz from -85dBc to -90dBc. ... 25
- Added typical currents for power consumption Mode 2a, 2b and 2d. ... 30
- Changed the interpolation factor from 12x to 18x (typo) ... 30

Revision History (continued)

- Added typical currents for power consumption Mode 5a, 5b and 5d. ... 32
- Changed power consumption Mode 5 to Mode 5c and updated the typical currents ... 32
- Added typical currents for power consumption Mode 11a, 11b, 11c and 11d. ... 36
- Added Figure 61, "RX HD2 vs DSA Setting and Temperature at 3.6GHz". ... 50
- Added Figure 65, "RX HD3 vs DSA Setting and Temperature at 3.6GHz". ... 50
- Deleted the duplicated plot of RX Inband SFDR (±200 MHz) vs Input Amplitude and Temperature at 4.9GHz. See Figure 111 ... 55
- Added the note of "measured after HD2 trim" in RX HD2 plots. ... 56
- Added Figure 101, "RX HD2 vs DSA and Temperature at 4.9GHz". ... 56
- Changed Figure 113, "RX Non-HD2/3 vs DSA Setting at 4.9GHz", replacing the duplicated plot of Figure 112with the correct plot. ... 58
- Changed the note of "with 0.9 GHz matching" to "with 0.8 GHz matching" in Figure 126. ... 60
- Added Figure 142, "RX HD2 vs DSA Setting and Temperature at 0.8 GHz" ... 63
- Added Figure 145, "RX HD3 vs DSA Setting and Temperature at 0.8GHz" ... 64
- Changed the note of "with 1.75 GHz matching" to "with 1.8GHz matching" in Figure 167. ... 67
- Changed " 1.75 GHz" to "1.9 GHz" in the caption of Figure 183 - Figure 190 ... 70
- Added the note of "decimated by 24" in Figure 193. ... 72
- Added the note of "A_{out} = -0.5dBFS" in the TX full scale output power plots at 2.6GHz (Figure 199 - Figure 202). ... 73
- Changed the DSA range (x-axis) up to 39dB in Figure 203 - Figure 219, and Figure 221. ... 73
- Changed the TX IMD3 vs tone spacing test condition from -12dBFS each tone to -13dBFS each tone in Figure 222, Figure 316, Figure 364 - Figure 366 and Figure 421. ... 76
- Changed the TX IMD3 vs tone spacing test condition from -7dBFS each tone to -13dBFS each tone in Figure 223, Figure 317, Figure 369 and Figure 422. ... 77
- Added text note of "dither = 1" in Figure 223. ... 77
- Added "dither = 1" in the text note of Figure 224. ... 77
- Changed the DSA range (x-axis) up to 39dB in Figure 233 - Figure 236. ... 78
- Changed the text note of "output power = -13dBFS" to "A_{out} = -1dBFS" in Figure 251. ... 82
- Added the note of "A_{out} = -0.5dBFS" in the TX full scale output power plots at 3.5GHz (Figure 253 - Figure 254). ... 82
- Changed the DSA range (x-axis) up to 39dB in Figure 253 , and Figure 255- Figure 272. ... 82
- Added TX NSD vs DSA setting at 3.5GHz plot, Figure 271 ... 86
- Changed the text note of "Including PCB and cable losses" to "Excluding PCB and cable losses" in Figure 294 - Figure 296 ... 90
- Added the note of "A_{out} = -0.5dBFS" in the TX full scale output power plots at 4.9GHz (Figure 294 - Figure 297). ... 90
- Changed the typo of "2.6GHz" to "4.9GHz" in the caption of Figure 319. ... 94
- Changed the typo of "4.9GHz" to "0.85GHz" in the caption of Figure 348. ... 99
- Changed the typo of "2.6GHz" to "0.85GHz" in the caption of Figure 350. ... 99
- Changed the typos of f_{CENTER} from 2.6GHz to 0.85GHz and matching from 2.6GHz to 0.8GHz in the text note of Figure 365 ... 102
- Changed the note of "f_{DAC} = 8847.36MSPS" in Figure 392to "f_{DAC} = 5898.24MSPS" (typo). ... 106
- Added the note of "A_{out} = -0.5dBFS" for TX full scale output power plots at 1.8GHz (Figure 396 -Figure 402). ... 107
- Changed the typo of "2.6GHz" to "1.8GHz" in the caption of Figure 412. ... 110
- Changed the typo of "1.8GHz" to "1.8425GHz" in the caption of Figure 425. ... 112
- Changed the note of "f_{DAC} = 5898.24MSPS" in Figure 433 - Figure 444 to "f_{DAC} = 8847.36MSPS" (typo). ... 113

Changes from Original (December 2019) to Revision A **Page**

6 Device Comparison Table

DEVICE	# OF TX DUC AND RX DDC BANDS	TX/FB MAX DATA RATE	RX MAX DATA RATE	NUMBER OF FB ADCS
AFE7920	2	1474.56 MSPS (or 2x 737.28 MSPS)	737.28 MSPS (or 2x 368.64 MSPS)	2
AFE7921	1	491.52 MSPS	491.52 MSPS	2
AFE7988	2	1474.56 MSPS (or 2x 737.28 MSPS)	737.28 MSPS (or 2x 368.64 MSPS)	0 (1)
AFE7989	1	491.52 MSPS	491.52 MSPS	0 (1)

(1) For TDD systems with FB time sharing RX ADCs, two additional FB DDC paths are available.

7 Pin Configuration and Functions

AFE7920/21: ABJ Package
400-Pin FCBGA
Top View

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	
20	VDD1P2 TXCLK	2TXOUT+	2TXOUT-	VDD1P2 TXCLK	VDD1P8TX	1TXOUT-	1TXOUT+	VDD1P8TX	VSSTX	VDD1P2 PLLCLK REF	VDD1P8 PLLVCO	VSSTX	VDD1P8TX	3TXOUT+	3TXOUT-	VDD1P8TX	VDD1P2 TXCLK	4TXOUT-	4TXOUT+	VDD1P2 TXCLK	20
19	VSSTXCLK	VSSTX	VSSTX	VSSTXCLK	VSSTX	VSSTX	VSSTX	VSSTX	PLL _LDOUT	SYSREF+	SYSREF-	VSSPLL	VSSTX	VSSTX	VSSTX	VSSTX	VSSTXCLK	VSSTX	VSSTX	VSSTXCLK	19
18	VSSFBCLK	VSSFBCLK	VSSTX	VSSTX	VSSTX	VSSTX	VSSTX	VSSTX	VSSPLL CLKREF	VDD1P2 PLLCLK REF	VDD1P2 PLLCLK REF	VSSPLL CLKREF	VSSTX	VSSTX	VSSTX	VSSTX	VSSTX	VSSTX	VSSFBCLK	VSSFBCLK	18
17	VDD1P8 FBCLK	VSSFB	VSSTX	VDD1P2 TXENC	VSSTXENC	VSSTX	VDD1P8 TXDAC	VDD1P8 TXDAC	VSS PLLRXCML	REFCLK+	REFCLK-	VSS PLLRXCML	VDD1P8 TXDAC	VDD1P8 TXDAC	VSSTX	VSSTXENC	VDD1P2 TXENC	VSSTX	VSSFB	VDD1P8 FBCLK	17
16	1FBIN+	VSSFB	VDD1P8FB	VDD1P2FB	VSSTXENC	GTR_7 _SPIB2SEN	GTR_17 _SPIB1CLK	GTR_14 _SPIB1SEN	VSSPLL FBCML	VDD1P8PLL	VDD1P8PLL	VSSPLL FBCML	GTL_7 _ALARM1	GTL_15 _GPIO3	GTL_18 _SPIASDO	VSSTXENC	VDD1P2FB	VDD1P8FB	VSSFB	2FBIN+	16
15	1FBIN-	VSSFB	VDD1P8FB	VDD1P2FB	VDD1P2FB	GTR_15 _RESETZ	GTR_13 _TRST	GTR_3 _TXTDD1	GTR_9 _SPIB2SDO	VDD1P2 PLLRXCML	VDD1P2 PLLFBCML	GTL_3 _AUX0	GTL_2 _ALARM2	GTL_4 _SPIACLK	GTL_6 _RXTDD2	VDD1P2FB	VDD1P2FB	VDD1P8FB	VSSFB	2FBIN-	15
14	VDD1P8 FBCLK	VSSFB	VSSFB	VDD1P2FB	VDD1P2RX	GTR_5 _TDO	GTR_18 _TDI	GTR_4 _TCLK	GTR_2 _SPIB2CLK	GTR_8 _FBTDD1	GTL_8 _AUX1	GTL_9 _AUX2	GTL_17 _SPIASDIO	GTL_1 _SPEEP	GTL_5 _SPIASEN	VDD1P2RX	VDD1P2FB	VSSFB	VSSFB	VDD1P8 FBCLK	14
13	VDD1P2RX	VSSRX	VSSRX	VSSRX	VDD1P2RX	VDD1P2RX	GTR_0 _RXGSWAP	GTR_6 _SPIB2 _SDIO	GND_ESD	DVDD0P9	DVDD0P9	GND_ESD	GTL_0 _GPIO2	GTL_11 _AUX3	VDD1P2RX	VDD1P2RX	VSSRX	VSSRX	VSSRX	VDD1P2RX	13
12	1RXIN+	VSSRX	VSSRX	VSSRX	VDD1P2RX	VDD1P2RX	GTR_11 _SPIB1 _SDO	GTR_1 _GPIO1	DGND	DVDD0P9	DVDD0P9	DGND	GTL_13 _AUX4	GTL_12 _BIST1	VDD1P2RX	VDD1P2RX	VSSRX	VSSRX	VSSRX	3RXIN+	12
11	1RXIN-	VSSRX	VDD1P8RX	VDD1P8RX	VDD1P2RX	VDD1P2RX	GTR_10 _TMS	GTR_12 _SPIB1 _SDIO	DGND	DVDD0P9	DVDD0P9	DGND	GTL_14 _AUX5	GTL_10 _BIST0	VDD1P2RX	VDD1P2RX	VDD1P8RX	VDD1P8RX	VSSRX	3RXIN-	11
10	VDD1P2RX	VSSRX	VDD1P8RX	VDD1P8RX	VDD1P8RX	VDD1P8RX	GBR_6 _RXBLNB	GBR_5 _FSPIDB	DGND	DVDD0P9	DVDD0P9	DGND	GBL_5 _GPIO15	GBL_6 _GPIO16	VDD1P8RX	VDD1P8RX	VDD1P8RX	VDD1P8RX	VSSRX	VDD1P2RX	10
9	VDD1P8 RXCLK	VSSRXCLK	VDD1P8RX	VDD1P8RX	VDD1P8RX	VDD1P8RX	GBR_9 _SYNCB _OUT0-	GBR_7 _SYNCB _OUT0+	DGND	DVDD0P9	DVDD0P9	DGND	GBL_7 _SYNCB _OUT1+	GBL_9 _SYNCB _OUT1-	VDD1P8RX	VDD1P8RX	VDD1P8RX	VDD1P8RX	VSSRXCLK	VDD1P8 RXCLK	9
8	2RXIN-	VSSRX	VSSRXCLK	GND_ESD	GBR_10 _FSPICLKA	VDD1P8RX	GBR_13 _GPIO8	GBR_8 _SYNCB _IN0+	DGND	DVDD0P9	DVDD0P9	DGND	GBL_8 _SYNCB _IN1+	GBL_13 _GPIO19	VDD1P8RX	GBL_10 _GPIO17	GND_ESD	VSSRXCLK	VSSRX	4RXIN-	8
7	2RXIN+	VSSRX	VSSRXCLK	GND_ESD	GBR_11 _RXTDD1	GBR_14 _FSPIDA	GBR_12 _GPIO7	GBR_17 _SYNCB _IN0-	DGND	DVDD0P9	DVDD0P9	DGND	GBL_17 _SYNCB _IN1-	GBL_12 _FSPICLKD	GBL_14 _FSPIDD	GBL_11 _GPIO18	GND_ESD	VSSRXCLK	VSSRX	4RXIN+	7
6	VDD1P8 RXCLK	VSSRXCLK	GBR_0 _GPIO4	GBR_19 _GPIO12	GBR_16 _GPIO10	GBR_1 _GPIO5	GBR_15 _GPIO9	VDD1P8 GPIO	DGND	DVDD0P9	DVDD0P9	DGND	VDD1P8 GPIO	GBL_15 _FSPIDC	GBL_1 _FBTDD2	GBL_16 _RXCLNB	GBL_19 _GPIO20	GBL_0 _GPIO13	VSSRXCLK	VDD1P8 RXCLK	6
5	VSSRXCLK	VSSRXCLK	GBR_18 _GPIO11	GBR_2 _RXALNB	GBR_4 _GPIO6	GBR_3 _FSPICLKB	IFORCE	VSSGPIO	DGND	DVDD0P9	DVDD0P9	DGND	VSSGPIO	VSENSE	GBL_3 _GPIO14	GBL_4 _RXDLNB	GBL_2 _FSPICLKC	GBL_18 _TXTDD2	VSSRXCLK	VSSRXCLK	5
4	VSST	VSST	1STX+	VDDT0P9	2STX+	VDDA1P8	3STX-	VDDA1P8	4STX-	VSST	VSST	5STX-	VDDA1P8	6STX-	VDDA1P8	7STX+	VDDT0P9	8STX+	VSST	VSST	4
3	1SRX+	VSST	1STX-	VDDT0P9	2STX-	VDDA1P8	3STX+	VDDA1P8	4STX+	SERDES _AMUX1	SERDES _AMUX2	5STX+	VDDA1P8	6STX+	VDDA1P8	7STX-	VDDT0P9	8STX-	VSST	8SRX+	3
2	1SRX-	VSST	VSST	VSST	VSST	VSST	VSST	VSST	VSST	DVDD0P9	DVDD0P9	VSST	VSST	VSST	VSST	VSST	VSST	VSST	VSST	8SRX-	2
1	VSST	2SRX+	2SRX-	VSST	3SRX+	3SRX-	VSST	4SRX+	4SRX-	VSST	VSST	5SRX-	5SRX+	VSST	6SRX-	6SRX+	VSST	7SRX-	7SRX+	VSST	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	

- TX Outputs
- RX Inputs
- FB Inputs
- Clock Inputs
- Serdes Receivers
- Serdes Transmitters
- MISC Analog
- GPIO
- 0.9V Supplies
- 1.2V Supplies
- 1.8V Supplies
- GROUND

AFE7988/89: ABJ Package
400-Pin FCBGA
Top View

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	
20	VDD1P2 TXCLK	2TXOUT+	2TXOUT-	VDD1P2 TXCLK	VDD1P8TX	1TXOUT-	1TXOUT+	VDD1P8TX	VSSTX	VDD1P2 PLLCLK REF	VDD1P8 PLLVCO	VSSTX	VDD1P8TX	3TXOUT+	3TXOUT-	VDD1P8TX	VDD1P2 TXCLK	4TXOUT-	4TXOUT+	VDD1P2 TXCLK	20
19	VSSTXCLK	VSSTX	VSSTX	VSSTXCLK	VSSTX	VSSTX	VSSTX	VSSTX	PLL _LDOUT	SYSREF+	SYSREF-	VSSPLL	VSSTX	VSSTX	VSSTX	VSSTX	VSSTXCLK	VSSTX	VSSTX	VSSTXCLK	19
18	VSSFBCLK	VSSFBCLK	VSSTX	VSSTX	VSSTX	VSSTX	VSSTX	VSSTX	VSSPLL CLKREF	VDD1P2 PLLCLK REF	VDD1P2 PLLCLK REF	VSSPLL CLKREF	VSSTX	VSSTX	VSSTX	VSSTX	VSSTX	VSSTX	VSSFBCLK	VSSFBCLK	18
17	VDD1P8 FBCLK	VSSFB	VSSTX	VDD1P2 TXENC	VSSTXENC	VSSTX	VDD1P8 TXDAC	VDD1P8 TXDAC	VSS PLLRXCML	REFCLK+	REFCLK-	VSS PLLRXCML	VDD1P8 TXDAC	VDD1P8 TXDAC	VSSTX	VSSTXENC	VDD1P2 TXENC	VSSTX	VSSFB	VDD1P8 FBCLK	17
16	NC	VSSFB	VDD1P8FB	VDD1P2FB	VSSTXENC	GTR_7 _SPIB2SEN	GTR_17 _SPIB1CLK	GTR_14 _SPIB1SEN	VSSPLL FBCML	VDD1P8PLL	VDD1P8PLL	VSSPLL FBCML	GTL_7 _ALARM1	GTL_15 _GPIO3	GTL_18 _SPIASDO	VSSTXENC	VDD1P2FB	VDD1P8FB	VSSFB	NC	16
15	NC	VSSFB	VDD1P8FB	VDD1P2FB	VDD1P2FB	GTR_15 _RESETZ	GTR_13 _TRST	GTR_3 _TXTDD1	GTR_9 _SPIB2SDO	VDD1P2 PLLRXCML	VDD1P2 PLLFBCML	GTL_3 _AUX0	GTL_2 _ALARM2	GTL_4 _SPIACLK	GTL_6 _RXTDD2	VDD1P2FB	VDD1P2FB	VDD1P8FB	VSSFB	NC	15
14	VDD1P8 FBCLK	VSSFB	VSSFB	VDD1P2FB	VDD1P2RX	GTR_5 _TDO	GTR_18 _TDI	GTR_4 _TCLK	GTR_2 _SPIB2CLK	GTR_8 _FBTDD1	GTL_8 _AUX1	GTL_9 _AUX2	GTL_17 _SPIASDIO	GTL_1 _SPEEP	GTL_5 _SPIASEN	VDD1P2RX	VDD1P2FB	VSSFB	VSSFB	VDD1P8 FBCLK	14
13	VDD1P2RX	VSSRX	VSSRX	VSSRX	VDD1P2RX	VDD1P2RX	GTR_0 _RXGSWAP	GTR_6 _SPIB2 _SDIO	GND_ESD	DVDD0P9	DVDD0P9	GND_ESD	GTL_0 _GPIO2	GTL_11 _AUX3	VDD1P2RX	VDD1P2RX	VSSRX	VSSRX	VSSRX	VDD1P2RX	13
12	1RXIN+	VSSRX	VSSRX	VSSRX	VDD1P2RX	VDD1P2RX	GTR_11 _SPIB1 _SDO	GTR_1 _GPIO1	DGND	DVDD0P9	DVDD0P9	DGND	GTL_13 _AUX4	GTL_12 _BIST1	VDD1P2RX	VDD1P2RX	VSSRX	VSSRX	VSSRX	3RXIN+	12
11	1RXIN-	VSSRX	VDD1P8RX	VDD1P8RX	VDD1P2RX	VDD1P2RX	GTR_10 _TMS	GTR_12 _SPIB1 _SDIO	DGND	DVDD0P9	DVDD0P9	DGND	GTL_14 _AUX5	GTL_10 _BIST0	VDD1P2RX	VDD1P2RX	VDD1P8RX	VDD1P8RX	VSSRX	3RXIN-	11
10	VDD1P2RX	VSSRX	VDD1P8RX	VDD1P8RX	VDD1P8RX	VDD1P8RX	GBR_6 _RXBLNB	GBR_5 _FSPIDB	DGND	DVDD0P9	DVDD0P9	DGND	GBL_5 _GPIO15	GBL_6 _GPIO16	VDD1P8RX	VDD1P8RX	VDD1P8RX	VDD1P8RX	VSSRX	VDD1P2RX	10
9	VDD1P8 RXCLK	VSSRXCLK	VDD1P8RX	VDD1P8RX	VDD1P8RX	VDD1P8RX	GBR_9 _SYNCB _OUT0-	GBR_7 _SYNCB _OUT0+	DGND	DVDD0P9	DVDD0P9	DGND	GBL_7 _SYNCB _OUT1+	GBL_9 _SYNCB _OUT1-	VDD1P8RX	VDD1P8RX	VDD1P8RX	VDD1P8RX	VSSRXCLK	VDD1P8 RXCLK	9
8	2RXIN-	VSSRX	VSSRXCLK	GND_ESD	GBR_10 _FSPICLKA	VDD1P8RX	GBR_13 _GPIO8	GBR_8 _SYNCB _IN0+	DGND	DVDD0P9	DVDD0P9	DGND	GBL_8 _SYNCB _IN1+	GBL_13 _GPIO19	VDD1P8RX	GBL_10 _GPIO17	GND_ESD	VSSRXCLK	VSSRX	4RXIN-	8
7	2RXIN+	VSSRX	VSSRXCLK	GND_ESD	GBR_11 _RXTDD1	GBR_14 _FSPIDA	GBR_12 _GPIO7	GBR_17 _SYNCB _IN0-	DGND	DVDD0P9	DVDD0P9	DGND	GBL_17 _SYNCB _IN1-	GBL_12 _FSPICLKD	GBL_14 _FSPIDD	GBL_11 _GPIO18	GND_ESD	VSSRXCLK	VSSRX	4RXIN+	7
6	VDD1P8 RXCLK	VSSRXCLK	GBR_0 _GPIO4	GBR_19 _GPIO12	GBR_16 _GPIO10	GBR_1 _GPIO5	GBR_15 _GPIO9	VDD1P8 GPIO	DGND	DVDD0P9	DVDD0P9	DGND	VDD1P8 GPIO	GBL_15 _FSPIDC	GBL_1 _FBTDD2	GBL_16 _RXCLNB	GBL_19 _GPIO20	GBL_0 _GPIO13	VSSRXCLK	VDD1P8 RXCLK	6
5	VSSRXCLK	VSSRXCLK	GBR_18 _GPIO11	GBR_2 _RXALNB	GBR_4 _GPIO6	GBR_3 _FSPICLKB	IFORCE	VSSGPIO	DGND	DVDD0P9	DVDD0P9	DGND	VSSGPIO	VSENSE	GBL_3 _GPIO14	GBL_4 _RXDLNB	GBL_2 _FSPICLKC	GBL_18 _TXTDD2	VSSRXCLK	VSSRXCLK	5
4	VSST	VSST	1STX+	VDDT0P9	2STX+	VDDA1P8	3STX-	VDDA1P8	4STX-	VSST	VSST	5STX-	VDDA1P8	6STX-	VDDA1P8	7STX+	VDDT0P9	8STX+	VSST	VSST	4
3	1SRX+	VSST	1STX-	VDDT0P9	2STX-	VDDA1P8	3STX+	VDDA1P8	4STX+	SERDES _AMUX1	SERDES _AMUX2	5STX+	VDDA1P8	6STX+	VDDA1P8	7STX-	VDDT0P9	8STX-	VSST	8SRX+	3
2	1SRX-	VSST	VSST	VSST	VSST	VSST	VSST	VSST	VSST	VDD0P9	VDD0P9	VSST	VSST	VSST	VSST	VSST	VSST	VSST	VSST	8SRX-	2
1	VSST	2SRX+	2SRX-	VSST	3SRX+	3SRX-	VSST	4SRX+	4SRX-	VSST	VSST	5SRX-	5SRX+	VSST	6SRX-	6SRX+	VSST	7SRX-	7SRX+	VSST	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	

TX Outputs
RX Inputs
Clock Inputs
Serdes Receivers
Serdes Transmitters
MISC Analog
GPIO
0.9V Supplies
1.2V Supplies
1.8V Supplies
GROUND

Pin Functions

BALL NAME	BALL NUMBER	I/O (1)	DESCRIPTION
RF INTERFACES			
1FBIN–	A15	I	Feedback Channel 1 RF inputs: negative terminal (AFE7920/21 only, NC for AFE7988/89)
1FBIN+	A16	I	Feedback Channel 1 RF inputs: positive terminal (AFE7920/21 only, NC for AFE7988/89)
2FBIN–	Y15	I	Feedback Channel 2 RF inputs: negative terminal (AFE7920/21 only, NC for AFE7988/89)

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

Pin Functions (continued)

BALL NAME	BALL NUMBER	I/O(1)	DESCRIPTION
2FBIN+	Y16	I	Feedback Channel 2 RF inputs: positive terminal (AFE7920/21 only, NC for AFE7988/89)
1RXIN–	A11	I	Receiver Channel 1 RF input: negative terminal. Input can be time shared for FB path on AFE7988/AFE7989.
1RXIN+	A12	I	Receiver Channel 1 RF input: positive terminal. Input can be time shared for FB path on AFE7988/AFE7989.
2RXIN–	A8	I	Receiver Channel 2 RF input: negative terminal
2RXIN+	A7	I	Receiver Channel 2 RF input: positive terminal
3RXIN–	Y11	I	Receiver Channel 3 RF input: negative terminal. Input can be time shared for FB path on AFE7988/AFE7989.
3RXIN+	Y12	I	Receiver Channel 3 RF input: positive terminal. Input can be time shared for FB path on AFE7988/AFE7989.
4RXIN–	Y8	I	Receiver Channel 4 RF input: negative terminal
4RXIN+	Y7	I	Receiver Channel 4 RF input: positive terminal
1TXOUT–	F20	O	Transmitter Channel 1 RF output: negative terminal. Connect to 1.8 V when not used.
1TXOUT+	G20	O	Transmitter Channel 1 RF output: positive terminal. Connect to 1.8 V when not used.
2TXOUT–	C20	O	Transmitter Channel 2 RF output: negative terminal. Connect to 1.8 V when not used.
2TXOUT+	B20	O	Transmitter Channel 2 RF output: positive terminal. Connect to 1.8 V when not used.
3TXOUT–	R20	O	Transmitter Channel 3 RF output: negative terminal. Connect to 1.8 V when not used.
3TXOUT+	P20	O	Transmitter Channel 3 RF output: positive terminal. Connect to 1.8 V when not used.
4TXOUT–	V20	O	Transmitter Channel 4 RF output: negative terminal. Connect to 1.8 V when not used.
4TXOUT+	W20	O	Transmitter Channel 4 RF output: positive terminal. Connect to 1.8 V when not used.
DIFFERENTIAL CLOCKS INPUTS			
REFCLK–	L17	I	Reference Clock Inputs: negative terminal
REFCLK+	K17	I	Reference Clock Inputs: positive terminal
SYSREF–	L19	I	SYSREEF inputs: negative terminals
SYSREF+	K19	I	SYSREEF inputs: positive terminals
SerDes CML INTERFACE			
1SRX–	A2	I	CML SerDes Interface Lane 1 input: negative terminal
1SRX+	A3	I	CML SerDes Interface Lane 1 input: positive terminal
2SRX–	C1	I	CML SerDes Interface Lane 2 input: negative terminal
2SRX+	B1	I	CML SerDes Interface Lane 2 input: positive terminal
3SRX–	F1	I	CML SerDes Interface Lane 3 input: negative terminal
3SRX+	E1	I	CML SerDes Interface Lane 3 input: positive terminal
4SRX–	J1	I	CML SerDes Interface Lane 4 input: negative terminal
4SRX+	H1	I	CML SerDes Interface Lane 4 input: positive terminal
5SRX–	M1	I	CML SerDes Interface Lane 5 input: negative terminal
5SRX+	N1	I	CML SerDes Interface Lane 5 input: positive terminal
6SRX–	R1	I	CML SerDes Interface Lane 6 input: negative terminal
6SRX+	T1	I	CML SerDes Interface Lane 6 input: positive terminal
7SRX–	V1	I	CML SerDes Interface Lane 7 input: negative terminal
7SRX+	W1	I	CML SerDes Interface Lane 7 input: positive terminal
8SRX–	Y2	I	CML SerDes Interface Lane 8 input: negative terminal

Pin Functions (continued)

BALL NAME	BALL NUMBER	I/O(1)	DESCRIPTION
8SRX+	Y3	I	CML SerDes Interface Lane 8 input: positive terminal
1STX–	C3	O	CML SerDes Interface Lane 1 output: negative terminal
1STX+	C4	O	CML SerDes Interface Lane 1 output: positive terminal
2STX–	E3	O	CML SerDes Interface Lane 2 output: negative terminal
2STX+	E4	O	CML SerDes Interface Lane 2 output: positive terminal
3STX–	G4	O	CML SerDes Interface Lane 3 output: negative terminal
3STX+	G3	O	CML SerDes Interface Lane 3 output: positive terminal
4STX–	J4	O	CML SerDes Interface Lane 4 output: negative terminal
4STX+	J3	O	CML SerDes Interface Lane 4 output: positive terminal
5STX–	M4	O	CML SerDes Interface Lane 5 output: negative terminal
5STX+	M3	O	CML SerDes Interface Lane 5 output: positive terminal
6STX–	P4	O	CML SerDes Interface Lane 6 output: negative terminal
6STX+	P3	O	CML SerDes Interface Lane 6 output: positive terminal
7STX–	T3	O	CML SerDes Interface Lane 7 output: negative terminal
7STX+	T4	O	CML SerDes Interface Lane 7 output: positive terminal
8STX–	V3	O	CML SerDes Interface Lane 8 output: negative terminal
8STX+	V4	O	CML SerDes Interface Lane 8 output: positive terminal
GPIO FUNCTIONS			
GBL_0_GPIO13	V6	I/O	GPIO.
GBL_1_FBTDD2	R6	I/O	Default location of FB TDD2 input signal.
GBL_2_FSPICLKC	U5	I/O	Default and recommended location of FSPI C clock (FSPI for factory use only, available as generic GPIO).
GBL_3_GPIO14	R5	I/O	GPIO.
GBL_4_RXDLNB	T5	I/O	Default location of RX channel D AGC LNA Bypass output signal.
GBL_5_GPIO15	N10	I/O	GPIO.
GBL_6_GPIO16	P10	I/O	GPIO.
GBL_7_SYNCB_OUT1+	N9	I/O	Default location of JESD Sync\ 1 output differential positive terminal.
GBL_8_SYNCB_IN1+	N8	I/O	Default location of JESD Sync\ 1 input differential positive terminal.
GBL_9_SYNCB_OUT1–	P9	I/O	Default location of JESD Sync\ 1 output differential negative terminal.
GBL_10_GPIO17	T8	I/O	GPIO.
GBL_11_GPIO18	T7	I/O	GPIO.
GBL_12_FSPICLKD	P7	I/O	Default and recommended location of FSPI D clock (FSPI for factory use only, available as generic GPIO).
GBL_13_GPIO19	P8	I/O	GPIO.
GBL_14_FSPIDD	R7	I/O	Default and recommended location of FSPI D data (FSPI for factory use only, available as generic GPIO).
GBL_15_FSPIDC	P6	I/O	Default and recommended location of FSPI C clock (FSPI for factory use only, available as generic GPIO).
GBL_16_RXCLNB	T6	I/O	Default location of RX channel C AGC LNA Bypass output signal.
GBL_17_SYNCB_IN1–	N7	I/O	Default location of JESD Sync\ 1 input differential negative terminal.
GBL_18_TXTDD2	V5	I/O	Default location of TX TDD2 input signal.
GBL_19_GPIO20	U6	I/O	GPIO.
GBR_0_GPIO4	C6	I/O	GPIO.
GBR_1_GPIO5	F6	I/O	GPIO.

Pin Functions (continued)

BALL NAME	BALL NUMBER	I/O(1)	DESCRIPTION
GBR_2_RXALNB	D5	I/O	Default location of RX channel A AGC LNA Bypass output signal.
GBR_3_FSPICLKB	F5	I/O	Default and recommended location of FSPI B clock (FSPI for factory use only, available as generic GPIO).
GBR_4_GPIO6	E5	I/O	GPIO.
GBR_5_FSPIDB	H10	I/O	Default and recommended location of FSPI B data (FSPI for factory use only, available as generic GPIO).
GBR_6_RXBLNB	G10	I/O	Default location of RX channel B AGC LNA Bypass output signal.
GBR_7_SYNCB_OUT0+	H9	I/O	Default location of JESD Sync\ 0 output differential positive terminal.
GBR_8_SYNCB_IN0+	H8	I/O	Default location of JESD Sync\ 0 input differential positive terminal.
GBR_9_SYNCB_OUT0–	G9	I/O	Default location of JESD Sync\ 0 output differential negative terminal.
GBR_10_FSPICLKA	E8	I/O	Default location of FSPI A clock (FSPI for factory use only, available as generic GPIO).
GBR_11_RXTDD1	E7	I/O	Default location of RX TDD1 input signal.
GBR_12_GPIO7	G7	I/O	GPIO.
GBR_13_GPIO8	G8	I/O	GPIO.
GBR_14_FSPIDA	F7	I/O	Default and recommended location of FSPI A clock (FSPI for factory use only, available as generic GPIO).
GBR_15_GPIO9	G6	I/O	GPIO.
GBR_16_GPIO10	E6	I/O	GPIO.
GBR_17_SYNCB_IN0–	H7	I/O	Default location of JESD Sync\ 0 input differential negative terminal.
GBR_18_GPIO11	C5	I/O	GPIO.
GBR_19_GPIO12	D6	I/O	GPIO.
GTL_0_GPIO2	N13	I/O	GPIO.
GTL_1_SLEEP	P14	I/O	Default location of Sleep input signal.
GTL_2_ALARM2	N15	I/O	Default location of Alarm 2 output signal.
GTL_3_AUX0	M15	I/O	GPIO or auxiliary low-speed ADC input 0
GTL_4_SPIACLK	P15	I/O	Fixed Location of SPI A Clock.
GTL_5_SPIASEN	R14	I/O	Fixed Location of SPI A Send Enable.
GTL_6_RXTDD2	R15	I/O	Default location of RX TDD2 input signal.
GTL_7_ALARM1	N16	I/O	Default location of Alarm 1 output signal.
GTL_8_AUX1	L14	I/O	GPIO or auxiliary low-speed ADC input 1.
GTL_9_AUX2	M14	I/O	GPIO or auxiliary low-speed ADC input 2.
GTL_10_BIST0	P11	I/O	Fixed Location for BIST0 Function. Set low when using JTAG, set high for normal operation.
GTL_11_AUX3	P13	I/O	GPIO or auxiliary low-speed ADC input 3.
GTL_12_BIST1	P12	I/O	Fixed Location for BIST1 Function. Set high when using JTAG, set low for normal operation.
GTL_13_AUX4	N12	I/O	GPIO or auxiliary low-speed ADC input 4.
GTL_14_AUX5	N11	I/O	GPIO or auxiliary low-speed ADC input 5.
GTL_15_GPIO3	P16	I/O	GPIO.
GTL_17_SPIASDIO	N14	I/O	Fixed Location of SPI A Serial Data Input (3- and 4-wire mode) or Output (3 wire mode only).
GTL_18_SPIASDO	R16	I/O	Fixed Location of SPI A Serial Data Output in 4-wire mode.
GTR_0_RXGSWAP	G13	I/O	Default location of RX gain swap input.
GTR_1_GPIO1	H12	I/O	GPIO.

Pin Functions (continued)

BALL NAME	BALL NUMBER	I/O(1)	DESCRIPTION
GTR_2_SPIB2CLK	J14	I/O	Default and recommended location of SPI B2 clock.
GTR_3_TXTDD1	H15	I/O	Default location of TX TDD1 input signal.
GTR_4_TCLK	H14	I/O	Fixed location for JTAG Test Clock.
GTR_5_TDO	F14	I/O	Fixed location for JTAG Test Data Out.
GTR_6_SPIB2_SDIO	H13	I/O	Default and recommended location of SPI B2 serial data input/output.
GTR_7_SPIB2SEN	F16	I/O	Default and recommended location of SPI B2 enable input.
GTR_8_FBTDD1	K14	I/O	Default location of FB TDD1 input signal.
GTR_9_SPIB2SDO	J15	I/O	Default and recommended location of SPI B2 serial data output (4-wire mode)
GTR_10_TMS	G11	I/O	Fixed location for JTAG Test Mode Select.
GTR_11_SPIB1_SDO	G12	I/O	Default and recommended location of SPI B1 enable input.
GTR_12_SPIB_SDIO	H11	I/O	Default and recommended location of SPI B1 serial data input/output.
GTR_13_TRST	G15	I/O	Fixed location for JTAG Test Reset. Must be pulled low when the JTAG port is not used.
GTR_14_SPIB1SEN	H16	I/O	Default and recommended location of SPI B1 enable input.
GTR_15_RESETZ	F15	I/O	Fixed Location for reset function. Chip Reset to default register settings.
GTR_17_SPIB1CLK	G16	I/O	Default and recommended location of SPI B1 clock.
GTR_18_TDI	G14	I/O	Fixed location for JTAG Test Data Input.
POWER SUPPLIES			
DVDD	K2, K5, K6, K7, K8, K9, K10, K11, K12, K13, L2, L5, L6, L7, L8, L9, L10, L11, L12, L13	—	0.9-V digital power supply
VDD1P2FB	D14, D15, D16, E15, U14, U15, U16, T15	—	1.2-V supply for FB ADCs.
VDD1P8FB	C15, C16, V15, V16	—	1.8-V supply for FB ADC.
VDD1P8FBCLK	A14, A17, Y17, Y14	—	1.8-V supply for FB ADC clock.
VDD1P2PLLCLKREF	K20, K18, L18	—	1.2-V supply for PLL.
VDDPLL1P2FBCML	L15	—	1.2-V supply for PLL clock distribution to FB ADC.
VDDPLL1P2RXCML	K15	—	1.2-V supply for clock distribution to RX ADC.
VDD1P8PLL	K16, L16	—	1.8-V supply for PLL.
VDD1P8PLLVCO	L20	—	1.8-V supply for PLL/VCO. This is a sensitive net and requires extra care in layout.
VDD1P2RX	A10, A13, E11, E12, E13, E14,F11, F12, F13, R11, R12, R13, T11, T12, T13, T14, Y10, Y13	—	1.2-V supply for RX ADCs.
VDD1P8RX	C9, C10, C11, D9, D10, D11, E9, E10, F8, F9, F10, R8, R9, R10, T9, T10, U9, U10, U11, V9, V10, V11	—	1.8-V supply for RX ADCs.
VDD1P8RXCLK	A6, A9, Y6, Y9	—	1.8-V supply for RX ADC clocks.
VDD1P2TXENC	D17, U17	—	1.2-V supply for DAC encoder.
VDD1P2TXCLK	A20, D20, U20, Y20	—	1.2-V supply for DAC clock.
VDD1P8TX	E20, H20, N20, T20	—	1.8-V supply for DAC.
VDD1P8TXDAC	G17, H17, N17, P17	—	1.8-V supply for DAC.
VDD1P8GPIO	H6, N6	—	1.8-V supply for GPIO.
VDDA1P8	F3, F4, H3, H4, R3, R4, N3, N4	—	SerDes analog 1.8-V power supply.
VDDT0P9	D3, D4, U3, U4	—	SerDes digital 0.9-V power supply.

Pin Functions (continued)

BALL NAME	BALL NUMBER	I/O(1)	DESCRIPTION
GROUNDS			
DGND	J5, J6, J7, J8, J9, J10, J11, J12, M5, M6, M7, M8, M9, M10, M11, M12	—	Digital core ground
VSSGPIO	H5, N5	—	GPIO ground.
VSSFB	B14, B15, B16, B17, C14, V14, W14, W15, W16, W17	—	Ground for FB ADC supply.
VSSFBCLK	A18, B18, W18, Y18	—	Ground for FB ADC 1.8-V clock supply.
GND_ESD	D7, D8, J13, M13, U7, U8	—	Ground for ESD protection circuits.
VSSRX	B7, B8, B10, B11, B12, C12, D12, B13, C13, D13, W7, W8, W10, W11, W13, U12, V12, W12, U13, V13	—	Ground for RX ADC.
VSSRXCLK	A5, B5, B6, B9, C7, C8, W5, W6, W9, Y5, V7, V8	—	Ground for RX ADC clocks.
VSSTX	B19, C17, C18, C19, D18, E18, E19, F17, F18, F19, G18, G19, H18, H19, J20, M20, N18, N19, P18, P19, R17, R18, R19, T18, T19, U18, V17, V18, V19, W19	—	Ground for TX DAC.
VSSTXENC	E16, E17, T16, T17	—	Ground for TX DAC encoder.
VSSTXCLK	A19, D19, U19, Y19	—	Ground for TX DAC clock.
VSSPLL	M19	—	Ground for PLL.
VSSPLLFBCML	J16, M16	—	Ground for FB ADC clock.
VSSPLLCLKREF	J18, M18	—	Ground for CLKREF PLL.
VSSPLLRXCML	J17, M17	—	Ground for RX ADC clock.
VSST	A1, A4, B2, B3, B4, C2, D1, D2, E2, F2, G1, G2, H2, J2, K1, K4, L1, L4, M2, N2, P1, P2, R2, T2, U1, U2, V2, W2, W3, W4, Y1, Y4	—	SerDes ground.
OTHERS			
IFORCE	G5	—	Reserved for TI use only. Do not connect.
PLL_LDOUT	J19	—	Connect with 100-nF capacitor to GND
SerDes_AMUX1	K3	—	
SerDes_AMUX2	L3	—	
VSENSE	P5	—	Process test: sense voltage (TI use only). Do not connect.

8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply Voltage Range	DVDD0P9, VDDT0P9	–0.3	1.2	V
	VDD1P2RX, VDD1P2TXCLK, VDD1P2TXENC, VDD1P2PLL, VDD1P2PLLCLKREF, VDD1P2FB, VDD1P2FBCML, VDD1P2RXCML	–0.3	1.4	V
	VDD1P8RX, VDD1P8RXCLK, VDD1P8TX, VDD1P8TXDAC, VDD1P8TXENC, VDD1P8PLL, VDD1P8PLLVCO, VDD1P8FB, VDD1P8FBCLK, VDD1P8GPIO, VDDA1P8	–0.5	2.1	V
Pin Volatge Range	{1/2/3/4}RXIN+/-	–0.5	VDDRX1P8+0.3	V
	1FBIN+/-, 2FB+/-	–0.5	VDDFB1P8+0.3	V
	{1/2/3/4}TXOUT+/-	–0.5	VDDTX1P8+0.3	V
	REFCLK+/-, SYSREF+/-	–0.3	1.4	V
	{1:8}SRX+/-	–0.3	1.4	V
	{1:8}STX+/-	–0.3	1.4	V
	GPIO{B/C/D/E}x, SPICLK, SPISDIO, SPISDO, SPISEN, RESETZ, BISTB0, BISTB1	–0.5	VDD1P8GPIO + 0.3	V
	IFORCE, VSENSE	–0.3	VDDCLK1P8 + 0.3	V
	SRDAMUX1, SRDAMUX2	–0.3	VDDA1P8+0.3	V
Peak Input Current	any input		20	mA
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

8.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	1000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins	150	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
DVDD0P9, VDDT0P9	Supply voltage 0.9V	0.9	0.925	0.95	V
VDD1P2{RX/TXCLK/TXENC/FB/PLL/PLLCLKREF/FBCML/RXCML}	Supply voltage 1.2V	1.15	1.2	1.25	V
VDD1P8{RX/RXCLK/TX/TXDAC/TXENC/PLL/PLLVCO/FB/FBCLK/GPIO}, VDDA1P8	Supply voltage 1.8V	1.75	1.8	1.85	V
T_A	Ambient temperature	–40		85	°C
T_J	Operating Junction Temperature			110(1)	°C
	Maximum Operating Junction Temperature	125			°C

(1) Prolonged use at or above this junction temperature can increase the device failure-in-time (FIT) rate. Refer to SBAA403 application note for additional details

8.4 Thermal Information

THERMAL METRIC(1)		AFE79xx ABJ (FC-BGA) 400 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	15.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.51	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	4.85	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.08	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	4.8	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

8.5 Transmitter Electrical Characteristics

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 491.52MSPS, f_{DAC} = 11796.48MSPS; Internal PLL, f_{REF} = 491.52MSPS; interleave mode, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 16.22Gbps; TX clock dither enabled, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{RFout}	RF output frequency range	f_{DAC} = 11796.48 MSPS, 1st Nyquist	600		5500	MHz
		f_{DAC} = 8847.36 MSPS, 1st Nyquist	600		4200	
		f_{DAC} = 5898.24 MSPS, 1st Nyquist	600		2700	
		f_{DAC} = 5898.24 MSPS, 2nd Nyquist	3200		5500	
		f_{DAC} = 8847.36 MSPS, 2nd Nyquist	4600		6000	MHz
P_{max_FS}	Max Full Scale Output Power, max gain 1 tone, at device pins	f_{out} = 850 MHz, f_{DAC} = 5898.24 MSPS, -0.5dBFS		4.2		dBm
	Max Full Scale Output Power, max gain 1 tone, at device pins	f_{out} = 1800 MHz, f_{DAC} = 5898.24 MSPS, -0.5dBFS		4.6		dBm
	Max Full Scale Output Power, max gain 1 tone, at device pins	f_{out} = 2600 MHz, f_{DAC} = 8847.36 MSPS, -0.5dBFS		4.0		dBm
		f_{out} = 3500 MHz, f_{DAC} = 11796.48 MSPS, -0.5dBFS		3.9		dBm
	Max Full Scale Output Power, max gain 1 tone, at device pins	f_{out} = 4900 MHz, f_{DAC} = 11796.48 MSPS, -0.5dBFS		3.1		dBm
	Max Full Scale Output Power, max gain 1 tone, at device pins	f_{out} = 3500 MHz, f_{DAC} = 5898.24 MSPS, -0.5dBFS, straight mode		1.0		dBm
	Max Full Scale Output Power, max gain 1 tone, at device pins	f_{out} = 4900 MHz, f_{DAC} = 5898.24 MSPS, -0.5dBFS, straight mode		0.1		dBm
	Max Full Scale Output Power, max gain 1 tone, at device pins	f_{out} = 4900 MHz, f_{DAC} = 8847.36 MSPS, -0.5dBFS, straight mode		-0.7		dBm
R_{TERM}	Output termination resistor	Default setting		50		Ω
ATT_{range}	DSA Attenuation range			40.0		dB
ATT_{step}	DSA Analog Attenuation step			1.0		dB
	DSA Attenuation step accuracy (DNL)	0 < Atten < 40dB, before calibration		±0.2		dB
		0 < Atten < 40dB, after calibration		±0.1		dB
$ATT_{phase-err}$	DSA Gain Steps Phase accuracy, any 8dB range	f_{out} = 850MHz (1)		±1		deg
		f_{out} = 1800MHz (1)		±1		deg
		f_{out} =2600MHz (1)		±1		deg
		f_{out} = 3500MHz (1)		±1		
		f_{out} = 4900MHz (1)		±1		deg
G_{flat}	Gain flatness	any 20MHz		0.1		dB
		600MHz BW, F_{out} < 4.9G		1.2		
IMD3	3rd Order Intermodulation distortion, 2 tones at f_{IF}±10 MHz -13dBFS each tone	f_{out} = 850MHz		-74.4		dBc
		f_{out} = 1800MHz		-71.1		dBc
		f_{out} = 2600MHz		-73		dBc
		f_{out} = 3500MHz		-72		dBc
		f_{out} = 4900MHz		-67.8		dBc
SFDR	Spurious Free Dynamic Range (within Nyquist zone)	f_{out} = 850 MHz, f_{DAC} = 11796.48 MSPS		50.8		dBc
		f_{out} = 1800 MHz, f_{DAC} = 11796.48 MSPS		51.9		dBc
		f_{out} = 2600 MHz, f_{DAC} = 11796.48 MSPS		42		dBc
		f_{out} = 3500 MHz, f_{DAC} = 11796.48 MSPS		44		dBc
		f_{out}= 4900 MHz, f_{DAC} = 11796.48 MSPS		46.1		dBc

(1) After DSA calibration procedure

Transmitter Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 491.52MSPS, f_{DAC} = 11796.48MSPS; Internal PLL, f_{REF} = 491.52MSPS; interleave mode, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 16.22Gbps; TX clock dither enabled, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_S/2 - f_{OUT}$	Interleaving Image	f_{DAC} = 5898.24MSPS, interleave mode		-51.9		dBc
		f_{DAC} = 8847.36 MSPS, interleave mode		-46.0		dBc
		f_{DAC} = 11796.48MSPS, interleave mode		-41		dBc
HD2	2nd Harmonic Distortion (within Nyquist zone) A_{OUT}=-12dBFS	f_{out} = 850 MHz, f_{DAC} = 5898.24 MSPS		-60.1		dBc
		f_{out} = 1800 MHz, f_{DAC} = 5898.24 MSPS		-63.7		dBc
		f_{out} = 2600 MHz		-45		dBc
		f_{out} = 3500 MHz		-57		dBc
		f_{out}= 4900 MHz, f_{DAC} = 11796.48 MSPS		-58.0		dBc
HD3	3rd Harmonic Distortion (within Nyquist zone) A_{OUT}=-12dBFS	f_{out} = 850 MHz, f_{DAC} = 5898.24 MSPS		-80.4		dBc
		f_{out} = 1800 MHz, f_{DAC} = 5898.24 MSPS		-79.4		dBc
		f_{out} = 2600 MHz		-77		dBc
		f_{out} = 3500 MHz		-77		dBc
		f_{out}= 4900 MHz, f_{DAC} =11796.48 MSPS		-78.0		dBc
HDn, n >= 4	Harmonic Distortion n >= 4 (within Nyquist zone) A_{OUT}=-12dBFS	f_{out} = 850 MHz, f_{DAC} = 5898.24 MSPS		-92.7		dBc
		f_{out} = 1800 MHz, f_{DAC} = 5898.24 MSPS		-98.0		dBc
		f_{out} = 2600 MHz		-84		dBc
		f_{out} = 3500 MHz		-87		dBc
		f_{out}= 4900 MHz, f_{DAC} =11796.48 MSPS		-87.0		dBc
SFDR +/- 250 MHz	Spurious Free Dynamic Range within +/- 250 MHz	f_{out} = 850 MHz, f_{DAC} = 11796.48 MSPS		68.5		dBc
		f_{out} = 1800 MHz, f_{DAC} = 11796.48 MSPS		79.4		dBc
		f_{out} = 2600 MHz, f_{DAC} = 11796.48 MSPS		77		dBc
		f_{out} = 3500 MHz, f_{DAC} = 11796.48 MSPS		75		dBc
		f_{out}= 4900 MHz, f_{DAC} = 11796.48 MSPS		76.0		dBc
		f_{out} = 850 MHz, f_{DAC} = 5898.24 MSPS		68.5		dBc
		f_{out} = 1800 MHz, f_{DAC} = 5898.24 MSPS		79.4		dBc
		f_{out} = 2600 MHz, f_{DAC} = 8847.36 MSPS		77		dBc
		f_{out} = 3500 MHz, f_{DAC} = 8847.36 MSPS		75		dBc
$f_S/4$	Fixed Spur	f_{DAC} = 5898.24MSPS		-64		dBFS
		f_{DAC} = 8847.36MSPS		-75		dBFS
		f_{DAC} = 11796.48MSPS		-67		dBFS
$f_S/2$	Fixed Spur	f_{DAC} = 5898.24MSPS		-49		dBFS
		f_{DAC} = 8847.36MSPS		-48		dBFS
		f_{DAC} = 11796.48 MSPS		-48		dBFS
$3*f_S/4$	Fixed Spur	2nd Nyquist, f_{DAC} = 5898.24MSPS		-76		dBFS
		2nd Nyquist, f_{DAC} = 8847.36MSPS		-89		dBFS
		2nd Nyquist, f_{DAC} = 11796.48MSPS		-63		dBFS

Transmitter Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 491.52MSPS, f_{DAC} = 11796.48MSPS; Internal PLL, f_{REF} = 491.52MSPS; interleave mode, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 16.22Gbps; TX clock dither enabled, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$ACPR_{1xcarr}$	ACPR - 1 carrier, LTE 20MHz E-TM1.1 carrier f_{out} = 0.85 GHz	Atten=0dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFs		-68.7		dBc
		Atten=20dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFs		-66.1		dBc
		Atten=28dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFs		-62.2		dBc
		Atten=39dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFs		-51.6		dBc
$ACPR_{1xcarr}$	ACPR - 1 carrier, LTE 20MHz E-TM1.1 carrier f_{out} = 1.8425 GHz	Atten=0dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFs		-70.7		dBc
		Atten=20dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFs		-68.3		dBc
		Atten=28dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFs		-62.9		dBc
		Atten=39dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFs		-52.0		dBc
$ACPR_{1xcarr}$	ACPR - 1 carrier, LTE 20MHz E-TM1.1 carrier f_{out} = 2.6 GHz	Atten=0dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFs		-71		dBc
		Atten=20dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFs		-68		dBc
		Atten=28dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFs		-62		dBc
		Atten=39dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFs		-51.3		dBc
$ACPR_{1xcarr}$	ACPR - 1 carrier, LTE 20MHz E-TM1.1 carrier f_{out} = 3.5 GHz	Atten=0dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFs		-70		dBc
		Atten=20dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFs		-67		dBc
		Atten=28dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFs		-60		dBc
		Atten=39dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFs		-49.8		dBc
$ACPR_{1xcarr}$	ACPR - 1 carrier, LTE 20MHz E-TM1.1 carrier f_{out} = 4.9 GHz	Atten=0dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFs		-68.8		dBc
		Atten=20dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFs		-65.9		dBc
		Atten=28dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFs		-60.6		dBc
		Atten=39dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFs		-49.5		dBc

Transmitter Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 491.52MSPS, f_{DAC} = 11796.48MSPS; Internal PLL, f_{REF} = 491.52MSPS; interleave mode, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 16.22Gbps; TX clock dither enabled, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$ACPR_{1xcarr}$	ACPR - 1 carrier, NR 100MHz E-TM1.1 carrier f_{out} = 2.6 GHz	Atten=0dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFs		-65		dBc
		Atten=20dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFs		-62		dBc
		Atten=20dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFs		-55		dBc
		Atten=39dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFs		-44.3		dBc
$ACPR_{1xcarr}$	ACPR - 1 carrier, NR 100MHz E-TM1.1 carrier f_{out} = 3.5 GHz	Atten=0dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFs		-64		dBc
		Atten=20dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFs		-59		dBc
		Atten=28dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFs		-52		dBc
		Atten=39dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFs		-41.1		dBc
$ACPR_{1xcarr}$	ACPR - 1 carrier, NR 100MHz E-TM1.1 carrier f_{out} = 4.9 GHz	Atten=0dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFs		-64.1		dBc
		Atten=20dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFs		-60.4		dBc
		Atten=28dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFs		-53.5		dBc
		Atten=39dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFs		-42.5		dBc

Transmitter Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 491.52MSPS, f_{DAC} = 11796.48MSPS; Internal PLL, f_{REF} = 491.52MSPS; interleave mode, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 16.22Gbps; TX clock dither enabled, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
EVM	Error Vector Magnitude, 1x 20MHz E-TM3.1/3.1a, no ref. clock noise	F_{out} =0.85 GHz, f_{DAC} = 11796.48MSPS, P_{OUT}=-13dBFs		0.2		%
		F_{out} =1.8425 GHz, f_{DAC} = 11796.48MSPS, P_{OUT}=-13dBFs		0.3		%
		F_{out} =2.6 GHz, f_{DAC} = 11796.48MSPS, P_{OUT}=-13dBFs		0.28		%
		F_{out} =3.5 GHz, P_{OUT}=-13dBFs		0.38		%
		F_{out} =4.9 GHz, P_{OUT}=-13dBFs		0.4		%
NSD_{dBFS}	Noise Spectral Density 20MHz offset f_{OUT} = 0.85 GHz	Atten=0dB, f_{DAC} = 5898.24MSPS, Pout=-13dBFs		-156.3		dBFS/Hz
		Atten=20dB, f_{DAC} = 5898.24MSPS, Pout=-13dBFs		-151.1		dBFS/Hz
		Atten=28dB, f_{DAC} = 5898.24MSPS, Pout=-13dBFs		-145.3		dBFS/Hz
		Atten=39dB, f_{DAC} = 5898.24MSPS, Pout=-13dBFs		-134.5		dBFS/Hz
NSD_{dBFS}	Noise Spectral Density 20MHz offset f_{OUT} = 1.8 GHz	Atten=0dB, f_{DAC} = 5898.24MSPS, Pout=-13dBFs		-158.4		dBFS/Hz
		Atten=20dB, f_{DAC} = 5898.24MSPS, Pout=-13dBFs		-152.2		dBFS/Hz
		Atten=28dB, f_{DAC} = 5898.24MSPS, Pout=-13dBFs		-145.6		dBFS/Hz
		Atten=39dB, f_{DAC} = 5898.24MSPS, Pout=-13dBFs		-134.6		dBFS/Hz
NSD_{dBFS}	Noise Spectral Density 20MHz offset f_{OUT} = 2.6 GHz	Atten=0dB, f_{DAC} = 8847.36MSPS, Pout=-13dBFs		-157		dBFS/Hz
		Atten=20dB, f_{DAC} = 8847.36MSPS, Pout=-13dBFs		-151		dBFS/Hz
		Atten=28dB, f_{DAC} = 8847.36MSPS, Pout=-13dBFs		-144		dBFS/Hz
		Atten=39dB, f_{DAC} = 8847.36MSPS, Pout=-13dBFs		-133.0		dBFS/Hz
NSD_{dBFS}	Noise Spectral Density 20MHz offset F_{out} =3.5 GHz	Atten=0dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFs		-158		dBFS/Hz
		Atten=20dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFs		-150		dBFS/Hz
		Atten=28dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFs		-143		dBFS/Hz
		Atten=39dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFs		-131.8		dBFS/Hz
NSD_{dBFS}	Noise Spectral Density 20MHz offset F_{out} =4.9 GHz	Atten=0dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFs		-155.5		dBFS/Hz
		Atten=20dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFs		-147.8		dBFS/Hz
		Atten=28dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFs		-140.8		dBFS/Hz
		Atten=39dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFs		-129.6		dBFS/Hz
S22	Output Return Loss, +/- fc * 10%	with matching		-17		dB

Transmitter Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 491.52MSPS, f_{DAC} = 11796.48MSPS; Internal PLL, f_{REF} = 491.52MSPS; interleave mode, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 16.22Gbps; TX clock dither enabled, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Isolation	Near Channel: 1TXOUT to 2TXOUT or 3TXOUT to 4TXOUT(2)	f_{out} = 900 MHz, f_{DAC} = 8847.36MSPS, straight mode		-49.1		dB
		f_{out} = 1850 MHz, f_{DAC} = 8847.36MSPS, straight mode		-59.3		dB
		f_{out} = 2600 MHz, f_{DAC} = 8847.36MSPS, straight mode		-65		dB
		f_{out} = 3500 MHz, f_{DAC} = 8847.36MSPS, straight mode		-66		dB
		f_{out}= 4900 MHz, f_{DAC} = 8847.36MSPS, straight mode		-60		dB
	Far Channel: 1/2TXOUT to 3/4TXOUT	f_{out} = 900 MHz, f_{DAC} = 8847.36MSPS, straight mode		-89.9		dB
		f_{out} = 1850 MHz, f_{DAC} = 8847.36MSPS, straight mode		-90.9		dB
		f_{out} = 2600 MHz, f_{DAC} = 8847.36MSPS, straight mode		-93		dB
		f_{out} = 3500 MHz, f_{DAC} = 8847.36MSPS, straight mode		-94		dB
		f_{out}= 4900 MHz, f_{DAC} = 8847.36MSPS, straight mode		-83.2		dB

(2) Measured with differential 50 ohm across TxP/M. The DC bias to 1.8V to each TxP/M at each pin remains and is not removed. Other external components on the TX paths are disconnected.

8.6 RF ADC Electrical Characteristics

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; RX Output Rate = 491.52MSPS, f_{ADC} = 2949.12MSPS; Internal PLL, f_{REF} = 491.52MSPS; nominal power supplies; DSA Setting =4dB; SerDes rate =24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
F_{RFin}	RF input frequency range		600		6000	MHz
$P_{FS\_CW,min}$	Min Full scale input power, at device pins (1)	f_{IN} = 830 MHz, DSA=0dB		-2.9		dBm
		f_{IN} = 1760 MHz, DSA=0dB		-2.8		dBm
		f_{IN} = 2610 MHz, DSA=0dB		-1.8		dBm
		f_{IN} = 3610 MHz, DSA=0dB		-0.4		dBm
		f_{IN} = 4910 MHz, DSA=0dB		0.1		dBm
$P_{FS\_CW,MAX}$	MAX Full scale input power - relaibility limited, at device pins	f_{IN} = 830 MHz		16.7		dBm
		f_{IN} = 1760 MHz		17.0		dBm
		f_{IN} = 2610 MHz		18		dBm
		f_{IN} = 3610 MHz		18.5		dBm
		f_{IN} = 4910 MHz		19.3		dBm
S11	Input Return Loss	with matching network		-12.0		dB
ATT_{range}	DSA Attenuation range			25.0		dB
ATT_{step}	DSA Attenuation step			0.5		dB
	DSA Attenuation step accuracy	Delta=Gatt(X)-Gatt(X-1), F_{in}=3610MHz, after calibration		±0.1		dB
	DSA Gain Steps Phase accuracy any 8dB range	F_{in}=3610MHz, after calibration		±0.9		deg
	DSA Gain Steps Phase accuracy any 8dB range	F_{in}=4910MHz, after calibration		±1.8		deg
G_{flat}	Gain flatness	Measured Over 80MHz BW		0.2		dB
		Measured Over 200MHz BW		0.5		dB
		Measured Over 400MHz BW		1.1		dB
NSD	Noise Density (small signal)	f_{IN} = 830 MHz, DSA = 4dB (2)		-155.2		dBFS/Hz
		f_{IN} = 1760 MHz, DSA = 4dB (2)		-155.0		dBFS/Hz
		f_{IN} = 2610 MHz, DSA = 4dB (2)		-154.4		dBFS/Hz
		f_{IN} = 3610 MHz, DSA = 4dB (2)		-154.1		dBFS/Hz
		f_{IN} = 4910 MHz, DSA = 4dB (2)		-155.1		dBFS/Hz
NSD	Noise Density (small signal)	f_{IN} = 830 MHz, 4<=Atten<=22		-156.0		dBFS/Hz
		fIN = 1760 MHz, 4<=Atten<=22		-155.8		dBFS/Hz
		f_{IN} = 2610 MHz, 4<=Atten<=22		-155.7		dBFS/Hz
		f_{IN} = 3610 MHz, 4<=Atten<=22		-155.4		dBFS/Hz
		f_{IN} = 4910 MHz, 4<=Atten<=22		-155.8		dBFS/Hz
NF_{min}	Noise Figure min DSA Atten=0 - 3dB	f_{IN} = 830 MHz		19.1		dB
		f_{IN} = 1760 MHz		19.0		dB
		f_{IN} = 2610 MHz		20.9		dB
		f_{IN} = 3610 MHz		22.8		dB
		f_{IN} = 4910 MHz		22.4		dB
NF	Noise Figure DSA Atten=4dB	f_{IN} = 830 MHz (3)		20.0		dB
		f_{IN} = 1760 MHz (3)		20.6		dB
		f_{IN} = 2610 MHz (3)		21.9		dB
		f_{IN} = 3610 MHz (3)		23.5		dB
		f_{IN} = 4910 MHz (3)		24.4		dB

(1) The minimum input fullscale is with 3dB digital gain. The noise figure remains constant over the digital gain range.
(2) From DSA = 3dB down to 0dB, NSD increases 1dB per DSA dB
(3) NF increase 1dB per DSA 1dB above DSA = 3dB

RF ADC Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; RX Output Rate = 491.52MSPS, f_{ADC} = 2949.12MSPS; Internal PLL, f_{REF} = 491.52MSPS; nominal power supplies; DSA Setting =4dB; SerDes rate =24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
NF_{max}	Noise Figure DSA Atten=20dB	f_{IN} = 830 MHz		34.7		dB
		f_{IN} = 1760 MHz		35.2		dB
		f_{IN} = 2610 MHz		36.0		dB
		f_{IN} = 3610 MHz		37.3		dB
		f_{IN} = 4910 MHz		37.6		dB
IMD3	3rd order intermodulation 2 tones at at f_{IN} ± 10MHz -7dBFS each tone	f_{IN} = 840 MHz, 4<=Atten<=12		-82.4		dBc
		f_{IN} = 1770 MHz, 4<=Atten<=12		-84.1		dBc
		f_{IN} = 2610 MHz, 4<=Atten<=12		-74		dBc
		f_{IN} = 3610 MHz, 4<=Atten<=12		-77		dBc
		f_{IN} = 4920 MHz, 4<=Atten<=12		-75.9		dBc
SFDR	Spurious Free Dynamic Range within output bandwidth, A_{IN} = -3 dBFS	f_{IN} = 830 MHz		88.2		dBFS
		f_{IN} = 1760 MHz		80.6		dBFS
		f_{IN} = 2610 MHz		88		dBFS
		f_{IN} = 3610 MHz		84		dBFS
		f_{IN} = 4910 MHz		78.9		dBFS
HD2	2nd Harmonic Distortion A_{IN} = -3 dBFS(4)	f_{IN} = 830 MHz, with board trim, DDC Bypass (TI only test mode)		-85.5		dBFS
		f_{IN} = 1760 MHz, with board trim, DDC Bypass (TI only test mode)		-90.5		dBFS
		f_{IN} = 2610 MHz, with board trim, DDC Bypass (TI only test mode)		-88		dBFS
		f_{IN} = 3610 MHz, with board trim, DDC Bypass (TI only test mode)		-87		dBFS
		f_{IN} = 4910 MHz, with board trim, DDC Bypass (TI only test mode)		-84.2		dBFS
HD3	3rd Harmonic Distortion A_{IN} = -3 dBFS	f_{IN} = 830 MHz, DDC Bypass (TI only test mode)		-80.2		dBFS
		f_{IN} = 1760 MHz, DDC Bypass (TI only test mode)		-85.3		dBFS
		f_{IN} = 2610 MHz, DDC Bypass (TI only test mode)		-86		dBFS
		f_{IN} = 3610 MHz, DDC Bypass (TI only test mode)		-78		dBFS
		f_{IN} = 4910 MHz, DDC Bypass (TI only test mode)		-75.4		dBFS
HDn, n>3	SFDR excl. HD2 and HD3 A_{IN} = -3 dBFS	f_{IN} = 830 MHz		-88.2		dBFS
		f_{IN} = 1760 MHz		-80.6		dBFS
		f_{IN} = 2610 MHz		-88		dBFS
		f_{IN} = 3610 MHz		-84		dBFS
		f_{IN} = 4910 MHz		-81.7		dBFS
SFDR	Spurious Free Dynamic Range A_{IN} = -13 dBFS 0<=Atten<=16	f_{IN} = 830 MHz		89.2		dBFS
		f_{IN} = 1760 MHz		88.8		dBFS
		f_{IN} = 2610 MHz		95		dBFS
		f_{IN} = 3610 MHz		90		dBFS
		f_{IN} = 4910 MHz		89.8		dBFS

(4) After HD2 trim on specific printed circuit board.

RF ADC Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; RX Output Rate = 491.52MSPS, f_{ADC} = 2949.12MSPS; Internal PLL, f_{REF} = 491.52MSPS; nominal power supplies; DSA Setting =4dB; SerDes rate =24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
HD2	2nd Harmonic Distortion A_{IN} = -13 dBFS 0<=Atten<=16	f_{IN} = 830 MHz, with board trim, DDC Bypass (TI only test mode)		-79.0		dBFS
		f_{IN} = 1760 MHz, with board trim, DDC Bypass (TI only test mode)		-101.6		dBFS
		f_{IN} = 2610 MHz, with board trim, DDC Bypass (TI only test mode)		-100		dBFS
		f_{IN} = 3610 MHz, with board trim, DDC Bypass (TI only test mode)		-101		dBFS
		f_{IN} = 4910 MHz, with board trim, DDC Bypass (TI only test mode)		-99.1		dBFS
HD3	3rd Harmonic Distortion A_{IN} = -13 dBFS 0<=Atten<=16	f_{IN} = 830 MHz, DDC Bypass (TI only test mode)		-95.4		dBFS
		f_{IN} = 1760 MHz, DDC Bypass (TI only test mode)		-95.2		dBFS
		f_{IN} = 2610 MHz, DDC Bypass (TI only test mode)		-98		dBFS
		f_{IN} = 3610 MHz, DDC Bypass (TI only test mode)		-97		dBFS
		f_{IN} = 4910 MHz, DDC Bypass (TI only test mode)		-94.0		dBFS
HDn, n>3	SFDR excl. HD2 and HD3 A_{IN} = -13 dBFS 0<=Atten<=16	f_{IN} = 830 MHz		-89.2		dBFS
		f_{IN} = 1760 MHz		-88.8		dBFS
		f_{IN} = 2610 MHz		-95		dBFS
		f_{IN} = 3610 MHz		-90		dBFS
		f_{IN} = 4910 MHz		-90.0		dBFS
RX-RX/FB Isolation	Near Channel: 1RXIN to 2RXIN 3RXIN to 4RXIN 1FBIN to 1RXIN 2FBIN to 3RXIN	f_{IN} = 830 MHz		-76.6		dBc
		f_{IN} = 1760 MHz		-70.9		dBc
		f_{IN} = 2610 MHz		-73.5		dBc
		f_{IN} = 3610 MHz		-76.9		dBc
		f_{IN} = 4910 MHz		-65.3		dBc
TX-FB Isolation	Near Channel: 1TXOUT to 1FBIN 3TXOUT to 2FBIN	f_{IN} = 830 MHz		-84.3		dBc
		f_{IN} = 1760 MHz		-87.7		dBc
		f_{IN} = 2610 MHz		-85		dBc
		f_{IN} = 3610 MHz		-75		dBc
		f_{IN} = 4910 MHz		-81.5		dBc
TX-RX Isolation	1TXOUT to 1RXIN 3TXOUT to 2RXIN	f_{IN} = 830 MHz		-85.9		dBc
		f_{IN} = 1760 MHz		-86.9		dBc
		f_{IN} = 2610 MHz		-91		dBc
		f_{IN} = 3610 MHz		-83		dBc
		f_{IN} = 4910 MHz		-81.9		dBc

8.7 PLL/VCO/Clock Electrical Characteristics

Typical values at TA = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; Reference clock input frequency 491.52MHz (unless otherwise noted), $f_{DAC} = f_{VCO}$, $f_{OUT} = f_{DAC}/4$, normalized to f_{VCO}.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{VCO1}	VCO1 min frequency				7.3	GHz
	VCO1 max frequency		8.01			GHz
f_{VCO2}	VCO2 min frequency				8.8	GHz
	VCO2 max frequency		9.01			GHz
f_{VCO3}	VCO3 min frequency				9.7	GHz
	VCO3 max frequency		10.01			GHz
f_{VCO4}	VCO4 min frequency				11.6	GHz
	VCO4 max frequency		12.01			GHz
DIV_{DAC}	DAC sample rate divider			1 or 2		
DIV_{ADC}	ADC sample rate divider			2, 3, 4 or 6		
PN_{VCO}	Closed Loop Phase Noise F_{PLL} = 11.79848 GHz F_{REF}=491.52MHz	600kHz		-113		dBc/Hz
		800kHz		-116		dBc/Hz
		1MHz		-119		dBc/Hz
		1.8MHz		-125		dBc/Hz
		5MHz		-133		dBc/Hz
		50MHz		–141		dBc/Hz
	Closed Loop Phase Noise F_{PLL}=8.84736 GHz F_{REF}=491.52MHz	600kHz		-114		dBc/Hz
		800kHz		–118		dBc/Hz
		1MHz		–120		dBc/Hz
		1.8MHz		–127		dBc/Hz
		5MHz		–135		dBc/Hz
		50MHz		–142		dBc/Hz
	Closed Loop Phase Noise F_{PLL}= 9.8403 GHz F_{REF}=491.52MHz	600kHz		–113		dBc/Hz
		800kHz		–116		dBc/Hz
		1MHz		–119		dBc/Hz
		1.8MHz		–125		dBc/Hz
		5MHz		–134		dBc/Hz
		50MHz		–140		dBc/Hz
	Closed Loop Phase Noise F_{PLL}= 7.86432GHz F_{REF}=491.52MHz	600kHz		–116		dBc/Hz
		800kHz		–119		dBc/Hz
		1MHz		–122		dBc/Hz
		1.8MHz		–127		dBc/Hz
		5MHz		–136		dBc/Hz
		50MHz		–143		dBc/Hz
F_{rms}	Clock PLL integrated phase error(1)	f_{PLL}=11.79848 GHz, [1KHz, 100MHz]		-43.4		dBc/Hz
		f_{PLL}=8.8536 GHz, [1KHz, 100MHz]		-47.6		dBc/Hz
		f_{PLL}=9.8304 GHz, [1KHz, 100MHz]		-46.2		dBc/Hz
f_{PFD}	PFD frequency		100		500	MHz
PN_{pll_flat}	Normalized PLL flat Noise	f_{VCO} = 11796.48MHz		–226.5		dBc/Hz
F_{REF}	Input Clock frequency		0.1		12	GHz
V_{SS}	Input Clock level		0.6		1.8	Vppdiff
Coupling				AC Coupling Only		

(1) not including the reference clock contribution

PLL/VCO/Clock Electrical Characteristics (continued)

Typical values at TA = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; Reference clock input frequency 491.52MHz (unless otherwise noted), $f_{DAC} = f_{VCO}$, $f_{OUT} = f_{DAC}/4$, normalized to f_{VCO}.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	REFCLK input impedance(2)	Parallel resistance		100		Ω
		Parallel capacitance		0.5		pF

(2) Refer to S11 data available from TI for impedance vs frequency

8.8 Digital Electrical Characteristics

Typical values at TA = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CML SerDes Inputs [8:1]SRX+/-						
V_{SRDIFF}	SerDes Receiver Input Amplitude	differential	100		1200	mVpp
V_{SRCOM}	SerDes Input Common Mode			400		mV
Z_{SRdiff}	SerDes Internal Differential Termination (1)			100		Ω
F_{SerDes}	SerDes Bit Rate	Full rate mode	19		29.5	Gbps
		Half rate mode	9.5		16.25	Gbps
		Quarter rate mode	4.75		8.125	Gbps
	Insertion Loss Tolerance (2)	Serdes supply = 1.8V		25		dB
TJ	Total Jitter Tolerance				0.42	UI
CML SerDes Outputs [8:1]STX+/-						
V_{STDIFF}	SerDes Transmitter Output Amplitude	differential	500		1000	mVpp
V_{STCOM}	SerDes Output Common Mode			450		mV
Z_{STdiff}	SerDes Output Impedance			100		Ω
TRF	Output rise and fall time	20-80%	8			ps
TEQS	Equalization range				7	dB
TTJ	Output total jitter				0.21	UI
CMOS I/O: GPIO{B/C/D/E}x, SPICLK, SPISDIO, SPISDO, SPISEN, RESETZ, BISTB0, BISTB1						
V_{IH}	High-Level Input Voltage		0.6×VDD1 P8GPIO			V
V_{IL}	Low-Level Input Voltage				0.4×VDD1 P8GPIO	V
I_{IH}	High-Level Input Current		–250		250	mA
I_{IL}	Low-Level Input Current		–250		250	mA
C_L	CMOS input capacitance			2		pF
V_{OH}	High-Level Input Voltage		VDD1P8G PIO–0.2			V
V_{OL}	Low-Level Input Voltage				0.2	V
Differential Inputs: SYSREF+/- Mode A						
$Clock_{MODE}$				PLL Clock Mode Only		
$F_{SYSREFMAX}$	SYSREF Input Frequency Maximum			40		MHz
$V_{SWINGSRMAX}$	SYSREF Input Swing Maximum			1.8		Vppdiff (3)
$V_{SWINGSRMIN}$	SYSREF Input Swing Minimum	f_{REF} < 500MHz		0.3		Vppdiff (3)
$V_{SWINGSRMIN}$	SYSREF Input Swing Minimum	f_{REF} > 500MHz		0.6		Vppdiff (3)
$V_{COMSRMAX}$	SYSREF Input Common Mode Voltage Maximum			0.8		V
$V_{COMSRMIN}$	SYSREF Input Common Mode Voltage Minimum			0.6		V
Z_T	Input termination	differential		100 (1)		Ω
C_L	Input capacitance	Each pin to GND		0.5		pF
LVDS Inputs: 0SYNCIN+/- and 1SYNCIN+/-						
V_{ICOM}	Input Common Voltage			1.2		V
V_{ID}	Differential Input Voltage swing			450		Vppdiff (3)
Z_T	Input termination	differential		100		Ω

(1) SYSREF termination is programmable between 100Ω, 150Ω and 300Ω
(2) Loss tolerance is bump to bump from STX to SRX
(3) Vppdiff is the difference between the maximum differential voltage (positive value) and minimum differential voltage (negative value).

Digital Electrical Characteristics (continued)

Typical values at TA = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LVDS Outputs: 0SYNCOUT+/- and 1SYNCOUT+/-						
V_{OCOM}	Output Common Voltage			1.2		V
V_{OD}	Differential Output Voltage swing			500		Vppdiff (3)
Z_T	Internal Termination			100		Ω

8.9 Power Supply Electrical Characteristics

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 737.28MSPS, f_{DAC} = 8847.36MSPS interleave mode; f_{ADC} = 2949.12MSPS; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 1: 4T2F - FDD FB 100% on, no RX TX/FB Rate: 491.52 Msps Single Band: 12x Int, FB 6x Dec f_{DAC} = 5898.24 SPS f_{ADC} = 2949.12MSPS f_{TX} = 1.85 GHz 64/66 coding, 16.22Gbps TX: 4-8-4-1, FB: 2-4-4-1		948.2		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			533.7		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVCO			77.3		mA
I_{VDD1P2}	Group 2A: VDD1P2FB + VDD1P2RX			299.4		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			804.5		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			49.1		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			2041.3		mA
P_{diss}	Power Dissipation			6027.1		mW

Power Supply Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 737.28MSPS, f_{DAC} = 8847.36MSPS interleave mode; f_{ADC} = 2949.12MSPS; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 2a: TDD 4T1F (RX Standby) Dual Band: 18x Int, FB 6x Dec, RX 24x Dec TX/FB Rate 491.52 Msps RX Rate 122.88 Msps f_{DAC} = 8847.36MSPS f_{ADC} = 2949.12MSPS f_{OUT}=f_{IN}= 1.9, 2.6 GHz 64/66 coding, 16.22Gbps TX: 8-16-4-1, FB: 2-4-4-1, RX: 2-16-16-1		863.4		mA
				717.2		mA
				75.3		mA
I_{VDD1P2}	Group 2A: VDD1P2FB + VDD1P2RX			187.5		mA
				1069.5		mA
				41.3		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			2733.3		mA
P_{diss}	Power Dissipation			6998.2		mW
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 2b: TDD 4R (TX Standby) Dual Band: 18x Int, FB 6x Dec, RX 24x Dec TX/FB Rate 491.52 Msps RX Rate 122.88 Msps f_{DAC} = 8847.36MSPS f_{ADC} = 2949.12MSPS f_{OUT}=f_{IN}= 1.9, 2.6 GHz 64/66 coding, 16.22Gbps TX: 8-16-4-1, FB: 2-4-4-1, RX: 2-16-16-1		785.7		mA
				773.9		mA
				74.6		mA
I_{VDD1P2}	Group 2A: VDD1P2FB + VDD1P2RX			592.5		mA
				173.5		mA
				40.8		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			1835.9		mA
P_{diss}	Power Dissipation			5562.1		mW
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 2c: 4T4R - TDD 1F shared with RX TX 75%, RX 25%, FB 75% Dual Band: 18x Int, FB 6x Dec, RX 24x Dec TX/FB Rate 491.52 Msps RX Rate 122.88 Msps f_{DAC} = 8847.36MSPS f_{ADC} = 2949.12MSPS f_{OUT}=f_{IN}= 1.9, 2.6 GHz 64/66 coding, 16.22Gbps TX: 8-16-4-1, FB: 2-4-4-1, RX: 2-16-16-1		844.0		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			731.4		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVCO			75.1		mA
I_{VDD1P2}	Group 2A: VDD1P2FB + VDD1P2RX			288.8		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			845.4		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			41.1		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			2508.9		mA
P_{diss}	Power Dissipation			6639.2		mW

Power Supply Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 737.28MSPS, f_{DAC} = 8847.36MSPS interleave mode; f_{ADC} = 2949.12MSPS; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 2d: FDD 4T4R Dual Band: 18x Int, FB 6x Dec, RX 24x Dec TX/FB Rate 491.52 Msps RX Rate 122.88 Msps f_{DAC} = 8847.36MSPS f_{ADC} = 2949.12MSPS f_{OUT}=f_{IN}= 1.9, 2.6 GHz 64/66 coding, 16.22Gbps TX: 8-16-4-1, FB: 2-4-4-1, RX: 2-16-16-1		1331.6		mA
				945.2		mA
				75.0		mA
I_{VDD1P2}	Group 2A: VDD1P2FB + VDD1P2RX			596.0		mA
				1084.2		mA
				41.7		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			3354.5		mA
P_{diss}	Power Dissipation			9318.3		mW
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 3: 4T4R2F - FDD FB 100% on TX Dual Band: 12x Int, FB 6x Dec RX Dual Band: RX 24x TX/FB Rate 491.52 Msps RX Rate 122.88 Msps f_{DAC} = 11796.48 MSPS f_{ADC} = 2949.12 MSPS f_{TX} = 1.85 + 2.15 GHz f_{RX} = 1.75 + 1.88 GHz 64/66 coding, 16.22Gbps TX: 8-16-4-1, FB: 2-4-4-1, RX: 2-16-16-1		1668.6		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			965.1		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVCO			77.6		mA
I_{VDD1P2}	Group 2A: VDD1P2FB + VDD1P2RX			893.4		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			879.5		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			50.7		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			3826.9		mA
P_{diss}	Power Dissipation			10513.0		mW
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 4: 4T4R2F - FDD FB 100% on 7.5 GSPS DAC, 2.5 GSPS ADC Single Band: 15x Int, FB 5x Dec Dual Band: RX 20x TX/FB Rate 491.52 Msps RX Rate 122.88 Msps f_{DAC} = 7372.8 MSPS f_{ADC} = 2457.6 MSPS f_{TX} = 1.85 + 2.15 GHz f_{RX} = 1.75 + 1.88 GHz 64/66 coding, 16.22Gbps TX: 4-8-4-1, FB: 2-4-4-1, RX: 2-16-16-1		1611.5		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			694.5		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVCO			72.8		mA
I_{VDD1P2}	Group 2A: VDD1P2FB + VDD1P2RX			768.5		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			940.5		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			45.5		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			3000.5		mA
P_{diss}	Power Dissipation			9087.4		mW

Power Supply Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 737.28MSPS, f_{DAC} = 8847.36MSPS interleave mode; f_{ADC} = 2949.12MSPS; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 5a: TDD 4T1F (RX Standby) Single Band: 12x Int, FB 3x Dec, RX 6x Dec TX/FB Rate = 983.04 Msps RX Rate 491.52 Msps f_{DAC} = 11796.48 MSPS f_{ADC} = 2949.12 MSPS fTX = 3.5 GHz fRX =3.5 GHz 64/66 coding, 16.22Gbps TX: 8-8-2-1, FB: 4-4-4-2, RX: 4-8-4-1		860.0		mA
				790.2		mA
				78.0		mA
I_{VDD1P2}	Group 2A: VDD1P2FB + VDD1P2RX			185.0		mA
				849.6		mA
				44.3		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			2849.7		mA
P_{diss}	Power Dissipation			6970.0		mW
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 5b: TDD 4R (TX Standby) Single Band: 12x Int, FB 3x Dec, RX 6x Dec TX/FB Rate = 983.04 Msps RX Rate 491.52 Msps f_{DAC} = 11796.48 MSPS f_{ADC} = 2949.12 MSPS fTX = 3.5 GHz fRX =3.5 GHz 64/66 coding, 16.22Gbps TX: 8-8-2-1, FB: 4-4-4-2, RX: 4-8-4-1		779.1		mA
				846.6		mA
				77.3		mA
I_{VDD1P2}	Group 2A: VDD1P2FB + VDD1P2RX			585.9		mA
				185.3		mA
				43.8		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			1831.8		mA
P_{diss}	Power Dissipation			5691.9		mW
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 5c: 4T4R - TDD 1F shared with RX TX 75%, RX 25%, FB 75% Single Band: 12x Int, FB 3x Dec, RX 6x Dec TX/FB Rate = 983.04 Msps RX Rate 491.52 Msps f_{DAC} = 11796.48 MSPS f_{ADC} = 2949.12 MSPS f_{TX} = 3.5 GHz f_{RX} =3.5 GHz 64/66 coding, 16.22Gbps TX: 8-8-2-1, FB: 4-4-4-2, RX: 4-8-4-1		839.7		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			804.3		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVCO			77.8		mA
I_{VDD1P2}	Group 2A: VDD1P2FB + VDD1P2RX			285.2		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			683.5		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			44.1		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			2595.2		mA
P_{diss}	Power Dissipation			6650.4		mW

Power Supply Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 737.28MSPS, f_{DAC} = 8847.36MSPS interleave mode; f_{ADC} = 2949.12MSPS; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 5d: FDD 4T4R Single Band: 12x Int, FB 3x Dec, RX 6x Dec TX/FB Rate = 983.04 Msps RX Rate 491.52 Msps f_{DAC} = 11796.48 MSPS f_{ADC} = 2949.12 MSPS fTX = 3.5 GHz fRX =3.5 GHz 64/66 coding, 16.22Gbps TX: 8-8-2-1, FB: 4-4-4-2, RX: 4-8-4-1		1330.4		mA
				911.9		mA
				77.7		mA
I_{VDD1P2}	Group 2A: VDD1P2FB + VDD1P2RX			605.7		mA
				882.2		mA
				47.0		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			3358.4		mA
P_{diss}	Power Dissipation			9040.1		mW
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 6a: TDD 4T1FB (RX in Standby) TX 9G and FB 3G -16bit: 368.64M; DSA = 6dB, interleave mode RX 3G : 368.64M. 16 bit, Standby Serdes: 25gbps) -> 2 lanes for Rx/FB (lane shared) and 2lanes for Tx		667.0		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			431.0		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVCO			75.0		mA
I_{VDD1P2}	Group 2A: VDD1P2FB + VDD1P2RX			210.0		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			677.0		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			39.0		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			2152.0		mA
P_{diss}	Power Dissipation			5162.0		mW
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 6b: TDD 4R (TX in Standby) TX 9G and FB 3G -16bit: 368.64M; DSA = 6dB, interleave mode, Standby RX 3G : 368.64M. 16 bit Serdes: 25gbps) -> 2 lanes for Rx/FB (lane shared) and 2lanes for Tx		787.0		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			424.0		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVCO			75.0		mA
I_{VDD1P2}	Group 2A: VDD1P2FB + VDD1P2RX			582.0		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			169.0		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			39.0		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			1650.0		mA
P_{diss}	Power Dissipation			4747.0		mW
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 6c: TDD 4T4R1FB TX 9G and FB 3G -16bit: 368.64M; DSA = 6dB, interleave mode, 75% on RX 3G : 368.64M. 16 bit 25% on Serdes: 25gbps) -> 2 lanes for Rx/FB (lane shared) and 2lanes for Tx		697.0		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			429.0		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVCO			75.0		mA
I_{VDD1P2}	Group 2A: VDD1P2FB + VDD1P2RX			303.0		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			550.0		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			39.0		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			2026.0		mA
P_{diss}	Power Dissipation			5058.0		mW

Power Supply Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 737.28MSPS, f_{DAC} = 8847.36MSPS interleave mode; f_{ADC} = 2949.12MSPS; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 6d: FDD 4T4R TX 9G and FB 3G -16bit: 368.64M; DSA = 6dB, interleave mode, RX 3G : 368.64M. 16 bit Serdes: 25gbps) -> 2 lanes for Rx/FB (lane shared) and 2lanes for Tx		1100.4		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			676.7		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVCO			74.6		mA
I_{VDD1P2}	Group 2A: VDD1P2FB + VDD1P2RX			596.4		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			705.8		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			46.2		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			2473.5		mA
P_{diss}	Power Dissipation			7177.0		mW
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 7a: TDD 4T1FB (RX iin Standby) TX 9G and FB 3G -16bit: 368.64M; DSA = 6dB, non-interleave mode RX 3G : 368.64M. 16 bit, Standby Serdes: 25gbps) -> 2 lanes for Rx/FB (lane shared) and 2lanes for Tx		658.1		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			431.1		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVCO			75.3		mA
I_{VDD1P2}	Group 2A: VDD1P2FB + VDD1P2RX			189.2		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			1041.1		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			39.0		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			2208.7		mA
P_{diss}	Power Dissipation			5607.0		mW
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 7b: TDD 4R (TX in Standby) TX 9G and FB 3G -16bit: 368.64M; DSA = 6dB, , non-interleave mode, Standby RX 3G : 368.64M. 16 bit Serdes: 25gbps) -> 2 lanes for Rx/FB (lane shared) and 2lanes for Tx		789.5		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			471.3		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVCO			73.4		mA
I_{VDD1P2}	Group 2A: VDD1P2FB + VDD1P2RX			599.3		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			169.6		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			39.1		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			1645.3		mA
P_{diss}	Power Dissipation			4851.9		mW

Power Supply Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 737.28MSPS, f_{DAC} = 8847.36MSPS interleave mode; f_{ADC} = 2949.12MSPS; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 7c: TDD 4T4R1FB TX 9G and FB 3G -16bit: 368.64M; DSA = 6dB, , non-interleave mode, 75% on RX 3G : 368.64M. 16 bit 25% on Serdes: 25gbps) -> 2 lanes for Rx/FB (lane shared) and 2lanes for Tx		691.0		mA
I_{VDD1P8}	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			441.2		mA
I_{VDD1P8}	Group 3C: VDD1P8PLL + VDD1P8PLLVCO			74.8		mA
I_{VDD1P2}	Group 2A: VDD1P2FB + VDD1P2RX			291.7		mA
I_{VDD1P2}	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			823.2		mA
I_{VDD1P2}	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			39.0		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			2067.9		mA
P_{diss}	Power Dissipation			5418.2		mW
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 7d: FDD 4T4R1FB TX 9G and FB 3G -16bit: 368.64M; DSA = 6dB, , non-interleave mode, RX 3G : 368.64M. 16 bit Serdes: 25gbps) -> 2 lanes for Rx/FB (lane shared) and 2lanes for Tx		1283.8		mA
I_{VDD1P8}	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			752.0		mA
I_{VDD1P8}	Group 3C: VDD1P8PLL + VDD1P8PLLVCO			74.6		mA
I_{VDD1P2}	Group 2A: VDD1P2FB + VDD1P2RX			750.5		mA
I_{VDD1P2}	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			1077.6		mA
I_{VDD1P2}	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			47.7		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			2695.5		mA
P_{diss}	Power Dissipation			8475.5		mW
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 8: same configuration as mode 7, Sleep Mode. SLEEP pin is pull high.		20.3		mA
I_{VDD1P8}	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			292.8		mA
I_{VDD1P8}	Group 3C: VDD1P8PLL + VDD1P8PLLVCO			12.6		mA
I_{VDD1P2}	Group 2A: VDD1P2FB + VDD1P2RX			4.6		mA
I_{VDD1P2}	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			54.3		mA
I_{VDD1P2}	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			15.3		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			313.1		mA
P_{diss}	Power Dissipation			956.8		mW

Power Supply Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 737.28MSPS, f_{DAC} = 8847.36MSPS interleave mode; f_{ADC} = 2949.12MSPS; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 9: 4T4R2F - FDD FB 100% on TX Single Band: 24x Int, FB 12x Dec RX Single Band: RX 24x TX/FB Rate 245.76 Msps RX Rate 122.88 Msps f_{DAC} = 5898.24 MSPS f_{ADC} = 2949.12 MSPS f_{TX} = 0.85 GHz f_{RX} = 0.8 GHz 8/10 coding, 9.8304Gbps TX: 4-8-4-1, FB: 2-4-4-1, RX: 2-8-8-1		1593.2		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			840.6		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVCO			77.3		mA
I_{VDD1P2}	Group 2A: VDD1P2FB + VDD1P2RX			905.0		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			817.7		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			52.1		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			2405.2		mA
P_{diss}	Power Dissipation			8814.3		mW
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 10: 4T4R2F - FDD FB 100% on TX Single Band: 18x Int, FB 6x Dec RX Single Band: RX 12x TX/FB Rate 491.52 Msps RX Rate 245.76 Msps f_{DAC} = 8847.36 MSPS f_{ADC} = 2949.12 MSPS f_{TX} = 1.85 GHz f_{RX} = 1.75 GHz 8/10 coding, 9.8304Gbps TX: 8-8-2-1, FB: 4-4-2-1, RX: 4-8-4-1		1626.2		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			976.4		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVCO			74.6		mA
I_{VDD1P2}	Group 2A: VDD1P2FB + VDD1P2RX			902.7		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			1111.9		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			48.0		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			3578.9		mA
P_{diss}	Power Dissipation			10515.0		mW
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 11a: TDD 4T1F (RX Standby) Single Band: 9x Int, FB 3x Dec, RX 6x Dec TX/FB Rate = 983.04 Msps RX Rate 491.52 Msps f_{DAC} = 8847.36 MSPS, interleaved mode, f_{ADC} = 2949.12 MSPS fTX = 3.5 GHz fRX =3.5 GHz 64/66 coding, 16.22Gbps TX: 8-8-2-1, FB: 4-4-4-2, RX: 4-8-4-1		843.5		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			791.9		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVCO			74.6		mA
I_{VDD1P2}	Group 2A: VDD1P2FB + VDD1P2RX			193.2		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			703.7		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			45.3		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			2617.3		mA
P_{diss}	Power Dissipation			6564.0		mW

Power Supply Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 737.28MSPS, f_{DAC} = 8847.36MSPS interleave mode; f_{ADC} = 2949.12MSPS; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 11b: TDD 4R (TX Standby) Single Band: 9x Int, FB 3x Dec, RX 6x Dec TX/FB Rate = 983.04 Msps RX Rate 491.52 Msps f_{DAC} = 8847.36 MSPS, interleaved mode, f_{ADC} = 2949.12 MSPS fTX = 3.5 GHz fRX =3.5 GHz 64/66 coding, 16.22Gbps TX: 8-8-2-1, FB: 4-4-4-2, RX: 4-8-4-1		770.1		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			847.3		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVCO			73.8		mA
I_{VDD1P2}	Group 2A: VDD1P2FB + VDD1P2RX			596.3		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			178.8		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			44.0		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			1939.7		mA
P_{diss}	Power Dissipation			5772.6		mW
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 11c: TDD 4T4R (1F shared with RX, TX 75%, RX 25%, FB 75%) Single Band: 9x Int, FB 3x Dec, RX 6x Dec TX/FB Rate = 983.04 Msps RX Rate 491.52 Msps f_{DAC} = 8847.36 MSPS, interleaved mode, f_{ADC} = 2949.12 MSPS fTX = 3.5 GHz fRX =3.5 GHz 64/66 coding, 16.22Gbps TX: 8-8-2-1, FB: 4-4-4-2, RX: 4-8-4-1		825.1		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			805.7		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVCO			74.4		mA
I_{VDD1P2}	Group 2A: VDD1P2FB + VDD1P2RX			294.0		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			572.4		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			45.0		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			2447.9		mA
P_{diss}	Power Dissipation			6366.1		mW
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 11d: FDD 4T4R Single Band: 9x Int, FB 3x Dec, RX 6x Dec TX/FB Rate = 983.04 Msps RX Rate 491.52 Msps f_{DAC} = 8847.36 MSPS, interleaved mode, f_{ADC} = 2949.12 MSPS fTX = 3.5 GHz fRX =3.5 GHz 64/66 coding, 16.22Gbps TX: 8-8-2-1, FB: 4-4-4-2, RX: 4-8-4-1		1322.1		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			895.6		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVCO			74.6		mA
I_{VDD1P2}	Group 2A: VDD1P2FB + VDD1P2RX			606.9		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			730.2		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			46.2		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			3067.2		mA
P_{diss}	Power Dissipation			8546.4		mW

8.10 Timing Requirements

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 737.28MSPS, f_{DAC} = 8847.36MSPS; f_{ADC} = 2949.12MSPS; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

		MIN	NOM	MAX	UNIT
Timing: SYSREF+/-					
$t_{s(SYSREF)}$	Setup Time, SYSREF+/- Valid to Rising Edge of CLK+/-		50		ps
$t_{h(SYSREF)}$	Hold Time, SYSREF+/- Valid after Rising Edge of CLK+/-		50		ps
Timing: Serial ports					
$t_{s(SENB)}$	Setup Time, SENB to Rising Edge of SCLK		15		ns
$t_{h(SENB)}$	Hold Time, SENB after last Rising Edge of SCLK (1)		5 + t_{SCLK}		ns
$t_{s(SDIO)}$	Setup Time, SDIO valid to Rising Edge of SCLK		15		ns
$t_{h(SDIO)}$	Hold Time, SDIO valid after Rising Edge of SCLK		5		ns
$t_{(SCLK)\_W}$	SCLK period: registers write		25		ns
$t_{(SCLK)\_R}$	SCLK period: registers read		50		ns
$t_{(SCLK)\_R}$	SCLK period: temp sensor (2)		1000		ns
$t_{d(data\_out)}$	Minimum Data Output delay after Falling Edge of SCLK		0		ns
	Maximum Data Output delay after Falling Edge of SCLK		15		ns
t_{RESET}	Minimum RESETZ Pulse Width		1		ms

(1) SDEN\\ need to be held one more extra clock cycle with the last SCLK edge
(2) Temp sensor requires a maximum of 1MHz SCLK cycle.

8.11 Switching Characteristics

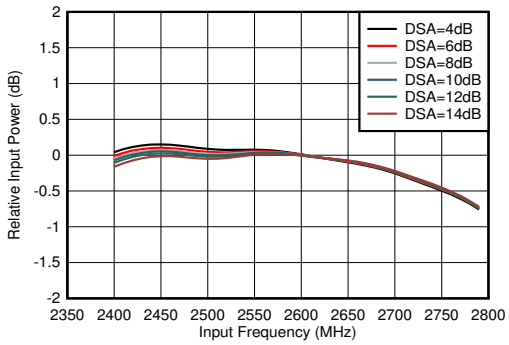
Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 737.28MSPS, f_{DAC} = 8847.36MSPS; f_{ADC} = 2949.12MSPS; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TX Channel Latency						
	SerDes Receiver Analog Delay	Full rate		2.8		ns
	JESD to TX output Latency	LMFSHd=2-8-8-1, 368.64 MSPS input rate, 24x Interpolation, Serdes rate = 16.22Gbps (JESD204C)		152		interface clock cycles
		LMFSHd=8-16-4-1, 491.52 MSPS 24x Interpolation, Serdes rate = 16.22Gbps (JESD204C)		176		
		LMFSHd=4-16-8-1, 245.76 MSPS 48x Interpolation, Serdes rate = 16.22Gbps (JESD204C)		124		
		LMFSHd=2-16-16-1, 122.88 MSPS 96x Interpolation, Serdes rate = 16.22Gbps (JESD204C)		97		
RX Channel Latency						
	SerDes Transmitter Analog Delay			3.6		ns
	RX input to JESD output Latency	LMFS=2-8-8-1, 368.64 MSPS, 8x Decimation, Serdes rate = 16.22Gbps (JESD204C)		118		
	RX input to JESD output Latency	LMFS=2-16-16-1, 122.88 MSPS, 24x Decimation, Serdes rate = 16.22Gbps (JESD204C)		92		interface clock cycles
		LMFS=4-16-8-1, 245.76 MSPS, 12x Decimation, Serdes rate = 16.22Gbps (JESD204C)		108		
		LMFS=4-8-4-1, 491.52 MSPS, 6x Decimation, Serdes rate = 16.22Gbps (JESD204C)		153		
FB Channel Latency						
	SerDes Transmitter Analog Delay			3.6		ns
	FB input to JESD output Latency	LMFS=1-2-8-1, 368.64 MSPS, 8x Decimation		151		interface clock cycles
		LMFS=2-4-4-1, 491.52 MSPS, 6x Decimation		177		

8.12 Typical Characteristics

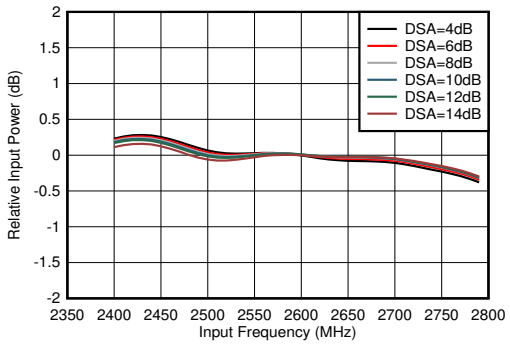
8.12.1 RX Typical Characteristics

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz, output sample rate = 491.52MSPS (decimate by 6), Internal PLL/VCO, f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB, unless otherwise noted.



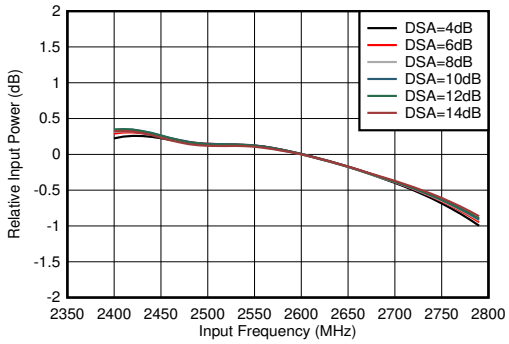
With matching, normalized to power at 2.6 GHz for each DSA setting

Figure 1. RX Inband Gain Flatness for Channel 1RX, f_{IN} = 2600 MHz



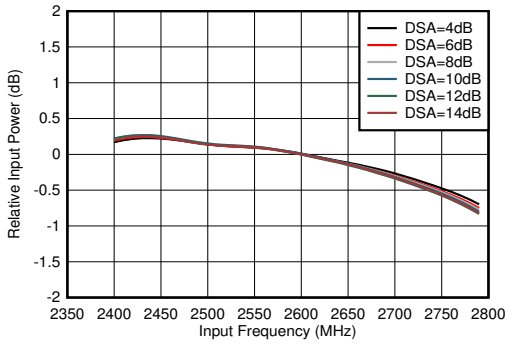
With matching, normalized to power at 2.6 GHz for each DSA setting

Figure 2. RX Inband Gain Flatness for Channel 2RX, f_{IN} = 2600 MHz



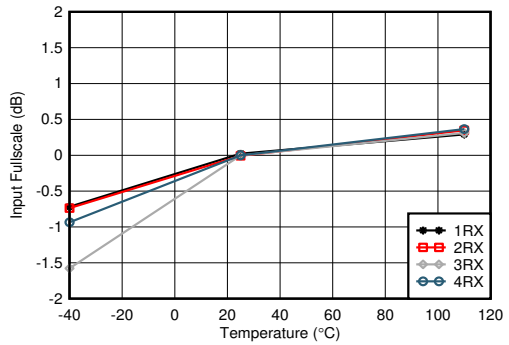
With matching, normalized to power at 2.6 GHz for each DSA setting

Figure 3. RX Inband Gain Flatness for Channel 3RX, f_{IN} = 2600 MHz



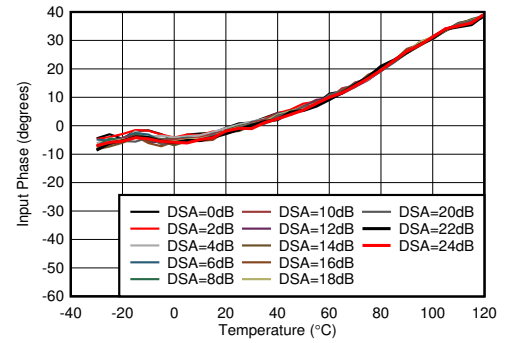
With matching, normalized to power at 2.6 GHz for each DSA setting

Figure 4. RX Inband Gain Flatness for Channel 4RX, f_{IN} = 2600 MHz



With 2.6 GHz matching, normalized to fullscale at 25°C for each channel

Figure 5. RX Input Fullscale vs Temperature and Channel at 2.6 GHz

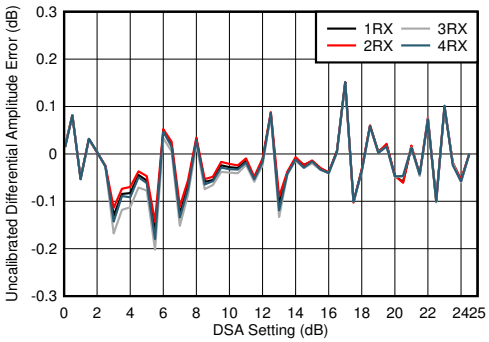


With 2.6 GHz matching, normalized to phase at 25°C

Figure 6. RX Input Phase vs Temperature and DSA at f_{OUT} = 2.6 GHz

RX Typical Characteristics (continued)

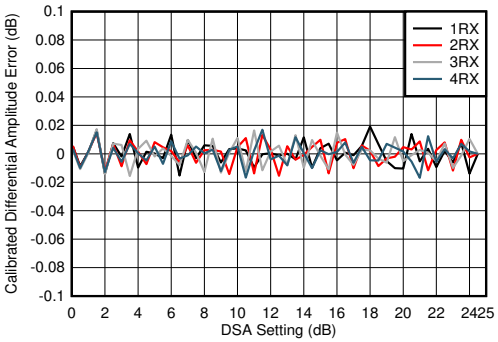
Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz, output sample rate = 491.52MSPS (decimate by 6), Internal PLL/VCO, f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB, unless otherwise noted.



With 2.6 GHz matching

Differential Amplitude Error = P_{IN}(DSA Setting – 1) – P_{IN}(DSA Setting) + 1

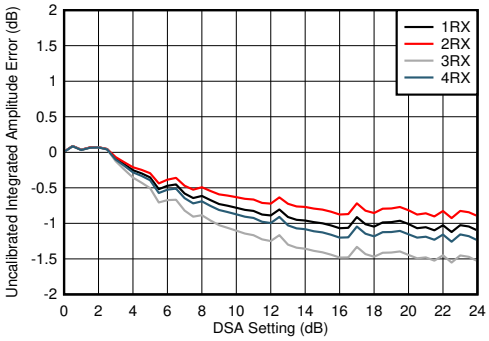
Figure 7. RX Uncalibrated Differential Amplitude Error vs DSA Setting at 2.6 GHz



With 2.6 GHz matching

Differential Amplitude Error = P_{IN}(DSA Setting – 1) – P_{IN}(DSA Setting) + 1

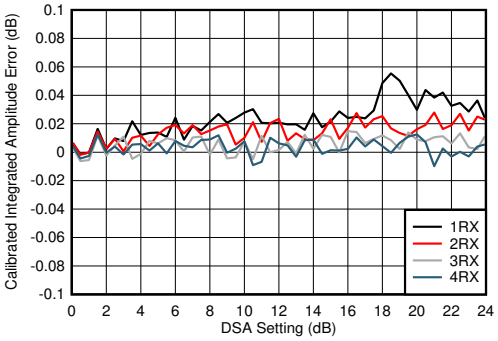
Figure 8. RX Calibrated Differential Amplitude Error vs DSA Setting at 2.6 GHz



With 2.6 GHz matching

Integrated Amplitude Error = P_{IN}(DSA Setting) – P_{IN}(DSA Setting = 0) + (DSA Setting)

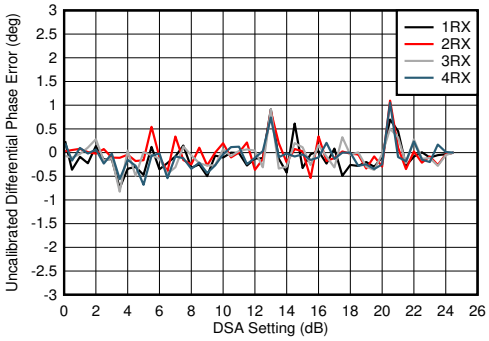
Figure 9. RX Uncalibrated Integrated Amplitude Error vs DSA Setting at 2.6 GHz



With 2.6 GHz matching

Integrated Amplitude Error = P_{IN}(DSA Setting) – P_{IN}(DSA Setting = 0) + (DSA Setting)

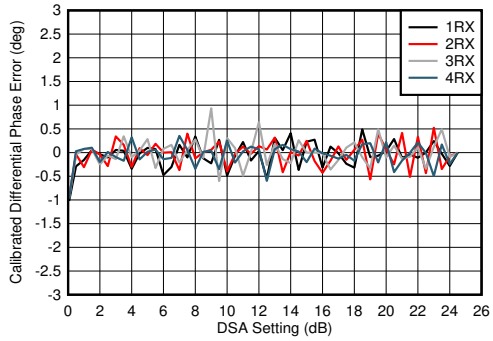
Figure 10. RX Calibrated Integrated Amplitude Error vs DSA Setting at 2.6 GHz



With 2.6 GHz matching

Differential Phase Error = $Phase_{IN}$(DSA Setting – 1) – $Phase_{IN}$(DSA Setting)

Figure 11. RX Uncalibrated Differential Phase Error vs DSA Setting at 2.6 GHz



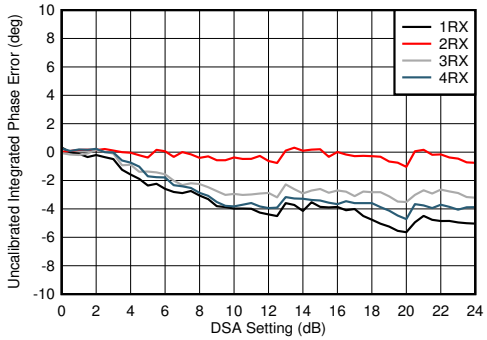
With 2.6 GHz matching

Differential Phase Error = $Phase_{IN}$(DSA Setting – 1) – $Phase_{IN}$(DSA Setting)

Figure 12. RX Calibrated Differential Phase Error vs DSA Setting at 2.6 GHz

RX Typical Characteristics (continued)

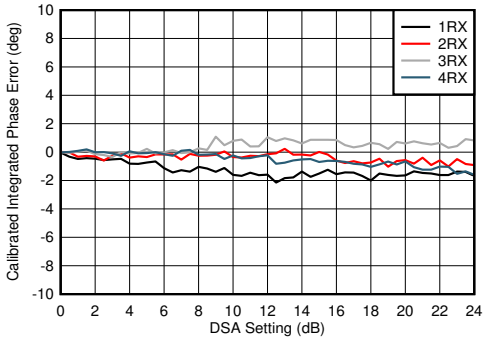
Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz, output sample rate = 491.52MSPS (decimate by 6), Internal PLL/VCO, f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB, unless otherwise noted.



With 2.6 GHz matching

Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

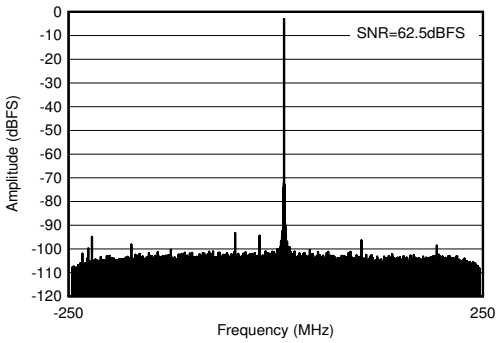
Figure 13. RX Uncalibrated Integrated Phase Error vs DSA Setting at 2.6 GHz



With 2.6 GHz matching

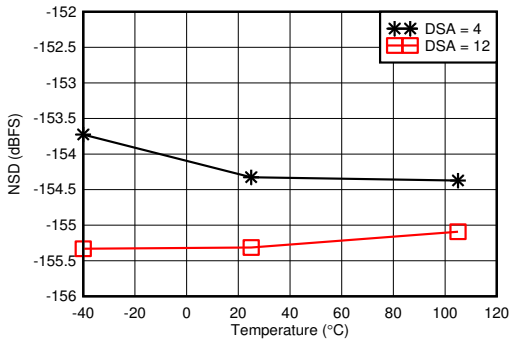
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

Figure 14. RX Calibrated Integrated Phase Error vs DSA Setting at 2.6 GHz



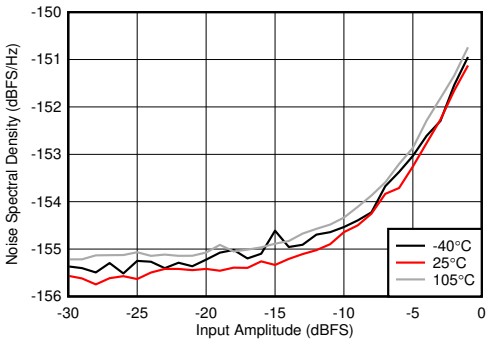
With 2.6 GHz matching, f_{IN} = 2610 MHz, A_{IN}= –3 dBFS

Figure 15. RX Output FFT at 2.6 GHz



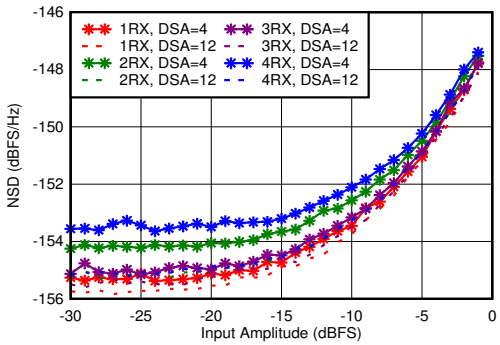
With 2.6 GHz matching, 12.5-MHz offset from tone

Figure 16. RX Noise Spectral Density vs Temperature at 2.6 GHz



With 2.6 GHz matching, DSA Setting = 12 dB, 12.5-MHz offset from tone

Figure 17. RX Noise Spectral Density vs Input Amplitude and Temperature at 2.6 GHz

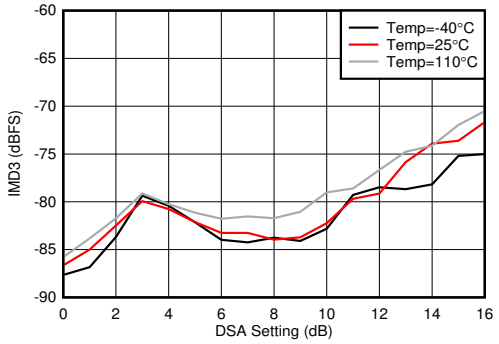


With 2.6 GHz matching, 12.5-MHz offset from tone

Figure 18. RX Noise Spectral Density vs Input Amplitude and Channel at 2.6 GHz

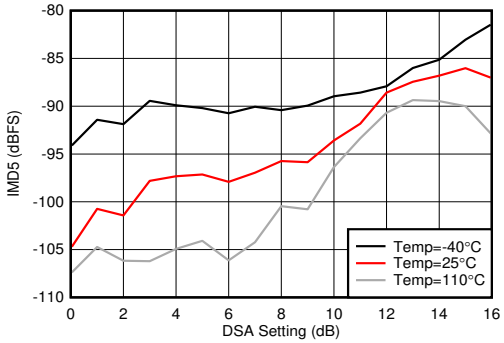
RX Typical Characteristics (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz, output sample rate = 491.52MSPS (decimate by 6), Internal PLL/VCO, f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB, unless otherwise noted.



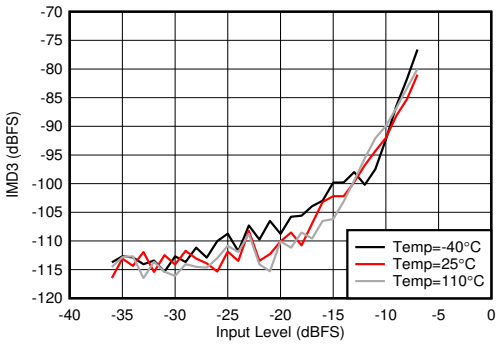
With 2.6 GHz matching, each tone –7 dBFS, tone spacing = 20 MHz

Figure 19. RX IMD3 vs DSA Setting and Temperature at 2.6 GHz



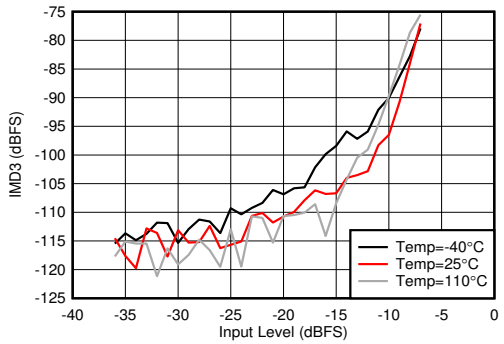
With 2.6 GHz matching, each tone –7 dBFS, tone spacing = 20 MHz

Figure 20. RX IMD5 vs DSA Setting and Temperature at 2.6 GHz



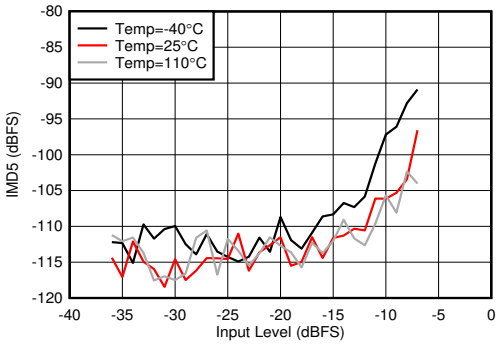
With 2.6 GHz matching, tone spacing = 20 MHz, DSA = 4 dB

Figure 21. RX IMD3 vs Input Level and Temperature at 2.6 GHz



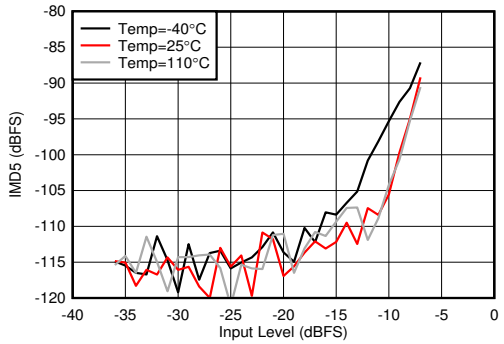
With 2.6 GHz matching, tone spacing = 20 MHz, DSA = 12 dB

Figure 22. RX IMD3 vs Input Level and Temperature at 2.6 GHz



With 2.6 GHz matching, tone spacing = 20 MHz, DSA = 12 dB

Figure 23. RX IMD5 vs Input Level and Temperature at 2.6 GHz

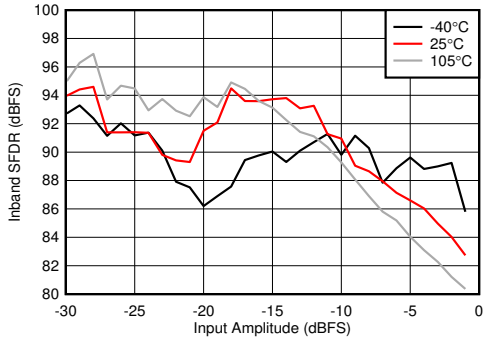


With 2.6 GHz matching, tone spacing = 20 MHz, DSA = 12 dB

Figure 24. RX IMD5 vs Input Level and Temperature at 2.6 GHz

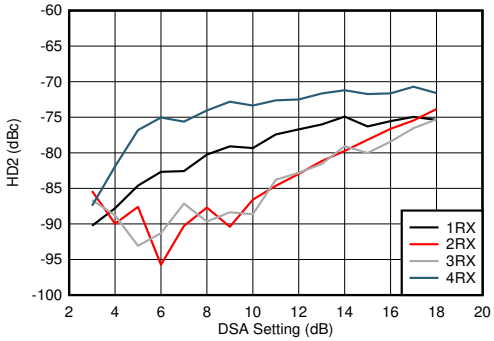
RX Typical Characteristics (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz, output sample rate = 491.52MSPS (decimate by 6), Internal PLL/VCO, f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB, unless otherwise noted.



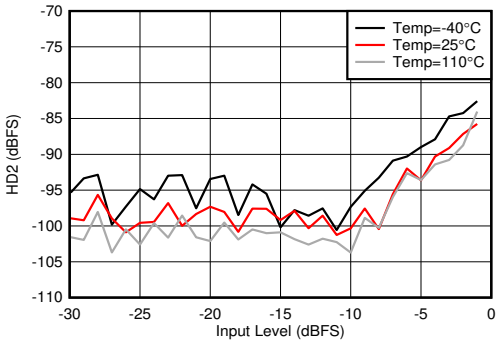
With 2.6 GHz matching, decimate by 8, DSA Setting = 12 dB

Figure 25. RX Inband SFDR (±150 MHz) vs Input Amplitude and Temperature at 2.6 GHz



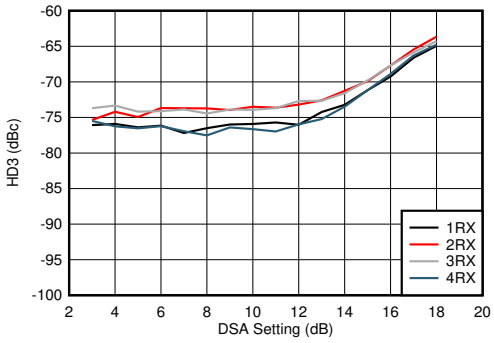
With 2.6 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 26. RX HD2 vs DSA Setting and Channel at 2.6 GHz



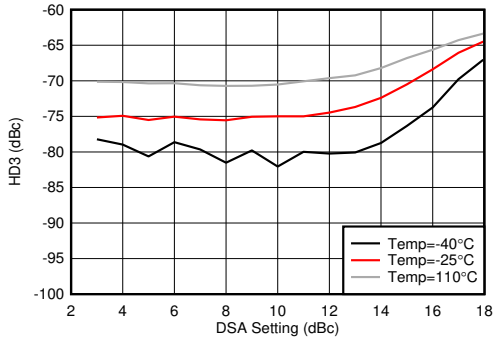
With 2.6 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 27. RX HD2 vs Input Level and Temperature at 2.6 GHz



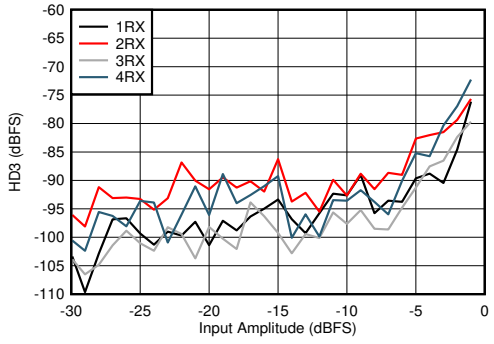
With 2.6 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 28. RX HD3 vs DSA Setting and Channel at 2.6 GHz



With 2.6 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 29. RX HD3 vs DSA Setting and Temperature at 2.6 GHz

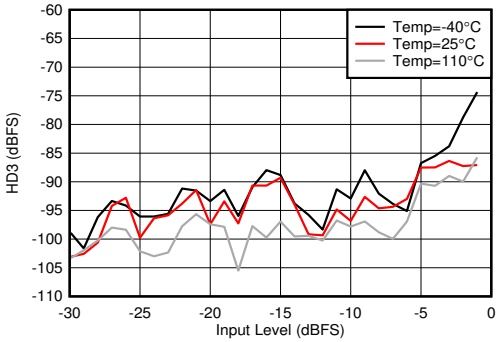


With 2.6 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 30. RX HD3 vs Input Level and Channel at 2.6 GHz

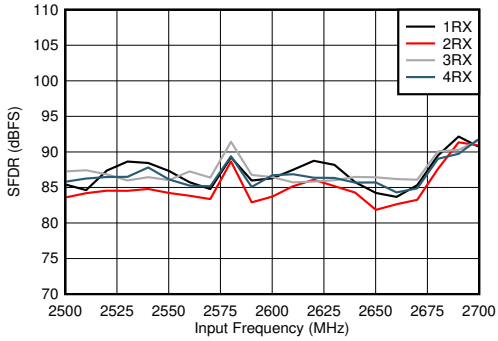
RX Typical Characteristics (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz, output sample rate = 491.52MSPS (decimate by 6), Internal PLL/VCO, f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB, unless otherwise noted.



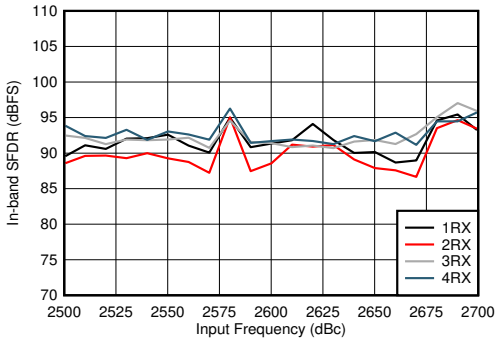
With 2.6 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 31. RX HD3 vs Input Level and Temperature at 2.6 GHz



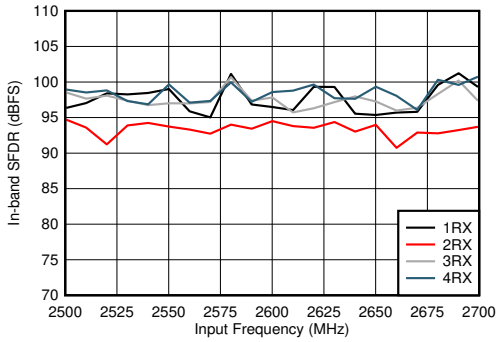
With 2.6 GHz matching

Figure 32. RX In-Band SFDR (±200 MHz) vs Frequency With A_{IN}= –1 dBFS at 2.6 GHz



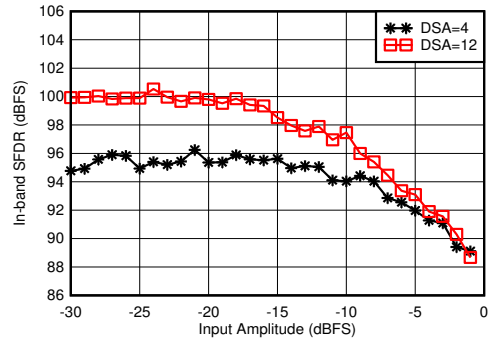
With 2.6 GHz matching

Figure 33. RX In-Band SFDR (±200 MHz) vs Frequency With A_{IN}= –6 dBFS at 2.6 GHz



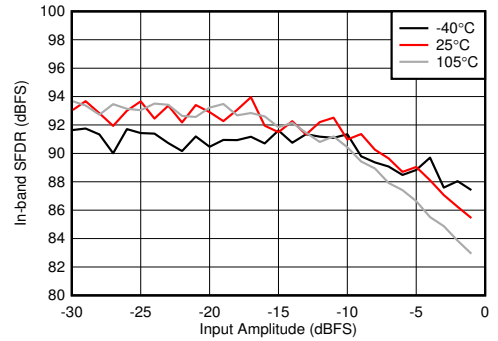
With 2.6 GHz matching

Figure 34. RX In-Band SFDR (±200 MHz) vs Frequency With A_{IN}= –12 dBFS at 2.6 GHz



With 2.6 GHz matching

Figure 35. RX In-Band SFDR (±200 MHz) vs Input Amplitude at 2.6 GHz

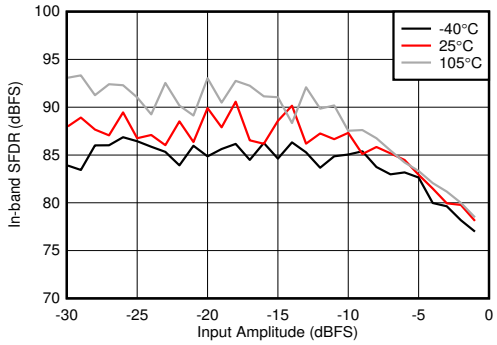


With 2.6 GHz matching

Figure 36. RX In-Band SFDR (±200 MHz) vs Input Amplitude and Temperature at 2.6 GHz

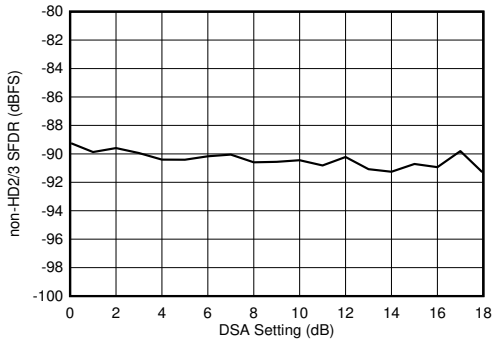
RX Typical Characteristics (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz, output sample rate = 491.52MSPS (decimate by 6), Internal PLL/VCO, f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB, unless otherwise noted.



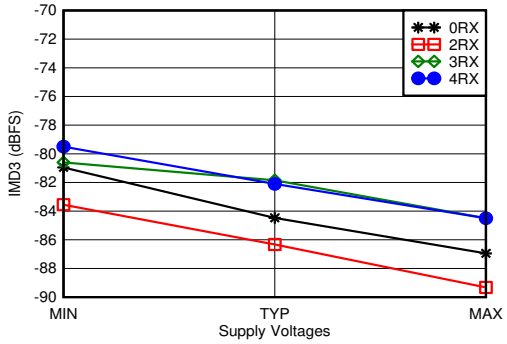
With 2.6 GHz matching, decimate by 4

Figure 37. RX In-Band SFDR (±300 MHz) vs Input Amplitude and Temperature at 2.6 GHz



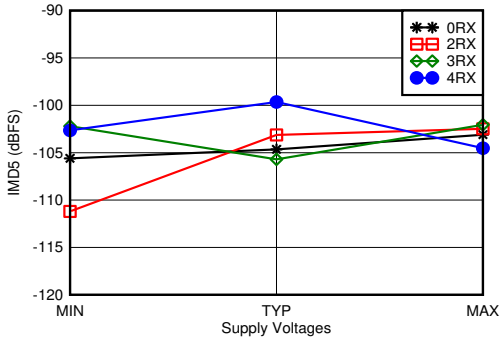
With 2.6 GHz matching

Figure 38. RX Non-HD2/3 vs DSA Setting at 2.6 GHz



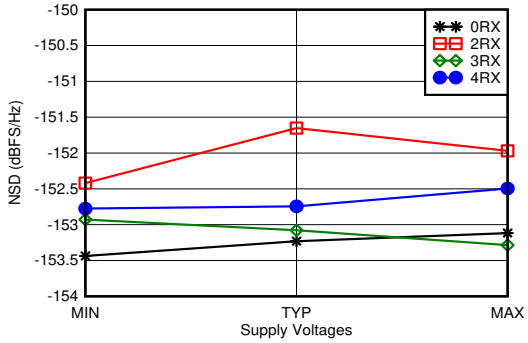
With 2.6 GHz matching, –7 dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

Figure 39. RX IMD3 vs Supply and Channel at 2.6 GHz



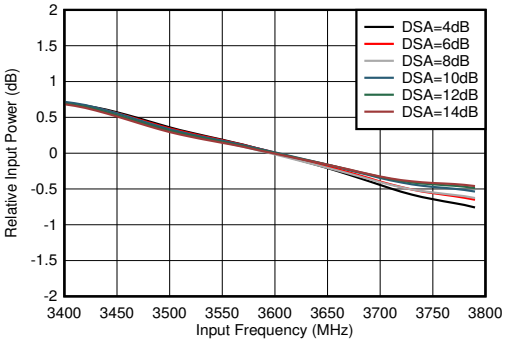
With 2.6 GHz matching, –7 dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

Figure 40. RX IMD5 vs Supply and Channel at 2.6 GHz



With 2.6 GHz matching, 12.5-MHz offset, all supplies at MIN, TYP, or MAX recommended operating voltages

Figure 41. RX Noise Spectral Density vs Supply and Channel at 2.6 GHz

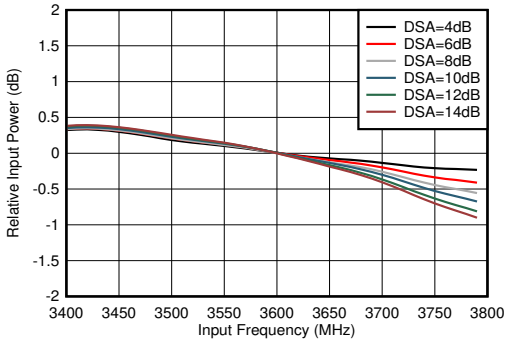


With 3.6 GHz matching, normalized to 3.6 GHz

Figure 42. RX In-Band Gain Flatness for Channel 1RX, f_{IN} = 3600 MHz

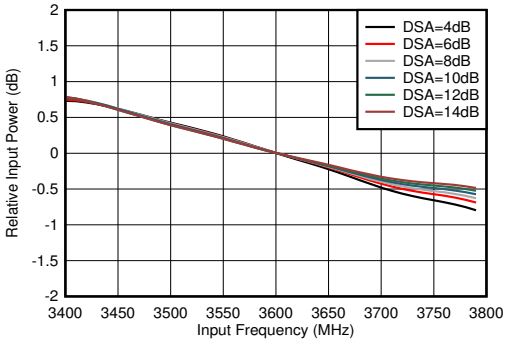
RX Typical Characteristics (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz, output sample rate = 491.52MSPS (decimate by 6), Internal PLL/VCO, f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB, unless otherwise noted.



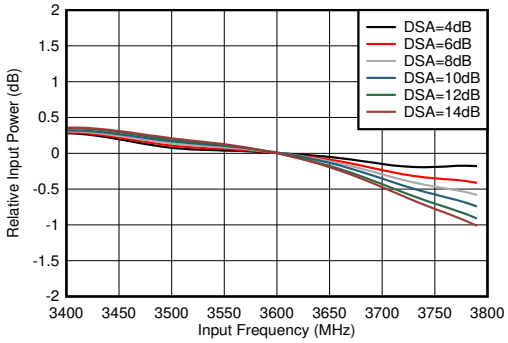
With 3.6 GHz matching, normalized to 3.6 GHz

Figure 43. RX In-Band Gain Flatness for Channel 2RX, f_{IN} = 3600 MHz



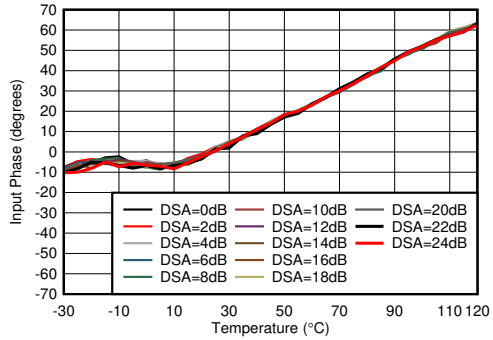
With 3.6 GHz matching, normalized to 3.6 GHz

Figure 44. RX In-Band Gain Flatness for Channel 3RX, f_{IN} = 3600 MHz



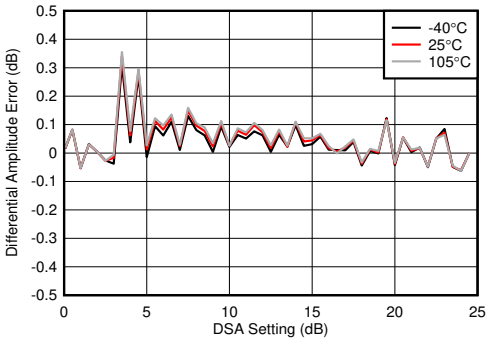
With 3.6 GHz matching, normalized to 3.6 GHz

Figure 45. RX In-Band Gain Flatness for Channel 4RX, f_{IN} = 3600 MHz



With 3.6 GHz matching, normalized to phase at 25°C

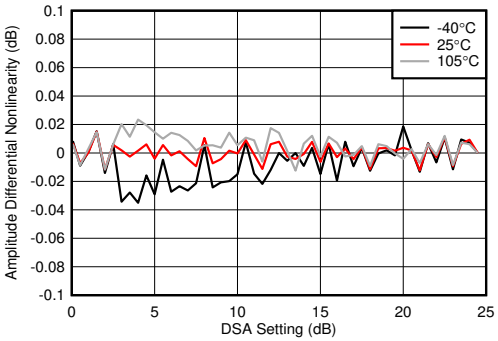
Figure 46. RX Input Phase vs Temperature at 3.6 GHz



With 3.6 GHz matching

Differential Amplitude Error = P_{IN}(DSA Setting – 1) – P_{IN}(DSA Setting) + 1

Figure 47. RX Uncalibrated Differential Amplitude Error vs DSA Setting at 3.6 GHz



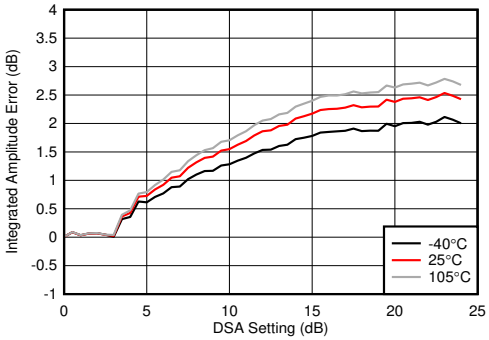
With 3.6 GHz matching

Differential Amplitude Error = P_{IN}(DSA Setting – 1) – P_{IN}(DSA Setting) + 1

Figure 48. RX Calibrated Differential Amplitude Error vs DSA Setting at 3.6 GHz

RX Typical Characteristics (continued)

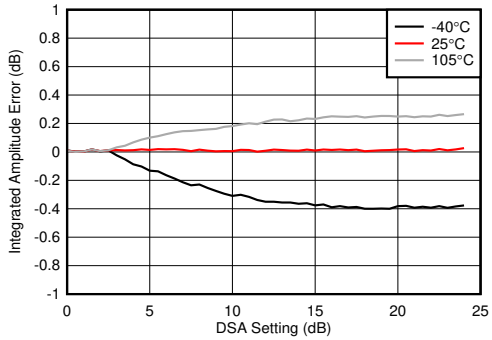
Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz, output sample rate = 491.52MSPS (decimate by 6), Internal PLL/VCO, f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB, unless otherwise noted.



With 3.6 GHz matching

Integrated Amplitude Error = P_{IN}(DSA Setting) – P_{IN}(DSA Setting = 0) + (DSA Setting)

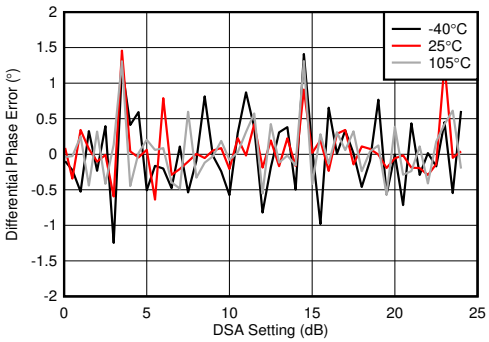
Figure 49. RX Uncalibrated Integrated Amplitude Error vs DSA Setting at 3.6 GHz



With 3.6 GHz matching

Integrated Amplitude Error = P_{IN}(DSA Setting) – P_{IN}(DSA Setting = 0) + (DSA Setting)

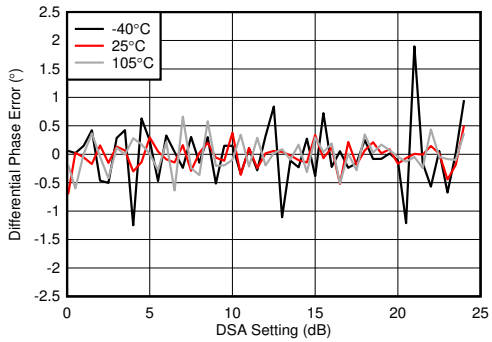
Figure 50. RX Calibrated Integrated Amplitude Error vs DSA Setting at 3.6 GHz



With 3.6 GHz matching

Differential Phase Error = $Phase_{IN}$(DSA Setting – 1) – $Phase_{IN}$(DSA Setting)

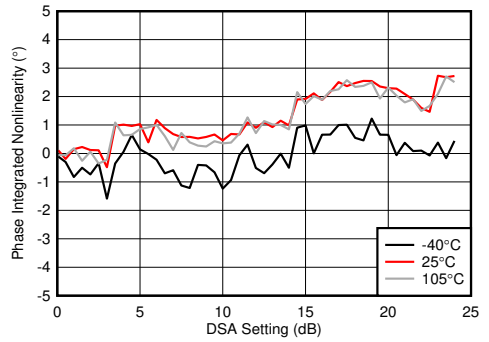
Figure 51. RX Uncalibrated Phase Error vs DSA Setting at 3.6 GHz



With 3.6 GHz matching

Differential Phase Error = $Phase_{IN}$(DSA Setting – 1) – $Phase_{IN}$(DSA Setting)

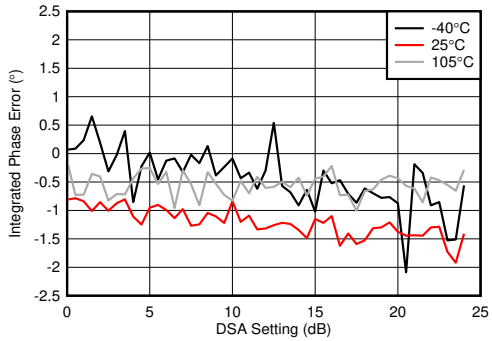
Figure 52. RX Calibrated Differential Phase Error vs DSA Setting at 3.6 GHz



With 3.6 GHz matching

Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

Figure 53. RX Uncalibrated Integrated Phase Error vs DSA Setting at 3.6 GHz



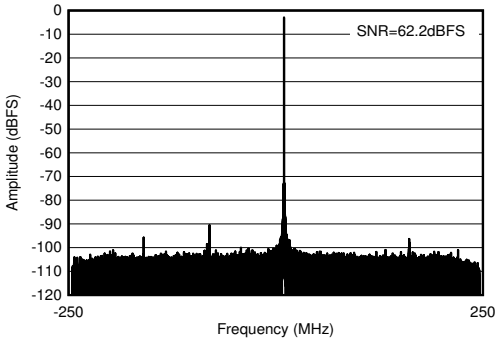
With 3.6 GHz matching

Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

Figure 54. RX Calibrated Integrated Phase Error vs DSA Setting at 3.6 GHz

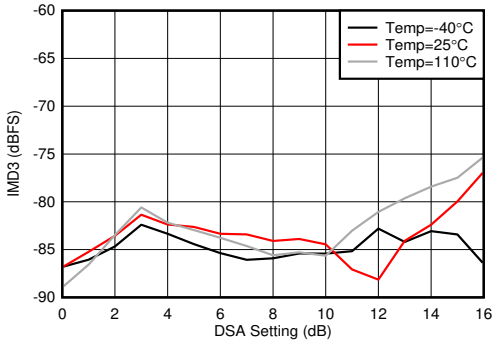
RX Typical Characteristics (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz, output sample rate = 491.52MSPS (decimate by 6), Internal PLL/VCO, f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB, unless otherwise noted.



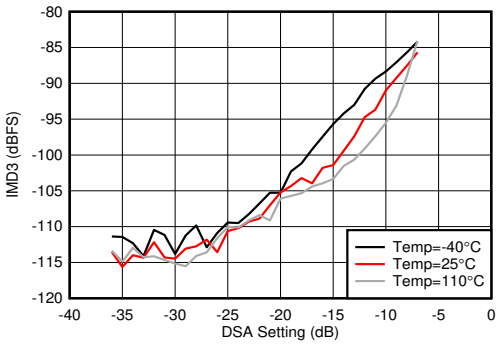
With 3.6 GHz matching , f_{IN} = 3610 MHz, A_{IN} = –3 dBFS

Figure 55. RX Output FFT at 3.6 GHz



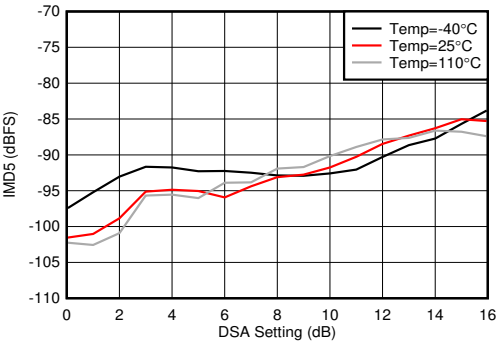
With 3.5 GHz matching, each tone at –7 dBFS, 20-MHz tone spacing

Figure 56. RX IMD3 vs DSA Setting and Temperature at 3.6 GHz



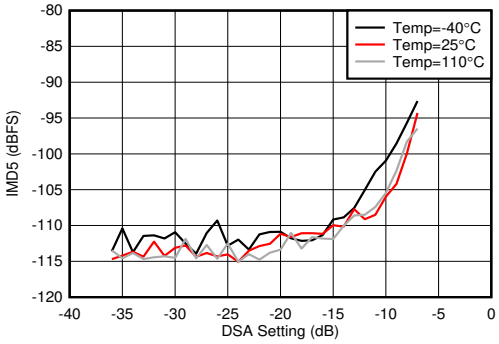
With 3.5 GHz matching, 20-MHz tone spacing

Figure 57. RX IMD3 vs Input Level and Temperature at 3.6 GHz



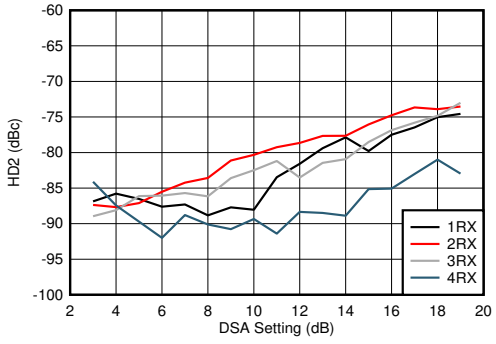
With 3.5 GHz matching, each tone at –7 dBFS, 20-MHz tone spacing

Figure 58. RX IMD5 vs DSA Setting and Temperature at 3.6 GHz



With 3.5 GHz matching, 20-MHz tone spacing

Figure 59. RX IMD5 vs Input Level and Temperature at 3.6 GHz

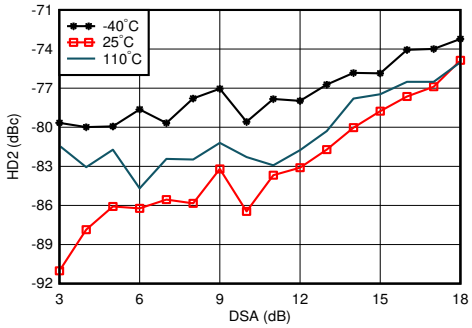


With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 60. RX HD2 vs DSA Setting and Channel at 3.6 GHz

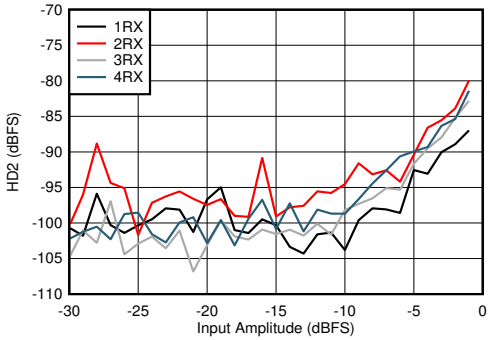
RX Typical Characteristics (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz, output sample rate = 491.52MSPS (decimate by 6), Internal PLL/VCO, f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB, unless otherwise noted.



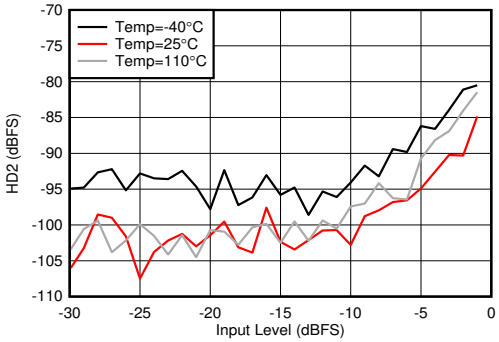
With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 61. RX HD2 vs DSA Setting and Temperature at 3.6 GHz



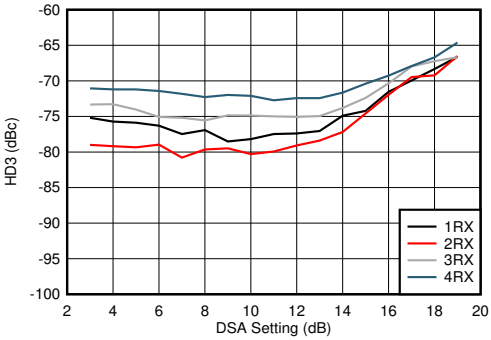
With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 62. RX HD2 vs Input Level and Channel at 3.6 GHz



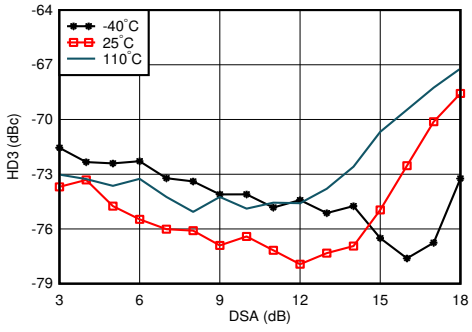
With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 63. RX HD2 vs Input Level and Temperature at 3.6 GHz



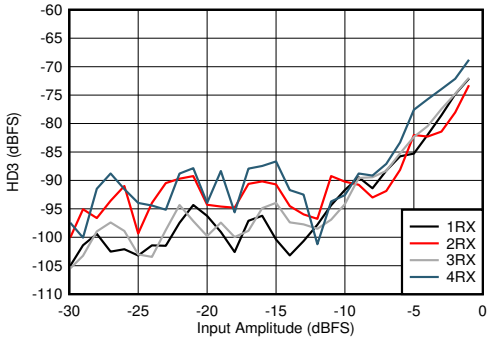
With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 64. RX HD3 vs DSA Setting and Channel at 3.6 GHz



With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 65. RX HD3 vs DSA Setting and Temperature at 3.6 GHz

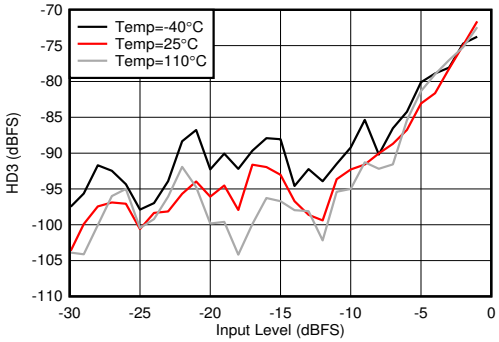


With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 66. RX HD3 vs Input Level and Channel at 3.6 GHz

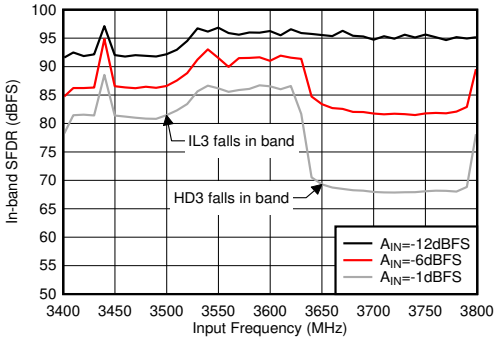
RX Typical Characteristics (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz, output sample rate = 491.52MSPS (decimate by 6), Internal PLL/VCO, f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB, unless otherwise noted.



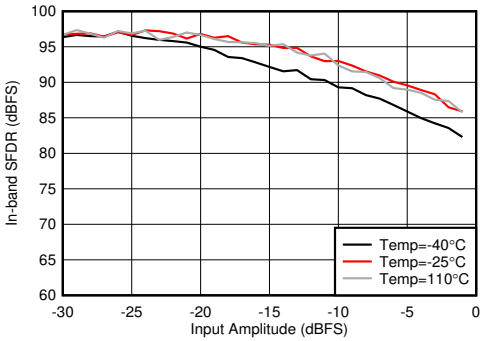
With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 67. RX HD3 vs Input Level and Temperature at 3.6 GHz



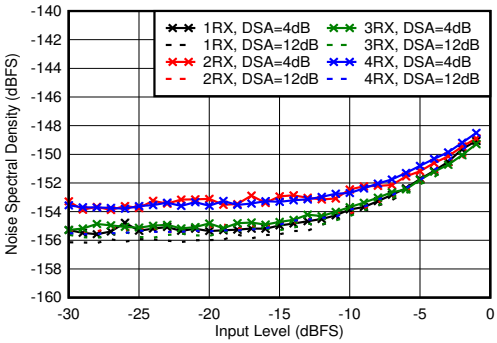
With 3.5 GHz matching

Figure 68. RX In-Band SFDR (±200 MHz) vs Frequency and Input Level at 3.6 GHz



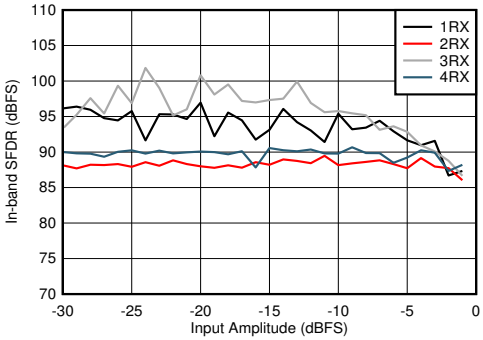
With 3.5 GHz matching

Figure 69. RX In-Band SFDR (±200 MHz) vs Input Level and Temperature at 3.6 GHz



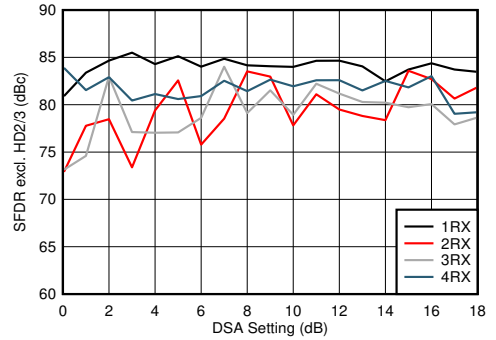
With 3.5 GHz matching, 12.5-MHz offset from tone

Figure 70. RX Noise Spectral Density vs Input Level and DSA Setting at 3.6 GHz



With 3.5 GHz matching

Figure 71. RX In-Band SFDR (±200 MHz) vs Input Level and Channel at 3.6 GHz

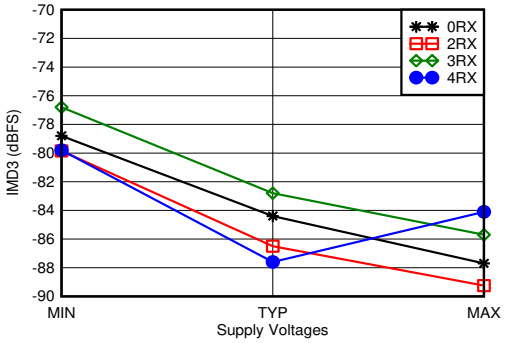


With 3.5 GHz matching

Figure 72. RX SFDR Excluding HD2/3 vs DSA Setting and Channel at 3.6 GHz

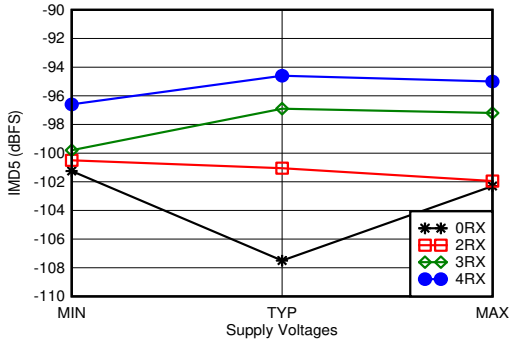
RX Typical Characteristics (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz, output sample rate = 491.52MSPS (decimate by 6), Internal PLL/VCO, f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB, unless otherwise noted.



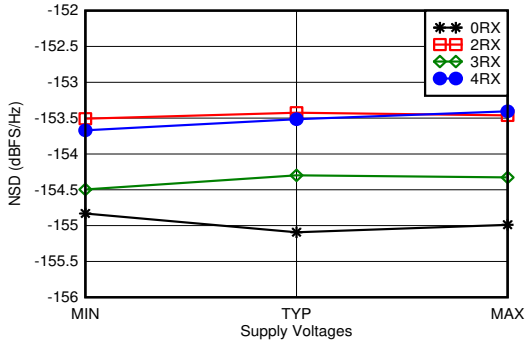
With 3.6 GHz matching, –7 dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

Figure 73. RX IMD3 vs Supply Voltage and Channel at 3.6 GHz



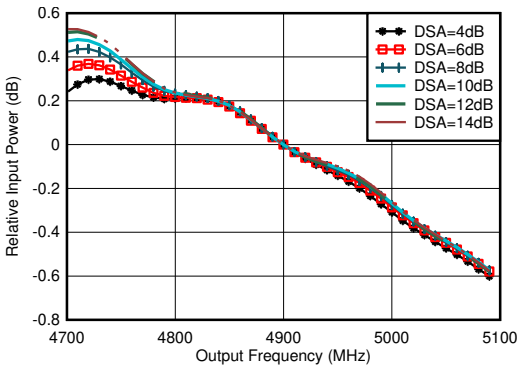
With 3.6 GHz matching, –7 dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

Figure 74. RX IMD5 vs Supply Voltage and Channel at 3.6 GHz



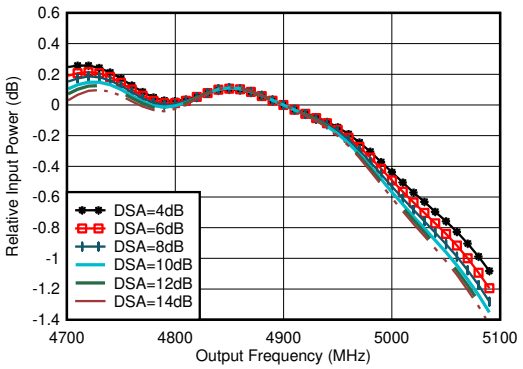
With 3.6 GHz matching, tone at –20 dBFS, 12.5-MHz offset frequency, all supplies at MIN, TYP, or MAX recommended operating voltages

Figure 75. RX Noise Spectral Density vs Supply Voltage and Channel at 3.6 GHz



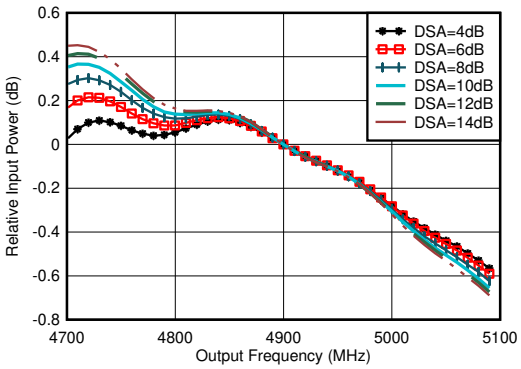
With matching, normalized to power at 4.9GHz for each DSA setting

Figure 76. RX Inband Gain Flatness for Channel 1RX, f_{IN} = 4900 MHz



With matching, normalized to power at 4.9GHz for each DSA setting

Figure 77. RX Inband Gain Flatness for Channel 2RX, f_{IN} = 4900 MHz

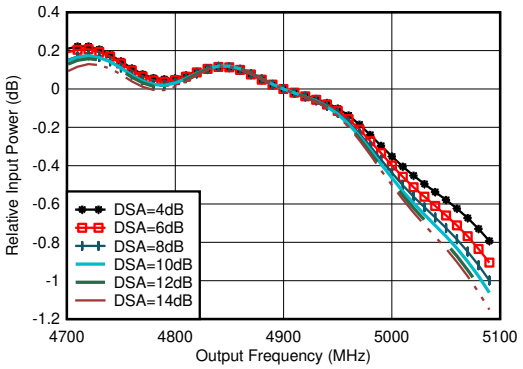


With matching, normalized to power at 4.9GHz GHz for each DSA setting

Figure 78. RX Inband Gain Flatness for Channel 3RX, f_{IN} = 4900 MHz

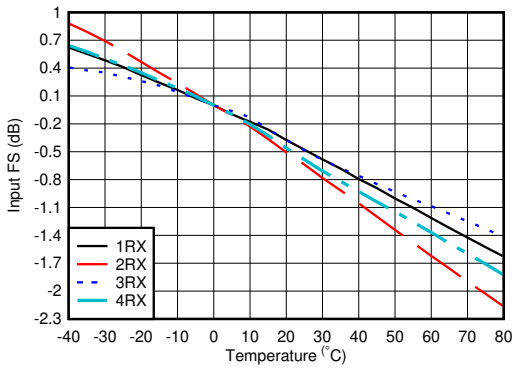
RX Typical Characteristics (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz, output sample rate = 491.52MSPS (decimate by 6), Internal PLL/VCO, f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB, unless otherwise noted.



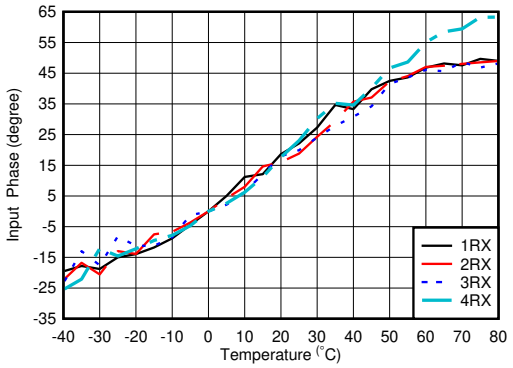
With matching, normalized to power at 4.9 GHz for each DSA setting

Figure 79. RX Inband Gain Flatness for Channel 4RX, f_{IN} = 4900 MHz



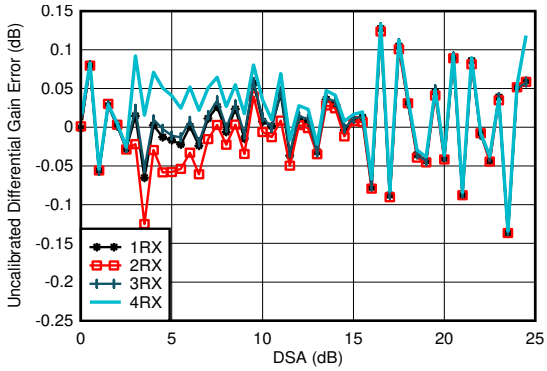
With 4.9 GHz matching, normalized to fullscale at 25°C for each channel

Figure 80. RX Input Fullscale vs Temperature and Channel at 4.9 GHz



With 4.9 GHz matching, normalized to phase at 25°C

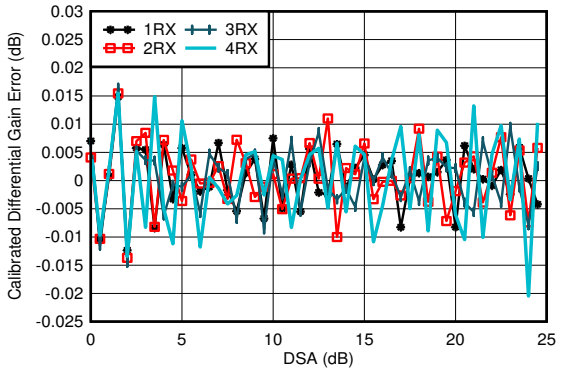
Figure 81. RX Input Phase vs Temperature and DSA at f_{OUT} = 4.9 GHz



With 4.9 GHz matching

Differential Amplitude Error = P_{IN}(DSA Setting – 1) – P_{IN}(DSA Setting) + 1

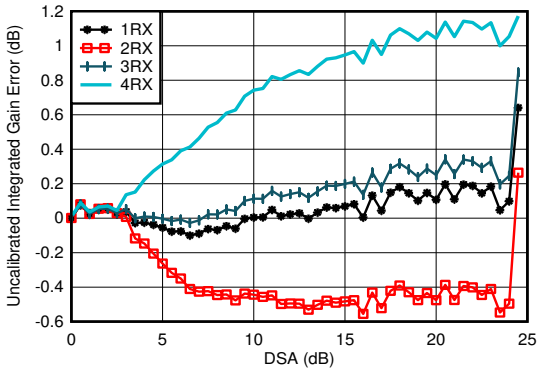
Figure 82. RX Uncalibrated Differential Amplitude Error vs DSA Setting at 4.9 GHz



With 4.9 GHz matching

Differential Amplitude Error = P_{IN}(DSA Setting – 1) – P_{IN}(DSA Setting) + 1

Figure 83. RX Calibrated Differential Amplitude Error vs DSA Setting at 4.9 GHz



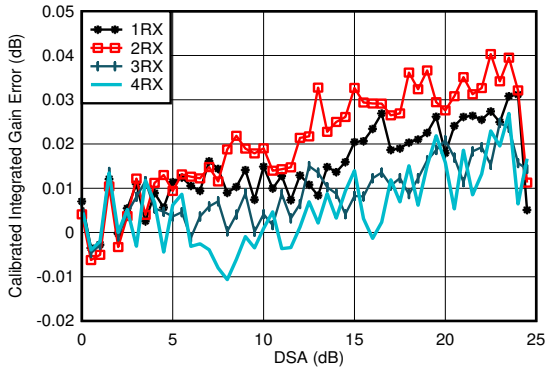
With 4.9 GHz matching

Integrated Amplitude Error = P_{IN}(DSA Setting) – P_{IN}(DSA Setting = 0) + (DSA Setting)

Figure 84. RX Uncalibrated Integrated Amplitude Error vs DSA Setting at 4.9 GHz

RX Typical Characteristics (continued)

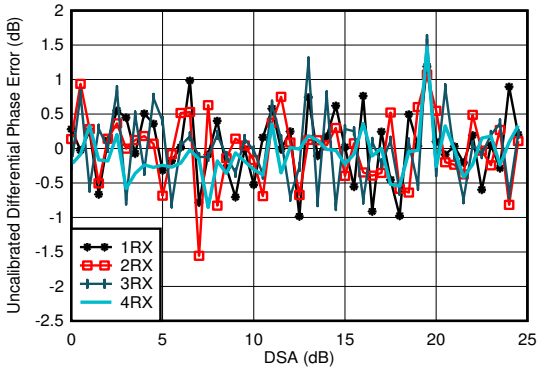
Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz, output sample rate = 491.52MSPS (decimate by 6), Internal PLL/VCO, f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB, unless otherwise noted.



With 4.9 GHz matching

Integrated Amplitude Error = P_{IN}(DSA Setting) – P_{IN}(DSA Setting = 0) + (DSA Setting)

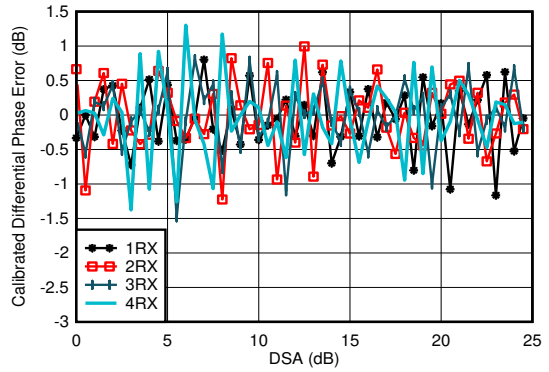
Figure 85. RX Calibrated Integrated Amplitude Error vs DSA Setting at 4.9 GHz



With 4.9 GHz matching

Differential Phase Error = $Phase_{IN}$(DSA Setting – 1) – $Phase_{IN}$(DSA Setting)

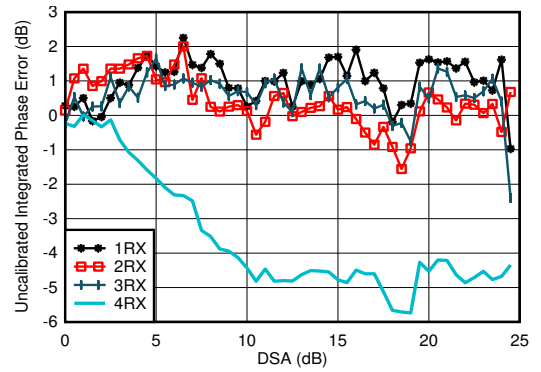
Figure 86. RX Uncalibrated Differential Phase Error vs DSA Setting at 4.9 GHz



With 4.9 GHz matching

Differential Phase Error = $Phase_{IN}$(DSA Setting – 1) – $Phase_{IN}$(DSA Setting)

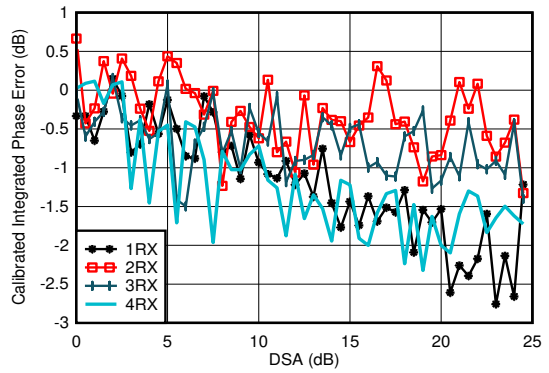
Figure 87. RX Calibrated Differential Phase Error vs DSA Setting at 4.9 GHz



With 4.9 GHz matching

Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

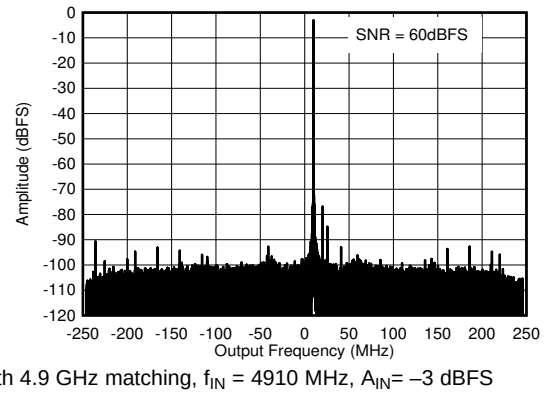
Figure 88. RX Uncalibrated Integrated Phase Error vs DSA Setting at 4.9 GHz



With 4.9 GHz matching

Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

Figure 89. RX Calibrated Integrated Phase Error vs DSA Setting at 4.9 GHz

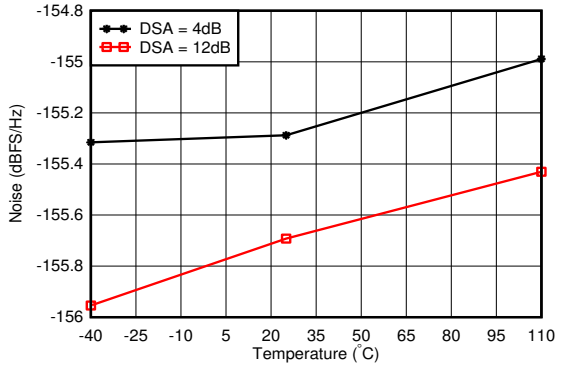


With 4.9 GHz matching, f_{IN} = 4910 MHz, A_{IN}= –3 dBFS

Figure 90. RX Output FFT at 4.9 GHz

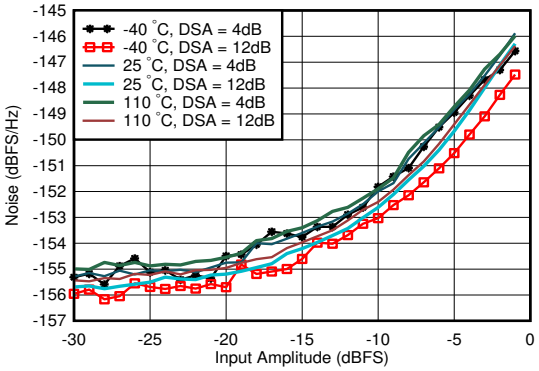
RX Typical Characteristics (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz, output sample rate = 491.52MSPS (decimate by 6), Internal PLL/VCO, f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB, unless otherwise noted.



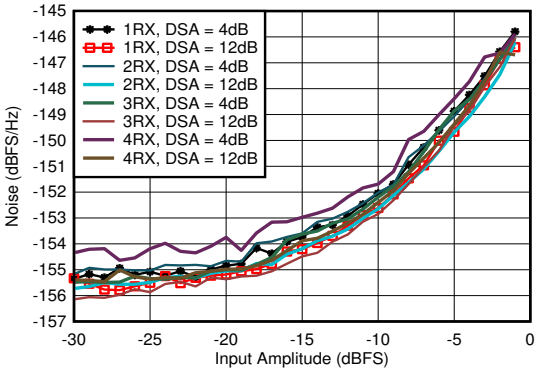
With 4.9 GHz matching, 12.5-MHz offset from tone

Figure 91. RX Noise Spectral Density vs Temperature at 4.9 GHz



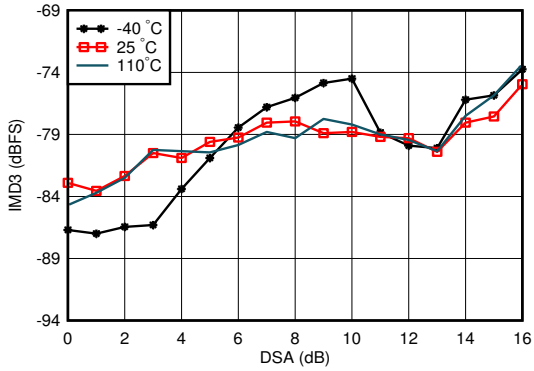
With 4.9 GHz matching, DSA Setting = 12 dB, 12.5-MHz offset from tone

Figure 92. RX Noise Spectral Density vs Input Amplitude and Temperature at 4.9 GHz



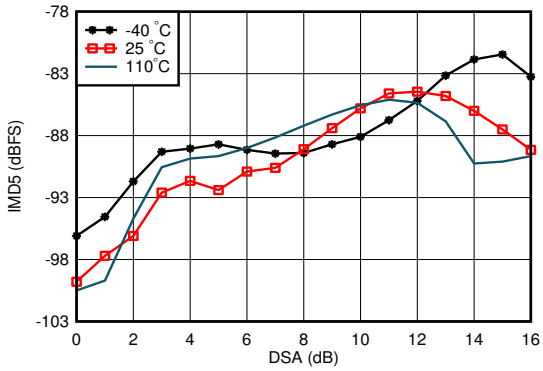
With 4.9 GHz matching, 12.5-MHz offset from tone

Figure 93. RX Noise Spectral Density vs Input Amplitude and Channel at 4.9 GHz



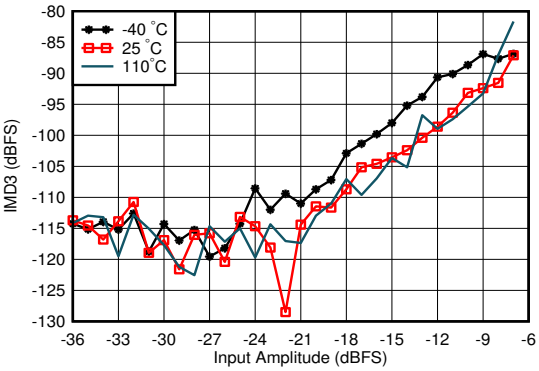
With 4.9 GHz matching, each tone –7 dBFS, tone spacing = 20 MHz

Figure 94. RX IMD3 vs DSA Setting and Temperature at 4.9 GHz



With 4.9 GHz matching, each tone –7 dBFS, tone spacing = 20 MHz

Figure 95. RX IMD5 vs DSA Setting and Temperature at 4.9 GHz

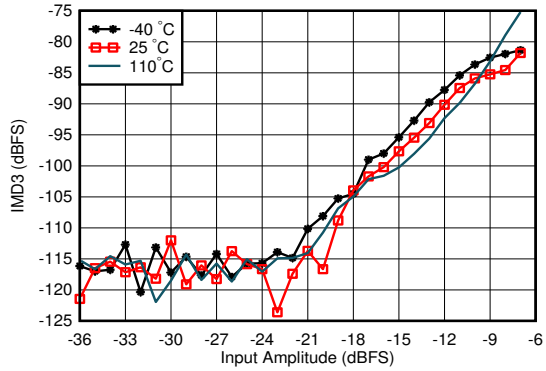


With 4.9 GHz matching, tone spacing = 20 MHz, DSA = 4 dB

Figure 96. RX IMD3 vs Input Level and Temperature at 4.9 GHz

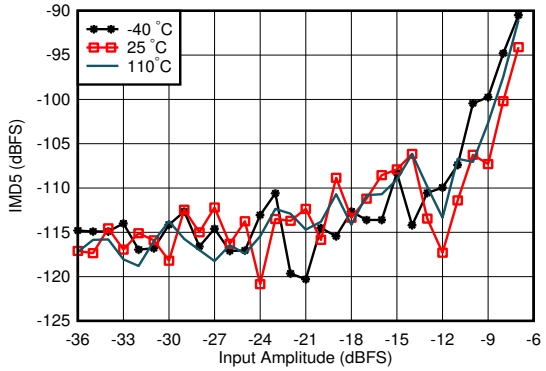
RX Typical Characteristics (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz, output sample rate = 491.52MSPS (decimate by 6), Internal PLL/VCO, f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB, unless otherwise noted.



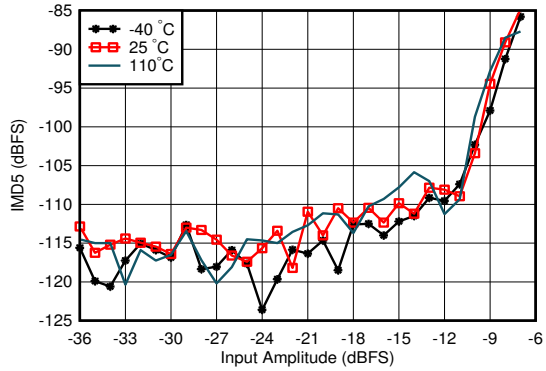
With 4.9 GHz matching, tone spacing = 20 MHz, DSA = 12 dB

Figure 97. RX IMD3 vs Input Level and Temperature at 4.9 GHz



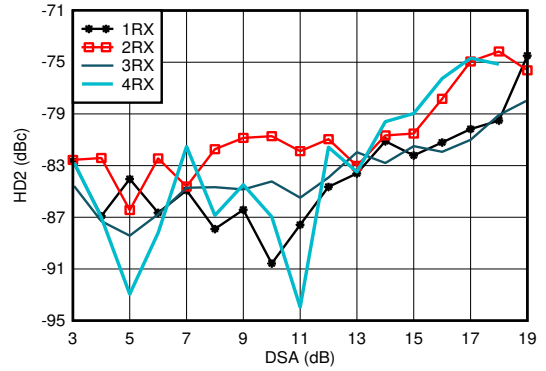
With 4.9 GHz matching, tone spacing = 20 MHz, DSA = 4 dB

Figure 98. RX IMD5 vs Input Level and Temperature at 4.9 GHz



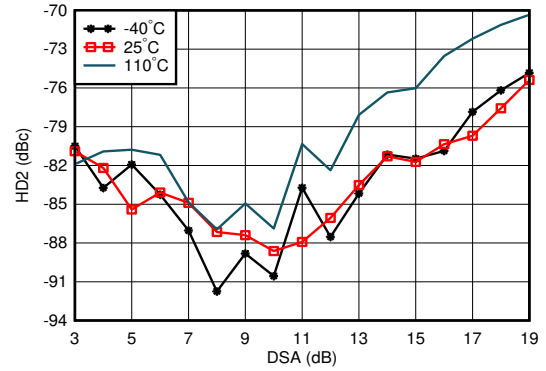
With 4.9 GHz matching, tone spacing = 20 MHz, DSA = 12 dB

Figure 99. RX IMD5 vs Input Level and Temperature at 4.9 GHz



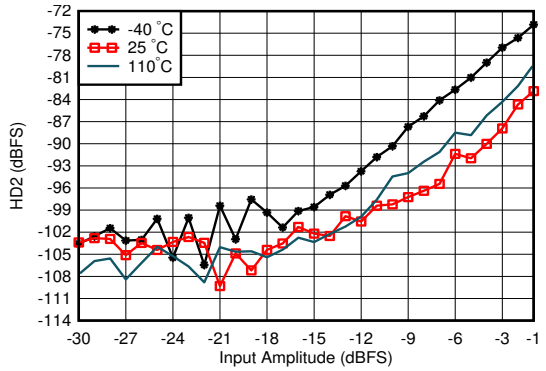
With 4.9 GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

Figure 100. RX HD2 vs DSA Setting and Channel at 4.9 GHz



With 4.9 GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

Figure 101. RX HD2 vs DSA and Temperature at 4.9 GHz

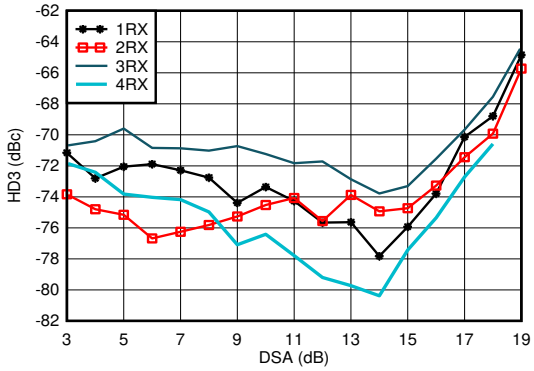


With 4.9 GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

Figure 102. RX HD2 vs Input Level and Temperature at 4.9 GHz

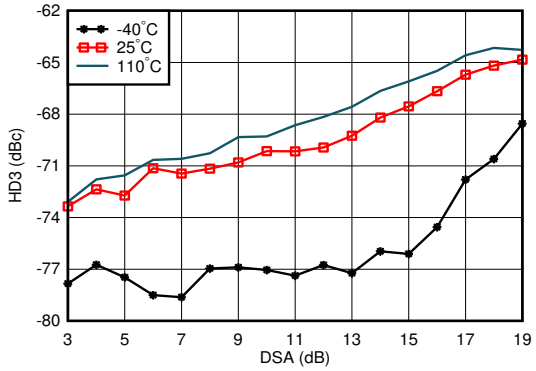
RX Typical Characteristics (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz, output sample rate = 491.52MSPS (decimate by 6), Internal PLL/VCO, f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB, unless otherwise noted.



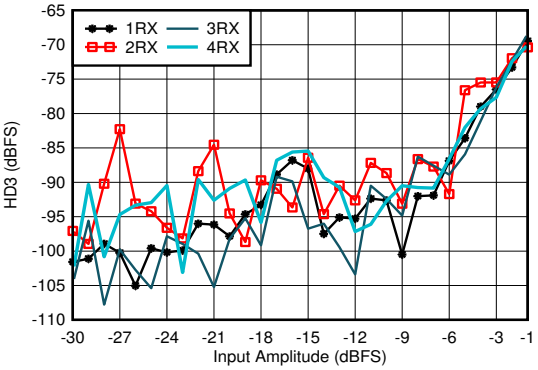
With 4.9 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 103. RX HD3 vs DSA Setting and Channel at 4.9 GHz



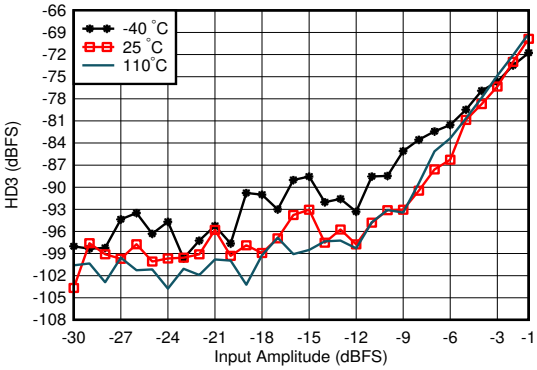
With 4.9 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 104. RX HD3 vs DSA Setting and Temperature at 4.9 GHz



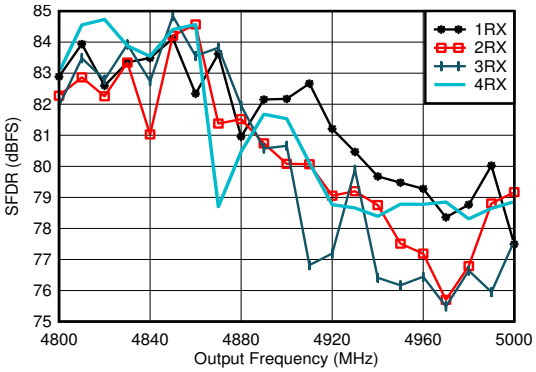
With 4.9 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 105. RX HD3 vs Input Level and Channel at 4.9 GHz



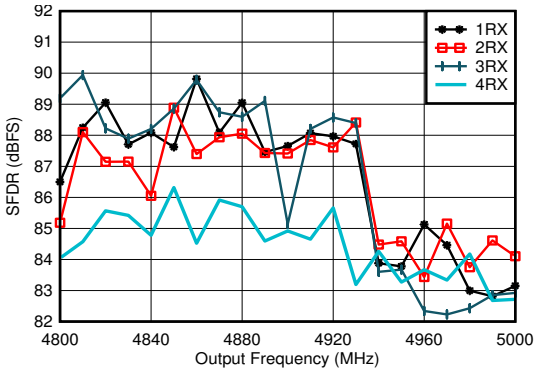
With 4.9 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 106. RX HD3 vs Input Level and Temperature at 4.9 GHz



With 4.9 GHz matching, decimated by 12

Figure 107. RX In-Band SFDR (±100 MHz) vs Frequency With A_{IN}= –1 dBFS at 4.9 GHz

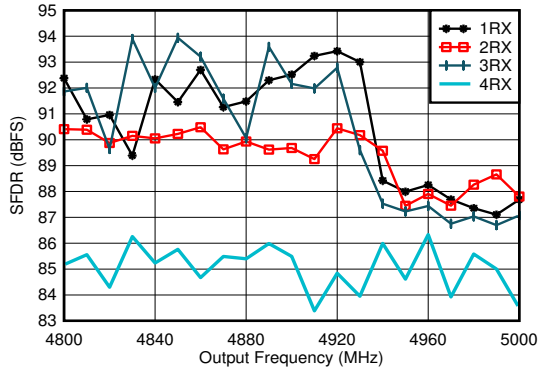


With 4.9 GHz matching, decimated by 12

Figure 108. RX In-Band SFDR (±100 MHz) vs Frequency With A_{IN}= –6 dBFS at 4.9 GHz

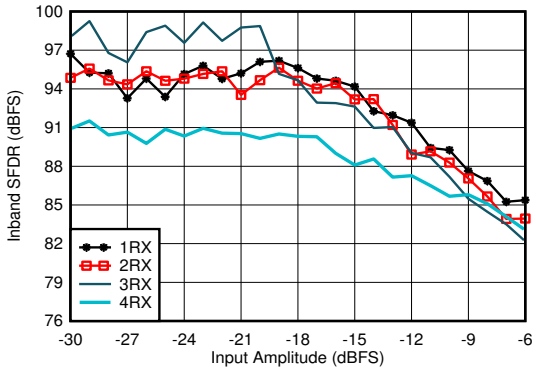
RX Typical Characteristics (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz, output sample rate = 491.52MSPS (decimate by 6), Internal PLL/VCO, f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB, unless otherwise noted.



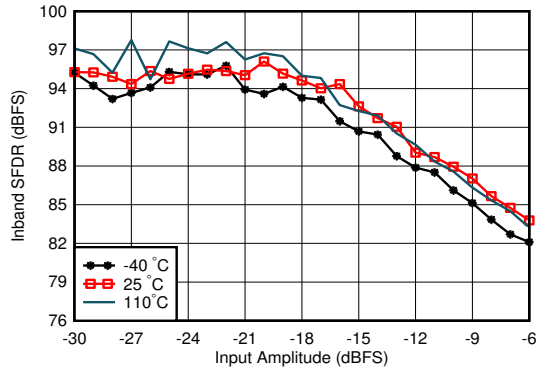
With 4.9 GHz matching, decimated by 12

Figure 109. RX In-Band SFDR (±100 MHz) vs Frequency With A_{IN}= –12 dBFS at 4.9 GHz



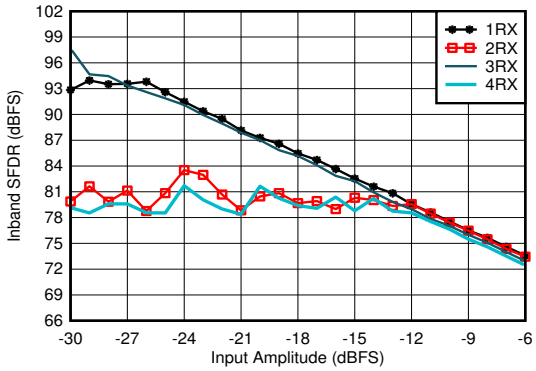
With 4.9 GHz matching

Figure 110. RX In-Band SFDR (±200 MHz) vs Input Amplitude at 4.9 GHz



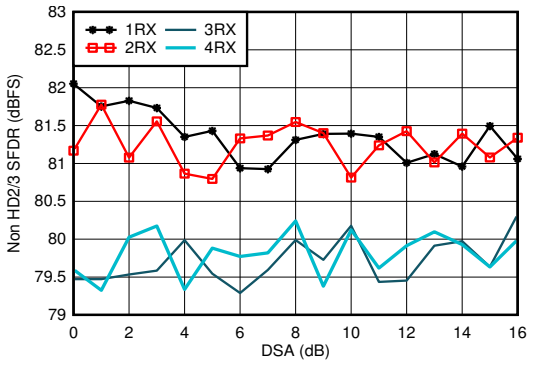
With 4.9 GHz matching

Figure 111. RX In-Band SFDR (±200 MHz) vs Input Amplitude and Temperature at 4.9 GHz



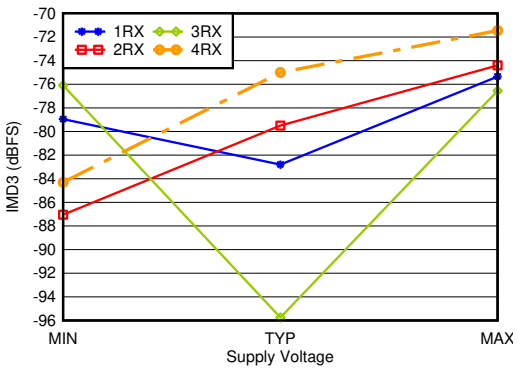
With 4.9 GHz matching, decimate by 3

Figure 112. RX In-Band SFDR (±400 MHz) vs Input Amplitude and Channel at 4.9 GHz



With 4.9 GHz matching

Figure 113. RX Non-HD2/3 vs DSA Setting at 4.9 GHz

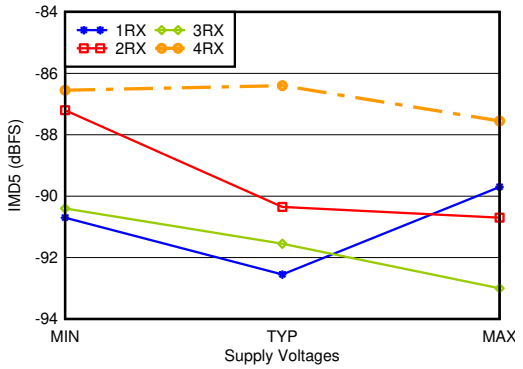


With 4.9 GHz matching, –7 dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

Figure 114. RX IMD3 vs Supply and Channel at 4.9 GHz

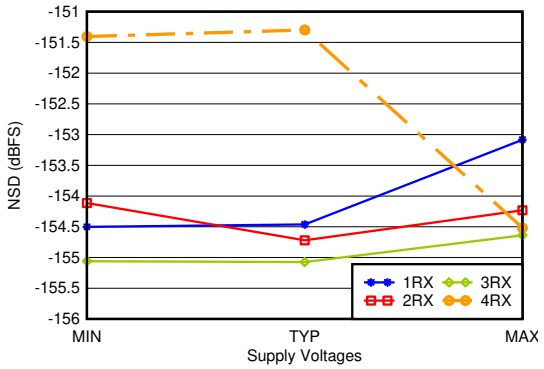
RX Typical Characteristics (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz, output sample rate = 491.52MSPS (decimate by 6), Internal PLL/VCO, f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB, unless otherwise noted.



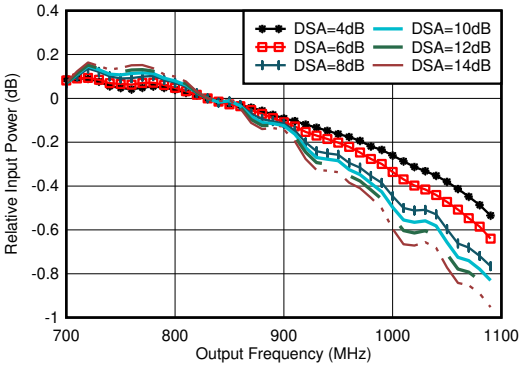
With 4.9 GHz matching, –7 dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

Figure 115. RX IMD5 vs Supply and Channel at 4.9 GHz



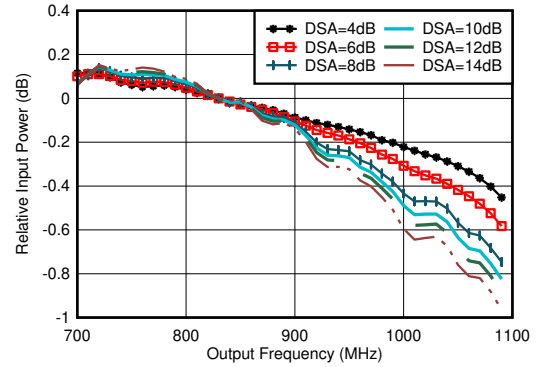
With 4.9 GHz matching, 12.5-MHz offset, all supplies at MIN, TYP, or MAX recommended operating voltages

Figure 116. RX Noise Spectral Density vs Supply and Channel at 4.9 GHz



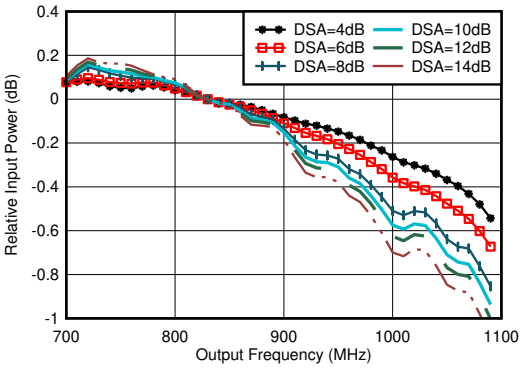
With 0.8 GHz matching, normalized to 830 MHz

Figure 117. RX In-Band Gain Flatness for Channel 1RX, f_{IN} = 830 MHz



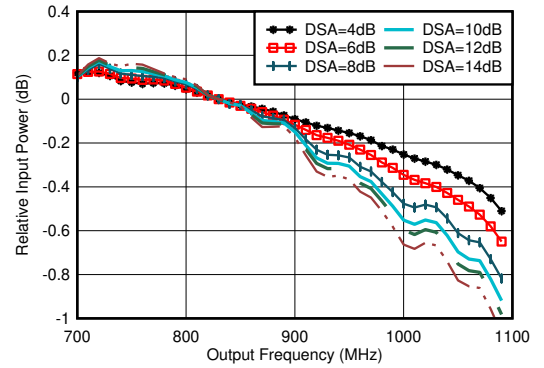
With 0.8 GHz matching, normalized to power at 830 MHz for each DSA setting

Figure 118. RX Inband Gain Flatness for Channel 2RX, f_{IN} = 830 MHz



With 0.8 GHz matching, normalized to power at 830 MHz for each DSA setting

Figure 119. RX Inband Gain Flatness for Channel 3RX, f_{IN} = 830 MHz

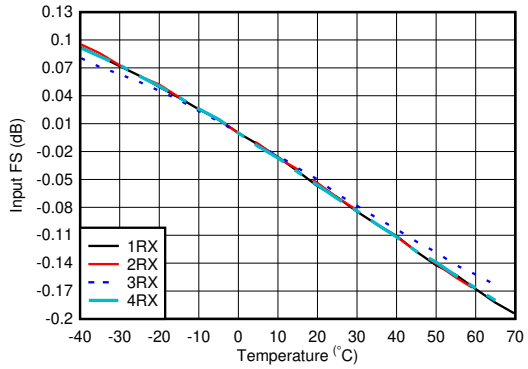


With 0.8 GHz matching, normalized to power at 830 MHz for each DSA setting

Figure 120. RX Inband Gain Flatness for Channel 4RX, f_{IN} = 830 MHz

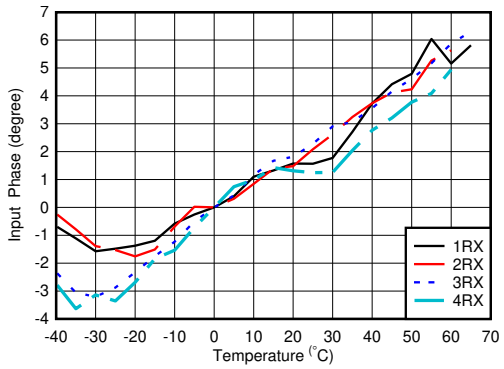
RX Typical Characteristics (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz, output sample rate = 491.52MSPS (decimate by 6), Internal PLL/VCO, f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB, unless otherwise noted.



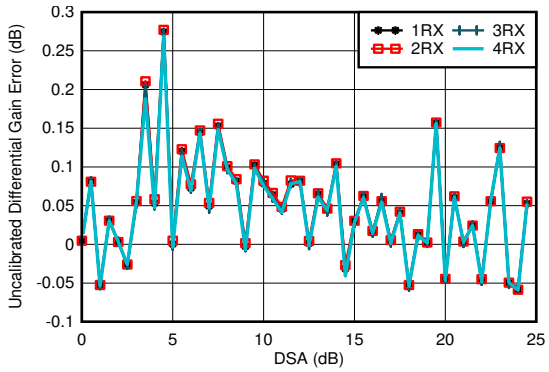
With 0.8 GHz matching, normalized to fullscale at 25°C for each channel

Figure 121. RX Input Fullscale vs Temperature and Channel at 0.8 GHz



With 0.8 GHz matching, normalized to phase at 25°C

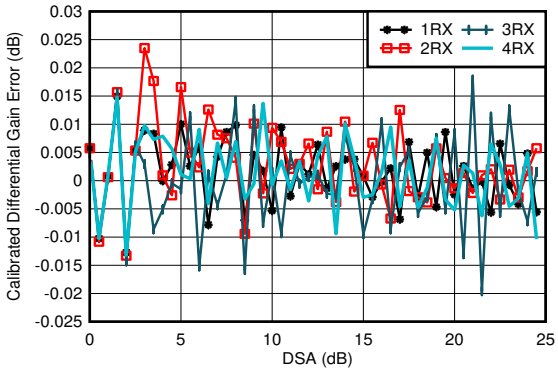
Figure 122. RX Input Phase vs Temperature and DSA at f_{OUT} = 0.8 GHz



With 0.8 GHz matching

Differential Amplitude Error = P_{IN}(DSA Setting – 1) – P_{IN}(DSA Setting) + 1

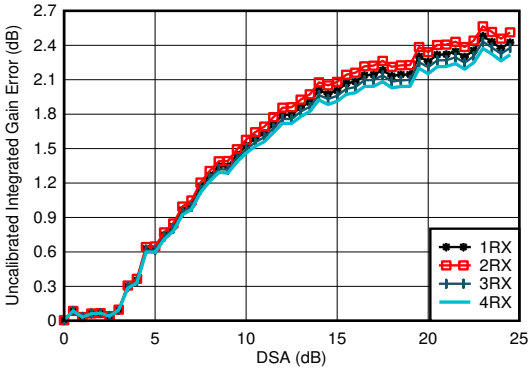
Figure 123. RX Uncalibrated Differential Amplitude Error vs DSA Setting at 0.8 GHz



With 0.8 GHz matching

Differential Amplitude Error = P_{IN}(DSA Setting – 1) – P_{IN}(DSA Setting) + 1

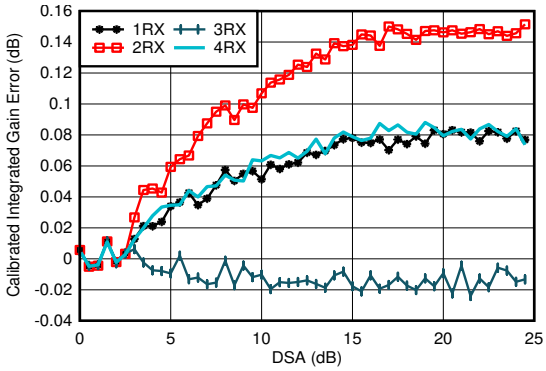
Figure 124. RX Calibrated Differential Amplitude Error vs DSA Setting at 0.8 GHz



With 0.8 GHz matching

Integrated Amplitude Error = P_{IN}(DSA Setting) – P_{IN}(DSA Setting = 0) + (DSA Setting)

Figure 125. RX Uncalibrated Integrated Amplitude Error vs DSA Setting at 0.8 GHz



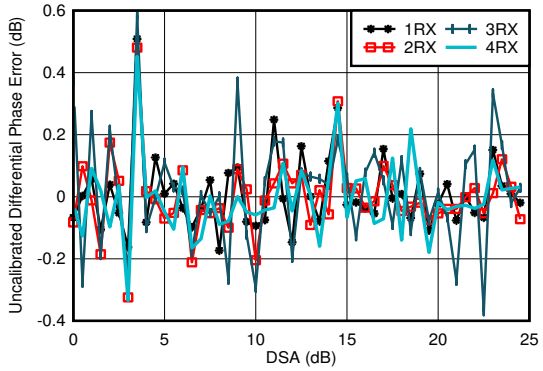
With 0.8 GHz matching

Integrated Amplitude Error = P_{IN}(DSA Setting) – P_{IN}(DSA Setting = 0) + (DSA Setting)

Figure 126. RX Calibrated Integrated Amplitude Error vs DSA Setting at 2.6 GHz

RX Typical Characteristics (continued)

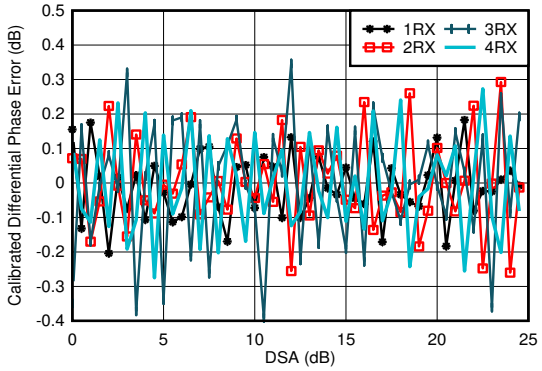
Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz, output sample rate = 491.52MSPS (decimate by 6), Internal PLL/VCO, f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB, unless otherwise noted.



With 0.8 GHz matching

Differential Phase Error = $Phase_{IN}$(DSA Setting – 1) – $Phase_{IN}$(DSA Setting)

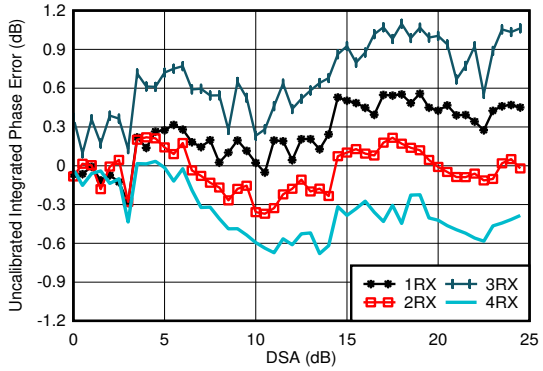
Figure 127. RX Uncalibrated Differential Phase Error vs DSA Setting at 0.8 GHz



With 0.8 GHz matching

Differential Phase Error = $Phase_{IN}$(DSA Setting – 1) – $Phase_{IN}$(DSA Setting)

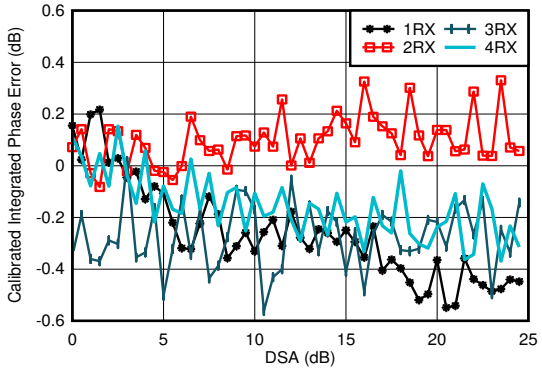
Figure 128. RX Calibrated Differential Phase Error vs DSA Setting at 0.8 GHz



With 0.8 GHz matching

Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

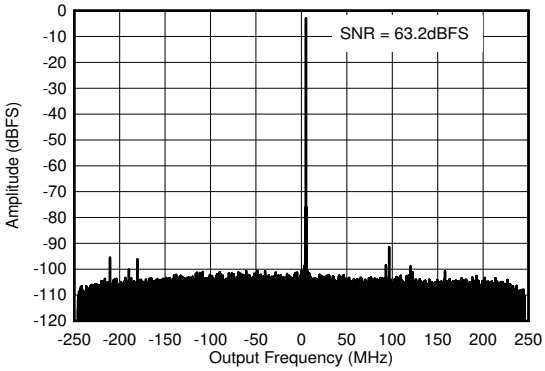
Figure 129. RX Uncalibrated Integrated Phase Error vs DSA Setting at 0.8 GHz



With 0.8 GHz matching

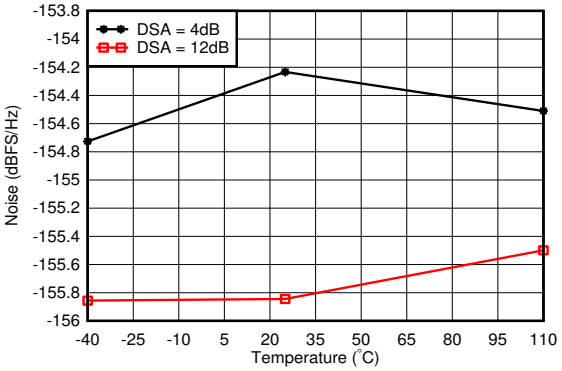
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

Figure 130. RX Calibrated Integrated Phase Error vs DSA Setting at 0.8 GHz



With 0.8 GHz matching, f_{IN} = 840 MHz, A_{IN}= –3 dBFS

Figure 131. RX Output FFT at 0.8 GHz

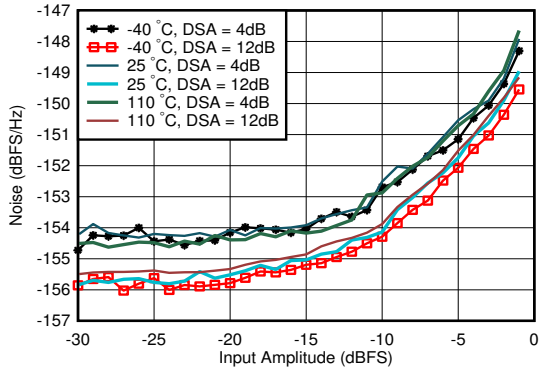


With 0.8 GHz matching, 12.5-MHz offset from tone

Figure 132. RX Noise Spectral Density vs Temperature at 0.8 GHz

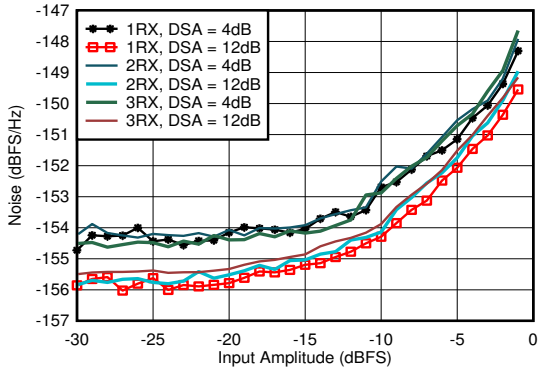
RX Typical Characteristics (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz, output sample rate = 491.52MSPS (decimate by 6), Internal PLL/VCO, f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB, unless otherwise noted.



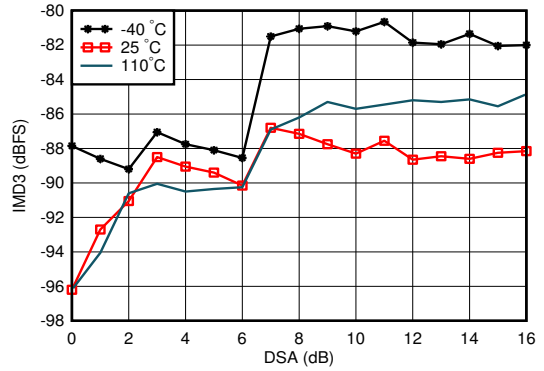
With 0.8 GHz matching, DSA Setting = 12 dB, 12.5-MHz offset from tone

Figure 133. RX Noise Spectral Density vs Input Amplitude and Temperature at 0.8 GHz



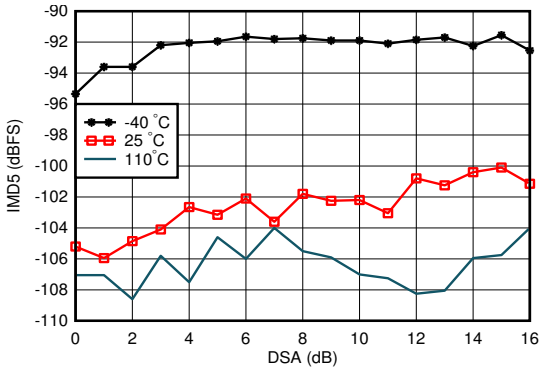
With 0.8 GHz matching, 12.5-MHz offset from tone

Figure 134. RX Noise Spectral Density vs Input Amplitude and Channel at 0.8 GHz



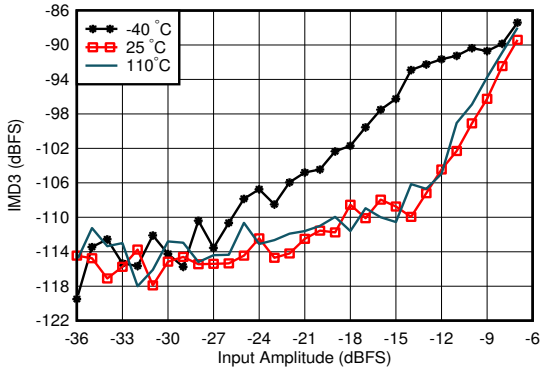
With 0.8 GHz matching, each tone –7 dBFS, tone spacing = 20 MHz

Figure 135. RX IMD3 vs DSA Setting and Temperature at 0.8 GHz



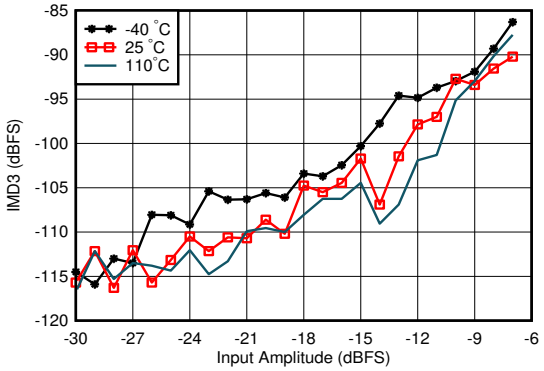
With 0.8 GHz matching, each tone –7 dBFS, tone spacing = 20 MHz

Figure 136. RX IMD5 vs DSA Setting and Temperature at 0.8 GHz



With 0.8 GHz matching, tone spacing = 20 MHz, DSA = 4 dB

Figure 137. RX IMD3 vs Input Level and Temperature at 0.8 GHz

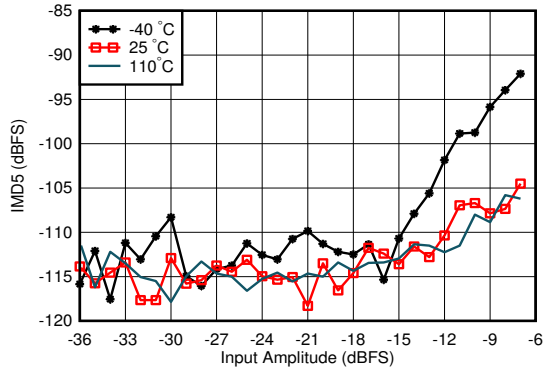


With 0.8 GHz matching, tone spacing = 20 MHz, DSA = 12 dB

Figure 138. RX IMD3 vs Input Level and Temperature at 0.8 GHz

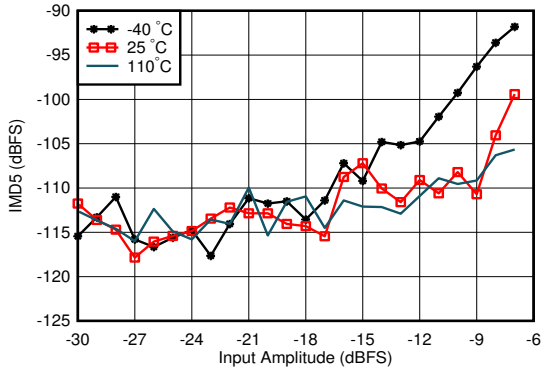
RX Typical Characteristics (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz, output sample rate = 491.52MSPS (decimate by 6), Internal PLL/VCO, f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB, unless otherwise noted.



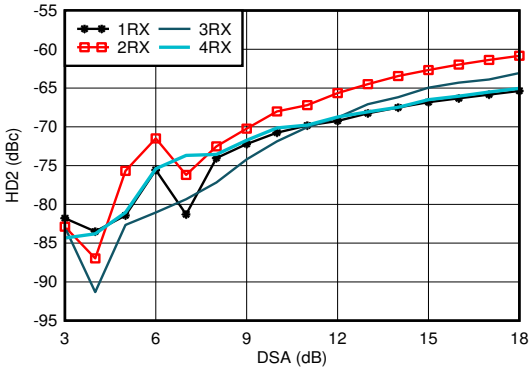
With 0.8 GHz matching, tone spacing = 20 MHz, DSA = 12 dB

Figure 139. RX IMD5 vs Input Level and Temperature at 0.8 GHz



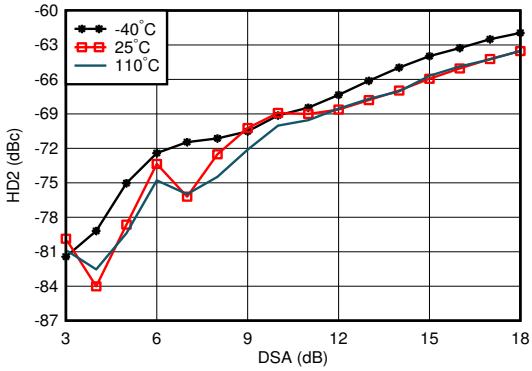
With 2.6 GHz matching, tone spacing = 20 MHz, DSA = 12 dB

Figure 140. RX IMD5 vs Input Level and Temperature at 2.6 GHz



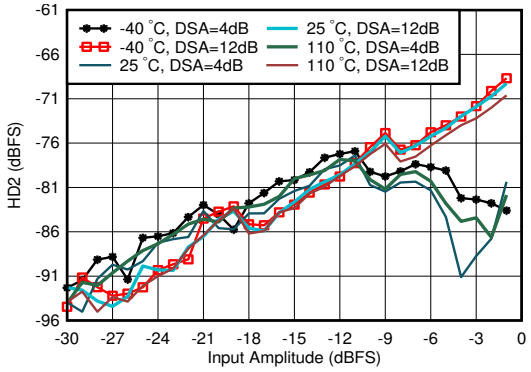
With 0.8 GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

Figure 141. RX HD2 vs DSA Setting and Channel at 0.8 GHz



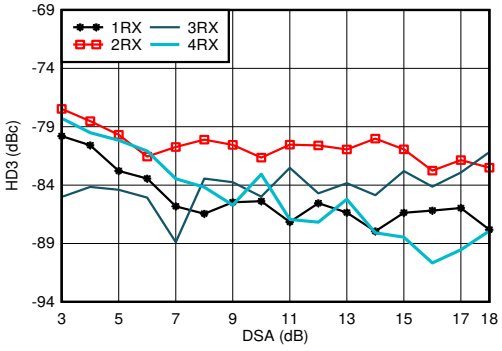
With 0.8 GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

Figure 142. RX HD2 vs DSA Setting and Temperature at 0.8 GHz



With 0.8 GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

Figure 143. RX HD2 vs Input Level and Temperature at 0.8 GHz

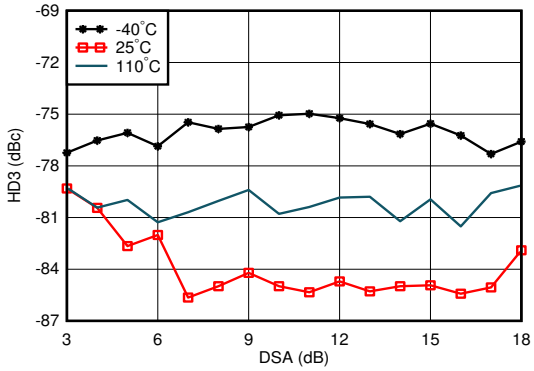


With 0.8 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 144. RX HD3 vs DSA Setting and Channel at 0.8 GHz

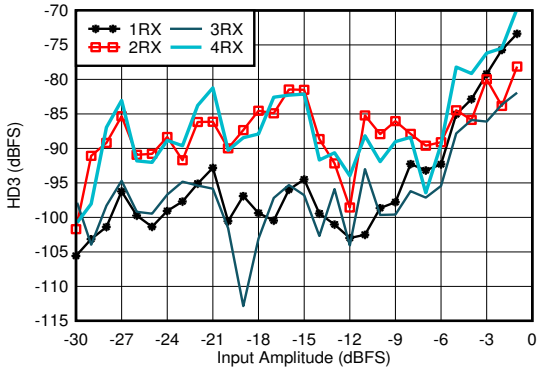
RX Typical Characteristics (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz, output sample rate = 491.52MSPS (decimate by 6), Internal PLL/VCO, f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB, unless otherwise noted.



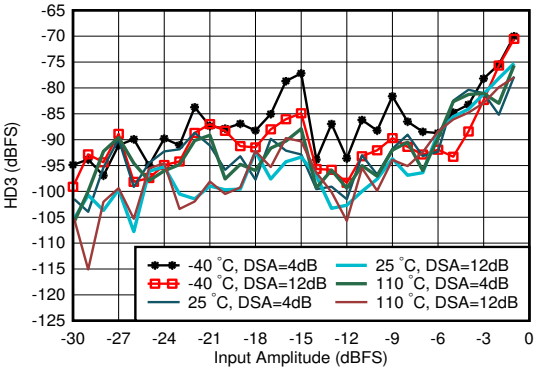
With 0.8 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 145. RX HD3 vs DSA Setting and Temperature at 0.8 GHz



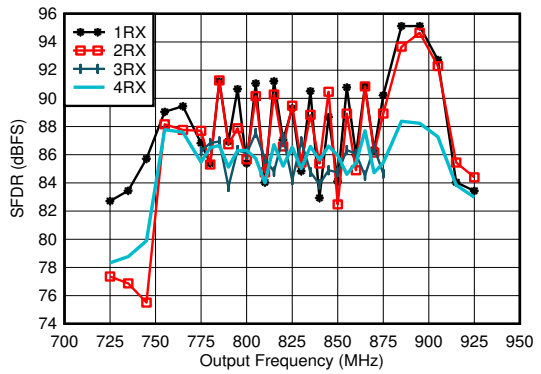
With 0.8 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 146. RX HD3 vs Input Level and Channel at 0.8 GHz



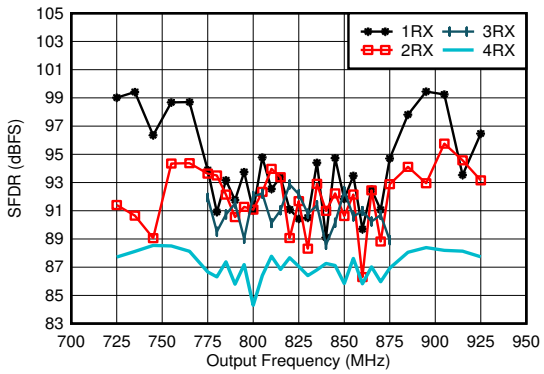
With 0.8 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 147. RX HD3 vs Input Level and Temperature at 0.8 GHz



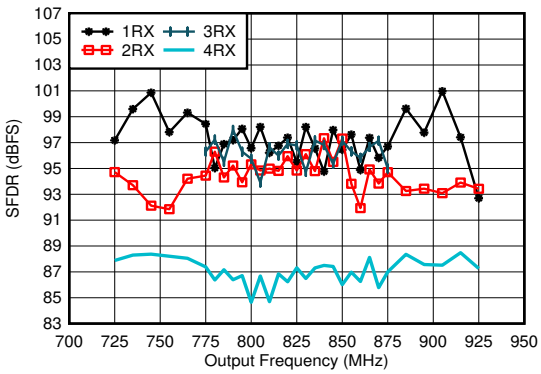
With 0.8 GHz matching, decimated by 12

Figure 148. RX In-Band SFDR (±100 MHz) vs Frequency With A_{IN}= –1 dBFS at 0.8 GHz



With 0.8 GHz matching, decimated by 12

Figure 149. RX In-Band SFDR (±100 MHz) vs Frequency With A_{IN}= –6 dBFS at 0.8 GHz

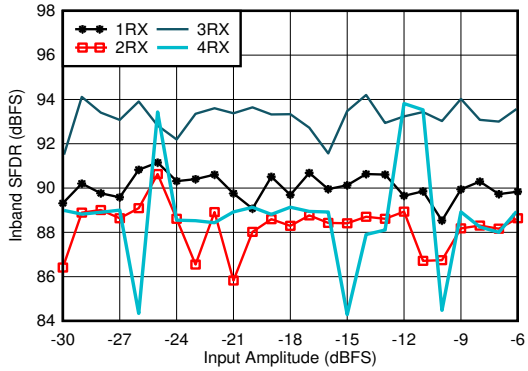


With 0.8 GHz matching, decimated by 12

Figure 150. RX In-Band SFDR (±100 MHz) vs Frequency With A_{IN}= –12 dBFS at 0.8 GHz

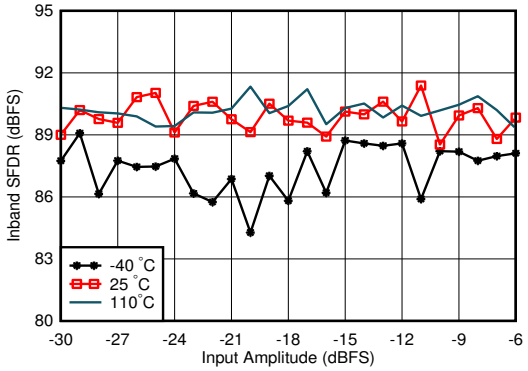
RX Typical Characteristics (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz, output sample rate = 491.52MSPS (decimate by 6), Internal PLL/VCO, f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB, unless otherwise noted.



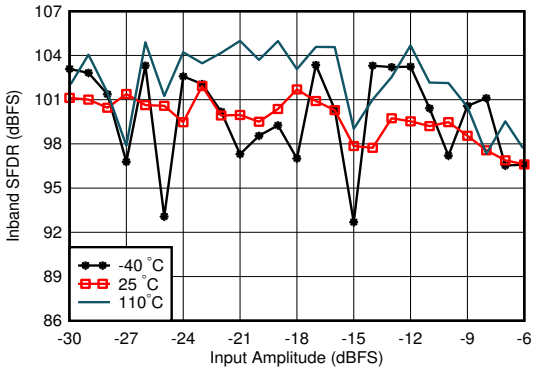
With 0.8 GHz matching

Figure 151. RX In-Band SFDR (±200 MHz) vs Input Amplitude at 0.8 GHz



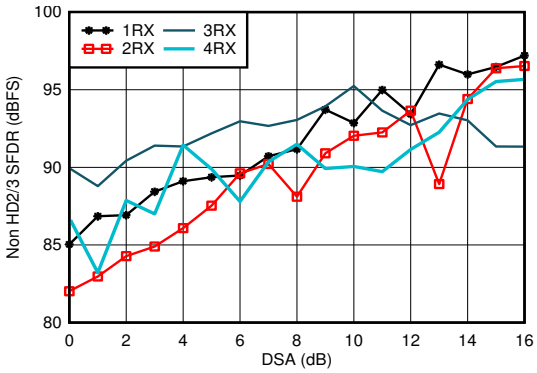
With 0.8 GHz matching

Figure 152. RX In-Band SFDR (±200 MHz) vs Input Amplitude and Temperature at 0.8 GHz



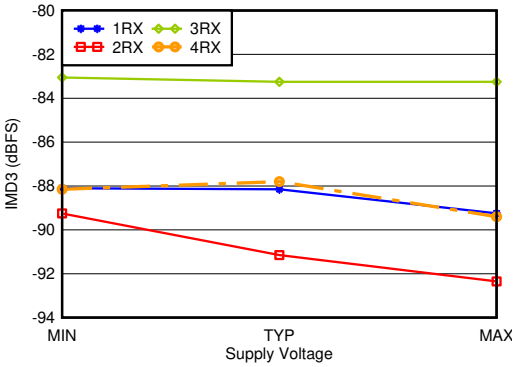
With 0.8 GHz matching, decimate by 24

Figure 153. RX In-Band SFDR (±50 MHz) vs Input Amplitude and Temperature at 0.8 GHz



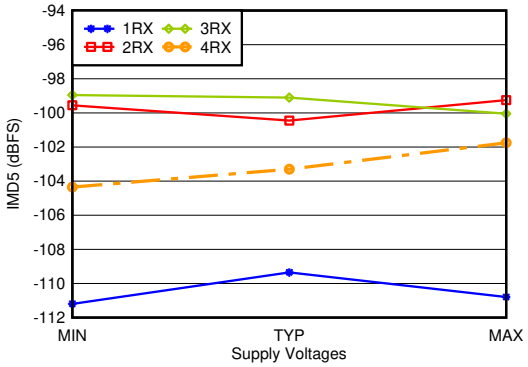
With 0.8 GHz matching

Figure 154. RX Non-HD2/3 vs DSA Setting at 0.8 GHz



With 0.8 GHz matching, –7 dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

Figure 155. RX IMD3 vs Supply and Channel at 0.8 GHz

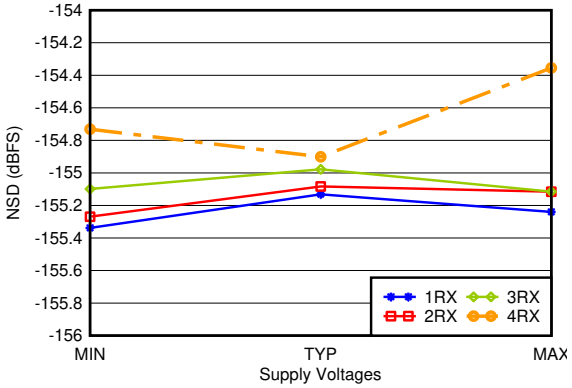


With 0.8 GHz matching, –7 dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

Figure 156. RX IMD5 vs Supply and Channel at 0.8 GHz

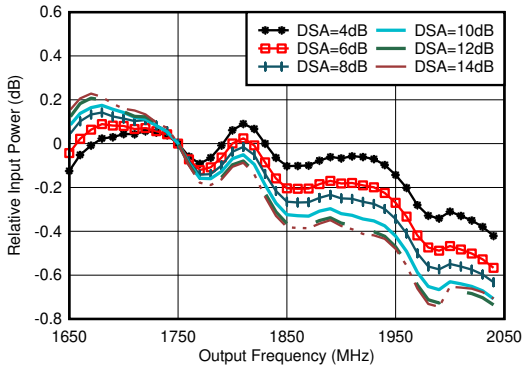
RX Typical Characteristics (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz, output sample rate = 491.52MSPS (decimate by 6), Internal PLL/VCO, f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB, unless otherwise noted.



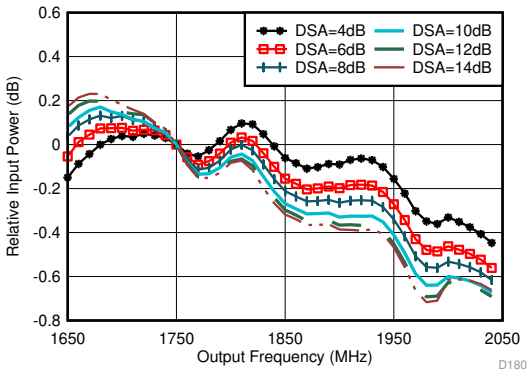
With 0.8 GHz matching, 12.5-MHz offset, all supplies at MIN, TYP, or MAX recommended operating voltages

Figure 157. RX Noise Spectral Density vs Supply and Channel at 0.8 GHz



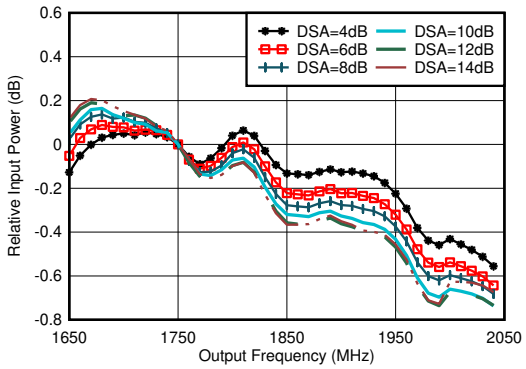
With 1.8 GHz matching, normalized to 1.75 GHz

Figure 158. RX In-Band Gain Flatness for Channel 1RX, f_{IN} = 1750 MHz



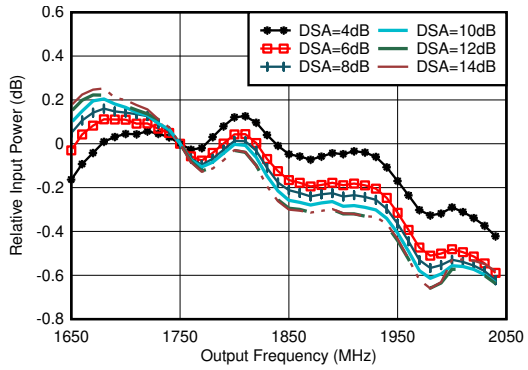
With 1.8 GHz matching, normalized to power at 1.75 GHz for each DSA setting

Figure 159. RX Inband Gain Flatness for Channel 2RX, f_{IN} = 1750 MHz



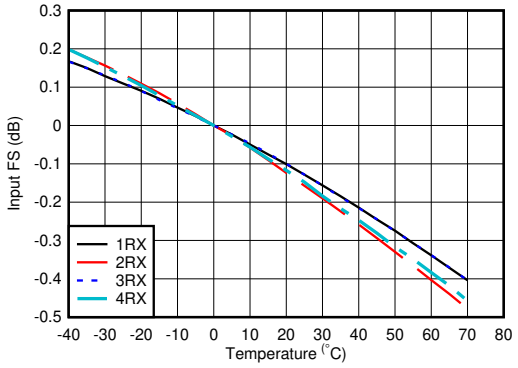
With 1.8 GHz matching, normalized to power at 1.75 GHz for each DSA setting

Figure 160. RX Inband Gain Flatness for Channel 3RX, f_{IN} = 1750 MHz



With 1,8 GHz matching, normalized to power at 1.75 GHz for each DSA setting

Figure 161. RX Inband Gain Flatness for Channel 4RX, f_{IN} = 1750 MHz

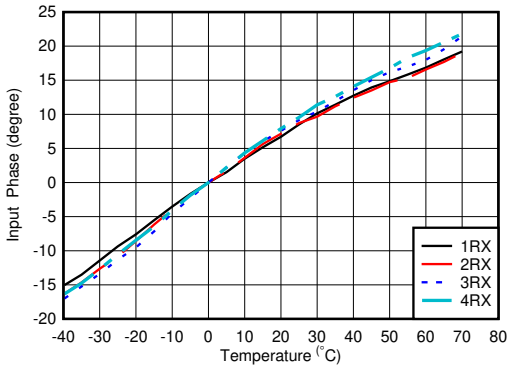


With 1.8 GHz matching, normalized to fullscale at 25°C for each channel

Figure 162. RX Input Fullscale vs Temperature and Channel at 1.75 GHz

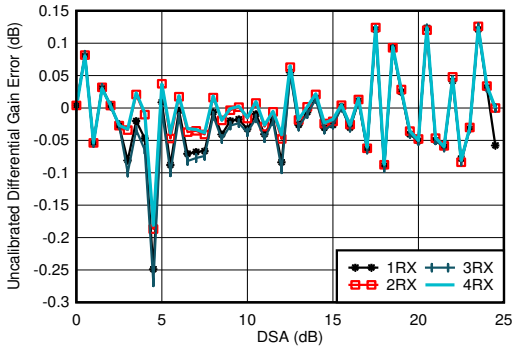
RX Typical Characteristics (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz, output sample rate = 491.52MSPS (decimate by 6), Internal PLL/VCO, f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB, unless otherwise noted.



With 2.6 GHz matching, normalized to phase at 25°C

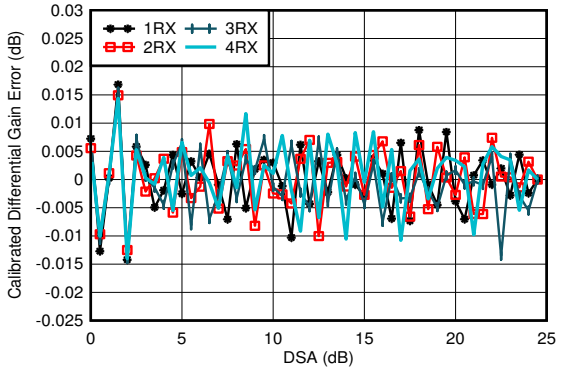
Figure 163. RX Input Phase vs Temperature and DSA at f_{IN} = 1.75 GHz



With 1.8 GHz matching

Differential Amplitude Error = P_{IN}(DSA Setting – 1) – P_{IN}(DSA Setting) + 1

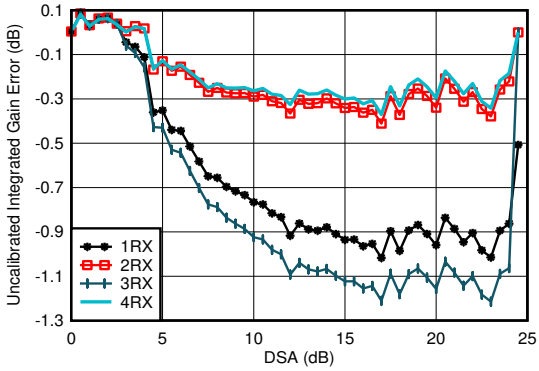
Figure 164. RX Uncalibrated Differential Amplitude Error vs DSA Setting at 1.75 GHz



With 1.8 GHz matching

Differential Amplitude Error = P_{IN}(DSA Setting – 1) – P_{IN}(DSA Setting) + 1

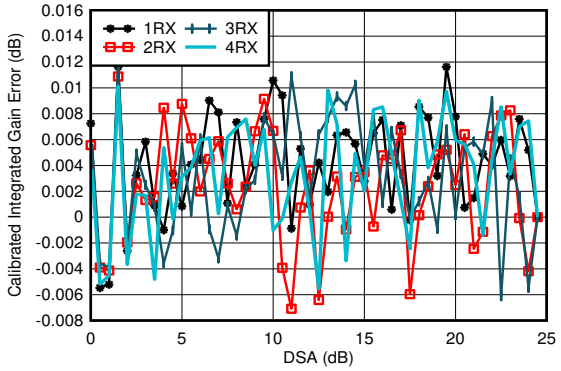
Figure 165. RX Calibrated Differential Amplitude Error vs DSA Setting at 1.75 GHz



With 1.8 GHz matching

Integrated Amplitude Error = P_{IN}(DSA Setting) – P_{IN}(DSA Setting = 0) + (DSA Setting)

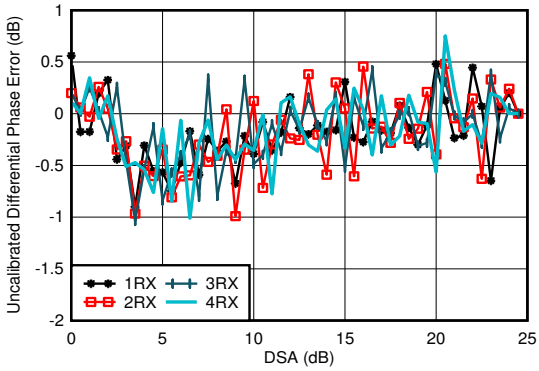
Figure 166. RX Uncalibrated Integrated Amplitude Error vs DSA Setting at 1.75 GHz



With 1.8 GHz matching

Integrated Amplitude Error = P_{IN}(DSA Setting) – P_{IN}(DSA Setting = 0) + (DSA Setting)

Figure 167. RX Calibrated Integrated Amplitude Error vs DSA Setting at 1.75 GHz



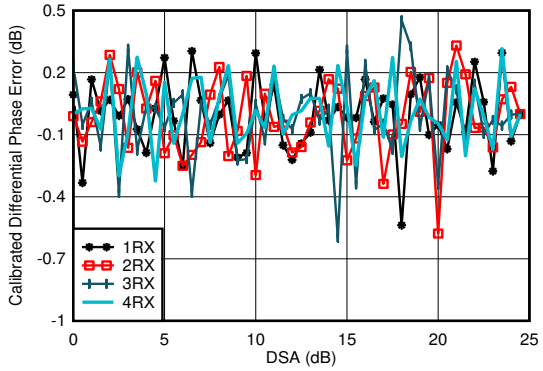
With 1.8 GHz matching

Differential Phase Error = $Phase_{IN}$(DSA Setting – 1) – $Phase_{IN}$(DSA Setting)

Figure 168. RX Uncalibrated Differential Phase Error vs DSA Setting at 1.75 GHz

RX Typical Characteristics (continued)

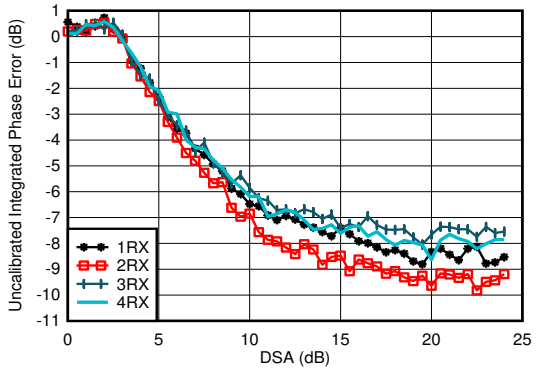
Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz, output sample rate = 491.52MSPS (decimate by 6), Internal PLL/VCO, f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB, unless otherwise noted.



With 1.8 GHz matching

Differential Phase Error = $Phase_{IN}$(DSA Setting – 1) – $Phase_{IN}$(DSA Setting)

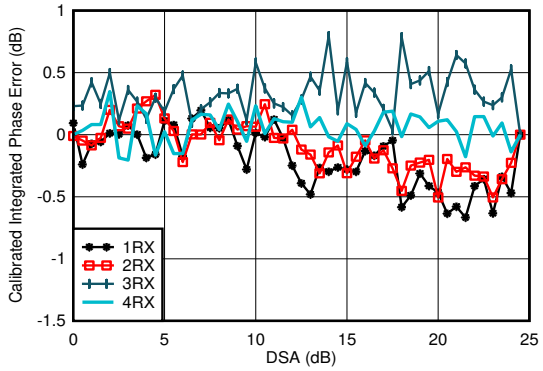
Figure 169. RX Calibrated Differential Phase Error vs DSA Setting at 1.75 GHz



With 1.8 GHz matching

Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

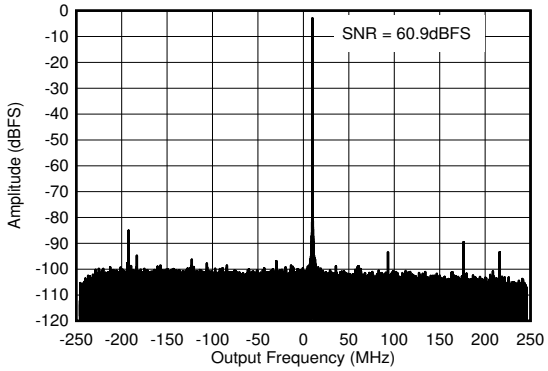
Figure 170. RX Uncalibrated Integrated Phase Error vs DSA Setting at 1.75 GHz



With 1.8 GHz matching

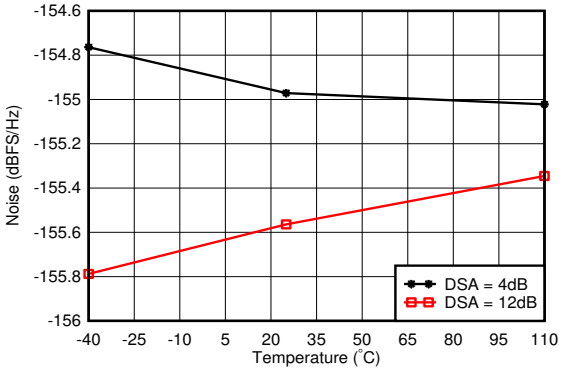
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

Figure 171. RX Calibrated Integrated Phase Error vs DSA Setting at 1.75 GHz



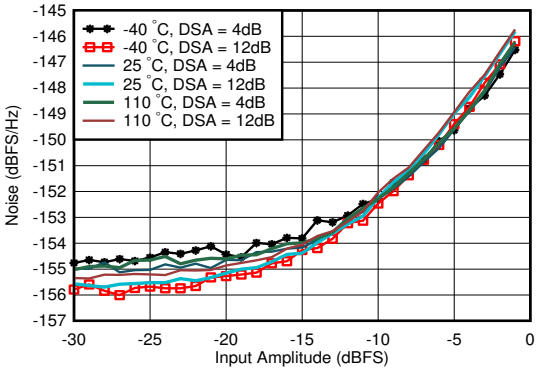
With 1.8 GHz matching, f_{IN} = 2610 MHz, A_{IN}= –3 dBFS

Figure 172. RX Output FFT at 1.75 GHz



With 1.8 GHz matching, 12.5-MHz offset from tone

Figure 173. RX Noise Spectral Density vs Temperature at 1.75 GHz

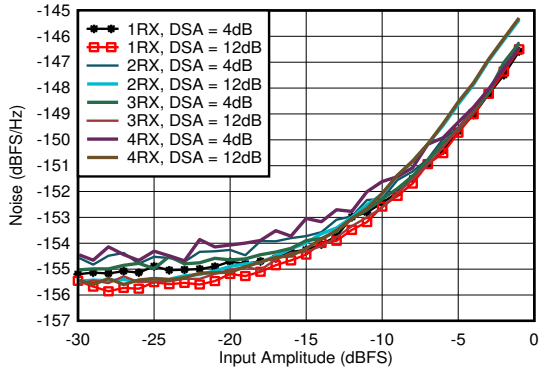


With 1.8 GHz matching, DSA Setting = 12 dB, 12.5-MHz offset from tone

Figure 174. RX Noise Spectral Density vs Input Amplitude and Temperature at 1.75 GHz

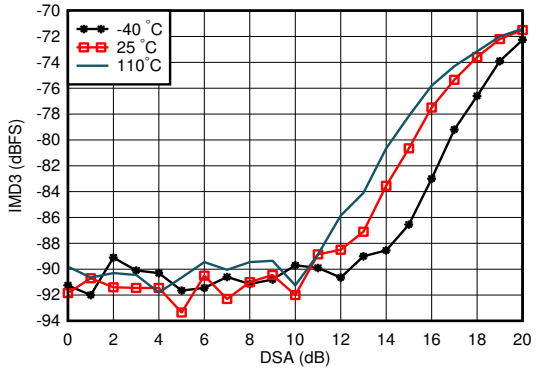
RX Typical Characteristics (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz, output sample rate = 491.52MSPS (decimate by 6), Internal PLL/VCO, f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB, unless otherwise noted.



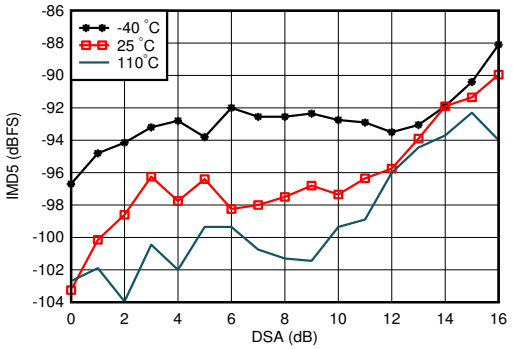
With 1.8 GHz matching, 12.5-MHz offset from tone

Figure 175. RX Noise Spectral Density vs Input Amplitude and Channel at 1.75 GHz



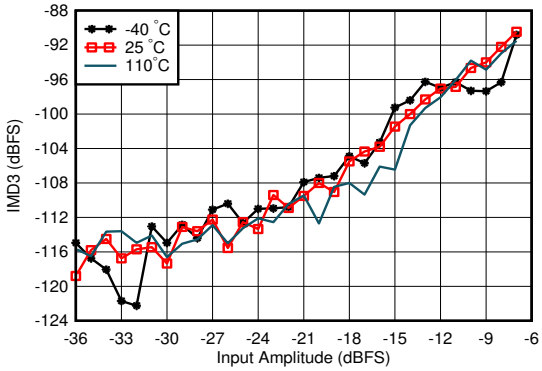
With 1.8 GHz matching, each tone –7 dBFS, tone spacing = 20 MHz

Figure 176. RX IMD3 vs DSA Setting and Temperature at 1.75 GHz



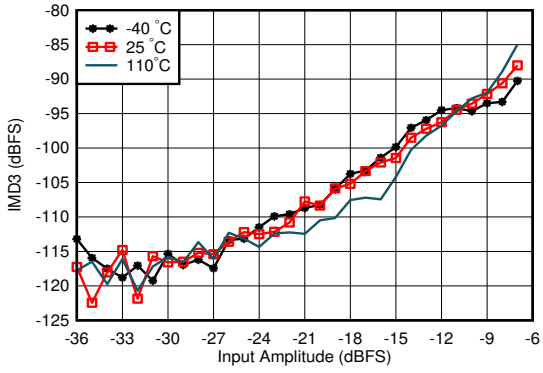
With 1.8 GHz matching, each tone –7 dBFS, tone spacing = 20 MHz

Figure 177. RX IMD5 vs DSA Setting and Temperature at 1.75 GHz



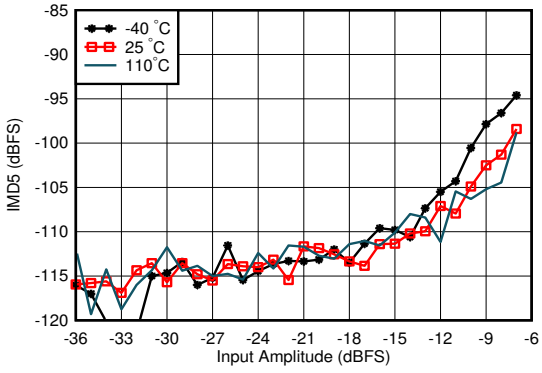
With 1.8 GHz matching, tone spacing = 20 MHz, DSA = 4 dB

Figure 178. RX IMD3 vs Input Level and Temperature at 1.75 GHz



With 1.8 GHz matching, tone spacing = 20 MHz, DSA = 12 dB

Figure 179. RX IMD3 vs Input Level and Temperature at 1.75 GHz

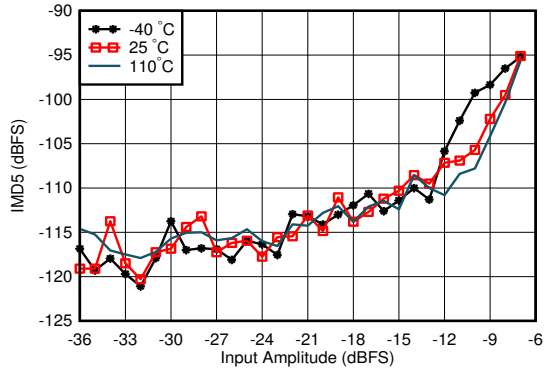


With 1.8 GHz matching, tone spacing = 20 MHz, DSA = 4 dB

Figure 180. RX IMD5 vs Input Level and Temperature at 1.75 GHz

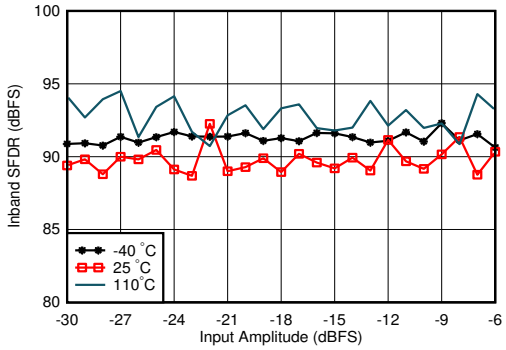
RX Typical Characteristics (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz, output sample rate = 491.52MSPS (decimate by 6), Internal PLL/VCO, f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB, unless otherwise noted.



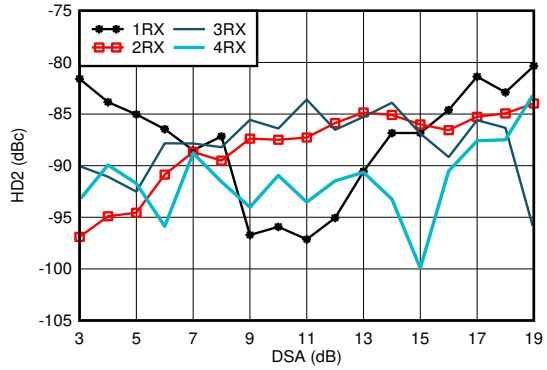
With 1.8 GHz matching, tone spacing = 20 MHz, DSA = 12 dB

Figure 181. RX IMD5 vs Input Level and Temperature at 1.75 GHz



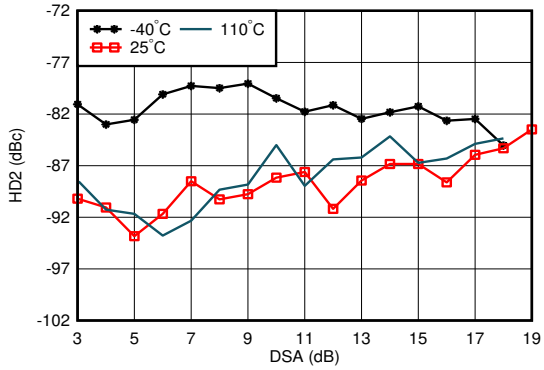
With 1.8 GHz matching, decimate by 24, DSA Setting = 4 dB

Figure 182. RX Inband SFDR (±50 MHz) vs Input Amplitude and Temperature at 1.75 GHz



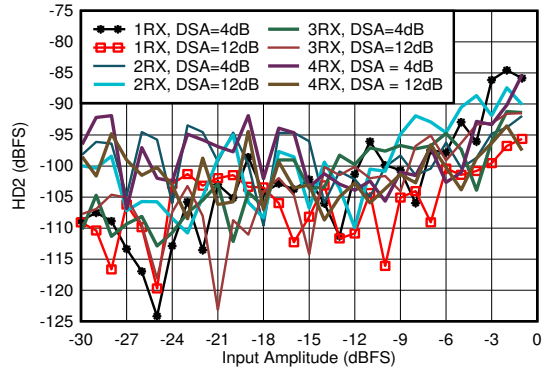
With 1.8 GHz matching, f_{in} = 1900MHz, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

Figure 183. RX HD2 vs DSA Setting and Channel at 1.9 GHz



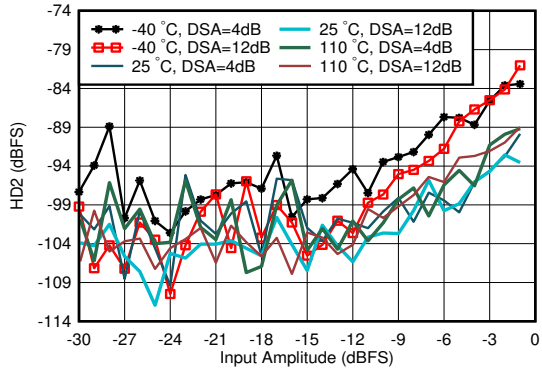
With 1.8 GHz matching, f_{in} = 1900MHz, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

Figure 184. RX HD2 vs DSA Setting and Temperature at 1.9 GHz



With 1.8 GHz matching, f_{in} = 1900MHz, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

Figure 185. RX HD2 vs Input Amplitude and Channel at 1.9 GHz

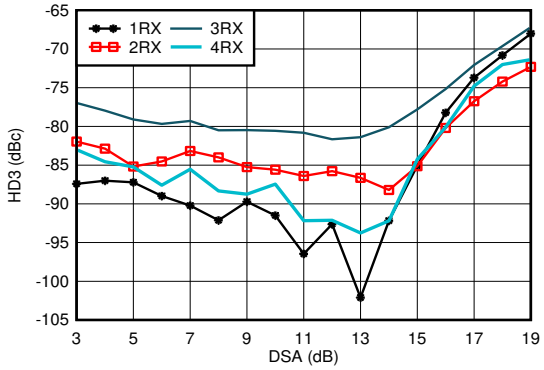


With 1.8 GHz matching, f_{in} = 1900MHz, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

Figure 186. RX HD2 vs Input Amplitude and Temperature at 1.9 GHz

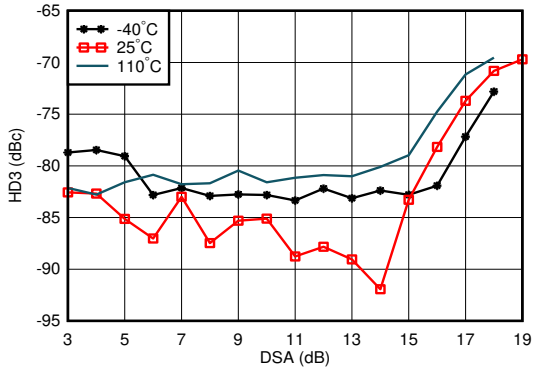
RX Typical Characteristics (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz, output sample rate = 491.52MSPS (decimate by 6), Internal PLL/VCO, f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB, unless otherwise noted.



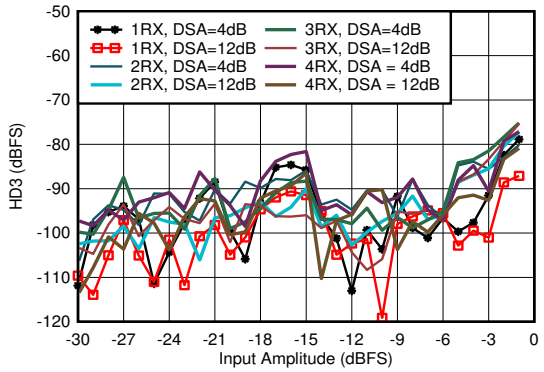
With 1.8 GHz matching, f_{in} = 1900MHz, DDC bypass mode (TI only mode for characterization)

Figure 187. RX HD3 vs DSA Setting and Channel at 1.9 GHz



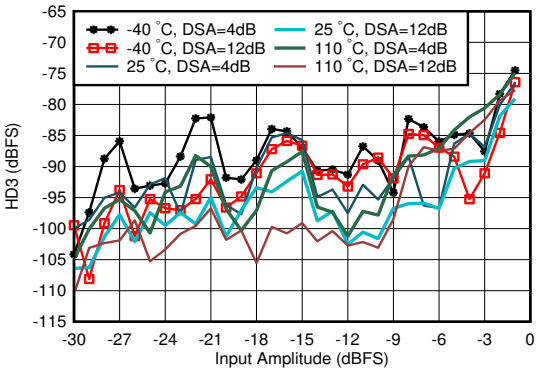
With 1.8 GHz matching, f_{in} = 1900MHz, DDC bypass mode (TI only mode for characterization)

Figure 188. RX HD3 vs DSA Setting and Temperature at 1.9 GHz



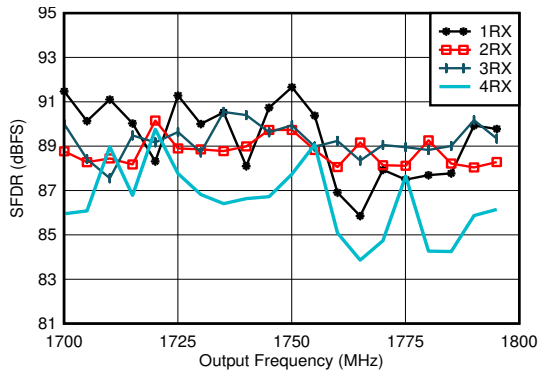
With 1.8 GHz matching, f_{in} = 1900MHz, DDC bypass mode (TI only mode for characterization)

Figure 189. RX HD3 vs Input Level and Channel at 1.9 GHz



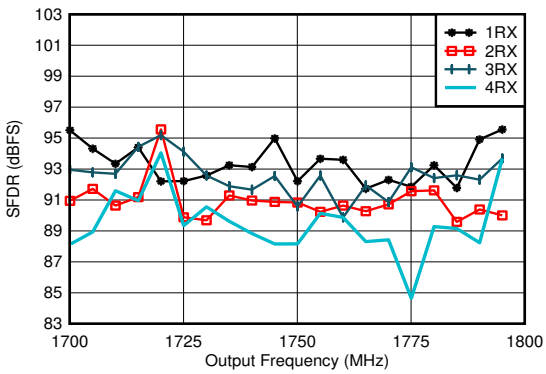
With 1.8 GHz matching, f_{in} = 1900MHz, DDC bypass mode (TI only mode for characterization)

Figure 190. RX HD3 vs Input Level and Temperature at 1.9 GHz



With 1.8 GHz matching, decimated by 24

Figure 191. RX In-Band SFDR (±50 MHz) vs Frequency With A_{IN}= –1 dBFS at 1.75 GHz

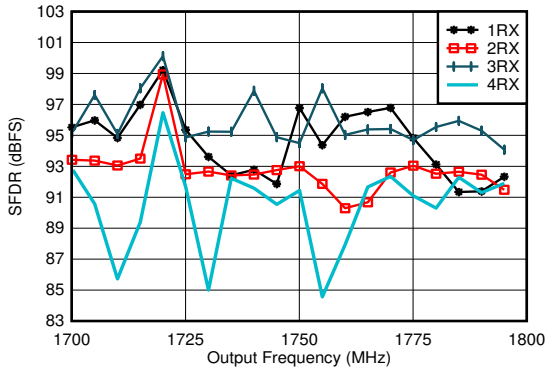


With 1.8 GHz matching, decimated by 24

Figure 192. RX In-Band SFDR (±50 MHz) vs Frequency With A_{IN}= –6 dBFS at 1.75 GHz

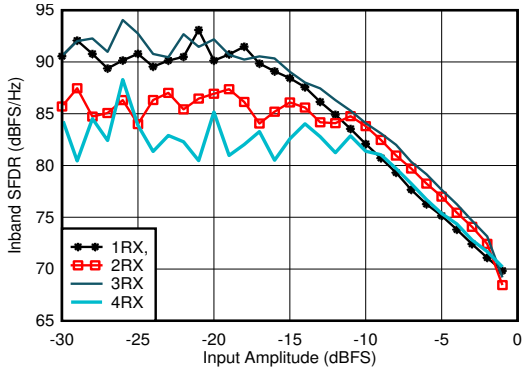
RX Typical Characteristics (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz, output sample rate = 491.52MSPS (decimate by 6), Internal PLL/VCO, f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB, unless otherwise noted.



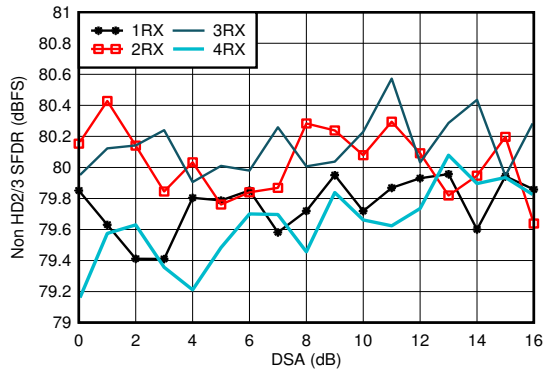
With 1.8 GHz matching, decimated by 24

Figure 193. RX In-Band SFDR (±50 MHz) vs Frequency With A_{IN}= –12 dBFS at 1.75 GHz



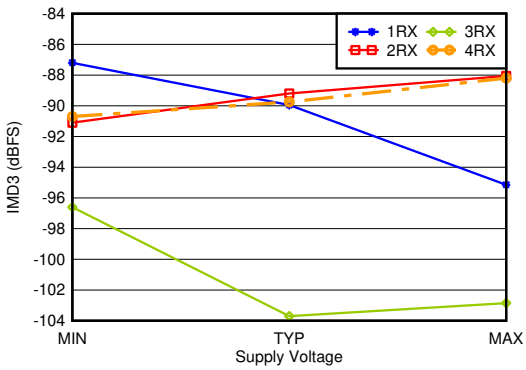
With 1.8 GHz matching, decimated by 3

Figure 194. RX In-Band SFDR (±400 MHz) vs Input Amplitude at 1.75 GHz



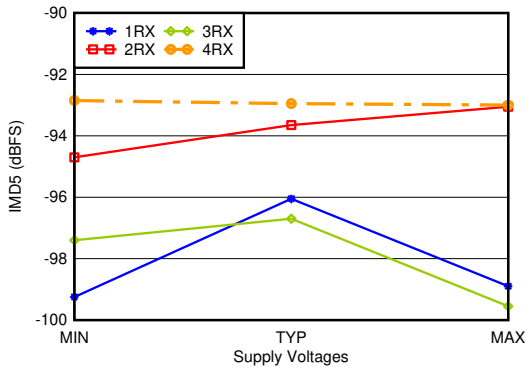
With 1.8 GHz matching

Figure 195. RX Non-HD2/3 vs DSA Setting at 1.75 GHz



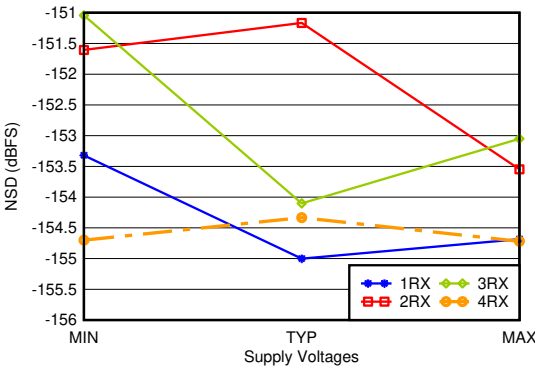
With 1.8 GHz matching, –7 dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

Figure 196. RX IMD3 vs Supply and Channel at 1.75 GHz



With 1.8 GHz matching, –7 dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

Figure 197. RX IMD5 vs Supply and Channel at 1.75 GHz

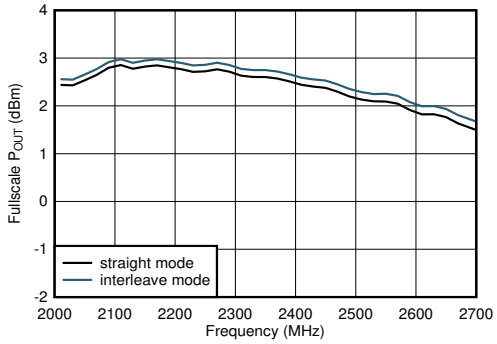


With 1.8 GHz matching, 12.5-MHz offset, all supplies at MIN, TYP, or MAX recommended operating voltages

Figure 198. RX Noise Spectral Density vs Supply and Channel at 1.75 GHz

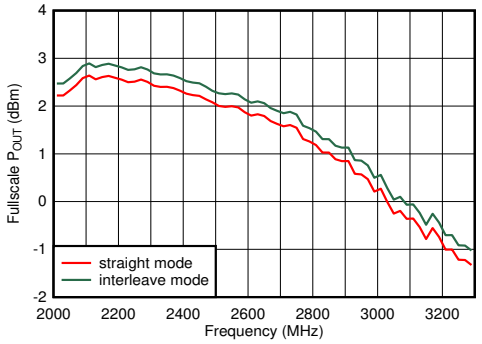
8.12.2 TX Typical Characteristics

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



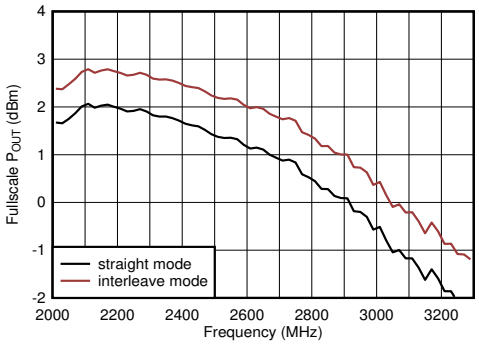
Including PCB and cable losses, A_{out} = -0.5dBFS, DSA = 0, 2.6 GHz matching

Figure 199. TX Full Scale vs RF Frequency at 5898.24MSPS



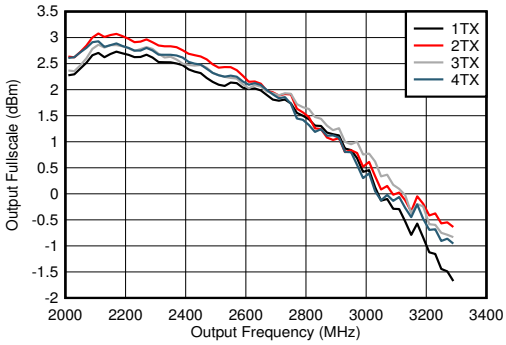
Including PCB and cable losses, A_{out} = -0.5dBFS, DSA = 0, 2.6 GHz matching

Figure 200. TX Full Scale vs RF Frequency at 8847.36MSPS



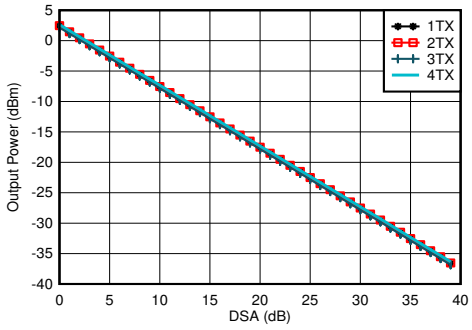
Including PCB and cable losses, A_{out} = -0.5dBFS, DSA = 0, 2.6 GHz matching

Figure 201. TX Full Scale vs RF Frequency at 11796.48MSPS



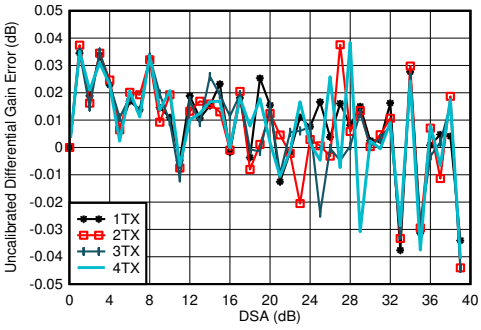
f_{DAC} = 8847.36MSPS, interleave mode, including PCB and cable losses, A_{out} = -0.5dBFS, DSA = 0, 2.6 GHz matching

Figure 202. TX Output Fullscale vs Output Frequency and Channel



f_{DAC} = 8847.36 MSPS, A_{out} = -0.5dBFS, matching 2.6 GHz

Figure 203. TX Output Power vs DSA Setting and Channel at 2.6 GHz



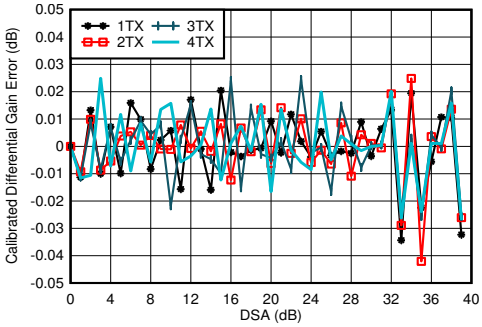
f_{DAC}=8847.36MSPS, straight mode, matching at 2.6 GHz

Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

Figure 204. TX Uncalibrated Differential Gain Error vs DSA Setting and Channel at 2.6 GHz

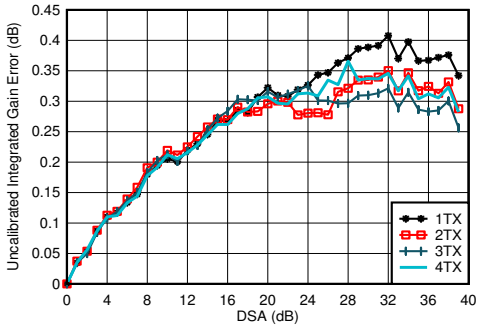
TX Typical Characteristics (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



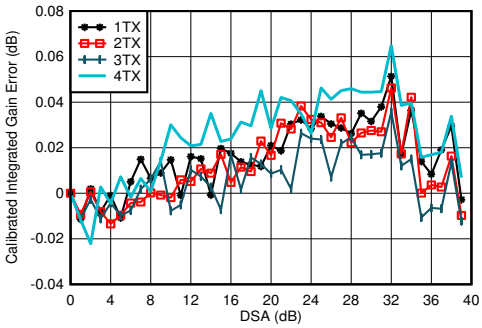
f_{DAC}=8847.36MSPS, straight mode, matching at 2.6 GHz
Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

Figure 205. TX Calibrated Differential Gain Error vs DSA Setting and Channel at 2.6 GHz



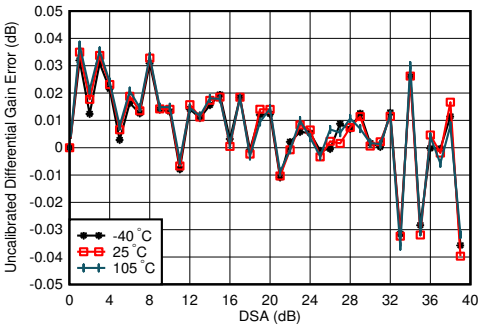
f_{DAC}=8847.36MSPS, straight mode, matching at 2.6 GHz
Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + (DSA Setting)

Figure 206. TX Uncalibrated Integrated Gain Error vs DSA Setting and Channel at 2.6 GHz



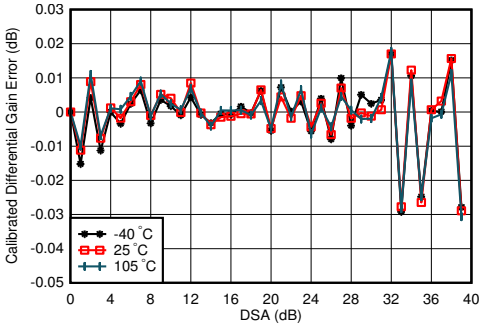
f_{DAC} = 8847.36MSPS, straight mode, matching at 2.6 GHz
Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + (DSA Setting)

Figure 207. TX Calibrated Integrated Gain Error vs DSA Setting and Channel at 2.6 GHz



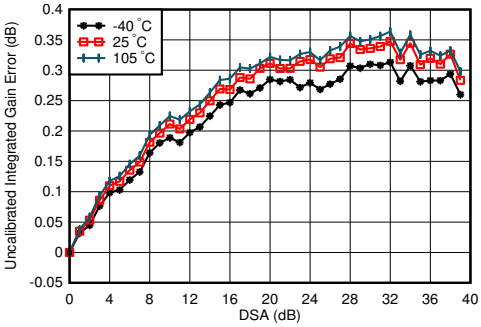
f_{DAC} = 8847.36MSPS, straight mode, matching at 2.6 GHz, channel with the median variation over DSA setting at 25°C
Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

Figure 208. TX Uncalibrated Differential Gain Error vs DSA Setting and Temperature at 2.6 GHz



f_{DAC} = 8847.36MSPS, straight mode, matching at 2.6 GHz, channel with the median variation over DSA setting at 25°C
Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

Figure 209. TX Calibrated Differential Gain Error vs DSA Setting and Temperature at 2.6 GHz

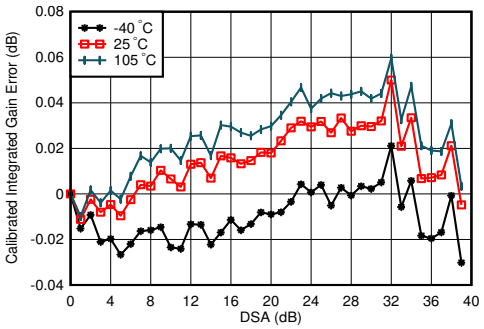


f_{DAC} = 8847.36MSPS, straight mode, matching at 2.6 GHz, channel with the median variation over DSA setting at 25°C
Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + (DSA Setting)

Figure 210. TX Uncalibrated Integrated Gain Error vs DSA Setting and Temperature at 2.6 GHz

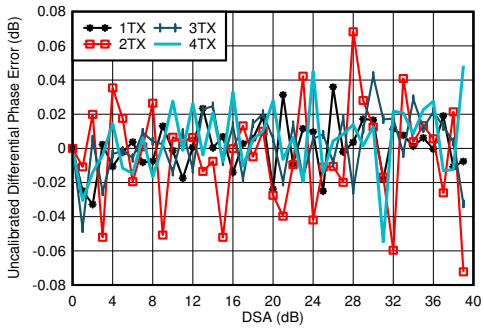
TX Typical Characteristics (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



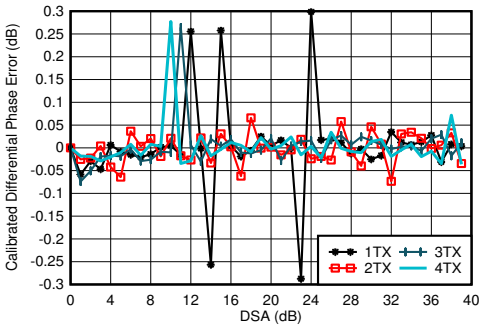
f_{DAC} = 8847.36MSPS, straight mode, matching at 2.6 GHz, channel with the median variation over DSA setting at 25°C
Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + (DSA Setting)

Figure 211. TX Calibrated Integrated Gain Error vs DSA Setting and Temperature at 2.6 GHz



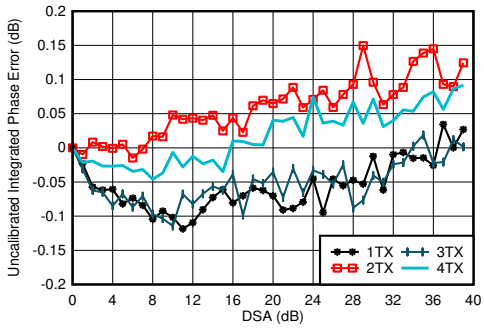
f_{DAC} = 8847.36MSPS, straight mode, matching at 2.6 GHz
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

Figure 212. TX Uncalibrated Differential Phase Error vs DSA Setting and Channel at 2.6 GHz



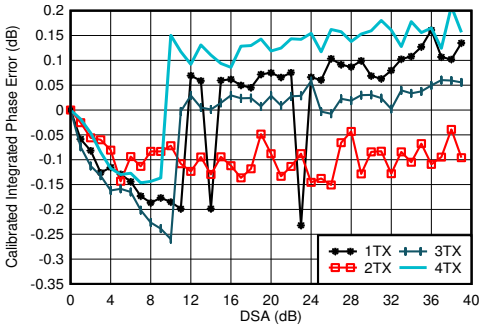
f_{DAC} = 8847.36MSPS, straight mode, matching at 2.6 GHz
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)
Phase DNL spike may occur at any DSA setting.

Figure 213. TX Calibrated Differential Phase Error vs DSA Setting and Channel at 2.6 GHz



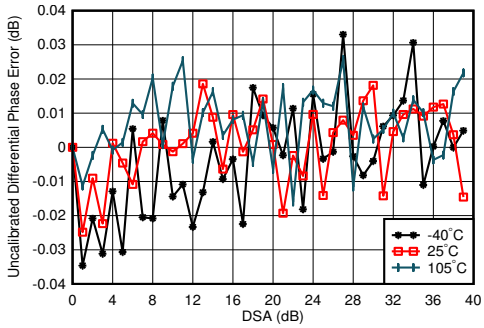
f_{DAC} = 8847.36MSPS, straight mode, matching at 2.6 GHz
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

Figure 214. TX Uncalibrated Integrated Phase Error vs DSA Setting and Channel at 2.6 GHz



f_{DAC} = 8847.36MSPS, straight mode, matching at 2.6 GHz
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

Figure 215. TX Calibrated Integrated Phase Error vs DSA Setting and Channel at 2.6 GHz

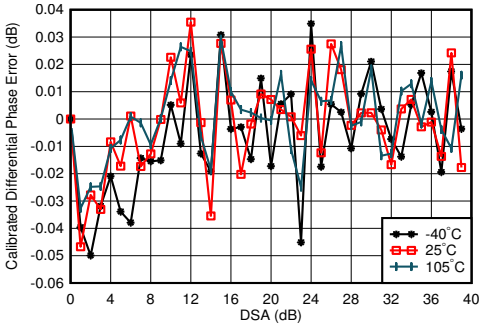


f_{DAC} = 8847.36MSPS, straight mode, matching at 2.6 GHz, channel with the median variation over DSA setting at 25°C
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

Figure 216. TX Uncalibrated Differential Phase Error vs DSA Setting and Temperature at 2.6 GHz

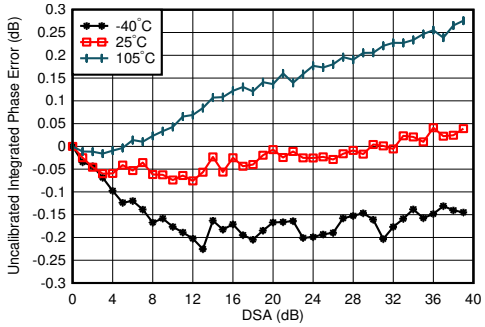
TX Typical Characteristics (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



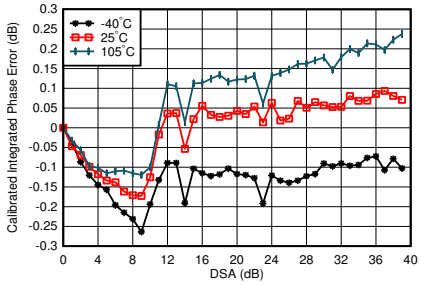
f_{DAC} = 8847.36MSPS, straight mode, matching at 2.6 GHz, channel with the median variation over DSA setting at 25°C
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

Figure 217. TX Calibrated Differential Phase Error vs DSA Setting and Temperature at 2.6 GHz



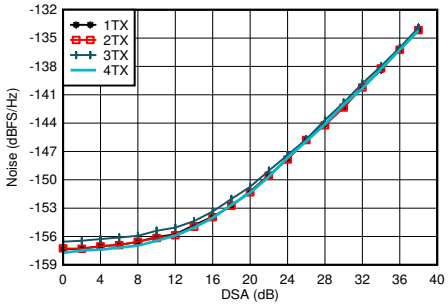
f_{DAC} = 8847.36MSPS, straight mode, matching at 2.6 GHz, channel with the medium variation over DSA setting at 25°C
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

Figure 218. TX Uncalibrated Integrated Phase Error vs DSA Setting and Temperature at 2.6 GHz



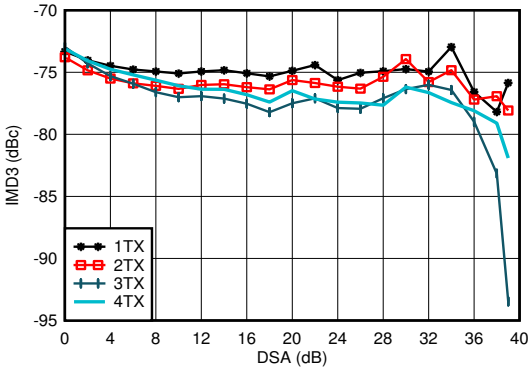
f_{DAC} = 8847.36MSPS, straight mode, matching at 2.6 GHz, channel with the median variation over DSA setting at 25°C
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

Figure 219. TX Calibrated Integrated Phase Error vs DSA Setting and Temperature at 2.6 GHz



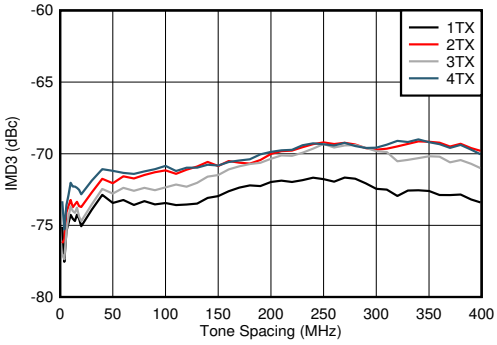
f_{DAC} = 8847.36MSPS, straight mode, matching at 2.6 GHz, P_{OUT} = –13 dBFS

Figure 220. TX Output Noise vs Channel and Attenuation at 2.6 GHz



f_{DAC} = 8847.36MSPS, straight mode, f_{CENTER} = 2.6 GHz, matching at 2.6 GHz, –13 dBFS each tone

Figure 221. TX IMD3 vs DSA Setting at 2.6 GHz

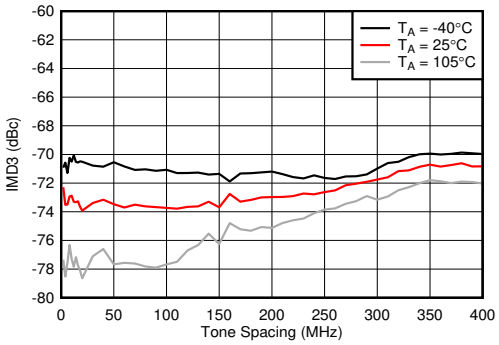


f_{DAC} = 8847.36MSPS, straight mode, f_{CENTER} = 2.6 GHz, matching at 2.6 GHz, –13 dBFS each tone

Figure 222. TX IMD3 vs Tone Spacing and Channel at 2.6 GHz

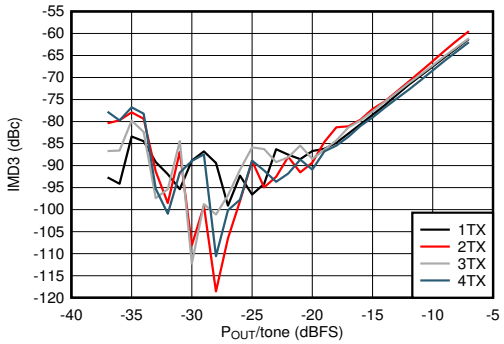
TX Typical Characteristics (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



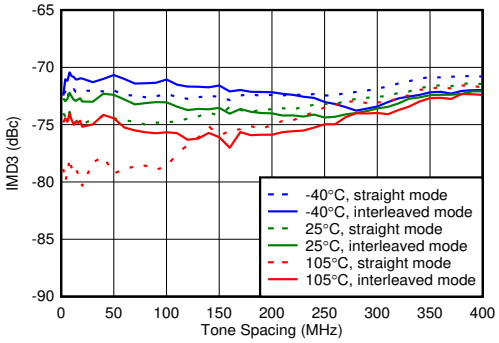
f_{DAC} = 8847.36MSPS, straight mode, f_{CENTER} = 2.6 GHz, matching at 2.6 GHz, –13 dBFS each tone, worst channel, dither = 1.

Figure 223. TX IMD3 vs Tone Spacing and Temperature at 2.6 GHz



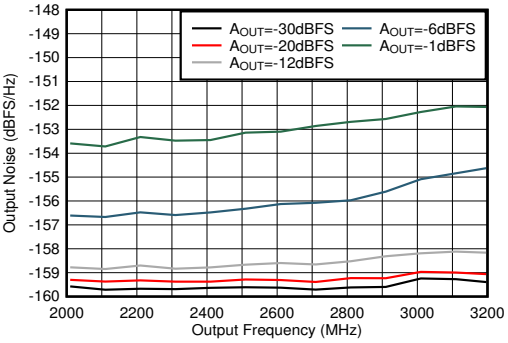
f_{DAC} = 8847.36MSPS, straight mode, f_{CENTER} = 2.6 GHz, $f_{SPACING}$ = 20 MHz, dither = 1, matching at 2.6 GHz

Figure 224. TX IMD3 vs Digital Level at 2.6 GHz



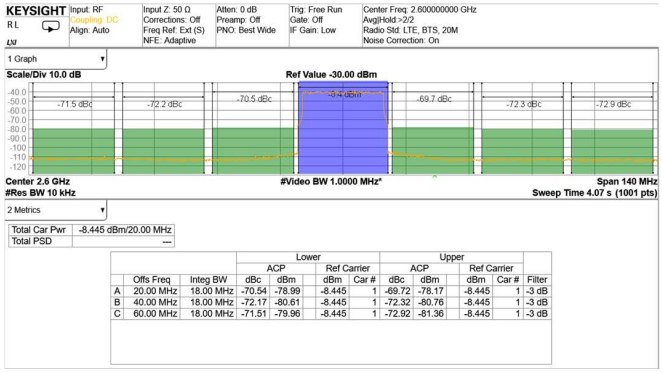
f_{DAC} = 8847.36MSPS, straight mode, f_{CENTER} = 2.6 GHz, matching at 2.6 GHz, –13 dBFS each tone

Figure 225. TX IMD3 vs Tone Spacing and Temperature



Matching at 2.6 GHz, Single tone, f_{DAC} = 11.79648GSPS, interleave mode, 40-MHz offset

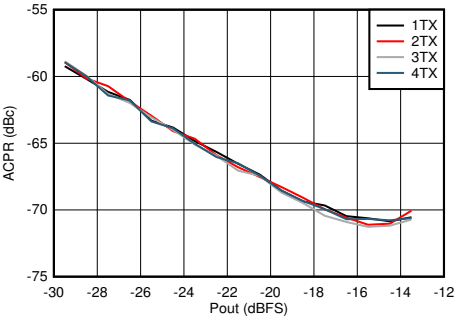
Figure 226. TX Single Tone Output Noise vs Frequency and Amplitude at 2.6 GHz



	Offs Freq	Integ BW	Lower ACP dBc	Lower ACP dBm	Lower Ref Carrier dBm	Lower Ref Carrier Car #	Upper ACP dBc	Upper ACP dBm	Upper Ref Carrier dBm	Upper Ref Carrier Car #	Filter
A	20.00 MHz	18.00 MHz	-70.54	-78.99	-8.445	1	-69.72	-78.17	-8.445	1	-3 dB
B	40.00 MHz	18.00 MHz	-72.17	-80.61	-8.445	1	-72.32	-80.76	-8.445	1	-3 dB
C	60.00 MHz	18.00 MHz	-71.51	-79.96	-8.445	1	-72.92	-81.36	-8.445	1	-3 dB

TM1.1, P_{OUT_RMS} = –13 dBFS

Figure 227. TX 20-MHz LTE Output Spectrum at 2.6 GHz (Band 41)

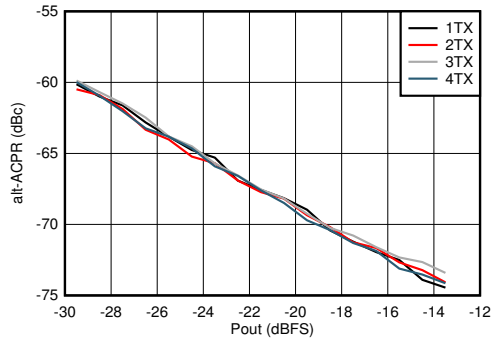


Matching at 2.6 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 228. TX 20-MHz LTE ACPR vs Digital Level at 2.6 GHz

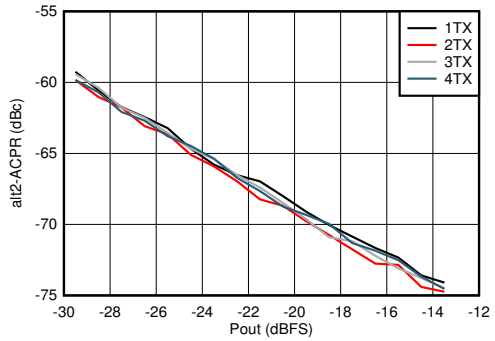
TX Typical Characteristics (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



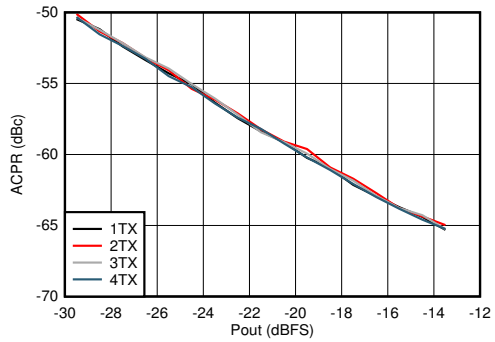
Matching at 2.6 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 229. TX 20-MHz LTE alt-ACPR vs Digital Level at 2.6 GHz



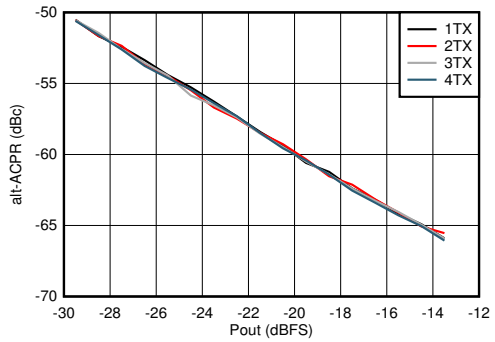
Matching at 2.6 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 230. TX 20-MHz LTE alt2-ACPR vs Digital Level at 2.6 GHz



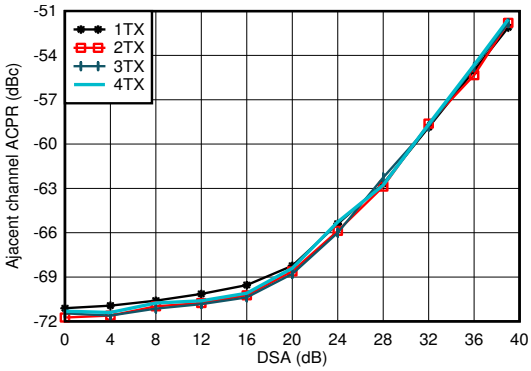
Matching at 2.6 GHz, single carrier 100-MHz BW TM1.1 NR

Figure 231. TX 100-MHz NR ACPR vs Digital Level at 2.6 GHz



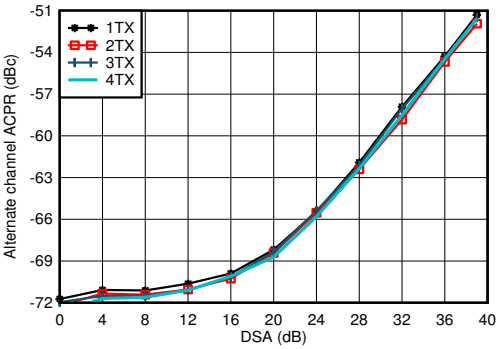
Matching at 2.6 GHz, single carrier 100-MHz BW TM1.1 NR

Figure 232. TX 100-MHz NR alt-ACPR vs Digital Level at 2.6 GHz



Matching at 2.6 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 233. TX 20-MHz LTE ACPR vs DSA at 2.6 GHz

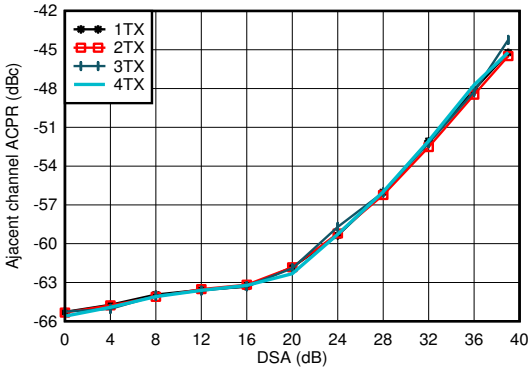


Matching at 2.6 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 234. TX 20-MHz LTE alt-ACPR vs DSA at 2.6 GHz

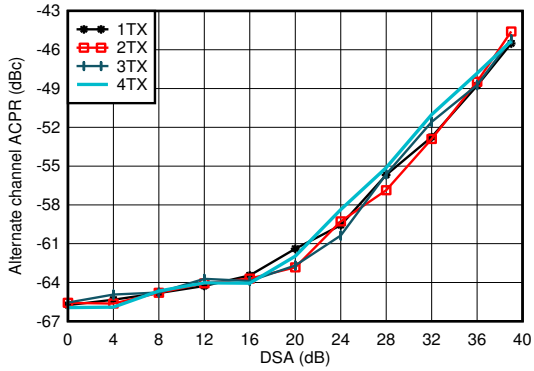
TX Typical Characteristics (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



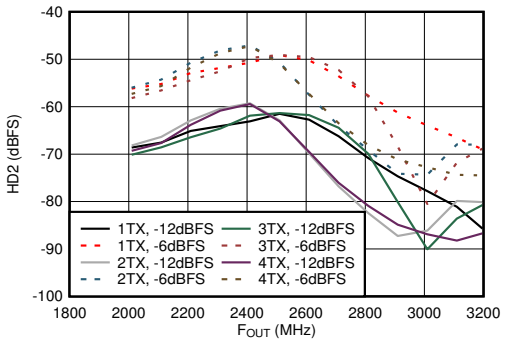
Matching at 2.6 GHz, single carrier 100-MHz BW TM1.1 NR

Figure 235. TX 100-MHz NR ACPR vs DSA at 2.6 GHz



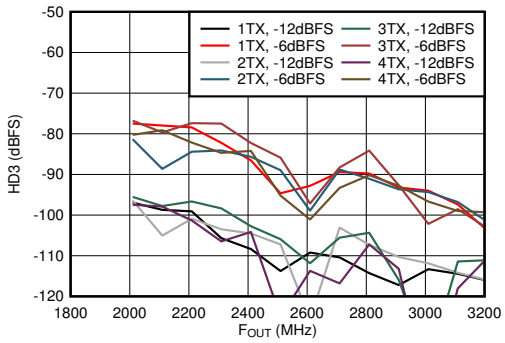
Matching at 2.6 GHz, single carrier 100-MHz BW TM1.1 NR

Figure 236. TX 100-MHz NR alt-ACPR vs DSA at 2.6 GHz



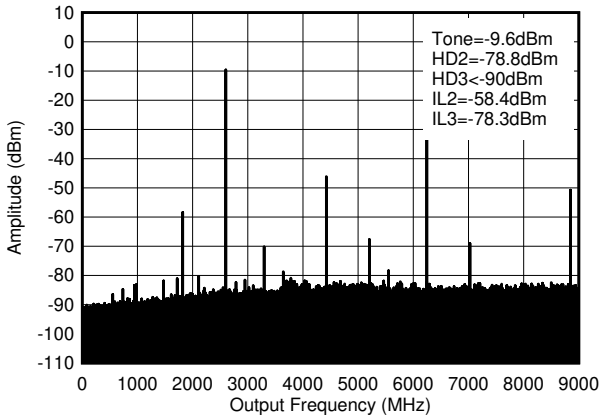
Matching at 2.6 GHz, f_{DAC} = 11.79648GSPS, interleave mode, normalized to output power at harmonic frequency

Figure 237. TX HD2 vs Digital Amplitude and Output Frequency at 2.6 GHz



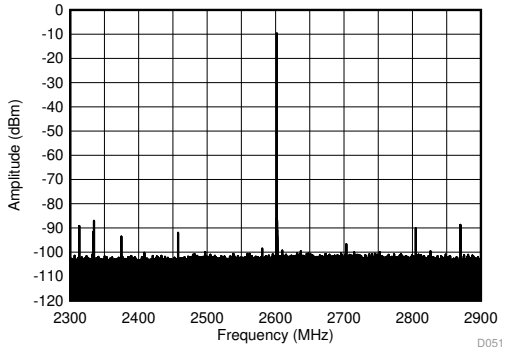
Matching at 2.6 GHz, f_{DAC} = 11.79648GSPS, interleave mode, normalized to output power at harmonic frequency

Figure 238. TX HD3 vs Digital Amplitude and Output Frequency at 2.6 GHz



f_{DAC} = 8847.36MSPS, interleave mode, 2.6 GHz matching, includes PCB and cable losses. ILn = $f_S/n \pm f_{OUT}$.

Figure 239. TX Single Tone (–12 dBFS) Output Spectrum at 2.6 GHz (0-f_{DAC})

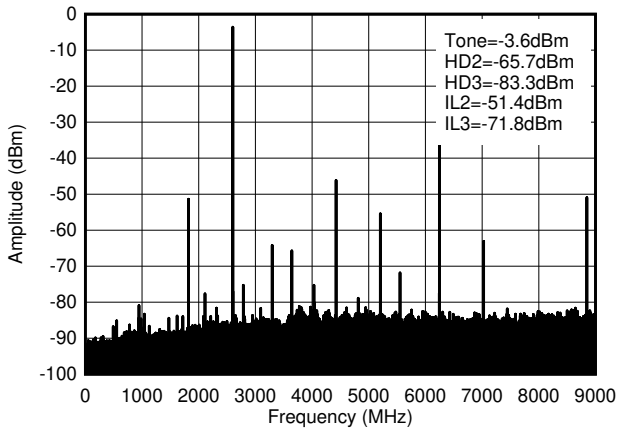


f_{DAC} = 8847.36MSPS, interleave mode, 2.6 GHz matching, includes PCB and cable losses

Figure 240. TX Single Tone (–12 dBFS) Output Spectrum at 2.6 GHz (±300 MHz)

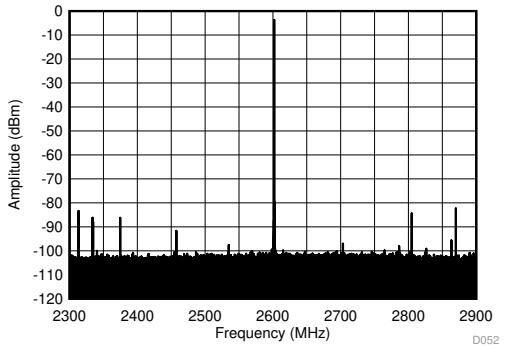
TX Typical Characteristics (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



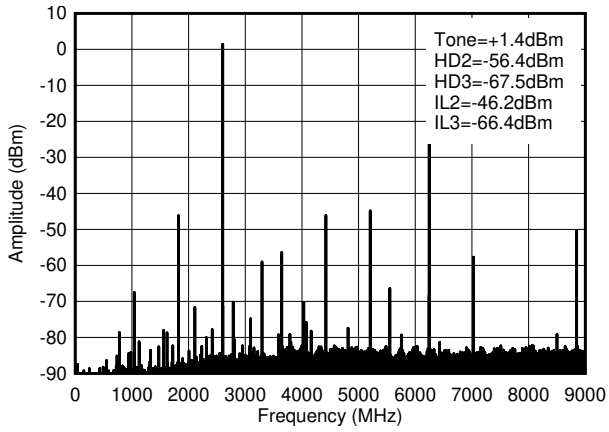
f_{DAC} = 8847.36MSPS, interleave mode, 2.6 GHz matching, includes PCB and cable losses. ILn = $f_S/n \pm f_{OUT}$.

Figure 241. TX Single Tone (–6 dBFS) Output Spectrum at 2.6 GHz (0-f_{DAC})



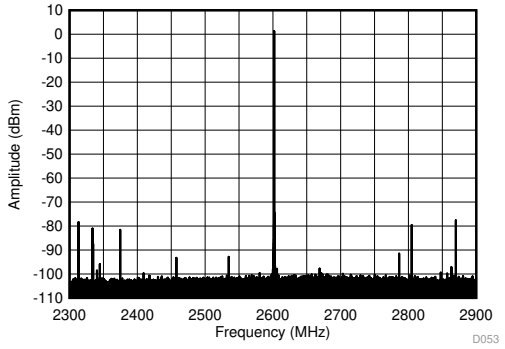
f_{DAC} = 8847.36MSPS, interleave mode, 2.6 GHz matching, includes PCB and cable losses

Figure 242. TX Single Tone (–6 dBFS) Output Spectrum at 2.6 GHz (±300 MHz)



f_{DAC} = 8847.36MSPS, interleave mode, 2.6 GHz matching, includes PCB and cable losses. ILn = $f_S/n \pm f_{OUT}$.

Figure 243. TX Single Tone (–1 dBFS) Output Spectrum at 2.6 GHz (0-f_{DAC})

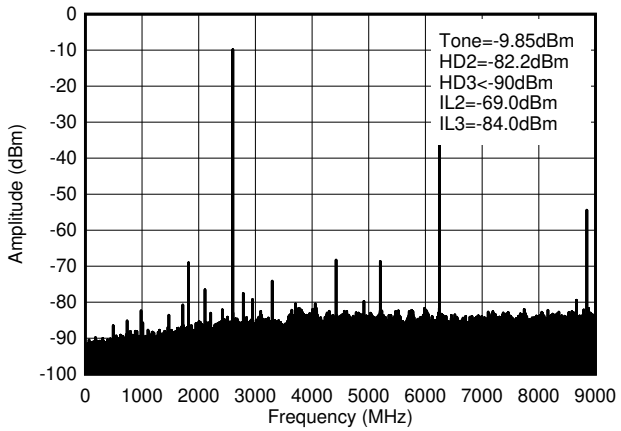


f_{DAC} = 8847.36MSPS, interleave mode, 2.6 GHz matching, includes PCB and cable losses

Figure 244. TX Single Tone (–1 dBFS) Output Spectrum at 2.6 GHz (±300 MHz)

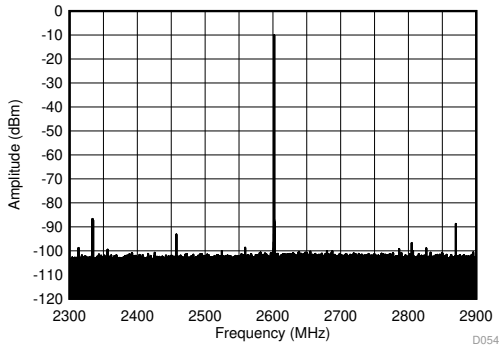
TX Typical Characteristics (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



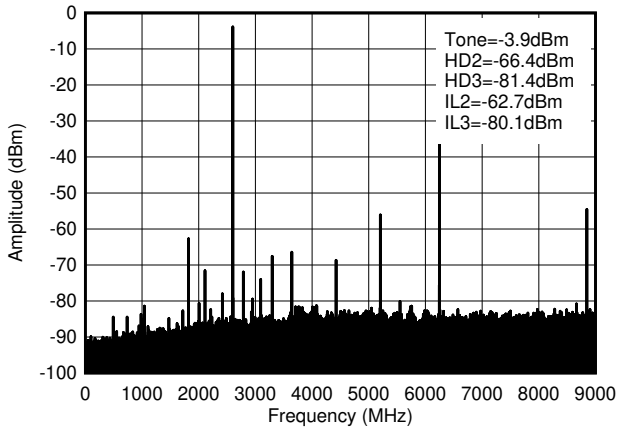
f_{DAC} = 8847.36MSPS, straight mode, 2.6 GHz matching, includes PCB and cable losses. ILn = $f_S/n \pm f_{OUT}$ and is due to mixing with digital clocks.

Figure 245. TX Single Tone (–12 dBFS) Output Spectrum at 2.6 GHz (0-f_{DAC})



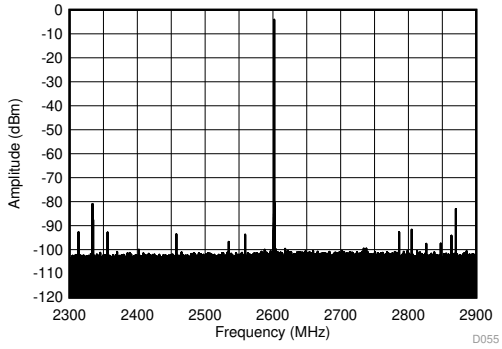
f_{DAC} = 8847.36MSPS, straight mode, 2.6 GHz matching, includes PCB and cable losses

Figure 246. TX Single Tone (–12 dBFS) Output Spectrum at 2.6 GHz (±300 MHz)



f_{DAC} = 8847.36MSPS, straight mode, 2.6 GHz matching, includes PCB and cable losses. ILn = $f_S/n \pm f_{OUT}$ and is due to mixing with digital clocks.

Figure 247. TX Single Tone (–6 dBFS) Output Spectrum at 2.6 GHz (0-f_{DAC})

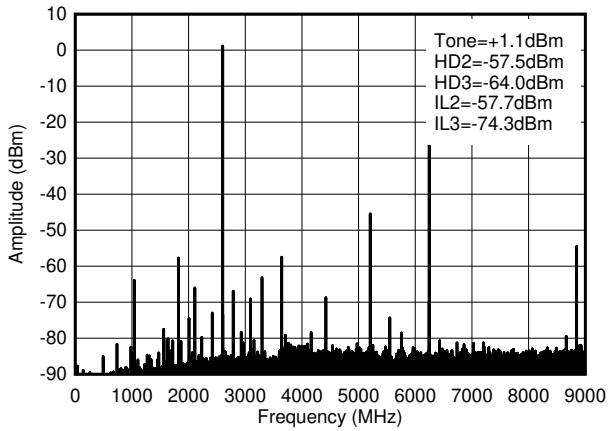


f_{DAC} = 8847.36MSPS, straight mode, 2.6 GHz matching, includes PCB and cable losses

Figure 248. TX Single Tone (–6 dBFS) Output Spectrum at 2.6 GHz (±300 MHz)

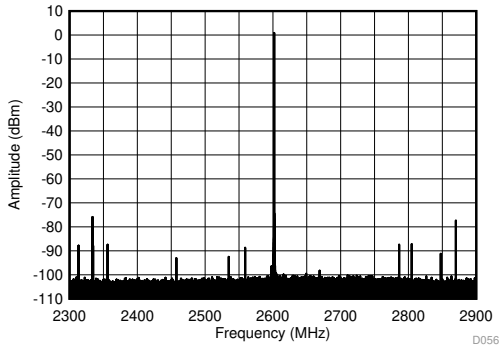
TX Typical Characteristics (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



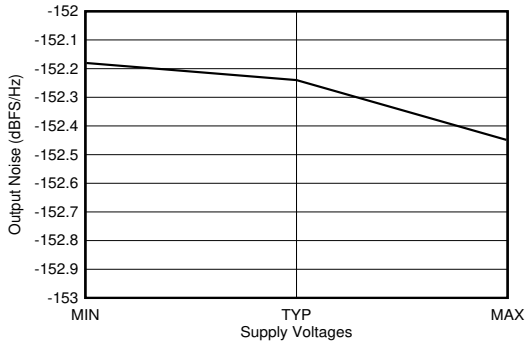
f_{DAC} = 8847.36MSPS, straight mode, 2.6 GHz matching, includes PCB and cable losses. ILn = $f_S/n \pm f_{OUT}$ and is due to mixing with digital clocks.

Figure 249. TX Single Tone (–1 dBFS) Output Spectrum at 2.6 GHz (0-f_{DAC})



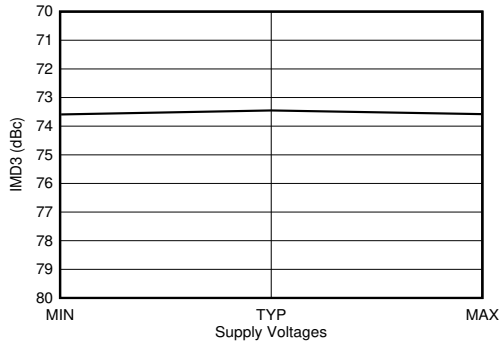
f_{DAC} = 8847.36MSPS, straight mode, 2.6 GHz matching, includes PCB and cable losses

Figure 250. TX Single Tone (–1 dBFS) Output Spectrum at 2.6 GHz (±300 MHz)



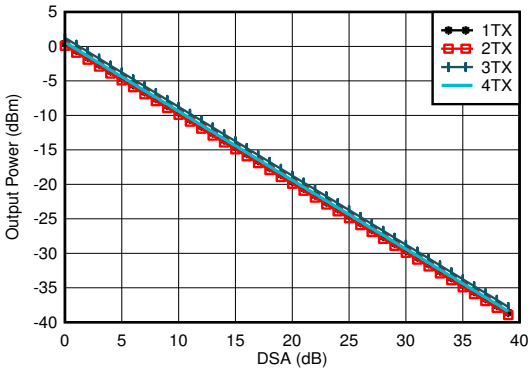
f_{DAC} = 11796.48MSPS, interleave mode, 2.6 GHz matching. 40-MHz offset from tone. Output Power = –1 dBFS. All supplies simultaneously at MIN, TYP, or MAX voltages.

Figure 251. TX Output Noise vs Supply Voltage at 2.6 GHz



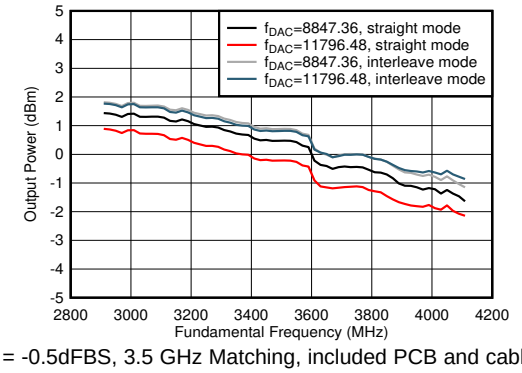
f_{DAC} = 11796.48MSPS, interleave mode, 2.6 GHz matching. 40-MHz offset from tone. Output Power = –13 dBFS. All supplies simultaneously at MIN, TYP, or MAX voltages.

Figure 252. TX IMD3 vs Supply Voltage at 2.6 GHz



A_{out} = -0.5dFBS, 3.5 GHz Matching, included PCB and cable losses

Figure 253. TX Output Power vs DSA Setting at 3.5 GHz

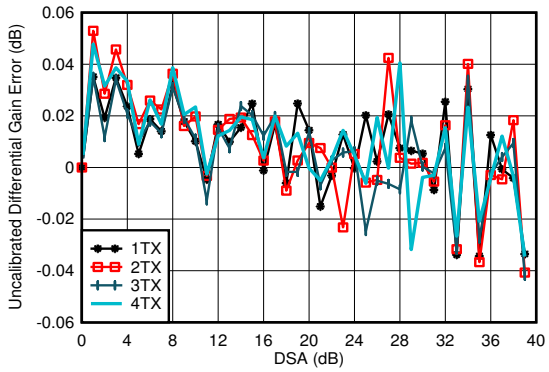


A_{out} = -0.5dFBS, 3.5 GHz Matching, included PCB and cable losses

Figure 254. TX Output Power vs Frequency

TX Typical Characteristics (continued)

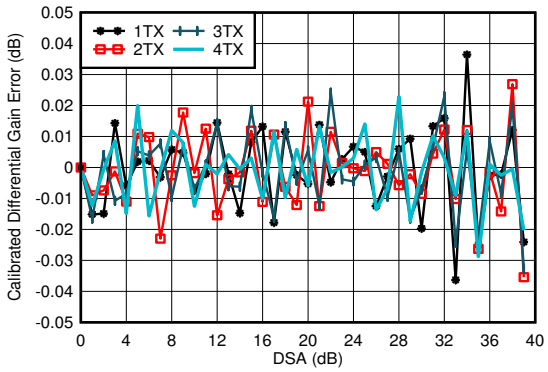
Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



3.5 GHz Matching, included PCB and cable losses

Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

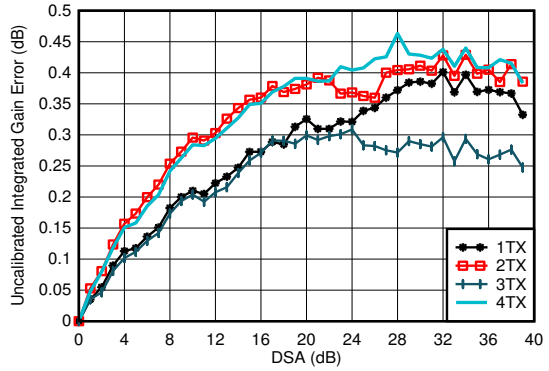
Figure 255. TX Uncalibrated Differential Gain Error vs DSA Setting and Channel at 3.5 GHz



3.5 GHz Matching, included PCB and cable losses

Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

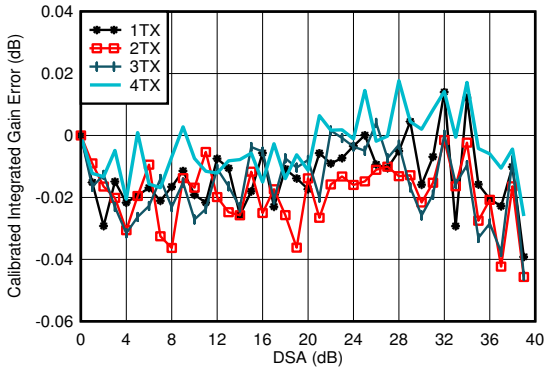
Figure 256. TX Calibrated Differential Gain Error vs DSA Setting and Channel at 3.5 GHz



3.5 GHz Matching, included PCB and cable losses

Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + (DSA Setting)

Figure 257. TX Uncalibrated Integrated Gain Error vs DSA Setting and Channel at 3.5 GHz



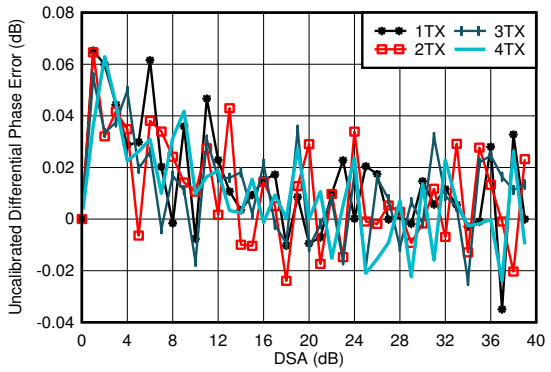
3.5 GHz Matching, included PCB and cable losses

Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + (DSA Setting)

Figure 258. TX Calibrated Integrated Gain Error vs DSA Setting and Channel at 3.5 GHz

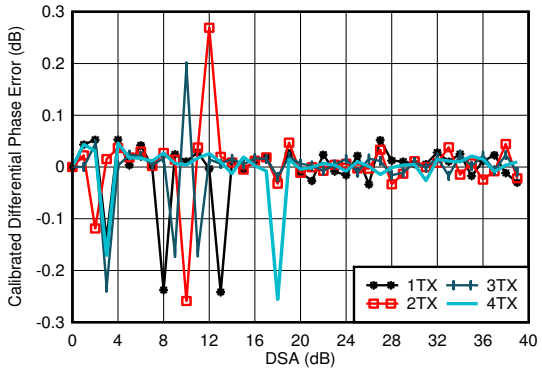
TX Typical Characteristics (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



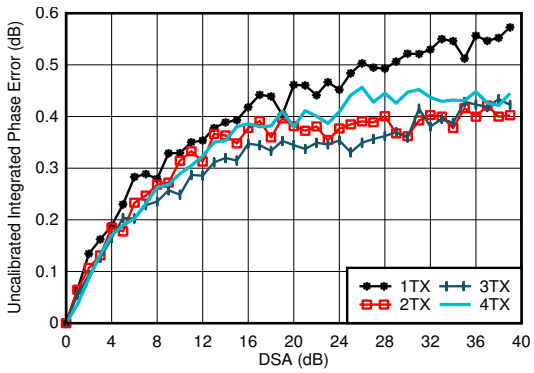
3.5 GHz Matching, included PCB and cable losses

Figure 259. TX Uncalibrated Differential Phase Error vs DSA Setting and Channel at 3.5 GHz



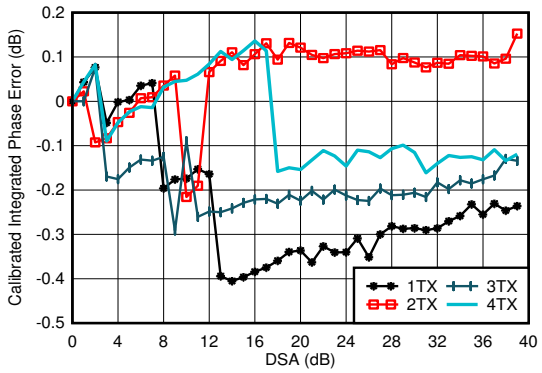
3.5 GHz Matching, included PCB and cable losses
Phase DNL spike may occur at any DSA setting.

Figure 260. TX Calibrated Differential Phase Error vs DSA Setting and Channel at 3.5 GHz



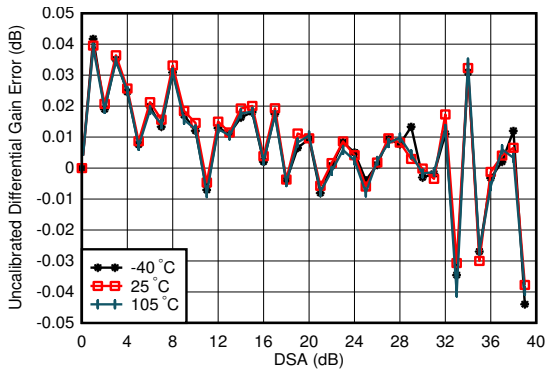
3.5 GHz Matching, included PCB and cable losses

Figure 261. TX Uncalibrated Integrated Phase Error vs DSA Setting and Channel at 3.5 GHz



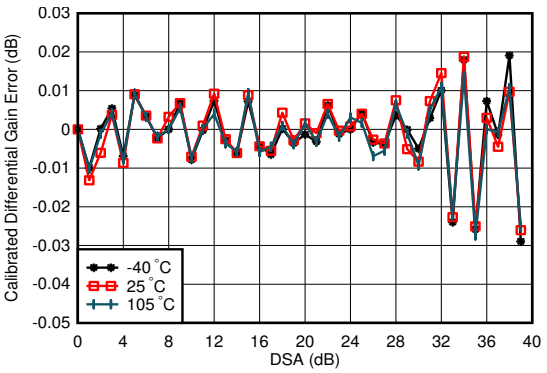
3.5 GHz Matching, included PCB and cable losses

Figure 262. TX Calibrated Integrated Phase Error vs DSA Setting and Channel at 3.5 GHz



3.5 GHz Matching, 0TX

Figure 263. TX Uncalibrated Differential Gain Error vs DSA Setting and Temperature at 3.5 GHz

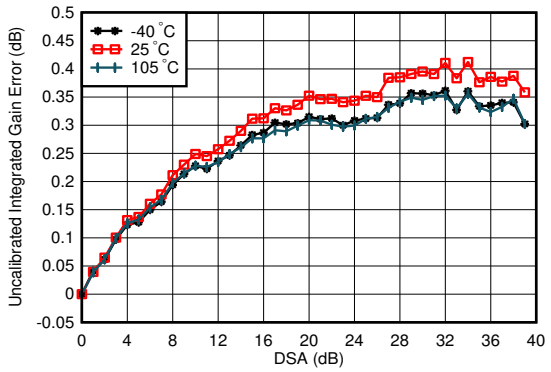


3.5 GHz Matching, 0TX, Calibrated at 25°C

Figure 264. TX Calibrated Differential Gain Error vs DSA Setting and Temperature at 3.5 GHz

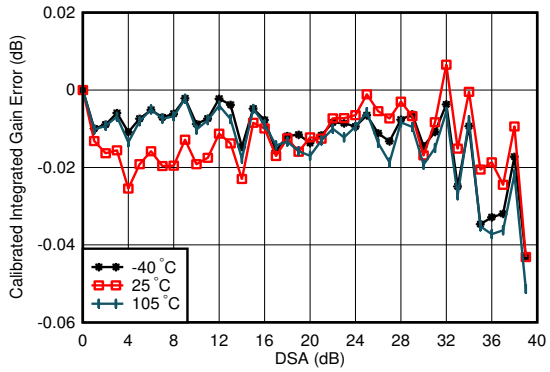
TX Typical Characteristics (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



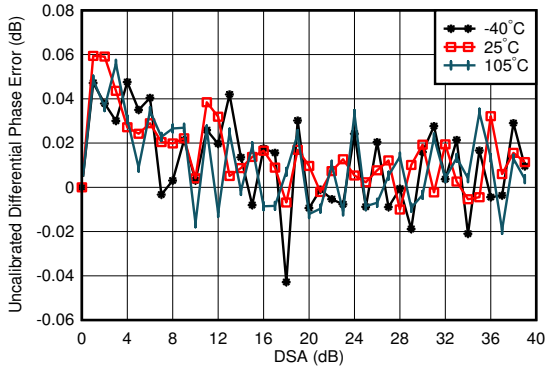
3.5 GHz Matching, 0TX

Figure 265. TX Uncalibrated Integrated Gain Error vs DSA Setting and Temperature at 3.5 GHz



3.5 GHz Matching, 0TX, Calibrated at 25°C

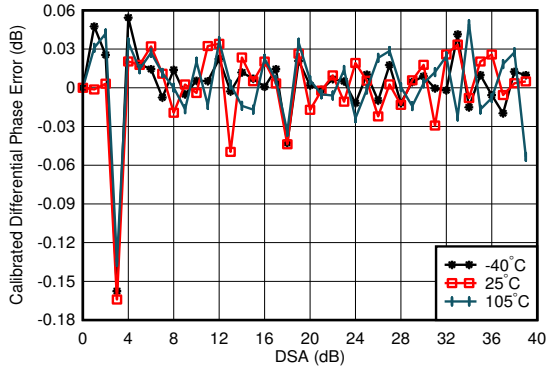
Figure 266. TX Calibrated Integrated Gain Error vs DSA Setting and Temperature at 3.5 GHz



3.5 GHz Matching, 0TX

Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

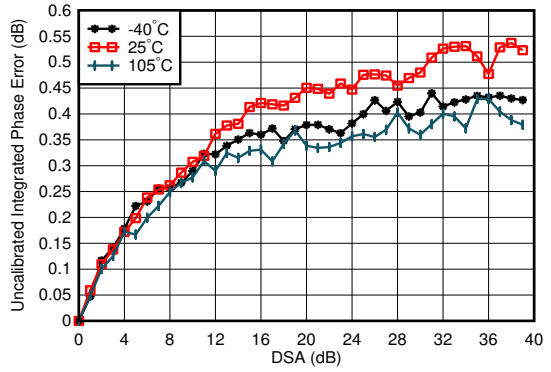
Figure 267. TX Uncalibrated Differential Phase Error vs DSA setting and Temperature at 3.5 GHz



3.5 GHz Matching, 0TX, Calibrated at 25°C

Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

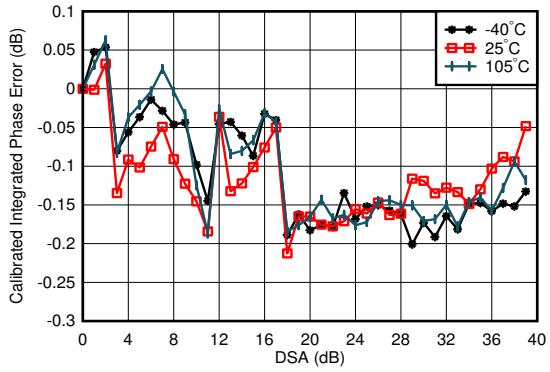
Figure 268. TX Calibrated Differential Phase Error vs DSA Setting and Temperature at 3.5 GHz



3.5 GHz Matching, 0TX

Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting=0)

Figure 269. TX Uncalibrated Integrated Phase Error vs DSA Setting and Temperature at 3.5 GHz



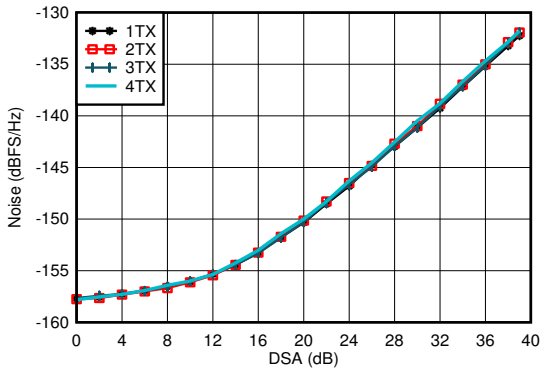
3.5 GHz Matching, 0TX, Calibrated at 25°C

Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

Figure 270. TX Calibrated Integrated Phase Error vs DSA Setting and Temperature at 3.5 GHz

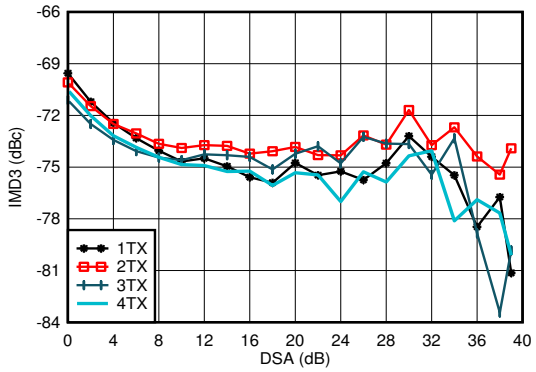
TX Typical Characteristics (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



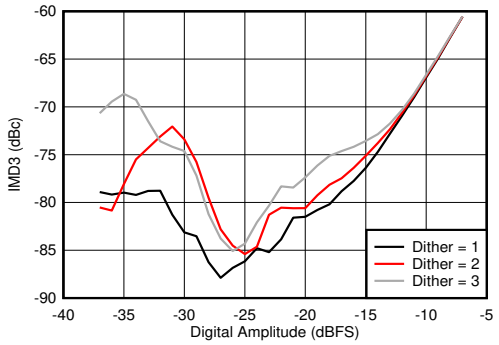
f_{DAC}=11796.48MSPS, interleave mode, matching at 3.5GHz, A_{out} = –13 dBFS.

Figure 271. TX NSD vs DSA Setting at 3.5 GHz



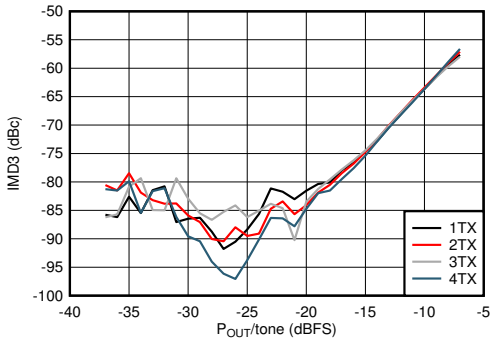
20-MHz tone spacing, 3.5 GHz Matching, –13 dBFS each tone, included PCB and cable losses

Figure 272. TX IMD3 vs DSA Setting at 3.5 GHz



20-MHz tone spacing, 3.5 GHz Matching, included PCB and cable losses

Figure 273. TX IMD3 vs Digital Amplitude and Dither Setting at 3.5 GHz



20-MHz tone spacing, 3.5 GHz Matching

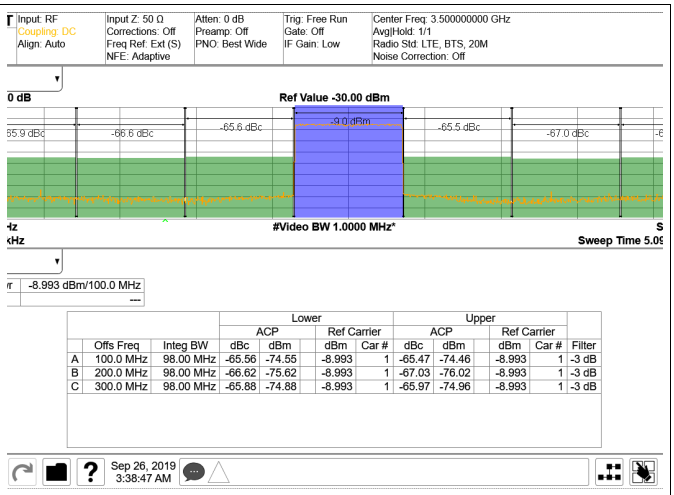
Figure 274. TX IMD3 vs Digital Amplitude and Channel at 3.5 GHz

TX Typical Characteristics (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled

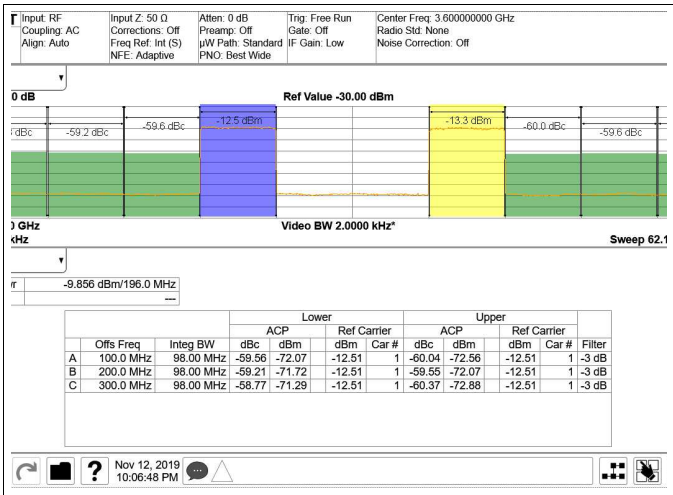
3.5 GHz Matching, single carrier 20-MHz BW TM1.1 LTE

Figure 275. TX 20-MHz LTE Output Spectrum at 3.5 GHz (Band 42)



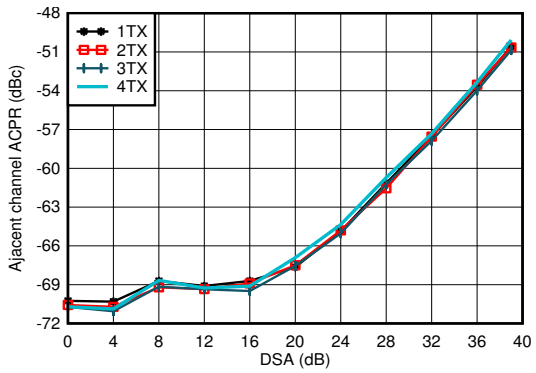
3.5 GHz Matching, single carrier 100-MHz BW NR TM1.1

Figure 276. TX 100-MHz NR Output Spectrum at 3.5 GHz (Band 42)



3.5 GHz Matching, single carrier 100-MHz BW NR TM1.1

Figure 277. TX 2 carrier 100-MHz NR Output Spectrum at 3.45 GHz and 3.75 GHz

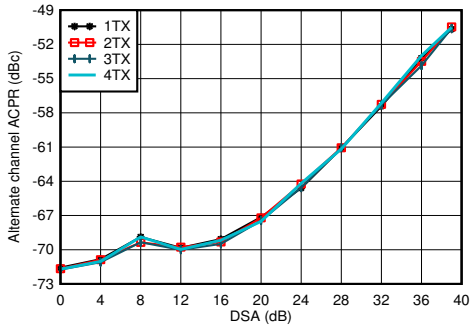


3.5 GHz Matching, single carrier 20-MHz BW TM1.1 LTE

Figure 278. TX 20-MHz LTE ACPR vs DSA Setting at 3.5 GHz

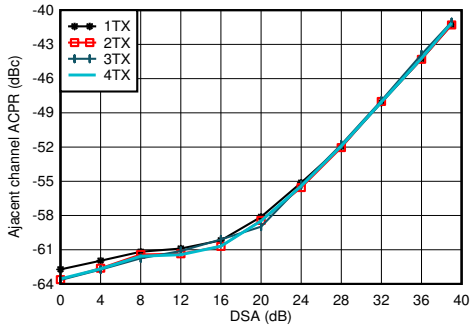
TX Typical Characteristics (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



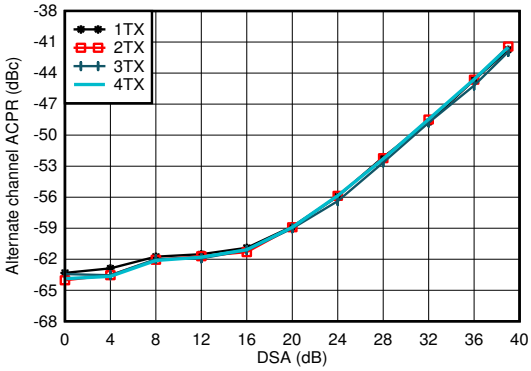
3.5 GHz Matching, single carrier 20-MHz BW TM1.1 LTE

Figure 279. TX 20-MHz LTE alt-ACPR vs DSA Setting at 3.5 GHz



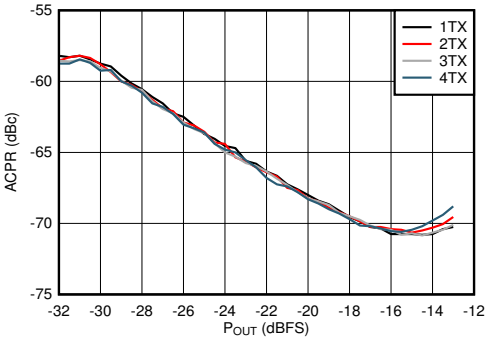
3.5 GHz Matching, single carrier 100-MHz BW NR TM1.1

Figure 280. TX 100-MHz NR ACPR vs DSA Setting at 3.5 GHz



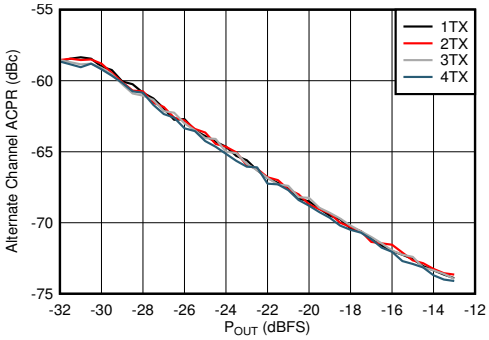
3.5 GHz Matching, single carrier 100-MHz BW NR TM1.1

Figure 281. TX 100-MHz NR alt-ACPR vs DSA Setting at 3.5 GHz



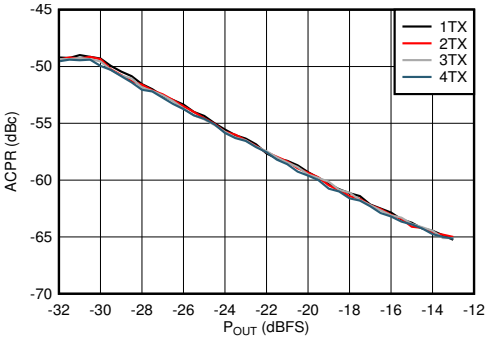
3.5 GHz Matching, single carrier 20-MHz BW TM1.1 LTE

Figure 282. TX 20-MHz LTE ACPR vs Digital Level at 3.5 GHz



3.5 GHz Matching, single carrier 20-MHz BW TM1.1 LTE

Figure 283. TX 20-MHz LTE alt-ACPR vs Digital Level at 3.5 GHz

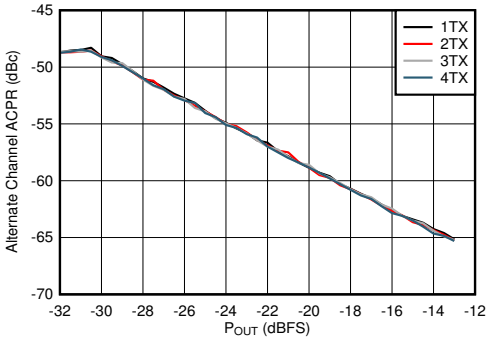


3.5 GHz Matching, single carrier 100-MHz BW NR TM1.1

Figure 284. TX 100-MHz NR ACPR vs Digital Level at 3.5 GHz

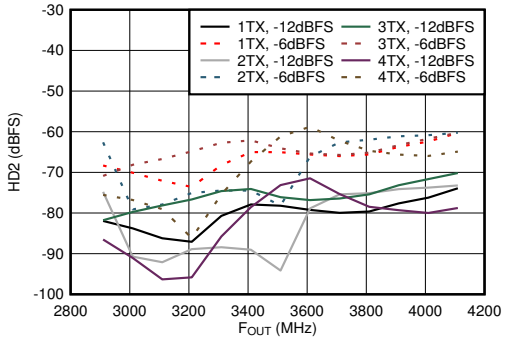
TX Typical Characteristics (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



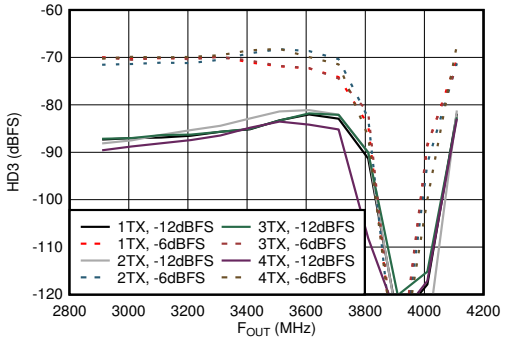
3.5 GHz Matching, single carrier 100-MHz BW NR TM1.1

Figure 285. TX 100-MHz NR alt-ACPR vs Digital Level at 3.5 GHz



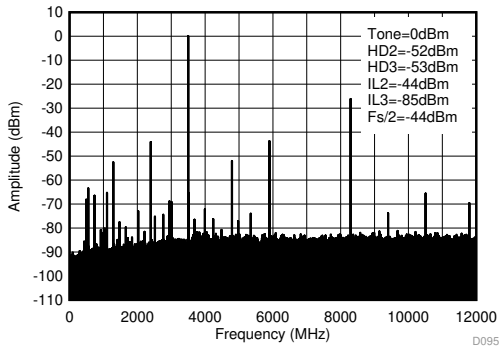
Matching at 3.5 GHz, f_{DAC} = 11.79648GSPS, interleave mode, normalized to output power at harmonic frequency

Figure 286. TX Single Tone HD2 vs Frequency and Digital Level at 3.5 GHz



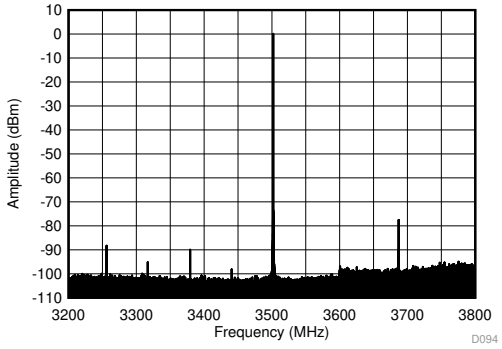
Matching at 3.5 GHz, f_{DAC} = 11.79648GSPS, interleave mode, normalized to output power at harmonic frequency. Dip is due to HD3 falling near DC.

Figure 287. TX Single Tone HD3 vs Frequency and Digital Level at 3.5 GHz



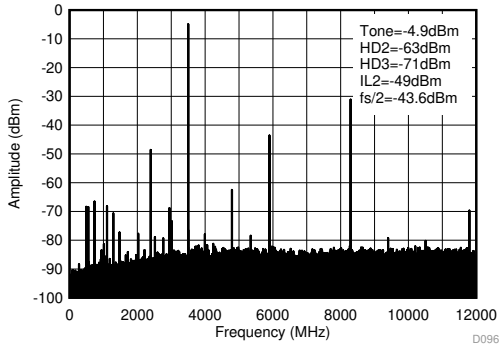
Matching at 3.5 GHz, f_{DAC} = 11.79648GSPS, interleave mode.

Figure 288. TX Single Tone (–1 dBFS) Output Spectrum at 3.5 GHz (0 - f_{DAC})



Matching at 3.5 GHz, f_{DAC} = 11.79648GSPS, interleave mode.

Figure 289. TX Single Tone (–1 dBFS) Output Spectrum at 3.5 GHz (±300 MHz)

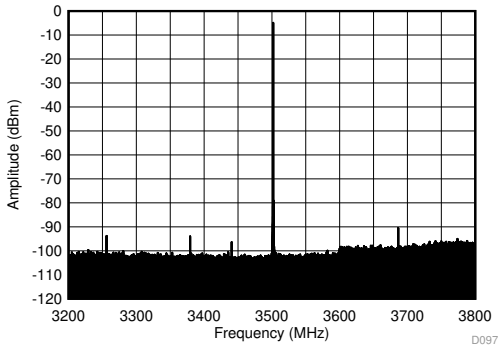


Matching at 3.5 GHz, f_{DAC} = 11.79648GSPS, interleave mode.

Figure 290. TX Single Tone (–6 dBFS) Output Spectrum at 3.5 GHz (0-f_{DAC})

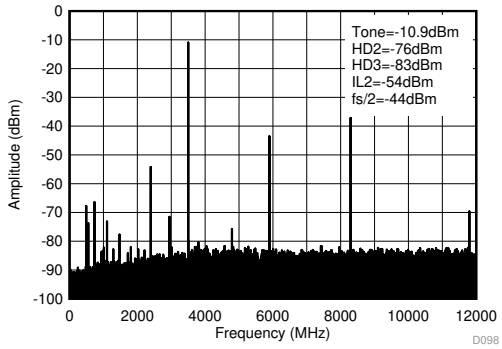
TX Typical Characteristics (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



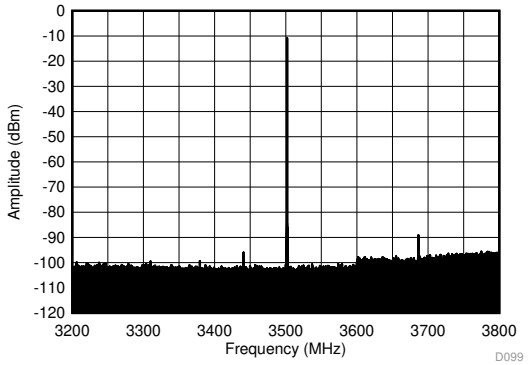
Matching at 3.5 GHz, f_{DAC} = 11.79648GSPS, interleave mode.

Figure 291. TX Single Tone (–6 dBFS) Output Spectrum at 3.5 GHz (±300 MHz)



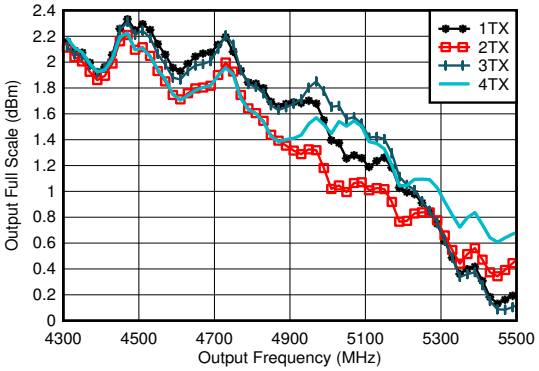
Matching at 3.5 GHz, f_{DAC} = 11.79648GSPS, interleave mode.

Figure 292. TX Single Tone (–12 dBFS) Output Spectrum at 3.5 GHz (0-f_{DAC})



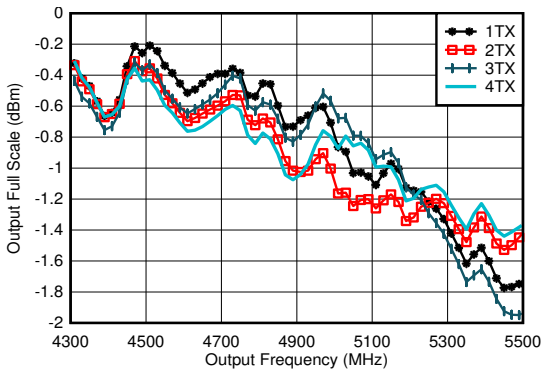
Matching at 3.5 GHz, f_{DAC} = 11.79648GSPS, interleave mode.

Figure 293. TX Single Tone (–12 dBFS) Output Spectrum at 3.5 GHz (±300 MHz)



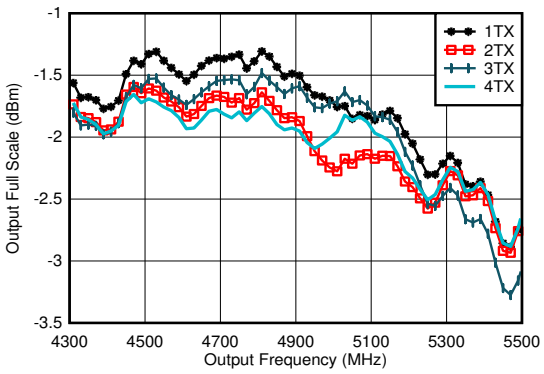
Excluding PCB and cable losses, A_{out} = -0.5dFBS, DSA = 0, 4.9 GHz matching

Figure 294. TX Full Scale vs RF Frequency and Channel at 11796.48MSPS



Excluding PCB and cable losses, A_{out} = -0.5dFBS, DSA = 0, 4.9 GHz matching

Figure 295. TX Full Scale vs RF Frequency and Channel at 5898.24MSPS, Straight Mode, 2nd Nyquist Zone

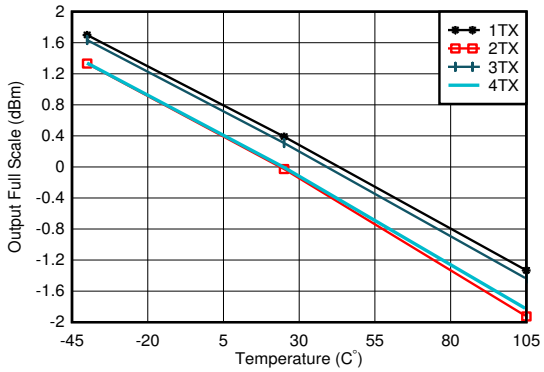


Excluding PCB and cable losses, A_{out} = -0.5dFBS, DSA = 0, 4.9 GHz matching

Figure 296. TX Full Scale vs RF Frequency and Channel at 8847.36MSPS, Straight Mode, 2nd Nyquist Zone

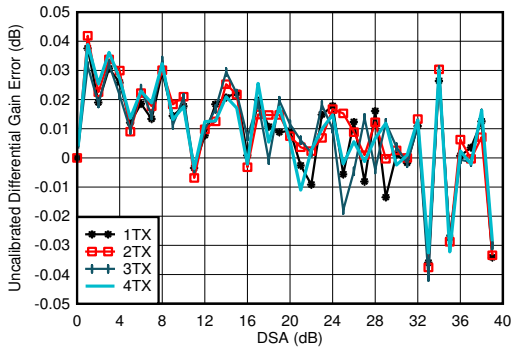
TX Typical Characteristics (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



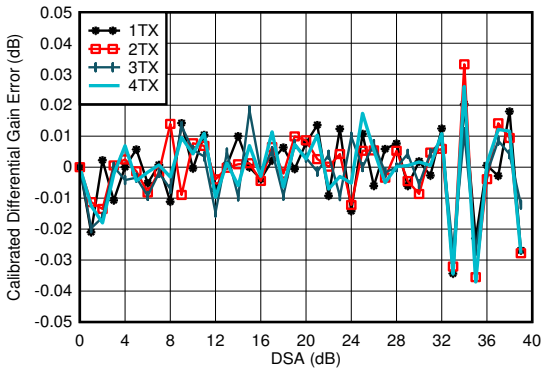
f_{DAC} = 11796.48 MSPS, A_{out} = -0.5dFBS, matching 4.9 GHz

Figure 297. TX Output Power vs DSA Setting and Channel at 4.9 GHz



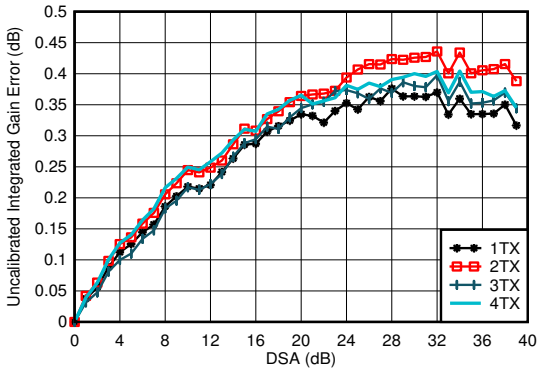
f_{DAC}=11796.48MSPS, interleave mode, matching at 4.9 GHz
Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

Figure 298. TX Uncalibrated Differential Gain Error vs DSA Setting and Channel at 4.9 GHz



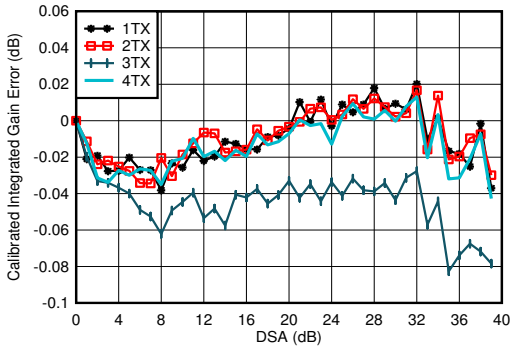
f_{DAC}=11796.48MSPS, interleave mode, matching at 4.9 GHz
Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

Figure 299. TX Calibrated Differential Gain Error vs DSA Setting and Channel at 4.9 GHz



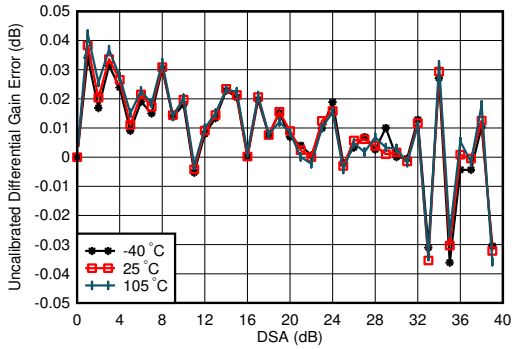
f_{DAC}=11796.48MSPS, interleave mode, matching at 4.9 GHz
Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + (DSA Setting)

Figure 300. TX Uncalibrated Integrated Gain Error vs DSA Setting and Channel at 4.9 GHz



f_{DAC} = 11796.48MSPS, interleave mode, matching at 4.9 GHz
Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + (DSA Setting)

Figure 301. TX Calibrated Integrated Gain Error vs DSA Setting and Channel at 4.9 GHz

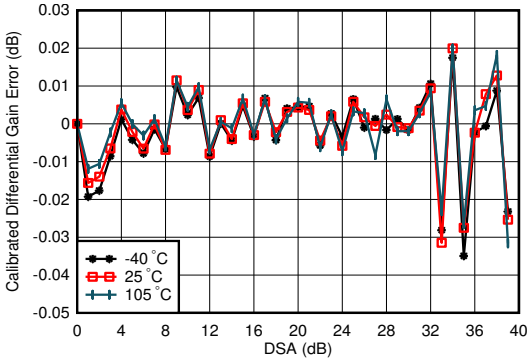


f_{DAC} = 11796.48MSPS, interleaved mode, matching at 4.9 GHz
Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

Figure 302. TX Uncalibrated Differential Gain Error vs DSA Setting and Temperature at 4.9 GHz

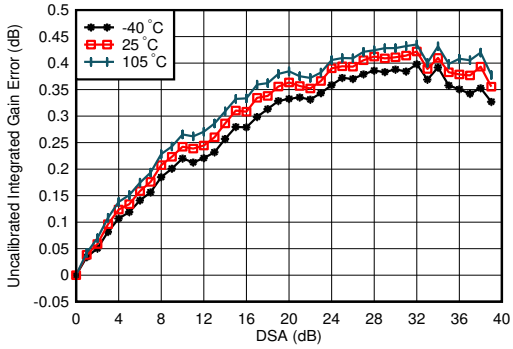
TX Typical Characteristics (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



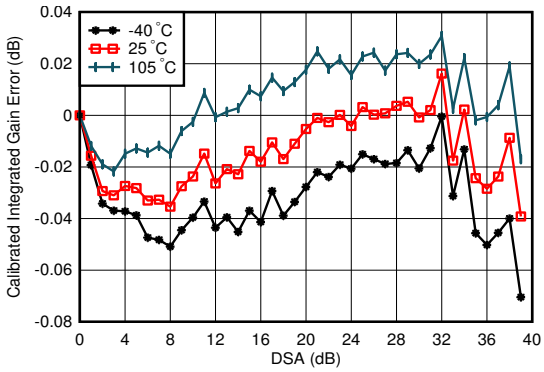
f_{DAC} = 11796.48MSPS, interleaved mode, matching at 4.9 GHz
Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

Figure 303. TX Calibrated Differential Gain Error vs DSA Setting and Temperature at 4.9 GHz



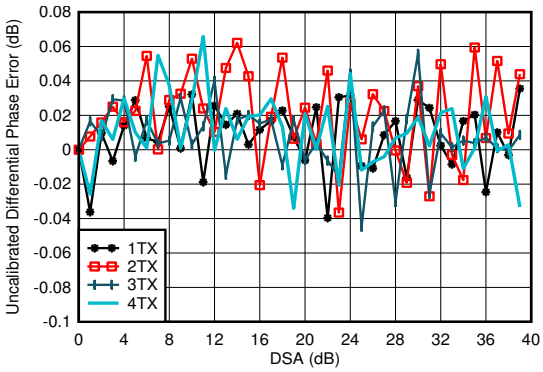
f_{DAC} = 11796.48MSPS, interleaved mode, matching at 4.9 GHz
Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + (DSA Setting)

Figure 304. TX Uncalibrated Integrated Gain Error vs DSA Setting and Temperature at 4.9 GHz



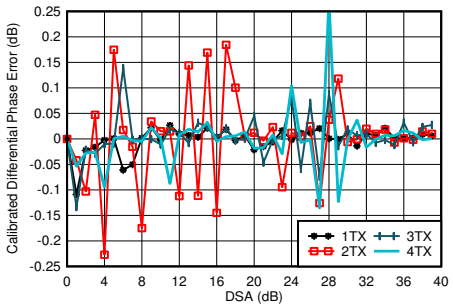
f_{DAC} = 11796.48MSPS, interleaved mode, matching at 4.9 GHz
Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + (DSA Setting)

Figure 305. TX Calibrated Integrated Gain Error vs DSA Setting and Temperature at 4.9 GHz



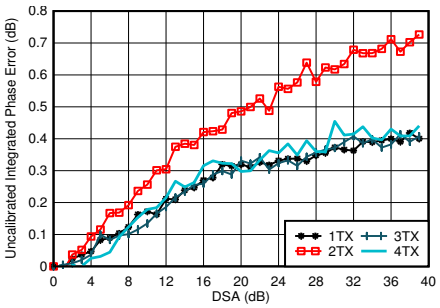
f_{DAC} = 11796.48MSPS, interleaved mode, matching at 4.9 GHz
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

Figure 306. TX Uncalibrated Differential Phase Error vs DSA Setting and Channel at 4.9 GHz



f_{DAC} = 11796.48MSPS, interleaved mode, matching at 4.9 GHz
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)
Phase DNL spike may occur at any DSA setting.

Figure 307. TX Calibrated Differential Phase Error vs DSA Setting and Channel at 4.9 GHz

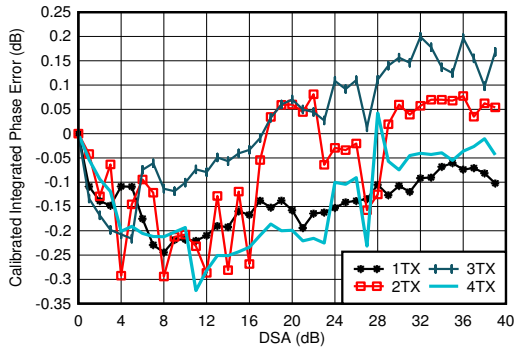


f_{DAC} = 11796.48MSPS, interleaved mode, matching at 4.9 GHz
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

Figure 308. TX Uncalibrated Integrated Phase Error vs DSA Setting and Channel at 4.9 GHz

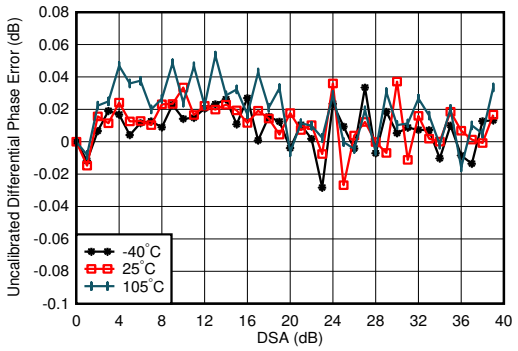
TX Typical Characteristics (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



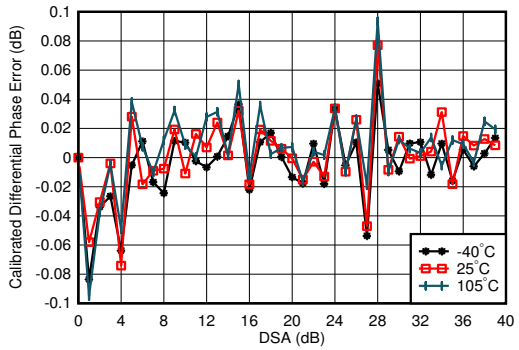
f_{DAC} = 11796.48MSPS, interleaved mode, matching at 4.9 GHz
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

Figure 309. TX Calibrated Integrated Phase Error vs DSA Setting and Channel at 4.9 GHz



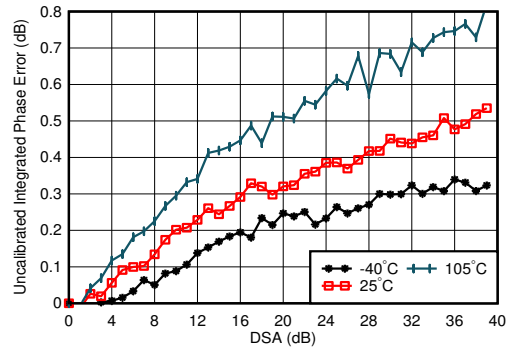
f_{DAC} = 11796.48MSPS, interleaved mode, matching at 4.9 GHz
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

Figure 310. TX Uncalibrated Differential Phase Error vs DSA Setting and Temperature at 4.9 GHz



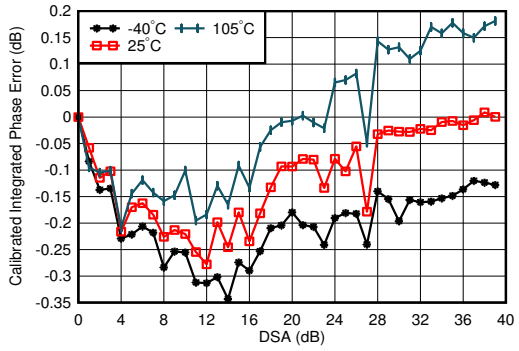
f_{DAC} = 11796.48MSPS, interleaved mode, matching at 4.9 GHz
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

Figure 311. TX Calibrated Differential Phase Error vs DSA Setting and Temperature at 4.9 GHz



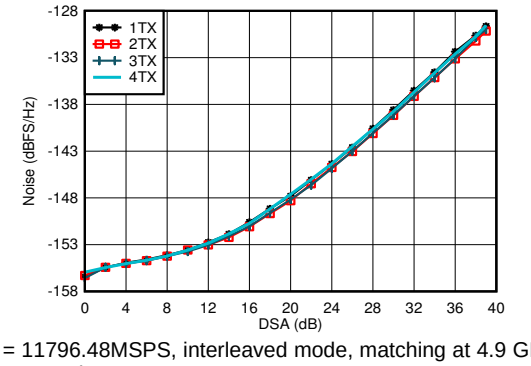
f_{DAC} = 11796.48MSPS, interleaved mode, matching at 4.9 GHz
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

Figure 312. TX Uncalibrated Integrated Phase Error vs DSA Setting and Temperature at 4.9 GHz



f_{DAC} = 11796.48MSPS, interleaved mode, matching at 4.9 GHz, channel with the median variation over DSA setting at 25°C
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

Figure 313. TX Calibrated Integrated Phase Error vs DSA Setting and Temperature at 4.9 GHz

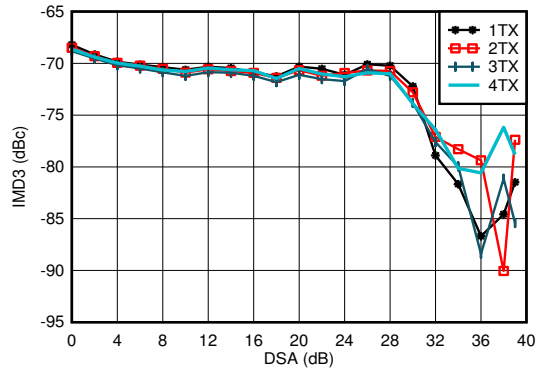


f_{DAC} = 11796.48MSPS, interleaved mode, matching at 4.9 GHz, P_{OUT} = –13 dBFS

Figure 314. TX Output Noise vs Channel and Attenuation at 2.6 GHz

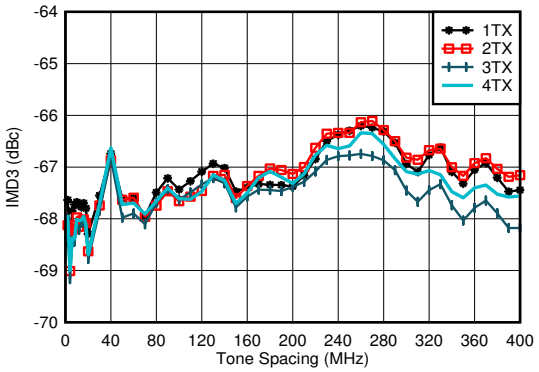
TX Typical Characteristics (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



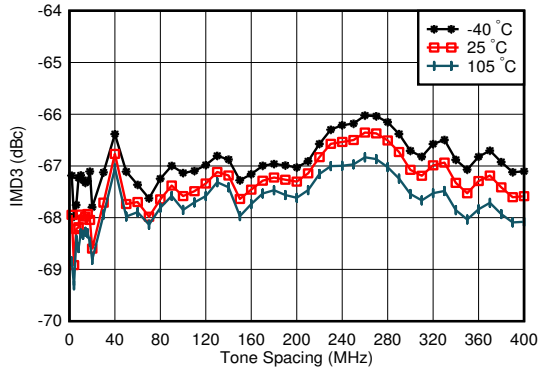
f_{DAC} = 11796.48MSPS, interleaved mode, matching at 4.9 GHz, f_{CENTER} = 4.9GHz, -13 dBFS each tone

Figure 315. TX IMD3 vs DSA Setting at 4.9 GHz



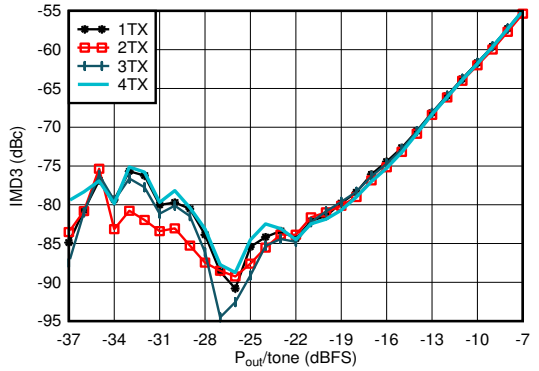
f_{DAC} = 11796.48MSPS, interleaved mode, matching at 4.9 GHz, f_{CENTER} = 4.9GHz, –13 dBFS each tone

Figure 316. TX IMD3 vs Tone Spacing and Channel at 4.9 GHz



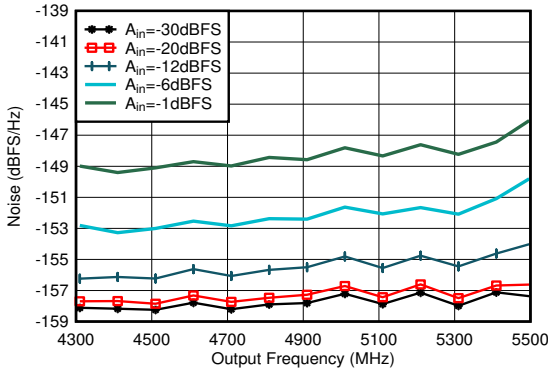
f_{DAC} = 11796.48MSPS, interleaved mode, matching at 4.9 GHz, f_{CENTER} = 4.9GHz, –13 dBFS each tone, worst channel

Figure 317. TX IMD3 vs Tone Spacing and Temperature at 4.9 GHz



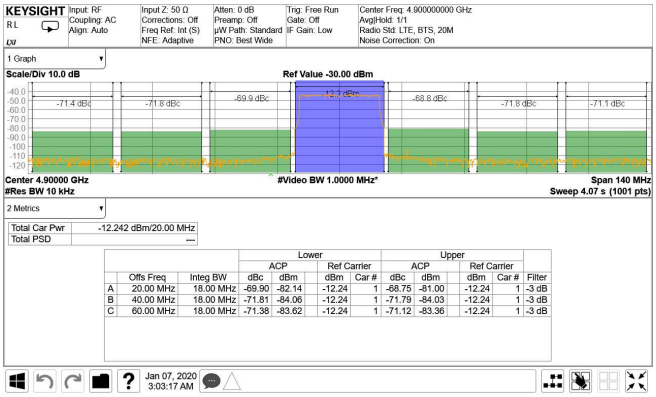
f_{DAC} = 11796.48MSPS, interleaved mode, matching at 4.9 GHz, f_{CENTER} = 4.9GHz, $f_{SPACING}$ = 20 MHz

Figure 318. TX IMD3 vs Digital Level at 4.9 GHz



Matching at 4.9 GHz, Single tone, f_{DAC} = 11.79648GSPS, interleave mode, 40-MHz offset, DSA=0dB

Figure 319. TX Single Tone Output Noise vs Frequency and Amplitude at 4.9 GHz

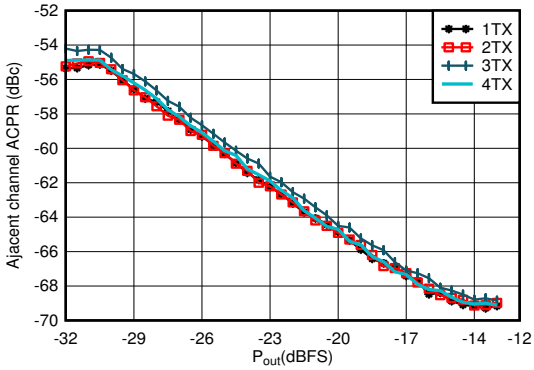


TM1.1, P_{OUT_RMS} = –13 dBFS

Figure 320. TX 20-MHz LTE Output Spectrum at 4.9 GHz

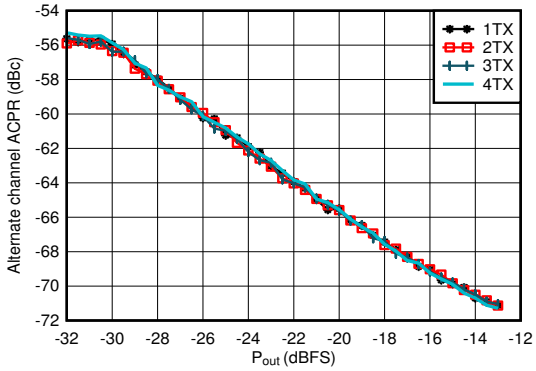
TX Typical Characteristics (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



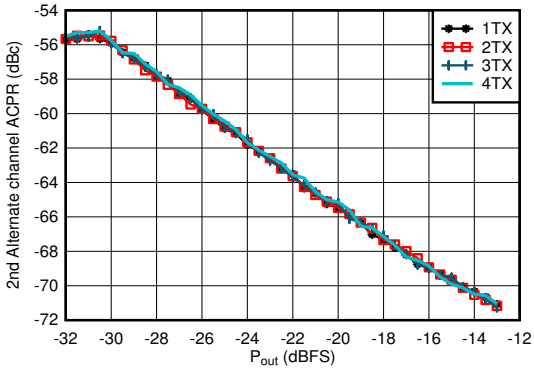
Matching at 4.9 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 321. TX 20-MHz LTE ACPR vs Digital Level at 4.9 GHz



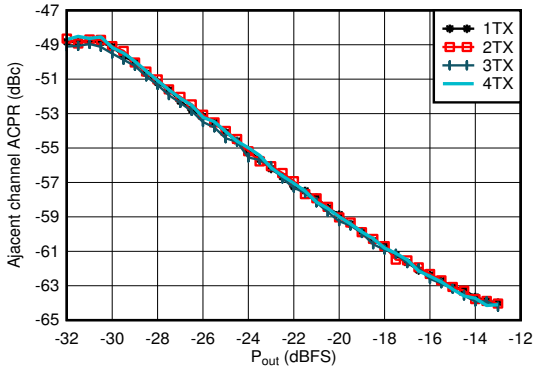
Matching at 4.9 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 322. TX 20-MHz LTE alt-ACPR vs Digital Level at 4.9 GHz



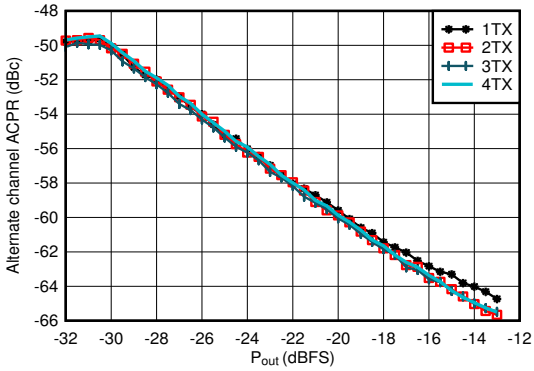
Matching at 4.9 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 323. TX 20-MHz LTE alt2-ACPR vs Digital Level at 4.9 GHz



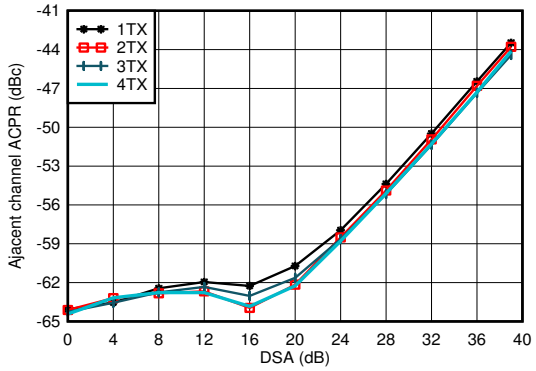
Matching at 4.9 GHz, single carrier 100-MHz BW TM1.1 NR

Figure 324. TX 100-MHz NR ACPR vs Digital Level at 4.9 GHz



Matching at 4.9 GHz, single carrier 100-MHz BW TM1.1 NR

Figure 325. TX 100-MHz NR alt-ACPR vs Digital Level at 4.9 GHz

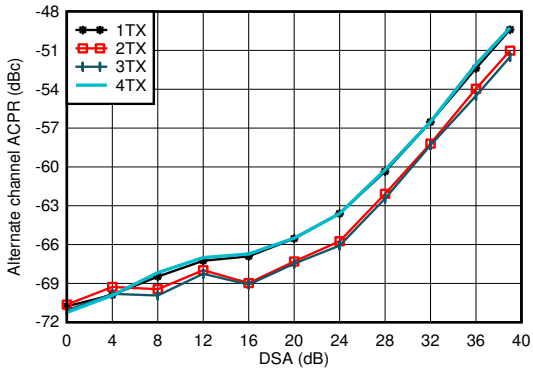


Matching at 4.9 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 326. TX 20-MHz LTE ACPR vs DSA at 4.9 GHz

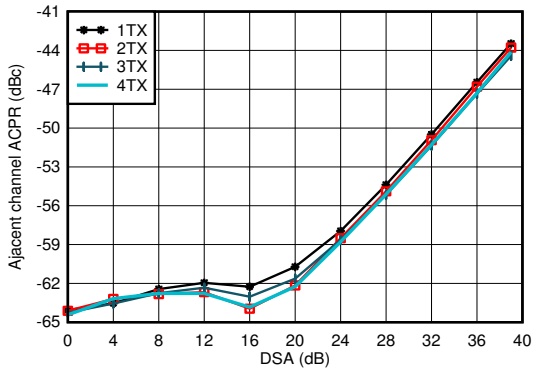
TX Typical Characteristics (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



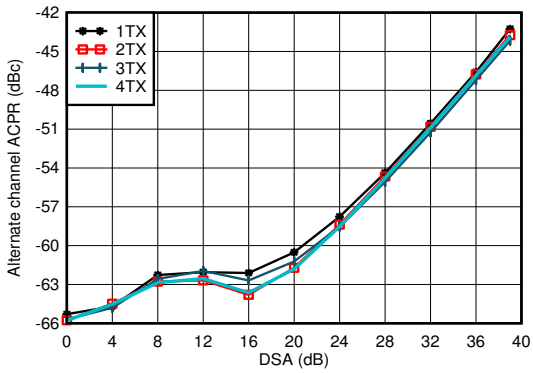
Matching at 4.9 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 327. TX 20-MHz LTE alt-ACPR vs DSA at 4.9 GHz



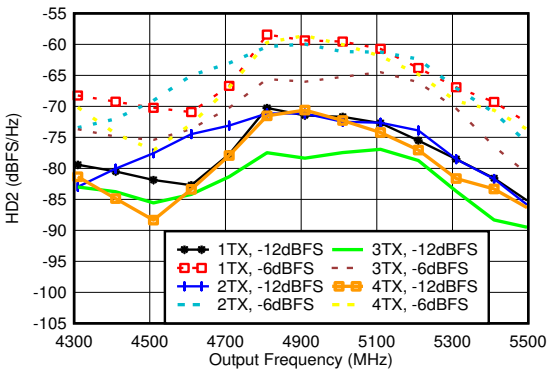
Matching at 4.9 GHz, single carrier 100-MHz BW TM1.1 NR

Figure 328. TX 100-MHz NR ACPR vs DSA at 4.9 GHz



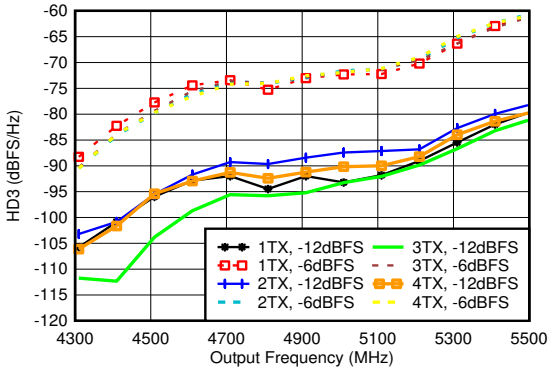
Matching at 4.9 GHz, single carrier 100-MHz BW TM1.1 NR

Figure 329. TX 100-MHz NR alt-ACPR vs DSA at 4.9 GHz



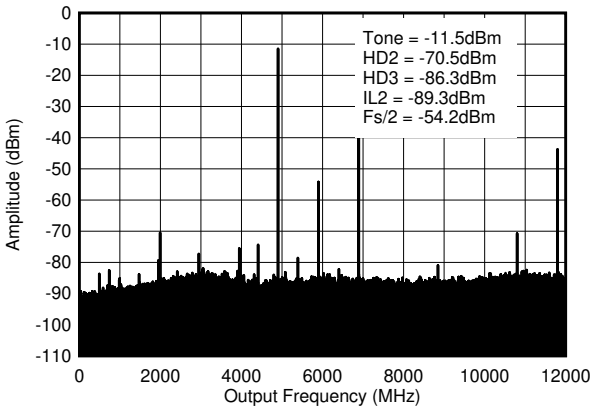
Matching at 4.9 GHz, f_{DAC} = 11.79648GSPS, interleave mode, normalized to output power at harmonic frequency

Figure 330. TX HD2 vs Digital Amplitude and Output Frequency at 4.9 GHz



Matching at 4.9 GHz, f_{DAC} = 11.79648GSPS, interleave mode, normalized to output power at harmonic frequency

Figure 331. TX HD3 vs Digital Amplitude and Output Frequency at 4.9 GHz

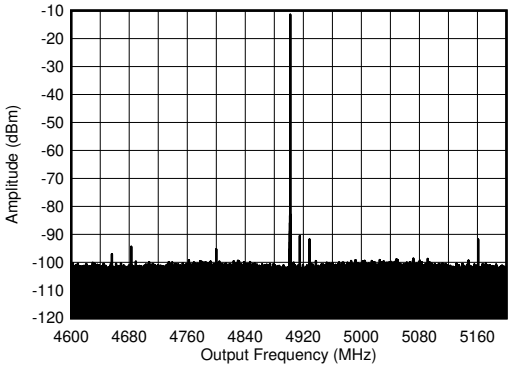


f_{DAC} = 11796.48MSPS, interleave mode, 4.9 GHz matching, includes PCB and cable losses. ILn = $f_S/n \pm f_{OUT}$.

Figure 332. TX Single Tone (–12 dBFS) Output Spectrum at 4.9 GHz (0-f_{DAC})

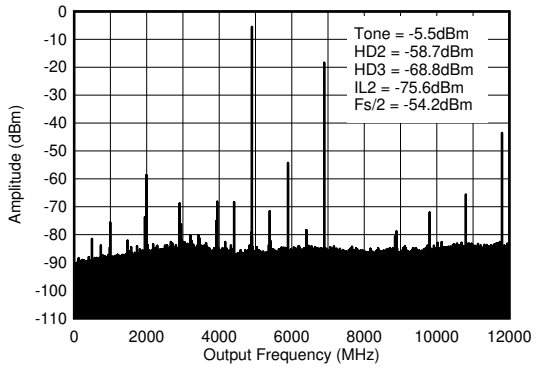
TX Typical Characteristics (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



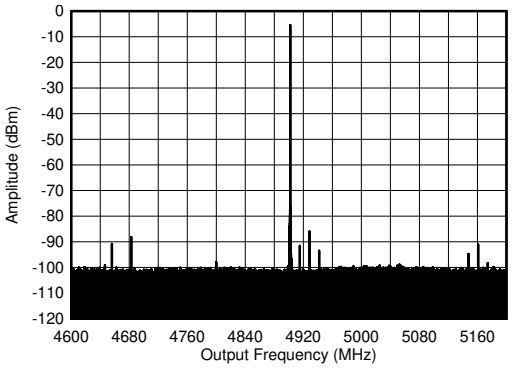
f_{DAC} = 11796.48MSPS, interleave mode, 4.9 GHz matching, includes PCB and cable losses

Figure 333. TX Single Tone (–12 dBFS) Output Spectrum at 4.9 GHz (±300 MHz)



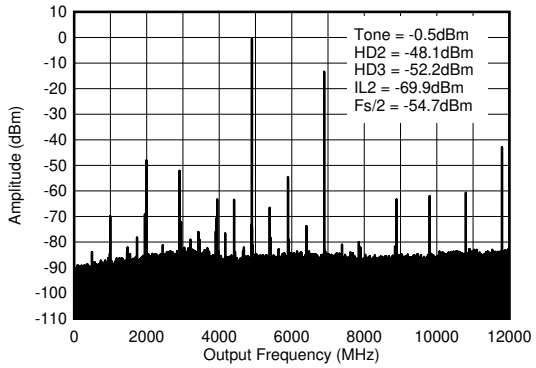
f_{DAC} = 11796.48MSPS, interleave mode, 4.9 GHz matching, includes PCB and cable losses. ILn = $f_S/n \pm f_{OUT}$.

Figure 334. TX Single Tone (–6 dBFS) Output Spectrum at 4.9 GHz (0-f_{DAC})



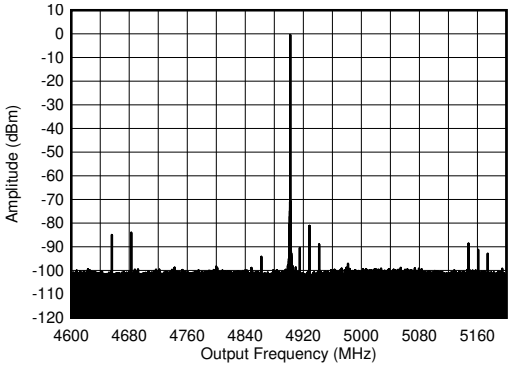
f_{DAC} = 11796.48MSPS, interleave mode, 4.9 GHz matching, includes PCB and cable losses

Figure 335. TX Single Tone (–6 dBFS) Output Spectrum at 4.9 GHz (±300 MHz)



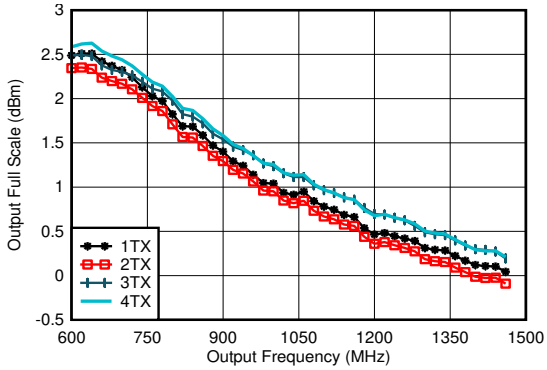
f_{DAC} = 11796.48MSPS, interleave mode, 4.9 GHz matching, includes PCB and cable losses. ILn = $f_S/n \pm f_{OUT}$.

Figure 336. TX Single Tone (–1 dBFS) Output Spectrum at 4.9 GHz (0-f_{DAC})



f_{DAC} = 11796.48MSPS, interleave mode, 4.9 GHz matching, includes PCB and cable losses

Figure 337. TX Single Tone (–1 dBFS) Output Spectrum at 4.9 GHz (±300 MHz)

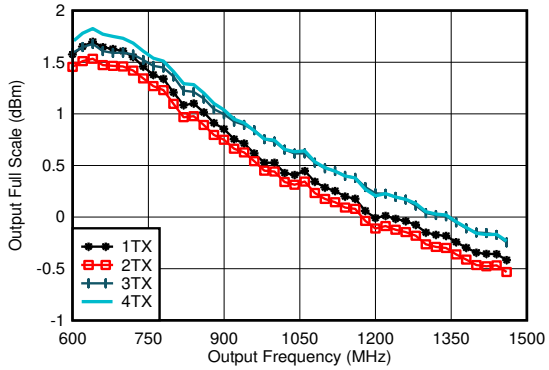


Including PCB and cable losses, A_{out} = -0.5dFBS, DSA = 0, 0.8 GHz matching

Figure 338. TX Full Scale vs RF Frequency and Channel at 5898.24MSPS, Straight Mode

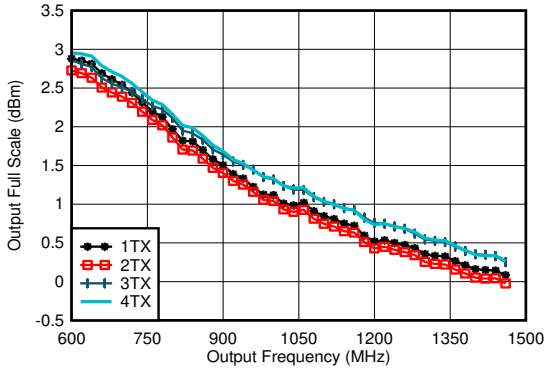
TX Typical Characteristics (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



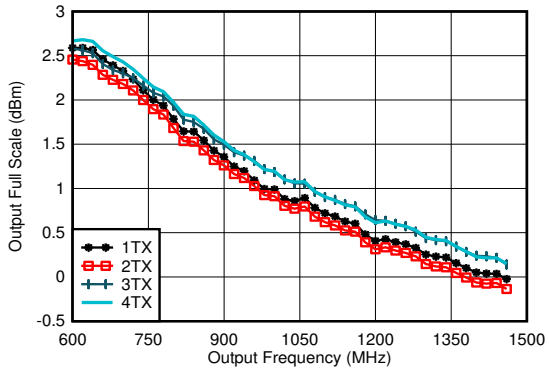
Including PCB and cable losses, A_{out} = -0.5dFBS, DSA = 0, 2.6 GHz matching

Figure 339. TX Full Scale vs RF Frequency and Channel at 8847.36MSPS, Straight Mode



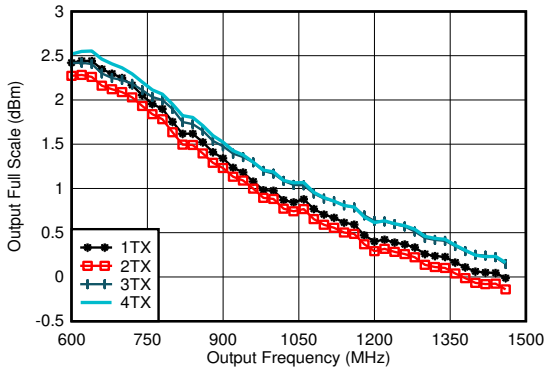
Including PCB and cable losses, A_{out} = -0.5dFBS, DSA = 0, 0.8 GHz matching

Figure 340. TX Full Scale vs RF Frequency and Channel at 5898.24MSPS, Interleave Mode



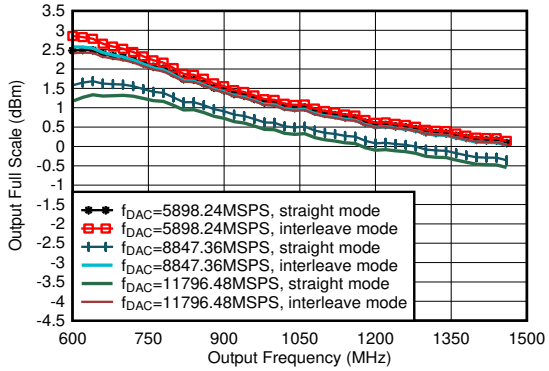
Including PCB and cable losses, A_{out} = -0.5dFBS, DSA = 0, 0.8 GHz matching

Figure 341. TX Full Scale vs RF Frequency and Channel at 8847.36MSPS, Interleave Mode



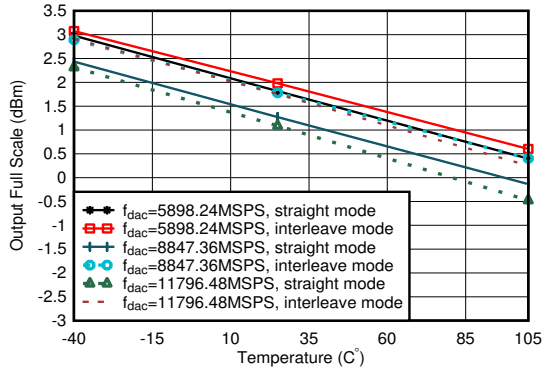
Including PCB and cable losses, A_{out} = -0.5dFBS, DSA = 0, 0.8 GHz matching

Figure 342. TX Full Scale vs RF Frequency and Channel at 11796.48MSPS, Interleave Mode



including PCB and cable losses, A_{out} = -0.5dFBS, DSA = 0, 0.8 GHz matching

Figure 343. TX Output Fullscale vs Output Frequency

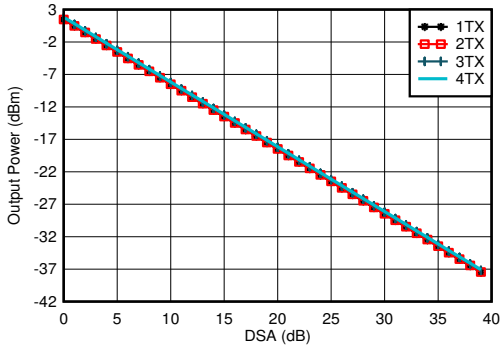


including PCB and cable losses, A_{out} = -0.5dFBS, DSA = 0, 0.8 GHz matching

Figure 344. TX Output Fullscale vs Temperature

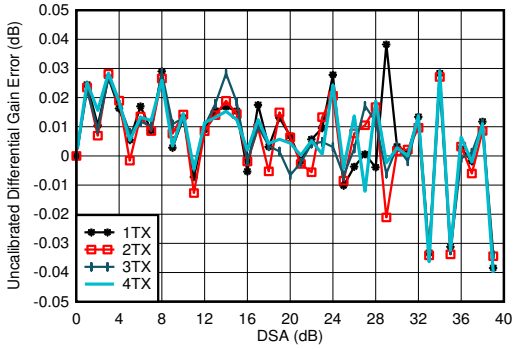
TX Typical Characteristics (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



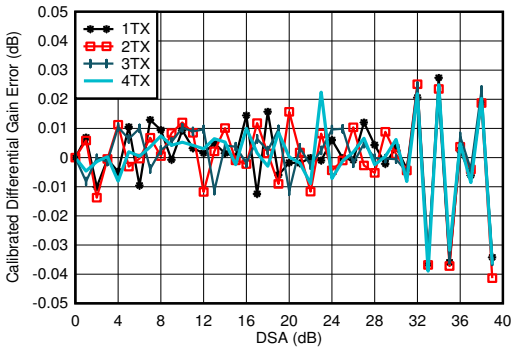
f_{DAC} = 11796.48 MSPS, interleave mode, A_{out} = -0.5dFBS, matching 0.8 GHz

Figure 345. TX Output Power vs DSA Setting and Channel at 0.85 GHz



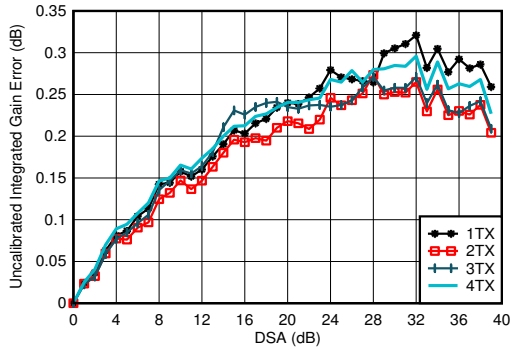
f_{DAC}=5898.24MSPS, interleave mode, matching at 0.8 GHz
Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

Figure 346. TX Uncalibrated Differential Gain Error vs DSA Setting and Channel at 0.85 GHz



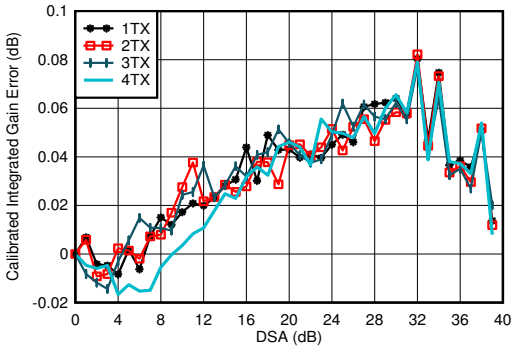
f_{DAC}=5898.24MSPS, interleave mode, matching at 0.8 GHz
Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

Figure 347. TX Calibrated Differential Gain Error vs DSA Setting and Channel at 0.85 GHz



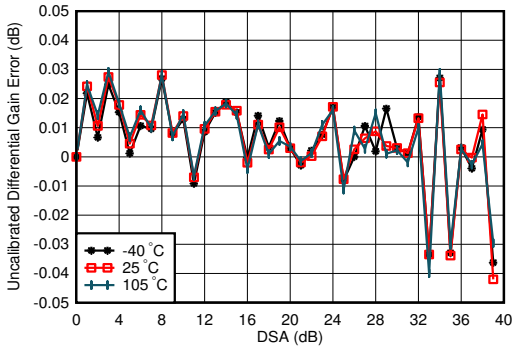
f_{DAC}=5898.24MSPS, interleave mode, matching at 0.8 GHz
Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + DSA Settings

Figure 348. TX Uncalibrated Integrated Gain Error vs DSA Setting and Channel at 0.85 GHz



f_{DAC}=5898.24MSPS, interleave mode, matching at 0.8 GHz
Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + DSA Setting

Figure 349. TX Calibrated Integrated Gain Error vs DSA Setting and Channel at 0.85 GHz

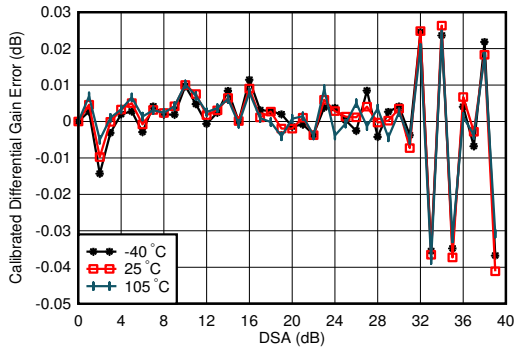


f_{DAC} = 5898.24MSPS, interleave mode, matching at 0.8 GHz
Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

Figure 350. TX Uncalibrated Differential Gain Error vs DSA Setting and Temperature at 0.85 GHz

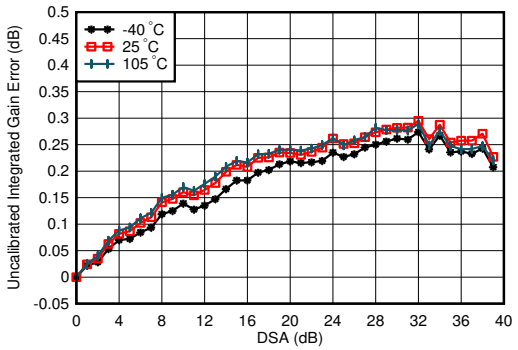
TX Typical Characteristics (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



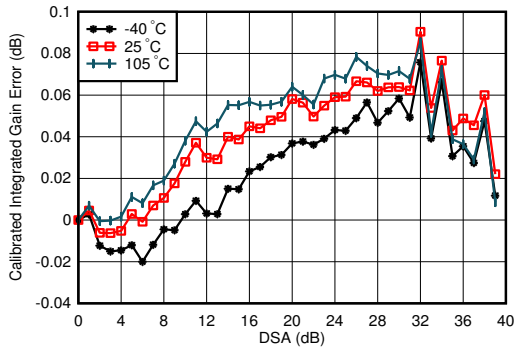
f_{DAC} = 5898.24MSPS, interleave mode, matching at 0.8 GHz
Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

Figure 351. TX Calibrated Differential Gain Error vs DSA Setting and Temperature at 0.85 GHz



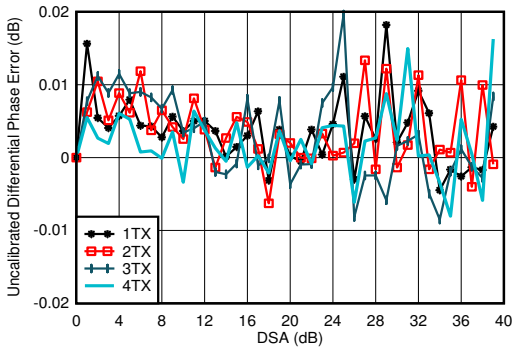
f_{DAC} = 5898.24MSPS, interleave mode, matching at 0.8 GHz
Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + DSA Setting

Figure 352. TX Uncalibrated Integrated Gain Error vs DSA Setting and Temperature at 0.85 GHz



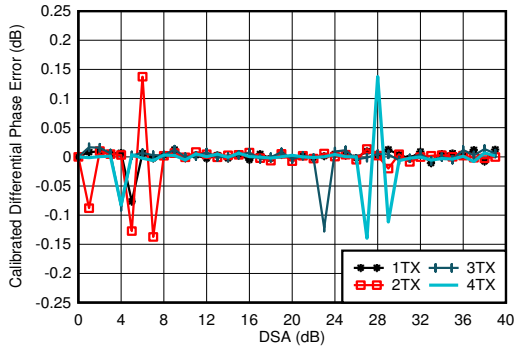
f_{DAC} = 5898.24MSPS, interleave mode, matching at 0.8 GHz
Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + DSA Setting

Figure 353. TX Calibrated Integrated Gain Error vs DSA Setting and Temperature at 0.85 GHz



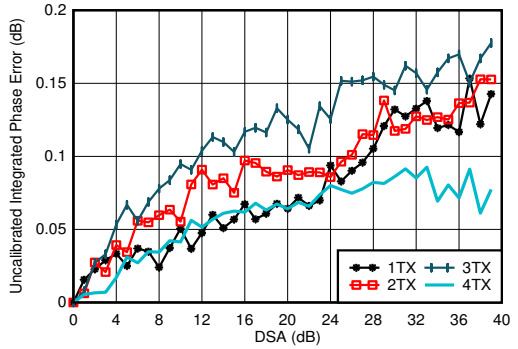
f_{DAC} = 5898.24MSPS, interleave mode, matching at 0.8 GHz
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

Figure 354. TX Uncalibrated Differential Phase Error vs DSA Setting and Channel at 0.85 GHz



f_{DAC} = 5898.24MSPS, interleave mode, matching at 0.8 GHz
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)
Phase DNL spike may occur at any DSA setting.

Figure 355. TX Calibrated Differential Phase Error vs DSA Setting and Channel at 0.85 GHz

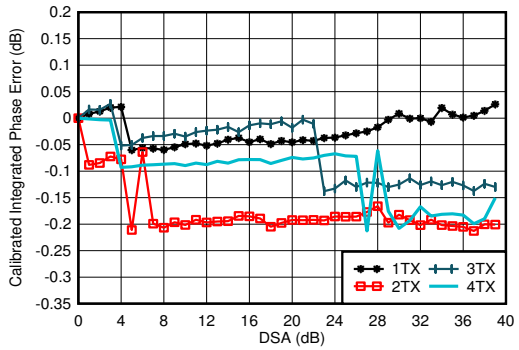


f_{DAC} = 5898.24MSPS, interleave mode, matching at 0.8 GHz
Integrated Phase Error = $Phase_{OUT}$(DSA Setting) – $Phase_{OUT}$(DSA Setting = 0)

Figure 356. TX Uncalibrated Integrated Phase Error vs DSA Setting and Channel at 0.85 GHz

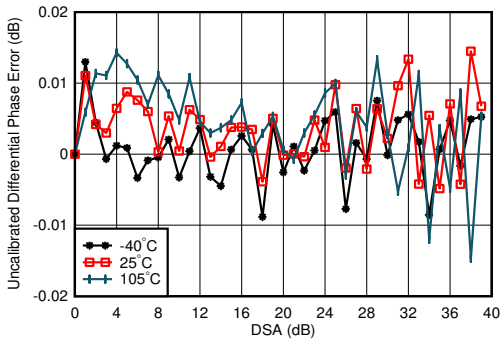
TX Typical Characteristics (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



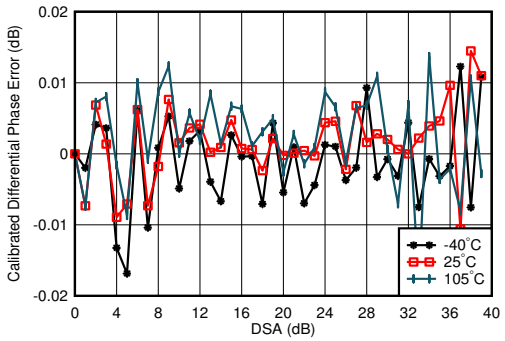
f_{DAC} = 5898.24MSPS, interleave mode, matching at 0.8 GHz
Integrated Phase Error = $Phase_{OUT}$(DSA Setting) – $Phase_{OUT}$(DSA Setting = 0)

Figure 357. TX Calibrated Integrated Phase Error vs DSA Setting and Channel at 0.85 GHz



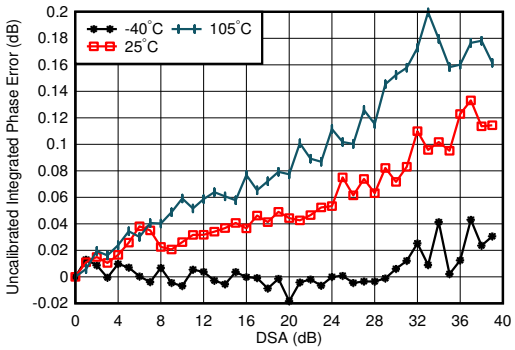
f_{DAC} = 5898.24MSPS, interleave mode, matching at 0.8 GHz
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting) + 1

Figure 358. TX Uncalibrated Differential Phase Error vs DSA Setting and Temperature at 0.85 GHz



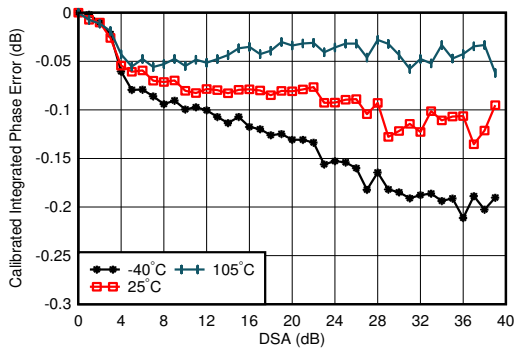
f_{DAC} = 5898.24MSPS, interleave mode, matching at 0.8 GHz, channel with the median variation over DSA setting at 25°C
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting) + 1

Figure 359. TX Calibrated Differential Phase Error vs DSA Setting and Temperature at 0.85 GHz



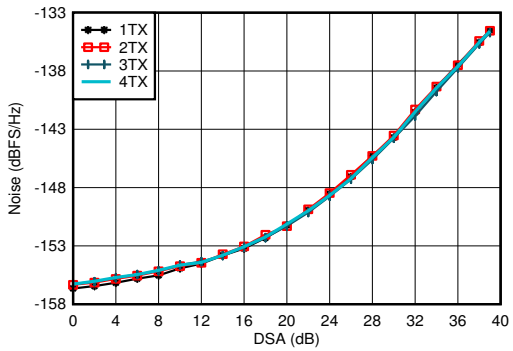
f_{DAC} = 5898.24MSPS, interleave mode, matching at 0.8 GHz
Integrated Phase Error = $Phase_{OUT}$(DSA Setting) – $Phase_{OUT}$(DSA Setting = 0)

Figure 360. TX Uncalibrated Integrated Phase Error vs DSA Setting and Temperature at 0.85 GHz



f_{DAC} = 5898.24MSPS, interleave mode, matching at 0.8 GHz
Integrated Phase Error = $Phase_{OUT}$(DSA Setting) – $Phase_{OUT}$(DSA Setting = 0)

Figure 361. TX Calibrated Integrated Phase Error vs DSA Setting and Temperature at 0.85 GHz

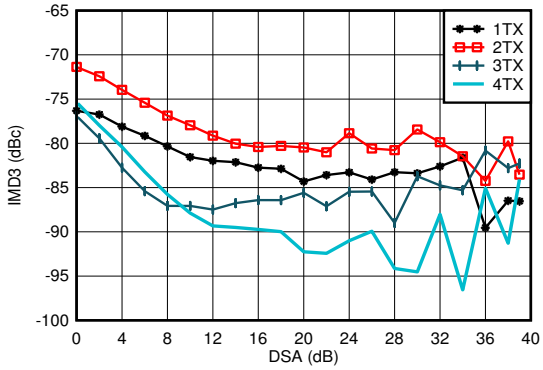


f_{DAC} = 5898.24MSPS, interleave mode, matching at 0.8 GHz, P_{OUT} = –13 dBFS

Figure 362. TX Output Noise vs Channel and Attenuation at 0.85 GHz

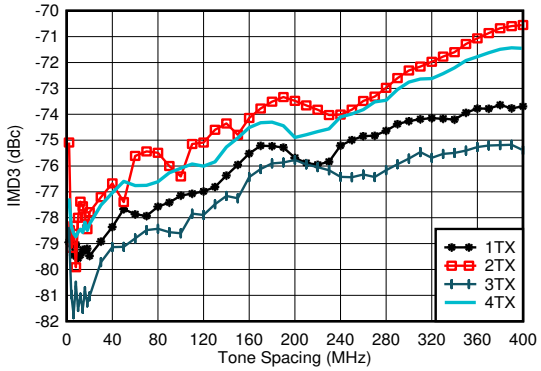
TX Typical Characteristics (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



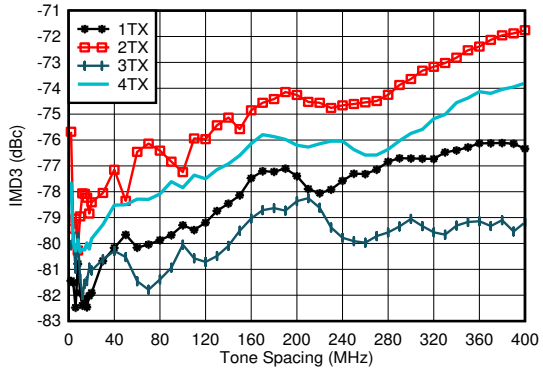
f_{DAC} = 11796.48MSPS, interleave mode, f_{CENTER} = 0.85 GHz, matching at 0.8 GHz, –13 dBFS each tone

Figure 363. TX IMD3 vs DSA Setting at 0.85 GHz



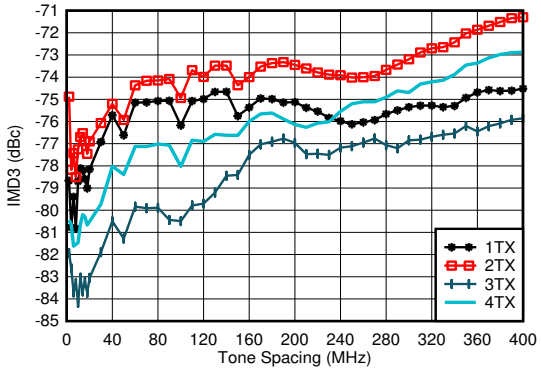
f_{DAC} = 5898.24MSPS, straight mode, f_{CENTER} = 0.85 GHz, matching at 0.8 GHz, –13 dBFS each tone

Figure 364. TX IMD3 vs Tone Spacing and Channel at 0.85 GHz



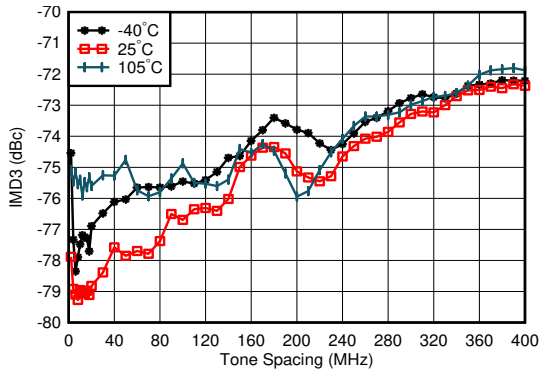
f_{DAC} = 8847.36MSPS, straight mode, f_{CENTER} = 0.85 GHz, matching at 0.8 GHz, –13 dBFS each tone

Figure 365. TX IMD3 vs Tone Spacing and Channel at 0.85 GHz



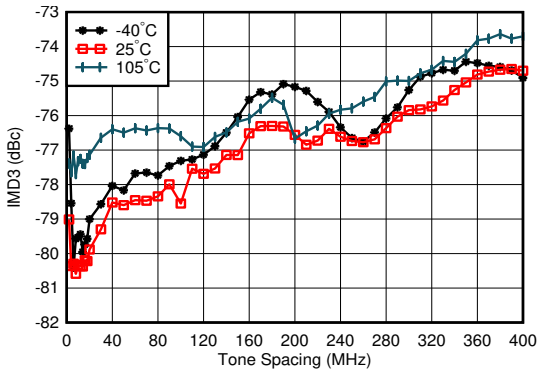
f_{DAC} = 11796.48MSPS, interleave mode, f_{CENTER} = 0.85 GHz, matching at 0.8 GHz, –13 dBFS each tone

Figure 366. TX IMD3 vs Tone Spacing and Channel at 0.85 GHz



f_{DAC} = 5898.24MSPS, straight mode, f_{CENTER} =0.85 GHz, matching at 0.8 GHz, –13 dBFS each tone, worst channel

Figure 367. TX IMD3 vs Tone Spacing and Temperature at 0.85 GHz

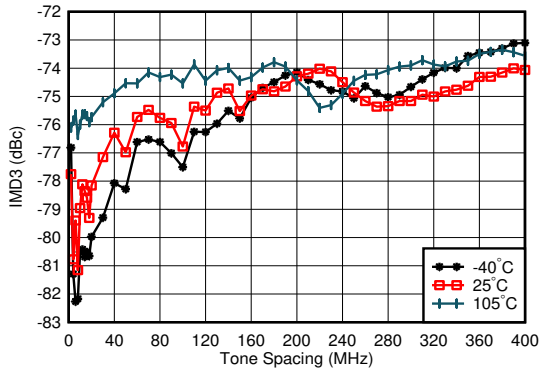


f_{DAC} = 8847.36MSPS, straight mode, f_{CENTER} =0.85 GHz, matching at 0.8 GHz, –13 dBFS each tone, worst channel

Figure 368. TX IMD3 vs Tone Spacing and Temperature at 0.85 GHz

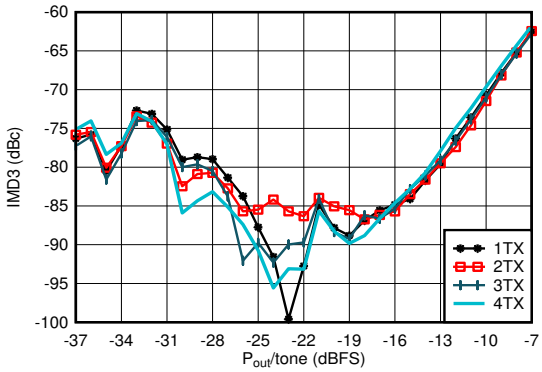
TX Typical Characteristics (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



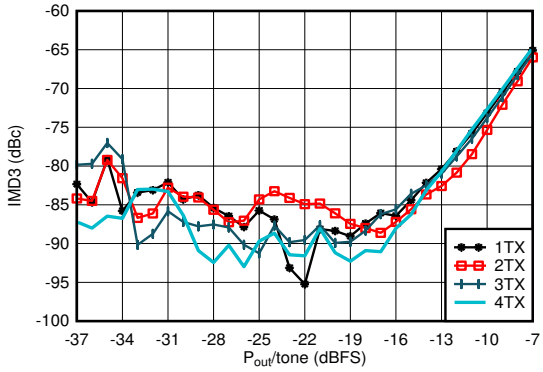
f_{DAC} = 11796.48MSPS, straight mode, f_{CENTER} =0.85 GHz, matching at 0.8 GHz, –13 dBFS each tone, worst channel

Figure 369. TX IMD3 vs Tone Spacing and Temperature at 0.85 GHz



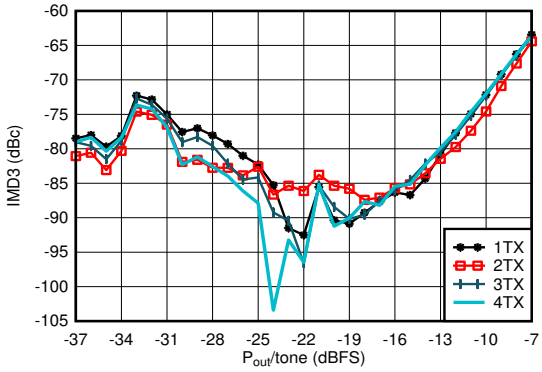
f_{DAC} = 5898.24MSPS, straight mode, f_{CENTER} = 0.85 GHz, $f_{SPACING}$ = 20 MHz, matching at 0.8 GHz

Figure 370. TX IMD3 vs Digital Level at 0.85 GHz



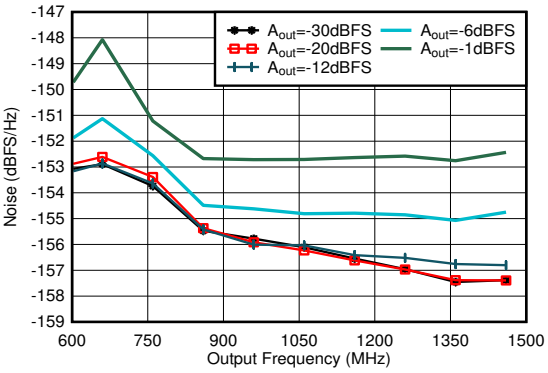
f_{DAC} = 8847.36MSPS, straight mode, f_{CENTER} = 0.85 GHz, $f_{SPACING}$ = 20 MHz, matching at 0.8 GHz

Figure 371. TX IMD3 vs Digital Level at 0.85 GHz



f_{DAC} = 11796.48MSPS, interleave mode, f_{CENTER} = 0.85 GHz, $f_{SPACING}$ = 20 MHz, matching at 0.8 GHz

Figure 372. TX IMD3 vs Digital Level at 0.85 GHz



Matching at 2.6 GHz, Single tone, f_{DAC} = 11.79648GSPS, interleave mode, 40-MHz offset, DSA = 0dB

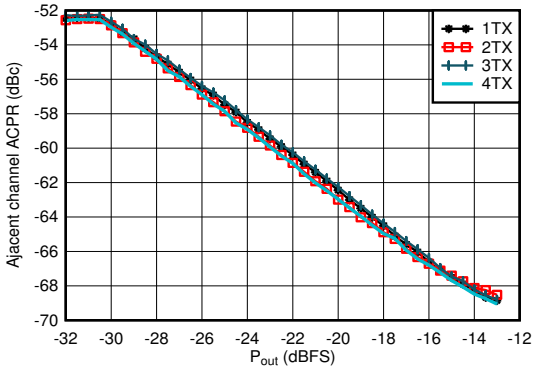
Figure 373. TX Single Tone Output Noise vs Frequency and Amplitude at 0.85 GHz

TM1.1, P_{OUT_RMS} = –13 dBFS

Figure 374. TX 20-MHz LTE Output Spectrum at 0.85 GHz

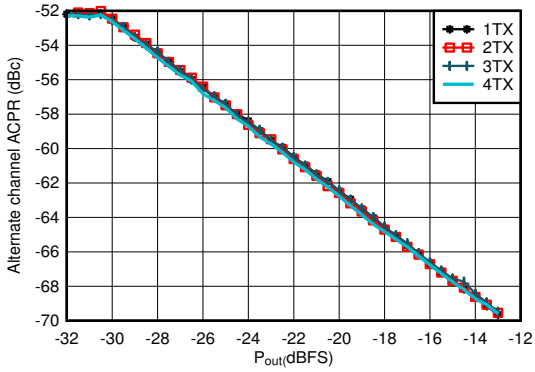
TX Typical Characteristics (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



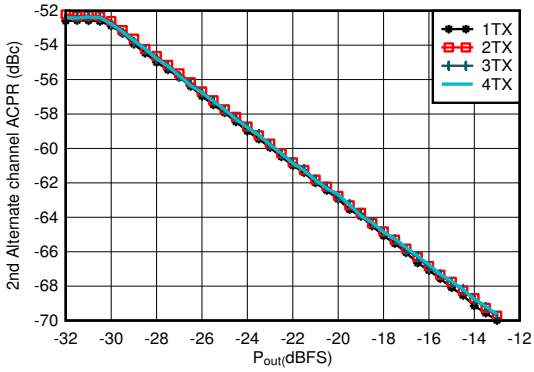
Matching at 0.8 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 375. TX 20-MHz LTE ACPR vs Digital Level at 0.85 GHz



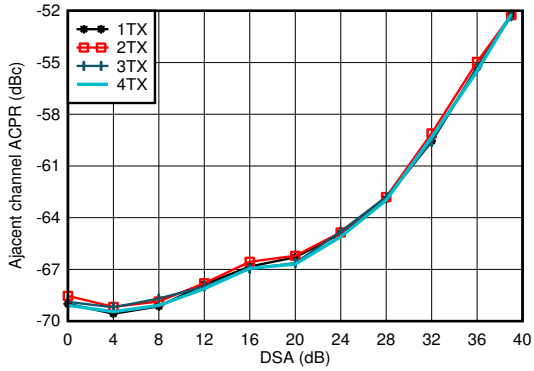
Matching at 0.8 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 376. TX 20-MHz LTE alt-ACPR vs Digital Level at 0.85 GHz



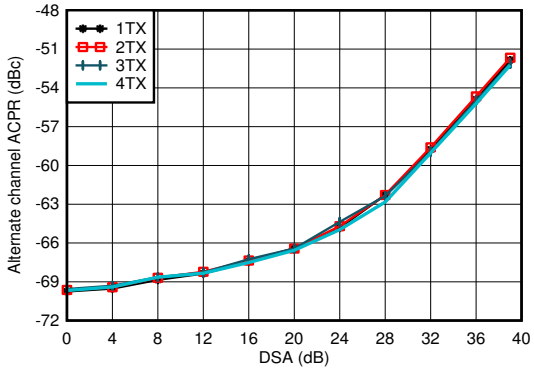
Matching at 0.8 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 377. TX 20-MHz LTE alt2-ACPR vs Digital Level at 0.85 GHz



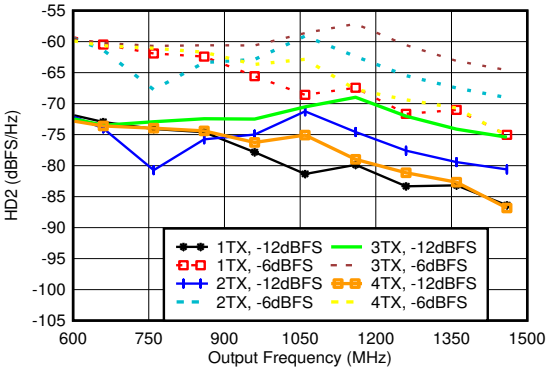
Matching at 0.8 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 378. TX 20-MHz LTE ACPR vs DSA at 0.85 GHz



Matching at 0.8 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 379. TX 20-MHz LTE alt-ACPR vs DSA at 0.85 GHz

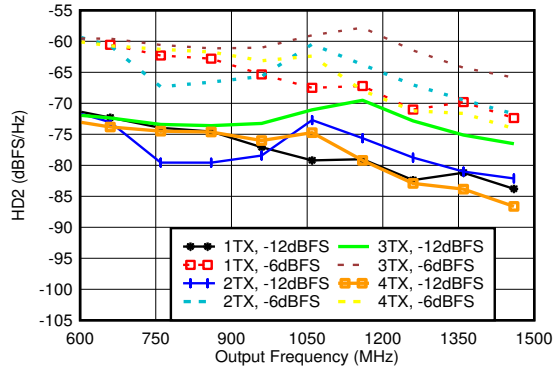


Matching at 0.8 GHz, f_{DAC} = 5898.24GSPS, straight mode

Figure 380. TX HD2 vs Digital Amplitude and Output Frequency at 0.85 GHz

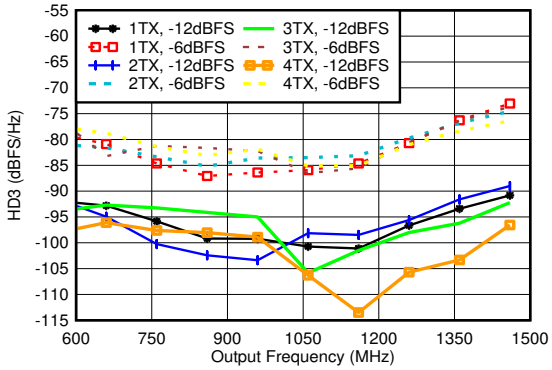
TX Typical Characteristics (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



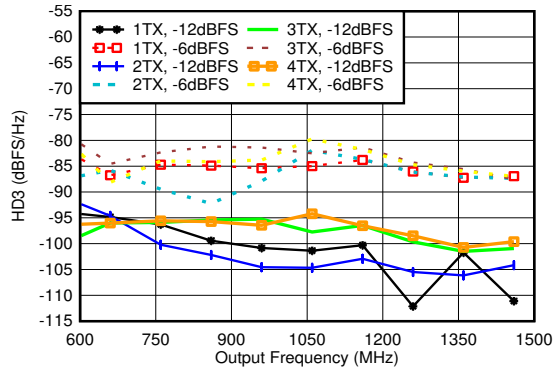
Matching at 0.8 GHz, f_{DAC} = 8847.36GSPS, straight mode

Figure 381. TX HD2 vs Digital Amplitude and Output Frequency at 0.85 GHz



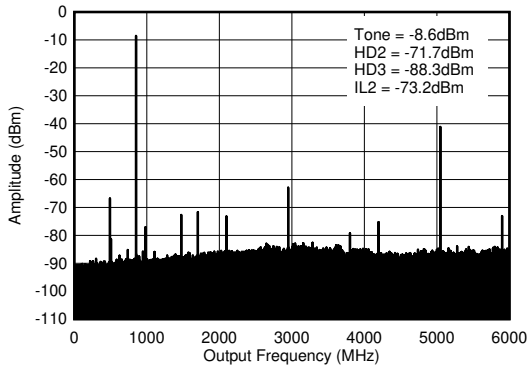
Matching at 0.8 GHz, f_{DAC} = 5898.24MSPS, straight mode, normalized to output power at harmonic frequency

Figure 382. TX HD3 vs Digital Amplitude and Output Frequency at 0.85 GHz



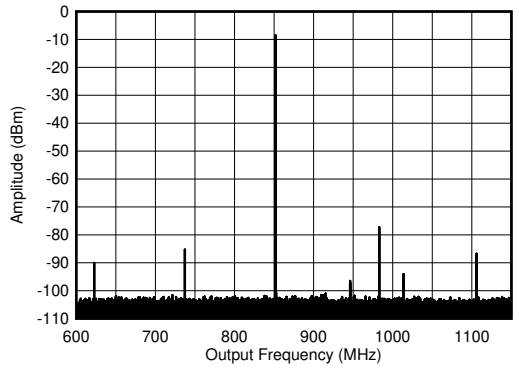
Matching at 0.8 GHz, f_{DAC} = 8847.36MSPS, straight mode, normalized to output power at harmonic frequency

Figure 383. TX HD3 vs Digital Amplitude and Output Frequency at 0.85 GHz



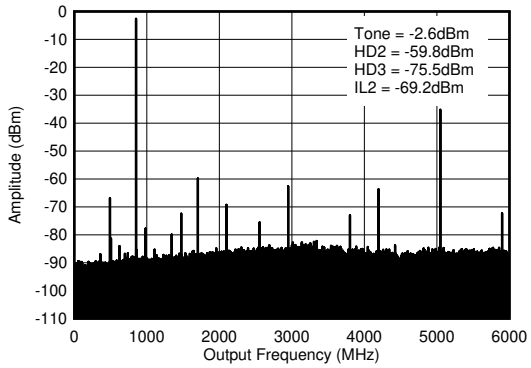
f_{DAC} = 5898.24MSPS, interleave mode, 0.8 GHz matching, includes PCB and cable losses. ILn = $f_S/n \pm f_{OUT}$.

Figure 384. TX Single Tone (–12 dBFS) Output Spectrum at 0.85 GHz (0-f_{DAC})



f_{DAC} = 5898.24MSPS, interleave mode, 0.8 GHz matching, includes PCB and cable losses

Figure 385. TX Single Tone (–12 dBFS) Output Spectrum at 0.85 GHz (±300 MHz)

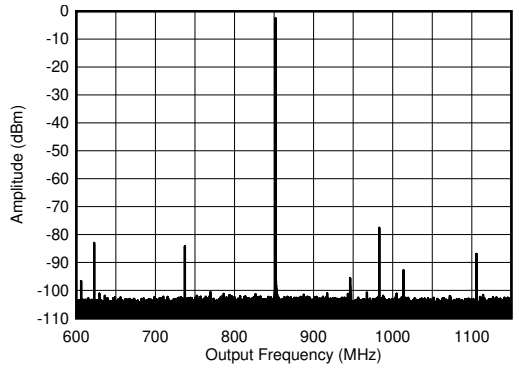


f_{DAC} = 5898.24MSPS, interleave mode, 0.8 GHz matching, includes PCB and cable losses. ILn = $f_S/n \pm f_{OUT}$.

Figure 386. TX Single Tone (–6 dBFS) Output Spectrum at 0.85 GHz (0-f_{DAC})

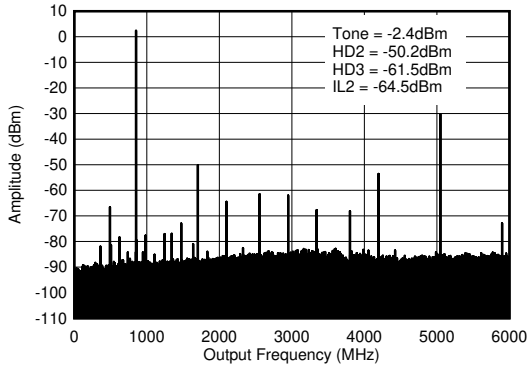
TX Typical Characteristics (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



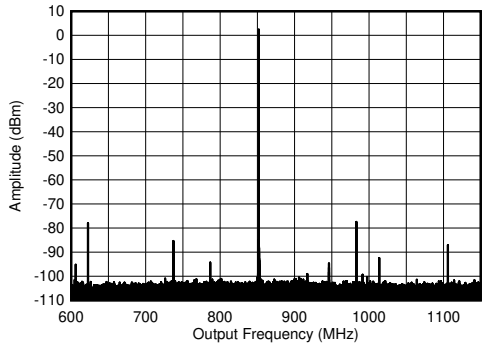
f_{DAC} = 5898.24MSPS, interleave mode, 0.8 GHz matching, includes PCB and cable losses

Figure 387. TX Single Tone (–6 dBFS) Output Spectrum at 0.85 GHz (±300 MHz)



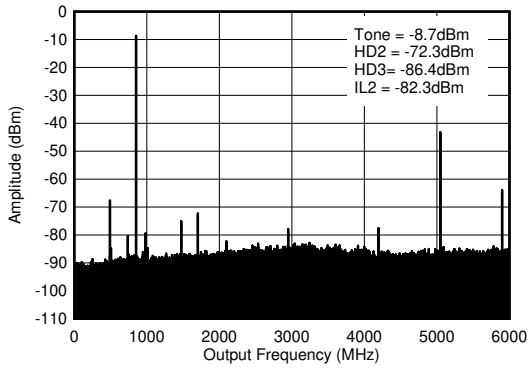
f_{DAC} = 5898.24MSPS, interleave mode, 0.8 GHz matching, includes PCB and cable losses. ILn = $f_S/n \pm f_{OUT}$.

Figure 388. TX Single Tone (–1 dBFS) Output Spectrum at 0.85 GHz (0-f_{DAC})



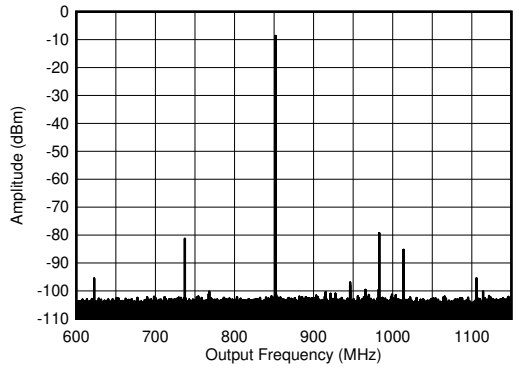
f_{DAC} = 5898.24MSPS, interleave mode, 0.8 GHz matching, includes PCB and cable losses

Figure 389. TX Single Tone (–1 dBFS) Output Spectrum at 0.85 GHz (±300 MHz)



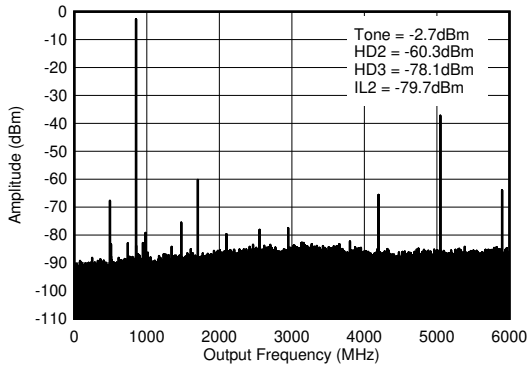
f_{DAC} = 5898.24MSPS, straight mode, 0.8 GHz matching, includes PCB and cable losses. ILn = $f_S/n \pm f_{OUT}$ and is due to mixing with digital clocks.

Figure 390. TX Single Tone (–12 dBFS) Output Spectrum at 0.85 GHz (0-f_{DAC})



f_{DAC} = 5898.24MSPS, straight mode, 0.8 GHz matching, includes PCB and cable losses

Figure 391. TX Single Tone (–12 dBFS) Output Spectrum at 0.85 GHz (±300 MHz)

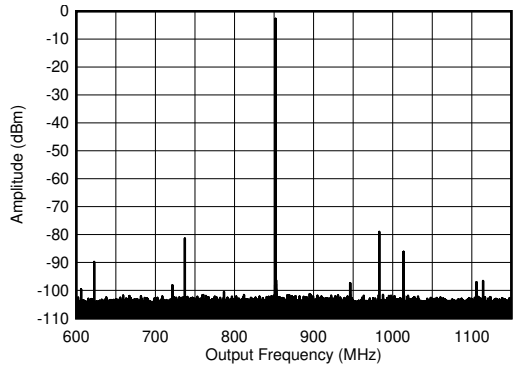


f_{DAC} = 5898.24MSPS, straight mode, 0.8 GHz matching, includes PCB and cable losses. ILn = $f_S/n \pm f_{OUT}$ and is due to mixing with digital clocks.

Figure 392. TX Single Tone (–6 dBFS) Output Spectrum at 0.85 GHz (0-f_{DAC})

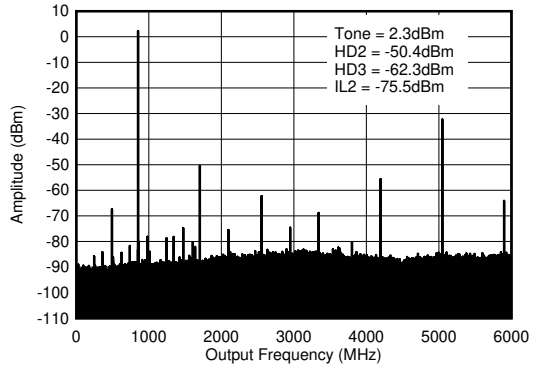
TX Typical Characteristics (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



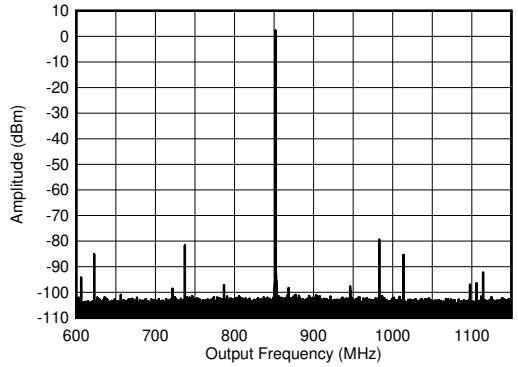
f_{DAC} = 5898.24MSPS, straight mode, 0.8 GHz matching, includes PCB and cable losses

Figure 393. TX Single Tone (–6 dBFS) Output Spectrum at 0.85 GHz (±300 MHz)



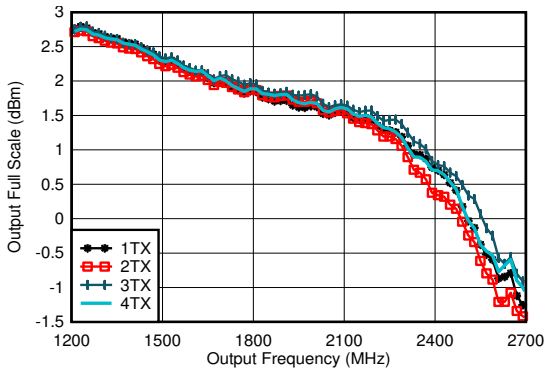
f_{DAC} = 5898.24MSPS, straight mode, 0.8 GHz matching, includes PCB and cable losses. ILn = $f_S/n \pm f_{OUT}$ and is due to mixing with digital clocks.

Figure 394. TX Single Tone (–1 dBFS) Output Spectrum at 0.85 GHz (0-f_{DAC})



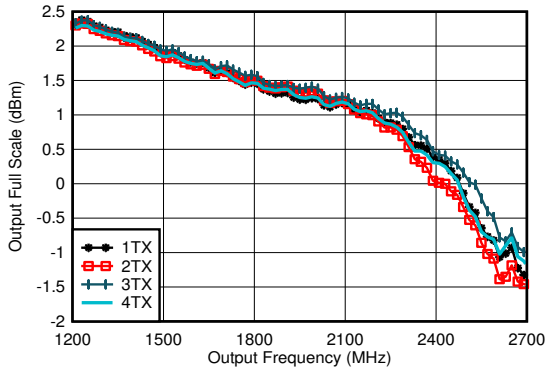
f_{DAC} = 5898.24MSPS, straight mode, 0.8 GHz matching, includes PCB and cable losses

Figure 395. TX Single Tone (–1 dBFS) Output Spectrum at 0.85 GHz (±300 MHz)



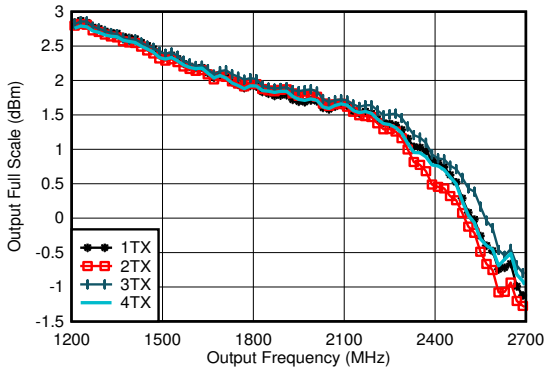
Including PCB and cable losses, A_{out} = -0.5dFBS, DSA = 0, 1.8 GHz matching

Figure 396. TX Full Scale vs RF Frequency and Channel at 5898.24MSPS, Straight Mode



Including PCB and cable losses, A_{out} = -0.5dFBS, DSA = 0, 1.8 GHz matching

Figure 397. TX Full Scale vs RF Frequency and Channel at 8847.36MSPS, Straight Mode

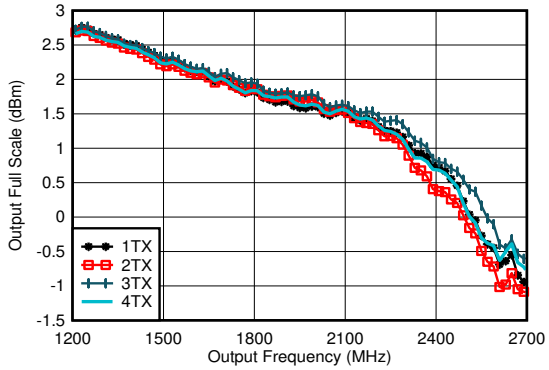


Including PCB and cable losses, A_{out} = -0.5dFBS, DSA = 0, 1.8 GHz matching

Figure 398. TX Full Scale vs RF Frequency and Channel at 5898.24MSPS, Interleave Mode

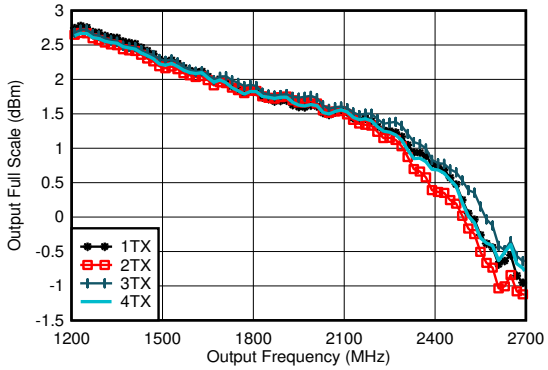
TX Typical Characteristics (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



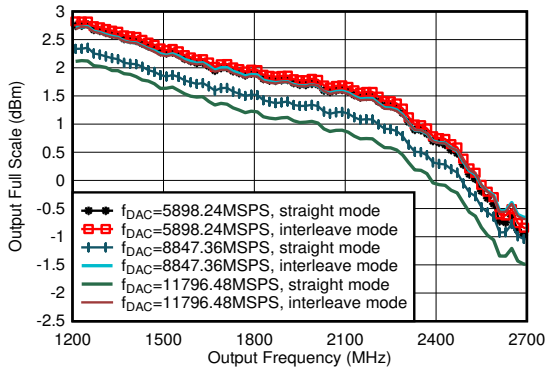
Including PCB and cable losses, A_{out} = -0.5dFBS, DSA = 0, 1.8 GHz matching

Figure 399. TX Full Scale vs RF Frequency and Channel at 8847.36MSPS, Interleave Mode



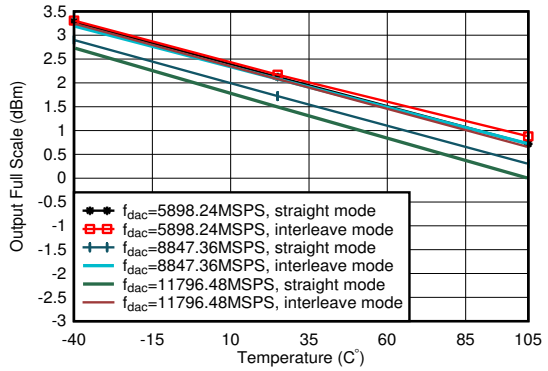
Iincluding PCB and cable losses, A_{out} = -0.5dFBS, DSA = 0, 1.8 GHz matching

Figure 400. TX Output Fullscale vs Output Frequency and Channel at 11796.48MSPS, Interleave Mode



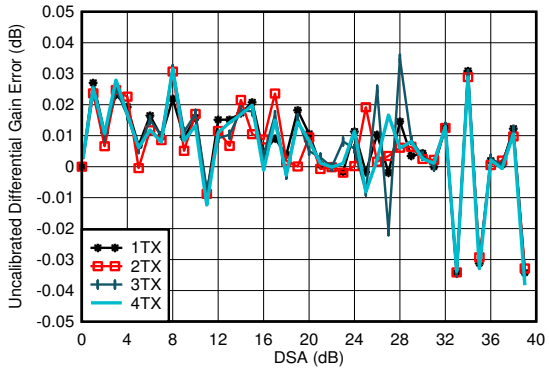
including PCB and cable losses, A_{out} = -0.5dFBS, DSA = 0, 1.8 GHz matching

Figure 401. TX Output Fullscale vs Output Frequency



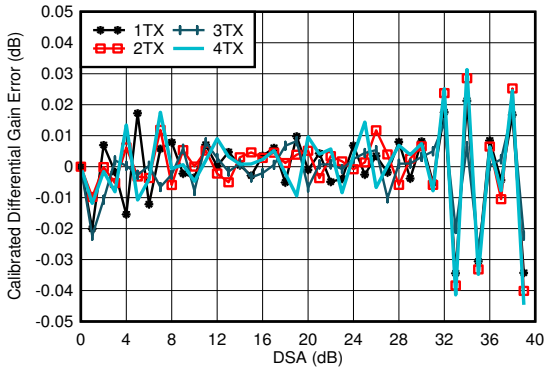
A_{out} = -0.5dFBS, matching 1.8 GHz

Figure 402. TX Output Power vs DSA Setting and Channel at 1.8 GHz



f_{DAC}=5898.24MSPS, interleave mode, matching at 1.8 GHz
Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

Figure 403. TX Uncalibrated Differential Gain Error vs DSA Setting and Channel at 1.8 GHz

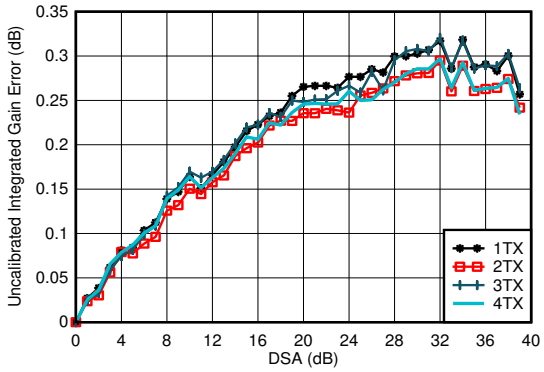


f_{DAC}=5898.24MSPS, interleave mode, matching at 1.8 GHz
Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

Figure 404. TX Calibrated Differential Gain Error vs DSA Setting and Channel at 1.8 GHz

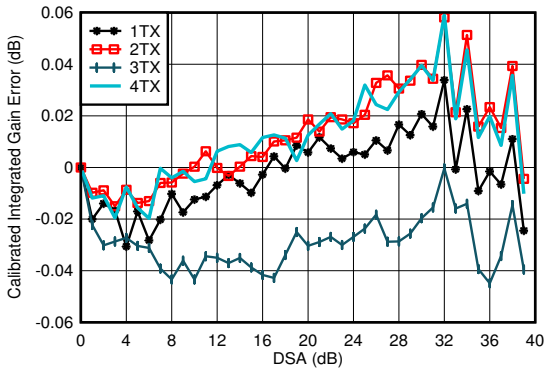
TX Typical Characteristics (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



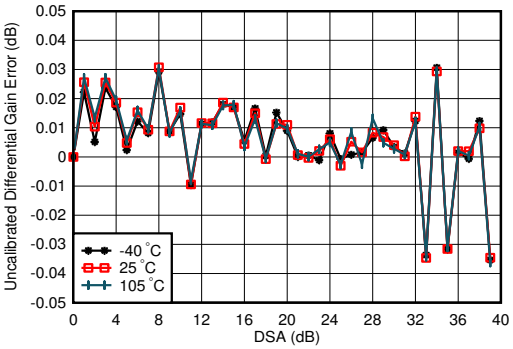
f_{DAC}=5898.24MSPS, interleave mode, matching at 1.8 GHz
Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + (DSA Setting)

Figure 405. TX Uncalibrated Integrated Gain Error vs DSA Setting and Channel at 1.8 GHz



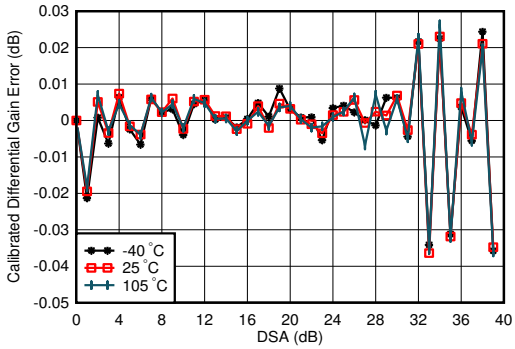
f_{DAC} = 5898.24MSPS, interleave mode, matching at 1.8 GHz
Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + (DSA Setting)

Figure 406. TX Calibrated Integrated Gain Error vs DSA Setting and Channel at 1.8 GHz



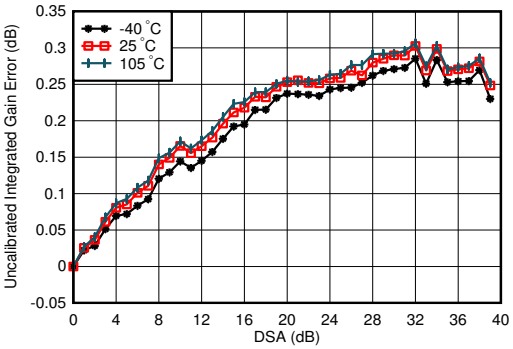
f_{DAC} = 5898.24MSPS, interleave mode, matching at 1.8 GHz
Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

Figure 407. TX Uncalibrated Differential Gain Error vs DSA Setting and Temperature at 1.8 GHz



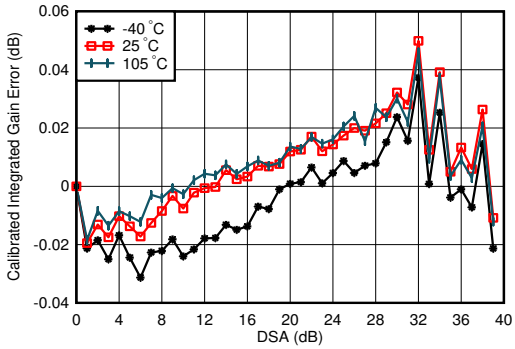
f_{DAC} = 5898.24MSPS, interleave mode, matching at 1.8 GHz
Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

Figure 408. TX Calibrated Differential Gain Error vs DSA Setting and Temperature at 1.8 GHz



f_{DAC} = 5898.24MSPS, interleave mode, matching at 1.8 GHz
Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + (DSA Setting)

Figure 409. TX Uncalibrated Integrated Gain Error vs DSA Setting and Temperature at 1.8 GHz

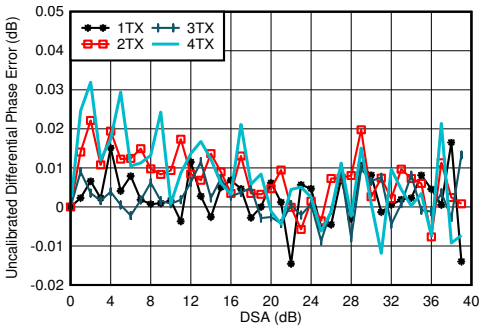


f_{DAC} = 5898.24MSPS, interleave mode, matching at 1.8 GHz
Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + (DSA Setting)

Figure 410. TX Calibrated Integrated Gain Error vs DSA Setting and Temperature at 1.8 GHz

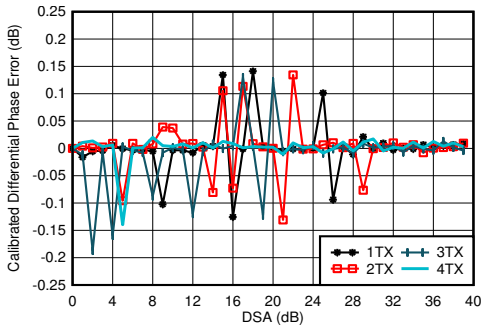
TX Typical Characteristics (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



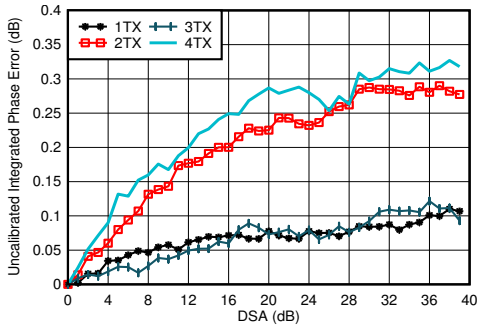
f_{DAC} = 5898.24MSPS, interleave mode, matching at 1.8 GHz
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

Figure 411. TX Uncalibrated Differential Phase Error vs DSA Setting and Channel at 1.8 GHz



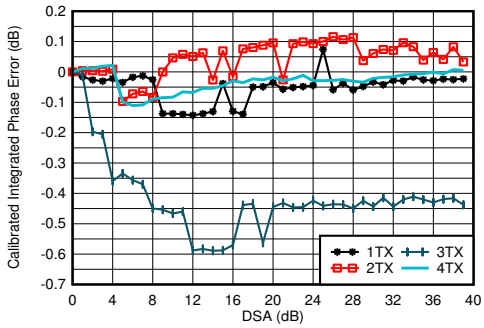
f_{DAC} = 8847.36MSPS, straight mode, matching at 2.6 GHz
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)
Phase DNL spike may occur at any DSA setting.

Figure 412. TX Calibrated Differential Phase Error vs DSA Setting and Channel at 1.8 GHz



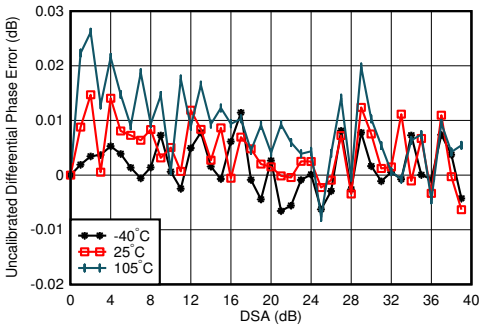
f_{DAC} = 5898.24MSPS, interleave mode, matching at 1.8 GHz
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

Figure 413. TX Uncalibrated Integrated Phase Error vs DSA Setting and Channel at 1.8 GHz



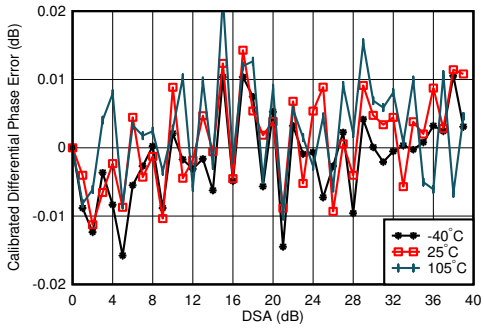
f_{DAC} = 5898.24MSPS, interleave mode, matching at 1.8 GHz
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

Figure 414. TX Calibrated Integrated Phase Error vs DSA Setting and Channel at 1.8 GHz



f_{DAC} = 5898.24MSPS, interleave mode, matching at 1.8 GHz
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

Figure 415. TX Uncalibrated Differential Phase Error vs DSA Setting and Temperature at 1.8 GHz

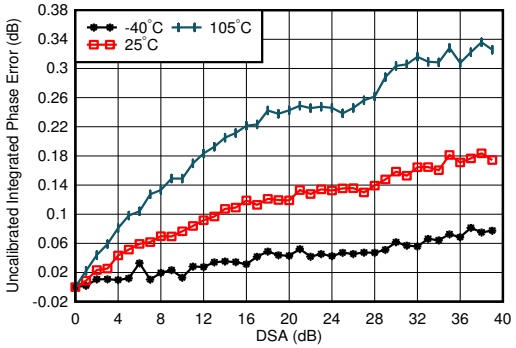


f_{DAC} = 5898.24MSPS, interleave mode, matching at 1.8 GHz, channel with the median variation over DSA setting at 25°C
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

Figure 416. TX Calibrated Differential Phase Error vs DSA Setting and Temperature at 1.8 GHz

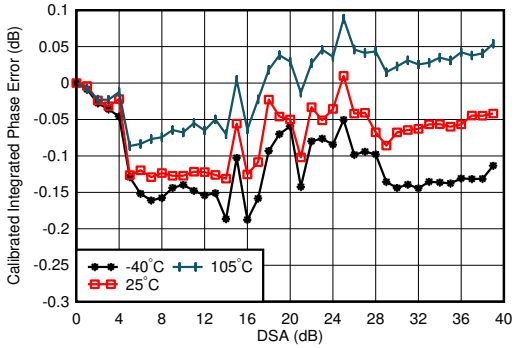
TX Typical Characteristics (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



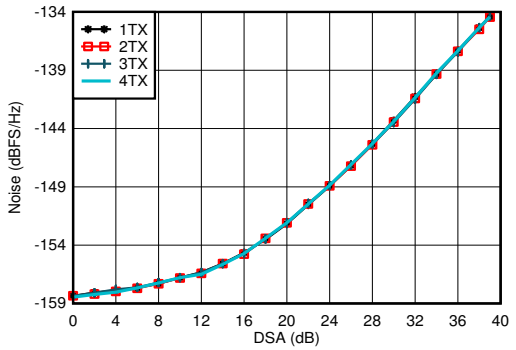
f_{DAC} = 5898.24MSPS, interleave mode, matching at 1.8 GHz, channel with the median variation over DSA setting at 25°C
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

Figure 417. TX Uncalibrated Integrated Phase Error vs DSA Setting and Temperature at 1.8 GHz



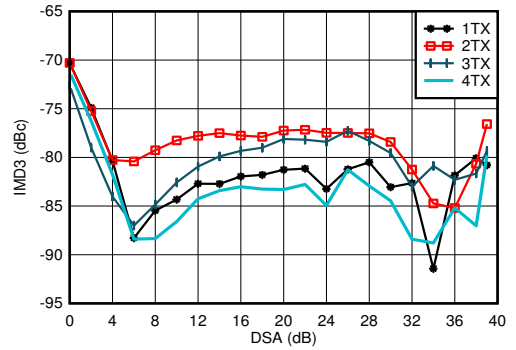
f_{DAC} = 5898.24MSPS, interleave mode, matching at 1.8 GHz, channel with the median variation over DSA setting at 25°C
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

Figure 418. TX Calibrated Integrated Phase Error vs DSA Setting and Temperature at 1.8 GHz



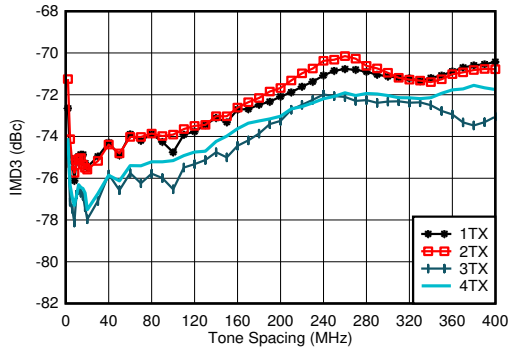
f_{DAC} = 5898.24MSPS, interleave mode, matching at 1.8 GHz, P_{OUT} = –13 dBFS

Figure 419. TX Output Noise vs Channel and Attenuation at 1.8 GHz



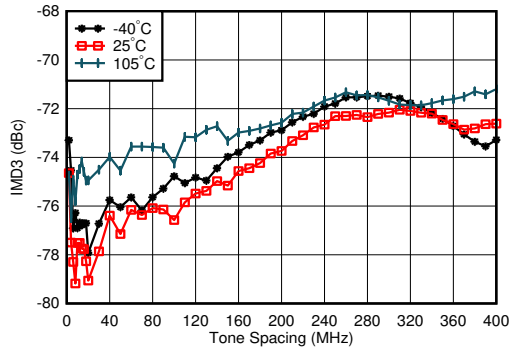
f_{DAC} = 11796.48MSPS, interleave mode, f_{CENTER} = 1.8 GHz, matching at 1.8 GHz, –13 dBFS each tone

Figure 420. TX IMD3 vs DSA Setting at 1.8 GHz



f_{DAC} = 11796.48MSPS, interleave mode, f_{CENTER} = 1.8 GHz, matching at 1.8 GHz, –13 dBFS each tone

Figure 421. TX IMD3 vs Tone Spacing and Channel at 1.8 GHz

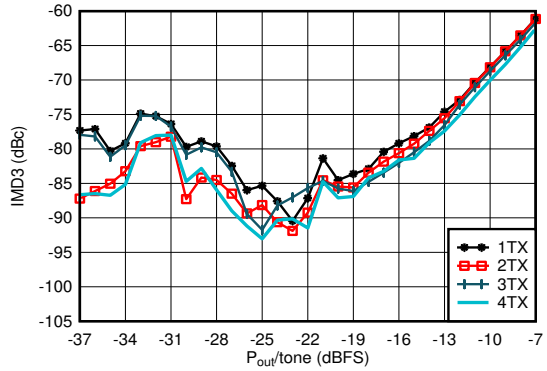


f_{DAC} = 11796.48MSPS, interleave mode, f_{CENTER} = 1.8 GHz, matching at 1.8 GHz, –13 dBFS each tone, worst channel

Figure 422. TX IMD3 vs Tone Spacing and Temperature at 1.8 GHz

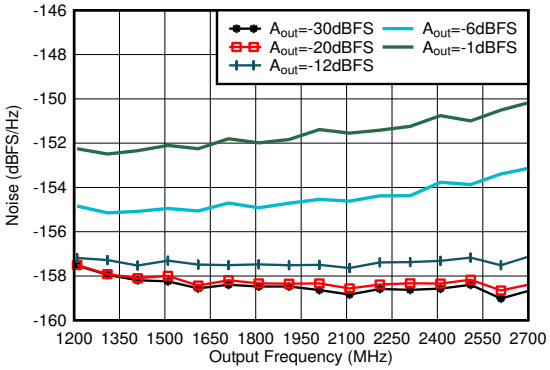
TX Typical Characteristics (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



f_{DAC} = 11796.48MSPS, interleave mode, f_{CENTER} = 1.8 GHz, $f_{SPACING}$ = 20 MHz, matching at 1.8 GHz

Figure 423. TX IMD3 vs Digital Level at 2.6 GHz

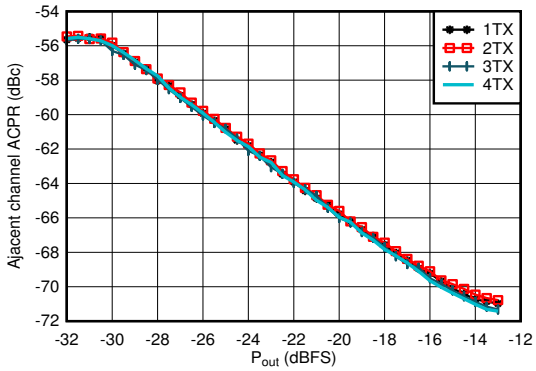


Matching at 2.6 GHz, Single tone, f_{DAC} = 11.79648GSPS, interleave mode, 40-MHz offset

Figure 424. TX Single Tone Output Noise vs Frequency and Amplitude at 1.8 GHz

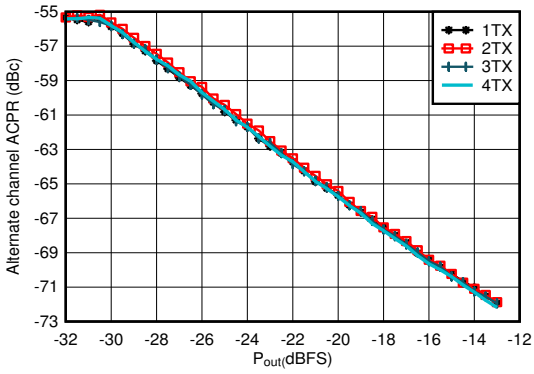
TM1.1, P_{OUT_RMS} = –13 dBFS

Figure 425. TX 20-MHz LTE Output Spectrum at 1.8425 GHz



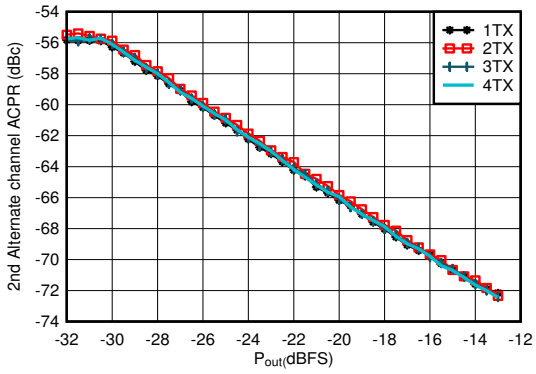
Matching at 1.8 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 426. TX 20-MHz LTE ACPR vs Digital Level at 1.8425 GHz



Matching at 1.8 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 427. TX 20-MHz LTE alt-ACPR vs Digital Level at 1.8425 GHz

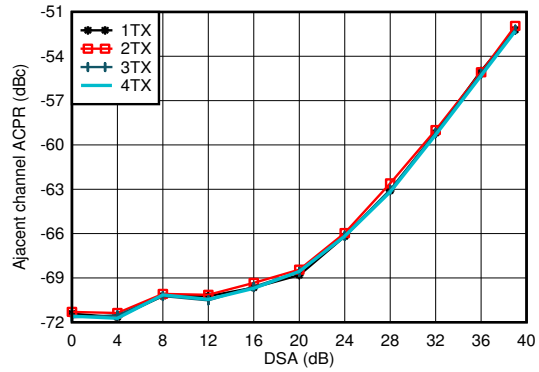


Matching at 1.8 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 428. TX 20-MHz LTE alt2-ACPR vs Digital Level at 1.8425 GHz

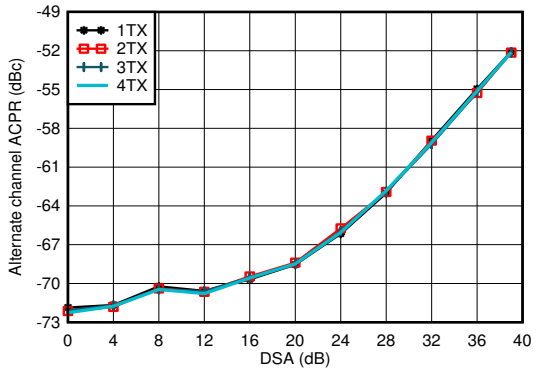
TX Typical Characteristics (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



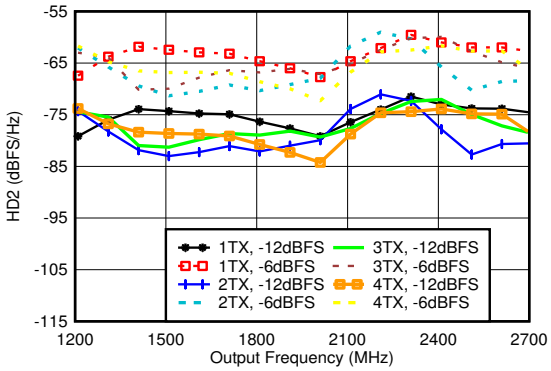
Matching at 1.8 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 429. TX 20-MHz LTE ACPR vs DSA at 2.6 GHz



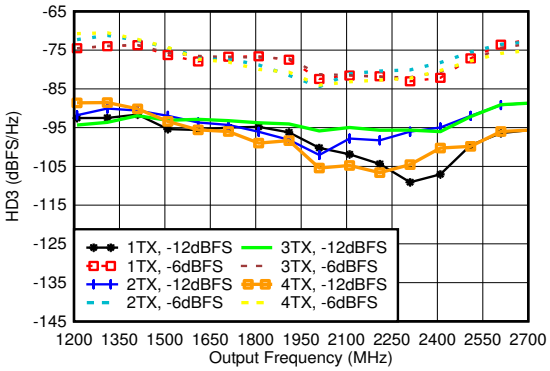
Matching at 1.8 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 430. TX 20-MHz LTE alt-ACPR vs DSA at 2.6 GHz



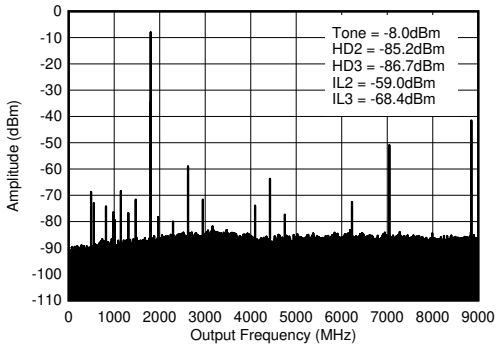
Matching at 1.8 GHz, f_{DAC} = 11.79648GSPS, interleave mode, normalized to output power at harmonic frequency

Figure 431. TX HD2 vs Digital Amplitude and Output Frequency at 1.8 GHz



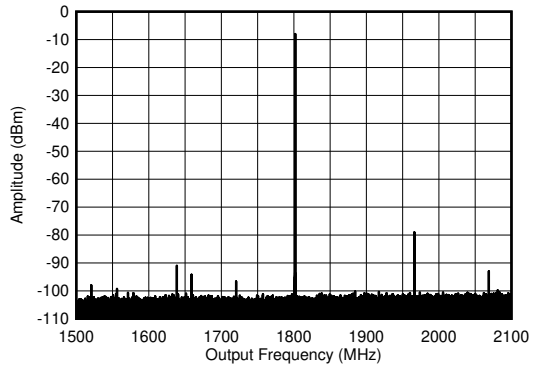
Matching at 1.8 GHz, f_{DAC} = 11.79648GSPS, interleave mode, normalized to output power at harmonic frequency

Figure 432. TX HD3 vs Digital Amplitude and Output Frequency at 1.8 GHz



f_{DAC} = 8847.36MSPS, interleave mode, 1.8 GHz matching, includes PCB and cable losses. ILn = $f_S/n \pm f_{OUT}$.

Figure 433. TX Single Tone (–12 dBFS) Output Spectrum at 1.8 GHz (0-f_{DAC})

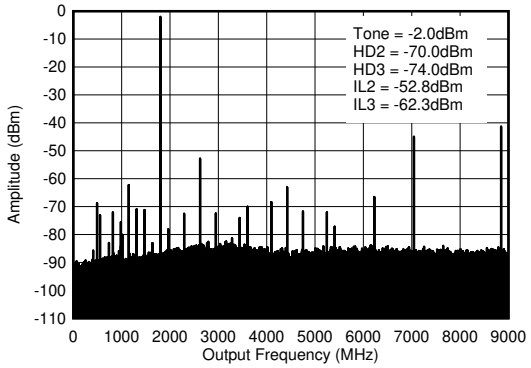


f_{DAC} = 8847.36MSPS, interleave mode, 1.8 GHz matching, includes PCB and cable losses

Figure 434. TX Single Tone (–12 dBFS) Output Spectrum at 1.8 GHz (±300 MHz)

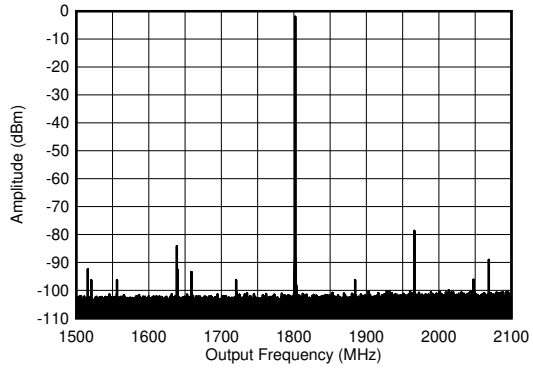
TX Typical Characteristics (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



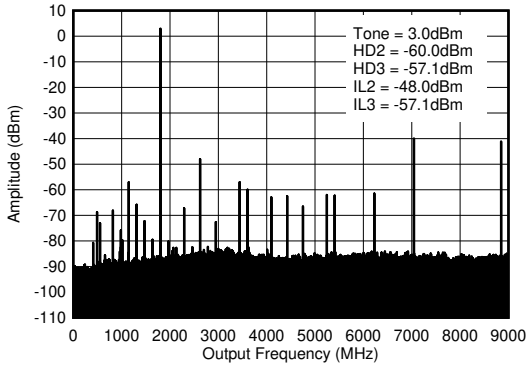
f_{DAC} = 8847.36MSPS, interleave mode, 1.8 GHz matching, includes PCB and cable losses. ILn = $f_S/n \pm f_{OUT}$.

Figure 435. TX Single Tone (–6 dBFS) Output Spectrum at 1.8 GHz (0-f_{DAC})



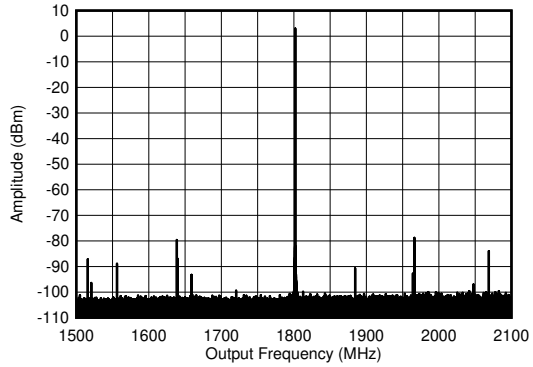
f_{DAC} = 8847.36MSPS, interleave mode, 1.8 GHz matching, includes PCB and cable losses

Figure 436. TX Single Tone (–6 dBFS) Output Spectrum at 1.8 GHz (±300 MHz)



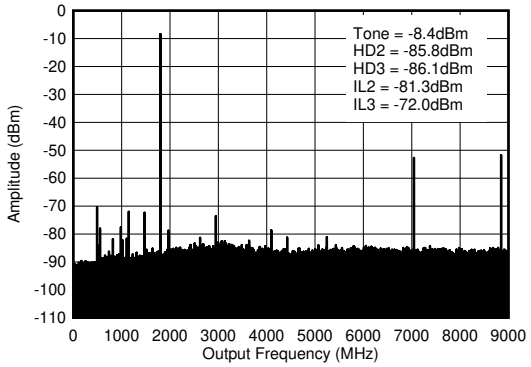
f_{DAC} = 8847.36MSPS, interleave mode, 1.8 GHz matching, includes PCB and cable losses. ILn = $f_S/n \pm f_{OUT}$.

Figure 437. TX Single Tone (–1 dBFS) Output Spectrum at 1.8 GHz (0-f_{DAC})



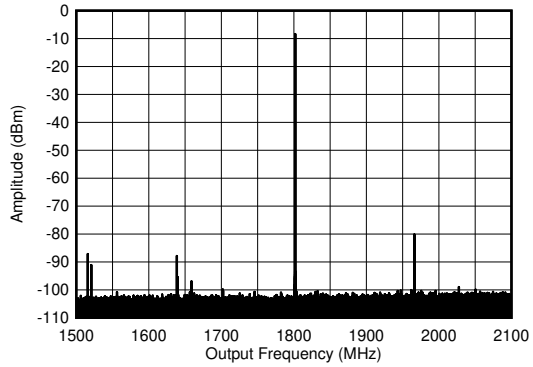
f_{DAC} = 8847.36MSPS, interleave mode, 1.8 GHz matching, includes PCB and cable losses

Figure 438. TX Single Tone (–1 dBFS) Output Spectrum at 1.8 GHz (±300 MHz)



f_{DAC} = 8847.36MSPS, straight mode, 1.8 GHz matching, includes PCB and cable losses. ILn = $f_S/n \pm f_{OUT}$ and is due to mixing with digital clocks.

Figure 439. TX Single Tone (–12 dBFS) Output Spectrum at 1.8 GHz (0-f_{DAC})

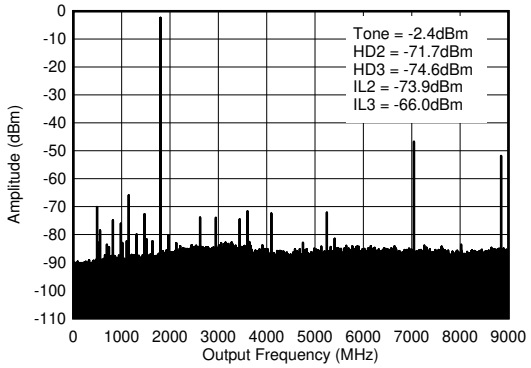


f_{DAC} = 8847.36MSPS, straight mode, 1.8 GHz matching, includes PCB and cable losses

Figure 440. TX Single Tone (–12 dBFS) Output Spectrum at 1.8 GHz (±300 MHz)

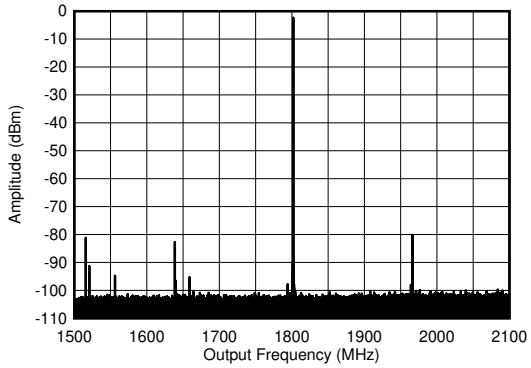
TX Typical Characteristics (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



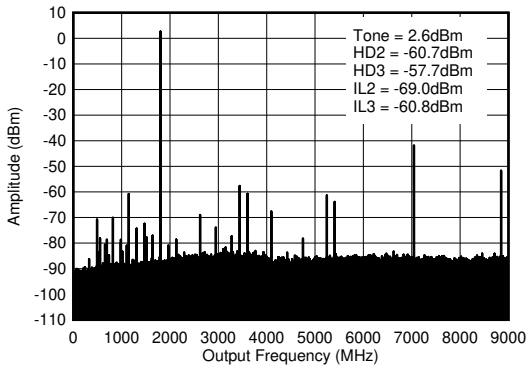
f_{DAC} = 8847.36MSPS, straight mode, 1.8 GHz matching, includes PCB and cable losses. ILn = $f_S/n \pm f_{OUT}$ and is due to mixing with digital clocks.

Figure 441. TX Single Tone (–6 dBFS) Output Spectrum at 1.8 GHz (0-f_{DAC})



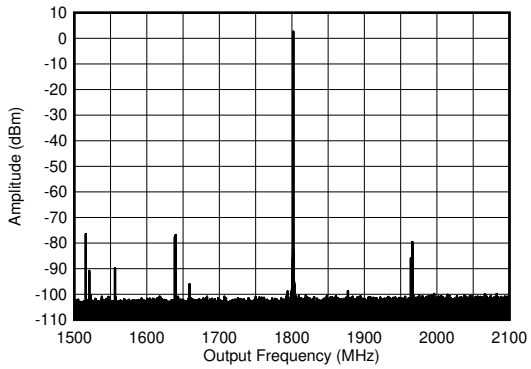
f_{DAC} = 8847.36MSPS, straight mode, 1.8 GHz matching, includes PCB and cable losses

Figure 442. TX Single Tone (–6 dBFS) Output Spectrum at 1.8 GHz (±300 MHz)



f_{DAC} = 8847.36MSPS, straight mode, 1.8 GHz matching, includes PCB and cable losses. ILn = $f_S/n \pm f_{OUT}$ and is due to mixing with digital clocks.

Figure 443. TX Single Tone (–1 dBFS) Output Spectrum at 1.8 GHz (0-f_{DAC})



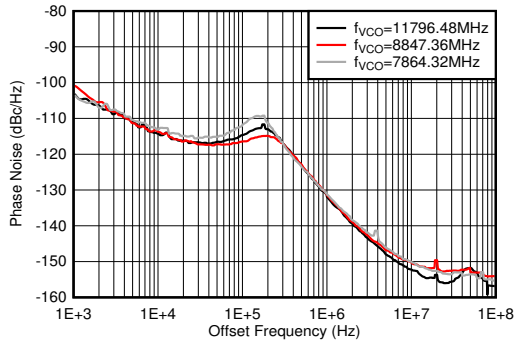
f_{DAC} = 8847.36MSPS, straight mode, 1.8 GHz matching, includes PCB and cable losses

Figure 444. TX Single Tone (–1 dBFS) Output Spectrum at 1.8 GHz (±300 MHz)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled

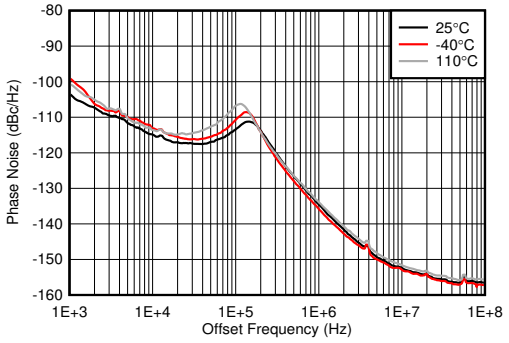
8.12.3 PLL and Clock Typical Characteristics

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, f_{REF} = 491.52 MHz, Phase noise measured at TX output



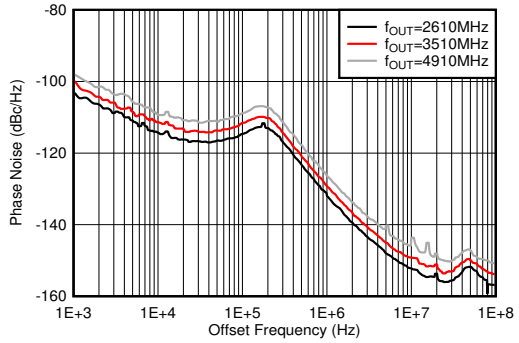
PLL enabled, f_{REF} = 491.52MSPS, measured at 2TXOUT

Figure 445. Phase Noise vs Offset Frequency and f_{VCO} at f_{OUT} = 2610 MHz



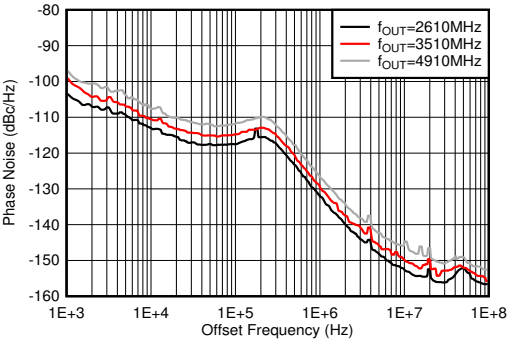
PLL enabled, f_{VCO} = 11796.48 MHz, f_{REF} = 491.52MSPS, measured at 2TXOUT

Figure 446. Phase Noise for 12-GHz VCO vs Offset Frequency and Temperature at f_{OUT} = 1910 MHz



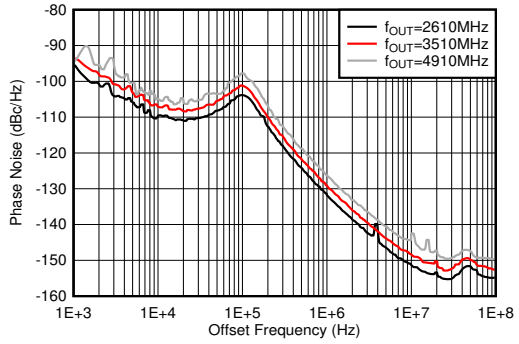
PLL enabled, f_{VCO} = 11796.48 MHz, f_{REF} = 491.52MSPS, measured at 2TXOUT

Figure 447. Phase Noise for 12-GHz VCO vs Offset Frequency and f_{OUT} at 25°C



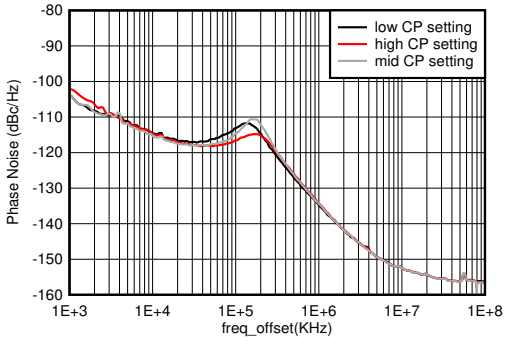
PLL enabled, f_{VCO} = 11796.48 MHz, f_{REF} = 491.52MSPS, measured at 2TXOUT

Figure 448. Phase Noise for 12-GHz VCO vs Offset Frequency and f_{OUT} at –40°C



PLL enabled, f_{VCO} = 11796.48 MHz, f_{REF} = 491.52MSPS, measured at 2TXOUT

Figure 449. Phase Noise for 12-GHz VCO vs Offset Frequency and f_{OUT} at 110°C

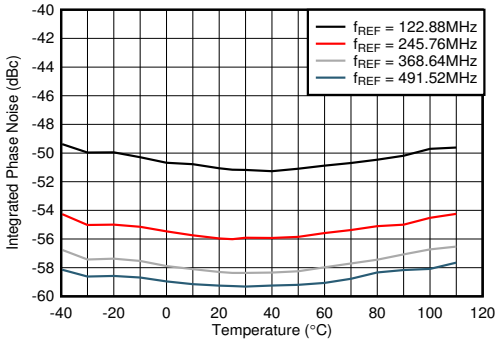


PLL enabled, f_{VCO} = 11796.48 MHz, f_{REF} = 491.52MSPS, measured at 2TXOUT

Figure 450. Phase Noise for 12-GHz VCO vs Offset Frequency and CP Setting at f_{OUT} = 2.6 GHz

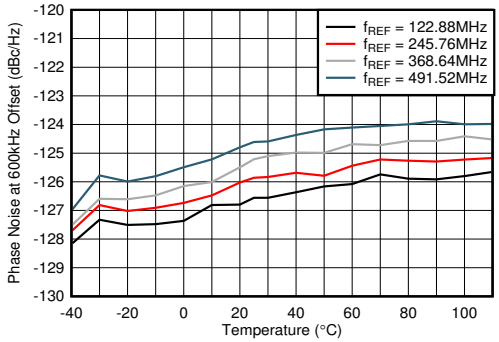
PLL and Clock Typical Characteristics (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, f_{REF} = 491.52 MHz, Phase noise measured at TX output



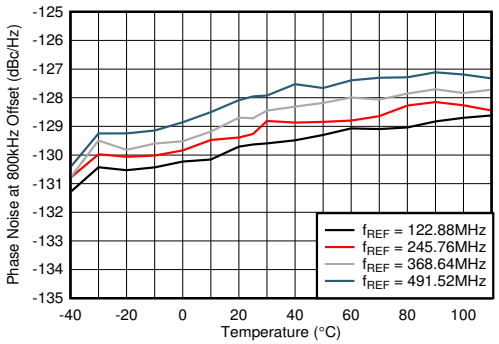
PLL enabled, f_{VCO} = 11796.48 MHz, 1-kHz to 100-MHz, single-sided integration bandwidth, measured at 2TXOUT

Figure 451. Integrated Phase Noise for 12-GHz VCO vs Temperature and f_{REF} at f_{OUT} = 2.6 GHz



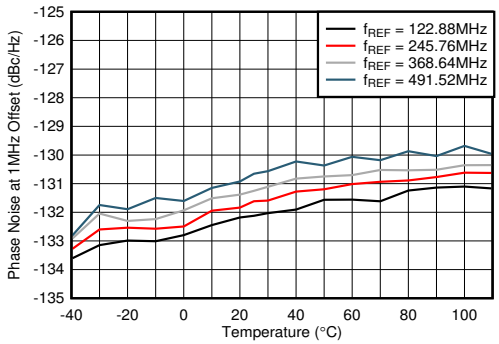
PLL enabled, f_{VCO} = 11796.48 MHz, measured at 2TXOUT

Figure 452. Phase Noise for 12-GHz VCO at 600kHz Offset vs Temperature and f_{REF} at f_{OUT} = 2.6 GHz



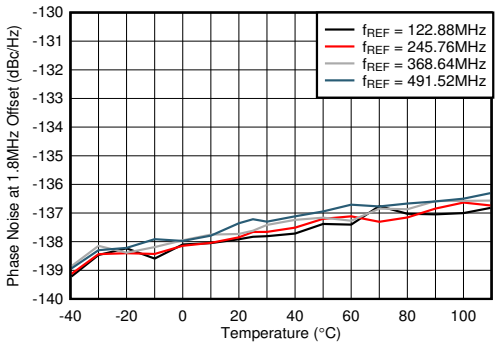
PLL enabled, f_{VCO} = 11796.48 MHz, measured at 2TXOUT

Figure 453. Phase Noise for 12-GHz VCO at 800-kHz Offset vs Temperature and f_{REF} at f_{OUT} = 2.6 GHz



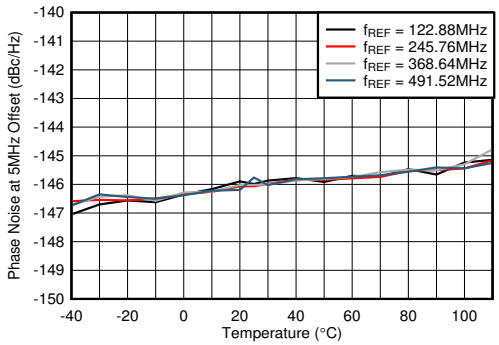
PLL enabled, f_{VCO} = 11796.48 MHz, measured at 2TXOUT

Figure 454. Phase Noise for 12-GHz VCO at 1-MHz Offset vs Temperature and f_{REF} at f_{OUT} = 2.6 GHz



PLL enabled, f_{VCO} = 11796.48 MHz, measured at 2TXOUT

Figure 455. Phase Noise for 12-GHz VCO at 1.8-MHz Offset vs Temperature and f_{REF} at f_{OUT} = 2.6 GHz

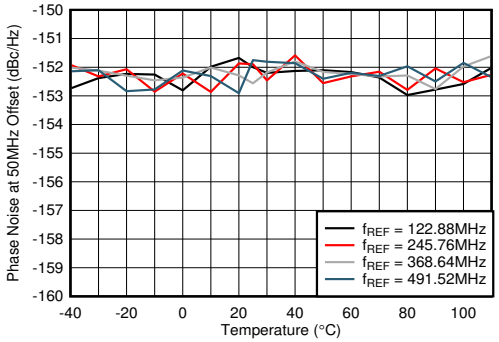


PLL enabled, f_{VCO} = 11796.48 MHz, measured at 2TXOUT

Figure 456. Phase Noise for 12-GHz VCO at 5-MHz Offset vs Temperature and f_{REF} at f_{OUT} = 2.6 GHz

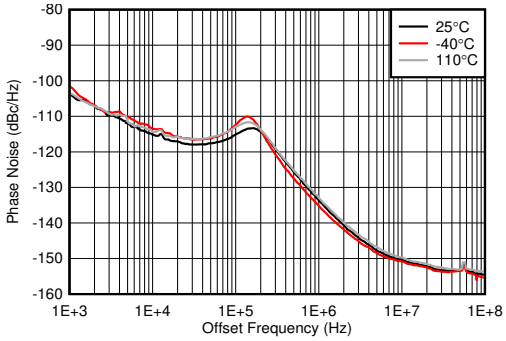
PLL and Clock Typical Characteristics (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, f_{REF} = 491.52 MHz, Phase noise measured at TX output



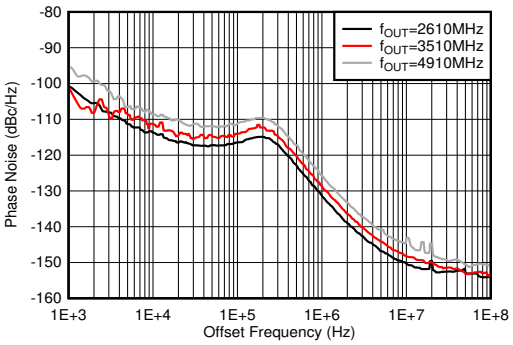
PLL enabled, f_{VCO} = 11796.48 MHz, measured at 2TXOUT

Figure 457. Phase Noise for 12-GHz VCO at 50-MHz Offset vs Temperature and f_{REF} at f_{OUT} = 2.6 GHz



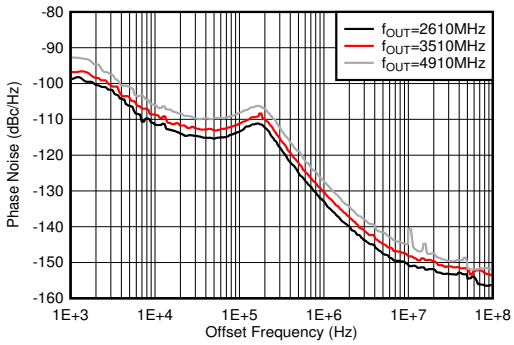
PLL enabled, f_{VCO} = 9830.4 MHz, f_{REF} = 491.52MSPS, measured at 2TXOUT

Figure 458. Phase Noise for 10-GHz VCO vs Offset Frequency and Temperature at f_{OUT} = 1910 MHz



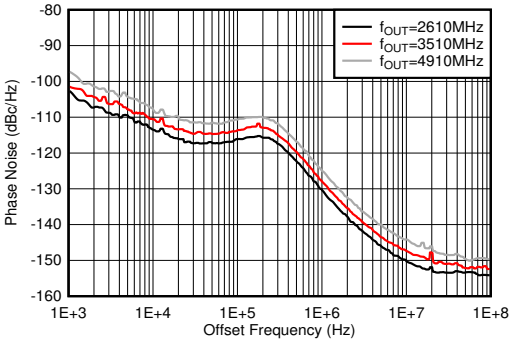
PLL enabled, f_{VCO} = 9830.4 MHz, f_{REF} = 491.52MSPS, measured at 2TXOUT

Figure 459. Phase Noise for 10-GHz VCO vs Offset Frequency and f_{OUT} at 25°C



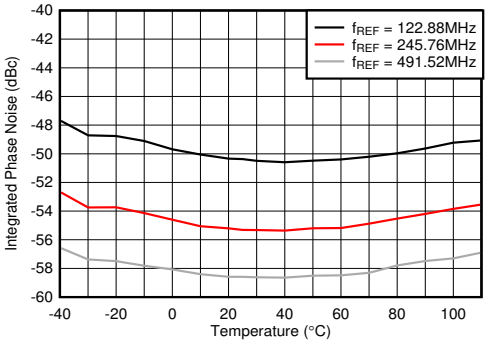
PLL enabled, f_{VCO} = 9830.4 MHz, f_{REF} = 491.52MSPS, measured at 2TXOUT

Figure 460. Phase Noise for 10-GHz VCO vs Offset Frequency and f_{OUT} at –40°C



PLL enabled, f_{VCO} = 9830.4 MHz, f_{REF} = 491.52MSPS, measured at 2TXOUT

Figure 461. Phase Noise for 10-GHz VCO vs Offset Frequency and f_{OUT} at 110°C

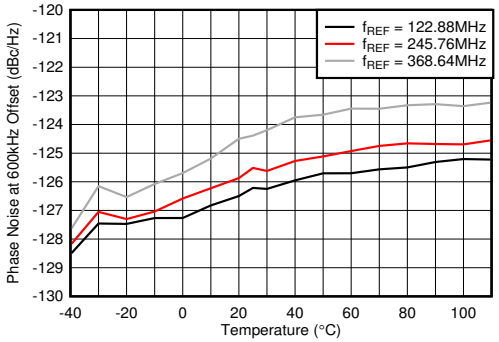


PLL enabled, f_{VCO} = 9830.4 MHz, 1-kHz to 100-MHz, single-sided integration bandwidth, measured at 2TXOUT

Figure 462. Integrated Phase Noise for 10-GHz VCO vs Temperature and f_{REF} at f_{OUT} = 2.6 GHz

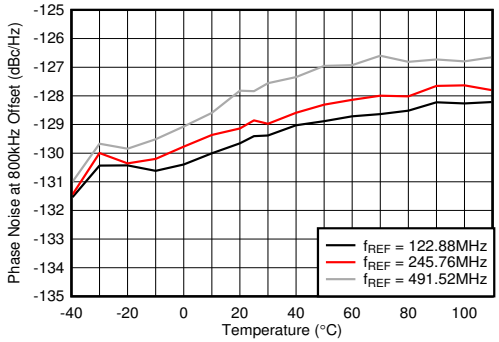
PLL and Clock Typical Characteristics (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, f_{REF} = 491.52 MHz, Phase noise measured at TX output



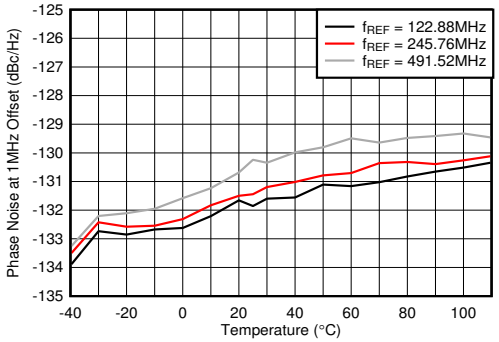
PLL enabled, f_{VCO} = 9830.4 MHz, measured at 2TXOUT

Figure 463. Phase Noise for 10-GHz VCO at 600 kHz vs Temperature and f_{REF} at f_{OUT} = 2.6 GHz



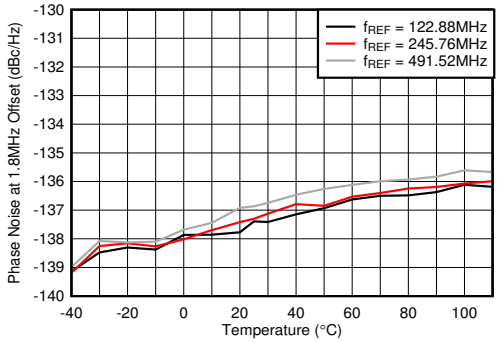
PLL enabled, f_{VCO} = 9830.4 MHz, measured at 2TXOUT

Figure 464. Phase Noise for 10-GHz VCO at 800 kHz vs Temperature and f_{REF} at f_{OUT} = 2.6 GHz



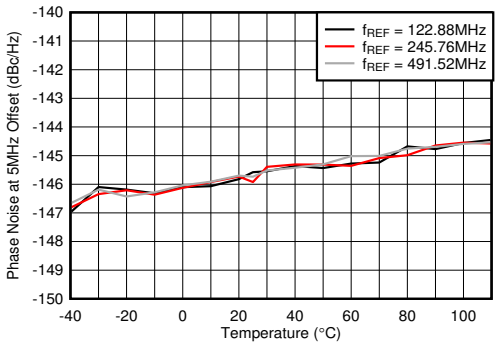
PLL enabled, f_{VCO} = 9830.4 MHz, measured at 2TXOUT

Figure 465. Phase Noise for 10-GHz VCO at 1 MHz vs Temperature and f_{REF} at f_{OUT} = 2.6 GHz



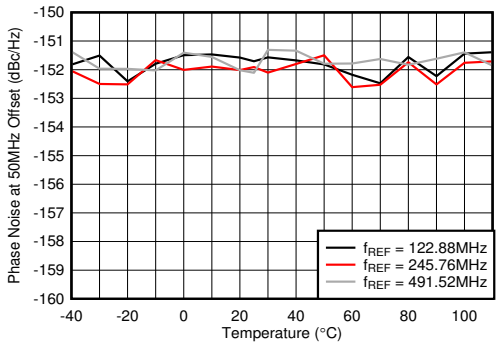
PLL enabled, f_{VCO} = 9830.4 MHz, measured at 2TXOUT

Figure 466. Phase Noise for 10-GHz VCO at 1.8 MHz vs Temperature and f_{REF} at f_{OUT} = 2.6 GHz



PLL enabled, f_{VCO} = 9830.4 MHz, measured at 2TXOUT

Figure 467. Phase Noise for 10-GHz VCO at 5 MHz vs Temperature and f_{REF} at f_{OUT} = 2.6 GHz

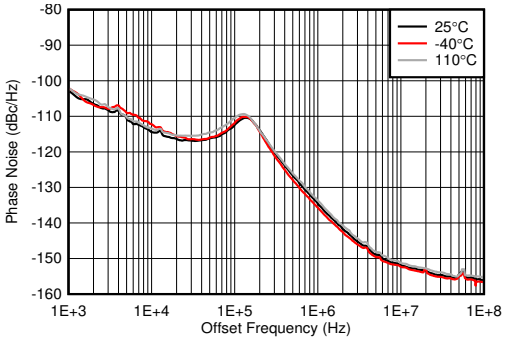


PLL enabled, f_{VCO} = 9830.4 MHz, measured at 2TXOUT

Figure 468. Phase Noise for 10-GHz VCO at 50 MHz vs Temperature and f_{REF} at f_{OUT} = 2.6 GHz

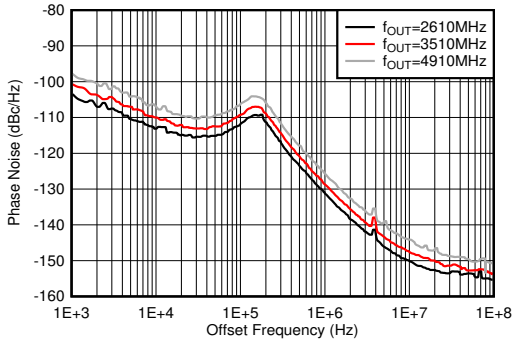
PLL and Clock Typical Characteristics (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, f_{REF} = 491.52 MHz, Phase noise measured at TX output



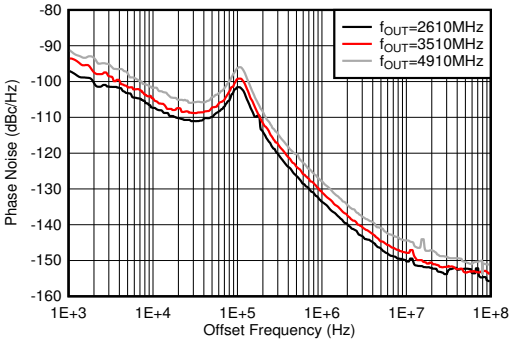
PLL enabled, f_{VCO} = 8847.36 MHz, f_{REF} = 491.52MSPS, measured at 2TXOUT

Figure 469. Phase Noise for 9-GHz VCO vs Offset Frequency and Temperature at f_{OUT} = 1910 MHz



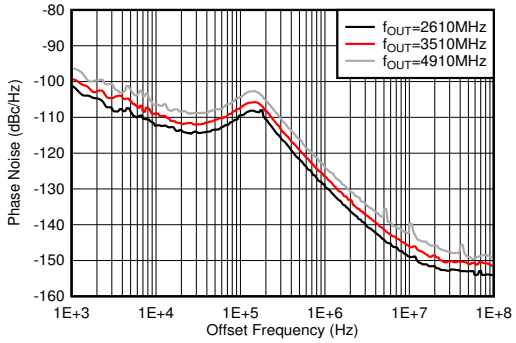
PLL enabled, f_{VCO} = 8847.36 MHz, f_{REF} = 491.52MSPS, measured at 2TXOUT

Figure 470. Phase Noise for 9-GHz VCO vs Offset Frequency and f_{OUT} at 25°C



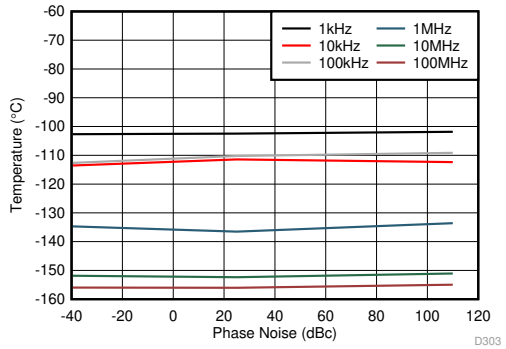
PLL enabled, f_{VCO} = 8847.36 MHz, f_{REF} = 491.52MSPS, measured at 2TXOUT

Figure 471. Phase Noise for 9-GHz VCO vs Offset Frequency and f_{OUT} at –40°C



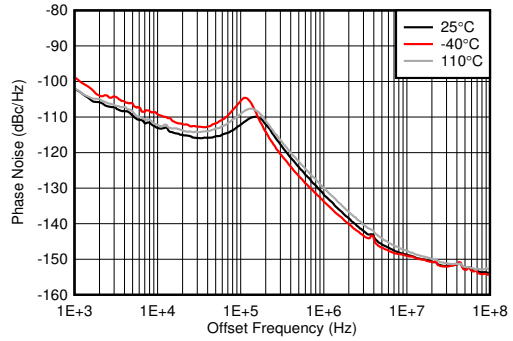
PLL enabled, f_{VCO} = 8847.36 MHz, f_{REF} = 491.52MSPS, measured at 2TXOUT

Figure 472. Phase Noise for 9-GHz VCO vs Offset Frequency and f_{OUT} at 110°C



PLL enabled, f_{VCO} = 8847.36 MHz, f_{REF} = 491.52MSPS, minimum LPF BW, measured at 2TXOUT

Figure 473. Phase Noise for 9-GHz VCO vs Temperature Over Offset Frequency at f_{OUT} = 2.6 GHz



PLL enabled, f_{VCO} = 7864.32 MHz, f_{REF} = 491.52MSPS, measured at 2TXOUT

Figure 474. Phase Noise for 8-GHz VCO vs Offset Frequency and Temperature at f_{OUT} = 1910 MHz

9 Detailed Description

9.1 Overview

The AFE79xx is a family of high performance multi-channel transceivers , integrating 4 RF sampling DAC transmitters, 4 RF sampling ADC receivers, and two RF sampling digitizing auxiliary chains (feedback paths - AFE792x only).

Each receiver (RX) and feedback (FB) path includes a DSA (Digital Step Attenuator), followed by a 3-GSPS RF sampling ADC (non-interleaved). Each receiver channel has an analog peak power detector and various digital power detectors to assist an external or internal autonomous AGC control, and a RF overload detector for device reliability protection. The RX ADC is followed by a flexible dual (AFE7920 and AFE7988 only) or single band DDC (digital down converter) to reduce the sample rate to only the bands of interest. The FB ADC is followed by a single wide BW DDC.

Each transmitter (TX) includes a dual (AFE7920 and AFE7988 only) or single band DUC (digital up converter), followed by a 12-GSPS RF sampling DAC driving a wideband RF amplifier (DSA). The DAC has zero order hold output to emphasize the 1st Nyquist output and a mixed mode output to emphasize the 2nd Nyquist zone.

Each DUC and DDC path integrates two independent NCOs that allows fast switching between two RF frequencies, while maintaining the phase of each NCO when not in use.

9.2 Functional Block Diagrams

The functional block diagram of the AFE7920/21 is shown in Figure 475 and the AFE7988/89 in Figure 476.

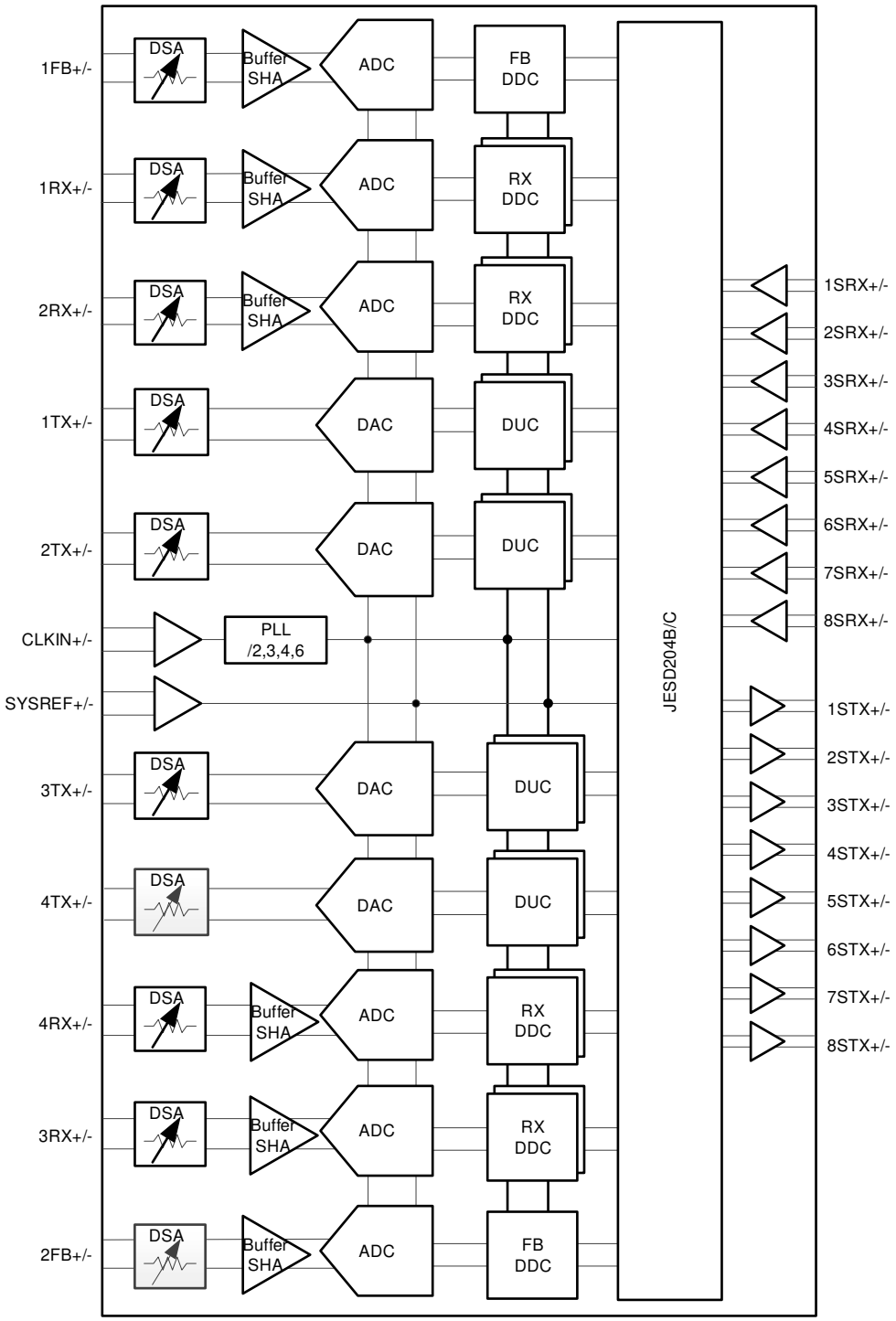


Figure 475. AFE7920/21 Block Diagram

Functional Block Diagrams (continued)

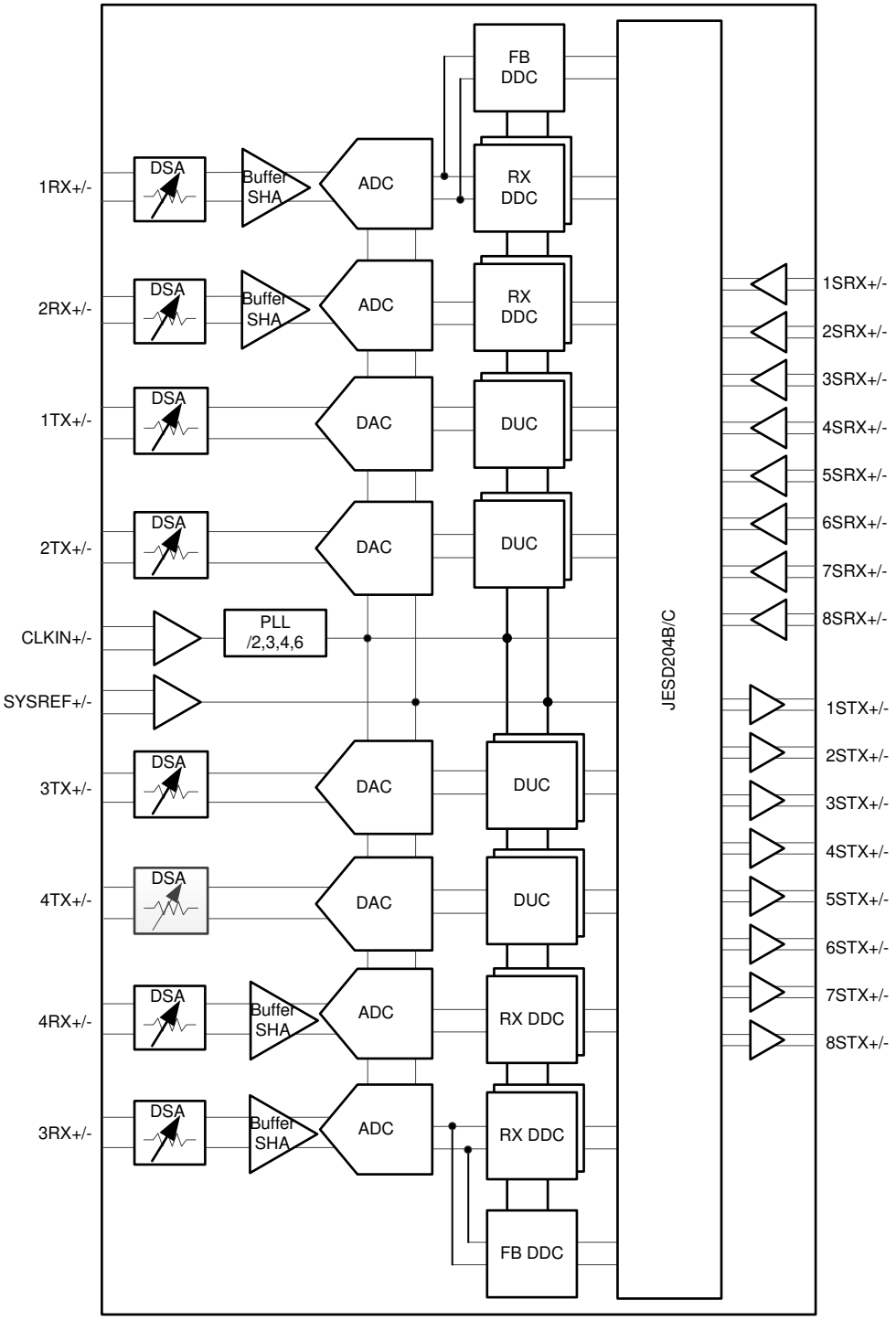


Figure 476. AFE7988/89 Functional Block Diagram

9.3 Feature Description

9.3.1 Operation Modes

The AFE79xx can be configured in the following operating modes:

- Power-On-Reset Mode: this is the status of the device at power up and after any device $\overline{\text{RESET}}$ event.
- Active Mode: all clocks are running, all PLL are locked, all circuits are properly biased, JESD links are established, and digital functions are turned on.
- Standby Mode: defined for the transmitters, receivers, and feedback chains. In this mode, the chain is set to minimum power dissipation, while maintaining a fast wake-up time to active mode (typically less than 2 µs), by selectively powering down blocks of the chain. The JESD links are maintained in this mode. This mode is configured through the SPI and then activated through the allocated enable GPIO pins.
- Sleep Mode: in this status the device power dissipation is further reduced compared to the Standby Mode, but the wake-up time to Active Mode is slower. The JESD links are shut down in this mode and will need to be re-established when coming out of sleep mode. The Sleep Mode can be configured through the SPI and it is activated through the Sleep pin. In the default configuration, all blocks are off, but the PLL, the internal power management bias and internal controller.

9.3.2 Receiver (RX) Chain

The AFE7920/88 receiver block diagram with dual DDCs is shown in Figure 477. The AFE7921/AFE7989 receiver block diagram with single DDC is shown in Figure 478. Peak power detectors, a DSA, and a 3-GSPS non-interleaved ADC form the analog portion of the RX chain. The digital section of the receive chain includes digital peak and RMS power detectors, an autonomous AGC, complex mixers to down convert the wanted signal to baseband, decimation filters to reduce the sample rate to the target output rate, a digital compensation block to provide constant input-to-output gain and an output format block.

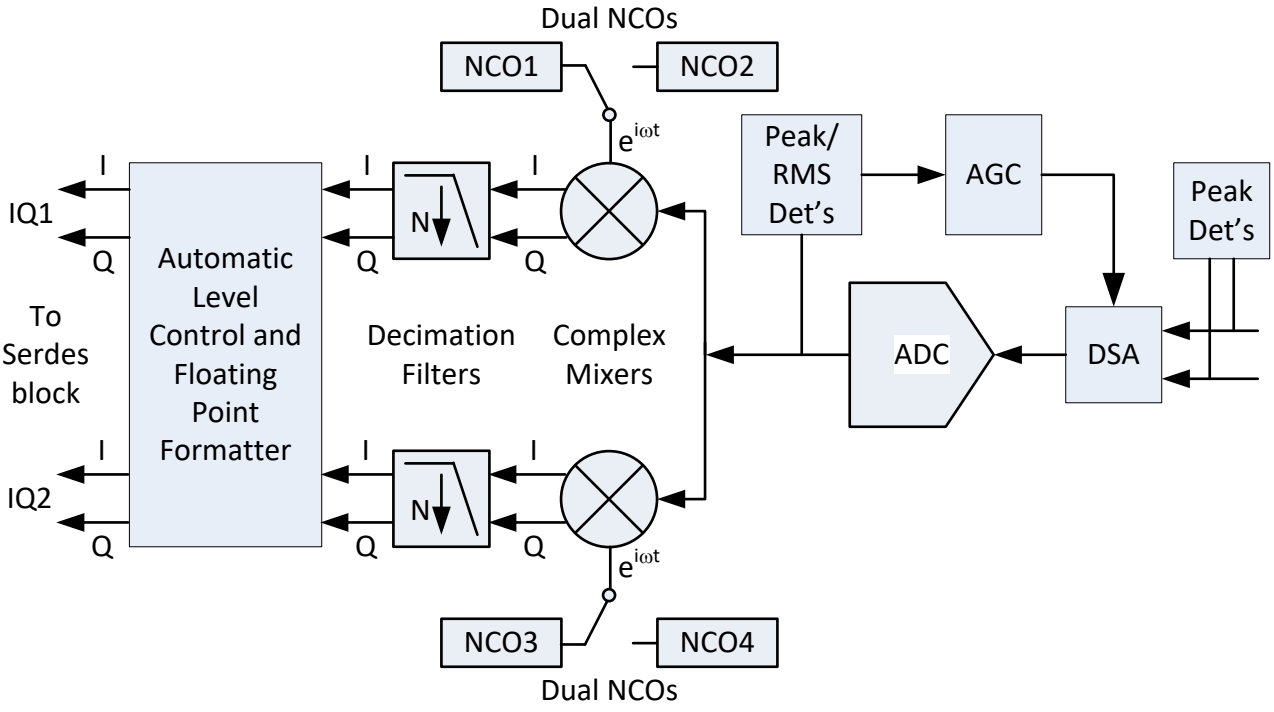


Figure 477. AFE7920/88 RX Chain Block Diagram

Feature Description (continued)

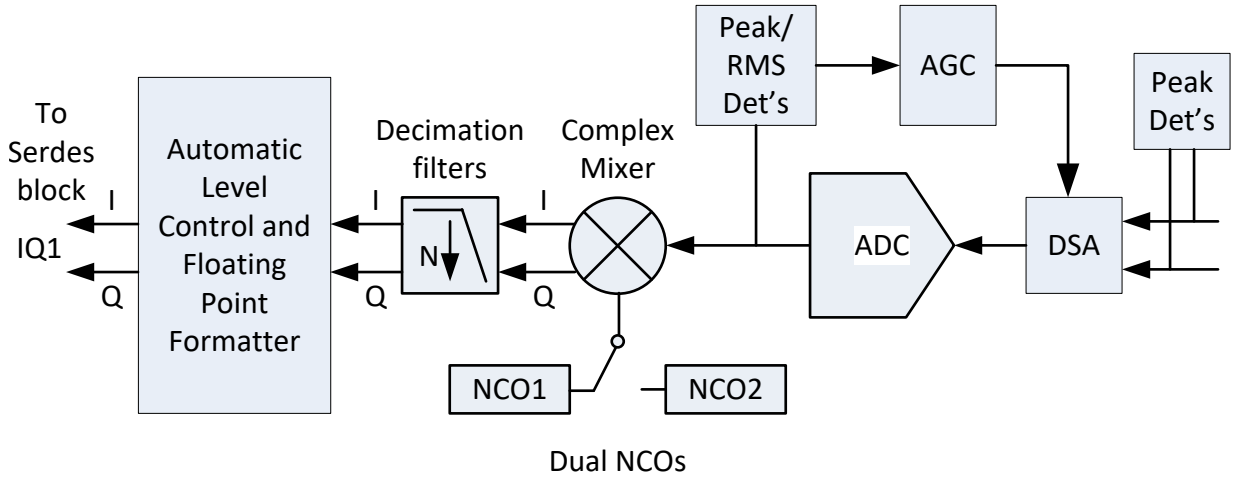


Figure 478. AFE7921/89 RX Chain Block Diagram

9.3.2.1 RX Chain DSA

The input stage of the receiver chain is a programmable Digital Step Attenuator (DSA), whose goal is to extend the effective dynamic range of the RX chain by attenuating the large signals before reaching the ADC. The attenuation setting of the DSA can be controlled in several ways through the Serial Programming Interface (SPI), GPIO pins, or an internal Automatic Gain Controller (AGC). At power up the default method to change the DSA setting is the direct access to the dedicated internal registers through the SPI. For a faster change of the DSA attenuation value, the AFE79xx has the option to use dedicated GPIO pins to directly control the DSA setting.

9.3.2.2 RX DSA Gain and Phase Correction

The RX DSA has a gain and phase correction block to reduce the offset in gain and phase for each DSA setting. This is expected to be calibrated in the customer factory or at start-up through the DSA calibration macro.

9.3.2.3 External DSA Control

The device supports different modes of the direct DSA control access through the pins.

- Parallel 3 bits per RX chain. In this mode, 3 GPIO balls are allocated for each RX chain to implement 3 bits control of the DSA. The actual DSA attenuation setting is defined according to Equation 1:

$$DSA\_ATT_{act} = \min(ATT_{min} + B[2..0] \times ATT_{step}, ATT_{max}) \quad (1)$$

  where
  - B[2..0] are the external controlling 3 bits (through parallel GPIO pins).
  - ATT_{min} is a variable defining the minimum attenuation. It is programmable through the SPI and it can be set differently for each of the 4 receiver chains.
  - ATT_{step} defines the step of the controlling word. It is programmable through the SPI and it can be set differently for each of the 4 receiver chains.
  - ATT_{max} is the maximum attenuation, configurable through the SPI up to 25 dB. It is possible to define two different ATT_{max} values, one for RX1/RX2 and one for RX3/RX4.
- Shared Parallel 5 or 6 bits with DSA select and latch. In this mode the 0 to 25 dB range of the DSA can be controlled by 5 or 6 parallel bits with 1-dB steps or 6 parallel bits with 0.5-dB steps. For every two receivers, there are allocated 5 pins for the parallel word control, a separate select and latch pins allow to load the DSA setting into the selected DSA.

When the AFE79xx internal AGC is enabled the RX chain DSA attenuation setting is directly controlled by the internal AGC block.

All the above modes can be configured through the SPI.

Feature Description (continued)

9.3.2.4 RX Peak and Power Detectors

Figure 479 shows the locations of the analog and digital detectors in the RX chain.

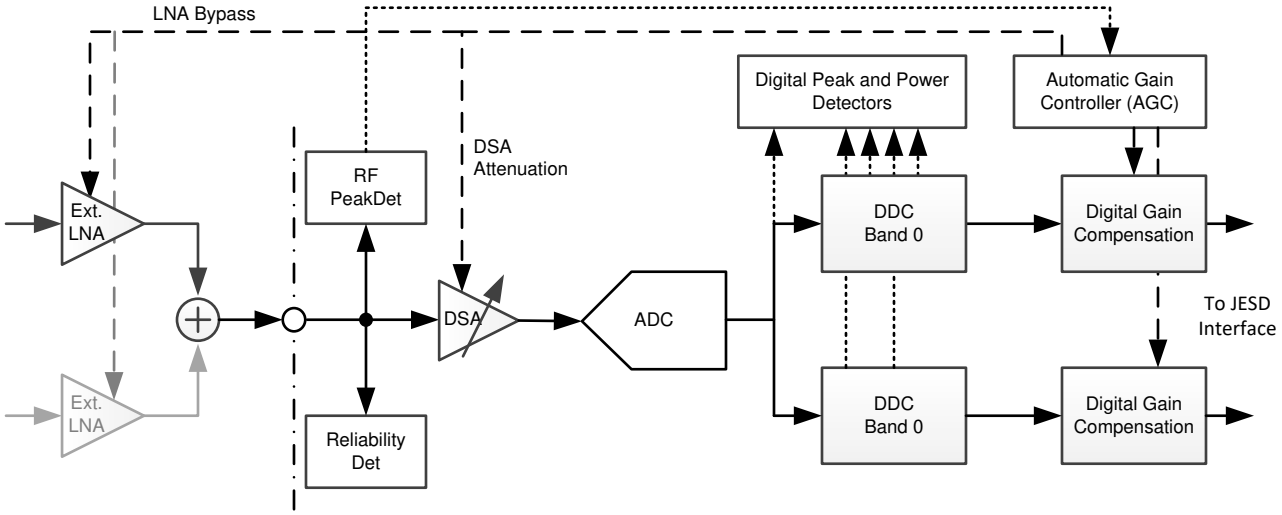


Figure 479. RX Chain: AGC and Detectors

9.3.2.4.1 RF/Analog Peak Detectors

Located at the RF input of each receiver chain, the RF/analog peak detector thresholds are scaled based on the actual DSA attenuation setting, and can be equivalent to the DSA output. Only an attack detector is available. Each one has programmable thresholds, configurable in 1-dB steps from –10 dBFS to +1 dBFS. The number of threshold crossings is counted over a block period, programmable from approximately 10 ns to 40 ms. The number of crossings is then compared to a programmable threshold, which then can generate a trigger.

In internal AGC mode, the detectors can be used to control the DSA gain and/or LNA bypass. In external AGC mode, the detectors outputs can be made available at dedicate GPIO pins.

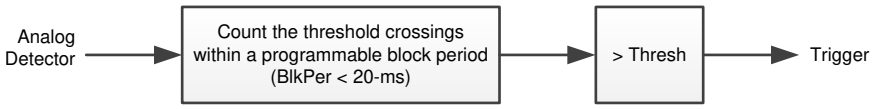


Figure 480. RF/Analog Peak Detector Block Diagram

9.3.2.4.2 Reliability RF Peak Detector

The AFE79xx integrates at the RF input pins of the receiver chain a dedicated peak detector that monitors the input levels to ensure that the levels do not exceed the maximum usable full scale power. Both attack and decay are built-in (in digital) to the same analog reliability detector. When the maximum full scale is exceeded, the DSA is set to maximum attenuation, the difference in gain is compensated in digital, and a flag available in the status register or through a dedicated pin is enabled.

The reset of the alarm can be done in 3 different modes:

- Decay detector indicating that signal level is lower than reliability levels.
- Decay detector indicating that signal level is lower than reliability levels along with an SPI bit set by the user.
- Automatically clear it after a programmable time.

The reliability detector mechanism is same in both internal and external AGC Mode.

9.3.2.4.3 ADC Digital Peak and Power Detector

At ADC output, there are multiple digital peak and power detectors. In a typical use case the peak detector is used to maintain the level at the ADC input below the programmed back-off.

Feature Description (continued)

Two independent thresholds for attack (big and small step) and decay (big and small step) can be configured. All four detectors are identical. The number of threshold crossings is counted over a programmable block period and compared to configurable target value to determine that the detector has triggered. In internal AGC mode, the detectors can be used to control the DSA gain and/or LNA bypass. In external AGC mode, each peak detector output can be made available at pins.

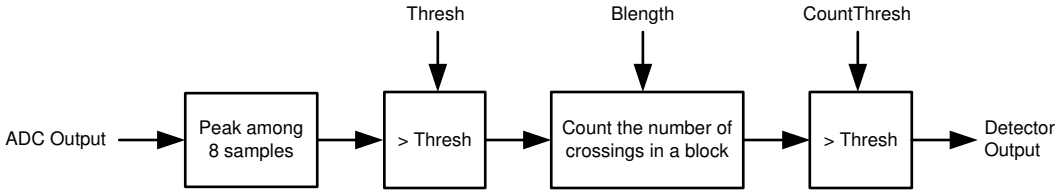


Figure 481. ADC Output Digital Peak Detector Block Diagram

Table 1. Digital Detectors Parameters

PARAMETER	DESCRIPTION	TYPE	RANGE
Thresh	Level comparison threshold	Linear 12-bit resolution	0 to 4095 Threshold in dBFs = 20 × Log(Thresh/4095)
Blength	Time interval where to count number of crossings	Integer	Integer multiples of $f_{ADC}/8$, up to 20 ms.
CountThresh	Number of crossing threshold	Integer	1 to Blength

The digital power detectors share the same tap off points as the digital peak detectors and have both attack and decay thresholds. Power is calculated as the square as the ADC output value. The integration time is between 10 ns and 10 ms, and the threshold can be configured between 0 and –30 dBFS with 0.2-dB steps (see Figure 482).

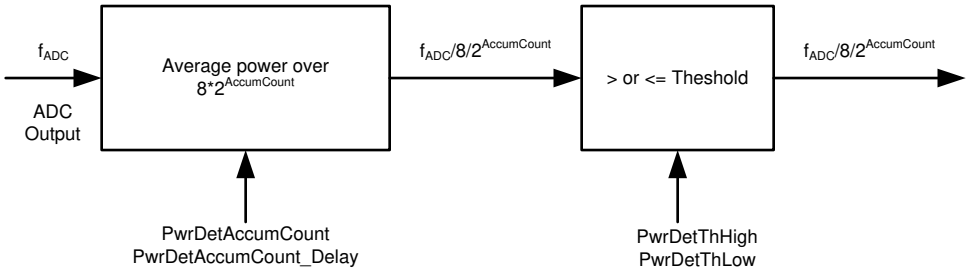


Figure 482. ADC Output Digital Power Detector Processing

9.3.2.4.4 DDC Digital Peak Detectors

The digital downconverter (DDC) offers various tap off points for digital peak detectors. In dual DDC modes, each DDC can have separate detectors. The block diagram of the detector is shown in Figure 483. The Max of the absolute value of I and Q is compared to a programmable threshold. The number of crossings within a time block of programmable length is counted, and this is compared to a threshold for the final detector output.

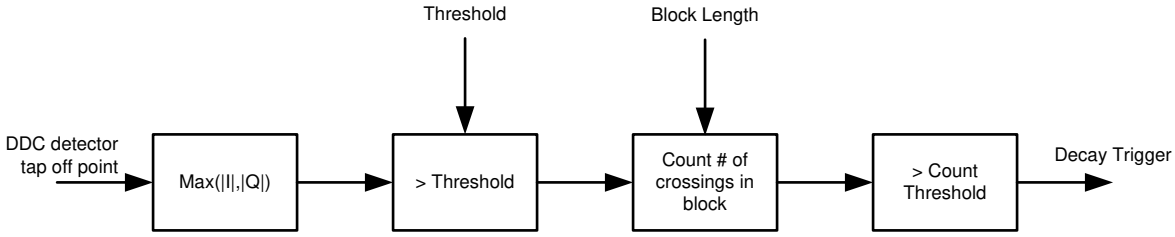


Figure 483. DDC Digital Peak Detector Block Diagram

It is expected that the tap off point either at the DDC output or before the final decimation state would be used. Table 2 shows the bandwidth of the tap off point before the final DDC decimation stage for different sample rates and decimation factors.

Table 2. DDC Detector Tap Off Point Before Final Stage

f_{ADC} (MSPS)	DECIMATION FACTOR	AGC BW (MHz)
2949.12	8	+/- 200
2457.6	10	+/- 200
2949.12	12	+/- 200
2949.12	16	+/- 150
2457.6	20	+/- 100
2949.12	24	+/- 100
2949.12	32	+/- 75
2457.6	40	+/- 50
2949.12	48	+/- 50

9.3.2.5 Internal Automatic Gain Control (AGC)

The AFE79xx receiver chain integrates all the blocks (multiple analog and digital detectors and an AGC controller) to enable an autonomous Automatic Gain Control. The AGC, detectors and gain control options are shown in Figure 479. Four different analog peak detectors are located in the RF portion of the RX chain. At the ADC output, there are four digital peak detectors and one power detector. There are also peak detectors in the digital down converters (DDCs), which are then band-specific for dual band devices and configurations.

In internal AGC mode, the output of each detector goes to the internal AGC controller that sets the RX DSA attenuation setting based on the programmed configuration, which includes comparison thresholds, integration time for attack and decay, and so forth. In this mode, the device has also the option to control an external gain step (like a LNA bypass control, for example) through dedicated GPIO pins. The integrated Digital Gain block can be used to implement the Digital Gain Compensation (DGC) function, which compensates for the RF gain change in digital so that the overall gain from analog input to JESD output is constant.

9.3.2.5.1 Timing Control of the AGC

The AGC has options for controlling how the AGC behaves during switching between IDLE, RX, and FB modes during TDD operation. For FDD, it is expected that the AGC would run continuously. The AGC start can also be delayed by the programmable value.

There are several options to specify the condition of the AGC during FB and IDLE modes and at the start of the RX mode. The AGC can be programmed to continue with the same gain as at the end of the previous RX mode. Alternatively, the AGC gain restarts with the default gain and LNA bypass state.

The maximum and minimum DSA setting can also be programmed. The DSA attenuation will not exceed this range. After the AGC changes the gain, the detector block accumulation will restart. The restart time can be delayed by a programmable value. This will prevent transitory effects of the gain change from affecting the next block accumulation.

The AGC can be frozen at the current gain settings and stop updating through SPI programming or the dedicated GPIO pins.

It is also possible to determine if the AGC DSA or LNA bypass setting has changed since the last inquiry through SPI programming and readback the DSA and LNA bypass actual values:

- TDD Mode – Carry over the RX gain from previous RX time slot.
  - Also has an option to start with a default gain setting for every RX time slot.
  - Decay Detectors can carry over the state from one RX time slot to the next RX time slot.
  - Attack Detectors are always reset during RX OFF
- Internal AGC Freeze either through register or pin – Freezes the state of the Detectors and the gain information
- Gain Swap Mode – treated similar as TDD Mode by the AGC Control algorithm
  - The gain will “be frozen during Gain Swap and continue after Gain Swap is removed” or “restart with

default setting after Gain Swap is removed”

– Analog Gain settings during “Gain Swap” can be configured for DSA and the LNA’s of both the bands

9.3.2.5.2 Temperature Compensation for External LNA Gain

The External LNA gain for one or both bands can be pre-configured through SPI registers as a function of temperature. There are 32 gains and phases as a function of temperature range for each band LNA. The device temperature can be used as an indicator of the external LNA temperature. Optionally, the external LNA gain can be dynamically programmed through SPI registers

9.3.2.5.3 AGC Flow

The AGC flow is shown in Figure 484. The flow starts with the reliability detectors, then attack detectors, and finally the decay detectors.

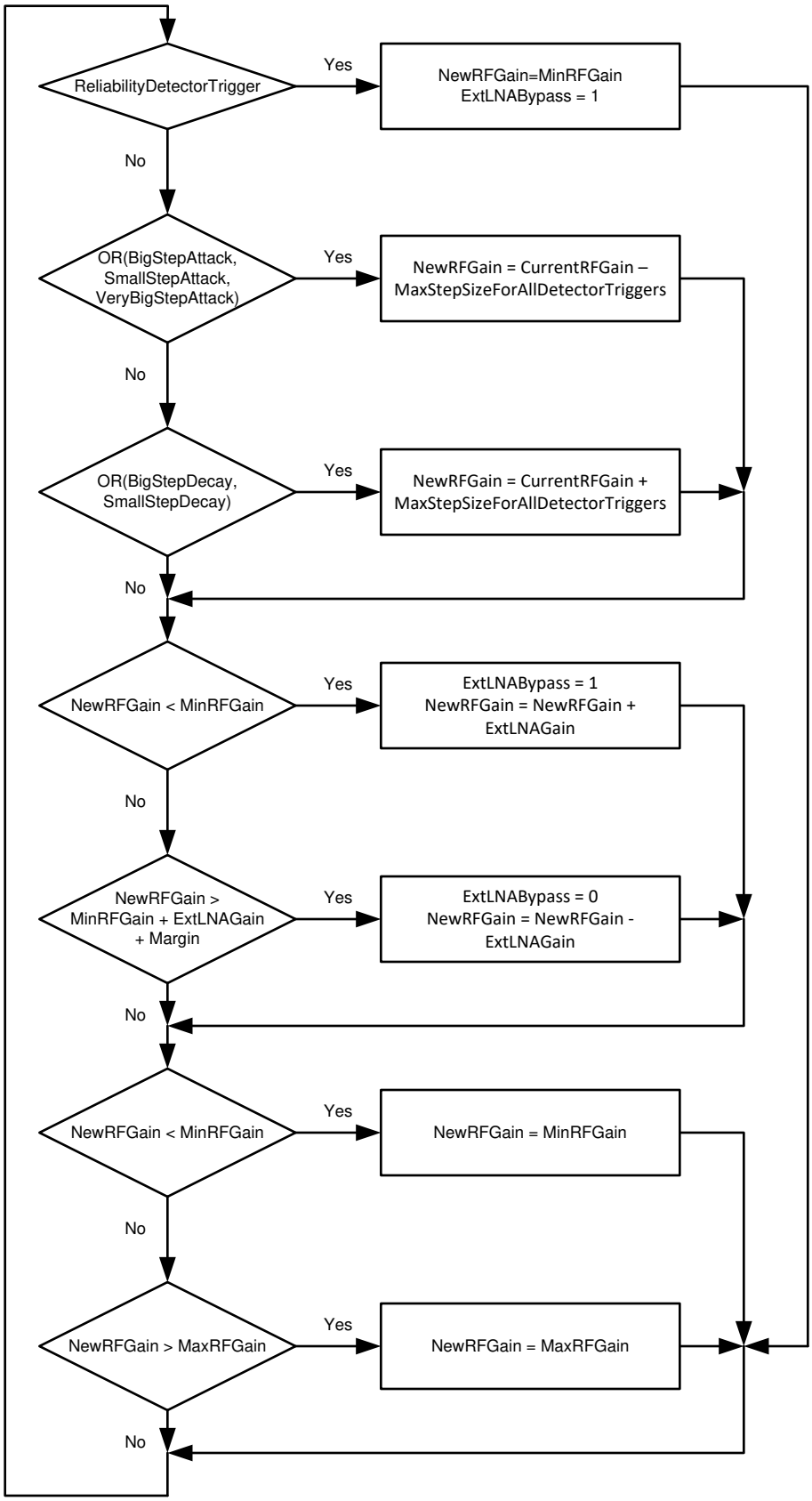


Figure 484. AGC Flow

9.3.2.5.4 Digital Gain Compensation (DGC) for Internal AGC

The AFE79xx has a digital gain compensation (DGC), also know as the automatic level control (ALC) block that provides constant gain from the device input (or LNA input when using the LNA bypass control) to the DGC output when using the internal AGC. As shown in Figure 485, the DGC block also has several methods to increase the range of the output data. In the first mode a floating point format is used to represent the output in 16 bits (Ex: 2 bits exponent, 1 bit sign, 13 bit mantissa). In the second mode, the gain to be applied to the signal is split into coarse and fine gains. The third mode is not to do any gain compensation, represent the data in 15 bits, and use an LSB to encode the 5-bit gain value (in dB) onto an LSB using a specified frame structure. In this case, any change in gain can be communicated only at the next frame (Ex: Frame Length = 20 bits) and cannot be on a sample-by-sample basis.

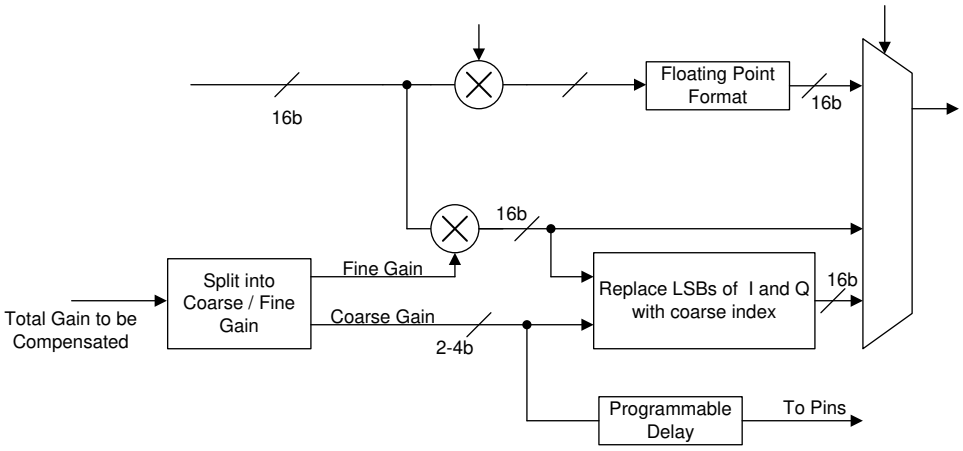


Figure 485. Digital Gain Compensation Modes

9.3.2.5.4.1 Floating Point Format

The device includes a floating point format for the RX output to account for the higher signal range provided when using the RX DSA. TI recommends to use 16-bit resolution, which is only available for JESD formats with 16 or more bits. Using a 12-bit JESD format is possible, but since 2 or 3 bits are used as an exponent, the floating point format with 12-bit JESD output resolution provides only 9 or 10 bits of significant resolution, which will result in a significant degradation in output SNR. The floating point format is defined as follows (similar to IEEE Standard 754-2008):

- S = sign, $S \in \{0, 1\}$
- E = exponent, $0 \le E \le 2^w - 1$, where w = width of the exponent field
- T = significand, $0 \le T \le 2^t - 1$, where t = width of the significant field = 16 – w – 1
- p = t + 1 = precision of the floating point number in bits

Option 1:

- For E = 0, the sample value $v = (-1)^S \times T$ (that is, $ABS(v) < 2^t$)
- For E > 0, sample value $v = (-1)^S \times (2^t + T) \times 2^{(E-1)}$ (that is, $ABS(v) \ge 2^t$).

Option 2:

- For all values of E, sample value = $v = (-1)^S \times T \times 2^E$.

The selection of option 1 or 2 is in register field FLOAT_PT_MODE. Allowed values for the exponent width (w) are 2 or 3, selected in field FLOAT_PT_FORMAT. The 16-bit word is formatted as in Table 3.

By default the gain compensation is justified at the maximum compensation so that the full-scale range is supported at the DGC output. It automatically computes this based on the gain range that must be supported by the DGC. This is indicated by the TOTAL_GAIN_RANGE register in DGC. The justification is rounded off on the higher side to power of 2 (multiples of 6.02 dB).

The conversion to floating point is as follows:

1. First, define Signal = DDC output bits × DGC gain (linear). The DDC output is 16 bits, and DGC = digital gain correction, which applies a gain equal to the total attenuation (DSA + external).

2. For optimum scaling, calculate the max possible value of signal, round up to nearest power of 2 – 1, and justify this to the maximum floating point value. So for example, 25 dB corresponds to 10^(25/20) = 17.78. This is rounded up to 32 linear (30.1 dB). This is a programmable value in the device.
3. Then for each data point, calculate signal and convert to floating point.

The conversion back to linear is straight forward, but needs to take into account the justification. For w = 3, the formula is (–1^float(15)) × float(11:0) × 2^(float(14:12)) × 2^(J-4), where J = 2^ ceiling(gain_range/20/LOG10(2)) is the justification. The value of 4 comes from the difference is the significant resolution and DDC output resolution.

Table 3. Floating Point Format

	MSB															LSB
BIT	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
w = 2	S	E1	E0	T12	T11	T10	T9	T8	T7	T6	T5	T4	T3	T2	T1	T0
w = 3	S	E2	E1	E0	T11	T10	T9	T8	T7	T6	T5	T4	T3	T2	T1	T0

9.3.2.5.4.2 Coarse/Fine Gain Mode

Another DGC Mode is the Coarse/Fine Gain Mode. The gain to be imparted to the signal is split into coarse and fine gains. Coarse step can be 2, 3, 4, 6, or 8 dB. The number of coarse bits is 2, 3, or 4. Fine gain is imparted to the data whereas the coarse index is encoded either through the LSBs of the data or through output GPIO pins. An offset for the fine gain in the range of 0 to 5 dB in 1-dB steps can be programmed, and TI recommends to set the offset to mod(6–(CoarseStep–1),6).

9.3.2.5.4.2.1 Coarse Gain Over LSB Encoding

If it is encoded through LSBs of the data, either the LSBs of both I and Q are used to encode the coarse gain, or the coarse gain is encoded completely in both I and Q. For example, if the coarse index is 2 bits either 1 LSB from I and Q are used or alternatively 2 LSBs of both I and Q are used for encoding the coarse gain on both I and Q. Similarly, a coarse index of 4 bits uses 2 LSBs of I and Q. TI recommends that this mode is used only with 16-bit or higher JESD formatting to prevent significant SNR loss due to a higher quantization noise with lower resolution. The modes supported are tabulated below in Table 4.

Table 4. Modes to Encode Coarse Index on LSBs of I and Q

MODE #	DESCRIPTION
1	2-bit Coarse Index, 1 LSB of I and Q
2	3-bit Coarse Index, 2 LSB of I and Q
3	4-bit Coarse Index, 2 LSBs of I and Q
4	2-bit Coarse Index, 2 LSBs of I(and repeated on Q)
5	3-bit Coarse Index, 3 LSBs of I(and repeated on Q)

When the Coarse Index is transmitted over I and Q, the LSBs of the coarse index are transmitted on I and the MSBs on Q by default. The I and Q LSBs can be swapped or inverted in order.

9.3.2.5.4.2.2 Coarse/Fine Gain Mode With Coarse Index Sent Over Pins

In this mode, the coarse index is sent over pins and hence all 16 bits can be used for data. A maximum of 3 pins are supported. For a 3-pin example, the mapping can be changed from [0 7] to [7 0] , which is the equivalent to doing a subtraction from 7.

The output through the pins can be delayed to better match the latency of the fine data through the JESD204B/C interface. The delay is a 12-bit number in units of f_{ADC}/8 clock cycles.

9.3.2.6 RX Chain Digital Block

The output of the RX ADC goes to the DDC blocks, consisting of a complex mixer followed by decimation block to reduce the sample rate of the output data. The output of the DDC goes to an digital gain compensation (DGC) block to optionally maintain a constant gain from RX analog input to digital output.

9.3.2.6.1 RX Digital Mux

The AFE79xx supports a mode where the output data of one ADC can be routed internally to the digital blocks of both DDC blocks in each 2 RX on the same side of the device (channels 1RX and 2RX are a group and channels 3RX and 4RX are a group). The unused ADC channel can be powered down. This allows up to 4 DDCs (or 2 DDCs in the wider bandwidth modes) to be used for two ADCs.

9.3.2.6.2 RX Delay Block

A programmable delay can be configured in integer multiples of the ADC clock period up to 31 clocks through 5 register bits. There may be an offset in delay between the 0 delay setting when enabled and when the delay is disabled.

9.3.2.6.3 RX Digital Mixers and NCOs

The digital mixer includes two NCOs, whose frequency can be set independently. The mixers can switch between two NCOs, each able to maintain the NCO phase at all times. The switch between the two NCOs can be controlled through the SPI or dedicated GPIO pin. The NCOs have two options for setting the frequency. First, they can have a 32-bit resolution with the frequency specified as the N × sample rate × $1/2^{32}$. Optionally, the NCOs can provide an exact 1-kHz raster for an input reference clock frequency of N × 61.44 MHz, where N is an integer. The NCOs and mixer provide a SFDR of 100 dB.

9.3.2.6.4 RX Decimation Block

The RX decimation block decimates the ADC data to the output sample rate. The decimation block is highly flexible, matching the interface rates to the possible ADC sample rates. Boxes with a number are valid modes, boxes without a number are not valid modes. The rates are listed in Table 5. The non-grey boxes have 2 DDCs for the AFE7920/88, while the grey boxes have 1 DDC only.

Table 5. RX Decimation Rates

		ADC SAMPLE RATE (MSPS)					
		1228.8	1474.56	1966.08	2211.84	2457.6	2949.12
Output Rate (MSPS)	61.44	20	24	32		40	48
	92.16		16		24		32
	122.88	10	12	16		20	24
	184.32		8		12		16
	245.76	5	6	8		10	12
	368.64		4		6		8
	491.52			4		5	6
	737.28						4

The digital decimation filters provide over 85 dB (90 dB for the final 2x decimation) of image rejection of the in-band signal. Passband is defined as 81.4% of the baseband sample rate and in-band peak-to-peak ripple is less than 0.2 dB. The decimation filter responses for decimation from 2949.12 MSPS are shown in through Figure 506.

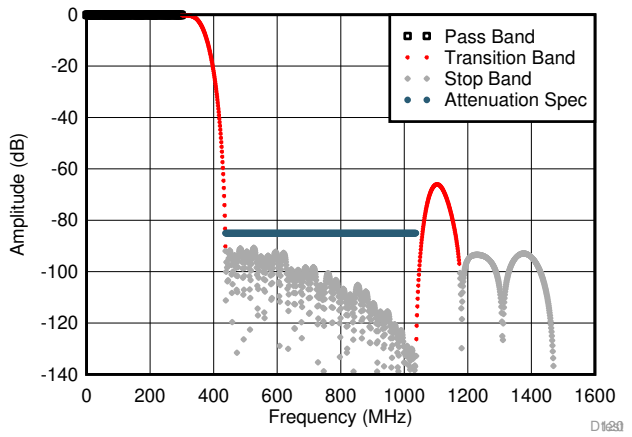


Figure 486. RX Filter Response for Decimation by 4 (Nyquist)

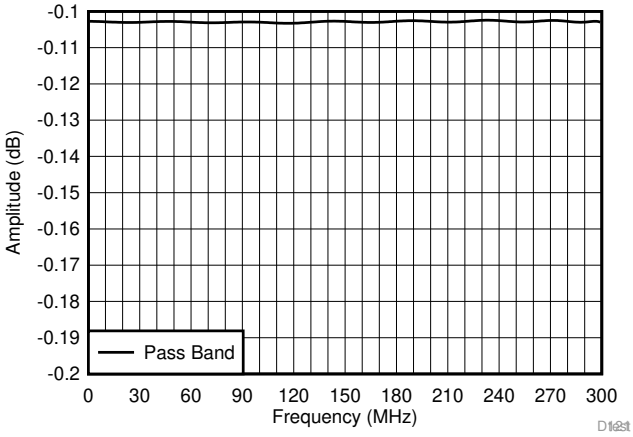


Figure 487. RX Filter Response for Decimation by 4 (Passband)

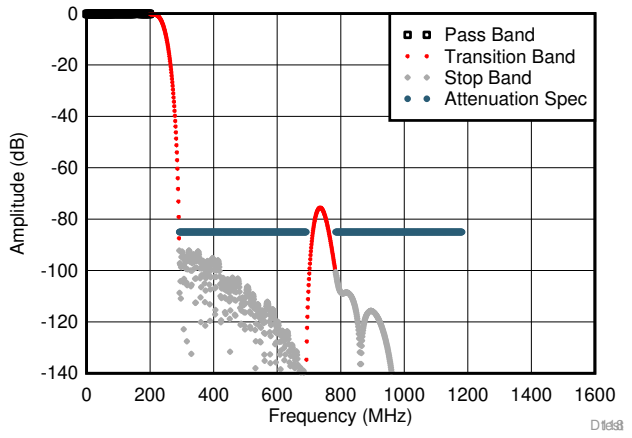


Figure 488. RX Filter Response for Decimation by 6 (Nyquist)

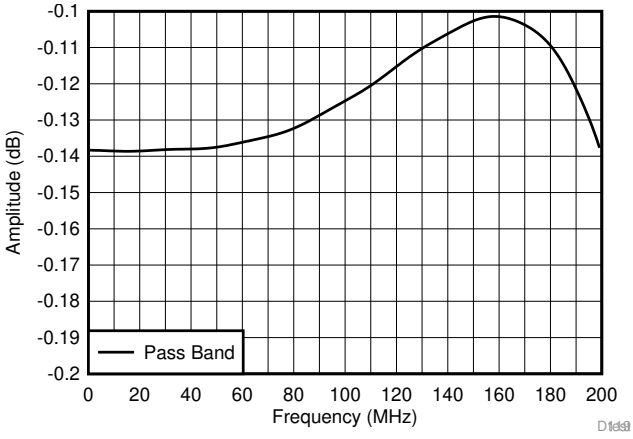


Figure 489. RX Filter Response for Decimation by 6 (Passband)

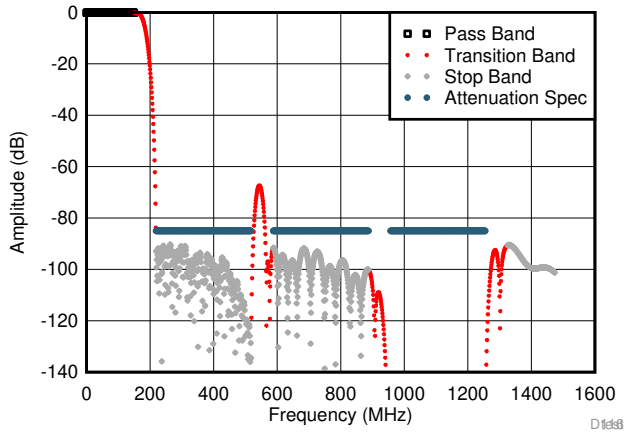


Figure 490. RX Filter Response for Decimation by 8 (Nyquist)

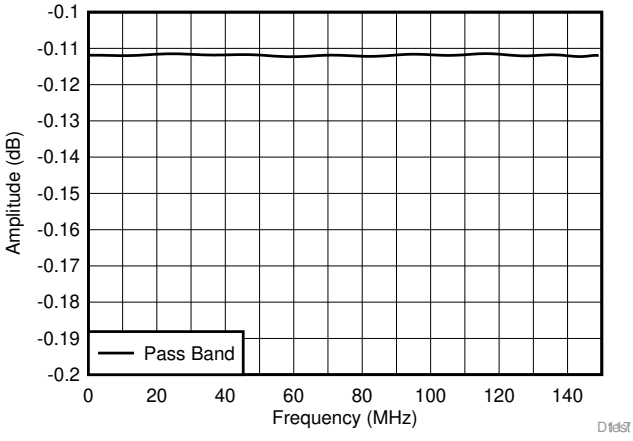


Figure 491. RX Filter Response for Decimation by 8 (Passband)

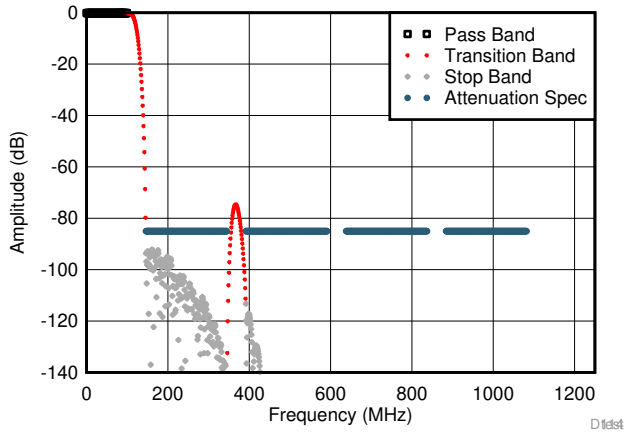


Figure 492. RX Filter Response for Decimation by 10 (Nyquist)

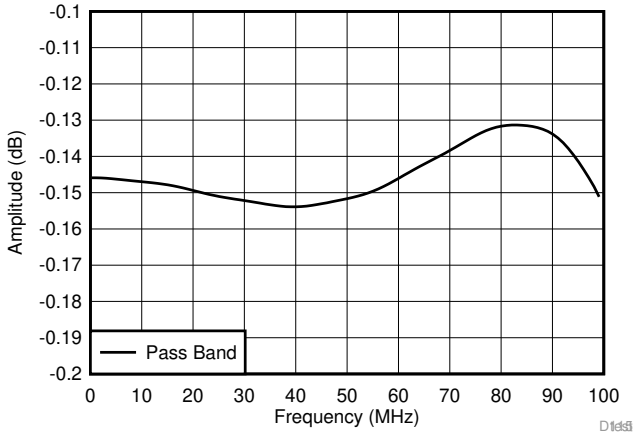


Figure 493. RX Filter Response for Decimation by 10 (Passband)

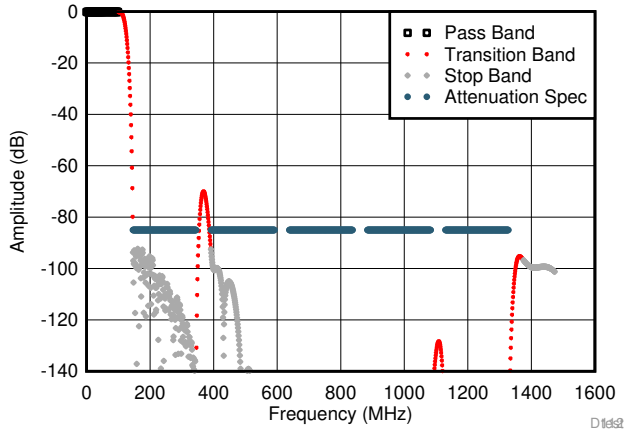


Figure 494. RX Filter Response for Decimation by 12 (Nyquist)

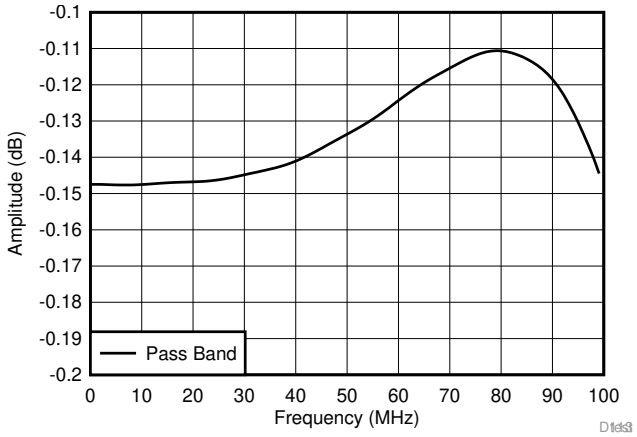


Figure 495. RX Filter Response for Decimation by 12 (Passband)

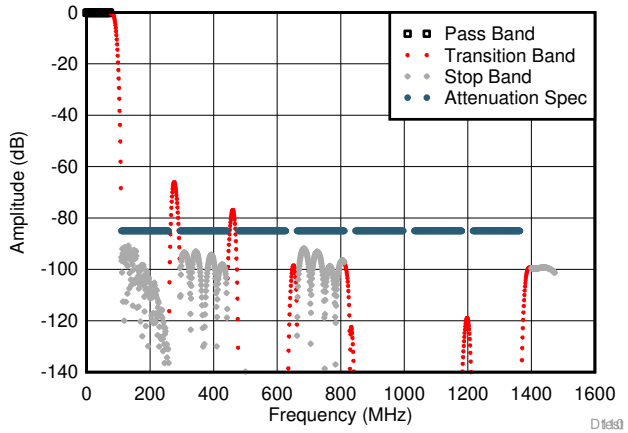


Figure 496. RX Filter Response for Decimation by 16 (Nyquist)

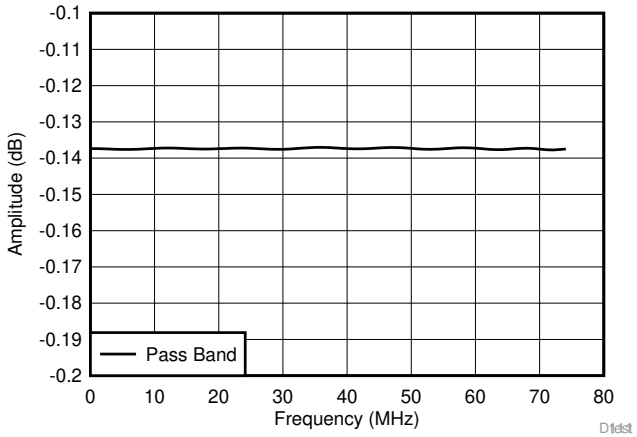


Figure 497. RX Filter Response for Decimation by 16 (Passband)

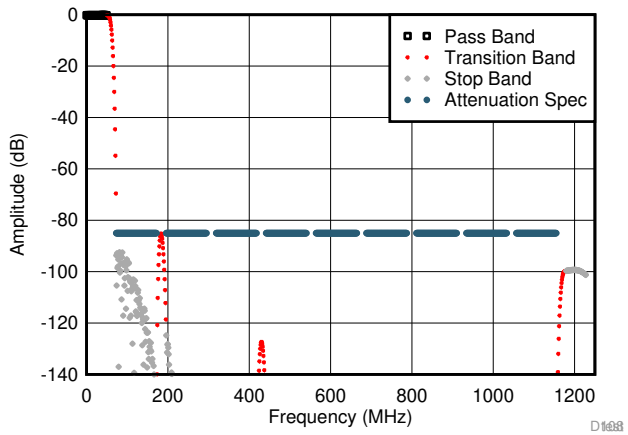


Figure 498. RX Filter Response for Decimation by 20 (Nyquist)

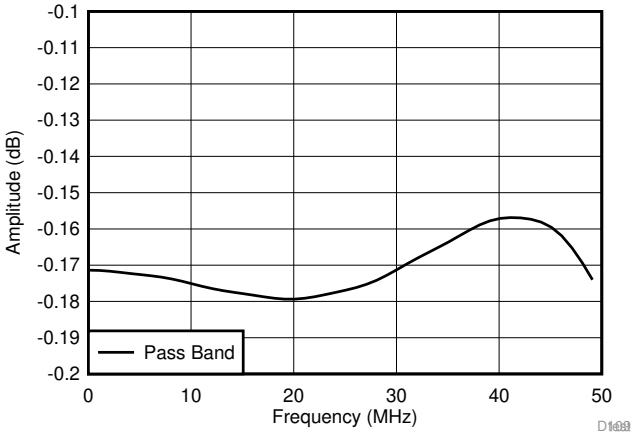


Figure 499. RX Filter Response for Decimation by 20 (Passband)

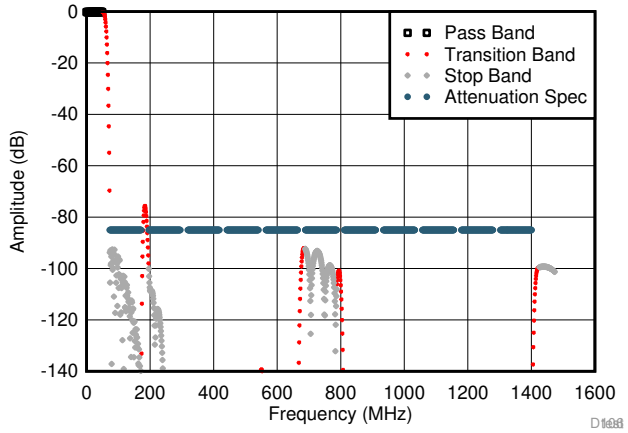


Figure 500. RX Filter Response for Decimation by 24 (Nyquist)

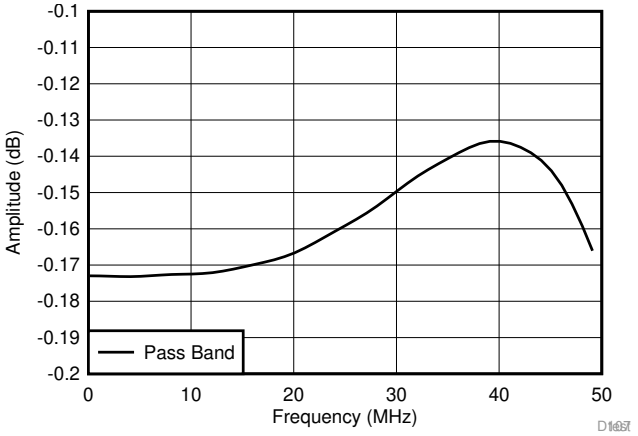


Figure 501. RX Filter Response for Decimation by 24 (Passband)

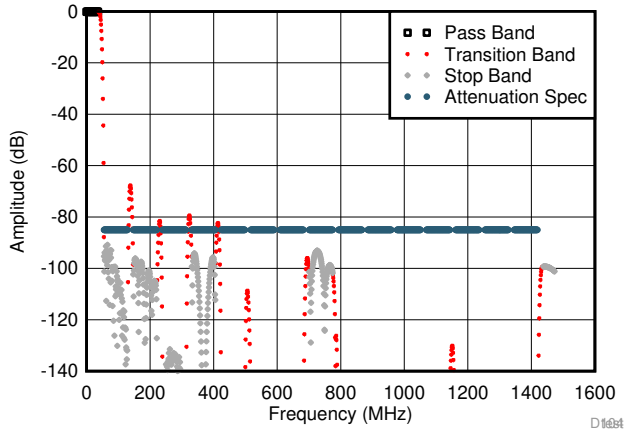


Figure 502. RX Filter Response for Decimation by 32 (Nyquist)

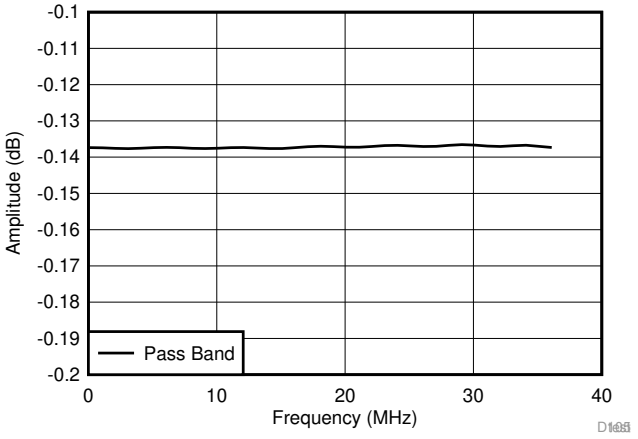


Figure 503. RX Filter Response for Decimation by 32 (Passband)

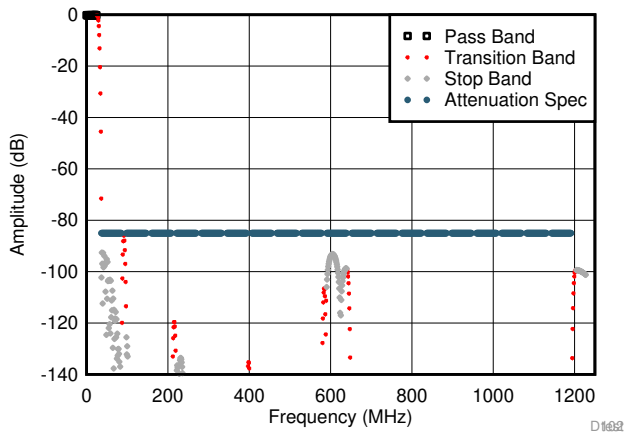


Figure 504. RX Filter Response for Decimation by 40 (Nyquist)

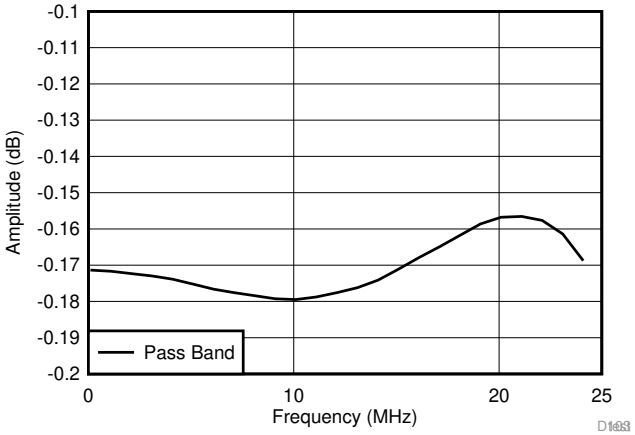


Figure 505. RX Filter Response for Decimation by 40 (Passband)

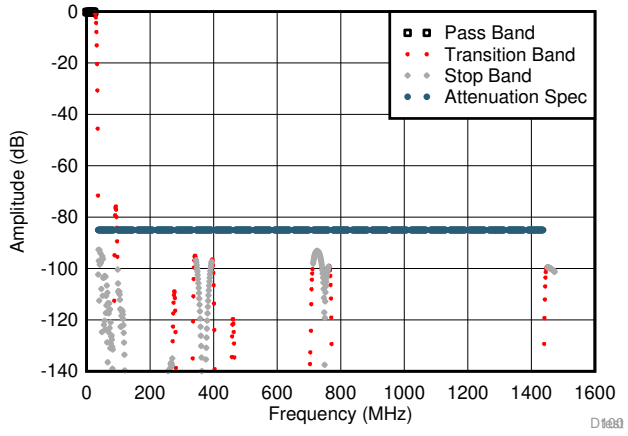


Figure 506. RX Filter Response for Decimation by 48 (Nyquist)

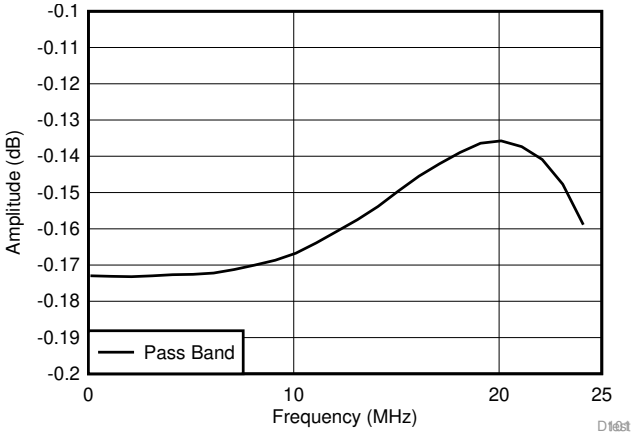


Figure 507. RX Filter Response for Decimation by 48 (Passband)

9.3.3 Transmitter (TX) Chain

The AFE79xx integrates 4 transmitters based on RF sampling DACs. The TX chain block diagram is shown in Figure 508 with a single DUC and in Figure 509 with dual DUCs. (AFE7920 and AFE7988 only). The DAC output operates up to 12 GSPS and is followed by a wideband RF amplifier (TX DSA). The digital section of the TX includes dual DUCs (AFE7920 and AFE7988 only) or single DUC to increase the input sample rate to the DAC sample rate. The digital block also include gain control and a PA protection block.

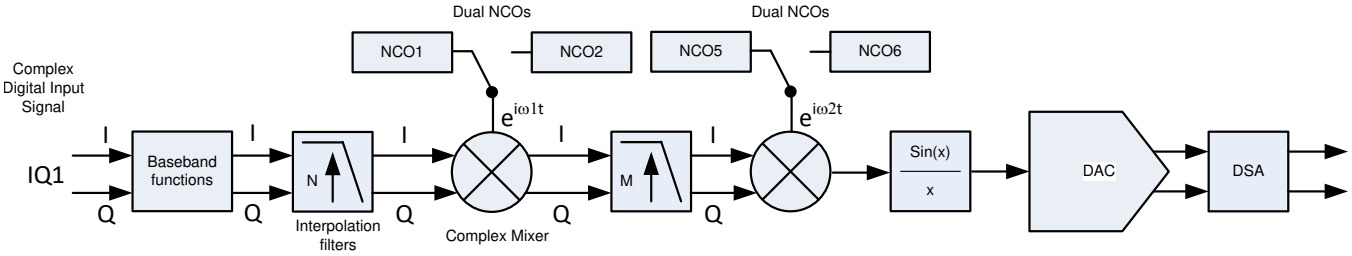


Figure 508. TX Chain Block Diagram With Single DUC

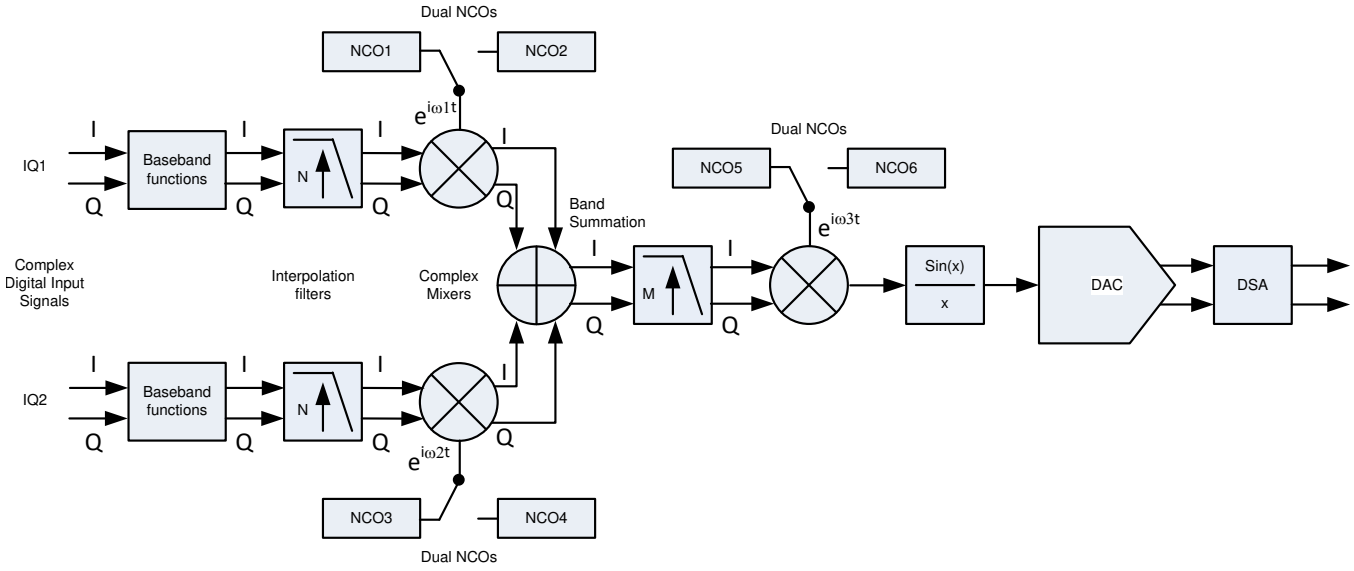


Figure 509. TX Chain Block Diagram With Dual DUCs

9.3.3.1 TX Chain Digital Block

The input to the TX chain is one or two complex signals from the JESD block. At the input sample rate are baseband functions and a signal measurement circuit for the PA protection block. This is followed by the digital upconverter and the Sin(x)/x filter.

9.3.3.1.1 Baseband Processing Functions

The baseband processor provides the following functions:

- Digital Gain
- TX DSA Gain and Phase Correction
- TX Frequency Response Correction
- TX Power Meter

9.3.3.1.1.1 Digital Gain

The digital gain block has a range of 13 dB in steps of 0.125 dB (a setting of 0 corresponds to maximum gain). A value of 52 corresponds to a full scale input signal being fullscale at the DAC, accounting for headroom for DSA calibration and Sin(x)/x compensation. When combined with an analog (DSA) gain change, the analog setting should be written first and then the digital gain setting so both will be simultaneously updated without a glitch.

The digital gain can also be programmed separately through a different register.

9.3.3.1.1.2 TX DSA Gain and Phase Correction

The TX DSA gain and phase correction block is used to reduce the offset in gain and phase for each DSA setting. This is expected to be calibrated in the customer factory or at start-up through the DSA calibration macro.

9.3.3.1.1.3 TX Frequency Response Correction

The TX has a correction filter that can provide a gain slope as a function of frequency to correct the DAC output frequency response across the band.

9.3.3.1.1.4 TX Power Meter

There are RMS power meters at each of the IQ input streams. The power meter measures the RMS power in a programmable window of samples 2^n samples, with n = [5,16]. The power meter is accurate to 0.3 dB for signal levels between 0 and –40 dBFS. The power meter is read through the SPI interface.

9.3.3.1.2 TX PA Protection

The AFE79xx incorporates an optional power amplifier protection (PAP) block to monitor when the input signal is too large (like when an interface error occurs and reduces the digital signal power for the DAC, for example).

The PAP block achieves the functionality of reducing the input signal that crosses the threshold through three main sub-blocks. These are PAP detectors, a PAP gain state machine, and a PAP gain module. The locations of the PAP blocks in the TX digital signal chain are shown in Figure 510 and Figure 511. One PAP state machine is dedicated for each TX1, TX2, TX3, and TX4 chains.

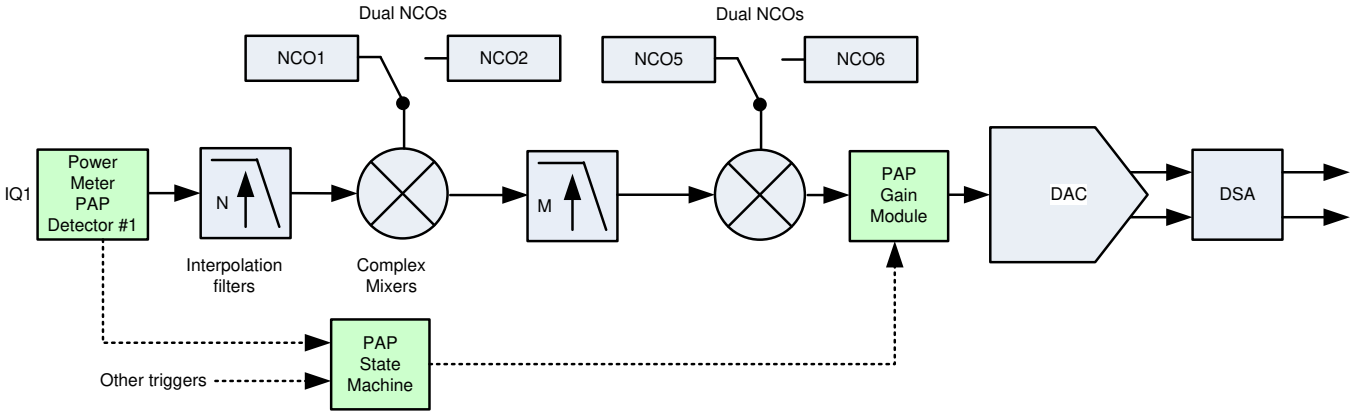


Figure 510. PAP Blocks in the TX Signal Chain of AFE7921/AFE7989

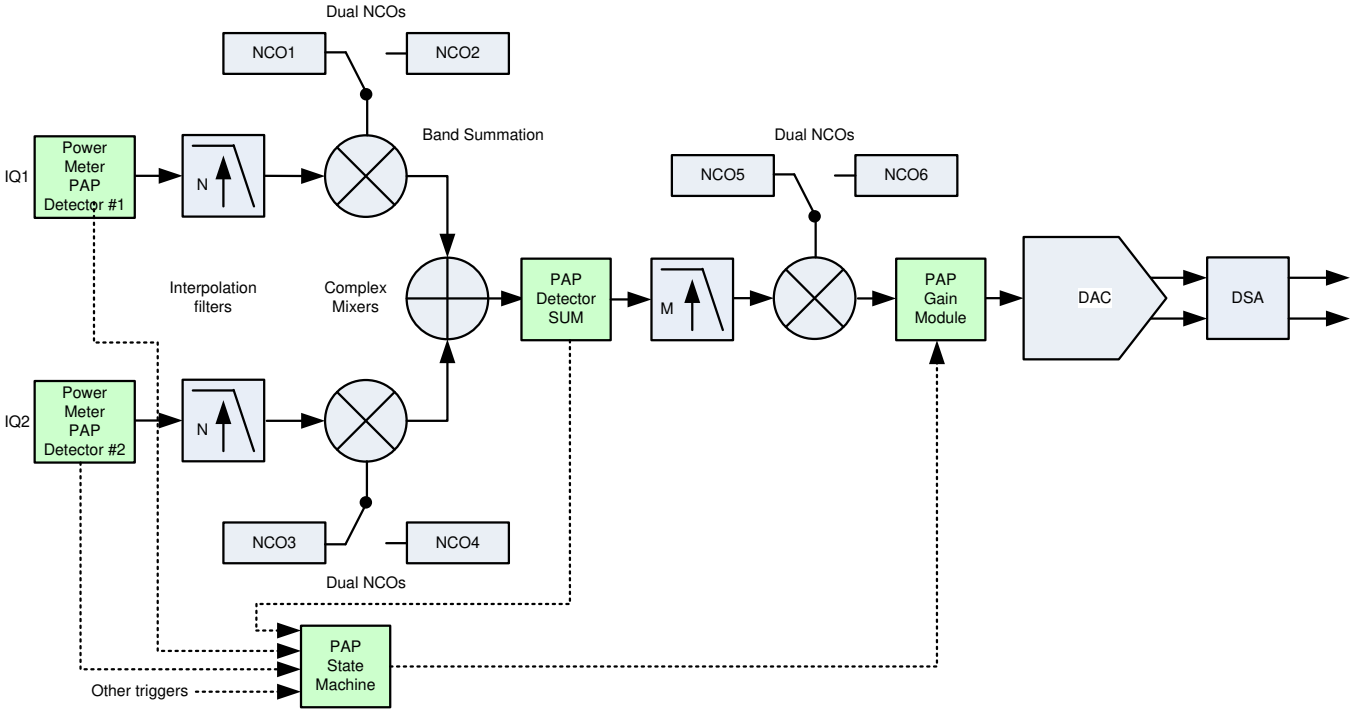


Figure 511. PAP Blocks in the TX Signal Chain of AFE7920/AFE7988

9.3.3.1.2.1 PAP Triggers

The PAP protection state machine can be triggered by alarms from the SerDes and JESD blocks, PLLs, power measurements on the TX signal, PAP triggers from other TX chains, TX over range signal, or a SPI register (see Figure 512). Each trigger can be enabled separately.

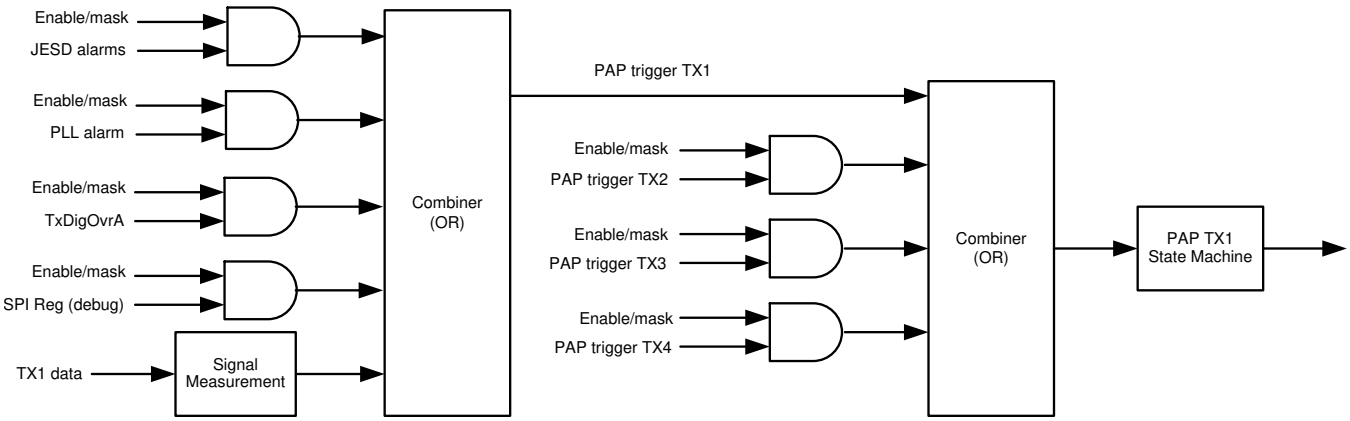


Figure 512. PAP Triggers for TX1

9.3.3.1.2.1.1 SerDes and JESD Triggers

The SerDes and JESD blocks have four different type of alarms, of which some are per lane and some others are common for all the lanes:

- FIFO errors – 1 per lane.
- Loss of Signal (LOS) errors – 1 per lane.
- Link errors – 1 per lane.
- SerDes PLL unlock error – common for all lanes.

Based on the JESD LMFS configuration, an error on a lane will require the corresponding TX chains to be shut down. For example, if 8 lanes are supporting 4 IQ TX chains, then even if only lane 1 (for TX1_I) has an error, both lane 1 and 2 (TX1_I and TX2_Q) will need alarms. So depending on the LMFS configuration, the JESD alarm to TX1 needs to be configured for example as:

- Lane1 error OR Lane2 error OR SerDes PLL error = TX1 JESD alarm
- Lane3 error OR Lane4 error OR SerDes PLL error = TX2 JESD alarm
- Lane5 error OR Lane6 error OR SerDes PLL error M TX3 JESD alarm
- Lane7 error OR Lane8 error OR SerDes PLL error M TX4 JESD alarm

Lane 1 error itself is the OR of all the per lane errors like FIFO error, LOS error and Link error. If 4 lanes support 4 IQ TX chains, then

- Lane1 error OR SerDes PLL error = TX1 JESD alarm
- Lane2 error OR SerDes PLL error = TX2 JESD alarm
- Lane3 error OR SerDes PLL error = TX3 JESD alarm
- Lane4 error OR SerDes PLL error = TX4 JESD alarm.

9.3.3.1.2.2 PLL Alarm Trigger

The unlock alarm from the device clock PLL is available to trigger the PAP state machine.

9.3.3.1.2.3 Average Power Trigger

The average power-based protection is based on power measurement in a moving window, and the module is dedicated for each TX chain. The window length is programmable to 32, 64, 96, or 128 samples. The average power measurement computes the envelop of the signal by taking abs of the complex signal I + jQ followed by average power measurement as shown in Figure 513.

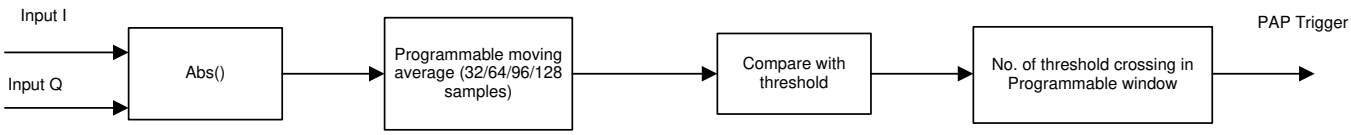


Figure 513. Average Power Based PA Protection on Abs of the Input Signal

The programmable window length and the threshold are both programmable in the range 1 to $2^{12} – 1$.

9.3.3.1.2.4 High Pass Filter Trigger

The high pass filter (HPF) based PA protection trigger provides another option in determining abnormal signals in the TX chain. The HPF taps are [–1 1 6 –6 –1 1]/16 and the frequency response across the Nyquist zone is shown in Figure 514.

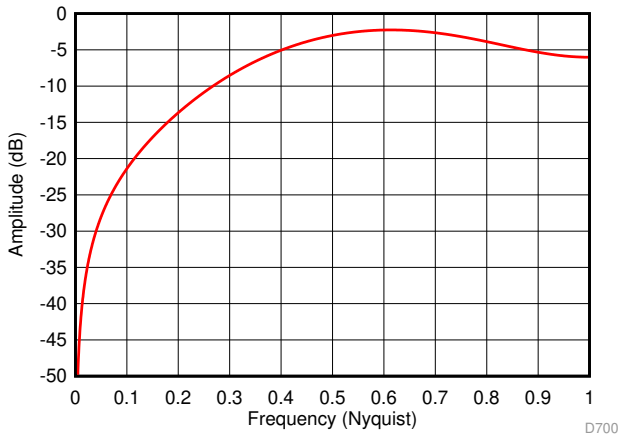


Figure 514. HPF Frequency Response

This HPF trigger has one detection mode:

- High pass filter on abs(I+jQ) and output is used to determine threshold crossing.

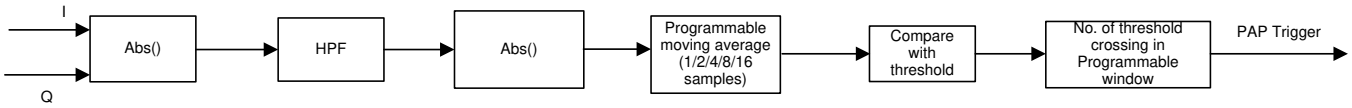


Figure 515. Programmable Filter Detector – Mode 3

The moving average power is compared with a threshold and the number of crossings in a programmable time window is computed. The time window is programmable from $1 – 2^4$ samples. If the number of crossings is higher than a threshold number of crossing then the PAP is triggered. The programmable window of length: $1 – 2^{12} – 1$ samples and the threshold is also 1 to $2^{12} – 1$.

9.3.3.1.2.5 PAP Gain State Machine

In a trigger event, the digital signal is scaled down before the DAC so that the abnormal samples do not reach the PA. The ramp down signal is multiplied to signal data path at the output of the interpolation filter. The PAP state machine is shown in Figure 516:

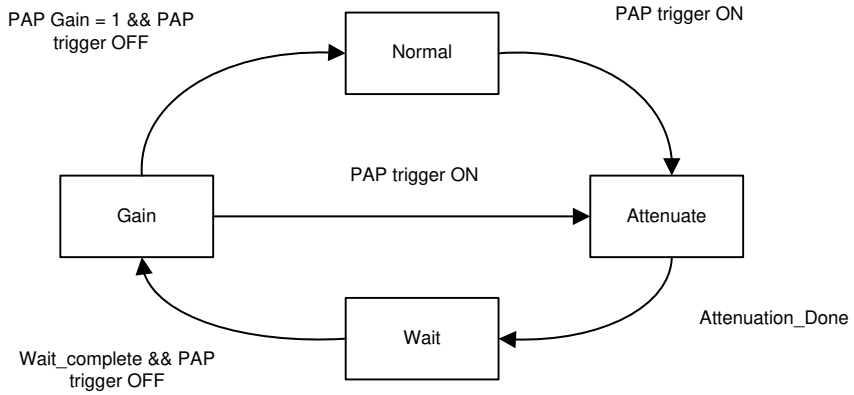


Figure 516. PAP State Machine

Once the PAP trigger ON is generated, the state machine moves to “Attenuate” state, where the attenuation of the signal is started. In the “Attenuate” state, the ramp down of the signal is done in one of two programmable modes:

- Linear ramp down: The start gain, gain step and time duration in a particular gain step for ramp down are all programmable.
- Cosine Ramp down: Attenuation of the form $(1 + \cos\theta)/2$ with θ going from 0 to π. The starting phase and time duration in a particular phase value are all programmable.

In addition to the ramp down, there are three programmable modes in the datapath:

- Regular Operation of Datapath: The signal datapath is working in the normal mode and is multiplied by the ramp down signal. In this mode, the PA protection is achieved by ramp down as even the offending sample with attenuation is passed to the PA.
- Holding the last good sample: The signal datapath holds the sample value at the interpolator filter the time instant at which the PA protection trigger occurs. The offending sample does not pass through the data chain. The PA protection trigger to the PAP state machine can be delayed to ensure the last good sample before the offending sample is held. The held datapath output is then multiplied by the ramp down. Once the ramp down signal reaches the end gain (or phase value) a Done signal is generated by the ramp down module. This Done signal is used to remove the holding of the samples. After the Done signal, the regular datapath operation begins though the output of the datapath is multiplied by the ramp down signal.
- Programmable Value to datapath: Instead of holding the last good sample, a programmable value in I and Q is forced into the datapath once the PAP state machine is triggered. The forcing of the programmable value to the datapath is removed once the Done signal is generated by the ramp down module. After the Done signal, the regular datapath operation begins though the output of the datapath is multiplied by the ramp down signal.

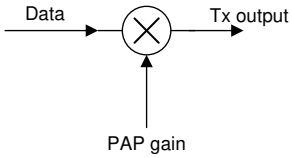


Figure 517. Multiplication of Signal Datapath to Ramp Down Signal

After attenuation is done, the PAP state machine moves into the Wait state, before checking the status of the PAP trigger. A programmable 16-bit counter is used in the Wait state.

After the wait time ends, the state machine moves to gain state only if the PAP trigger is OFF. If the PAP trigger is ON then the state machine continues to remain in Wait state. If the PAP trigger becomes OFF then the state machine moves to Gain state. The signal measurement PAP triggers (Average Power and Programmable Filter Triggers) continuously monitor the incoming signal and become OFF when the measurements does not exceed the threshold anymore. All other PAP triggers require the intervention of the Host to perform the necessary steps to remove the source of the error and then clear the Triggers.

Once again in the Gain state, the signal is multiplied by the ramp-up signal. The ramp-up is generated by the two modes:

- Linear ramp-up: Programmable ramp-up end and step. The end, step and time duration for the ramp-up are all different from the ramp-down values.
- Cosine ramp-up: the end phase and phase step are programmable and different from the cosine ramp down values.

If a PAP ON trigger occurs during the Gain state ramp-up then the state machine moves to Attenuate state. The starting gain in the Attenuate state is equal to the value at which the Gain state stopped.

9.3.3.2 Interpolation Block

The TX interpolation block interpolates the input data to the DAC sample rate and up converts the signals to the chosen frequencies. The interpolation block is highly flexible, matching the interface rates to the possible DAC sample rates. The rates are listed in the tables below. Boxes with a number are valid modes, boxes without a number are not valid modes. The non-grey boxes have 2 DUCs for the AFE7920 and AFE7988, while the grey boxes have 1 DDC only. The digital up-conversion is implemented with a two-stage architecture: front stage (interpolate by N) and back stage (interpolate by M). The front mixer stage sets the I/Q streams to the desired frequency spacing, after which the I/Q streams are summed together in the band summation block. The interpolation FIRs are also split into the front-FIR stage and back-FIR stage.

The input data rate to the front stage interpolation block is also listed in Table 6. The resulted multi-band signal is further interpolated and up-converted to the desired output RF frequency.

Table 6. Interpolation Factors Between Input and DAC Sample Rates

		DAC SAMPLE RATE (MSPS)							
		4423.68	**4915.20**	**5898.24**	**7372.80**	**7864.32**	**8847.36**	**9830.40**	**11796.48**
Input Rate (MSPS)	**122.88**	36	40	48	60	64	72	80	96
	184.32	24		32	40		48		64
	245.76	18	20	24	30	32	36	40	48
	368.64	12		16	20		24		32
	491.52	9	10	12	15	16	18	20	24
	737.28	6		8	10		12		16
	983.04	4.5		6	7.5	8	9	10	12
	1474.56	3		4			6		8
Dual DUC Combining Rates (MSPS)	**Half Rate**	1105.92	1228.8	1474.56	1228.8	983.04	1474.56	1228.8	1474.56
	Full Rate	2211.84	2457.6	2949.12	2457.6	1966.08	2949.12	2457.6	2949.12
M (2nd Stage) Interpolation	**Half Rate**	4	4	4	6	8	6	8	8
	Full Rate	2	2	2	3	4	3	4	4

9.3.3.3 Front Stage Interpolation Block

The front stage digital interpolation filters provide over 90 dB of image rejection of the in-band signal. Passband is defined as 80% of the baseband sample rate and in-band peak-to-peak ripple is for common interpolation factors below 0.1 dB, and in always better than 0.2 dB.

For signals with lower amplitudes at the edge of the passband (like with digital pre-distortion, for example), the bandwidth can also be extended.

The front stage interpolation filter responses are shown in Figure 518 through Figure 535. Interpolation by 2, 3, 4, 6, 8, and 12 are shown for half rate DUC combining mode at 1474.56 MSPS. The same responses for interpolation by 4, 6, 8, and 12 are valid for full rate DUC combining mode at 2949.12 MSPS by multiplying the x-axis by 2. Interpolation by 5, 10 are shown for half rate DUC combining mode at 1228.8 MSPS. The same responses are valid for full rate DUC combining mode at 2457.6 MSPS by simply multiplying the x-axis by 2. Interpolation by 20 is shown for the full rate DUC combining mode at 2457.6 MSPS as this is the only valid mode.

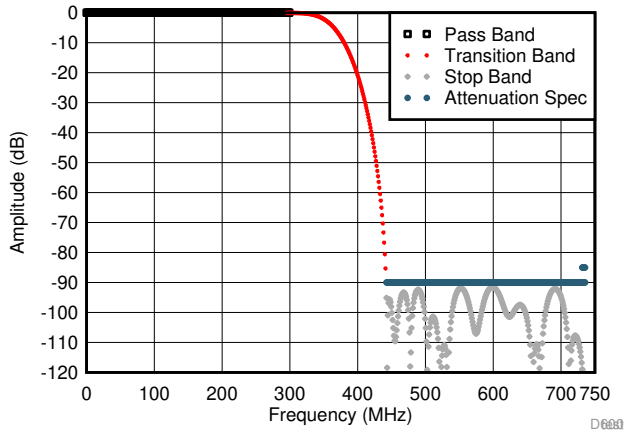


Figure 518. TX Front Stage Filter Response for Interpolate by 2 (Nyquist)

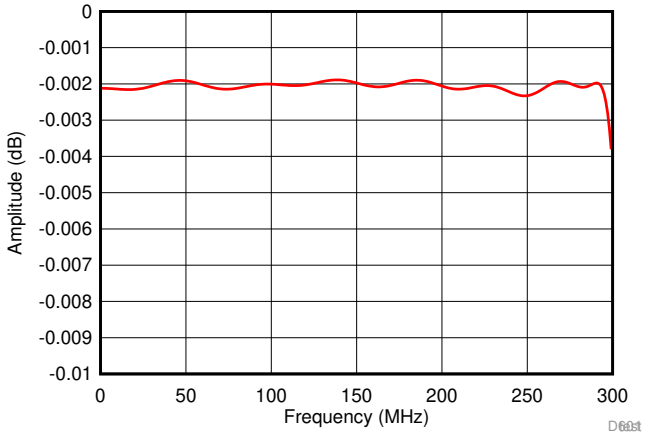


Figure 519. TX Front Stage Filter Response for Interpolate by 2 (Passband)

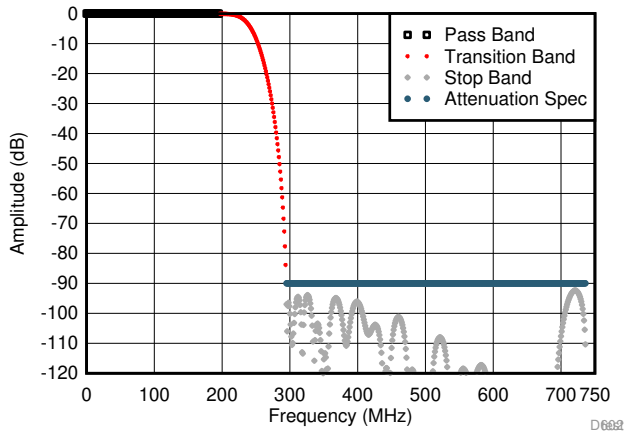


Figure 520. TX Front Stage Filter Response for Interpolate by 3 (Nyquist)

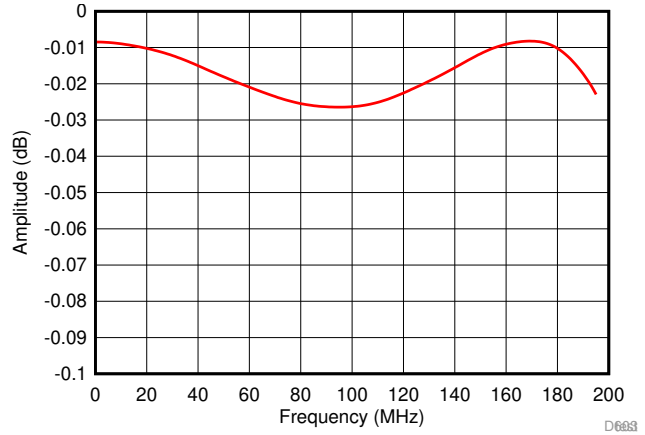


Figure 521. TX Front Stage Filter Response for Interpolate by 3 (Passband)

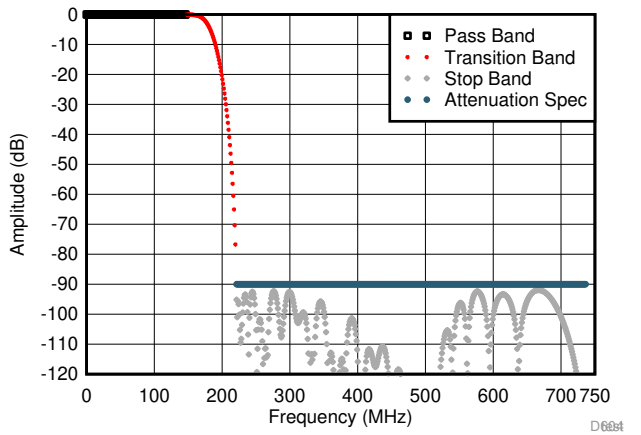


Figure 522. TX Front Stage Filter Response for Interpolate by 4 (Nyquist)

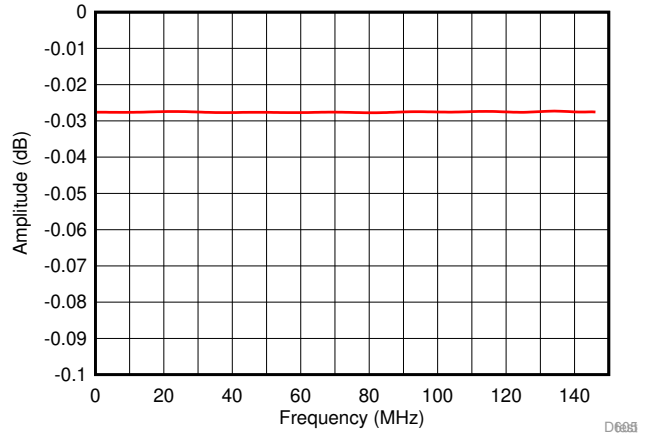


Figure 523. TX Front Stage Filter Response for Interpolate by 4 (Passband)

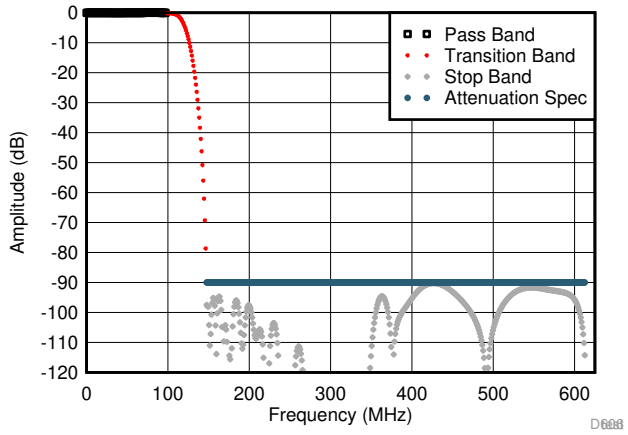


Figure 524. TX Front Stage Filter Response for Interpolate by 5 (Nyquist)

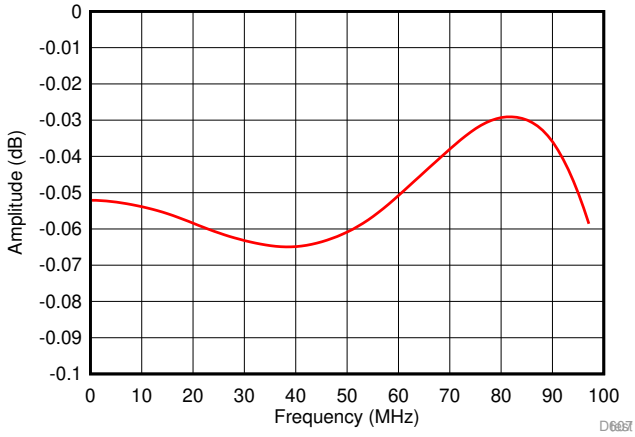


Figure 525. TX Front Stage Filter Response for Interpolate by 5 (Passband)

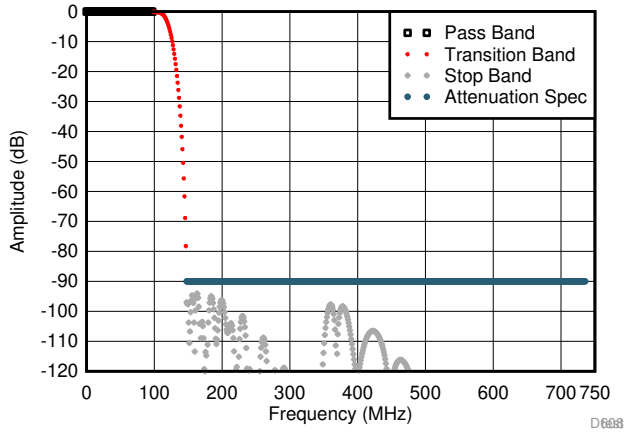


Figure 526. TX Front Stage Filter Response for Interpolate by 6 (Nyquist)

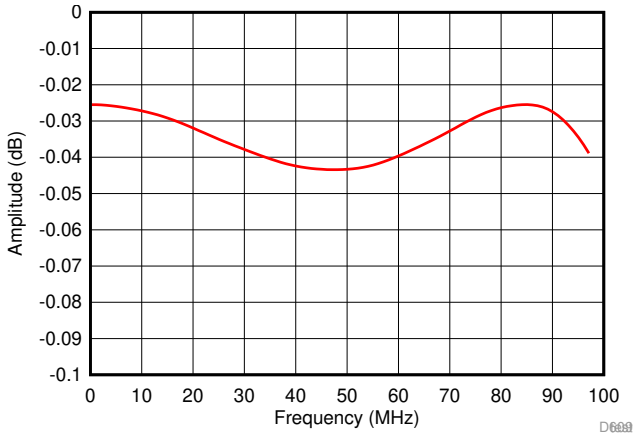


Figure 527. TX Front Stage Filter Response for Interpolate by 6 (Passband)

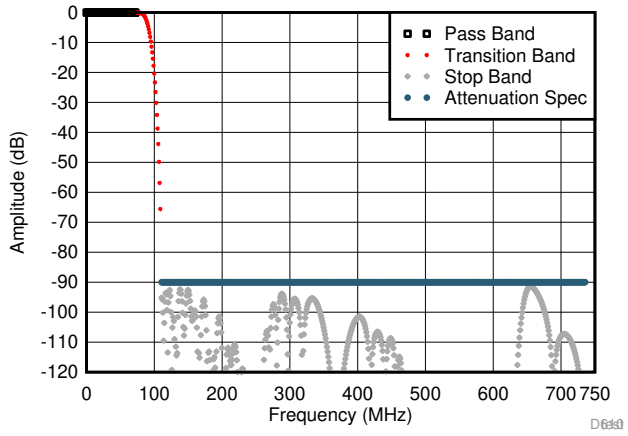


Figure 528. TX Front Stage Filter Response for Interpolate by 8 (Nyquist)

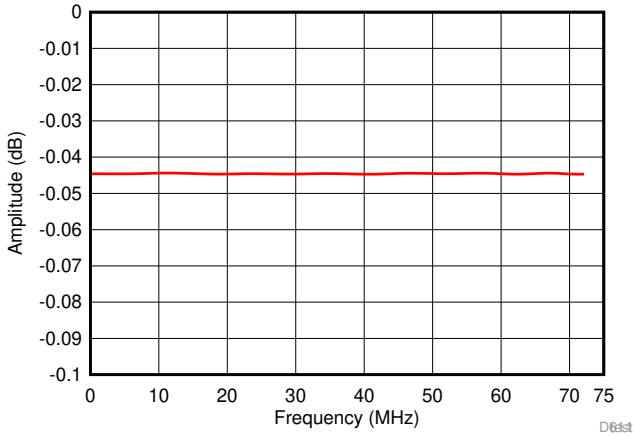


Figure 529. TX Front Stage Filter Response for Interpolate by 8 (Passband)

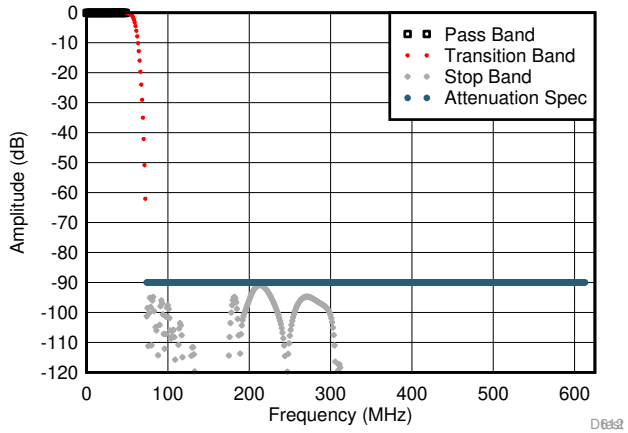


Figure 530. TX Front Stage Filter Response for Interpolate by 10 (Nyquist)

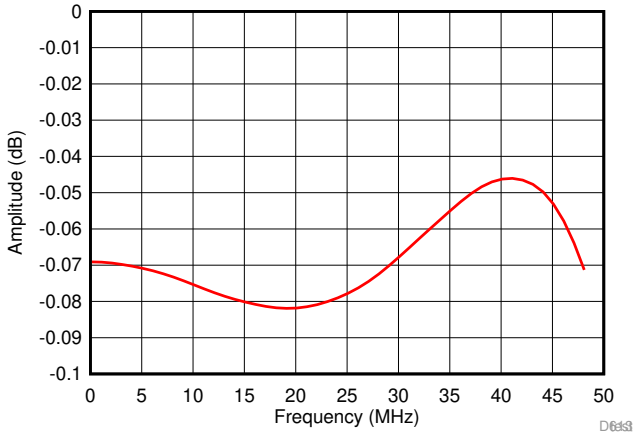


Figure 531. TX Front Stage Filter Response for Interpolate by 10 (Passband)

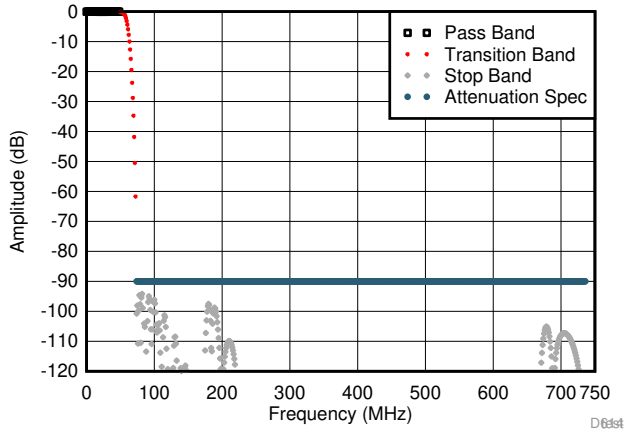


Figure 532. TX Front Stage Filter Response for Interpolate by 12 (Nyquist)

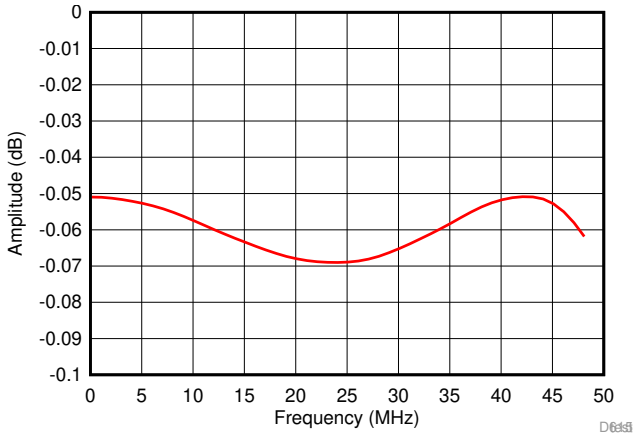


Figure 533. TX Front Stage Filter Response for Interpolate by 12 (Passband)

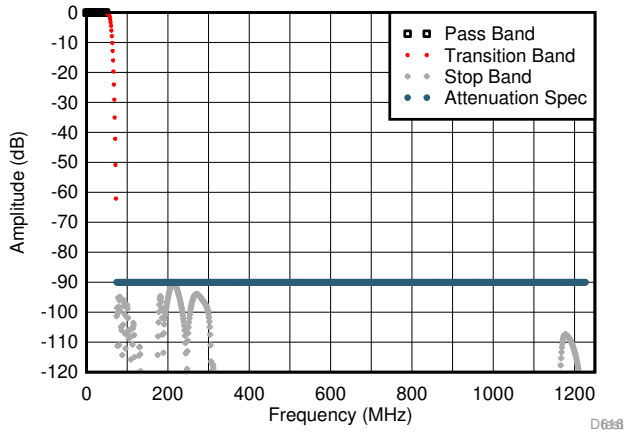


Figure 534. TX Front Stage Filter Response for Interpolate by 20 (Nyquist)

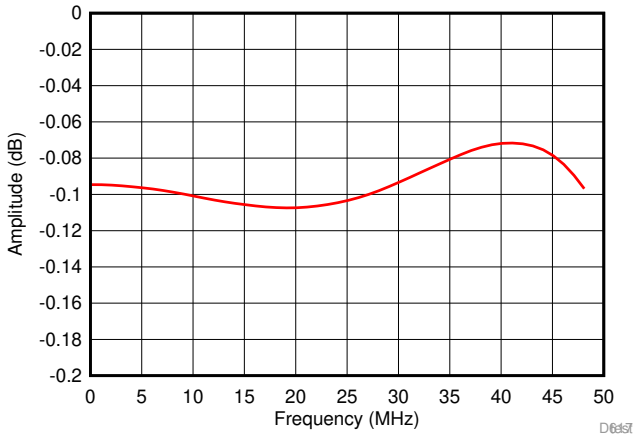


Figure 535. TX Front Stage Filter Response for Interpolate by 20 (Passband)

9.3.3.4 Back Stage Interpolation Block

The back stage digital interpolation filters provide over 90 dB of image rejection of the in-band signal. Passband is defined as 80% of the baseband sample rate and in-band peak-to-peak ripple is for common interpolation factors below 0.1 dB, and in always better than 0.2 dB.

For signals with lower amplitudes at the edge of the passband (like with digital pre-distortion, for example), the bandwidth can also be extended.

The back stage interpolation filter responses are shown in Figure 536 through Figure 545. Interpolation by 2 and 3 are shown for full rate DUC combining mode with an input rate of 2949.12 MSPS. Interpolation by 4 is shown for are shown for half rate DUC combining mode with an input rate of 1474.56 MSPS. The interpolation by 4 response is also value for full rate DUC combining mode with an input rate of 2949.12 MSPS by multiplying the x-axis by 2. The interpolation by 6 and 8 responses are shown for a half rate DUC combining mode of 1474.56 MSPS.

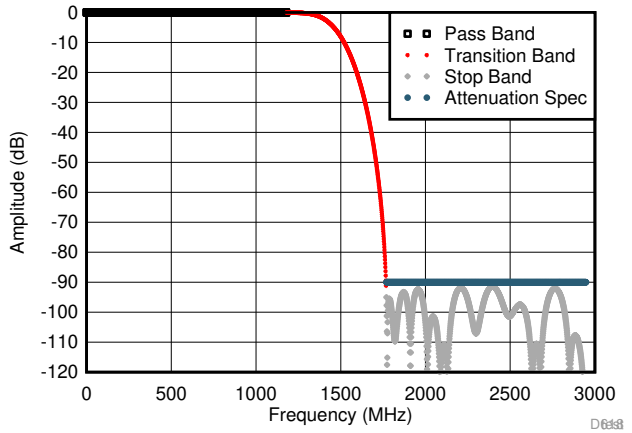


Figure 536. TX Back Stage Filter Response for Interpolate by 2 (Nyquist)

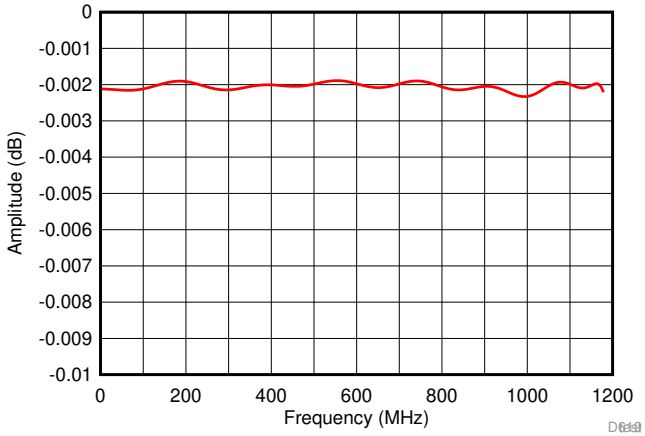


Figure 537. TX Back Stage Filter Response for Interpolate by 2 (Passband)

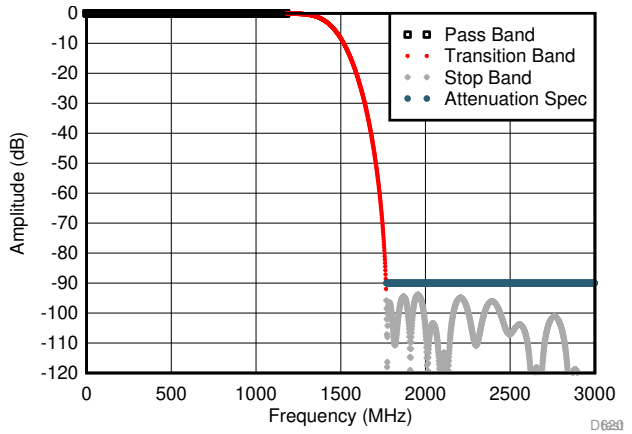


Figure 538. TX Back Stage Filter Response for Interpolate by 3 (Nyquist)

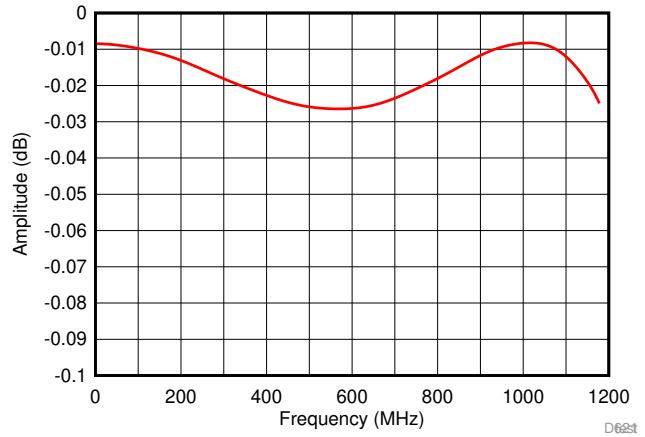


Figure 539. TX Back Stage Filter Response for Interpolate by 3 (Passband)

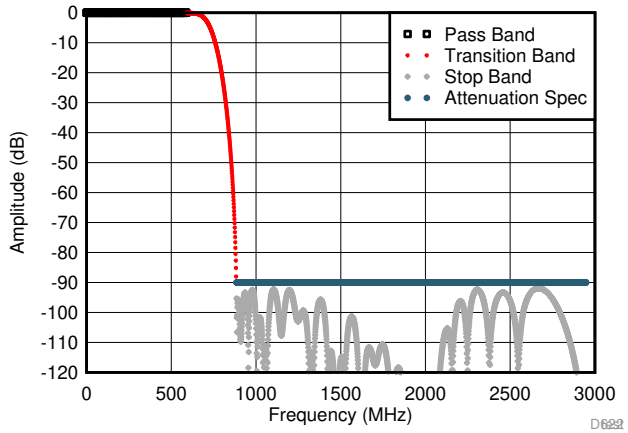


Figure 540. TX Back Stage Filter Response for Interpolate by 4 (Nyquist)

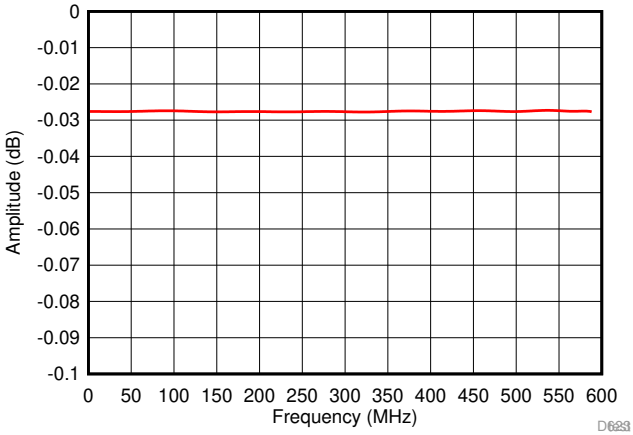


Figure 541. TX Back Stage Filter Response for Interpolate by 4 (Passband)

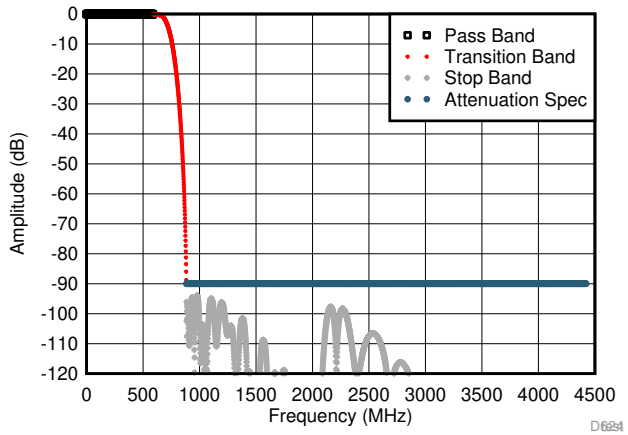


Figure 542. TX Back Stage Filter Response for Interpolate by 6 (Nyquist)

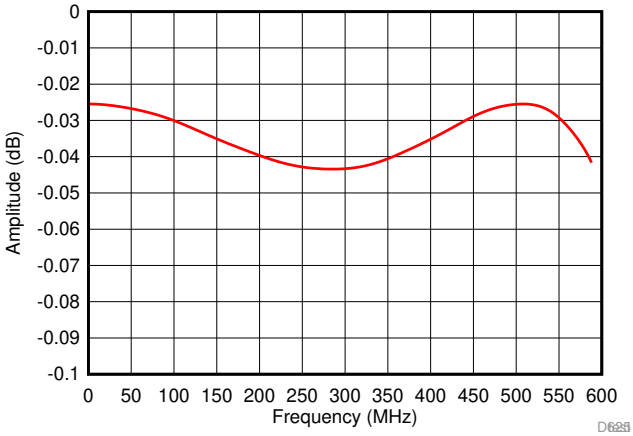


Figure 543. TX Back Stage Filter Response for Interpolate by 6 (Passband)

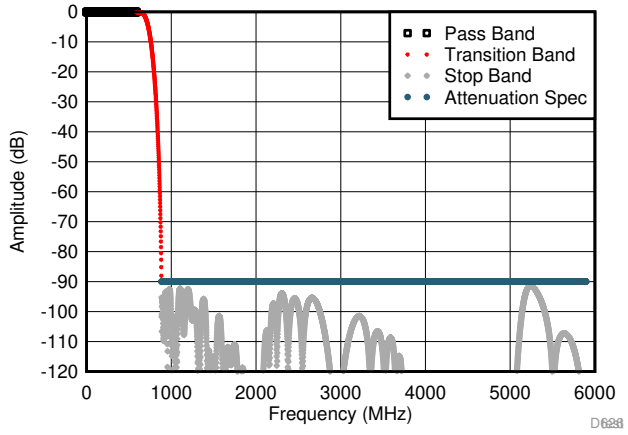


Figure 544. TX Back Stage Filter Response for Interpolate by 8 (Nyquist)

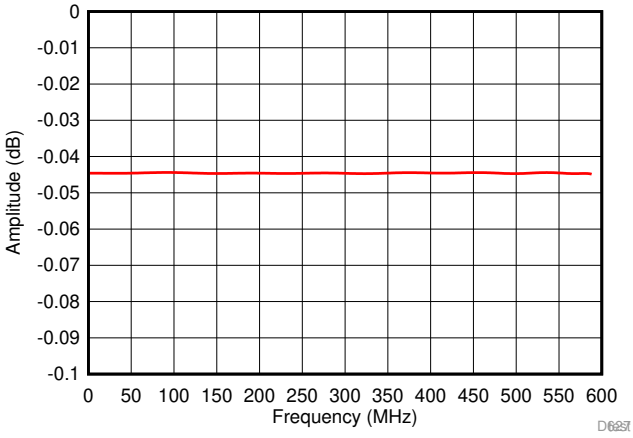


Figure 545. TX Back Stage Filter Response for Interpolate by 8 (Passband)

9.3.3.5 Digital Mixer and NCOs

The front and back mixers includes two NCOs each, whose frequency can be set independently. The mixers can switch between two NCOs, each able to maintain the NCO phase at all times. The switch between the two NCOs can be controlled through the SPI or dedicated GPIO pin. The NCOs have two options for setting the frequency. First, they can have a 32-bit resolution with the frequency specified as the N × sample rate × $1/2^{32}$. Optionally, the NCOs can provide an exact 1-kHz raster for an input reference clock frequency of N × 61.44 MHz, where N is an integer. The NCOs and mixer provide a SFDR of 100 dB.

9.3.3.6 Inverse Sinc Filter

The device has an inverse Sinc filter that runs at the DAC update rate (f^{DAC}) that can be used to flatten the frequency response of the sample-and-hold output. There are two different filters - one for a zero order hold output used in 1st Nyquist zone and another for the mixed mode output used in the 2nd Nyquist zone. The DAC sample-and-hold output sets the output current and holds it constant for one DAC clock cycle until the next sample, resulting in the well known sin(x)/x or Sinc(x) frequency response (Figure 546, red line). The inverse sinc filter response (Figure 546, black line) has the opposite frequency response from 0 to 0.4 × f_{DAC}, resulting in the combined response (Figure 546, grey line). Similar curves are shown in Figure 547 for the 2nd Nyquist zone mode.

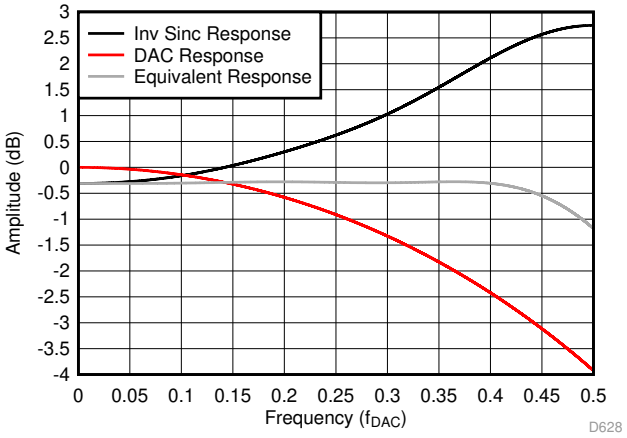


Figure 546. DAC, Inverse Sinc Filter and Composite Response for 1st Nyquist Zone

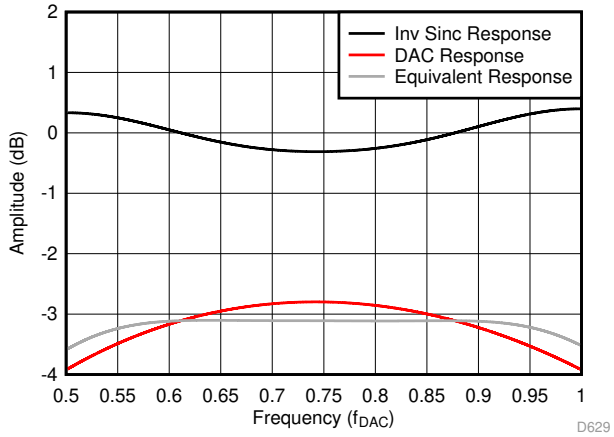


Figure 547. DAC, Inverse Sinc Filter and Composite Response for 2nd Nyquist Zone

The inverse sinc filters have a gain > 1 at some frequencies. Therefore, the signal input to the inverse sinc filter must be reduced from full scale to prevent saturation in the filter. The amount of back-off required depends on the signal frequency, and is set such that at the signal frequencies the combination of the input signal and filter response is less than 1 (0 dB). For example, if the signal input to inverse sinc filter is at 0.25 × f_{DAC}, the response of the 1st Nyquist inverse sinc filter is 0.6 dB, and the signal must be backed off from full scale by 0.6 dB to avoid saturation. The advantage of the inverse since filter having a positive gain at all frequencies is that the user is then able to optimize the back-off of the signal based on its frequency.

9.3.3.7 Delay Block

A programmable delay can be configured in integer multiples of the DAC clock period up to 31 clocks through a dedicated 5-bit SPI register. There may be an offset in delay between the 0 delay setting when enabled and when the delay is disabled.

9.3.3.8 TX RF Output Gain Control (TX DSA)

The output stage of each transmitter chain is a wideband differential RF amplifier with integrated gain control, which conceptually we will refer to as the TX DSA. The gain of the output stage is set through the SPI accessing the allocated register. AFE79xx supports also a mode where the TX new gain setting is applied only when a dedicated GPIO is enabled, which is configured through the SPI. Each transmitter chain has two internal registers (reg A and reg B) for the DSA setting. In default mode only one register is used and its value is directly applied to the DSA. It is possible to configure the device through SPI to support the use of both registers. In this case, the selection of the valid register is done through dedicated pins. Three GPIO configurations are supported: one, two and four pin options.

In the one pin configuration a single GPIO function is used. Select the use of Reg A or Reg B to set the DSA for all 4 transmitter chains (Low = Reg A; High = Reg B). The channels for the swap can be masked or unmasked through a SPI register.

In the two pins configuration, instead one GPIO function level controls the use of reg A (low) or Reg B value for the gain setting of TX1 and TX2; while the other two chains (TX3 and TX4) are controlled by a second GPIO function.

In the four pin configuration, each TX channel can be controlled separately by a GPIO function.

The AFE79xx supports a smooth change of TX DSA from one value to another. The TX DSA (in analog) supports gain steps of 0.25, 0.5, and 0.75 dB which can be used during the transition (the steady-state step size is 1 dB). The wait time in each step is programmable (as a Macro argument) with the resolution of 0.125 µs.

The AFE79xx can also use the TX digital gain in steps of 0.125 dB to make it look like the gain transition happens with steps of 0.125 dB. In the dual band case, the attenuation in each band can potentially move in different directions using the separate digital gain for each band.

9.3.3.9 Straight, Interleaved and Mixed Mode Outputs

The device TX can operate in either straight or interleaved mode. Interleaved mode uses a half rate clock to save power, but will have an image at $F_{DAC}/2 – F_{OUT}$. With TI factory trim, the spur will be below –50 dBc.

The device TX can also operate in a mixed mode, where the output is inverted after 1/2 of the DAC clock cycle. the results in the 2nd and 3rd Nyquist images to be emphasized with higher output power.

9.3.4 Feedback (FB) Chain

AFE7920/21 includes 2 Feedback (FB) chains based on direct RF sampling architecture whose block diagram is shown in Figure 548. The FB chain is normally used as observation path of the PA (power amplifier) output for an external linearization DPD engine. In the AFE7988/89, there are no feedback ADCs, but the feedback path DDCs can time share the RX ADC outputs.

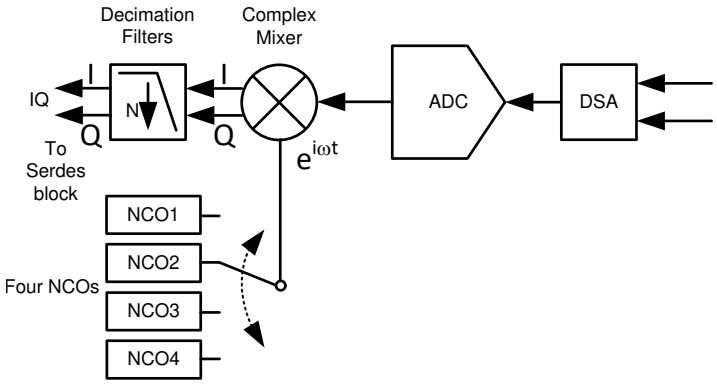


Figure 548. Feedback Path Block Diagram

9.3.4.1 Feedback Chain Analog Block

In AFE7920/21, the FB path analog block includes an input DSA and a RF sampling ADC. The DSA attenuation is set through the SPI. In AFE7988/89, there's no dedicated feedback chain analog block (ADC & DSA), and these blocks are time shared with the receiver paths.

9.3.4.2 FB Chain Digital Block

The digital section of the AFE79xx feedback chain is shown in Figure 548. The first function is a mixer to convert to a complex baseband signal. The mixer has four switchable NCOs, so for a multi-band application, the NCO phase for one band can be maintained when the other NCO for another band is being used. Following the mixer is a decimation stage.

9.3.4.3 Delay Block

A programmable delay can be configured in integer multiples of the ADC clock period up to 31 clocks through a dedicated 5-bit SPI register. There may be an offset in delay between the 0 delay setting when enabled and when the delay is disabled.

9.3.4.4 FB Peak Detector

The FB chain includes a peak detector at the ADC, whose output can be read through the SPI.

The digital peak detector first computes the peak value of the ADC over every 8 ADC samples. The overall peak among N such peaks is computed where N is the programmable block length. Block length(LSB is 8 full rate ADC CLKs) can be programmed with a 17 bit value. This peak value during the block is stored in an 8-bit SPI register Peak over 8 samples is compared against a programmable threshold (8 bit value). The number of level crossings during the block length N is stored in a 17-bit SPI register. The values in the registers are continuously updated. To read the peak detector output, it is required to stop the SPI registers update through a specific register bit. After the reading of the peak detector registers has been completed, it is required to clear the bit that holds the update. When ADC is in half rate mode, the peak is computed over 4 samples and block length is defined in terms of every 4 ADC clocks (or 8 full rate ADC clocks).

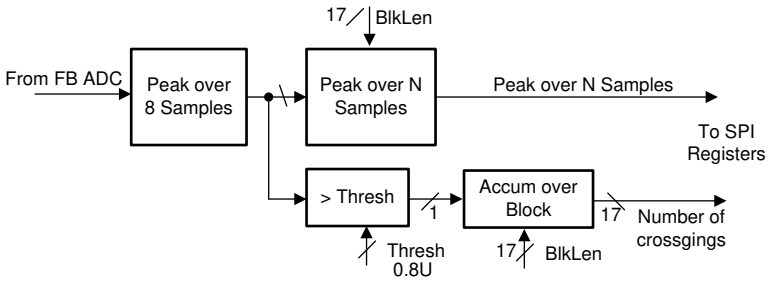


Figure 549. FB Peak Detector Block Diagram

9.3.4.5 FB Digital Mixer and NCOs

The FB path includes four NCOs, whose frequency can be set independently. The FB mixer can switch between four NCOs, each one running at different frequency, so the NCO phase is maintained at all times. The switch between the four NCOs can be controlled through the SPI or GPIO.

The NCOs have two options for setting the frequency. First, they can have a 32-bit resolution with the frequency specified as the N*sample rate × $1/2^{32}$. Optionally, the NCOs can provide an exact 1-kHz raster for an input reference clock frequency of N × 61.44 MHz, where N is an integer. The NCOs and mixer provide a SFDR of 100 dB.

9.3.4.6 FB Decimation Block

The FB decimation block decimates the ADC sample rate data to the output rate. The decimation block is highly flexible, matching the interface rates to the possible ADC sample rates. Unlike the RX path, there is only one DDC per FB path. The rates are listed in the tables below. Boxes without numbers are not valid modes of operation. In AFE7921/AFE7989, the maximum output data rate of the FB decimation block is 491.52MSPS.

For wide bandwidth modes such as decimate by 2 or 3, care should be taken to select the NCO so that the output bandwidth does not overlap an ADC Nyquist zone. For example, in decimate by 2 mode, the NCO frequency should be set to (2 × N – 1) × $f_{ADC}/4$ in the center of the Nyquist zone, where N is the Nyquist zone number. For decimate by 3, the NCO frequency should be set within approximately 250 MHz from the center of the Nyquist zone.

Table 7. Decimation Factors Between FB ADC and Output Sample Rates

		ADC SAMPLE (MSPS) RATE					
		1228.8	1474.56	1966.08	2211.84	2457.6	2949.12
Output Rate (MSPS)	122.88	10	12	16		20	24
	184.32		8		12		16
	245.76	5	6	8		10	12
	368.64		4		6		8
	491.52	2.5	3	4		5	6
	737.28		2		3		4
	983.04			2		2.5	3
	1474.56						2

The digital decimation filters provide over 85 dB of image rejection of the in-band signal. Passband is defined as 81.4% of the baseband sample rate and in-band peak-to-peak ripple is less than 0.04 dB.

The decimation filter responses for decimation from 2949.12 MSPS are shown in Figure 554 through Figure 555. The filter responses for other modes are available upon request from Texas Instruments.

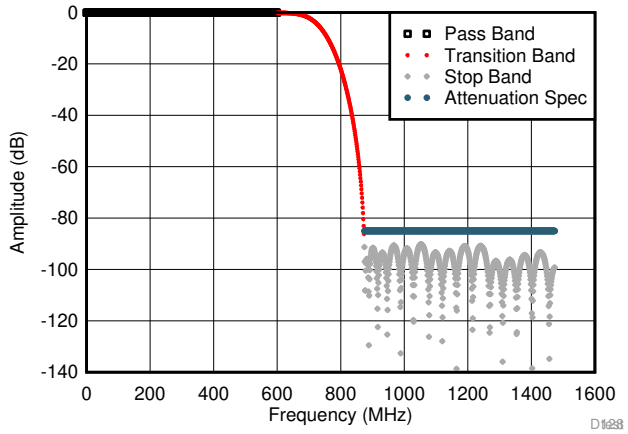


Figure 550. FB Filter Response for Decimation by 2 (Nyquist)

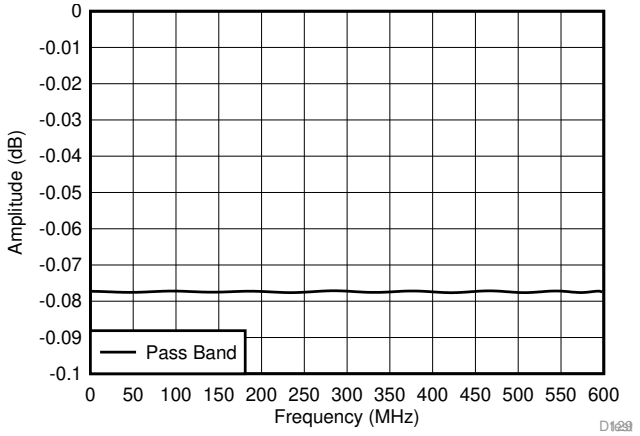


Figure 551. FB Filter Response for Decimation by 2 (Passband)

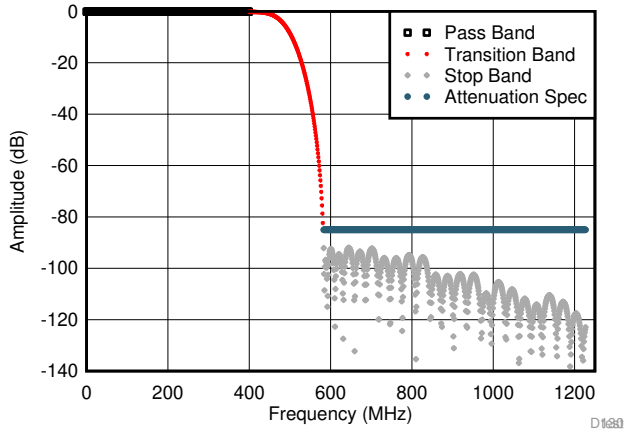


Figure 552. FB Filter Response for Decimation by 2.5 (Nyquist)

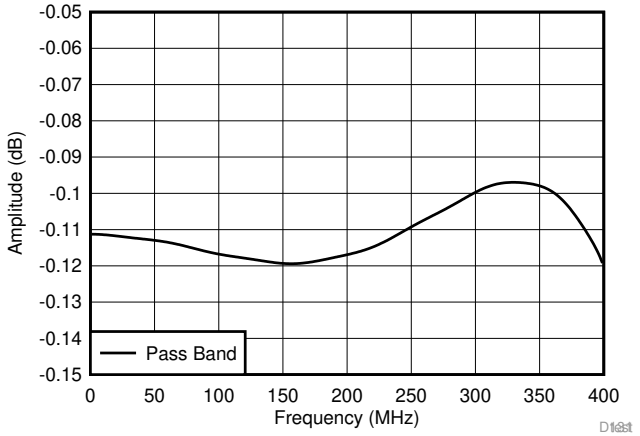


Figure 553. FB Filter Response for Decimation by 2.5 (Passband)

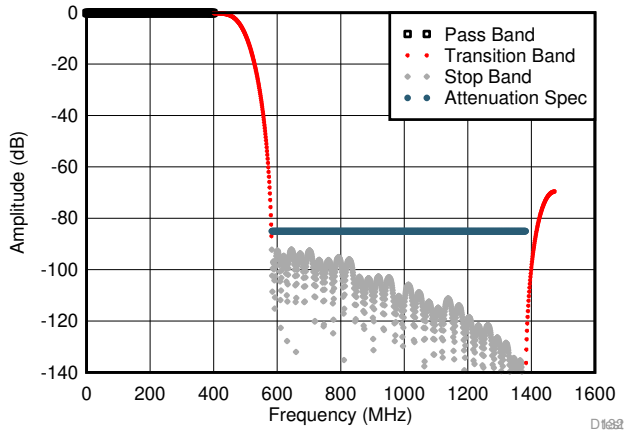


Figure 554. FB Filter Response for Decimation by 3 (Nyquist)

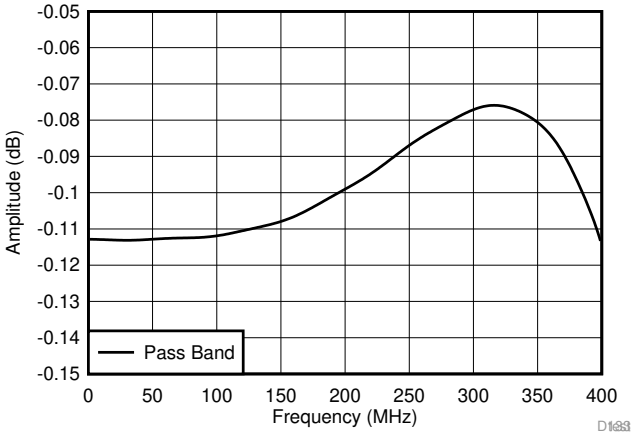


Figure 555. FB Filter Response for Decimation by 3 (Passband)

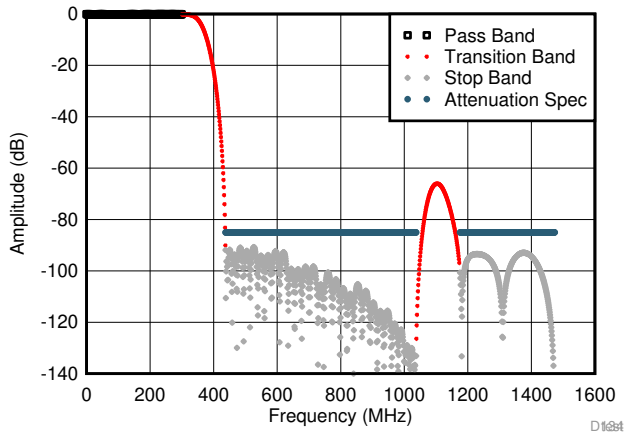


Figure 556. FB Filter Response for Decimation by 4 (Nyquist)

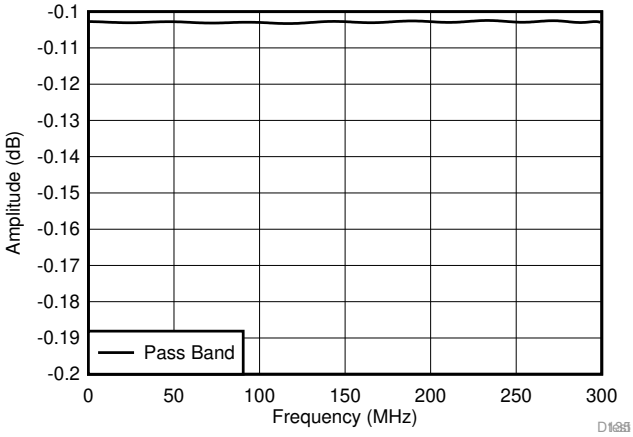


Figure 557. FB Filter Response for Decimation by 4 (Passband)

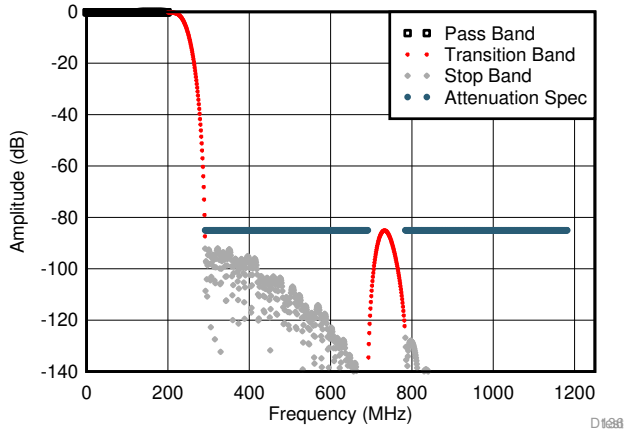


Figure 558. FB Filter Response for Decimation by 5 (Nyquist)

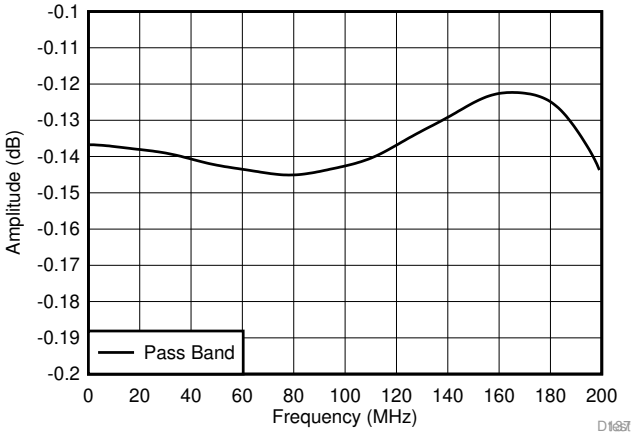


Figure 559. FB Filter Response for Decimation by 5 (Passband)

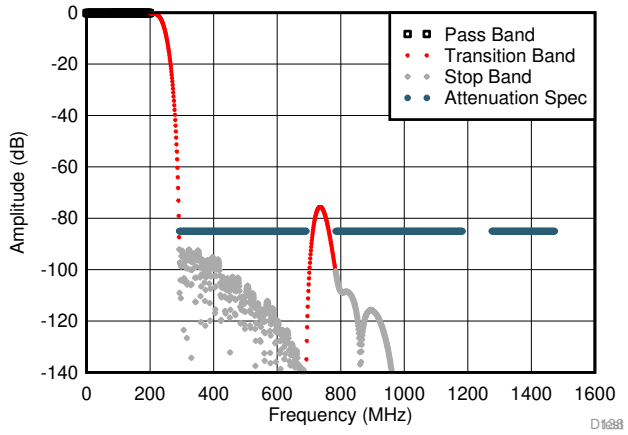


Figure 560. FB Filter Response for Decimation by 6 (Nyquist)

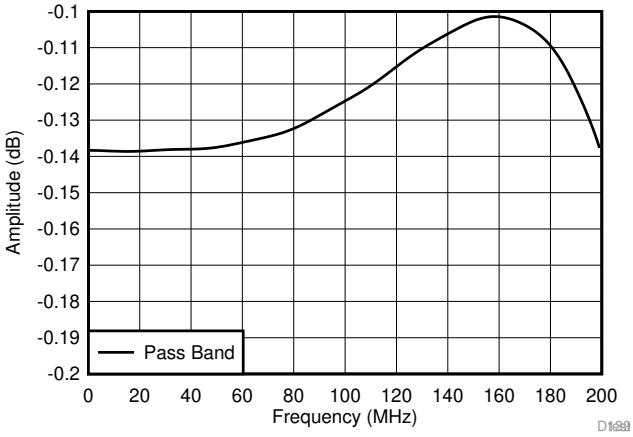


Figure 561. FB Filter Response for Decimation by 6 (Passband)

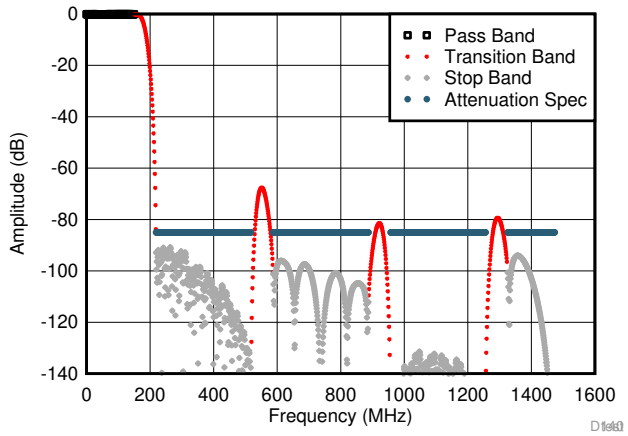


Figure 562. FB Filter Response for Decimation by 8 (Nyquist)

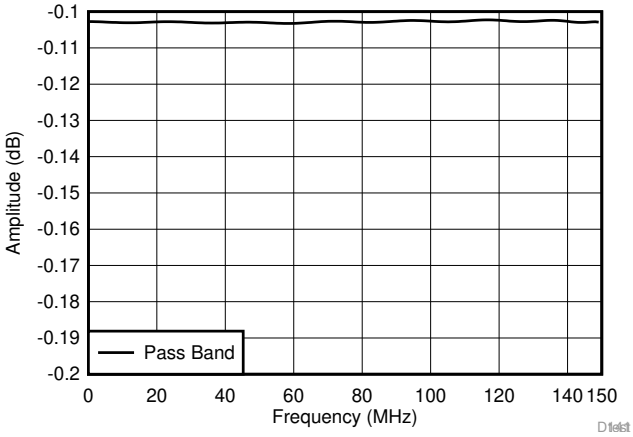


Figure 563. FB Filter Response for Decimation by 8 (Passband)

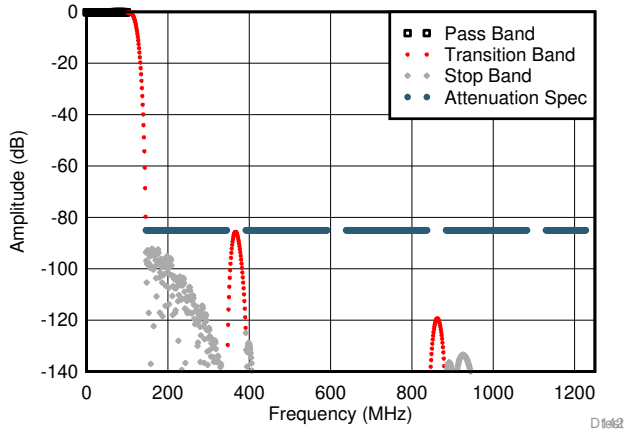


Figure 564. FB Filter Response for Decimation by 10 (Nyquist)

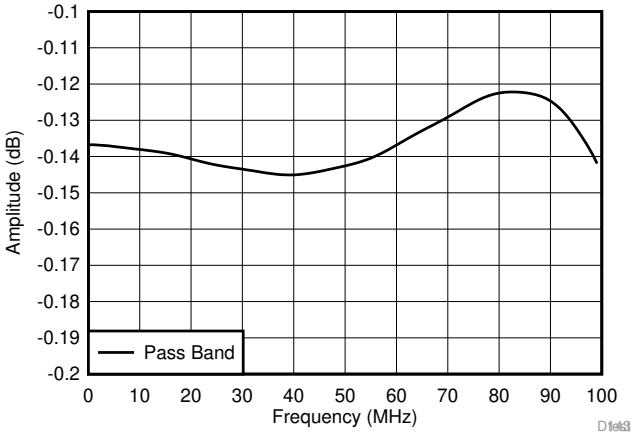


Figure 565. FB Filter Response for Decimation by 10 (Passband)

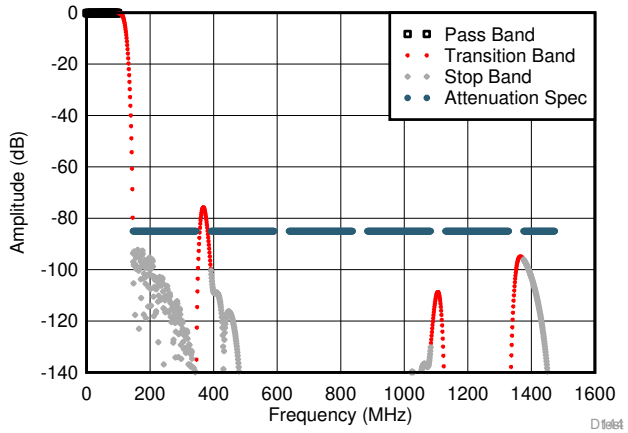


Figure 566. FB Filter Response for Decimation by 12 (Nyquist)

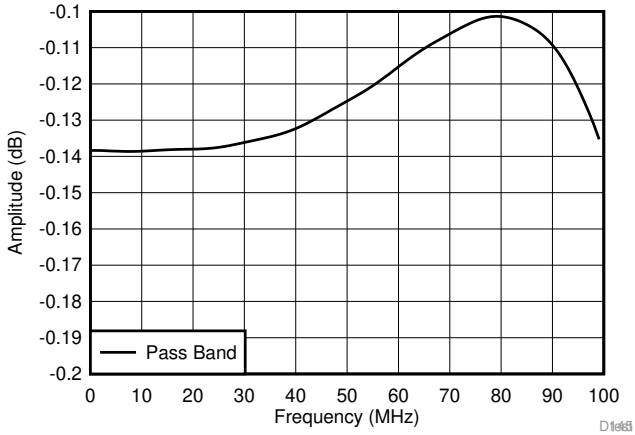


Figure 567. FB Filter Response for Decimation by 12 (Passband)

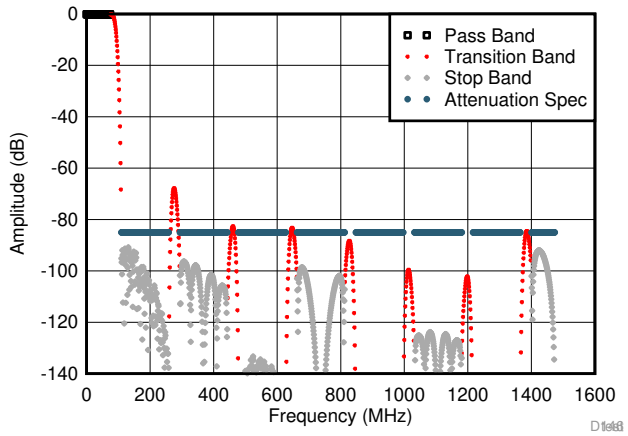


Figure 568. FB Filter Response for Decimation by 16 (Nyquist)

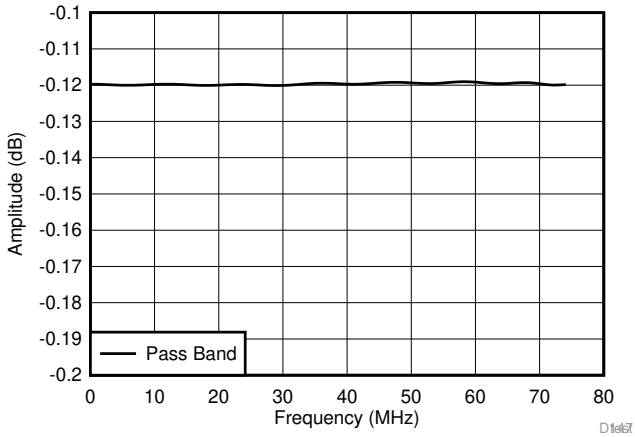


Figure 569. FB Filter Response for Decimation by 16 (Passband)

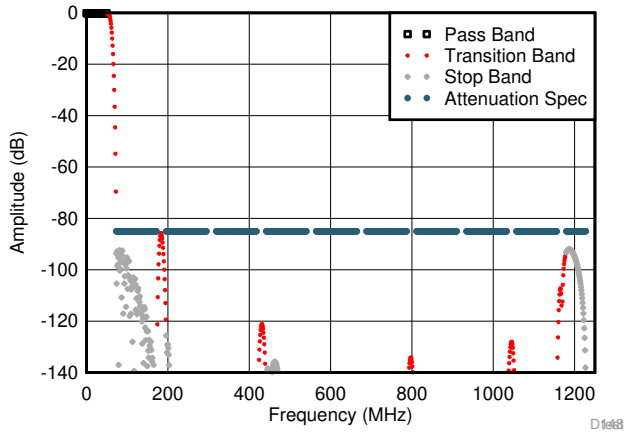


Figure 570. FB Filter Response for Decimation by 20 (Nyquist)

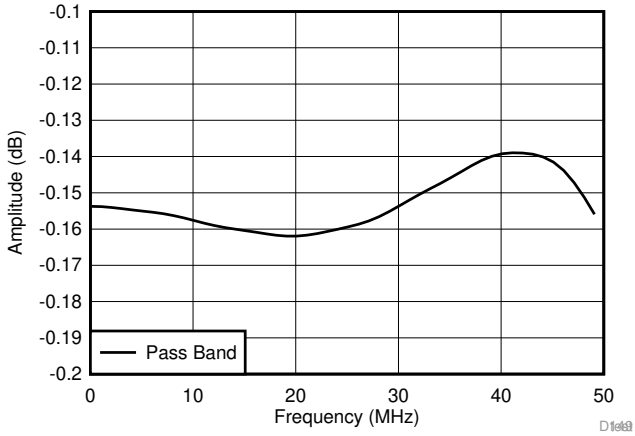


Figure 571. FB Filter Response for Decimation by 20 (Passband)

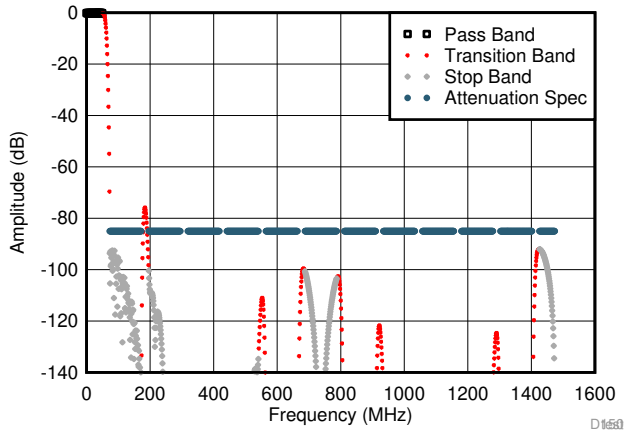


Figure 572. FB Filter Response for Decimation by 24 (Nyquist)

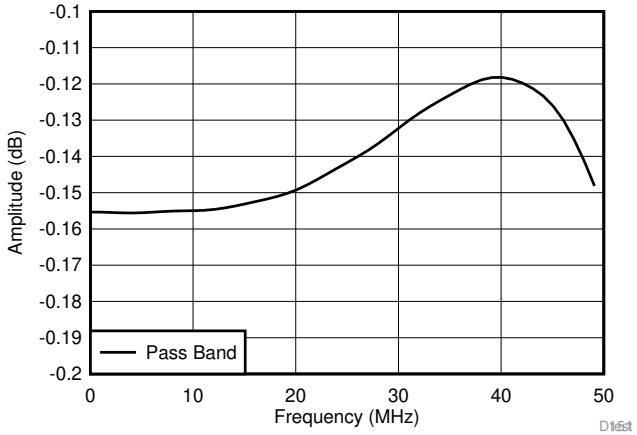


Figure 573. FB Filter Response for Decimation by 24 (Passband)

9.3.5 Synthesizers and Clocking

9.3.5.1 Internal PLL/VCO

The AFE79xx has an internal PLL with 4 separate VCOs to generate the clock at the DAC sample rate (or at 2x the DAC sample rate). The VCOs cover the common frequencies of 7372.8 MHz, 7864.32 MHz, 8847.36 MHz, 9830.4 MHz and 11796.48 MHz.

The recommended common reference clock frequency (F_{REF}) is 491.52 MHz, but the device can work with F_{REF} down to 122.88 MHz.

9.3.5.2 DAC/ADC Sample Rate Combinations

When using a divided DAC clock for the ADC clock (required for the FB ADCs), the available DAC and ADC sample rates combinations is given in Table 8:

Table 8. TX DAC / FB ADC Rate Combinations

÷	f_{DAC} (MSPS)								
	3932.16	**4423.68**	**4915.20**	**5898.24**	**7372.8**	**7864.32**	**8847.36**	**9830.40**	**11796.48**
2	1966.08	2211.84	2457.60	2949.12					
3		1474.56		1966.08	2457.6		2949.12		
4			1228.80	1474.56		1966.08	2211.84	2457.60	2949.12
6							1474.56		

The RX ADC rate can be independently selected from the FB ADC rate. Additionally, the RX ADC can use the input clock directly at the RX ADC sample rate. In that case the input clock is divided to provide the reference clock for the internal PLL/VCO.

9.3.5.3 Clock Distribution

The device has a flexible clock distribution circuit that is shown in Figure 574. The input clock can be used as a reference for the internal PLL/VCO and/or as an direct external clock for the DACs and ADCs. When used as a reference clock for the PLL/VCO, the input clock can be divided by the reference divider before the phase frequency detector (PFD). Each group of RX ADCs, FB ADCs or DAC can select either the PLL/VCO output or the external input clock. In this way for example, the RX ADCs can use the input clock directly, while a divided version of the input clock is used for the PLL/VCO, which then drives the DAC and FB ADCs.

When the reference divider is not equal to 1, the SYSREF input can be used to sync the N-divider. This is useful for synchronizing the PFD frequency of the on-chip PLLs across multiple devices.

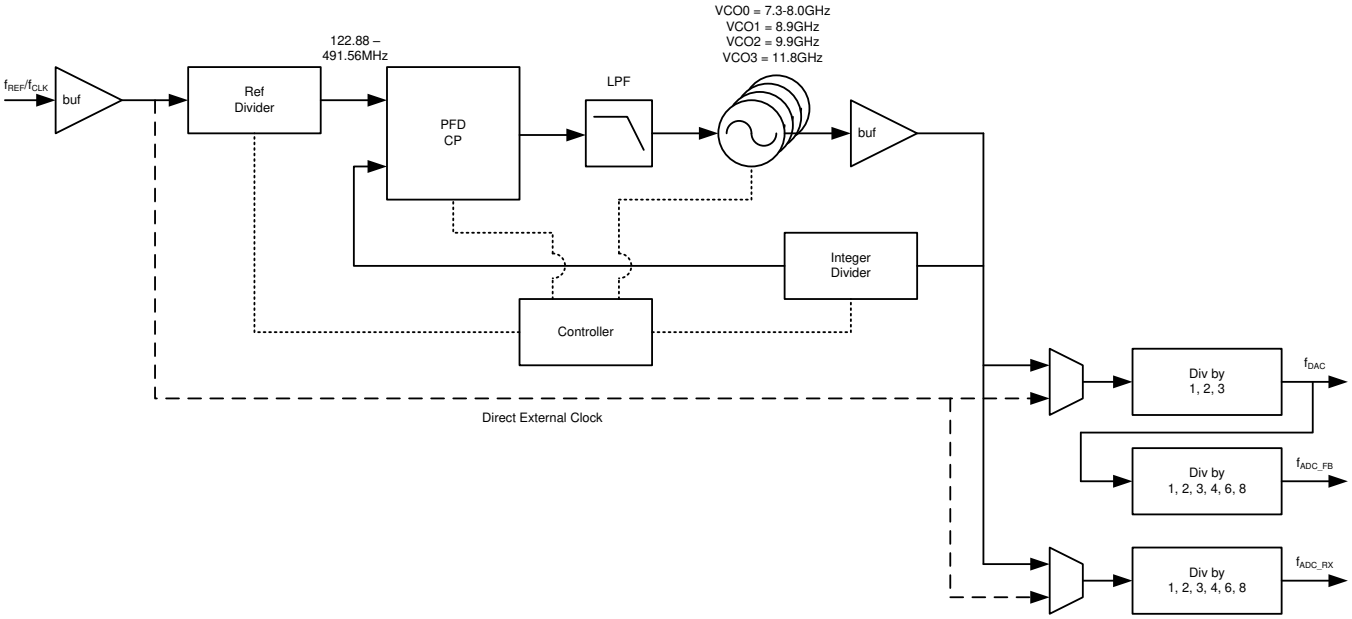


Figure 574. LO Distribution Chain

9.3.6 SYSREF Requirements

In many applications, such as multi antenna systems where the various transmit channels information is correlated, it is required that the latency across the link is deterministic and multiple devices are completely synchronized such that their outputs are phase aligned. The device achieves the deterministic latency using SYSREF to synchronize the devices internal dividers, signal processing blocks and elastic buffer. SYSREF is generated from the same clock domain as the device clock.

The SYSREF capture requirements are shown in Figure 575. Three SYSREF pulses are required to completely synchronize the device. These three pulses are necessary to synchronize the N-divider (if needed), clock divider for the digital logics, and the JESD204 link-up. A powerpoint regarding the SYSREF usage in the bring-up software flow is available from TI. For each pulse, a SPI register latch is programmed high, after which the 1st SYSREF pulse is captured and the following pulses are ignored. SYSREF then would need to be held low for the SPI latch to be programmed low then high again for the next pulse. After the 3 pulses, TI recommends that SYSREF is turned off or held low to prevent spurs coupling into the device clock.

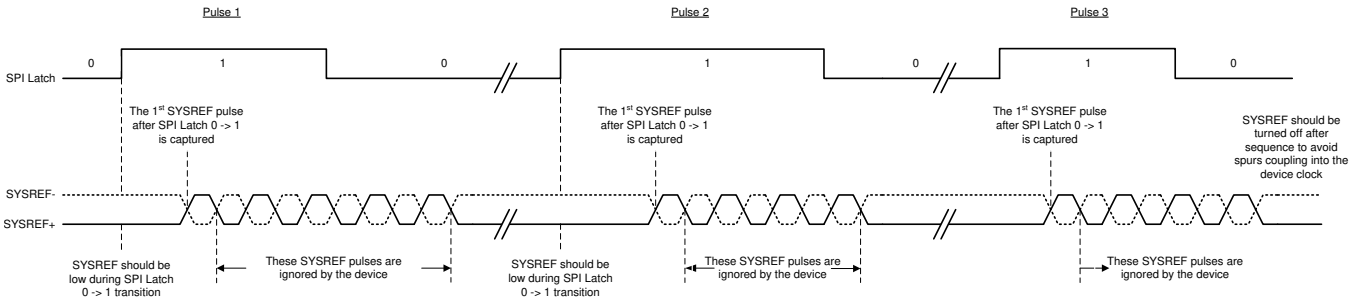


Figure 575. SYSREF Capture Requirements

The SYSREF pulse must match a gapped periodic timing with the frequency matching the following requirements:

- RX/FB ADC sampling rate/48
- TX DAC sampling rate/192
- RX/FB/TX Interface Rate/16
- In the 204B case, all lane rates/(80 × K × F) where K is the number of multi frames and F is the # of

octets/frame.

- In the 204C case, all lane rates/(2112 × E) where E is the number of Extended Multi Blocks.
- It should be a maximum of 5.76 MHz.

An Excel spreadsheet to calculate possible SYSREF frequencies is available from TI.

9.3.7 SerDes

The AFE79xx has two SerDes macros. Each SerDes macro is composed by a TX block with 4 transmitter lanes, a RX block with 4 receiver lanes, and a common PLL block for TX and a common PLL block for RX. A high level block diagram of each SerDes macro is shown in Figure 576. The SerDes supports multiple lane rates divided in 3 modes: Full, Half, and Quarter rate mode.

Table 9. SerDes Lane Rates

MODE	RATES
Full Rate	18.5 to 29.5 Gbps
Half Rate	9.25 to 16.25 Gbps
Quarter Rate	4.625 to 8.12 Gbps

Within each SerDes macro, each TX and RX lane can be enabled or disabled independently to optimize the power dissipation.

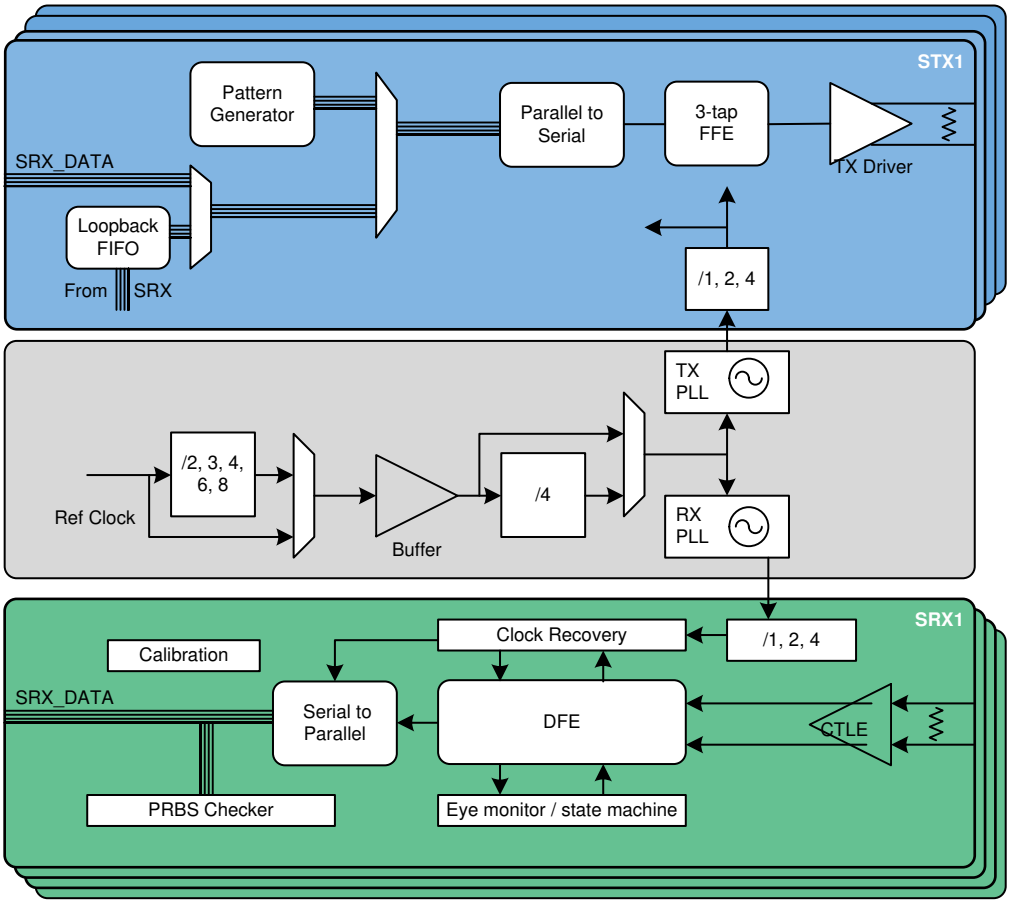


Figure 576. SerDes Block Diagram

9.3.7.1 SerDes Multiplexer

The device contains a multiplexer that is able to map any JESD stream to any SerDes transceiver. The SerDes rates will be limited by the common TX and RX PLLs so that the baud rate for each group of four SerDes will need to be related by a factor of 2 or 4.

9.3.7.2 SerDes Transmitter

Each SerDes transmitter incorporates a three tap finite impulse response (FIR) filter and a programmable output amplitude to compensate for frequency dependent loss in the transmission media. The 3-tap FFE for the TX pre-emphasis is defined by Equation 2:

$$x(k) = c_{-1}\, a(k + 1) + c_0\, a(k) + c_1\, a(k - 1) \quad (2)$$

where

- the binary input is {–1,1}.

All coefficients are register programmable with a step size of 1. The coefficients have to be set such that x(k) is less than or equal to 25 and is in accordance with Table 10.

Table 10. SerDes TX FFE Settings

MAIN CURSOR VALUE	POST-CURSOR VALUE	PRE-CURSOR VALUE	POST-CURSOR EQUALIZATION (dB)	PRE-CURSOR EQUALIZATION (dB)	POST-CURSOR SETTING	PRE-CURSOR SETTING	MAIN SETTING
25	0	0	0	0	000	000	000
23	0	0	0	0	000	000	001
21	0	0	0	0	000	000	010
19	0	0	0	0	000	000	011
17	0	0	0	0	000	000	100
15	0	0	0	0	000	000	101
13	0	0	0	0	000	000	110
11	0	0	0	0	000	000	111
24	–1	0	0.72	0	001	000	000
20	–1	0	0.87	0	001	000	010
16	–1	0	1.09	0	001	000	100
12	–1	0	1.45	0	001	000	110
23	–2	0	1.51	0	010	000	000
21	–2	0	1.66	0	010	000	001
15	–2	0	2.33	0	010	000	100
22	–3	0	2.38	0	011	000	000
13	–2	0	2.69	0	010	000	101
21	–4	0	3.35	0	100	000	000
19	–4	0	3.71	0	100	000	001
14	–3	0	3.78	0	011	000	100
17	–4	0	4.17	0	100	000	010
20	–5	0	4.44	0	101	000	000
15	–4	0	4.75	0	100	000	011
16	–5	0	5.62	0	101	000	010
19	–6	0	5.68	0	110	000	000
17	–6	0	6.41	0	110	000	001
18	–7	0	7.13	0	111	000	000
24	0	–1	0	0.72	000	001	000
20	0	–1	0	0.87	000	001	010
22	–2	–1	1.66	0.87	010	001	000
16	0	–1	0	1.09	000	001	100
20	–4	–1	3.71	1.09	100	001	000
12	0	–1	0	1.45	000	001	110
14	–2	–1	2.69	1.45	010	001	100

Table 10. SerDes TX FFE Settings (continued)

MAIN CURSOR VALUE	POST-CURSOR VALUE	PRE-CURSOR VALUE	POST-CURSOR EQUALIZATION (dB)	PRE-CURSOR EQUALIZATION (dB)	POST-CURSOR SETTING	PRE-CURSOR SETTING	MAIN SETTING
16	–4	–1	4.75	1.45	100	001	010
18	–6	–1	6.41	1.45	110	001	000
23	0	–2	0	1.51	000	010	000
21	0	–2	0	1.66	000	010	001
22	–1	–2	0.87	1.66	001	010	000
15	0	–2	0	2.33	000	010	100
19	–4	–2	4.17	2.33	100	010	000
22	0	–3	0	2.38	000	011	000
18	–5	–2	5.62	2.69	101	010	000
13	0	–2	0	2.69	000	010	101
14	–1	–2	1.45	2.69	001	010	100
17	–4	–2	4.75	2.69	100	010	001
21	0	–4	0	3.35	000	100	000
19	0	–4	0	3.71	000	100	001
20	–1	–4	1.09	3.71	001	100	000
18	–4	–3	4.75	3.78	100	011	000
14	0	–3	0	3.78	000	011	100
17	0	–4	0	4.17	000	100	010
19	–2	–4	2.33	4.17	010	100	000
20	0	–5	0	4.44	000	101	000
15	0	–4	0	4.75	000	100	011
16	–1	–4	1.45	4.75	001	100	010
18	–3	–4	3.78	4.75	011	100	000
17	–2	–4	2.69	4.75	010	100	001
16	0	–5	0	5.62	000	101	010
18	–2	–5	2.69	5.62	010	101	000
19	0	–6	0	5.68	000	110	000
18	–1	–6	1.45	6.41	001	110	000

In the Quarter Rate mode, the 3-tap FFE is not available.

Each SerDes transmitter driver has an internal termination resistor of 100 Ω, and its maximum peak-to-peak differential output voltage is 1 Vpp and programmable down to 500 mVpp.

9.3.7.3 SerDes Receiver

Each SerDes receiver consists of a Continuous Time Linear Equalizer (CTLE), followed by 1-tap adaptive decision feedback equalization (DFE). A clock recovery loop locks the incoming DFE data and makes the clock available to the common PLL block and can be used for the TX block if needed. The incoming signal first passes through the configurable CTLE. Then the remaining ISI at the CTLE output is removed by the DFE equalizer. DFE taps settings are constantly optimized based on the eye opening at the channel output. The data recovery block finds the optimal sampling phase for the equalized signal at the DFE output. The recovered clock, locked at the incoming data, is then used to generate the clock for the RX parallel data output.

The RX input includes an internal termination of 100-Ω differential. It does not integrate a DC-blocking capacitors, but each receiver lane can accept common-mode voltage within the range 0.4 V to 0.6 V. If the common voltage is outside this range, external series capacitors are required.

9.3.7.4 SerDes PLL, Common Block

The common block integrates two PLLs, one for the transmitters and one for the receivers; each PLL can be programmed separately. The TX PLL is shared by all 4 TX lanes and the RX PLL is shared by all 4 RX lanes. Each RX and TX lane has a dedicated clock divider by 1, 2, and 4, so that each lane can be configured independently into Full, Half, and Quarter rate mode. The VCO integrated in the both TX and RX covers the full rate mode frequency range (19.5 GHz to 32.5 GHz). The reference clock of the TX and RX PLL is derived from the external input reference clock through a programmable frequency divider with following division options: /1, /2, /3, /4, /6, and /8.

9.3.7.5 SerDes Test Modes

Each SerDes macro supports multiple test modes for self-test. In the TX block four self-generating PRBS patterns are available, as 32-bit repeating patterns, based on user register programmable data. The following PRBS patterns are supported:

1. PRBS9 ($x^9 + x^5 + 1$).
2. PRBS15 ($x^{15} + x^{14} + 1$)
3. PRBS23 ($x^{23} + x^{18} + 1$)
4. PRBS31 ($x^{31} + x^{28} + 1$)

The receiver chain integrates a checker for detecting the PRBS pattern error. It includes also an eye monitor to detect the eye height as well as generating more detailed eye diagrams, that can be read through the SPI.

The SerDes macro supports loopback of the RX block recovered data to the TX block through a FIFO. In this mode, the TX and RX lanes rate need to match. The loopback allows for full data path (TX and RX) verification.

9.3.8 JESD204B, JESD204C

9.3.8.1 Link Configuration and SYNC\ Interface

The AFE79xx interface can be configured with single or multiple links. The four transmitter chains and four received chains JESD can be arranged as single or dual links. The feedback path can be configured as single link. The possible link to SerDes lanes configurations are summarized in Table 11:

Table 11. JESD Link Configurations

	CONFIGURATION	DESCRIPTION
RX/FB Chains	6 links	1 link for each RX or FB chain. 4 links with 1 SerDes lane, 2 links with up to 2 SerDes lanes.
	4 links	2 links for RX and 2 links for FB, or 3 links for RX (2 on AB, 1 on CD), 1 link for FB.
	3 Links	2 links for RX and 1 link for FB chain; Each link for up to 2 SerDes lanes
	2 Links	1 link for RX and 1 link for FB; Each link for up to 4 SerDes lanes
	1 Link	1 link for RX chains for up to 8 SerDes lanes
	2 Links Shared	RX and FB sharing SerDes lanes: 2 links each one for up to 4 SerDes lanes
	1 Link Shared	RX and FB sharing SerDes lanes: 1 link for up to 4 SerDes lanes
TX Chains	4 Links	Each link for up to 2 SerDes lanes
	2 Links	Each link for up to 4 SerDes lanes
	1 Link	Single link for up to 8 SerDes lanes

The AFE79xx ballmap includes 4 balls for the SYNC| input and 4 balls for the SYNC| output. Both the 4 inputs and the 4 outputs can be programmed to support two differential LVDS or up to four single-ended CMOS inputs/outputs. The four pins SYNCINA/B/C/D are used for both the RX and FB chains. In addition, two other GPIO balls can be assigned to support 2 addition SYNC| inputs.

9.3.8.2 JESD204B/C Scrambler and Descrambler

For JESD204B, the scrambler is a 16-bit parallel self-synchronous scrambler based on the polynomial $1 + x^{14} + x^{15}$. For JESD204C, the scrambler is a 16-bit parallel self-synchronous scrambler based on the polynomial $1 + x^{58} + x^{39}$. From the standard specification, the scrambling process only occurs on the user data, not on the code group synchronization or the ILA sequence.

The descrambler processes the payload to reverse the effect of the scrambler using the same polynomial. From the JESD204B specification, the descrambling process only occurs on the user data, not on the code group synchronization or the ILA sequence.

9.3.8.3 JESD204B/C Frame Assembly

The JESD204B defines the following parameters:

- L = is the number of lanes
- M = is the number of I or Q streams per device (2 = 1 IQ pair, 4 = 2 IQ pairs, 8 = 4 IQ pairs)
- F = is the number of octets per frame clock period.
- S = is the number of samples per frame
- HD = is the High-Density bit which controls whether a sample may be divided over more lanes.
- N = NPRIME is the number of bits per sample (12 or 16 bits)

Same parameters are used for the JESD204C frame assembly.

9.3.8.3.1 JESD204B/C/H Frame Assembly for Transmitter Chains

The AFE79xx transmitter chains support multiple JESD modes, listed in the following Table 12 for 1 DUC per TX and Table 13 for 2 DUCs per TX (AFE7988/20 only). For each of the supported input rates, all possible L-M-F-S-Hd as single or dual links are listed with the associated SERDES RATEs, for both 8b/10b and 64b/66b encoding.

Table 12. JESD204B/C Formats for 1 DUC per TX Chain

INPUT RATE [MSPS]	RESOLUTION	ENCODING	SERDES RATE [Gbps]	L-M-F-S-Hd 1 LINK	L-M-F-S-Hd 2 LINKS	AVAILABLE IN AFE7921/AFE7989?
122.88	16	8/10b	19.6608	1-8-16-1-0		Yes
	16	8/10b	9.8304	2-8-8-1-0	1-4-8-1-0	Yes
	16	64/66b	16.22016	1-8-16-1-0		Yes
184.32	16	8/10b	7.3728	4-8-4-1-0	2-4-4-1-0	Yes
	16	8/10b	14.7456	2-8-8-1-0	1-4-8-1-0	Yes
	16	64/66b	12.16512	2-8-8-1-0	1-4-8-1-0	Yes
245.76	16	8/10b	19.6608	2-8-8-1-0	1-4-8-1-0	Yes
	16	8/10b	9.8304	4-8-4-1-0	2-4-4-1-0	Yes
	16	64/66b	16.22016	2-8-8-1-0	1-4-8-1-0	Yes
	16	64/66b	8.11008	4-8-4-1-0	2-4-4-1-0	Yes
368.64	16	8/10b	29.4912	2-8-8-1-0	1-4-8-1-0	Yes
	16	8/10b	19.6608	3-6-4-1-0		Yes
	16	8/10b	14.7456	4-8-4-1-0	2-4-4-1-0	Yes
	16	8/10b	7.3728	8-8-2-1-0	4-4-2-1-0	Yes
	16	64/66b	24.33024	2-8-8-1-0	1-4-8-1-0	Yes
	16	64/66b	12.16512	4-8-4-1-0	2-4-4-1-0	Yes
491.52	16	8/10b	19.6608	4-8-4-1-0	2-4-4-1-0	Yes
	16	8/10b	9.8304	8-8-2-1-0	4-4-2-1-0	Yes
	16	64/66b	16.22016	4-8-4-1-0	2-4-4-1-0	Yes
	16	64/66b	8.11008	8-8-2-1-0	4-4-2-1-0	Yes
	12	8/10b	29.4912	2-8-6-1-0	1-4-6-1-0	Yes
	12	8/10b	14.7456	4-8-3-1-0	2-4-3-1-0	Yes
	12	8/10b	7.3728	8-8-3-2-0	4-4-3-2-0	Yes
	12	64/66b	24.33024	2-8-6-1-0	1-4-6-1-0	Yes
	12	64/66b	12.16512	4-8-3-1-0	2-4-3-1-0	Yes
	24	64/66b	24.33024	4-8-6-1-0	2-4-6-1-0	Yes

Table 12. JESD204B/C Formats for 1 DUC per TX Chain (continued)

INPUT RATE [MSPS]	RESOLUTION	ENCODING	SERDES RATE [Gbps]	L-M-F-S-Hd 1 LINK	L-M-F-S-Hd 2 LINKS	AVAILABLE IN AFE7921/AFE7989?
737.28	16	8/10b	29.4912	4-8-4-1-0	2-4-4-1-0	No
	16	8/10b	14.7456	8-8-2-1-0	4-4-2-1-0	No
	16	64/66b	24.33024	4-8-4-1-0	2-4-4-1-0	No
	16	64/66b	24.33024	4-8-8-2-0	2-4-8-2-0	No
	16	64/66b	12.16512	8-8-2-1-0	4-4-2-1-0	No
	12	8/10b	22.1184	4-8-3-1-0	2-4-3-1-0	No
	12	8/10b	11.0592	8-8-3-2-0	4-4-3-2-0	No
983.04	16	8/10b	19.6608	8-8-2-1-0	4-4-2-1-0	No
	16	64/66b	16.22016	8-8-2-1-0	4-4-2-1-0	No
	12	64/66b	24.33024	4-8-3-1-0	2-4-3-1-0	No
	12	64/66b	12.16512	8-8-3-2-0	4-4-3-2-0	No
	24	64/66b	24.33024	8-8-3-1-0	4-4-3-1-0	No
1474.56	16	8/10b	29.4912	8-8-2-1-0	4-4-2-1-0	No
	16	64/66b	24.33024	8-8-2-1-0	4-4-2-1-0	No
	12	8/10b	22.1184	8-8-3-2-0	4-4-3-2-0	No

Table 13. JESD204B/C Formats for 2 DUCs per TX Chain

INPUT RATE [MSPS]	RESOLUTION	ENCODING	SERDES RATE [Gbps]	L-M-F-S-Hd 1 LINK	L-M-F-S-Hd 2 LINKS
122.88	16	8/10b	19.6608	2-16-16-1-0	1-8-16-1-0
	16	8/10b	9.8304	4-16-8-1-0	2-8-8-1-0
	16	64/66b	16.22016	2-16-16-1-0	1-8-16-1-0
	16	64/66b	8.11008	4-16-8-1-0	2-8-8-1-0
184.32	16	8/10b	29.4912	2-16-16-1-0	1-8-16-1-0
	16	8/10b	14.7456	4-16-8-1-0	2-8-8-1-0
	16	8/10b	7.3728	8-16-4-1-0	4-8-4-1-0
	16	64/66b	24.33024	2-16-16-1-0	1-8-16-1-0
	16	64/66b	12.16512	4-16-8-1-0	2-8-8-1-0
	16	64/66b	6.08256	8-16-4-1-0	4-8-4-1-0
245.76	16	8/10b	19.6608	4-16-8-1-0	2-8-8-1-0
	16	8/10b	9.8304	8-16-4-1-0	4-8-4-1-0
	16	64/66b	16.22016	4-16-8-1-0	2-8-8-1-0
	16	64/66b	8.11008	8-16-4-1-0	4-8-4-1-0
368.64	16	8/10b	29.4912	4-16-8-1-0	2-8-8-1-0
	16	8/10b	14.7456	8-16-4-1-0	4-8-4-1-0
	16	64/66b	24.33024	4-16-8-1-0	2-8-8-1-0
	16	64/66b	12.16512	8-16-4-1-0	4-8-4-1-0
491.52	16	8/10b	19.6608	8-16-4-1-0	4-8-4-1-0
	16	64/66b	16.22016	8-16-4-1-0	4-8-4-1-0
	12	8/10b	29.4912	4-16-6-1-0	2-8-6-1-0
	12	8/10b	14.7456	8-16-3-1-0	4-8-3-1-0
	12	64/66b	24.33024	4-16-6-1-0	2-8-6-1-0
	12	64/66b	12.16512	8-16-3-1-0	4-8-3-1-0
	24	64/66b	24.33024	8-16-3-1-0	
737.28	16	8/10b	29.4912	8-16-4-1-0	4-8-4-1-0
	16	64/66b	24.33024	8-16-4-1-0	4-8-4-1-0

9.3.8.3.2 JESD204B/C Frame Assembly for Receiver Chains

The AFE79xx receiver chains support multiple JESD modes, listed in the following Table 14 for 1 DDC per RX and Table 15 for 2 DDCs per RX (AFE7988/20 only). For each of the supported output rates, all possible LMFSHd as single or dual links are listed with the associated SERDES RATEs, for both 8b/10b and 64b/66b encoding. Figure 577 through Figure 593 contain the frame format for each of the modes. In these tables RXn_im[msb:lsb] and RXn_qm[msb:lsb] are bits from msb to lsb for the n^{th} (1,2,3,4) RX chain of the I and Q mth (0,1..) sample.

Table 14. JESD204B/C Formats for 1 DDC per RX Chain (4 RX)

OUTPUT RATE [MSPS]	OUTPUT RESOLUTION	ENCODING	SERDES RATE [Gbps]	L-M-F-S-Hd 1 LINK	L-M-F-S-Hd 2 LINKS	AVAILABLE IN AFE7921/AFE7988?
61.44	16	8/10b	19.6608	1-8-32-1-0		Yes
	16	8/10b	9.8304	1-8-16-1-0		Yes
	16	8/10b	4.9152	2-8-8-1-0	1-4-8-1-0	Yes
	24	8/10b	14.7456	1-8-24-1-0		Yes
	24	8/10b	7.3728	2-8-12-1-0	1-4-12-1-0	Yes
	24	64/66b	12.16512	1-8-24-1-0		Yes
92.16	16	8/10b	14.7456	1-8-16-1-0		Yes
	16	8/10b	7.3728	2-8-8-1-0	1-4-8-1-0	Yes
	16	64/66b	12.16512	1-8-16-1-0		Yes
	24	8/10b	11.0592	2-8-12-1-0	1-4-12-1-0	Yes
122.88	16	8/10b	4.9152	4-8-8-1-0	2-4-4-1-0	Yes
	16	8/10b	9.8304	2-8-8-1-0	1-4-8-1-0	Yes
	16	64/66b	8.11008	2-8-8-1-0	1-4-8-1-0	Yes
184.32	16	8/10b	29.4912	1-8-16-1-0		Yes
	16	8/10b	14.7456	2-8-8-1-0	1-4-8-1-0	Yes
	16	64/66b	24.33024	1-8-16-1-0		Yes
	16	64/66b	12.16512	2-8-8-1-0	1-4-8-1-0	Yes
	12	8/10b	22.1184	1-8-12-1-0		Yes
	12	8/10b	11.0592	2-8-6-1-0	1-4-6-1-0	Yes
245.76	16	8/10b	19.6608	2-8-8-1-0	1-4-8-1-0	Yes
	16	8/10b	9.8304	4-8-4-1-0	2-4-4-1-0	Yes
	16	64/66b	16.22016	2-8-8-1-0	1-4-8-1-0	Yes
	16	64/66b	8.11008	4-8-4-1-0	2-4-4-1-0	Yes
	12	8/10b	29.4912	1-8-12-1-0		Yes
	12	8/10b	14.7456	2-8-6-1-0	1-4-6-1-0	Yes
	12	64/66b	12.16512	2-8-6-1-0	1-4-6-1-0	Yes
	12	8/10b	7.3728	4-8-3-1-0	2-4-3-1-0	Yes
	12	64/66b	24.33024	1-8-12-1-0		Yes
	24	8/10b	14.7456	4-8-6-1-0	2-4-6-1-0	Yes
	24	64/66b	24.33024	2-8-12-1-0	1-4-12-1-0	Yes
368.64	16	8/10b	29.4912	2-8-8-1-0	1-4-8-1-0	Yes
	16	8/10b	14.7456	4-8-4-1-0	2-4-4-1-0	Yes
	16	8/10b	7.3728	8-8-2-1-0	4-4-2-1-0	Yes
	16	64/66b	24.33024	2-8-8-1-0	1-4-8-1-0	Yes
	16	64/66b	12.16512	4-8-4-1-0	2-4-4-1-0	Yes
	16	64/66b	6.08256	8-8-2-1-0	4-4-2-1-0	Yes
	16	8/10b	22.1184	2-8-6-1-0	1-4-3-1-0	Yes
	16	8/10b	11.0592	4-8-3-1-0	2-4-3-1-0	Yes

Table 14. JESD204B/C Formats for 1 DDC per RX Chain (4 RX) (continued)

OUTPUT RATE [MSPS]	OUTPUT RESOLUTION	ENCODING	SERDES RATE [Gbps]	L-M-F-S-Hd 1 LINK	L-M-F-S-Hd 2 LINKS	AVAILABLE IN AFE7921/AFE7988?
491.52	16	8/10b	19.6608	4-8-4-1-0	2-4-4-1-0	Yes
	16	8/10b	9.8304	8-8-2-1-0	4-4-2-1-0	Yes
	16	64/66b	16.22016	4-8-4-1-0	2-4-4-1-0	Yes
	12	8/10b	29.4912	2-8-6-1-0	1-4-3-1-0	Yes
	12	8/10b	14.7456	4-8-3-1-0	2-4-3-1-0	Yes
	12	8/10b	7.3728	8-8-3-2-0	4-4-3-2-0	Yes
	12	64/66b	24.33024	2-8-6-1-0	1-4-3-1-0	Yes
	12	64/66b	12.16512	4-8-3-1-0	2-4-3-1-0	Yes
	12	8/10b	14.7456	4-8-3-1-0	2-4-3-1-0	Yes
	24	8/10b	14.7456	8-8-3-1-0	4-4-3-1-0	Yes
	24	64/66b	24.33024	4-8-6-1-0	2-4-6-1-0	Yes
737.28	16	8/10b	29.4912	4-8-4-1-0	2-4-4-1-0	No
	16	8/10b	14.7456	8-8-2-1-0	4-4-2-1-0	No
	16	64/66b	24.33024	4-8-4-1-0	2-4-4-1-0	No
	16	64/66b	24.33024	4-8-8-2-0	2-4-8-2-0	No
	16	64/66b	12.16512	8-8-2-1-0	4-4-2-1-0	No
	12	8/10b	24.33024	4-8-3-1-0	2-4-3-1-0	No
	12	8/10b	12.16512	8-8-3-2-0	4-4-3-2-0	No

Octet	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Lane 1	RX1_i0[15:0]		RX1_q0[15:0]		RX2_i0[15:0]		RX2_q0[15:0]		RX3_i0[15:0]		RX3_q0[15:0]		RX4_i0[15:0]		RX4_q0[15:0]	

Figure 577. JESD204B/C Frame Format for RX Chain: L-M-F-S-Hd = 1-8-16-1-0 (One Link)

Octet	1	2	3	4	5	6	7	8
Lane 1	RX1_i0[15:0]		RX1_q0[15:0]		RX2_i0[15:0]		RX2_q0[15:0]	
Lane 2	RX3_i0[15:0]		RX3_q0[15:0]		RX4_i0[15:0]		RX4_q0[15:0]	

Figure 578. JESD204B/C Frame Format for RX Chain: L-M-F-S-Hd = 28810 (One Link)

Octet	1	2	3	4	5	6	7	8
Lane 1	RX1(3)_i0[15:0]		RX1(3)_q0[15:0]		RX2(4)_i0[15:0]		RX2(4)_q0[15:0]	

Figure 579. JESD204B/C Frame Format for RX Chain: L-M-F-S-Hd = 14810 (Two Links, 1 Link per Pair of RX Chains)

Octet	1	2	3	4
Lane 1	RX1_i0[15:0]		RX1_q0[15:0]	
Lane 2	RX2_i0[15:0]		RX2_q0[15:0]	
Lane 3	RX3_i0[15:0]		RX3_q0[15:0]	
Lane 4	RX4_i0[15:0]		RX4_q0[15:0]	

Figure 580. JESD204B/C Frame Format for RX Chain: L-M-F-S-Hd = 48410 (One Link)

Octet	1	2	3	4
Lane 1	RX1(3)_i0[15:0]		RX1(3)_q0[15:0]	
Lane 2	RX2(4)_i0[15:0]		RX2(4)_q0[15:0]	

Figure 581. JESD204B/C Frame Format for RX Chain: L-M-F-S-Hd = 24410 (Two Links, 1 Link per Pair of RX Chains)

Octet	1	2	3	4	5	6	7	8	9	10	11	12
Lane 1	RX1_i0[15:0]		Zeros [7:0]	RX1_q0[15:0]		Zeros [7:0]	RX2_i0[15:0]		Zeros [7:0]	RX2_q0[15:0]		Zeros [7:0]
Octet	13	14	15	16	17	18	19	20	21	22	23	24
Lane 1	RX3_i0[15:0]		Zeros [7:0]	RX3_q0[15:0]		Zeros [7:0]	RX4_i0[15:0]		Zeros [7:0]	RX4_q0[15:0]		Zeros [7:0]

Figure 582. JESD204B/C Frame Format for RX Chain: L-M-F-S-Hd = 1-8-24-1-0 (One Link)

Octet	1	2	3	4	5	6	7	8	9	10	11	12
Lane 1	RX1_i0[15:0]		Zeros [7:0]	RX1_q0[15:0]		Zeros [7:0]	RX2_i0[15:0]		Zeros [7:0]	RX2_q0[15:0]		Zeros [7:0]
Lane 2	RX3_i0[15:0]		Zeros [7:0]	RX3_q0[15:0]		Zeros [7:0]	RX4_i0[15:0]		Zeros [7:0]	RX4_q0[15:0]		Zeros [7:0]

Figure 583. JESD204B/C Frame Format for RX Chain: L-M-F-S-Hd = 2-8-12-1-0 (One Link)

Octet	1	2	3	4	5	6	7	8	9	10	11	12
Lane 1	RX1(3)_i0[15:0]		Zeros [7:0]	RX1(3)_q0[15:0]		Zeros [7:0]	RX2(4)_i0[15:0]		Zeros [7:0]	RX2(4)_q0[15:0]		Zeros [7:0]

Figure 584. JESD204B/C Frame Format for RX Chain: L-M-F-S-Hd = 1-4-12-1-0 (Two Links, 1 Link Per Pair of RX Chains)

Octet	1	2	3	4	5	6
Lane 1	RX1_i0[15:0]		Zeros [7:0]	RX1_q0[15:0]		Zeros [7:0]
Lane 2	RX2_i0[15:0]		Zeros [7:0]	RX2_q0[15:0]		Zeros [7:0]
Lane 3	RX3_i0[15:0]		Zeros [7:0]	RX3_q0[15:0]		Zeros [7:0]
Lane 4	RX4_i0[15:0]		Zeros [7:0]	RX4_q0[15:0]		Zeros [7:0]

Figure 585. JESD204B/C Frame Format for RX Chain: L-M-F-S-Hd = 48610 (One Link)

Octet	1	2	3	4	5	6
Lane 1	RX1(3)_i0[15:0]		Zeros [7:0]	RX1(3)_q0[15:0]		Zeros [7:0]
Lane 2	RX2(4)_i0[15:0]		Zeros [7:0]	RX2(4)_q0[15:0]		Zeros [7:0]

Figure 586. JESD204B/C Frame Format for RX Chain: L-M-F-S-Hd = 24610 (Two Links, 1 Link Per Pair of RX Chains)

Octet	1	2	3	4	5	6	7	8	9	10	11	12
Lane 1	RX1_i0[15:4]		RX1_q0[15:4]		RX2_i0[15:4]		RX2_q0[15:4]		RX3_i0[15:4]		RX3_q0[15:4]	
	RX4_i0[15:4]		RX4_q0[15:4]									

Figure 587. JESD204B/C Frame Format for RX Chain: L-M-F-S-Hd = 1-8-12-1-0 (One Link)

Octet	1	2	3	4	5	6
Lane 1	RX1_i0[15:4]	RX1_q0[15:4]		RX2_i0[15:4]	RX2_q0[15:4]	
Lane 2	RX3_i0[15:4]	RX3_q0[15:4]		RX4_i0[15:4]	RX4_q0[15:4]	

Figure 588. JESD204B/C Frame Format for RX Chain: L-M-F-S-Hd = 28610 (One Link)

Octet	1	2	3	4	5	6
Lane 1	RX1(3)_i0[15:4]	RX1(3)_q0[15:4]		RX2(4)_i0[15:4]	RX2(4)_q0[15:4]	

Figure 589. JESD204B/C Frame Format for RX Chain: L-M-F-S-Hd = 14610 (Two Links, 1 Link Per Pair of RX Chains)

Octet	1	2	3
Lane 1	RX1(3)_i0[15:4]	RX1(3)_q0[15:4]	
Lane 2	RX2(4)_i0[15:4]	RX2(4)_q0[15:4]	

Figure 590. JESD204B/C Frame Format for RX Chain: L-M-F-S-Hd = 24310 (Two Links, 1 Link Per Pair of RX Chains)

Octet	1	2	3
Lane 1	RX1_i0[15:4]	RX1_q0[15:4]	
Lane 2	RX2_i0[15:4]	RX2_q0[15:4]	
Lane 3	RX3_i0[15:4]	RX3_q0[15:4]	
Lane 4	RX4_i0[15:4]	RX4_q0[15:4]	

Figure 591. JESD204B/C Frame Format for RX Chain: L-M-F-S-Hd = 48310 (One Link)

Octet	1	2
Lane 1	RX1(3)_i0[15:0]	
Lane 2	RX1(3)_q0[15:0]	
Lane 3	RX2(4)_i0[15:0]	
Lane 4	RX2(4)_q0[15:0]	

Figure 592. JESD204B/C Frame Format for RX Chain: L-M-F-S-Hd = 44210 (Two Links, 1 Link Per Pair of RX Chains)

Octet	1	2	3	4	5	6	7	8
Lane 1	RX1_i0[15:0]		Zeros [15:0]		RX1_q0[15:0]		Zeros [15:0]	
Octet	9	10	11	12	13	14	15	16
Lane 1	RX2_i0[15:0]		Zeros [15:0]		RX2_q0[15:0]		Zeros [15:0]	
Octet	17	18	19	20	21	22	23	24
Lane 1	RX3_i0[15:0]		Zeros [15:0]		RX3_q0[15:0]		Zeros [15:0]	
Octet	25	26	27	28	29	30	31	32
Lane 1	RX4_i0[15:0]		Zeros [15:0]		RX4_q0[15:0]		Zeros [15:0]	

Figure 593. JESD204B/C Frame Format for RX Chain: L-M-F-S-Hd = 1-8-32-1-0 (One Link)

Table 15. JESD204B/C Formats For 2 DDCs per RX Chain

OUTPUT RATE [MSPS]	OUTPUT RESOLUTION	ENCODING	SERDES RATE [Gbps]	L-M-F-S-Hd 1 LINK	L-M-F-S-Hd 2 LINKS
61.44	16	8/10b	19.6608	1-16-32-1-0	
	16	64/66b	16.22016	1-16-32-1-0	
	16	8/10b	9.8304	2-16-16-1-0	1-8-16-1-0
	16	64/66b	8.11008	2-16-16-1-0	1-8-16-1-0
	24	8/10b	14.7456	2-16-24-1-0	1-8-24-1-0
	24	64/66b	12.16512	2-16-24-1-0	1-8-24-1-0
92.16	16	8/10b	14.7456	2-16-16-1-0	1-8-16-1-0
	16	64/66b	12.16512	2-16-16-1-0	1-8-16-1-0
	16	64/66b	24.33024	1-16-32-1-0	
	24	8/10b	22.1186	2-16-24-1-0	1-8-24-1-0
122.88	16	8/10b	19.6608	2-16-16-1-0	1-8-16-1-0
	16	8/10b	9.8304	4-16-8-1-0	2-8-8-1-0
	16	64/66b	16.22016	2-16-16-1-0	1-8-16-1-0
	16	64/66b	8.11008	4-16-8-1-0	2-8-8-1-0
	24	64/66b	24.33024	2-16-24-1-0	1-16-24-1-0
184.32	16	8/10b	29.4912	2-16-16-1-0	1-8-16-1-0
	16	8/10b	14.7456	4-16-8-1-0	2-8-8-1-0
	16	64/66b	24.33024	2-16-16-1-0	1-8-16-1-0
	16	64/66b	12.16512	4-16-8-1-0	2-8-8-1-0
245.76	16	8/10b	19.6608	4-16-8-1-0	2-8-8-1-0
	16	8/10b	9.8304	8-16-4-1-0	4-8-4-1-0
	16	64/66b	16.22016	4-16-8-1-0	2-8-8-1-0
	16	64/66b	8.11008	8-16-4-1-0	4-8-4-1-0
	12	64/66b	24.33024	2-16-6-1-0	1-8-6-1-0
	12	64/66b	12.16512	4-16-6-1-0	2-8-6-1-0
	24	64/66b	24.33024	4-16-6-1-0	2-8-6-1-0
368.64	16	8/10b	29.4912	4-16-8-1-0	2-8-8-1-0
	16	8/10b	14.7456	8-16-4-1-0	4-8-4-1-0
	16	64/66b	24.33024	4-16-8-1-0	2-8-8-1-0
	16	64/66b	12.16512	8-16-4-1-0	4-8-4-1-0

9.3.8.3.2.1 JESD204B/C Frame Assembly for Feedback Chain

The feedback chains support multiple JESD204B/C modes, listed in Table 16. In AFE7921/AFE7989, the maximum output data rate of feedback chain is 491.52MSPS.

Table 16. JESD204B/C Formats for Feedback Chain

OUTPUT RATE [MSPS]	RESOLUTION	ENCODING	SERDES RATE [Gbps]	L-M-F-S-Hd 1 LINK	L-M-F-S-Hd 2 LINKS	PAIRED RX JESD MODE FOR SHARED SERDES		AVAILABLE IN AFE7921/AFE7989?
						L-M-F-S-Hd	OUTPUT RATE	
122.88	12	8/10b	7.3728	1-4-6-1-0				Yes
	16	8/10b	9.8304	1-4-8-1-0				Yes
	16	8/10b	9.8304	1-4-16-2-0		1-8-16-1-0	61.44	Yes
	32	8/10b	19.6608	1-4-16-1-0				Yes
	32	64/66b	16.2208	1-4-16-1-0				Yes
	16	64/66b	8.1104	1-4-8-1-0				Yes
	24	8/10b	14.7456	1-4-12-1-0				Yes
	24	64/66b	12.16512	1-4-12-1-0				Yes
184.32	12	8/10b	11.0592	1-4-6-1-0				Yes
	16	8/10b	14.7456	1-4-8-1-0				Yes
	16	8/10b	7.3728	2-4-4-1-0	1-2-4-1-0			Yes
	16	8/10b	7.3728	2-4-8-2-0		2-8-8-1-0	92.16	Yes
	16	64/66b	12.16512	1-4-8-1-0				Yes
	16	8/10b	14.7456	1-4-16-2-0		1-8-16-1-0	92.16	Yes
	24	8/10b	22.1184	1-4-12-1-0				Yes
	24	8/10b	11.0592	2-4-6-1-0	1-2-6-1-0			Yes
245.76	12	64/66b	16.2208	1-4-12-1-0				Yes
	16	8/10b	19.6608	1-4-8-1-0				Yes
	16	8/10b	19.6608	1-4-16-2-0		2-16-16-1-0	122.88	Yes
	16	8/10b	9.8304	2-4-4-1-0	1-2-4-1-0			Yes
	16	8/10b	9.8304	2-4-8-2-0	1-2-8-2-0	2-8-8-1-0	122.88	Yes
	16	64/66b	16.22016	1-4-8-1-0				Yes
	16	64/66b	16.22016	1-4-16-2-0		2-16-16-1-0	122.88	Yes
	16	64/66b	8.11008	2-4-4-1-0	1-2-4-1-0			Yes
	16	64/66b	8.11008	2-4-8-2-0	1-2-8-2-0	2-8-8-1-0	122.88	Yes
	24	64/66b	24.33024	1-4-24-2-0		2-16-24-1-0	122.88	Yes
368.64	16	8/10b	29.4912	1-4-8-1-0				Yes
	16	8/10b	29.4912	1-4-16-2-0		1-8-16-1-0	184.32	Yes
						2-16-16-1-0	184.32	Yes
	16	8/10b	14.7456	2-4-4-1-0	1-2-4-1-0			Yes
	16	8/10b	14.7456	2-4-8-2-0	1-2-8-2-0	2-8-8-1-0	184.32	Yes
						4-16-8-1-0	184.32	Yes
	16	8/10b	7.3728	4-4-2-1-0	2-2-2-1-0			Yes
	16	8/10b	7.3728	4-4-4-2-0	2-2-4-2-0			Yes
	16	64/66b	24.33024	1-4-8-1-0				Yes
	16	64/66b	24.33024	1-4-16-2-0		1-8-16-1-0	184.32	Yes
						2-16-16-1-0	184.32	Yes
	16	64/66b	12.16512	2-4-4-1-0	1-2-4-1-0			Yes
	16	64/66b	12.16512	2-4-8-2-0	1-2-8-2-0	2-8-8-1-0	184.32	Yes
						4-16-8-1-0	184.32	Yes
	16	64/66b	6.08256	4-4-2-1-0	2-2-2-1-0			Yes
	16	64/66b	6.08256	4-4-4-2-0	2-2-4-2-0			Yes
	32	64/66b	24.33024	2-4-16-2-0	1-2-16-2-0	1-8-16-1-0	184.32	Yes
						2-16-16-1-0	184.32	Yes

Table 16. JESD204B/C Formats for Feedback Chain (continued)

OUTPUT RATE [MSPS]	RESOLUTION	ENCODING	SERDES RATE [Gbps]	L-M-F-S-Hd 1 LINK	L-M-F-S-Hd 2 LINKS	PAIRED RX JESD MODE FOR SHARED SERDES		AVAILABLE IN AFE7921/AFE7989?
						L-M-F-S-Hd	OUTPUT RATE	
491.52	16	8/10b	19.6608	2-4-4-1-0	1-2-4-1-0			Yes
	16	8/10b	19.6608	2-4-8-2-0	1-2-8-2-0	2-8-8-1-0	245.76	Yes
						4-16-8-1-0	245.76	Yes
	16	8/10b	9.8304	4-4-2-1-0	2-2-2-1-0			Yes
	16	8/10b	9.8304	4-4-4-2-0	2-2-4-2-0	4-8-4-1-0	245.76	Yes
						8-16-4-1-0	245.76	Yes
	16	64/66b	16.22016	2-4-4-1-0	1-2-4-1-0			Yes
	16	64/66b	16.22016	2-4-8-2-0	1-2-8-2-0	2-8-8-1-0	245.76	Yes
						4-16-8-1-0	245.76	Yes
	12	64/66b	24.33024	1-4-12-1-0		1-8-12-1-0	245.76	Yes
	12	64/66b	12.16512	2-4-6-1-0	1-2-6-1-0			Yes
	24	64/66b	24.33024	2-4-12-2-0	1-2-12-2-0	2-8-12-1-0	245.76	Yes
737.28	16	8/10b	29.4912	2-4-4-1-0	1-2-4-1-0			No
	16	8/10b	29.4912	2-4-8-2-0	1-2-8-2-0	2-8-8-1-0	368.64	No
						4-16-8-1-0	368.64	No
	16	8/10b	14.7456	4-4-2-1-0	2-2-2-1-0			No
	16	8/10b	14.7456	4-4-4-2-0	2-2-4-2-0	4-8-4-1-0	368.64	No
						8-16-4-1-0	368.64	No
	16	64/66b	24.33024	2-4-4-1-0	1-2-4-1-0			No
	16	64/66b	24.33024	2-4-8-2-0	1-2-8-2-0	2-8-8-1-0	368.64	No
						4-16-8-1-0	368.64	No
	16	64/66b	12.16512	4-4-4-2-0	2-2-4-2-0	4-8-4-1-0	368.64	No
						8-16-4-1-0	368.64	No
983.04	16	8/10b	19.6608	4-4-2-1-0	2-2-2-1-0			No
	16	8/10b	19.6608	4-4-4-2-0	2-2-4-2-0	4-8-4-1-0	491.52	No
	16	8/10b	9.8304	8-4-1-1-0	4-2-1-1-0			No
	16	8/10b	9.8304	8-4-2-2-0	4-2-2-2-0	8-8-2-1-0	491.52	No
	16	64/66b	16.22016	4-4-2-1-0	2-2-2-1-0			No
	16	64/66b	16.22016	4-4-4-2-0	2-2-4-2-0	4-8-4-1-0	491.52	No
	16	64/66b	8.11008	8-4-1-1-0	4-2-1-1-0			No
	16	64/66b	8.11008	8-4-2-2-0	4-2-2-2-0			No
	12	8/10b	29.4912	2-4-6-1-0	1-2-6-1-0	2-8-6-1-0	491.52	No
						4-8-6-1-0	491.52	No
	12	8/10b	14.7456	4-4-3-1-0	2-2-3-1-0			No
	12	64/66b	24.33024	2-4-6-1-0	1-2-6-1-0	2-8-6-1-0	491.52	No
						4-8-6-1-0	491.52	No
	12	64/66b	12.16512	4-4-3-1-0	2-2-3-1-0			No
	24	64/66b	24.33024	4-4-6-2-0	2-2-6-2-0	2-8-6-1-0	491.52	No
						4-8-6-1-0	491.52	No
1474.56	16	8/10b	29.4912	4-4-2-1-0	2-2-2-1-0			No
	16	8/10b	14.7456	8-4-2-1-0	4-2-2-1-0	8-8-2-1-0	737.28	No
	16	64/66b	24.33024	4-4-4-2-0	2-2-4-2-0	4-8-4-1-0	737.28	No
	16	64/66b	12.16512	8-4-2-1-0	4-2-2-1-0	8-8-2-1-0	737.28	No
	12	8/10b	22.1184	4-4-3-1-0	2-2-3-1-0			No

Table 17. JESD204B/C Formats for Feedback Chain

OUTPUT RATE [MSPS]	RESOLUTION	ENCODING	SERDES RATE [Gbps]	L-M-F-S-Hd 1 LINK	L-M-F-S-Hd 2 LINKS	PAIRED RX JESD MODE FOR SHARED SERDES	
						L-M-F-S-Hd	OUTPUT RATE
122.88	12	8/10b	7.3728	1-4-6-1-0			
	16	8/10b	9.8304	1-4-8-1-0			
	16	8/10b	9.8304	1-4-16-2-0		1-8-16-1-0	61.44
	32	8/10b	19.6608	1-4-16-1-0			
	32	64/66b	16.2208	1-4-16-1-0			
	16	64/66b	8.1104	1-4-8-1-0			
	24	8/10b	14.7456	1-4-12-1-0			
	24	64/66b	12.16512	1-4-12-1-0			
184.32	12	8/10b	11.0592	1-4-6-1-0			
	16	8/10b	14.7456	1-4-8-1-0			
	16	8/10b	7.3728	2-4-4-1-0	1-2-4-1-0		
	16	8/10b	7.3728	2-4-8-2-0		2-8-8-1-0	92.16
	16	64/66b	12.16512	1-4-8-1-0			
	16	8/10b	14.7456	1-4-16-2-0		1-8-16-1-0	92.16
	24	8/10b	22.1184	1-4-12-1-0			
	24	8/10b	11.0592	2-4-6-1-0	1-2-6-1-0		
245.76	12	64/66b	16.2208	1-4-12-1-0			
	16	8/10b	19.6608	1-4-8-1-0			
	16	8/10b	19.6608	1-4-16-2-0		2-16-16-1-0	122.88
	16	8/10b	9.8304	2-4-4-1-0	1-2-4-1-0		
	16	8/10b	9.8304	2-4-8-2-0	1-2-8-2-0	2-8-8-1-0	122.88
	16	64/66b	16.22016	1-4-8-1-0			
	16	64/66b	16.22016	1-4-16-2-0		2-16-16-1-0	122.88
	16	64/66b	8.11008	2-4-4-1-0	1-2-4-1-0		
	16	64/66b	8.11008	2-4-8-2-0	1-2-8-2-0	2-8-8-1-0	122.88
	24	64/66b	24.33024	1-4-24-2-0		2-16-24-1-0	122.88
368.64	16	8/10b	29.4912	1-4-8-1-0			
	16	8/10b	29.4912	1-4-16-2-0		1-8-16-1-0	184.32
						2-16-16-1-0	184.32
	16	8/10b	14.7456	2-4-4-1-0	1-2-4-1-0		
	16	8/10b	14.7456	2-4-8-2-0	1-2-8-2-0	2-8-8-1-0	184.32
						4-16-8-1-0	184.32
	16	8/10b	7.3728	4-4-2-1-0	2-2-2-1-0		
	16	8/10b	7.3728	4-4-4-2-0	2-2-4-2-0		
	16	64/66b	24.33024	1-4-8-1-0			
	16	64/66b	24.33024	1-4-16-2-0		1-8-16-1-0	184.32
						2-16-16-1-0	184.32
	16	64/66b	12.16512	2-4-4-1-0	1-2-4-1-0		
	16	64/66b	12.16512	2-4-8-2-0	1-2-8-2-0	2-8-8-1-0	184.32
						4-16-8-1-0	184.32
	16	64/66b	6.08256	4-4-2-1-0	2-2-2-1-0		
	16	64/66b	6.08256	4-4-4-2-0	2-2-4-2-0		
	32	64/66b	24.33024	2-4-16-2-0	1-2-16-2-0	1-8-16-1-0	184.32
						2-16-16-1-0	184.32

Table 17. JESD204B/C Formats for Feedback Chain (continued)

OUTPUT RATE [MSPS]	RESOLUTION	ENCODING	SERDES RATE [Gbps]	L-M-F-S-Hd 1 LINK	L-M-F-S-Hd 2 LINKS	PAIRED RX JESD MODE FOR SHARED SERDES	
						L-M-F-S-Hd	OUTPUT RATE
491.52	16	8/10b	19.6608	2-4-4-1-0	1-2-4-1-0		
	16	8/10b	19.6608	2-4-8-2-0	1-2-8-2-0	2-8-8-1-0	245.76
						4-16-8-1-0	245.76
	16	8/10b	9.8304	4-4-2-1-0	2-2-2-1-0		
	16	8/10b	9.8304	4-4-4-2-0	2-2-4-2-0	4-8-4-1-0	245.76
						8-16-4-1-0	245.76
	16	64/66b	16.22016	2-4-4-1-0	1-2-4-1-0		
	16	64/66b	16.22016	2-4-8-2-0	1-2-8-2-0	2-8-8-1-0	245.76
						4-16-8-1-0	245.76
	12	64/66b	24.33024	1-4-12-1-0		1-8-12-1-0	245.76
	12	64/66b	12.16512	2-4-6-1-0	1-2-6-1-0		
	24	64/66b	24.33024	2-4-12-2-0	1-2-12-2-0	2-8-12-1-0	245.76
737.28	16	8/10b	29.4912	2-4-4-1-0	1-2-4-1-0		
	16	8/10b	29.4912	2-4-8-2-0	1-2-8-2-0	2-8-8-1-0	368.64
						4-16-8-1-0	368.64
	16	8/10b	14.7456	4-4-2-1-0	2-2-2-1-0		
	16	8/10b	14.7456	4-4-4-2-0	2-2-4-2-0	4-8-4-1-0	368.64
						8-16-4-1-0	368.64
	16	64/66b	24.33024	2-4-4-1-0	1-2-4-1-0		
	16	64/66b	24.33024	2-4-8-2-0	1-2-8-2-0	2-8-8-1-0	368.64
						4-16-8-1-0	368.64
	16	64/66b	12.16512	4-4-4-2-0	2-2-4-2-0	4-8-4-1-0	368.64
						8-16-4-1-0	368.64
983.04	16	8/10b	19.6608	4-4-2-1-0	2-2-2-1-0		
	16	8/10b	19.6608	4-4-4-2-0	2-2-4-2-0	4-8-4-1-0	491.52
	16	8/10b	9.8304	8-4-1-1-0	4-2-1-1-0		
	16	8/10b	9.8304	8-4-2-2-0	4-2-2-2-0	8-8-2-1-0	491.52
	16	64/66b	16.22016	4-4-2-1-0	2-2-2-1-0		
	16	64/66b	16.22016	4-4-4-2-0	2-2-4-2-0	4-8-4-1-0	491.52
	16	64/66b	8.11008	8-4-1-1-0	4-2-1-1-0		
	16	64/66b	8.11008	8-4-2-2-0	4-2-2-2-0		
	12	8/10b	29.4912	2-4-6-1-0	1-2-6-1-0	2-8-6-1-0	491.52
						4-8-6-1-0	491.52
	12	8/10b	14.7456	4-4-3-1-0	2-2-3-1-0		
	12	64/66b	24.33024	2-4-6-1-0	1-2-6-1-0	2-8-6-1-0	491.52
						4-8-6-1-0	491.52
	12	64/66b	12.16512	4-4-3-1-0	2-2-3-1-0		
	24	64/66b	24.33024	4-4-6-2-0	2-2-6-2-0	2-8-6-1-0	491.52
						4-8-6-1-0	491.52
1474.56	16	8/10b	29.4912	4-4-2-1-0	2-2-2-1-0		
	16	8/10b	14.7456	8-4-2-1-0	4-2-2-1-0	8-8-2-1-0	737.28
	16	64/66b	24.33024	4-4-4-2-0	2-2-4-2-0	4-8-4-1-0	737.28
	16	64/66b	12.16512	8-4-2-1-0	4-2-2-1-0	8-8-2-1-0	737.28
	12	8/10b	22.1184	4-4-3-1-0	2-2-3-1-0		

9.3.9 Sharing SerDes Lanes

For base stations operating in TDD modes, downlink and uplink time-share the same frequency band. During the downlink slot, transmitters are active often along with feedback observation receivers (FB) to monitor the TX output for various purposes (ex: to assist the Digital Pre-distortion algorithm for Power Amplifier linearization). In uplink time slots transmitters along with the feedback observation receivers are typically inactive, and traffic receivers (RX) are active. AFE79xx supports the timesharing of same SerDes TX lanes between the RX and FB chains to optimize the use of the SerDes lanes and the power consumption of the device. This mode is enabled through the SPI. Then the dynamic switching between the RX chains and the FB path connection to the shared SerDes lanes is controlled using the RX and FB enable GPIO pins according to Table 18.

Table 18. RX/FB SerDes Sharing Switch Control

RXEN1/2[(b)]	1FBEN	RX CHAINS	FB CHAIN	SerDes LANES TO
1	0	On	Off	RX
0	1	Off	On	FB
1	1	On/Off	On/Off	RX/FB [(a)]
0	0	Off	Off	
(a) (1,1) case same as (1,0) or (0,1) based on a programmable configuration				
(b) Possible to select through the SPI which RXEN to use				

9.3.10 Low-Speed Digital I/O Configuration

The AFE79xx supports multiple modes where controls and data exchange happen through several allocated Low-Speed Digital I/O (GPIO) pins. Because the required I/Os by all supported modes exceeds the number of available pins, there are several pins that can be configured differently based on the active mode. All the allocated pins for low-speed I/O (GPIO) are shown in the ballmap (see *Pin Configuration and Functions*).

The AFE79xx supports flexible assignment of the GPIO functions to GPIO balls. However, some functions are fixed to certain balls, and other functions are only recommended and ensured for certain ballsTable 19.

Table 19. Fixed and Recommended GPIO Functions

TYPE	FUNCTION	BALL NAMES
Fixed	JTAG	GTR_13_TRST
		GTR_18_TDI
		GTR_4_TCLK
		GTR_5_TDO
		GTR_10_TMS
		GTL_10_BIST0
		GTL_12_BIST1
	SPI A	GTL_17_SPIASDIO
		GTL_18_SPIASDO
		GTL_4_SPIACLK
		GTL_5_SPIASEN
Recommended	SPI B1	GTR_11_SPIB1_SDO
		GTR_12_SPIB1_SDIO
		GTR_14_SPIB1SEN
		GTR_17_SPIB1CLK
	SPI B2	GTR_2_SPIB2CLK
		GTR_6_SPIB2_SDIO
		GTR_7_SPIB2SEN
		GTR_9_SPIB2SDO

The GPIO functions supported by the device are listed in Table 20.

Table 20. GPIO Functions

FUNCTION	# OF BALLS
Default (functions available after chip reset)	
JTAG	5 total (plus BIST0 and BIST1)
SPI A, SPI B1, SPI B2	12 total, 4 each
TDD switches	10 total, 4 each for TX, RX and 2 for FB
LNA Bypass	4 total, 1 each for each RX
Reset	1
JESD SYNC\ In	4 total, 2 x differential or 4x single ended
JESD SYNC\ Out	4 total, 2 x differential or 4x single ended
Other Available Functions	
Internal DSA control	12 total, 3 per RX
External DVGA control	6 total, 3 per RX 1/2 and 3/4
AGC Freeze	4 total, 1 per RX
NCO Select	10 total, 1 per TX, RX and FB
RX Peak Detectors	16 total, 4 per RX
RX Reliability Detectors	8 total, 2 per RX
DSA Swap	1 per TX, 1 per RX, 1 per FB

9.3.11 Available Alarms

Several alarms from different blocks can be enabled and monitored by AFE79xx. Some of them can be configured to trigger the PA protection feature (PAP Triggers) and or generate an interrupt signal. The device has two interrupt pins (INT1 and INT2). Through the SPI it is possible to configure which alarms can trigger the interrupt signal on each of the two pins. The list of all alarms available in the device is included in Table 21.

Table 21. Alarm List

ALARM	BLOCK	NOTES
SerDes PLL unlock	SerDes	SerDes PLL becomes unlocked. One per SerDes block (group of four transceivers)
Loss of signal detection	SerDes	SerDes does not detect any more signal transition
Frame Sync Error	JESD204B	Ctrl-K in middle of data
Multiframe alignment error	JESD204B	Failure in multi-frame alignment
Frame alignment error	JESD204B	Failure in frame alignment
Link configuration error	JESD204B	Wrong link configuration
Elastic buffer match error	JESD204B	First non-/K/ does not match the programmed data
Code synchronization error	JESD204B	
8b/10b not-in-table code error	JESD204B	
8b/10b disparity error	JESD204B	
Frame sync error	JESD204B	a /K/ symbol is detect while receiving data (8b/10b encoding)
Short pattern check	JESD204B	short pattern test fails.
Elastic buffer overflow	JESD204B/C	Bad RBD value
Frame Sync Error	JESD204C	Fixed ones error
Invalid SYNC Header	JESD204C	Wrong header is detected - '11' or '00'
CRC error	JESD204C	Error detected in the supported CRC3 or CRC12
EoEMB error	JESD204C	Wrong End of Extended Multi-Bock detected
EoMB error	JESD204C	Wrong End of Multi-Bock detected
CMD data not matching SPI register	JESD204C	cmd-data in CRC mode not matching with spi register bits
Header Parity Check	JESD204C	Parity error detected

Table 21. Alarm List (continued)

ALARM	BLOCK	NOTES
PLL unlock	PLL	Separate lock detect alarms for each RF and DC PLL
SPI conflict	SPI	Register access conflict between the two SPI
TX digital chain FIFO overflow	TX dig block	One FIFO overflow alarm for each of TX digital chain
RX digital chain FIFO overflow	RX dig block	One FIFO overflow alarm for each of RX digital chain
FB digital chain FIFO overflow	FB dig block	One FIFO overflow alarm for each of FB digital chain
Macro Complete	SPI	Macro execution is completed
Macro error	SPI	Macro terminated with an error
Input Signal Error	PAP block	Trigger from incoming signal measurements (average power or programmable filter power; see *TX PA Protection*)

9.3.12 TX and RX DSA Gain and Phase Error Calibration

The AFE79xx TX and RX DSA steps mismatch in amplitude and phase can be compensated through a dedicated calibration procedure. Such calibration should be performed once for each device on the final assembled board, because the actual source and load impedance seen by the device can affect the phase and amplitude mismatch. TI suggests to perform this calibration on the final assembled board at the customer factory for this reason.

The AFE79xx, during the calibration, computes and stores internally the gain and phase compensation parameters for all the 4 TX and 4 RX chains. At the end of calibration procedure, the host needs to read the calibration tables from the device internal memory and store in a non-volatile memory. The estimated calibration data packet size for 4 RX channels is approximately 1000 bytes, while the estimated calibration data packet size fo r4 TX channels is approximately 800 bytes.

When the device is used in normal mode, during the configuration, the host has to download the calibrations tables into the AFE79xx internal memory. These tables will then be used by the device to compensate the gain/phase errors of the DSA steps.

9.3.13 Auxiliary Low-Speed ADC

The device integrates a 12-bit, 200-ksps differential SAR ADC to enable the monitoring of external DC or low-speed signals. The ADC inputs are multiplexed to 6 pins on the package, to allow the measurements of multiple signals. The digital output words are accessed through the SPI.

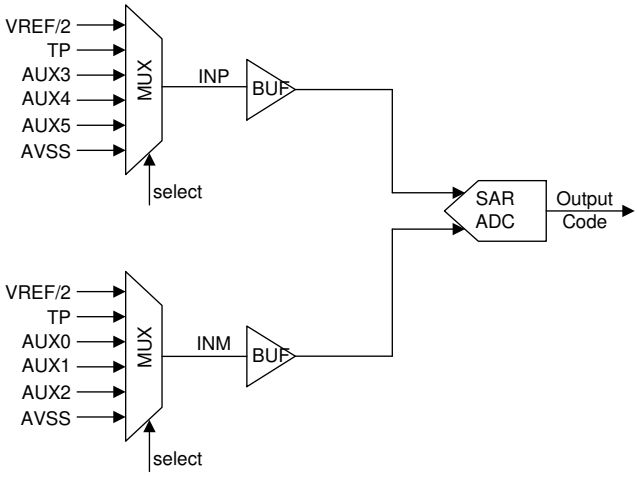


Figure 594. Auxiliary ADC Block Diagram

As shown in the block diagram, the differential ADC inputs can be connected through a multiplex to:

- the 6 package pins indicated as *_AUX0 through *_AUX5;
- $V_{REF}/2$ or
- Ground (AVSS).

V_{REF}/2, AVSS and TP are internal connections (TP are internal test points for debugging).V_{REF} is typically 1.4 V and it is generated internally. The SAR ADC samples the signals at its differential inputs. As such, by the correct configuration of the multiplex, it is possible to measure the level at any of the AUX input pins with reference to V_{REF}/2, ground or another AUX input. The ADC output code word is related to the input voltages by the following formula:

$$\frac{V_{INP} - V_{INM}}{V_{REF}} = \frac{2 * code + 1 - 4096}{4096} \quad (3)$$

The following 3 plots show the expected output code as function of the input voltage in 3 different measurement modes: differential, single-ended with other side connected to VREF/2; single-ended with the other side connected to ground.

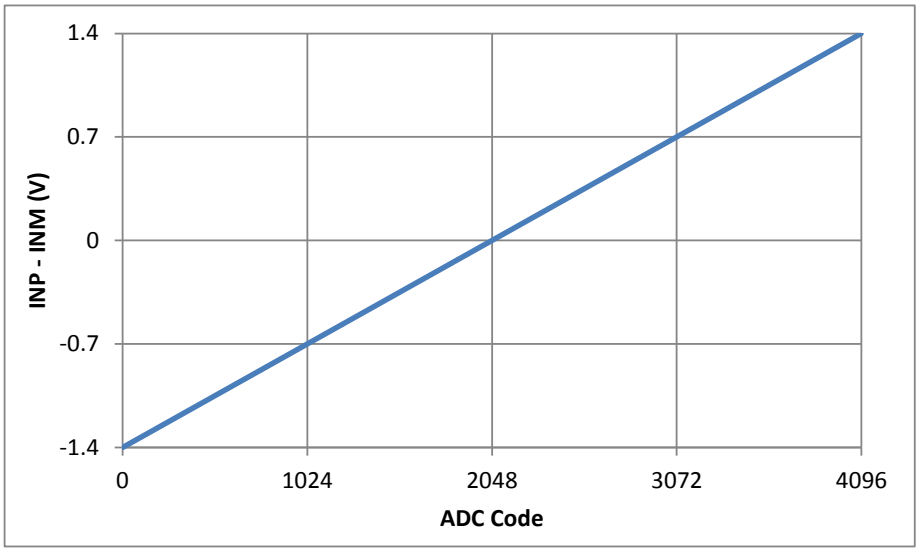


Figure 595. Input Differential Voltage vs Auxiliary ADC Output Code

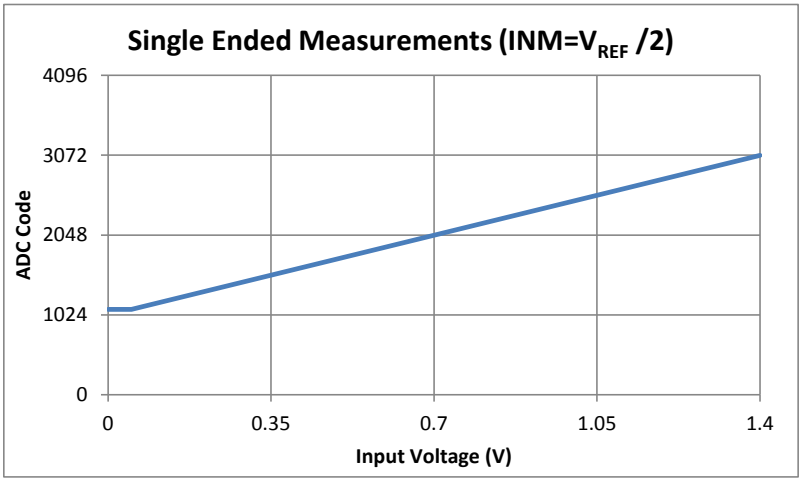


Figure 596. Auxiliary ADC Output Code vs Single-Ended Input (V_{REF}/2 Reference)

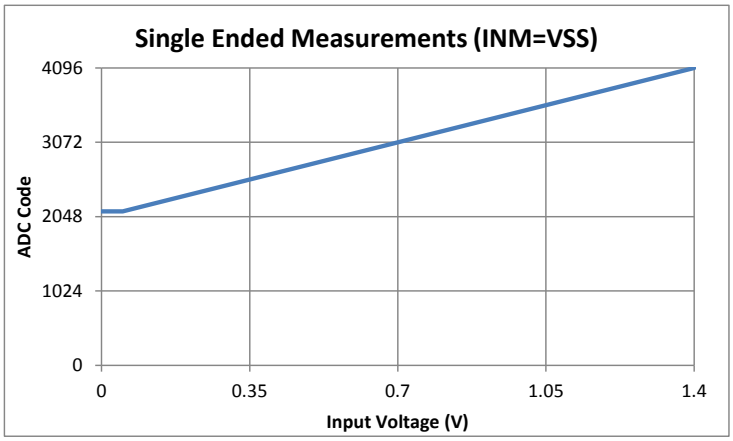


Figure 597. Auxiliary ADC Output Code vs Single-Ended Input (Ground Reference)

9.3.14 Serial Peripheral Interface (SPI)

The serial port of the AFE79xx is a flexible serial interface which communicates with industry standard microprocessors and microcontrollers. The interface provides read/write access to all registers used to define the operating modes of the AFE79xx. It is compatible with most synchronous transfer formats and can be configured as a 3 or 4 terminal interface through register field GLOBAL_4PIN in global register GLOBAL0. In both configurations, SCLK is the serial interface input clock and SDEN\ is serial interface enable. For 3 terminal configuration, SDIO is a bidirectional terminal for both data in and data out. For 4 terminal configuration, SDIO is bidirectional and SDO is data out only. Data is input into the device with the rising edge of SCLK. Data is output from the device on the falling edge of SCLK. The SPI registers except for global register GLOBAL0 and GLOBAL1 are reset by writing a "1" to GLOBAL_SOFT_RESET in the global register GLOBAL0.

Each read/write operation is framed by signal SDEN\ (Serial Data Enable Bar) asserted low. The first two bytes is the instruction cycle which identifies the following data transfer cycle as read or write as well as the 15-bit address to be accessed. The data transfer cycle consists of one byte. There are 64 pages of registers in the AFE79xx and address 0x00h-0x1Fh are assigned for global registers in every page. The particular register page is selected by writing "1" to the corresponding page selection bits through field GLOBAL_PAGE_SEL in the global register GLOBAL_PAGE_SEL0-GLOBAL_PAGE_SEL7 (address 0x10h-0x15h).

The AFE79xx includes two additional SPI interfaces (SPIB1, SPIB2)) with identical functions as the main SPI. The three SPIs can be accessed simultaneously as long as the accessed registers are not in the same page. Both main SPI and SPI-B1/2 also support streaming reads/writes and broadcasting as shown below. The address automatically increments or decrements depends on the setting of register field GLOBAL_ASCEND. The streaming addressing formation depends on the setting of register field GLOBAL_ADDRESSING_TYPE. Figure 598 and Figure 599 show the timing of a regular SPI write and read cycle. Figure 600 and Figure 601 show an example of SPI streaming write and read. Figure 602 and Figure 603 show the timing diagram of SPI write and read.

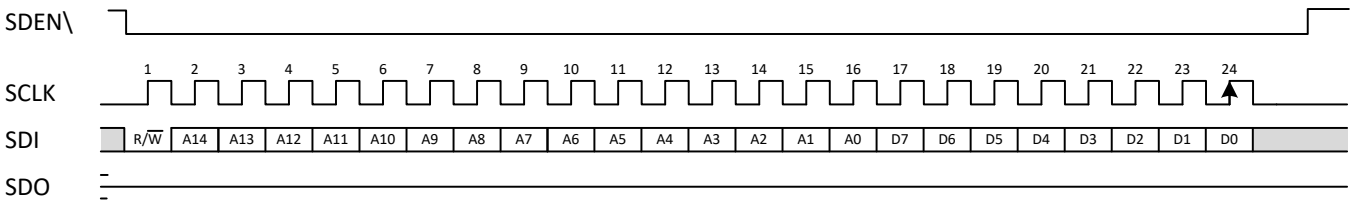


Figure 598. SPI Write Bus Cycle

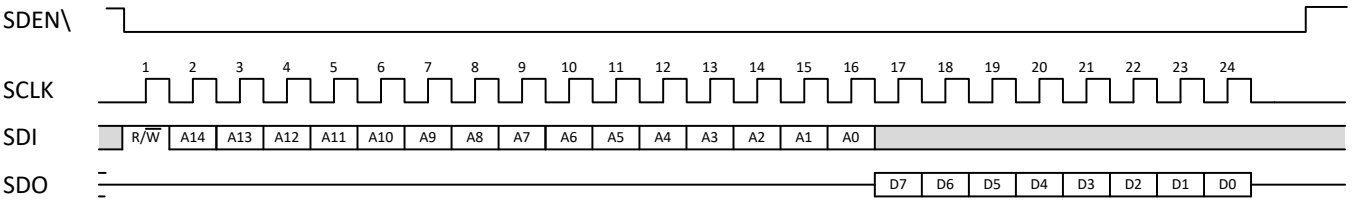


Figure 599. SPI Read Bus Cycle

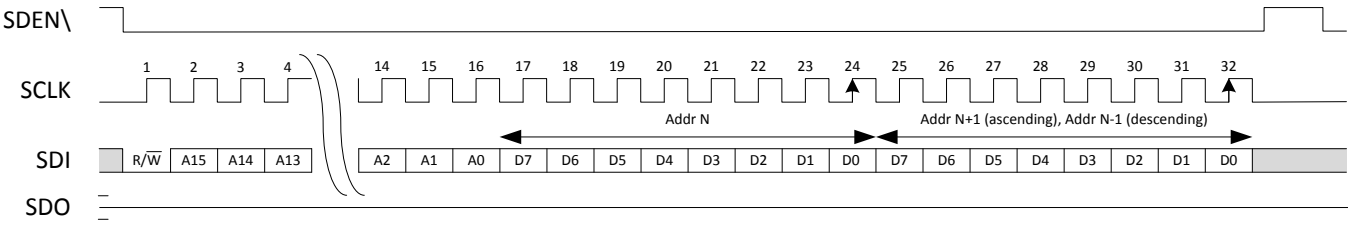


Figure 600. SPI Streaming Write Example

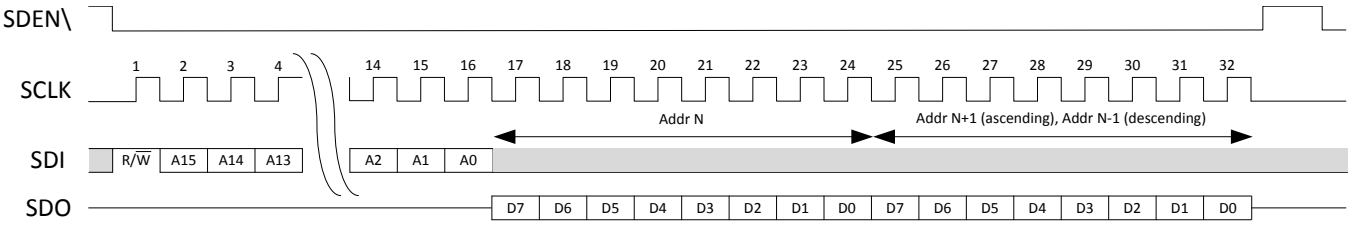


Figure 601. SPI Streaming Read Example

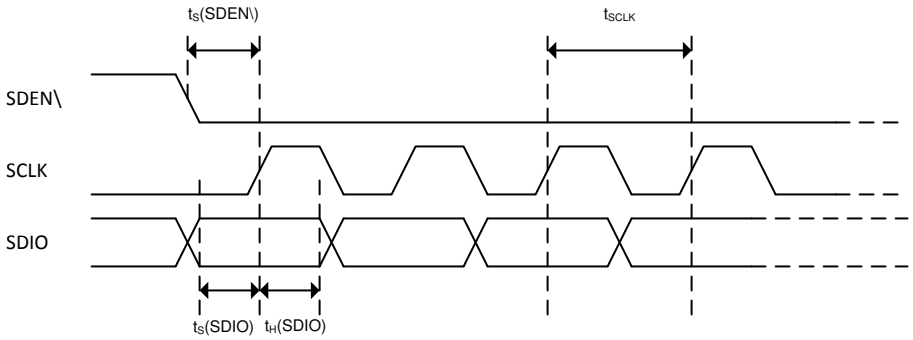


Figure 602. SPI Write Timing Diagram

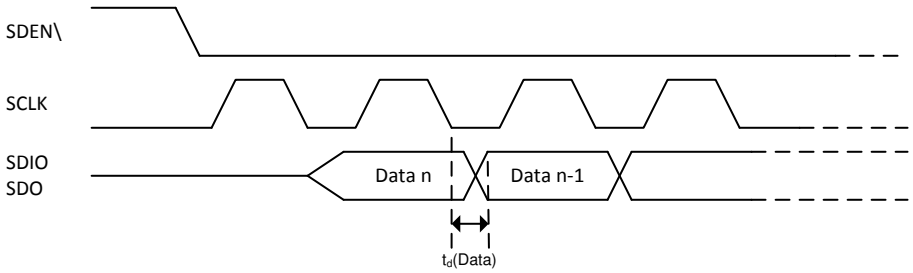


Figure 603. SPI Read Timing Diagram

9.4 Device Functional Modes

The AFE79xx supports very flexible configuration on the device functional modes. Each 2T2R1F half of the device can be configured independently. Each transmitter and receiver can work in Active Mode, Standby Mode, or Sleep Mode. With the transmitter and receiver in different operating modes, the whole device can operate at various functional modes:

- TDD mode with separate FB paths (AFE792x only)
- TDD mode with shared RX/FB ADCs and dynamic switching
- FDD mode with separate FB paths (AFE792x only)
- Transmitter only mode
- Receiver only mode

Note that all the above functional modes are configured separated for each 2T2R or 2T2R1F group. The status between standby and active for the TX/FB and RX channels are controlled by up to 10 GPIO functions, one per TX (TXTDDn, n = 1-4), RX (RXTDDn, n = 1-4) and FB (FBTDDn, n = 1-2) channels.

9.4.1 TDD Mode With Separate FB Paths AFE792x Only

In this mode, the FB and RX channels use separate ADCs. The TX/FB and RX channels are switched between active and standby states with the GPIO functions TXTDD, RXTDD, and FBTDD.

Note that the TDD control GPIOs pins are not mutually exclusive, so it is possible that for a certain period to time, both transmitters and receivers are in Active mode.

9.4.2 TDD Mode With Shared RX/FB ADCs and Dynamic Switching

In this mode, the RX and FB share the RX ADC and switches between the RX and FB DDCs using the TXTDDn, RXTDDn, and FBTDDn GPIO functions. It is also possible that both RX and FB are in standby states to save power if the FB channel is not needed.

9.4.3 FDD Mode With Separate FB Paths AFE792x Only

In this mode, the FB and RX channels use separate ADCs. Typically the TX and RX channels would be always active, with the FB channel possibly being toggled between the active and standby states to save power when not in use.

9.4.4 Transmitter Only Mode

In this mode, only the transmitter channels are in Active mode. The receivers can be put in standby mode by simply setting GPIO functions RXTDDn and FBTDDn to 0. It is also possible to set the transmitter and feedback chains in Standby mode or through off-state programming the dedicated internal registers in the SPI.

9.4.5 Receiver Only Mode

In this mode, only the receiver and feedback channels are in Active mode. The transmitter channels can be put in standby mode by simply setting GPIO functions TXTDDn to 0. It is also possible to set the transmitter and feedback chains in Standby mode or through off-state programming the dedicated internal registers in the SPI.

9.5 Programming

The AFE79xx software interaction is primarily an initial configuration, based on registers access through the SPI. The device is configured through the SPI using a combination of direct register reads/writes for simple configurations and register writes to initiate macros.

Macro commands abstract out the internal device configuration sequence to a simple set of configuration and simplify the host interaction. They reduce complex configurations into simple writes, avoid computation complexity on the host side, and provide simple status information in response.

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The AFE79xx is a highly integrated and flexible RF transceiver, which can be used by the customers in multiple use cases and modes of operation. Please refer to AFE79xx Configuration Guide (SBAA417) for detailed application information and configuration guide.

10.2 Typical Application

10.2.1 4T4R2F Band 1 + Band 3 FDD with GSM Macro Basestation Transceiver (AFE7920 Only)

10.2.1.1 System Schematic

Figure 604 shows a system block diagram for the AFE7920 when used in a 4-antenna FDD dual band macro base transceiver station (BTS) covering bands 1 and 3.

Typical Application (continued)

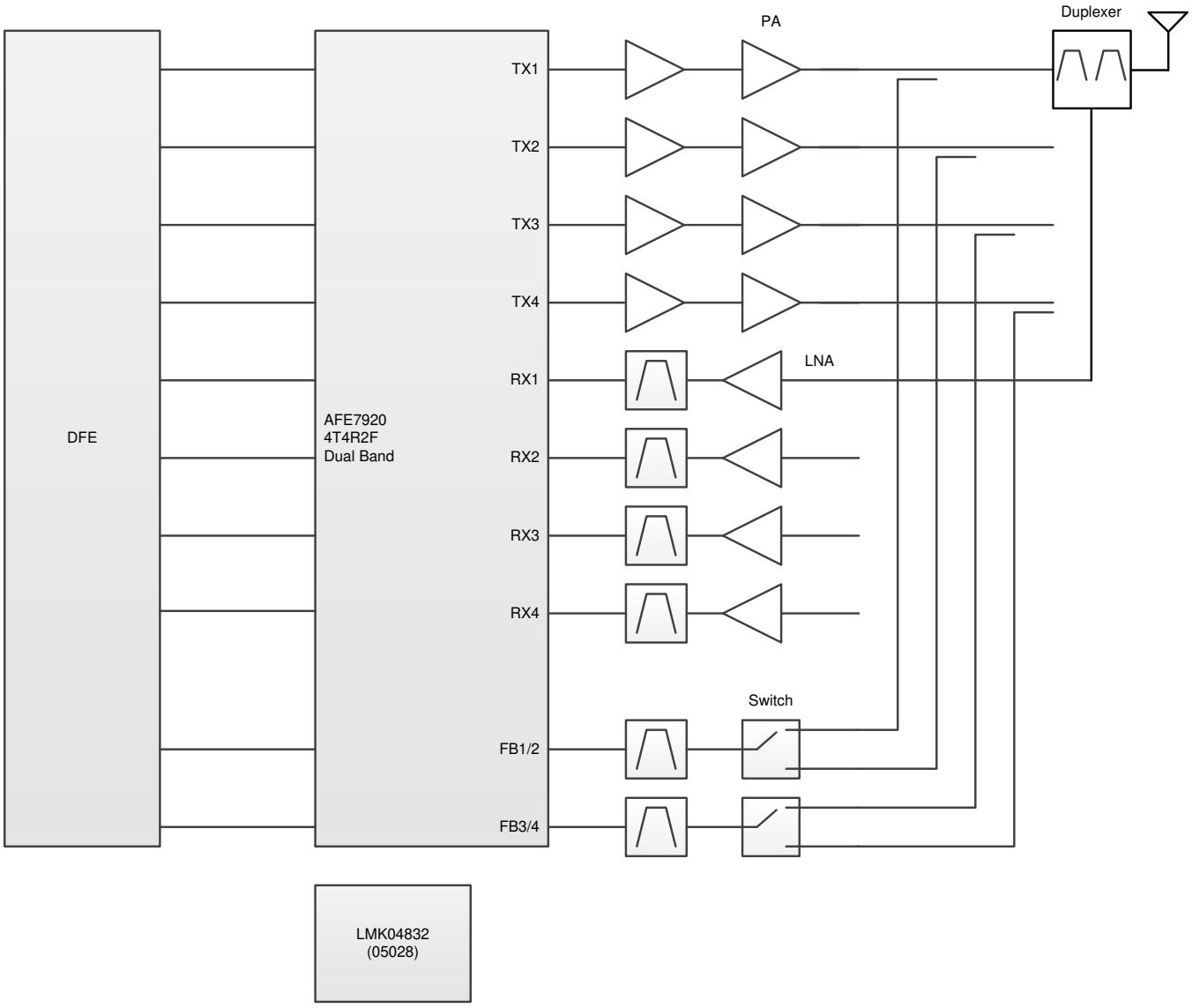


Figure 604. 4T4R2F FDD Block Diagram

10.2.1.2 Design Requirements

The uplink and downlink frequencies for band 1 and band 3 are listed in Table 22. Band 1 covers 60 MHz and band 3 covers 75 MHz.

Table 22. Frequencies for Band 1 and Band 3

BAND	UPLINK (MHz)	UPLINK BW (MHz)	DOWNLINK (MHz)	DOWNLINK BW (MHz)
1	1920 - 1980	60	2110 - 2170	60
3	1710 - 1785	75	1805 – 1880	75

The intra-band intermodulation expansion frequency range and bandwidth are shown in Table 23. 5^{th} order intra-band intermodulation products would cover a bandwidth of 635 MHz.

Table 23. Band 1 + Band 3 Intra-Band Intermodulation Frequencies

	DL BAND (MHz)			IMDx DPD EXPANSION FREQ (MHz)		
	LOW	HIGH	BW	3	5	7
Band 1	2110	2170	60	2230	2290	2350
Band 3	1805	1880	75	1730	1655	1580
Center Frequency				1980	1972.5	1965
Bandwidth				500	635	770

The 3rd order inter-band intermodulation frequencies are shown in Table 24. 3rd order inter-band intermodulation products cover a bandwidth of 960 MHz.

Table 24. Band 1 + Band 3 Inter-Band IMD3 Frequencies

INTER-BAND IMD3 FREQUENCIES (MHz)		
BAND	LOW FREQ	HIGH FREQ
Band 1	2110	2170
Band 3	1805	1880
IMD3	1500	2460

10.2.1.3 Detailed Design Procedure

Typical interface and converter sample rates for a band 1 + band 3 BTS are listed in Table 25.

Table 25. Sample and Interface Rates for a Band 1 + Band 3 Macro BTS

FUNCTION	VALUE
Input Clock Frequency	2457.6 MHz
PLL Reference Frequency	409.6 MHz (input clock divided by 6)
PLL/VCO Frequency	9830.4 MHz
RX ADC Sample Rate	2457.6 MSPS (using external clock directly)
RX Decimation Rate	24x
RX Interface Rate	122.88 MSPS (each for dual bands)
TX DAC Sample Rate	9830.4 MSPS
TX Interpolation Rate	15x
TX Interface Rate	983.04 MSPS
FB ADC Sample Rate	2457.6 MSPS (PLL/VCO divided by 4)
FB Decimation Rate	2.5x

First, the RX ADC clock is chosen as an external clock at 2457.6 MHz for two reasons. First, the large GSM blocking requirement at 800 kHz for GSM in band 3 requires an external clock for low phase noise. Second, the choice of 2457.6 MSPS is advantageous to avoid the 2nd and 3rd harmonics from blockers in either band from falling back in band. This is shown in the frequency plan in Figure 605, which shows the frequencies at which the 2nd and 3rd harmonics fall within bands 1 and 3. A dual band DDC with decimation of 24x provides an output interface rate of 122.88 MSPS complex, which provides 100 MHz per each band.

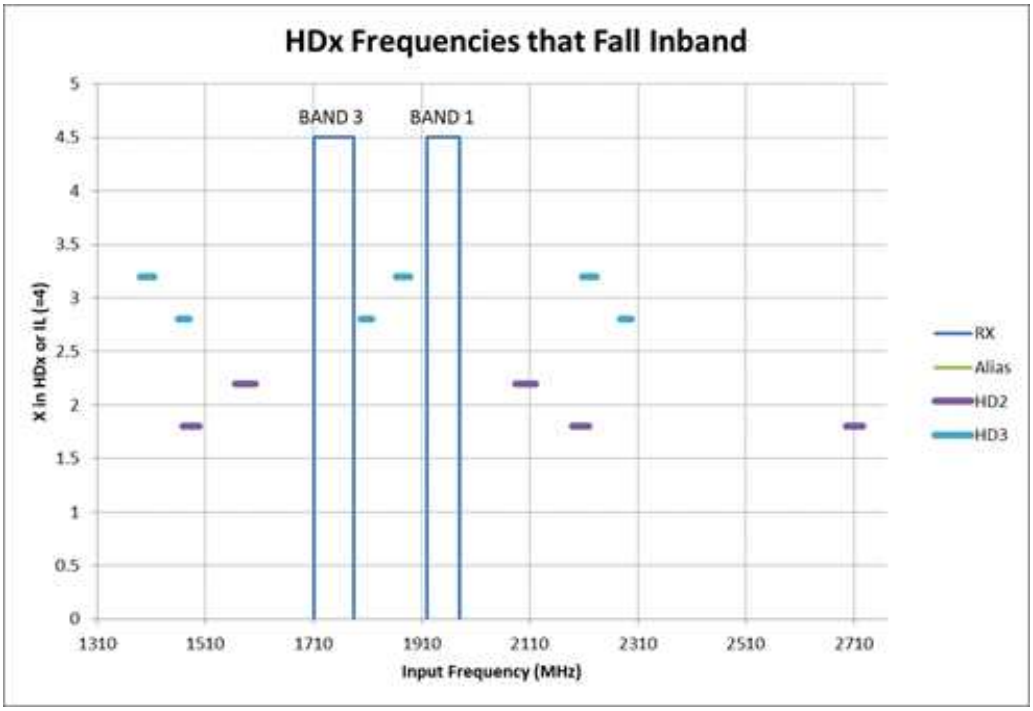


Figure 605. RX Frequency Plan for Band 1 + Band 3 With f_{ADC} = 2457.6 MSPS

Next, the TX DAC sample rate is chosen at 9830.4 MSPS, which is a compromise between a higher sample rate to increase the spacing to the 2nd Nyquist zone image and a lower sample rate to reduce the power consumption of the AFE7920. Other options would be 7372.8 MSPS. A TX interface rate of 9830.4 MSPS is chosen, which provide 800 MHz BW to cover IMD3 and IMD5 intra-band distortion products and the IMD3 inter-band distortion product.

For the FB ADC, a sample rate of 2457.6 MSPS is chosen, which is divided down from the PLL/VCO frequency. Having the same synthesizer for the TX and FB converters allows cancellation of phase noise up to approximately 1/loop_delay, where loop_delay is the is the delay in the analog path between the TX output and FB input. The FB DDC is configured to provide the same interface rate as the TX path, which is typical for systems with digital predistortion.

10.2.1.4 Application Curves

An example of the captured Band 1 + Band 3 spectrum with two-carrier LTE signals at the TX output is shown in Figure 606

Figure 606. Band 1 + Band 3 Output Spectrum With Two-Carrier LTE Signals

11 Power Supply Recommendations

11.1 Recommended Power Supply Groups

Table 26 lists the recommend power supply groups and sub-groups. Each supply group would typically share a voltage regulator, and each supply sub-group would be isolated by ferrite beads.

Table 26. Power Supply Groups

POWER SUPPLIES (BALL NAMES)	VOLTAGE (V)	POWER SUPPLY GROUP	POWER SUPPLY SUB-GROUP (EVM SUPPLY NAMES)
DVDD	0.9	1A	DVDD
VDDT0P9		1A	VDDT
VDD1P2FB	1.2	2A	VDD1P2FB
VDD1P2RX		2A	VDD1P2RX
VDD1P2TXCLK		2B	VDD1P2TX_CLK
VDD1P2TXENC		2B	VDD1P2TX_CLK
VDD1P2PLLFBCML		2C	VDD1P2PLL
VDD1P2PLLRXCML		2C	VDD1P2PLL
VDD1P2PLLCLKREF		2C	VDD1P2PLL
VDD1P8FB	1.8	3A	VDD1P8FB
VDD1P8RX		3A	VDD1P8RX
VDD1P8GPIO		3A	VDD1P8GPIO
VDD1P8TX		3B	VDD1P8TX
VDD1P8FBCLK		3B	VDD1P8FB_CLK
VDD1P8RXCLK		3B	VDD1P8RX_CLK
VDD1P8TXDAC		3B	VDD1P8TX_DAC
VDDA1P8		3B	VDD1P8PLL
VDD1P8PLLVCO		3C	VDD1P8PLLVCO
VDD1P8PLL		3C	VDD1P8PLL

11.2 Power Supply Sequence

The power supply bring-up sequence requirements are shown in Figure 607.

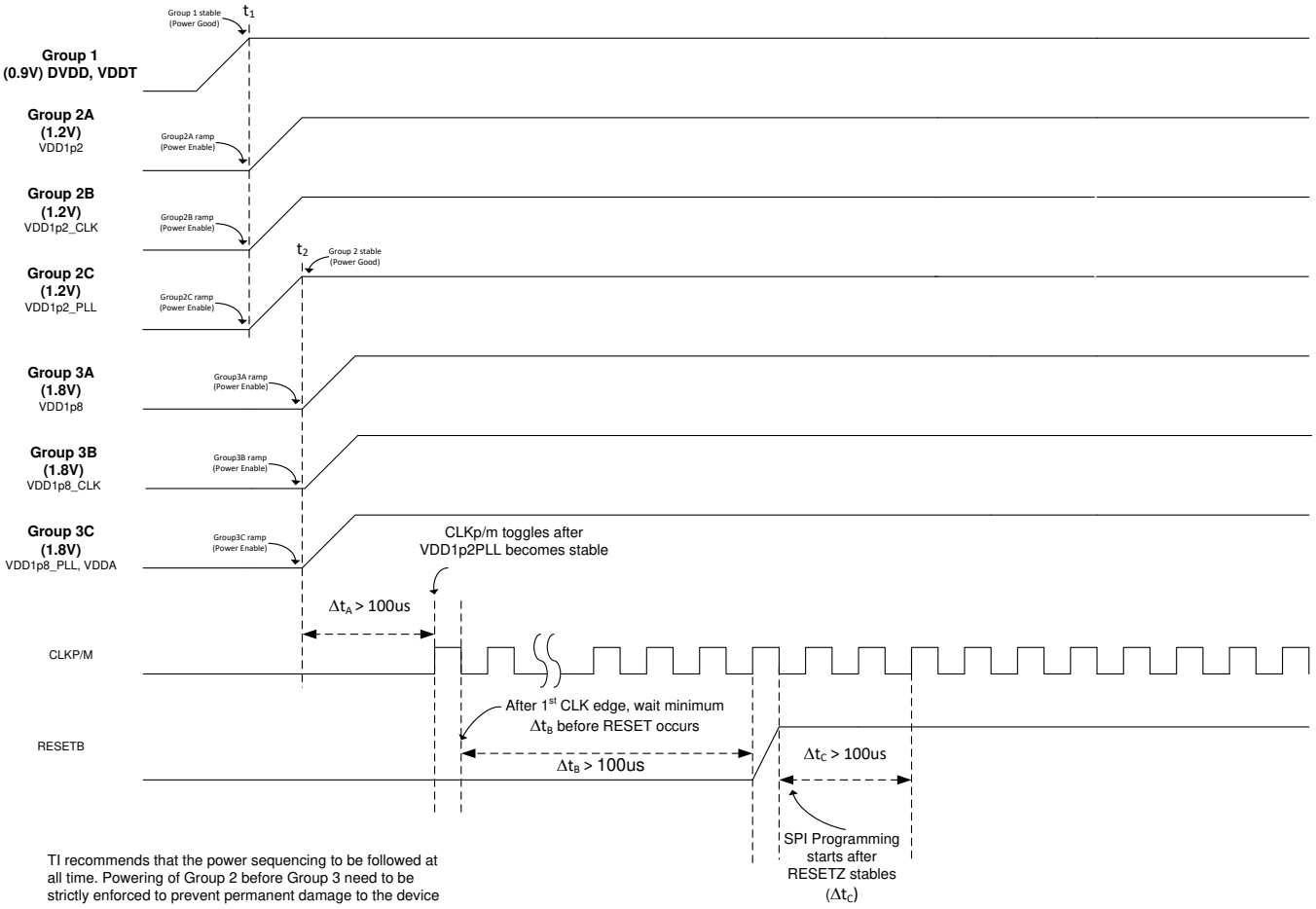


Figure 607. Power Supply Sequence Requirements

12 Layout

12.1 Layout Guidelines

TI recommends to follow the layout used on the AFE79xx EVM. Layout guidelines are found in the application note AFE79xx Layout Guide (SBAA405) and is available by request from TI.

12.1.1 Layout Examples

Layout and symbol files for the AFE79xx EVM are available from TI upon request.

13 Device and Documentation Support

13.1 Device Support

13.1.1 Third-Party Products Disclaimer

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13.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

Table 27. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
AFE7920	Click here	Click here	Click here	Click here	Click here
AFE7921	Click here	Click here	Click here	Click here	Click here
AFE7988	Click here	Click here	Click here	Click here	Click here
AFE7989	Click here	Click here	Click here	Click here	Click here

13.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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13.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

14.1 Package Option Addendum

14.1.1 Packaging Information

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (3)	MSL Peak Temp (4)	Op Temp (°C)	Device Marking (5) (6)
AFE7920IABJ	ACTIVE	FCBGA	ABJ	400	90	Green (RoHS& no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 85	AFE7920I
AFE7921IABJ	PREVIEW	FCBGA	ABJ	400	90	TBD	Call TI	Call TI	-40 to 85	
AFE7988IABJ	ACTIVE	FCBGA	ABJ	400	90	Green (RoHS& no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 85	AFE7988I
AFE7989IABJ	ACTIVE	FCBGA	ABJ	400	90	Green (RoHS& no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 85	AFE7989I

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

(4) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(5) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

(6) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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