# 1

JMODE=0, Fs=2700Msps
The evaluation was performed according to the procedure described in SLAU701A.
It was confirmed that the HSDC result was the same as the document.

# JMODE0 (SLAU701A)

- Connect a USB cable from the PC to the TSW14J57EVM
- Connect the power cable from the TSW14J57EVM to a 12-V DC power supply (stand-by). (the power switch on the TSW14J57EVM is in the "on" position)
- Connect a USB cable from the PC to the ADC12DJ3200EVM
- Connect the power cable from the ADC12DJ3200EVM to a 5-V DC power supply (stand-by).
- Connect the signal generator to the ADC12DJ3200EVM (RF output disabled).

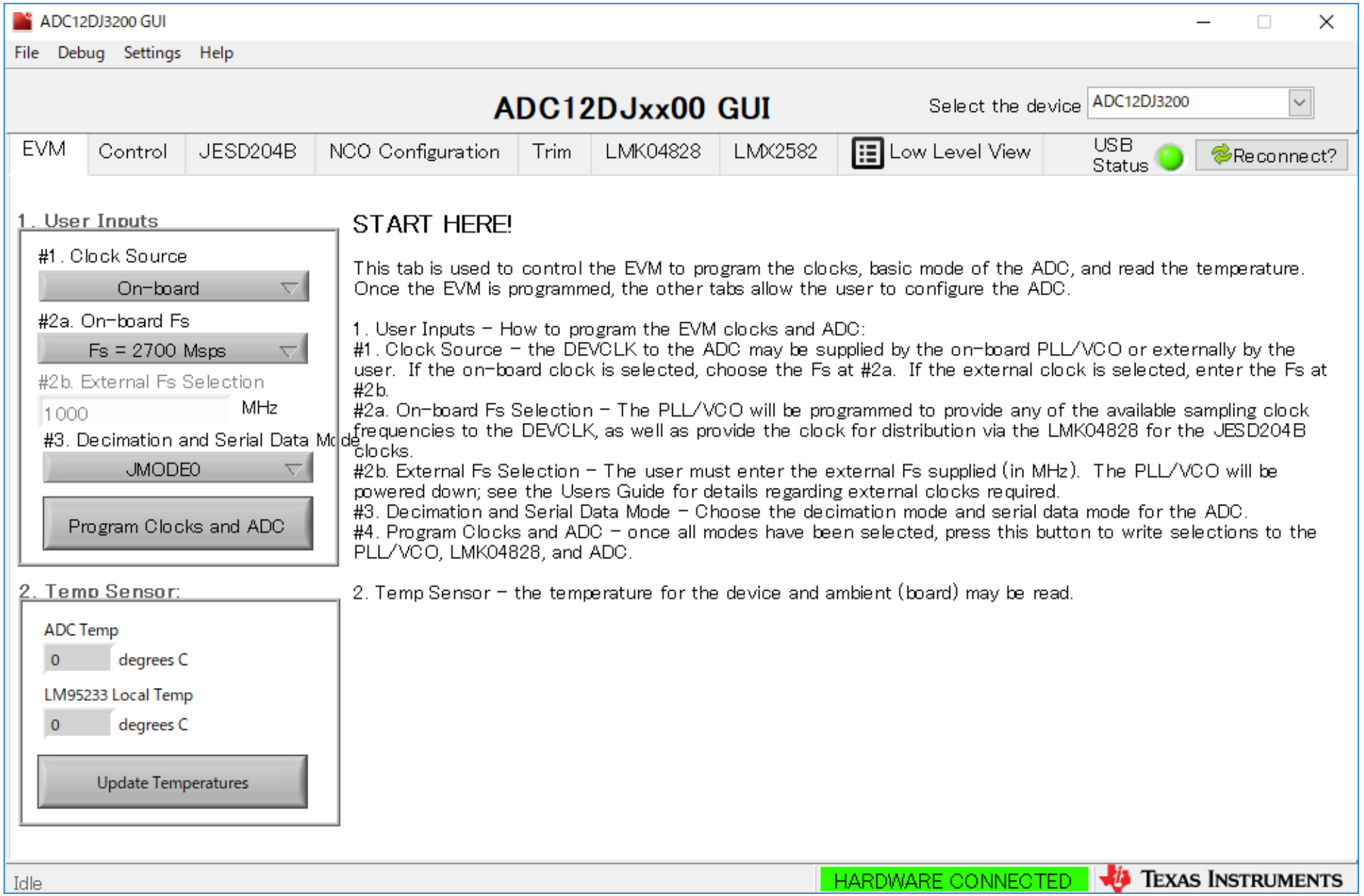
# JMODE0 (SLAU701A)

- Start the Windows PC.
- Turn on the 12-V power supply for the TSW14J57EVM.
  - Blue LEDs D10, D11, D13, D14, D15, D17, D18 and D19, and green LED D21 turn on.
- Turn on the 5-V power supply for the ADC12DJ3200EVM.
  - Green LEDs D7 and D8 turn on.
- Turn on the signal generator RF output of 0dBm, 1910MHz.

# JMODE0 (SLAU701A)

- Open the ADC12DJxx00EVM GUI.
- Select the on-board clock as the clock source.
- Select the Fs=2700Msps as the on-board Fs.
- Select the JMODE0 as the decimation and serial data mode.
- Click "program clock and ADC".
  - The green LED, PLL2 LCKD, turn on.

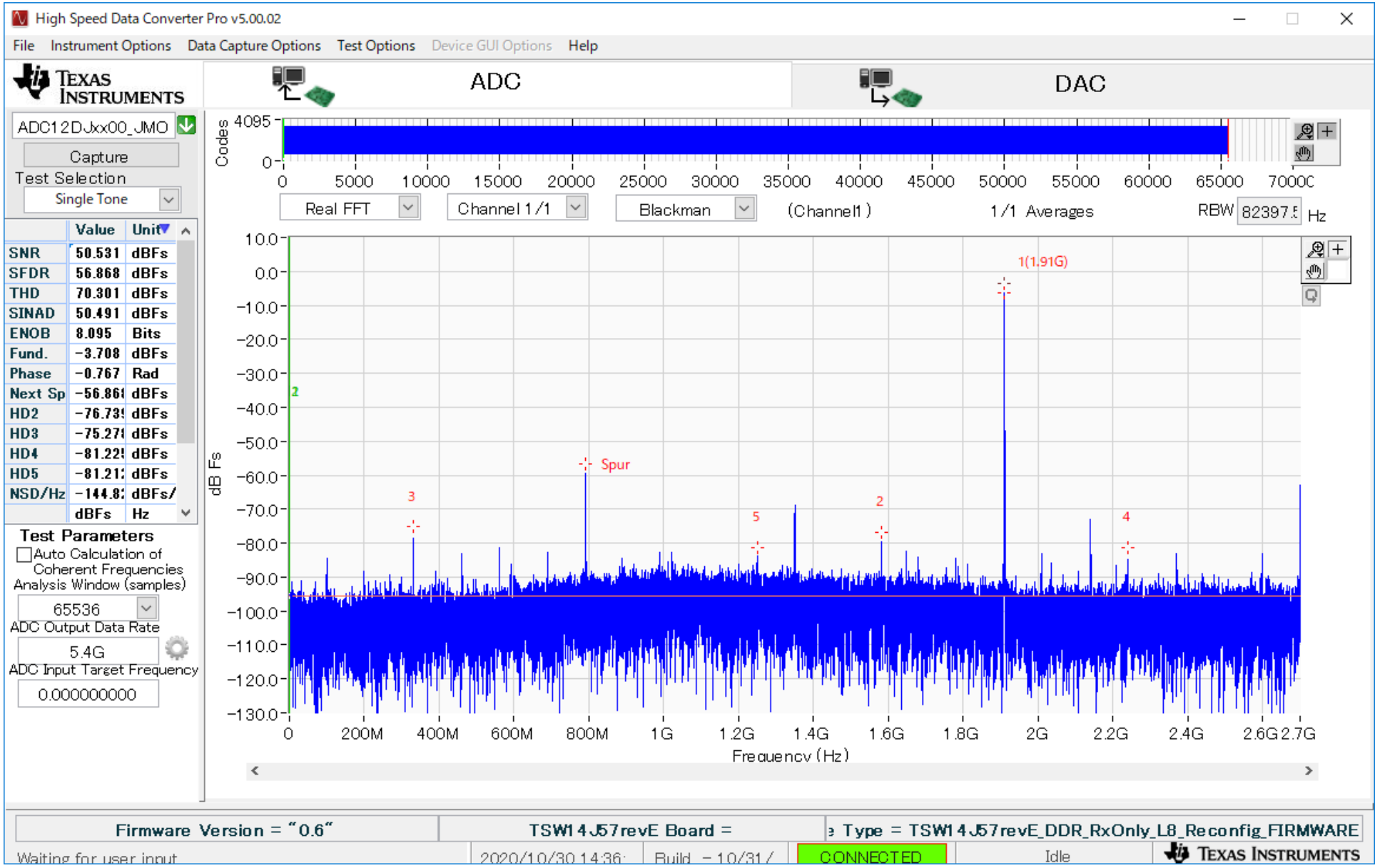
# JMODE0 (SLAU701A)



# JMODE0 (SLAU701A)

- Open the HSDC Pro v5.00.02.
- Click OK to confirm the serial number of the TSW14J57EVM device.
- "No firmware" popup will be displayed, click OK.
- Select the ADC12DJxx00_JMODE0 device from the ADC select pull-down.
- "Do you want to update the Firmware for ADC?" will be displayed, click OK.
  - LEDs D5, D8 and D9 turn on. LED, D2, flashes. LEDs, D1, D3, D6 and D7 turn off. (LED, D3, often turn on)
  - Firmware version = "0.6". The interface type = TSW14J57revE_DDR_RxOnly_L8_Reconfig_FIRMWARE.
- Enter the ADC Output Rate as "5400M".
- Popup will display "New lane rate is 10.8G, JESD ref-clock is 270M". Click OK.
- Click Capture button.

# JMODE0 (SLAU701A)



# 2

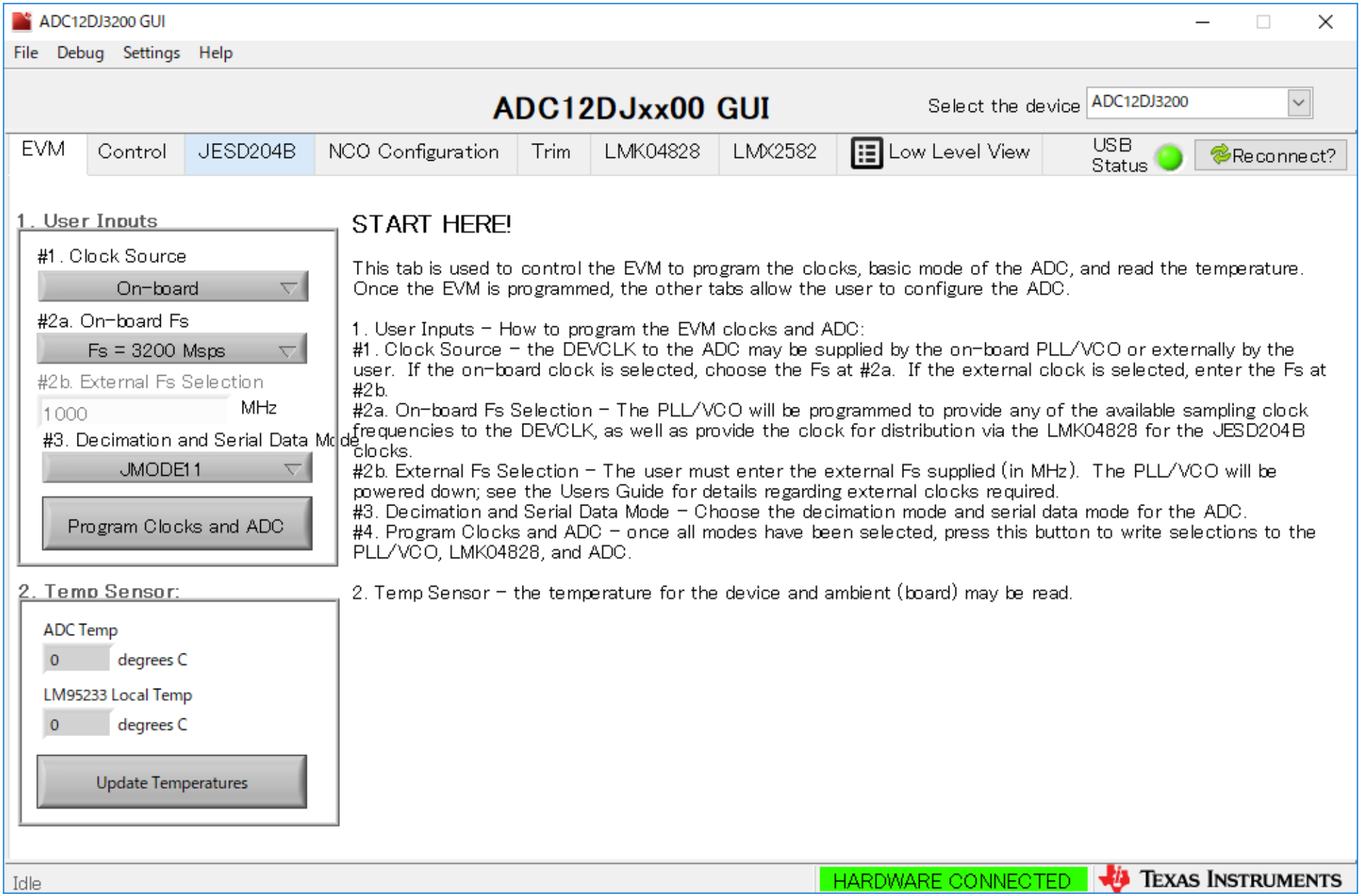
JMODE=11, Fs=3200MSPS,
NCO=2400MHz, Fin=1800 to 3000MHz
(2nd Nyquist Zone)
IQ seemed to be swapping. The largest spectrum of the HSDC complex FFT was marked with the 1' marker.

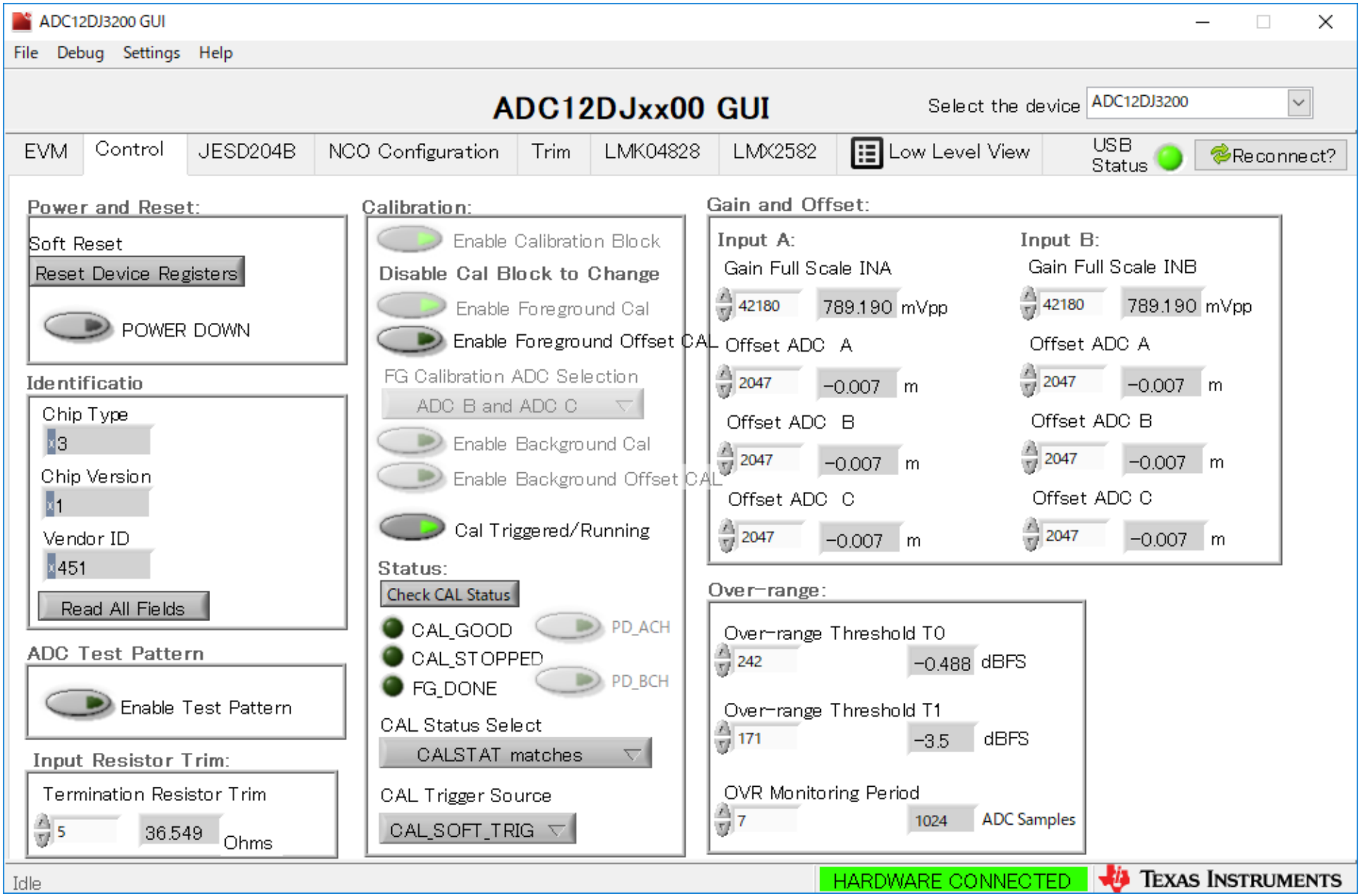
# JMODE11 (fnco=2400M)

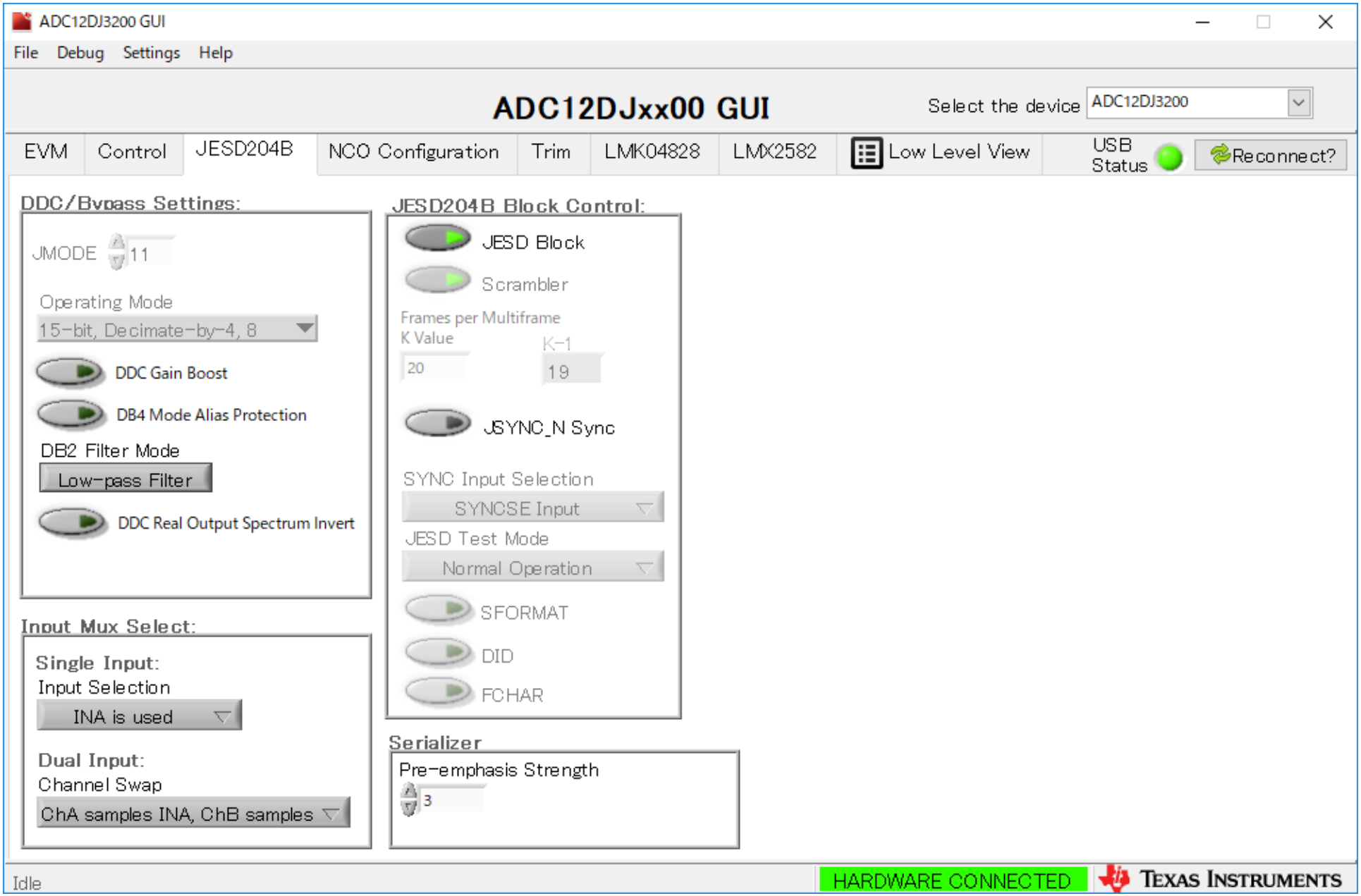
- In the ADC12DJxx00EVM GUI that has been opened above :
- Select the on-board clock as the clock source.
- Select the Fs=3200Msps as the on-board Fs.
- Select the JMODE11 as the decimation and serial data mode.
- Click "program clock and ADC".

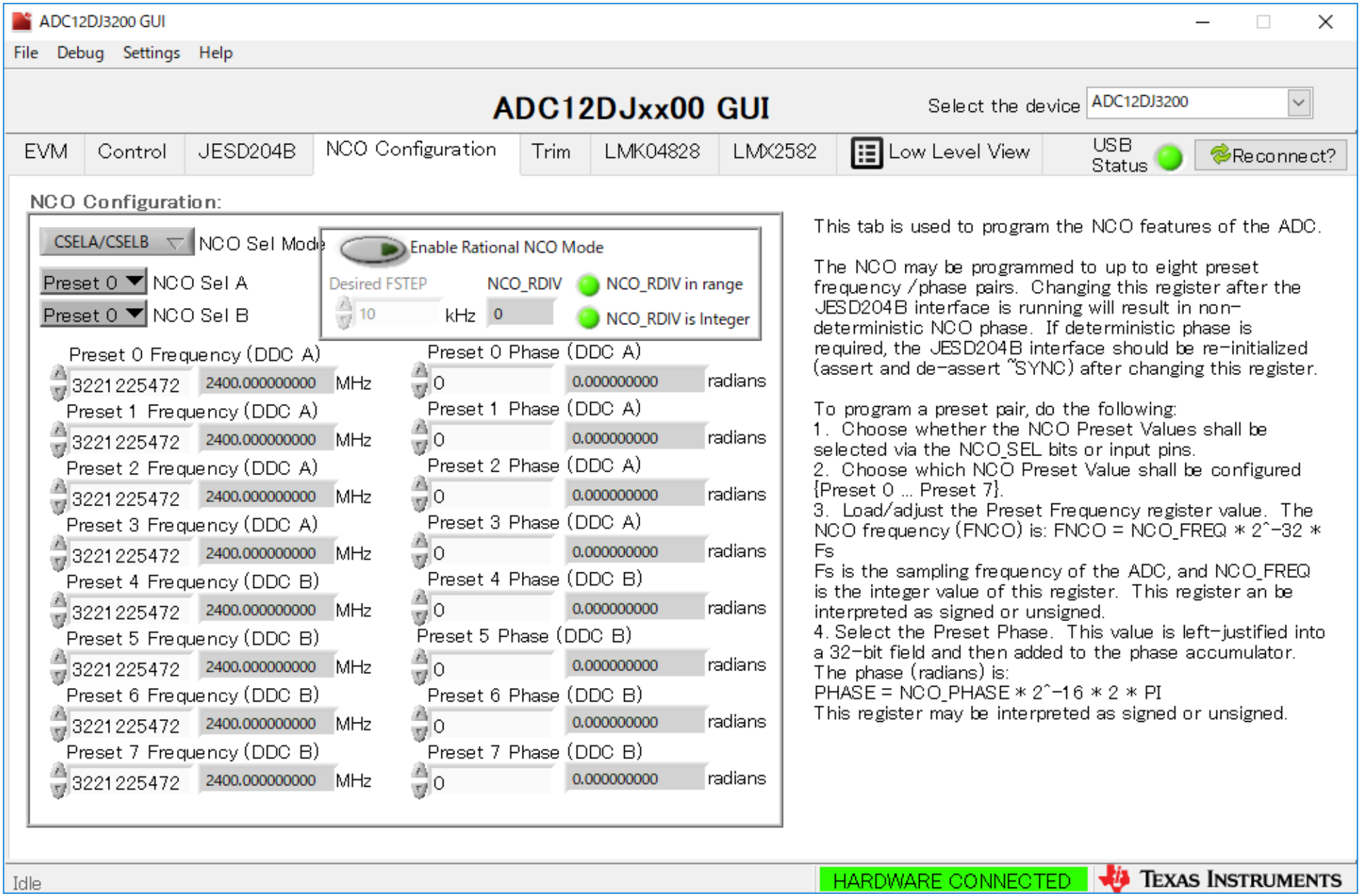
- NCO is the default value of 2400MHz.

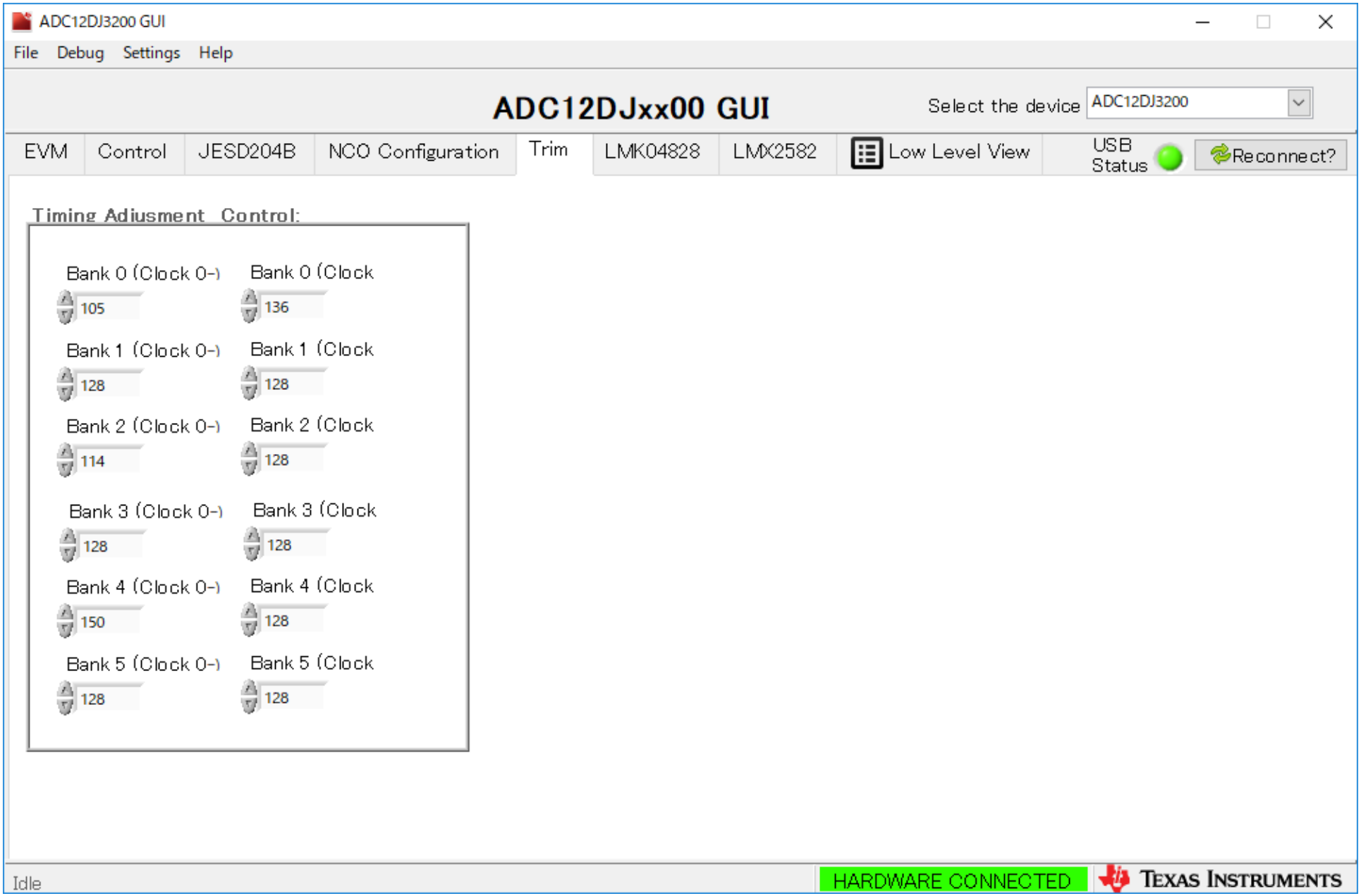
- Change the input frequency from the signal generator to 2.2GHz.

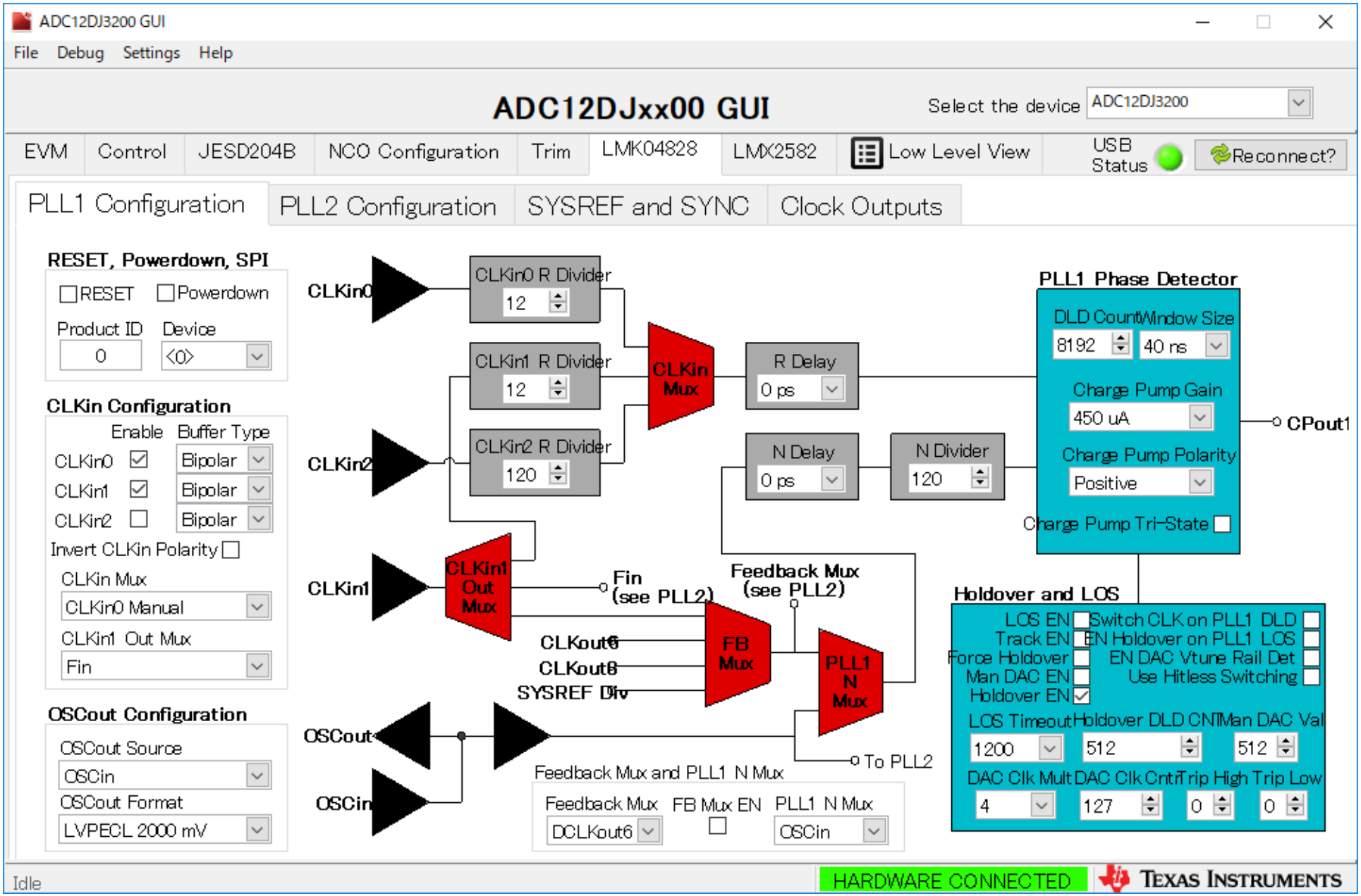

ADC12DJ3200 GUI
File
Debug
Settings
Help
ADC12DJxx00 GUI
Select the device
ADC12DJ3200
EVM
Control
JESD204B
NCO Configuration
Trim
LMK04828
LMX2582
Low Level View
USB Status
Reconnect?
1. User Inputs
#1. Clock Source
On-board
#2a. On-board Fs
Fs = 3200 Msps
#2b. External Fs Selection
1000
MHz
#3. Decimation and Serial Data Mode
JMODE11
Program Clocks and ADC
START HERE!
This tab is used to control the EVM to program the clocks, basic mode of the ADC, and read the temperature. Once the EVM is programmed, the other tabs allow the user to configure the ADC.
1. User Inputs – How to program the EVM clocks and ADC:
#1. Clock Source – the DEVCLK to the ADC may be supplied by the on-board PLL/VCO or externally by the user. If the on-board clock is selected, choose the Fs at #2a. If the external clock is selected, enter the Fs at #2b.
#2a. On-board Fs Selection – The PLL/VCO will be programmed to provide any of the available sampling clock frequencies to the DEVCLK, as well as provide the clock for distribution via the LMK04828 for the JESD204B clocks.
#2b. External Fs Selection – The user must enter the external Fs supplied (in MHz). The PLL/VCO will be powered down; see the Users Guide for details regarding external clocks required.
#3. Decimation and Serial Data Mode – Choose the decimation mode and serial data mode for the ADC.
#4. Program Clocks and ADC – once all modes have been selected, press this button to write selections to the PLL/VCO, LMK04828, and ADC.
2. Temp Sensor:
ADC Temp
0
degrees C
LM95233 Local Temp
0
degrees C
Update Temperatures
2. Temp Sensor – the temperature for the device and ambient (board) may be read.
Idle
HARDWARE CONNECTED
Texas Instruments

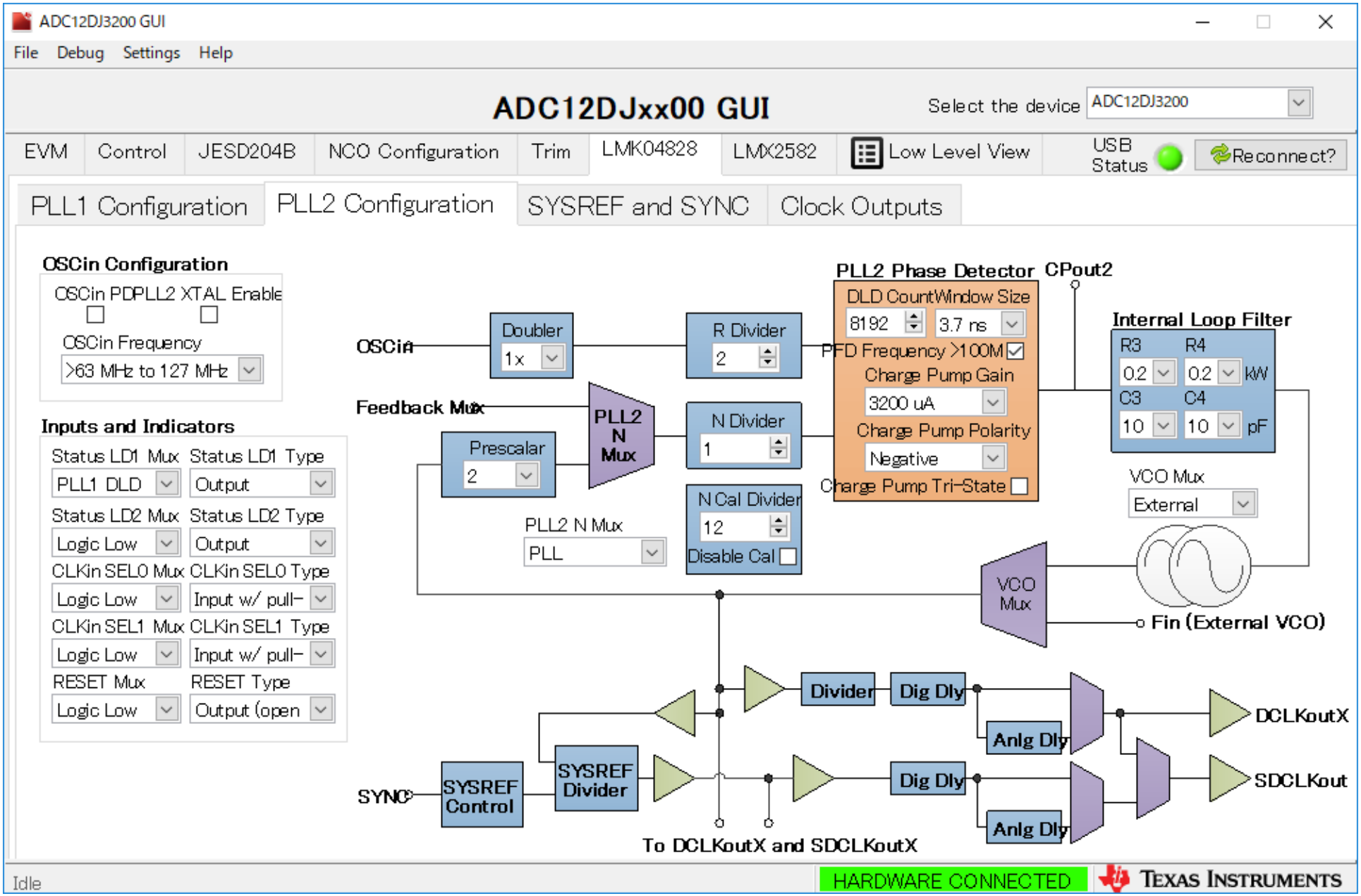

ADC12DJ3200 GUI
File Debug Settings Help
ADC12DJxx00 GUI
Select the device ADC12DJ3200
EVM Control JESD204B NCO Configuration Trim LMK04828 LMX2582 Low Level View
USB Status
Reconnect?
Power and Reset:
Soft Reset
Reset Device Registers
POWER DOWN
Identificatio
Chip Type
3
Chip Version
1
Vendor ID
451
Read All Fields
ADC Test Pattern
Enable Test Pattern
Input Resistor Trim:
Termination Resistor Trim
5
36.549
Ohms
Calibration:
Enable Calibration Block
Disable Cal Block to Change
Enable Foreground Cal
Enable Foreground Offset CAL
FG Calibration ADC Selection
ADC B and ADC C
Enable Background Cal
Enable Background Offset CAL
Cal Triggered/Running
Status:
Check CAL Status
CAL_GOOD
CAL_STOPPED
FG_DONE
PD_ACH
PD_BCH
CAL Status Select
CALSTAT matches
CAL Trigger Source
CAL_SOFT_TRIG
Gain and Offset:
Input A:
Gain Full Scale INA
42180
789.190
mVpp
Offset ADC A
2047
-0.007
m
Offset ADC B
2047
-0.007
m
Offset ADC C
2047
-0.007
m
Input B:
Gain Full Scale INB
42180
789.190
mVpp
Offset ADC A
2047
-0.007
m
Offset ADC B
2047
-0.007
m
Offset ADC C
2047
-0.007
m
Over-range:
Over-range Threshold T0
242
-0.488
dBFS
Over-range Threshold T1
171
-3.5
dBFS
OVR Monitoring Period
7
1024
ADC Samples
Idle
HARDWARE CONNECTED
Texas Instruments

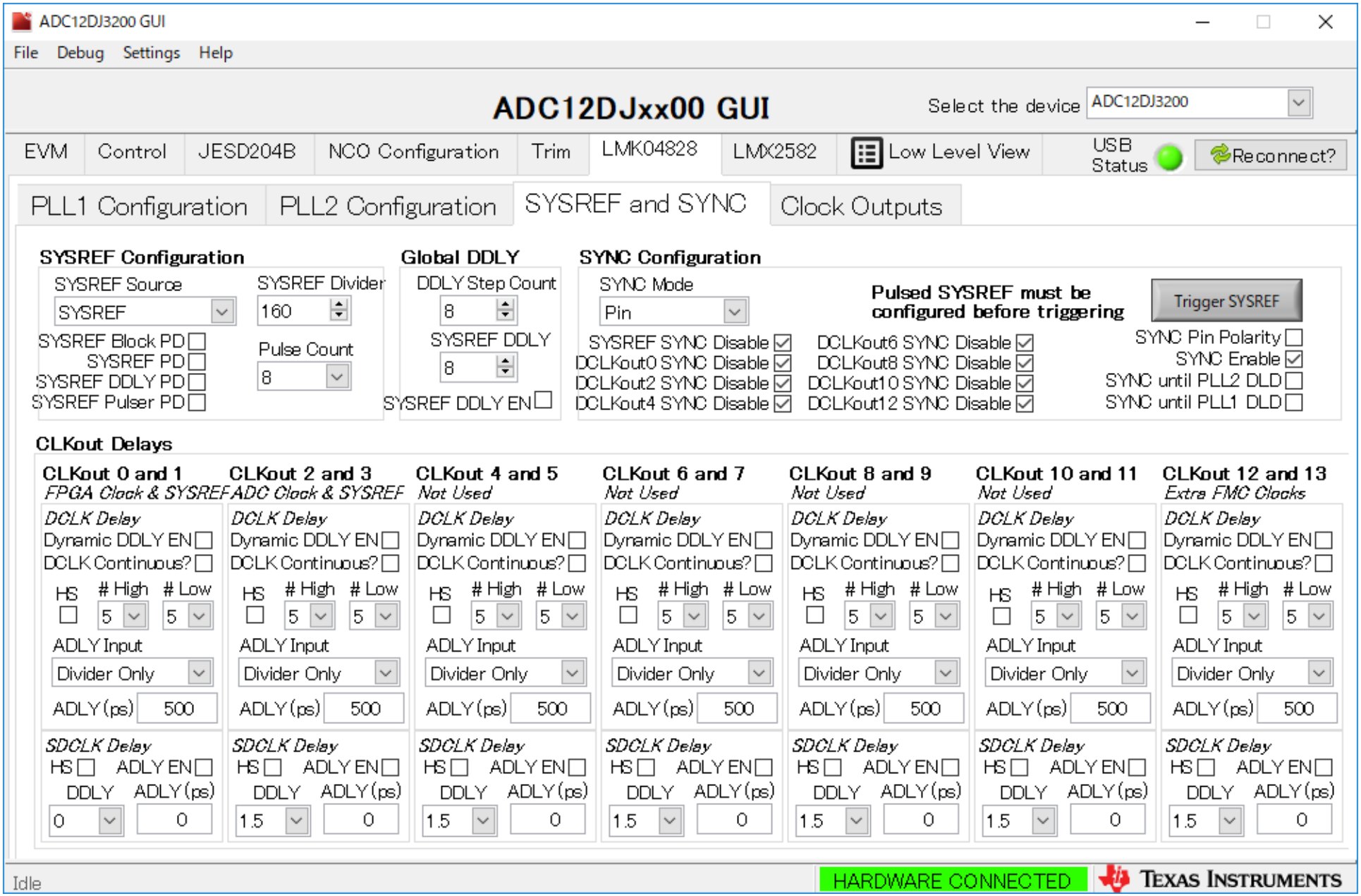

ADC12DJ3200 GUI
File
Debug
Settings
Help
ADC12DJxx00 GUI
Select the device
ADC12DJ3200
EVM
Control
JESD204B
NCO Configuration
Trim
LMK04828
LMX2582
Low Level View
USB Status
Reconnect?
DDC/Bypass Settings:
JMODE
11
Operating Mode
15-bit, Decimate-by-4, 8
DDC Gain Boost
DB4 Mode Alias Protection
DB2 Filter Mode
Low-pass Filter
DDC Real Output Spectrum Invert
JESD204B Block Control:
JESD Block
Scrambler
Frames per Multiframe
K Value
20
K-1
19
JSYNC_N Sync
SYNC Input Selection
SYNCSE Input
JESD Test Mode
Normal Operation
SFORMAT
DID
FCHAR
Input Mux Select:
Single Input:
Input Selection
INA is used
Dual Input:
Channel Swap
ChA samples INA, ChB samples
Serializer
Pre-emphasis Strength
3
Idle
HARDWARE CONNECTED
Texas Instruments

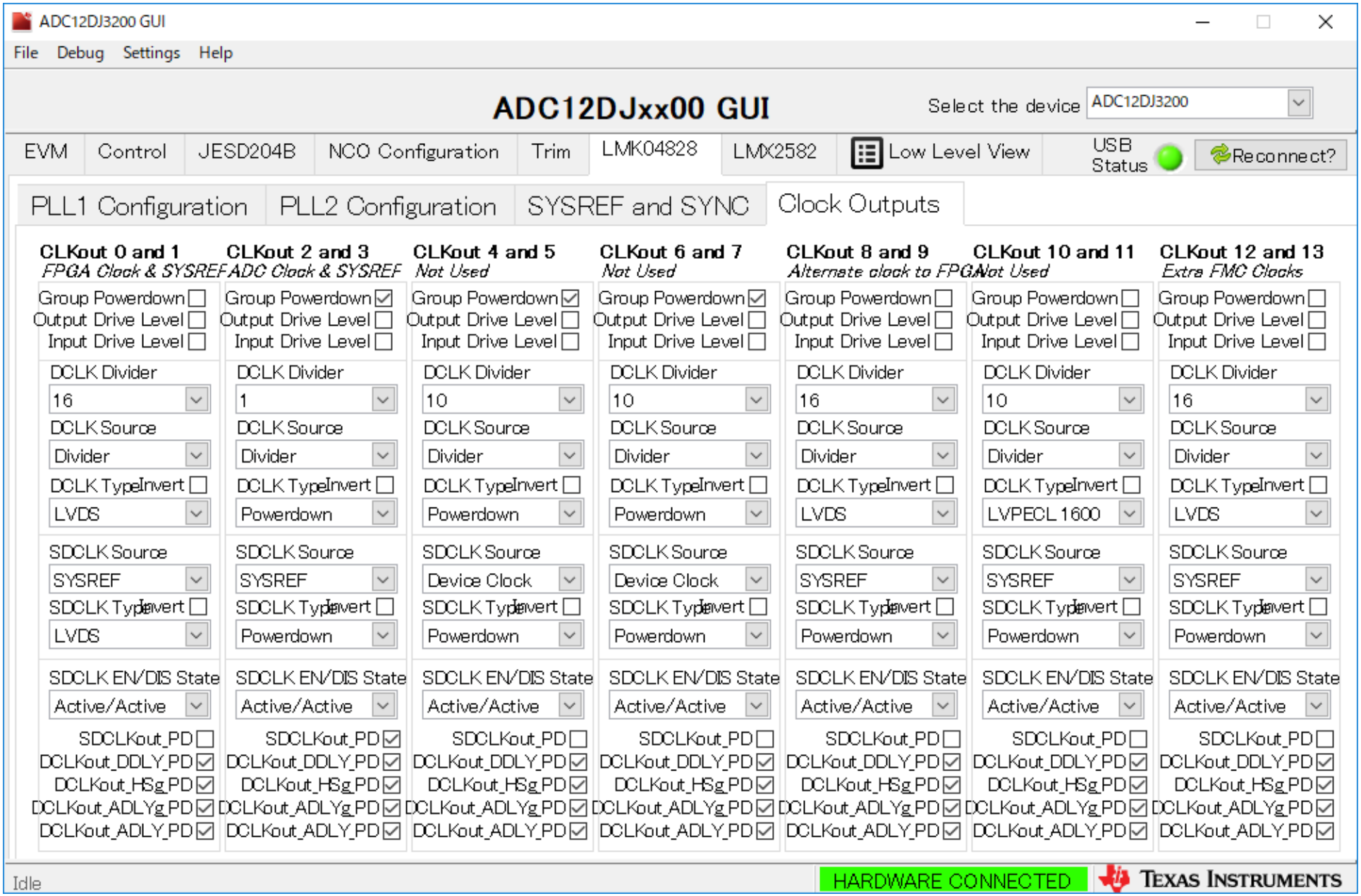

ADC12DJ3200 GUI
File Debug Settings Help
ADC12DJxx00 GUI
Select the device ADC12DJ3200
EVM Control JESD204B NCO Configuration Trim LMK04828 LMX2582 Low Level View
USB Status
Reconnect?
NCO Configuration:
CSELA/CSELB NCO Sel Mode
Enable Rational NCO Mode
Preset 0 NCO Sel A
Preset 0 NCO Sel B
Desired FSTEP
NCO_RDIV
NCO_RDIV in range
10 kHz 0
NCO_RDIV is Integer
Preset 0 Frequency (DDC A) 3221225472 2400.000000000 MHz
Preset 0 Phase (DDC A) 0 0.000000000 radians
Preset 1 Frequency (DDC A) 3221225472 2400.000000000 MHz
Preset 1 Phase (DDC A) 0 0.000000000 radians
Preset 2 Frequency (DDC A) 3221225472 2400.000000000 MHz
Preset 2 Phase (DDC A) 0 0.000000000 radians
Preset 3 Frequency (DDC A) 3221225472 2400.000000000 MHz
Preset 3 Phase (DDC A) 0 0.000000000 radians
Preset 4 Frequency (DDC B) 3221225472 2400.000000000 MHz
Preset 4 Phase (DDC B) 0 0.000000000 radians
Preset 5 Frequency (DDC B) 3221225472 2400.000000000 MHz
Preset 5 Phase (DDC B) 0 0.000000000 radians
Preset 6 Frequency (DDC B) 3221225472 2400.000000000 MHz
Preset 6 Phase (DDC B) 0 0.000000000 radians
Preset 7 Frequency (DDC B) 3221225472 2400.000000000 MHz
Preset 7 Phase (DDC B) 0 0.000000000 radians
This tab is used to program the NCO features of the ADC.
The NCO may be programmed to up to eight preset frequency /phase pairs. Changing this register after the JESD204B interface is running will result in non-deterministic NCO phase. If deterministic phase is required, the JESD204B interface should be re-initialized (assert and de-assert ~SYNC) after changing this register.
To program a preset pair, do the following:
1. Choose whether the NCO Preset Values shall be selected via the NCO_SEL bits or input pins.
2. Choose which NCO Preset Value shall be configured {Preset 0 ... Preset 7}.
3. Load/adjust the Preset Frequency register value. The NCO frequency (FNCO) is: FNCO = NCO_FREQ * 2^-32 * Fs
Fs is the sampling frequency of the ADC, and NCO_FREQ is the integer value of this register. This register an be interpreted as signed or unsigned.
4. Select the Preset Phase. This value is left-justified into a 32-bit field and then added to the phase accumulator. The phase (radians) is:
PHASE = NCO_PHASE * 2^-16 * 2 * PI
This register may be interpreted as signed or unsigned.
Idle
HARDWARE CONNECTED
Texas Instruments

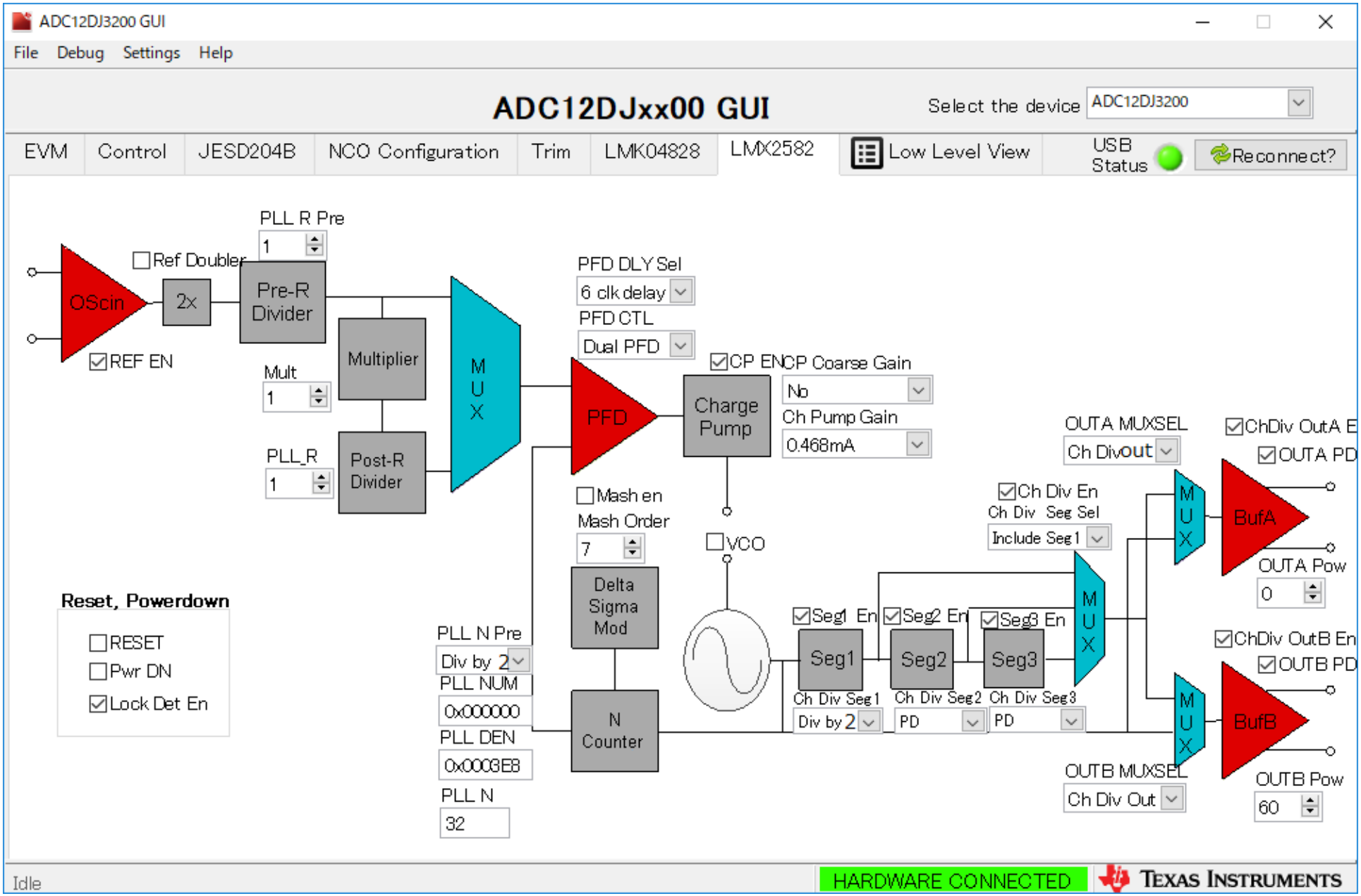

ADC12DJ3200 GUI
File
Debug
Settings
Help
ADC12DJxx00 GUI
Select the device
ADC12DJ3200
EVM
Control
JESD204B
NCO Configuration
Trim
LMK04828
LMX2582
Low Level View
USB Status
Reconnect?
Timing Adjusment Control:
Bank 0 (Clock 0-)
105
Bank 0 (Clock
136
Bank 1 (Clock 0-)
128
Bank 1 (Clock
128
Bank 2 (Clock 0-)
114
Bank 2 (Clock
128
Bank 3 (Clock 0-)
128
Bank 3 (Clock
128
Bank 4 (Clock 0-)
150
Bank 4 (Clock
128
Bank 5 (Clock 0-)
128
Bank 5 (Clock
128
Idle
HARDWARE CONNECTED
Texas Instruments


ADC12DJ3200 GUI
File Debug Settings Help
ADC12DJxx00 GUI
Select the device ADC12DJ3200
EVM Control JESD204B NCO Configuration Trim LMK04828 LMX2582 Low Level View
USB Status
Reconnect?
PLL1 Configuration PLL2 Configuration SYSREF and SYNC Clock Outputs
RESET, Powerdown, SPI
RESET Powerdown
Product ID Device
0 <0>
CLKin Configuration
Enable Buffer Type
CLKin0 Bipolar
CLKin1 Bipolar
CLKin2 Bipolar
Invert CLKin Polarity
CLKin Mux
CLKin0 Manual
CLKin1 Out Mux
Fin
OSCout Configuration
OSCout Source
OSCin
OSCout Format
LVPECL 2000 mV
CLKin0
CLKin1
CLKin2
OSCout
OSCin
CLKin0 R Divider 12
CLKin1 R Divider 12
CLKin2 R Divider 120
CLKin Mux
CLKin1 Out Mux
Fin (see PLL2)
CLKout6
CLKout8
SYSREF Div
FB Mux
R Delay 0 ps
N Delay 0 ps
N Divider 120
PLL1 N Mux
To PLL2
Feedback Mux (see PLL2)
Feedback Mux and PLL1 N Mux
Feedback Mux DCLKout6
FB Mux EN
PLL1 N Mux CSCin
PLL1 Phase Detector
DLD Count Window Size 8192 40 ns
Charge Pump Gain 450 uA
Charge Pump Polarity Positive
Charge Pump Tri-State
CPout1
Holdover and LOS
LOS EN
Track EN
Force Holdover
Man DAC EN
Holdover EN
Switch CLK on PLL1 DLD
EN Holdover on PLL1 LOS
EN DAC Vtune Rail Det
Use Hitless Switching
LOS Timeout 1200
Holdover DLD CNT 512
Man DAC Val 512
DAC Clk Mult 4
DAC Clk Cntr 127
Trip High 0
Trip Low 0
Idle
HARDWARE CONNECTED
Texas Instruments


ADC12DJ3200 GUI
File Debug Settings Help
ADC12DJxx00 GUI
Select the device ADC12DJ3200
EVM Control JESD204B NCO Configuration Trim LMK04828 LMX2582 Low Level View
USB Status
Reconnect?
PLL1 Configuration PLL2 Configuration SYSREF and SYNC Clock Outputs
OSCin Configuration
OSCin PD PLL2 XTAL Enable
OSCin Frequency
>63 MHz to 127 MHz
Inputs and Indicators
Status LD1 Mux PLL1 DLD
Status LD1 Type Output
Status LD2 Mux Logic Low
Status LD2 Type Output
CLKin SEL0 Mux Logic Low
CLKin SEL0 Type Input w/ pull-
CLKin SEL1 Mux Logic Low
CLKin SEL1 Type Input w/ pull-
RESET Mux Logic Low
RESET Type Output (open
OSCin
Doubler 1x
R Divider 2
PLL2 Phase Detector
DLD Count Window Size 8192 3.7 ns
PFD Frequency >100M
Charge Pump Gain 3200 uA
Charge Pump Polarity Negative
Charge Pump Tri-State
CPout2
Internal Loop Filter
R3 0.2 R4 0.2 kW
C3 10 C4 10 pF
Feedback Mux
PLL2 N Mux
Prescalar 2
N Divider 1
N Cal Divider 12
Disable Cal
PLL2 N Mux PLL
VCO Mux External
VCO Mux
Fin (External VCO)
Divider
Dig Dly
Anlg Dly
DCLKoutX
SYNC
SYSREF Control
SYSREF Divider
Dig Dly
Anlg Dly
SDCLKout
To DCLKoutX and SDCLKoutX
Idle
HARDWARE CONNECTED
Texas Instruments


ADC12DJ3200 GUI
File Debug Settings Help
ADC12DJxx00 GUI
Select the device ADC12DJ3200
EVM Control JESD204B NCO Configuration Trim LMK04828 LMX2582 Low Level View
USB Status
Reconnect?
PLL1 Configuration PLL2 Configuration SYSREF and SYNC Clock Outputs
SYSREF Configuration
SYSREF Source SYSREF
SYSREF Divider 160
Pulse Count 8
SYSREF Block PD
SYSREF PD
SYSREF DDLY PD
SYSREF Pulser PD
Global DDLY
DDLY Step Count 8
SYSREF DDLY 8
SYSREF DDLY EN
SYNC Configuration
SYNC Mode Pin
Pulsed SYSREF must be configured before triggering
Trigger SYSREF
SYSREF SYNC Disable
DCLKout0 SYNC Disable
DCLKout2 SYNC Disable
DCLKout4 SYNC Disable
DCLKout6 SYNC Disable
DCLKout8 SYNC Disable
DCLKout10 SYNC Disable
DCLKout12 SYNC Disable
SYNC Pin Polarity
SYNC Enable
SYNC until PLL2 DLD
SYNC until PLL1 DLD
CLKout Delays
CLKout 0 and 1 FPGA Clock & SYSREF
CLKout 2 and 3 ADC Clock & SYSREF
CLKout 4 and 5 Not Used
CLKout 6 and 7 Not Used
CLKout 8 and 9 Not Used
CLKout 10 and 11 Not Used
CLKout 12 and 13 Extra FMC Clocks
DCLK Delay
Dynamic DDLY EN
DCLK Continuous?
HS # High # Low
ADLY Input Divider Only
ADLY (ps) 500
SDCLK Delay
HS ADLY EN
DDLY ADLY (ps)
0 0
1.5 0
Idle
HARDWARE CONNECTED
Texas Instruments


ADC12DJ3200 GUI
File Debug Settings Help
ADC12DJxx00 GUI
Select the device ADC12DJ3200
EVM Control JESD204B NCO Configuration Trim LMK04828 LMX2582 Low Level View
USB Status
Reconnect?
PLL1 Configuration PLL2 Configuration SYSREF and SYNC Clock Outputs
CLKout 0 and 1 FPGA Clock & SYSREF
CLKout 2 and 3 ADC Clock & SYSREF
CLKout 4 and 5 Not Used
CLKout 6 and 7 Not Used
CLKout 8 and 9 Alternate clock to FPGA
CLKout 10 and 11 Not Used
CLKout 12 and 13 Extra FMC Clocks
Group Powerdown
Output Drive Level
Input Drive Level
DCLK Divider
16 1 10 10 16 10 16
DCLK Source
Divider
DCLK TypeInvert
LVDS Powerdown Powerdown LVDS LVPECL 1600 LVDS
SDCLK Source
SYSREF Device Clock SYSREF SYSREF
SDCLK TypeInvert
Powerdown
SDCLK EN/DIS State
Active/Active
SDCLKout_PD
DCLKout_DDLY_PD
DCLKout_HSg_PD
DCLKout_ADLYg_PD
DCLKout_ADLY_PD
Idle
HARDWARE CONNECTED
Texas Instruments

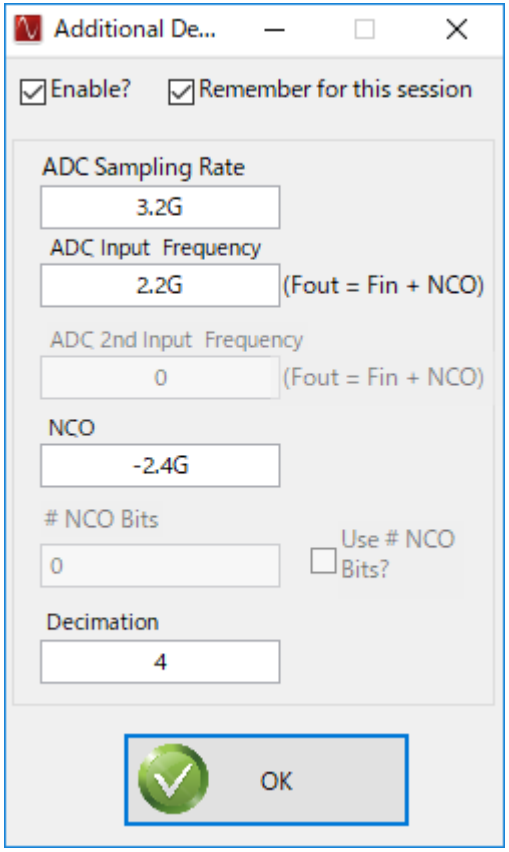

ADC12DJ3200 GUI
File
Debug
Settings
Help
ADC12DJxx00 GUI
Select the device
ADC12DJ3200
EVM
Control
JESD204B
NCO Configuration
Trim
LMK04828
LMX2582
Low Level View
USB Status
Reconnect?
PLL R Pre
1
Ref Doubler
OScin
2x
Pre-R Divider
REF EN
Mult
1
Multiplier
PLL_R
1
Post-R Divider
MUX
PFD DLY Sel
6 clk delay
PFD CTL
Dual PFD
PFD
CP EN
CP Coarse Gain
No
Charge Pump
Ch Pump Gain
0.468mA
Mash en
Mash Order
7
Delta Sigma Mod
VCO
PLL N Pre
Div by 2
PLL NUM
0x000000
PLL DEN
0x0003E8
PLL N
32
N Counter
Reset, Powerdown
RESET
Pwr DN
Lock Det En
Seg1 En
Seg2 En
Seg3 En
Seg1
Seg2
Seg3
Ch Div Seg1
Div by 2
Ch Div Seg2
PD
Ch Div Seg3
PD
Ch Div En
Ch Div Seg Sel
Include Seg1
OUTA MUXSEL
Ch Divout
ChDiv OutA E
OUTA PD
BufA
OUTA Pow
0
ChDiv OutB En
OUTB PD
BufB
OUTB MUXSEL
Ch Div Out
OUTB Pow
60
Idle
HARDWARE CONNECTED
Texas Instruments

# JMODE11 (fnco=2400M)

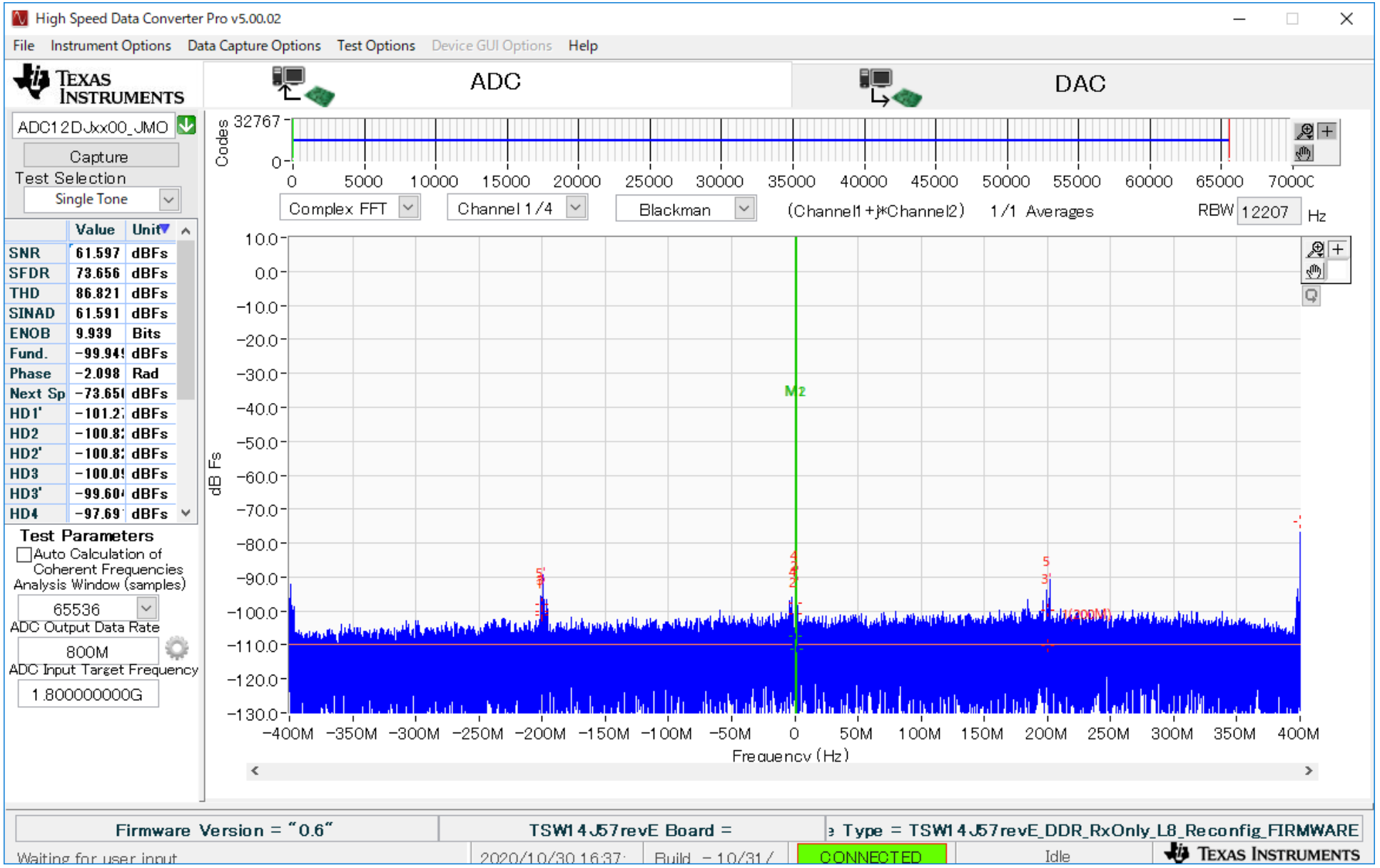
- In the HSDC Pro v5.00.02 that has been opened above :
- Select the ADC12DJxx00_JMODE11 device from the ADC select pull-down.
  - LEDs D5, D8 and D9 turn on. LED, D2, flashes. LEDs, D1, D3, D6 and D7 turn off. (LED, D3, often turn on)
  - Firmware version = "0.6". The interface type = TSW14J57revE_DDR_RxOnly_L8_Reconfig_FIRMWARE.
- Popup will display "The Sampling Rate entered exceeds the maximum rating of the ADC selected.", click OK.
- Popup will display "New lane rate is 54G, JESD ref-clock is 1.35G", Click OK.

# JMODE11 (fnco=2400M)

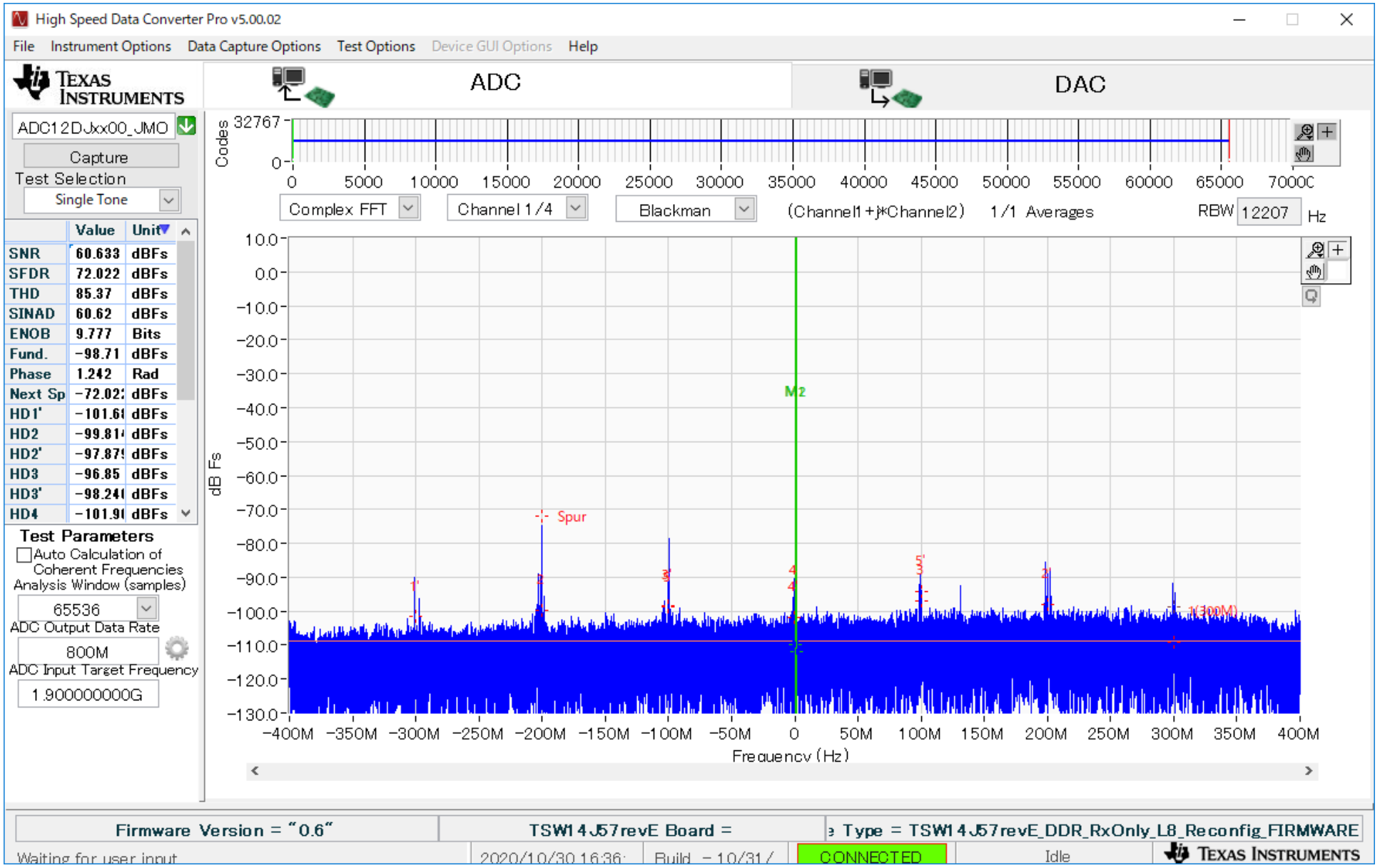
- Toggle the ADC Output Setup icon
  - Check Enable? and Remember for this session
  - ADC sample rate = 3.2G
  - ADC input freq = 2200M
  - NCO = -2400M
  - Decimation = 4
- Popup will display "New lane rate is 8G, JESD ref-clock is 200M", Click OK.
- Change to Complex FFT
- Click Capture button.


Additional De...
Enable?
Remember for this session
ADC Sampling Rate
3.2G
ADC Input Frequency
2.2G
(Fout = Fin + NCO)
ADC 2nd Input Frequency
0
(Fout = Fin + NCO)
NCO
-2.4G
# NCO Bits
0
Use # NCO Bits?
Decimation
4
OK

# HSDC_jmode11_fs3200M_fnco2400M_fin1800M

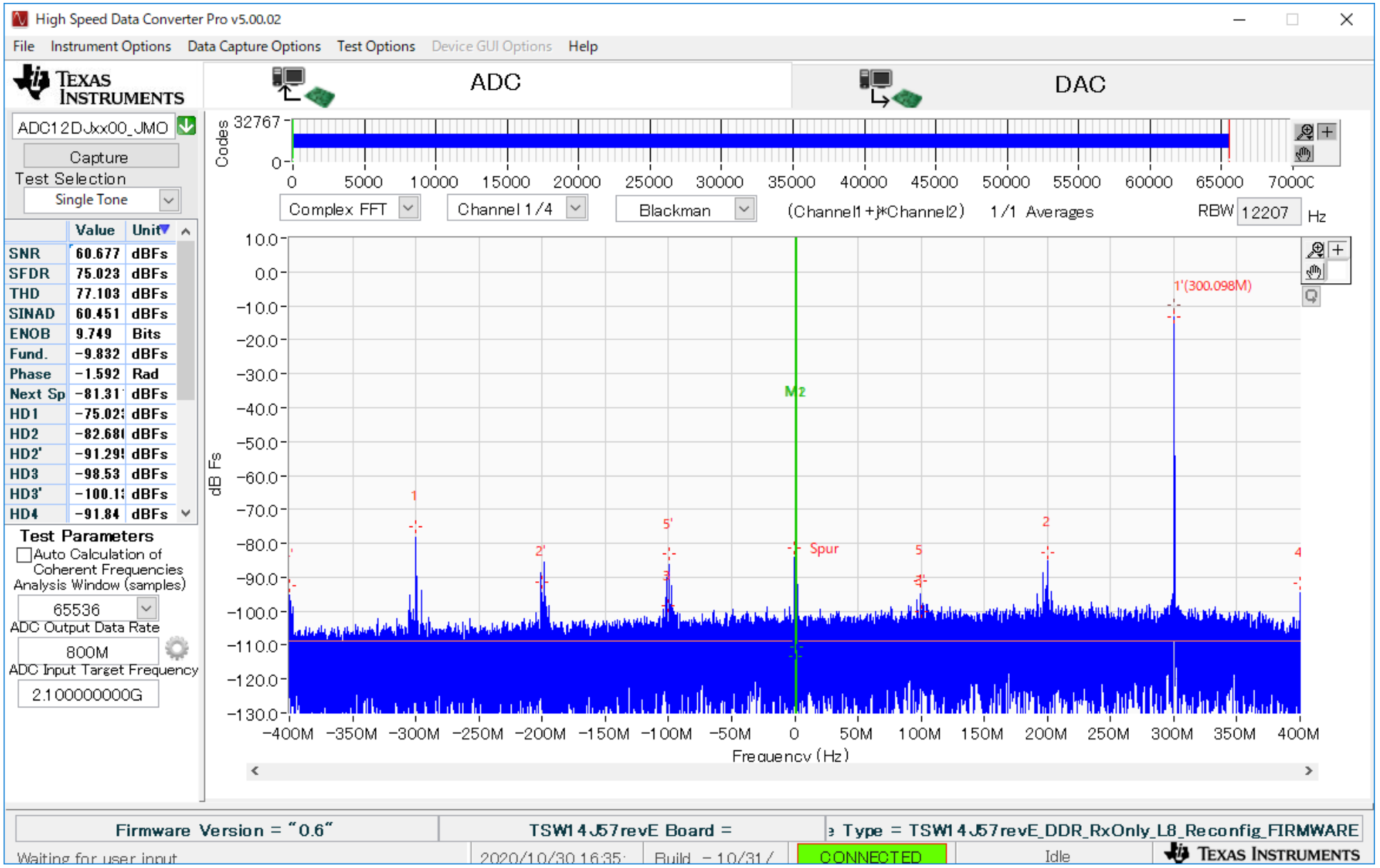


# HSDC_jmode11_fs3200M_fnco2400M_fin1900M

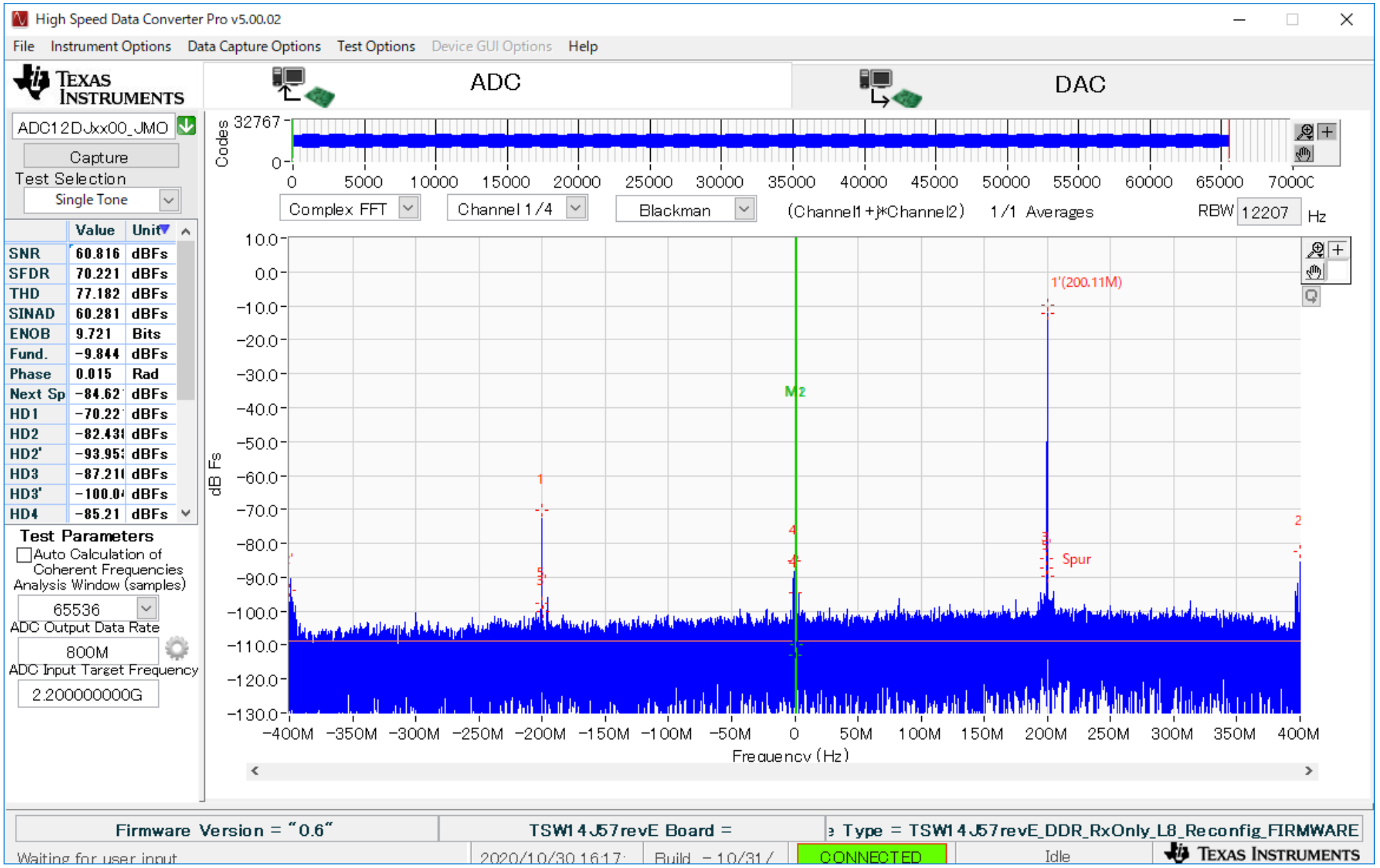


# HSDC_jmode11_fs3200M_fnco2400M_fin2000M

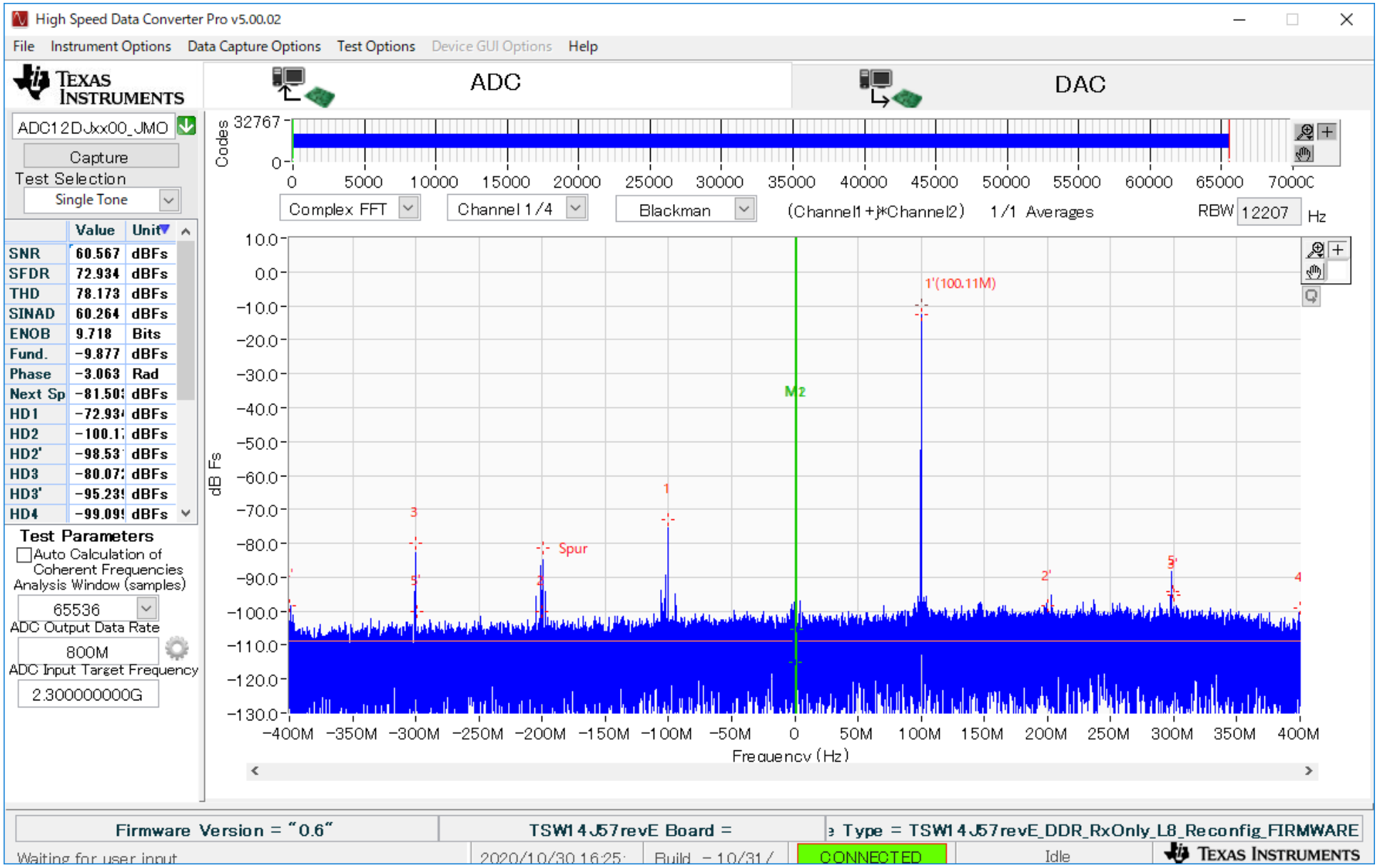
# HSDC_jmode11_fs3200M_fnco2400M_fin2100M



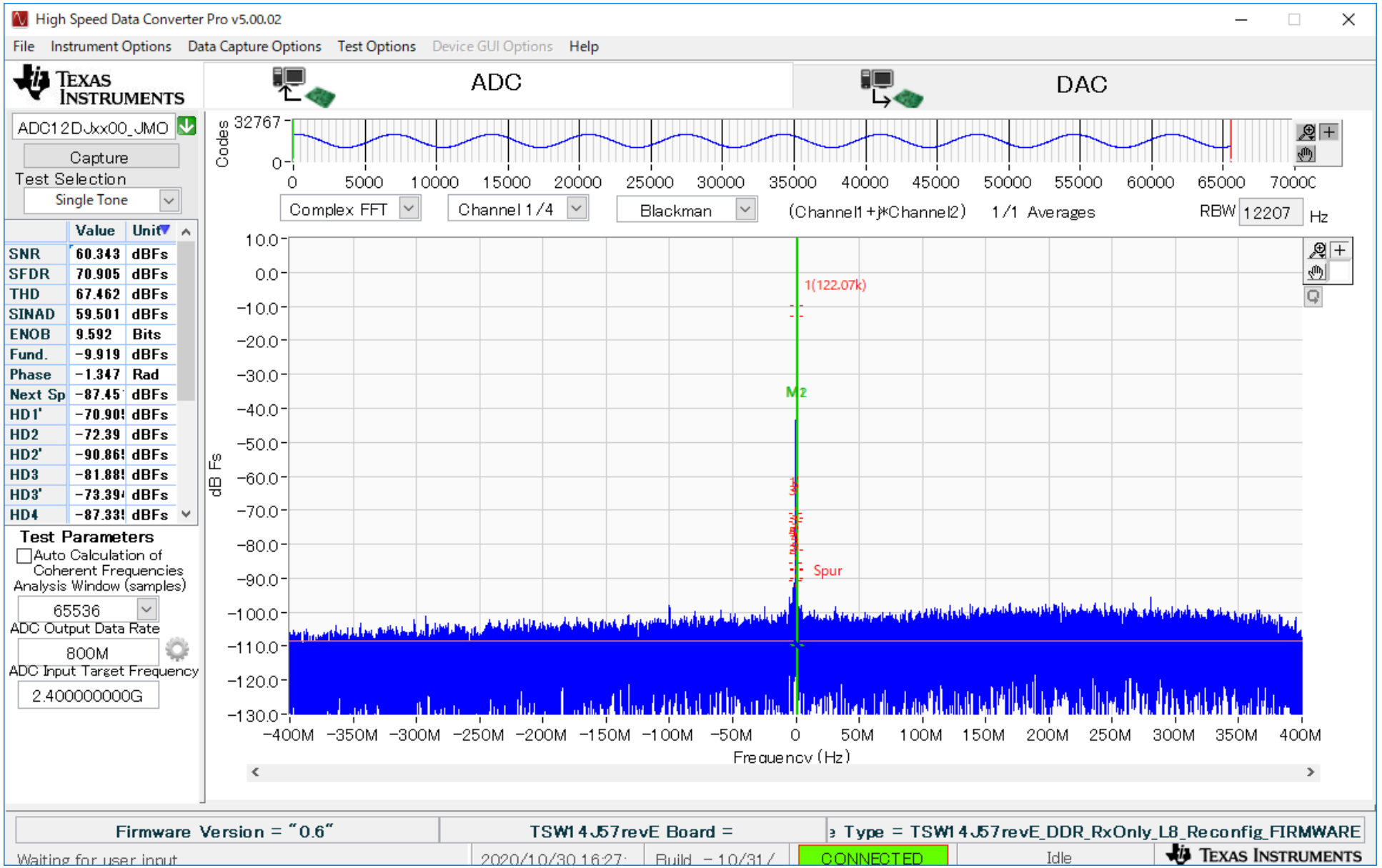
# HSDC_jmode11_fs3200M_fnco2400M_fin2200M



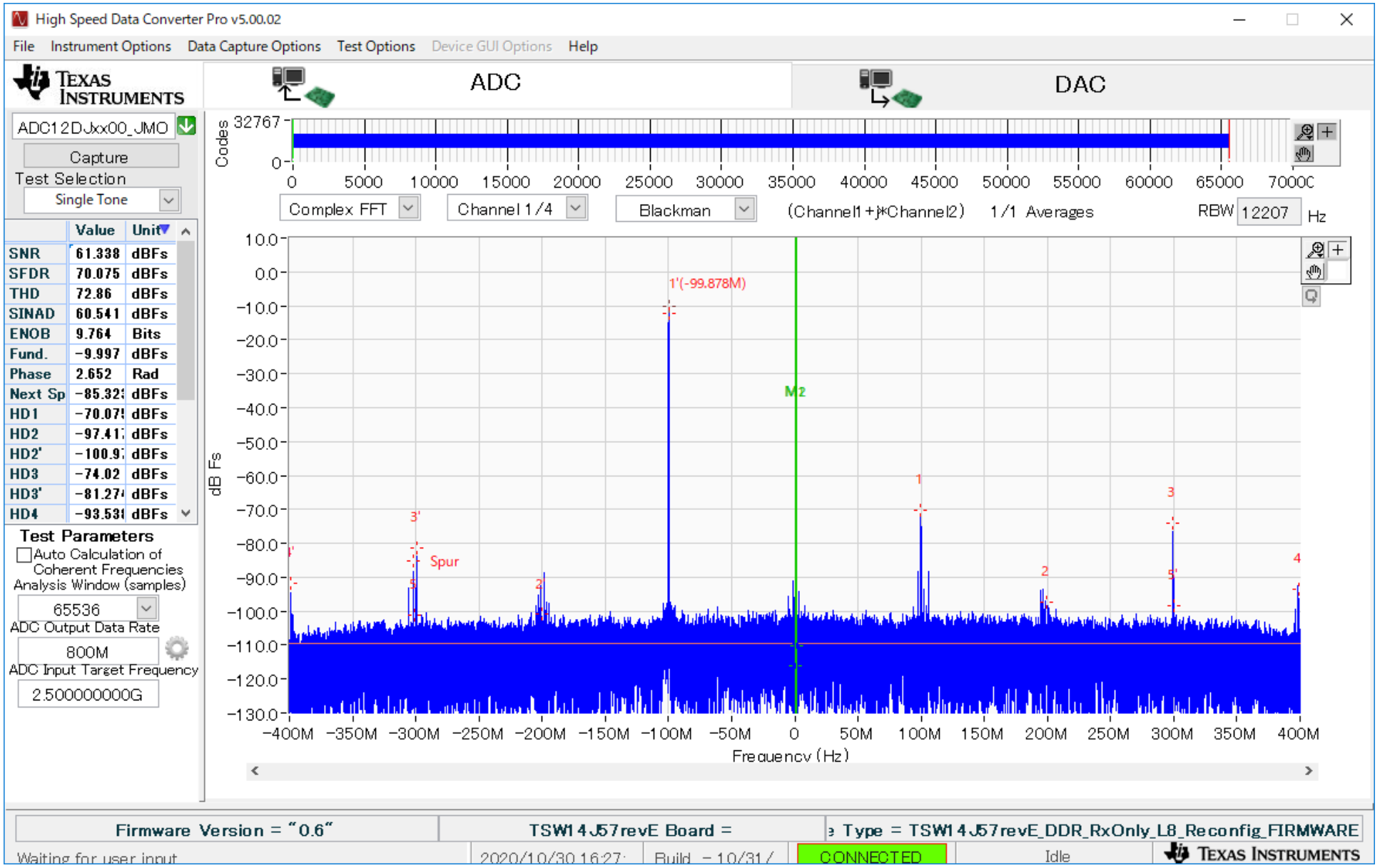
# HSDC_jmode11_fs3200M_fnco2400M_fin2300M



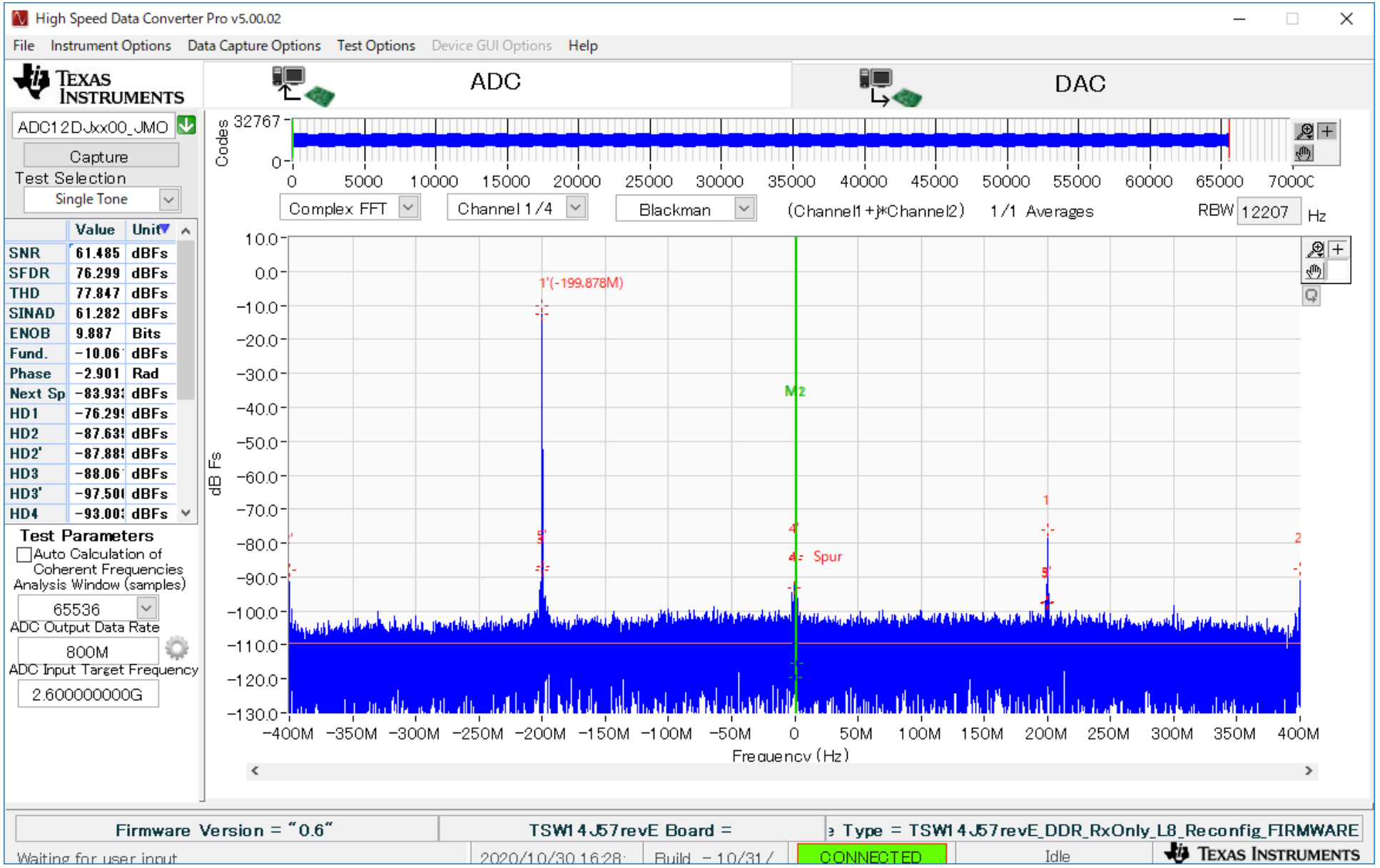
# HSDC_jmode11_fs3200M_fnco2400M_fin2400M



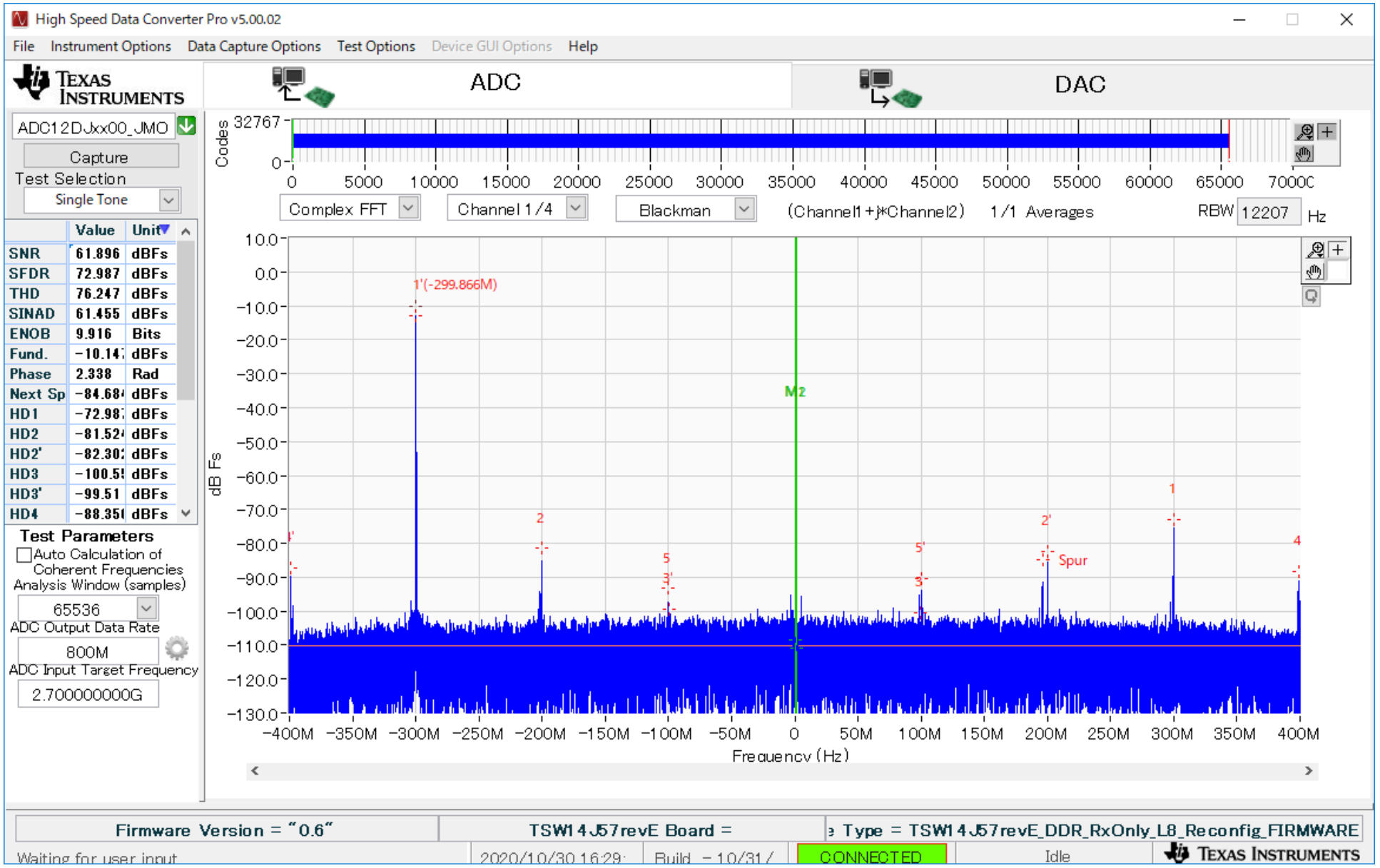
# HSDC_jmode11_fs3200M_fnco2400M_fin2500M



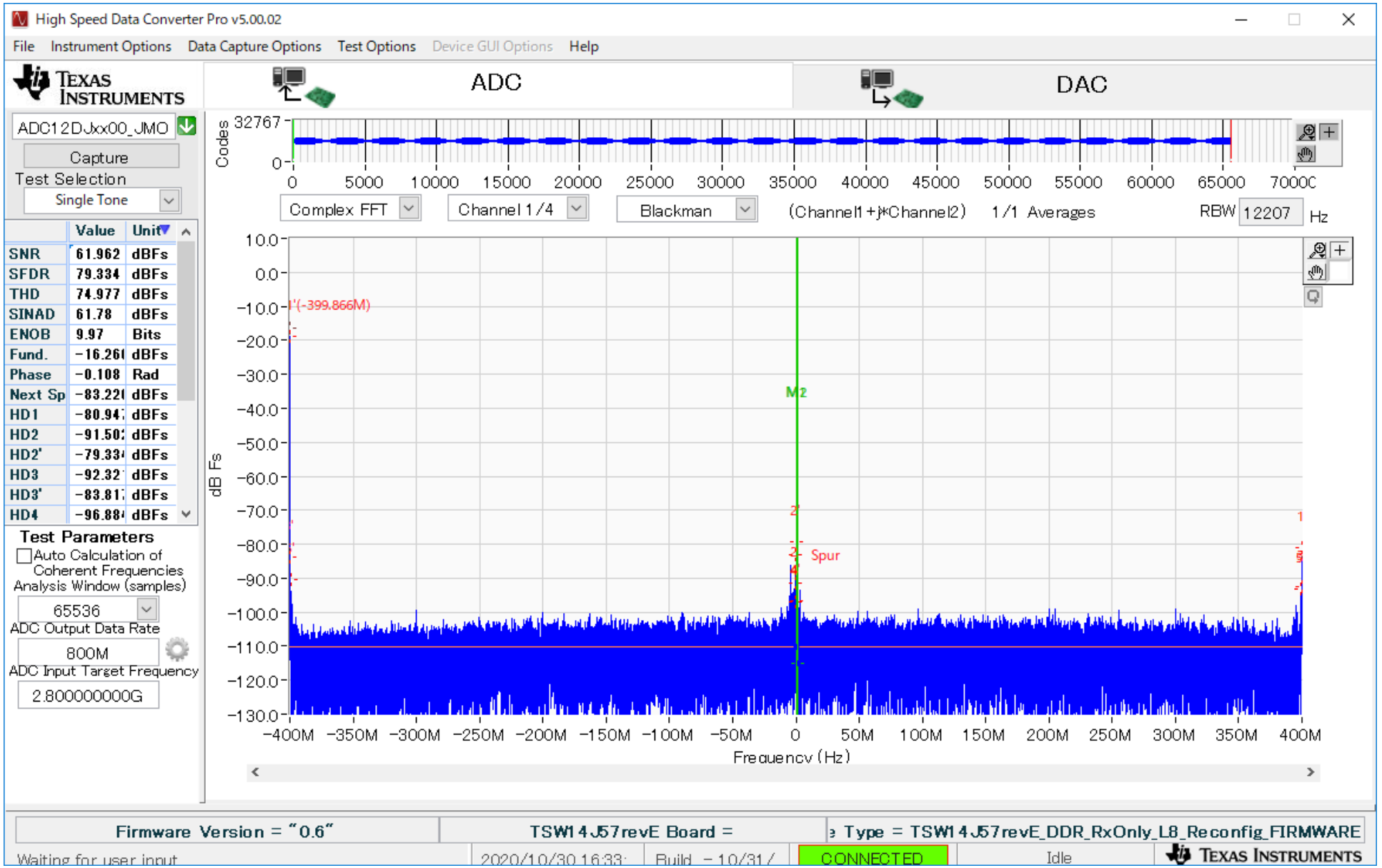
# HSDC_jmode11_fs3200M_fnco2400M_fin2600M



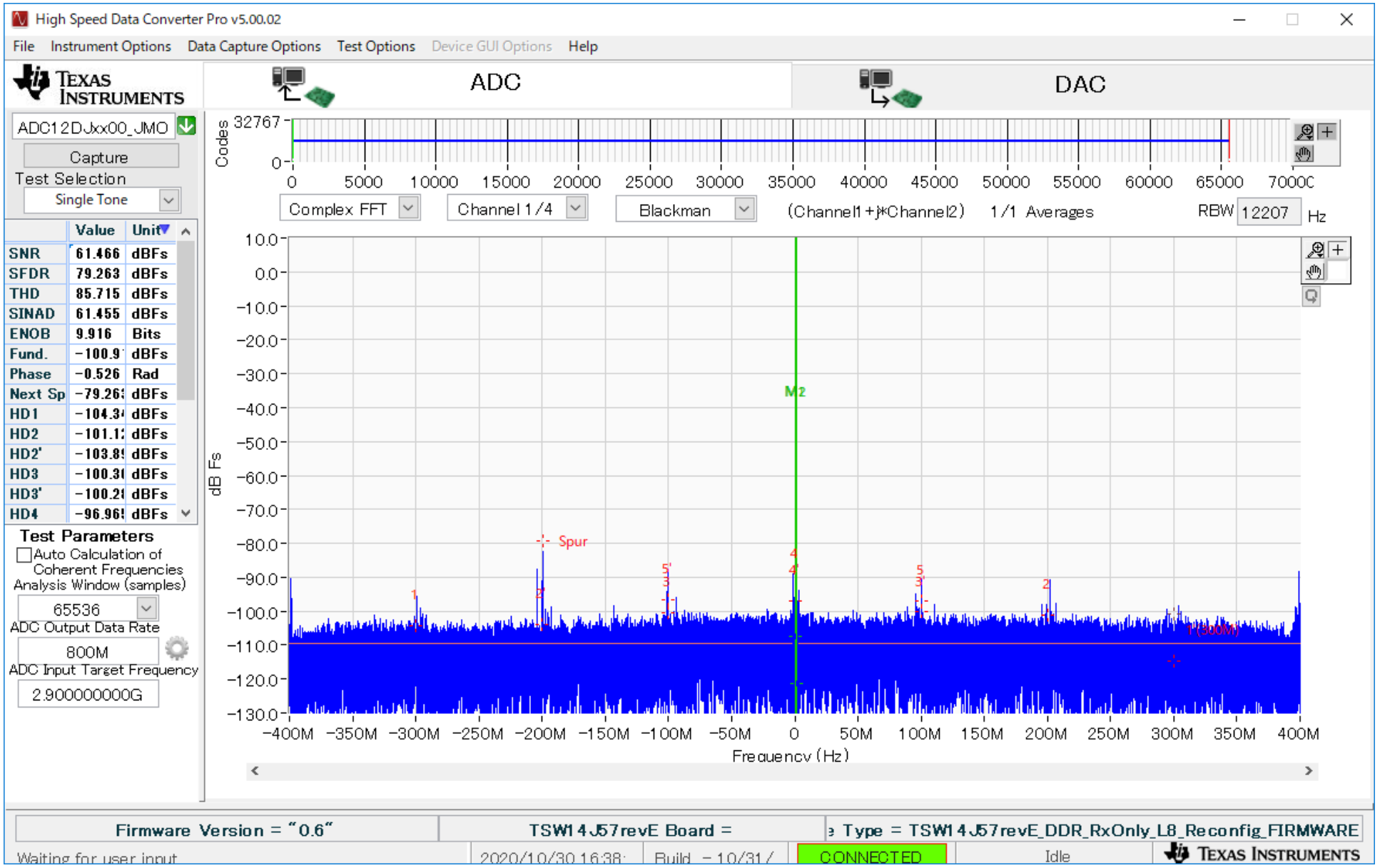
# HSDC_jmode11_fs3200M_fnco2400M_fin2700M



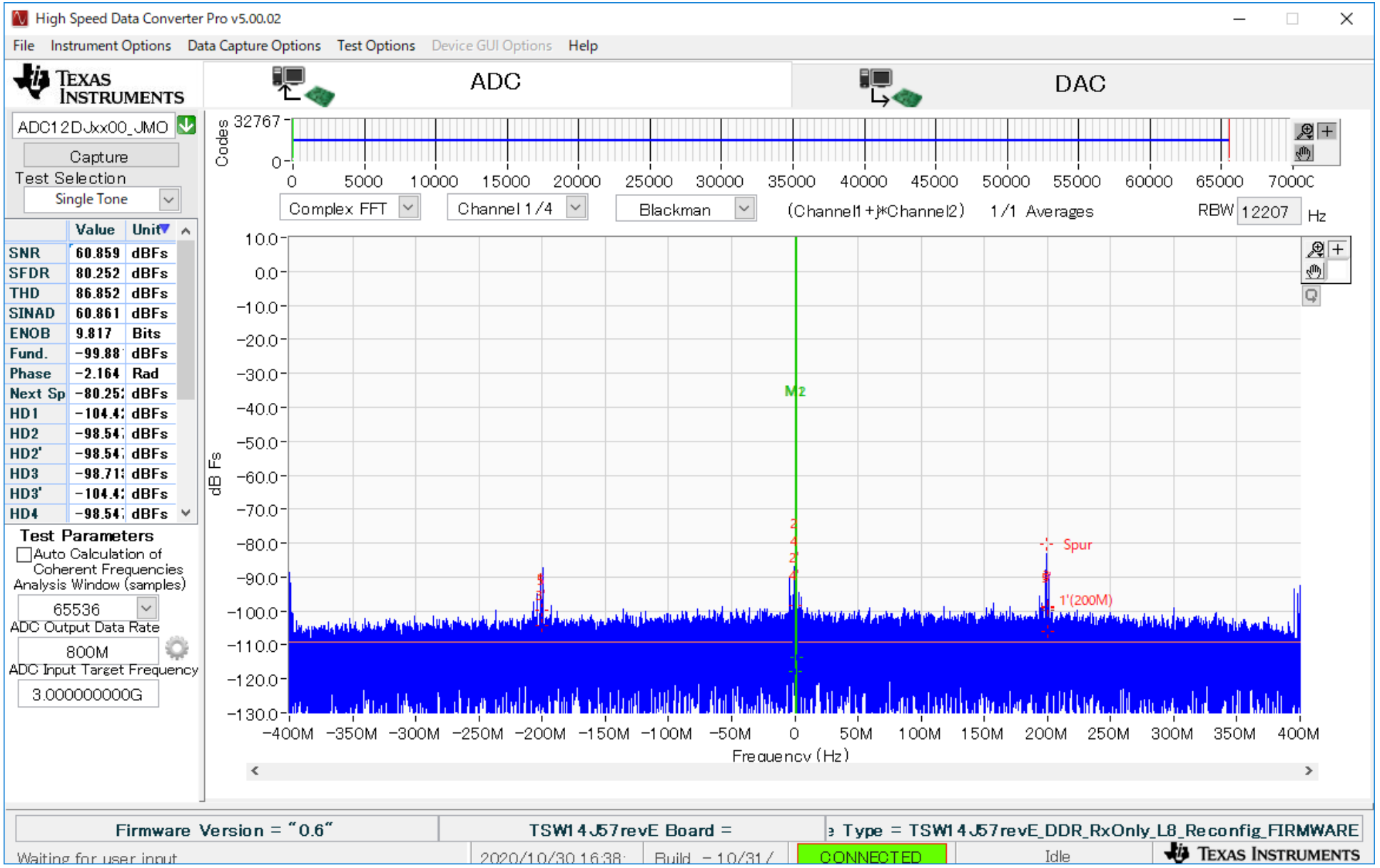
# HSDC_jmode11_fs3200M_fnco2400M_fin2800M



# HSDC_jmode11_fs3200M_fnco2400M_fin2900M



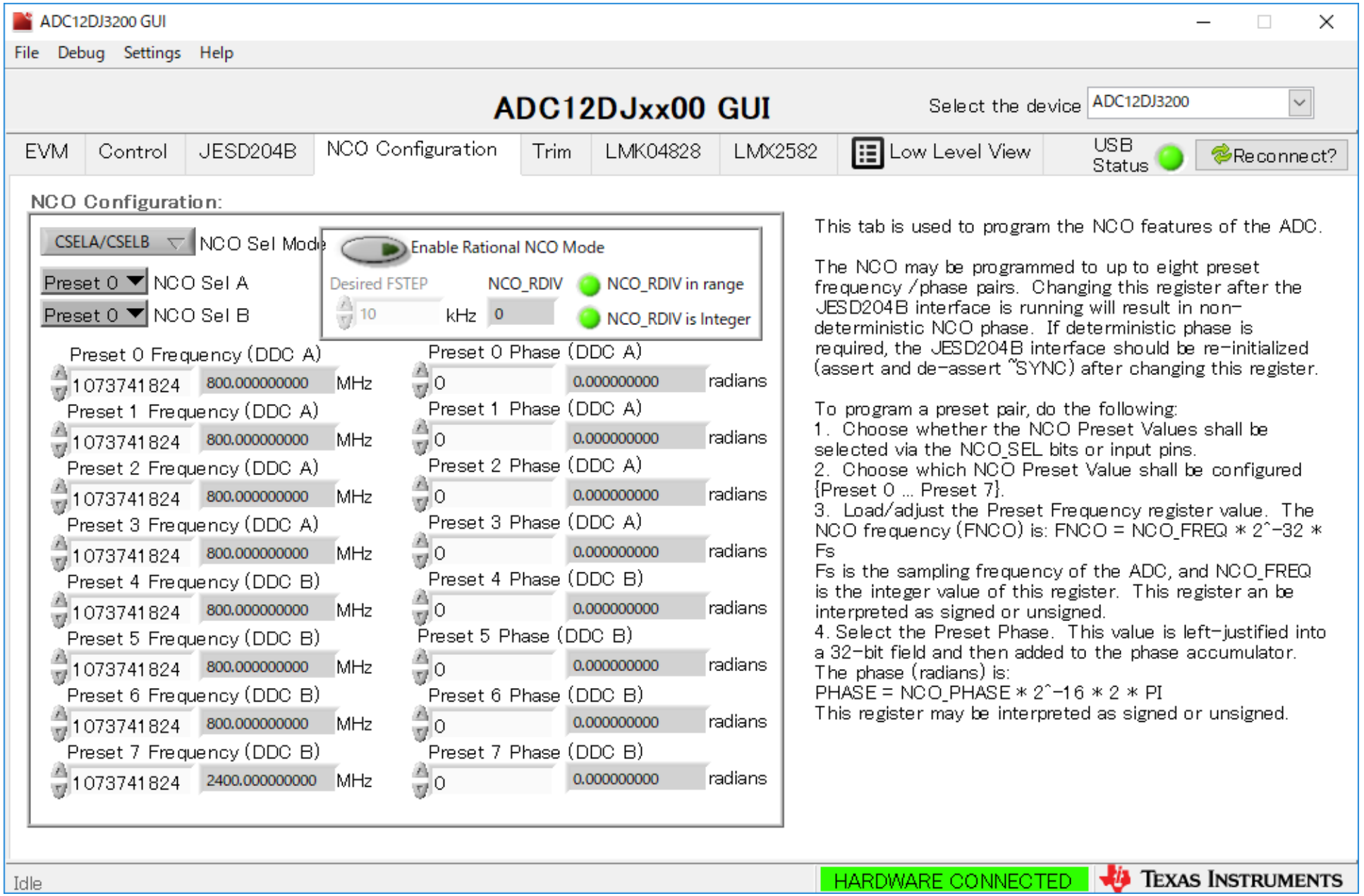
# HSDC_jmode11_fs3200M_fnco2400M_fin3000M



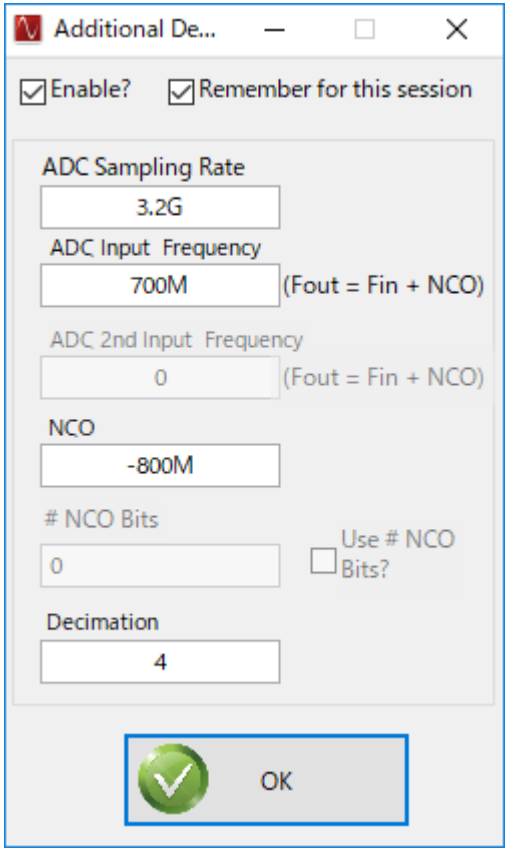
# 3

JMODE=11, Fs=3200MSPS,
NCO=800MHz, Fin=700 and 1000MHz
(1st Nyquist Zone)
IQ seemed to be swapping. The largest spectrum of the HSDC complex FFT was marked with the 1' marker. The same result was obtained when IQ data exported from HSDC was FFT by MATLAB.

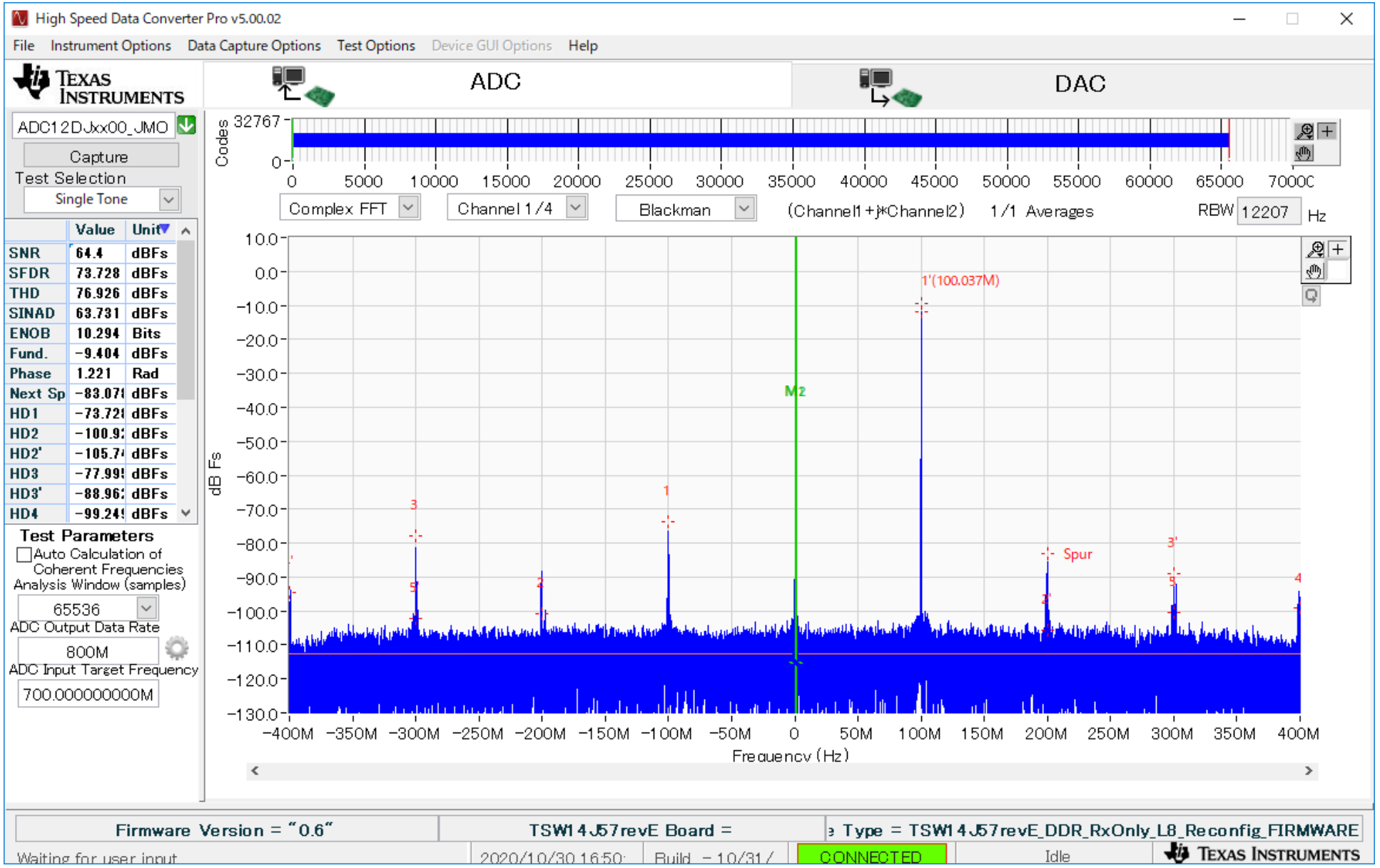
# Change the NCO frequency to 800MHz



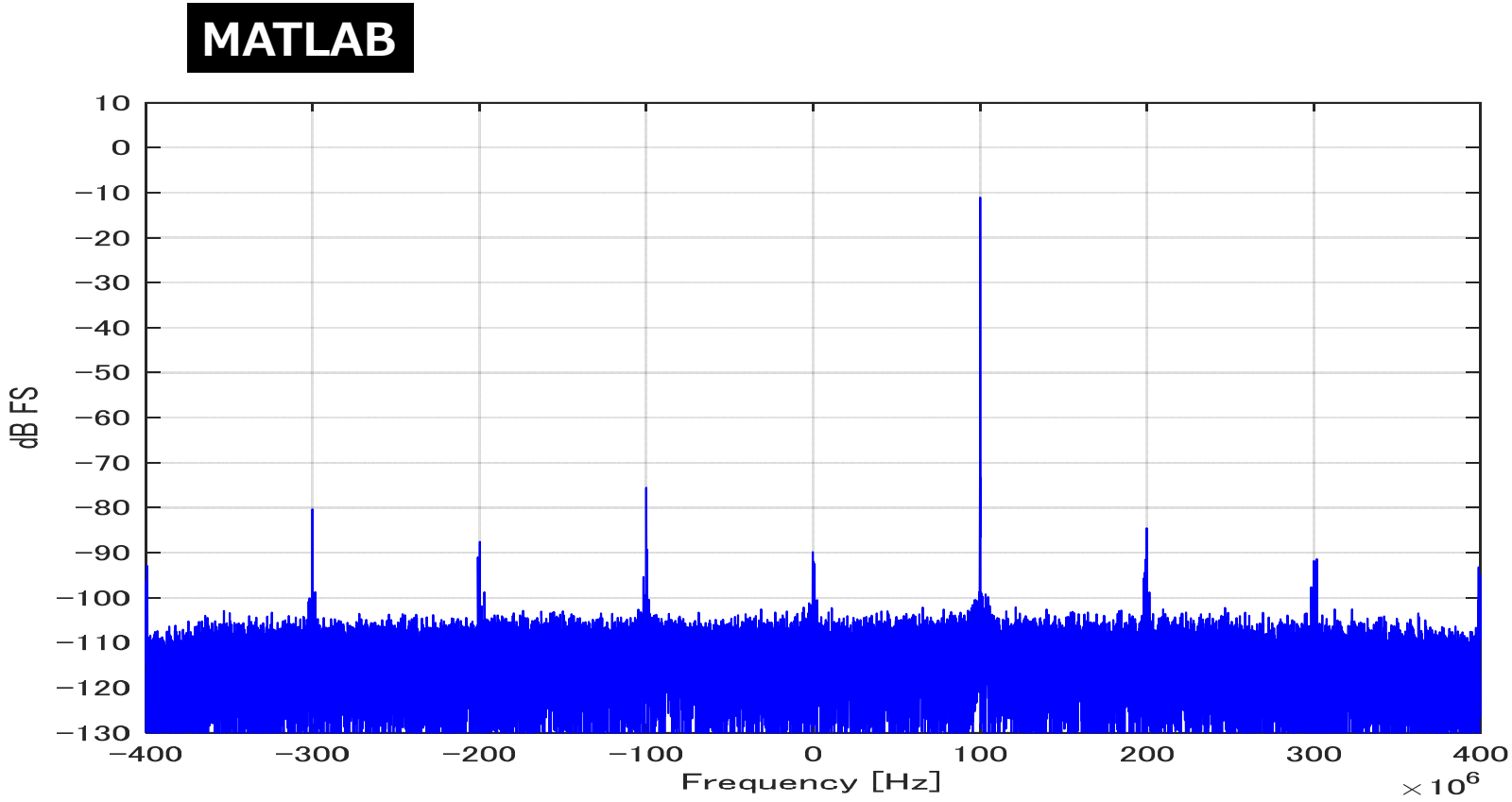
# Change the NCO and input frequency



# HSDC_jmode11_fs3200M_fnco800M_fin700M

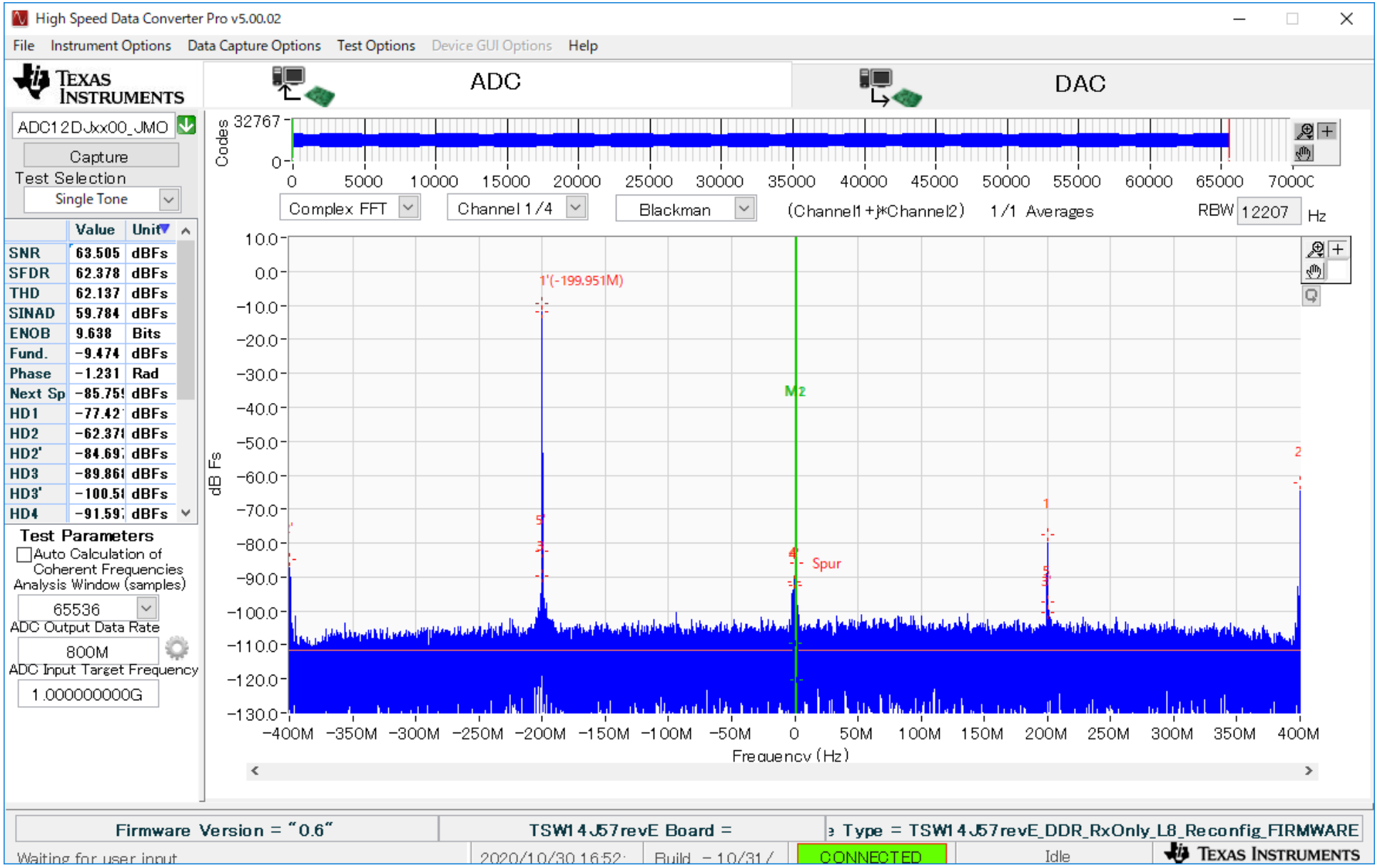


# FFT results by MATLAB for IQ data exported from HSDC

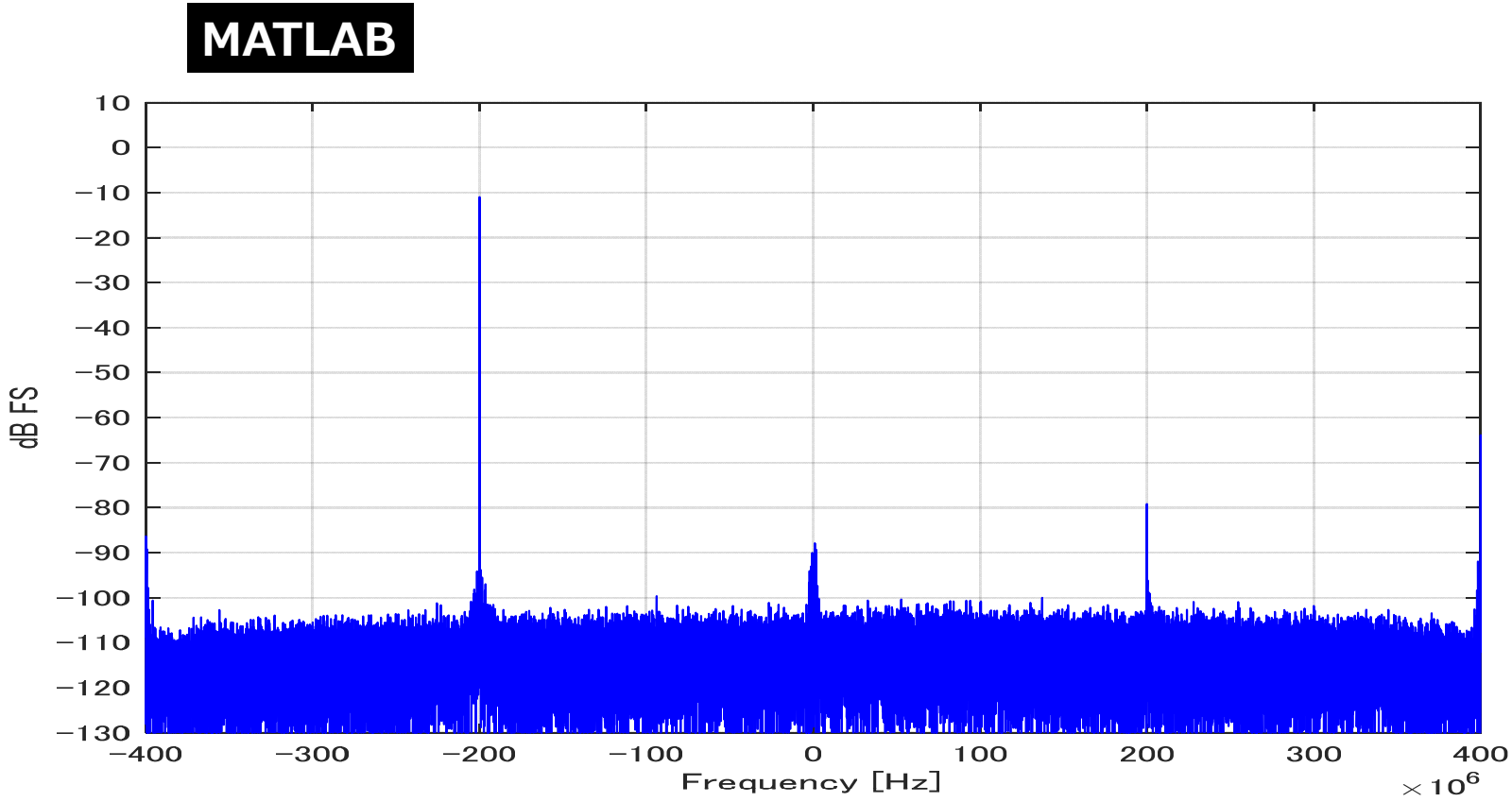



The results are very similar, but the marker index (primes) are reversed.

# HSDC_jmode11_fs3200M_fnco800M_fin1000M



# FFT results by MATLAB for IQ data exported from HSDC

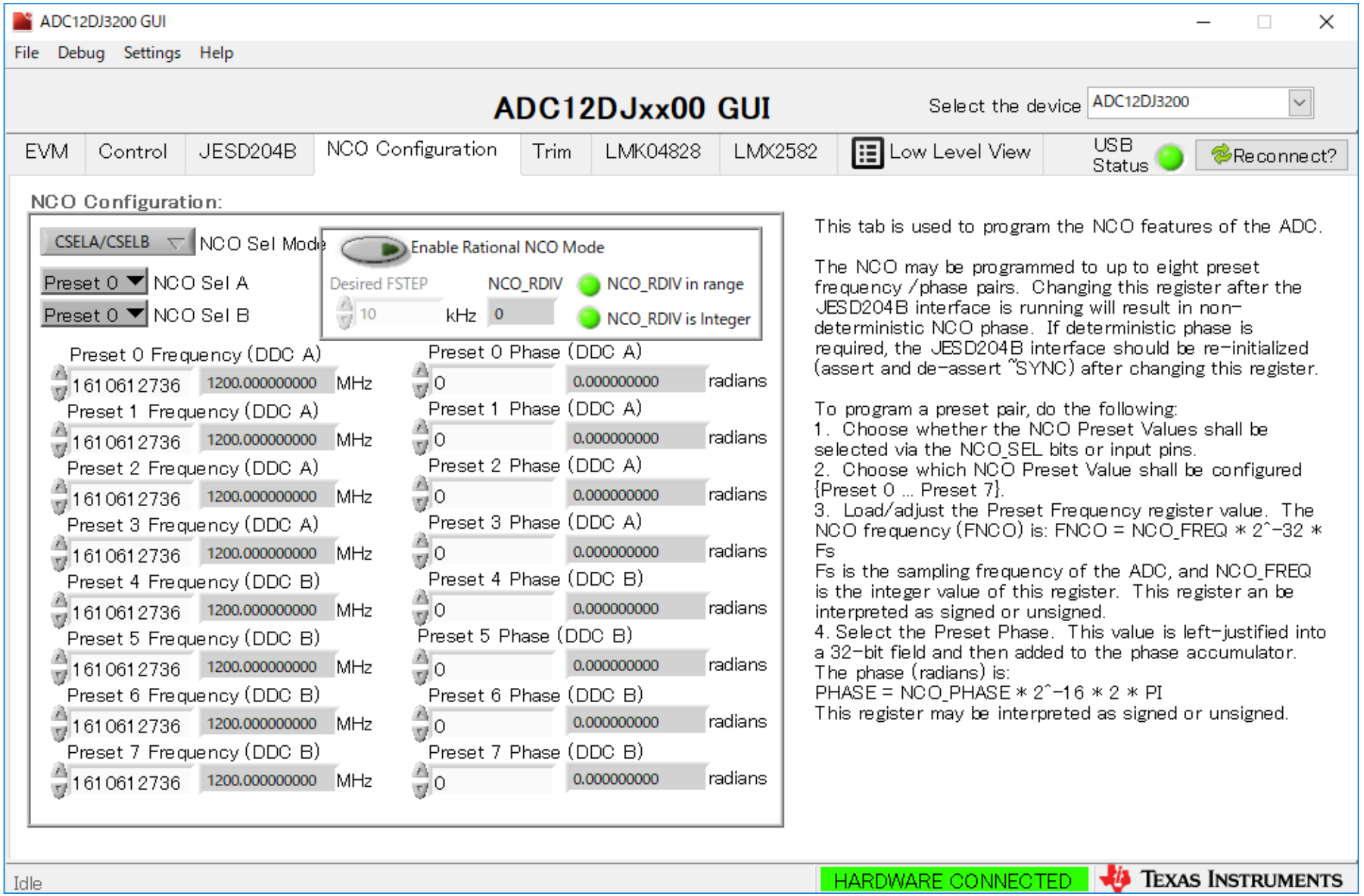



The results are very similar, but the marker index (primes) are reversed.

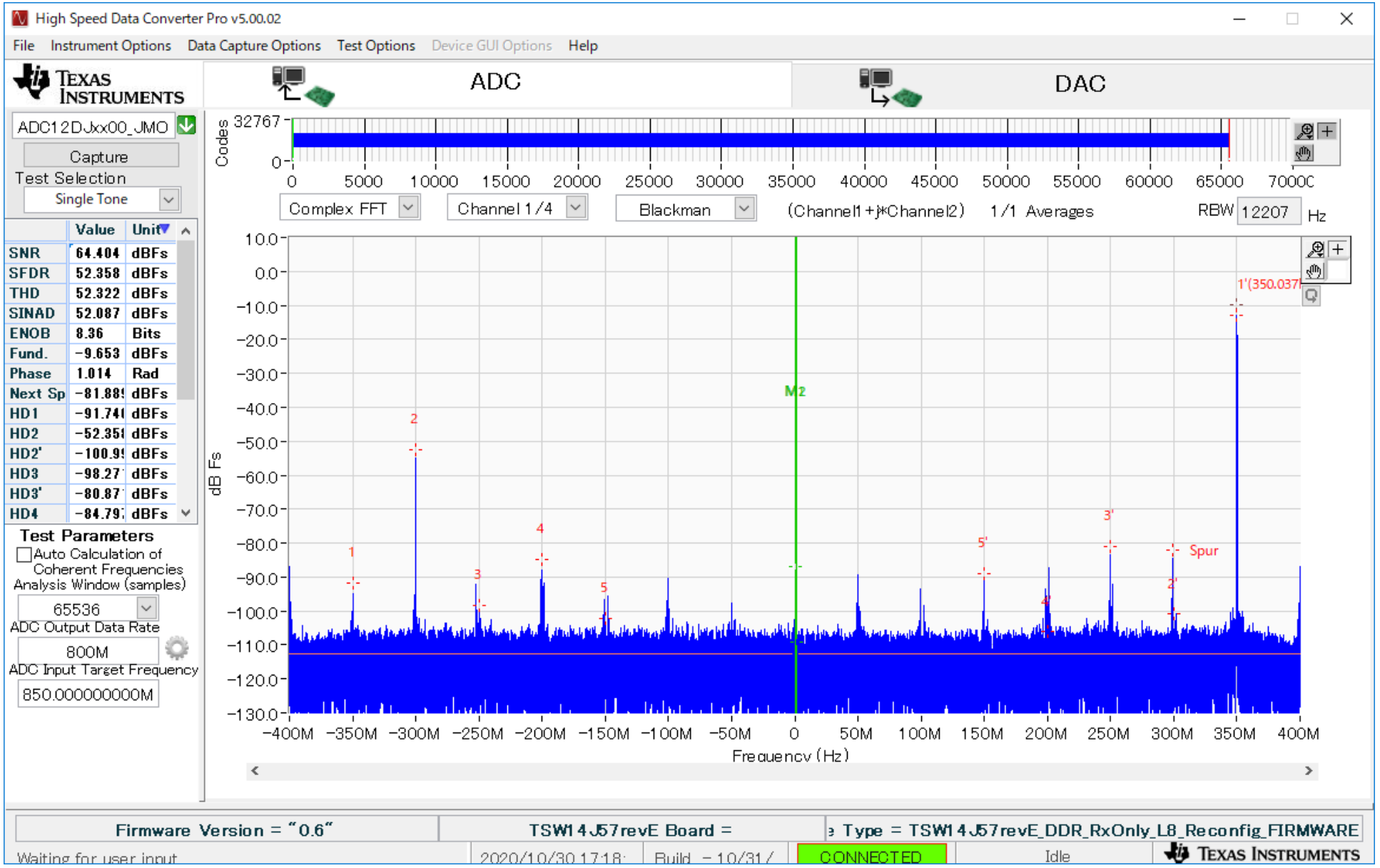
# 4

JMODE=11, Fs=3200MSPS,
NCO=1200MHz, Fin=850 to 1550MHz
(1st Nyquist Zone)
IQ seemed to be swapping. The largest spectrum of the HSDC complex FFT was marked with the 1' marker. Sometimes the FFT results are different between HSDC and MATLAB.

# Change the NCO frequency to 1200MHz

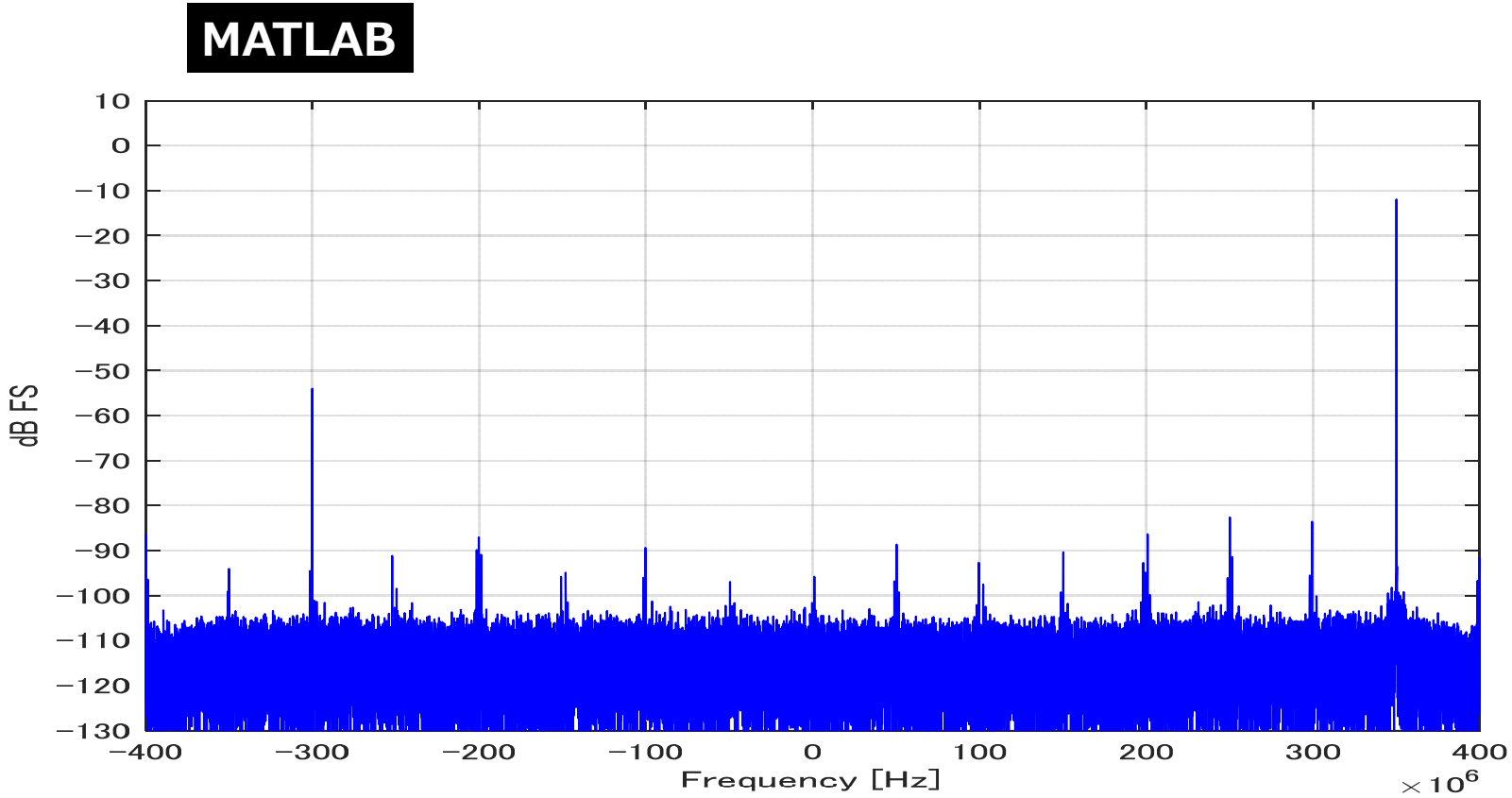


# HSDC_jmode11_fs3200M_fnco1200M_fin850M



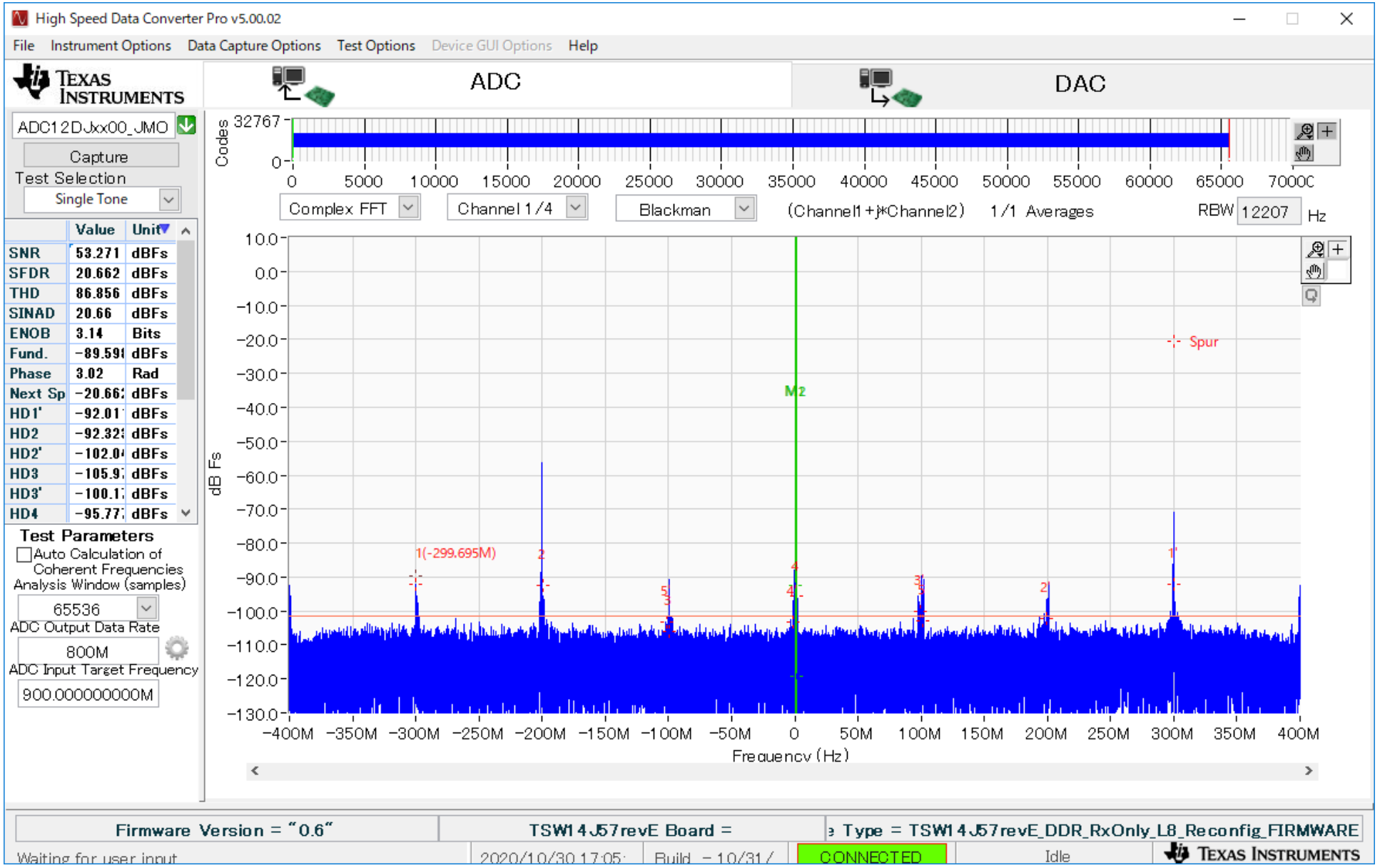
# HSDC_jmode11_fs3200M_fnco1200M_fin850M

FFT results by MATLAB for IQ data exported from HSDC



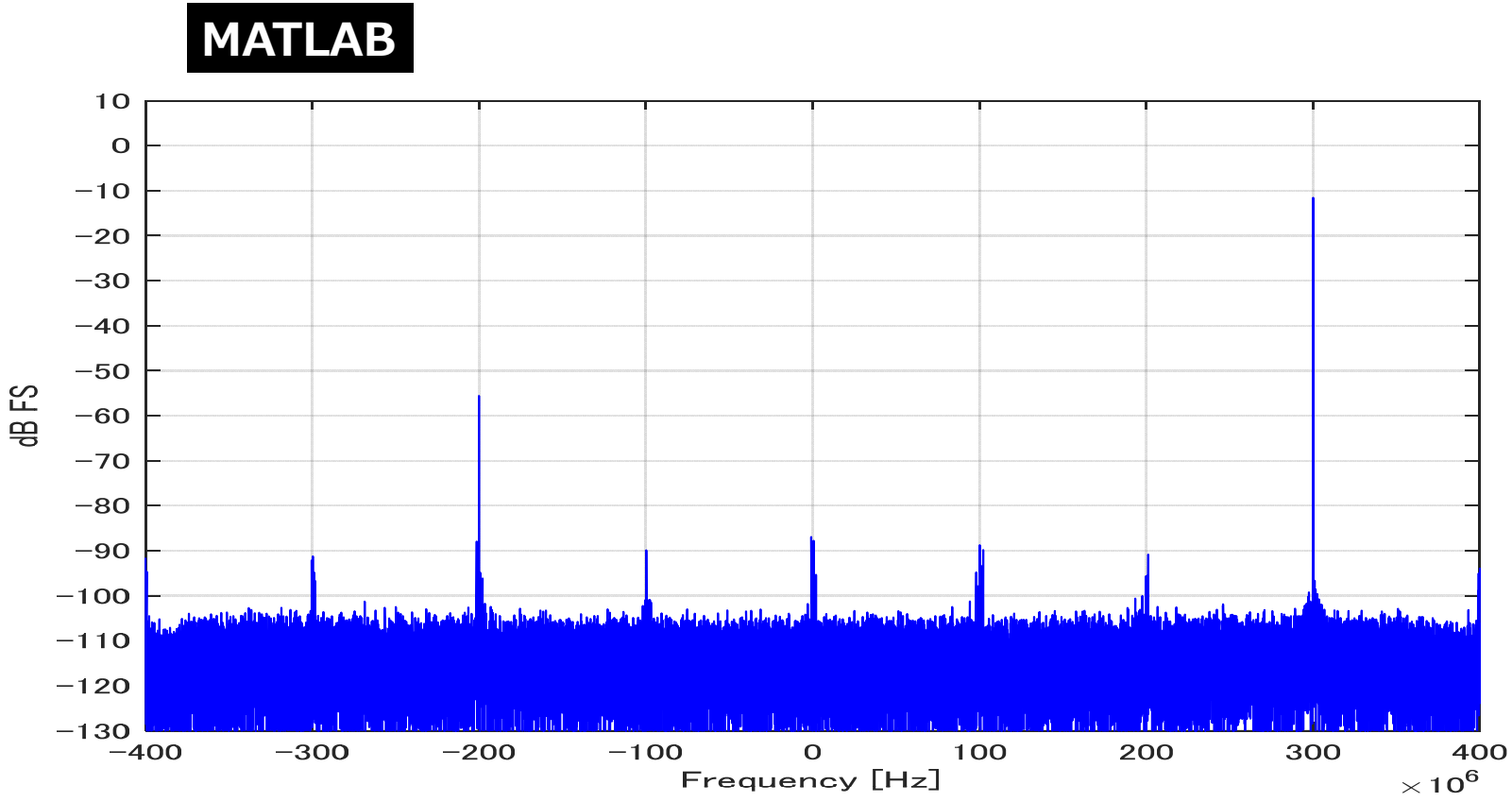

The results are very similar, but the marker index (primes) are reversed.

# HSDC_jmode11_fs3200M_fnco1200M_fin900M



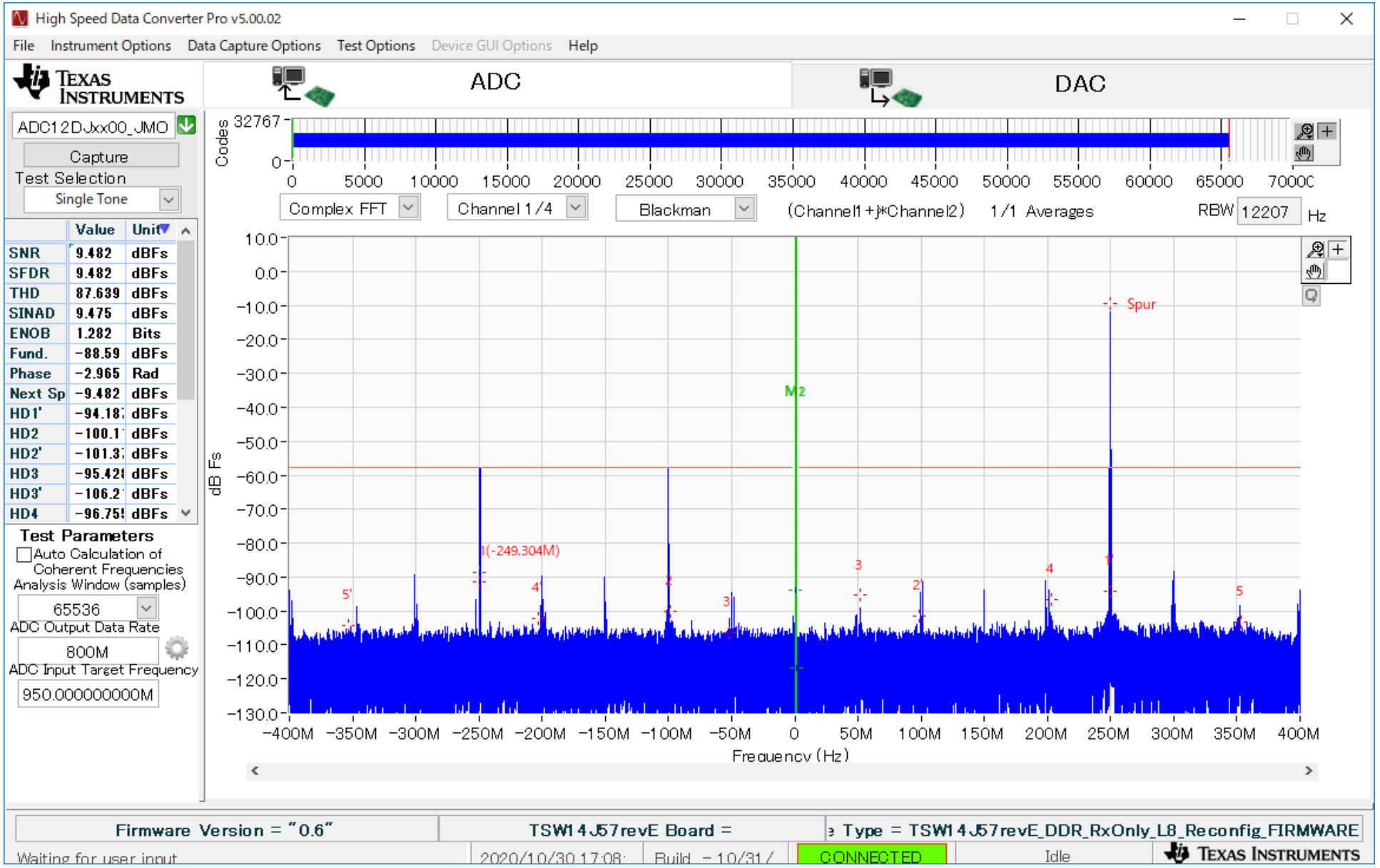
# HSDC_jmode11_fs3200M_fnco1200M_fin900M

FFT results by MATLAB for IQ data exported from HSDC



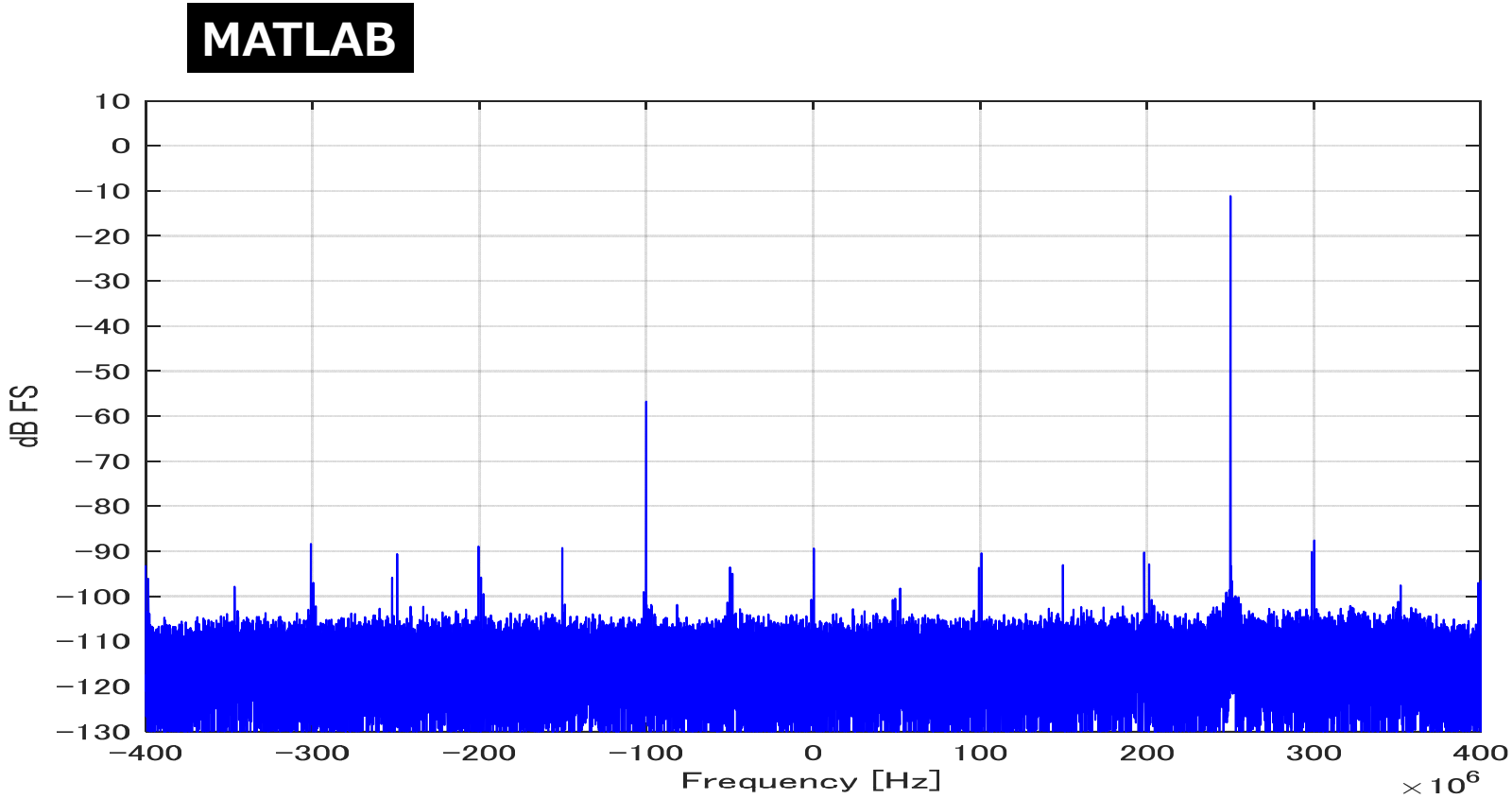

-10dBFS spectrum exists near +300MHz.

# HSDC_jmode11_fs3200M_fnco1200M_fin950M



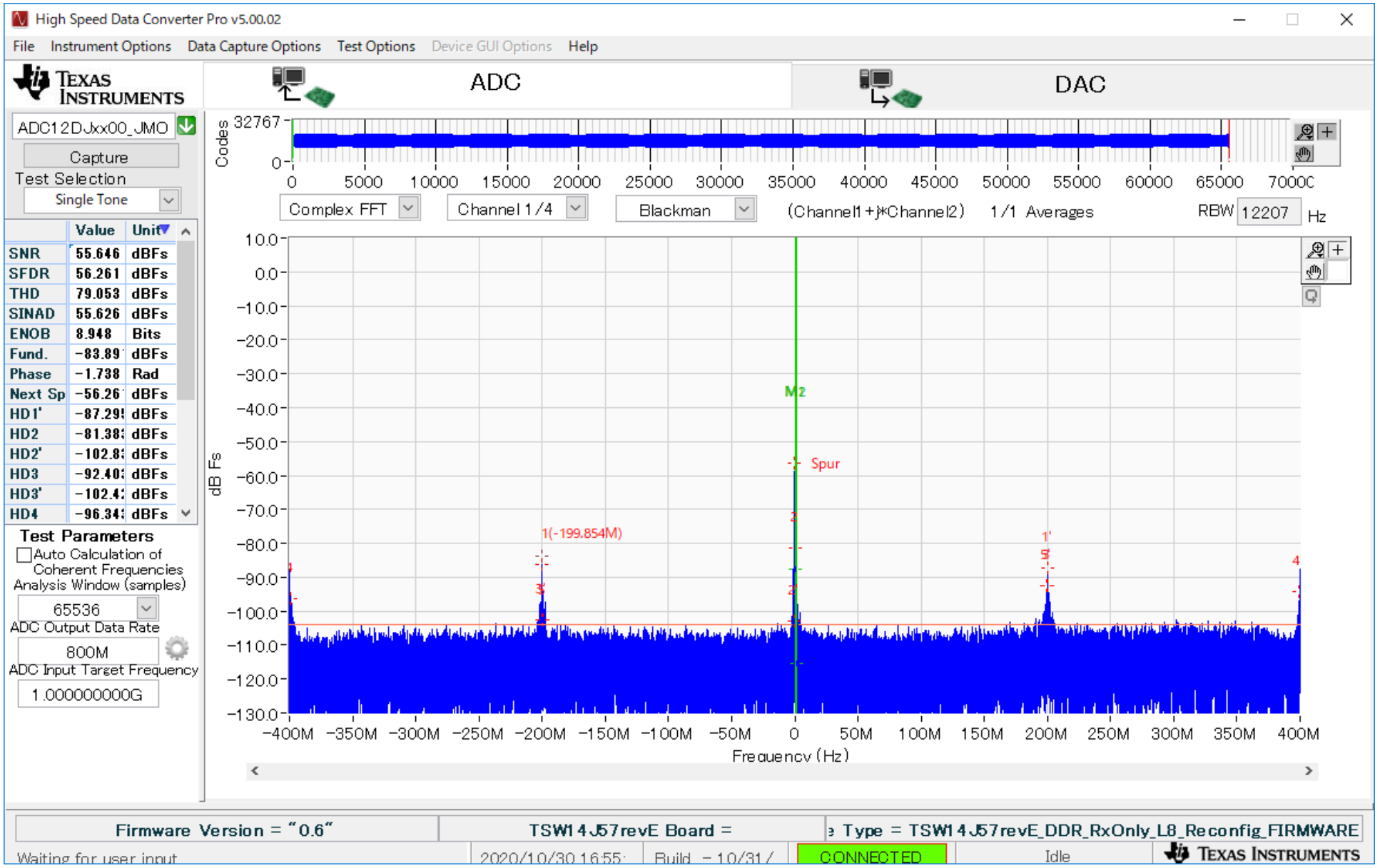
# HSDC_jmode11_fs3200M_fnco1200M_fin950M

FFT results by MATLAB for IQ data exported from HSDC



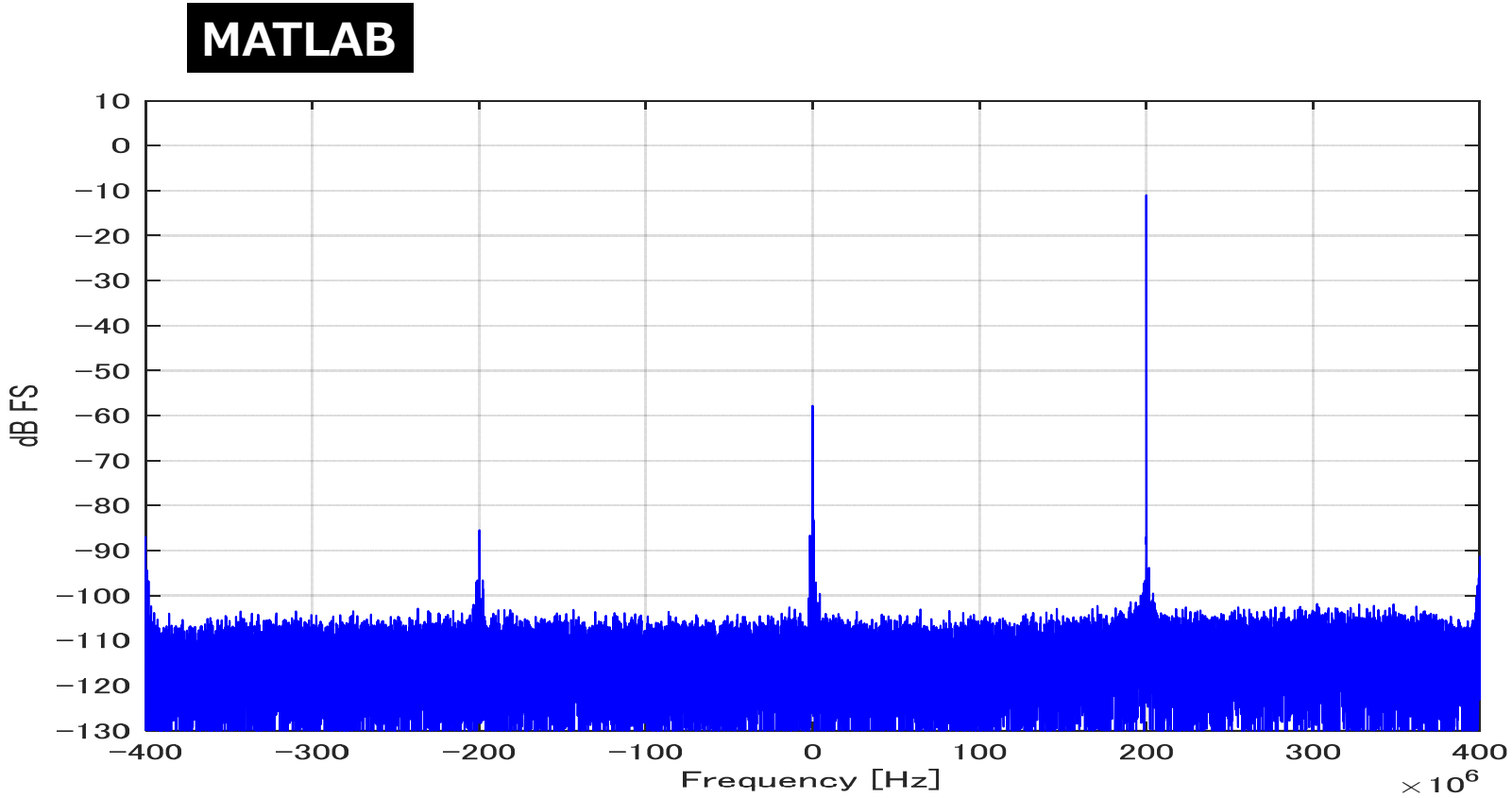

-60dBFS spurious around -250MHz disappears.

# HSDC_jmode11_fs3200M_fnco1200M_fin1000M



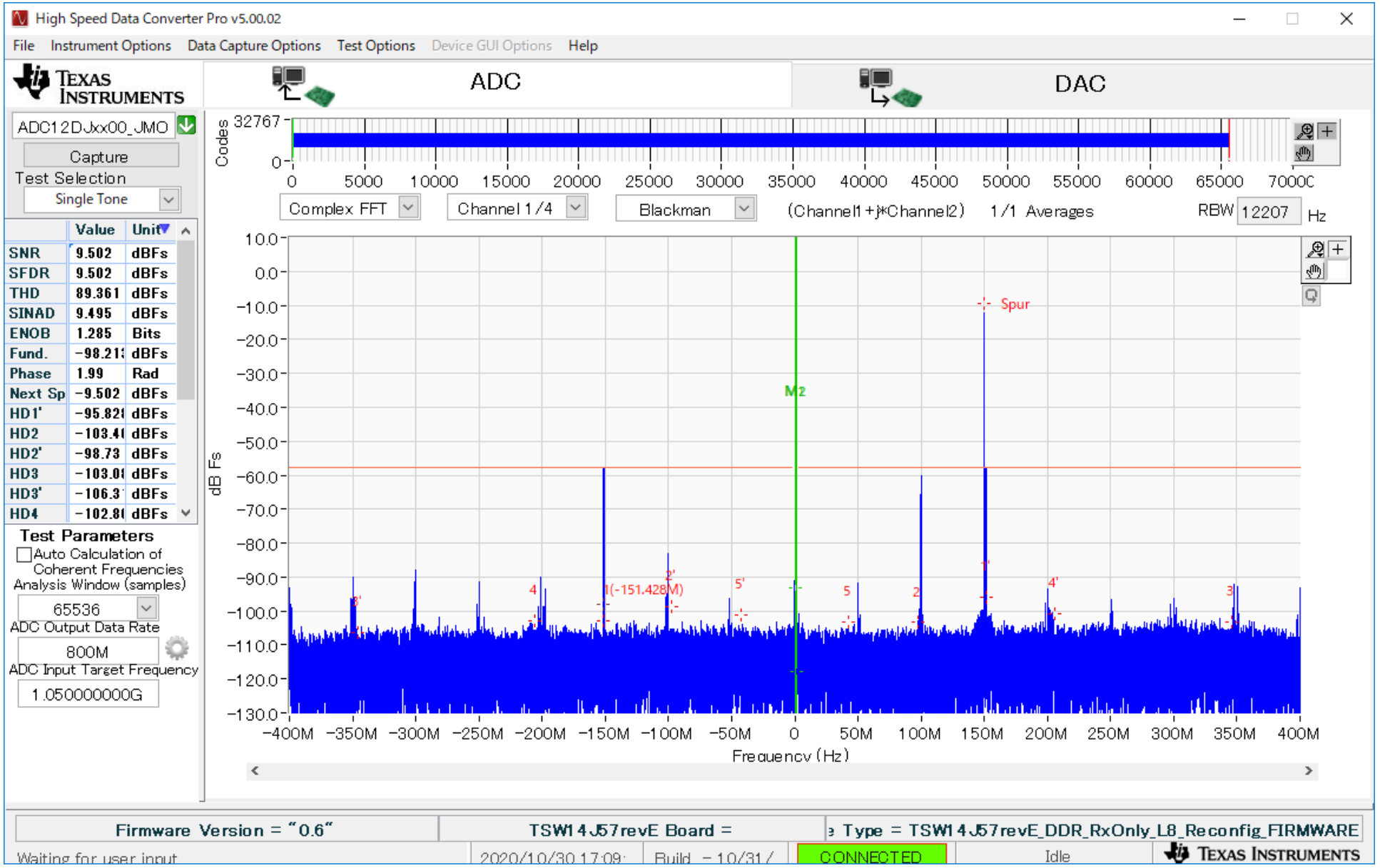
# HSDC_jmode11_fs3200M_fnco1200M_fin1000M

FFT results by MATLAB for IQ data exported from HSDC



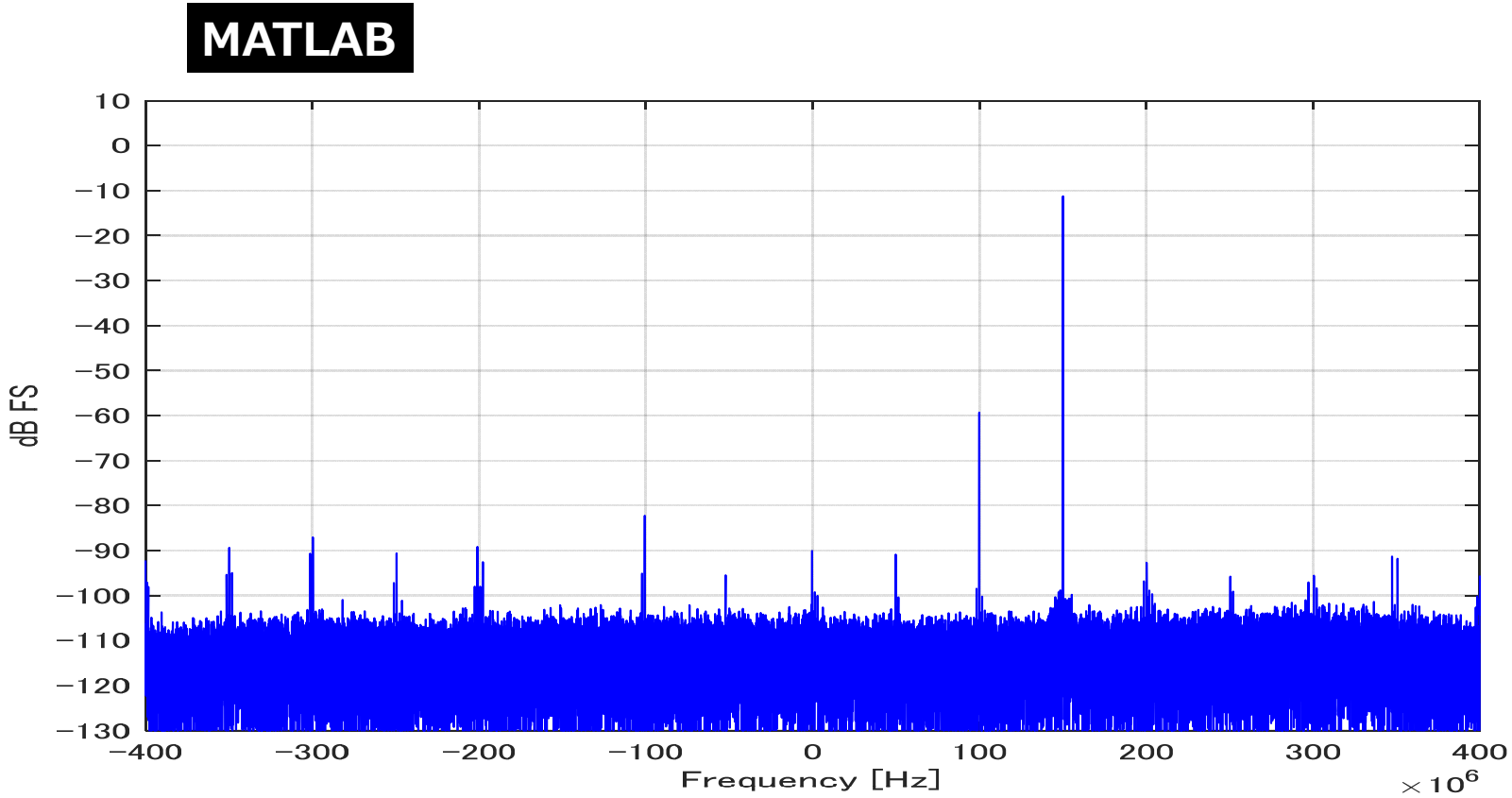

-10dBFS spectrum exists near +200MHz.

# HSDC_jmode11_fs3200M_fnco1200M_fin1050M



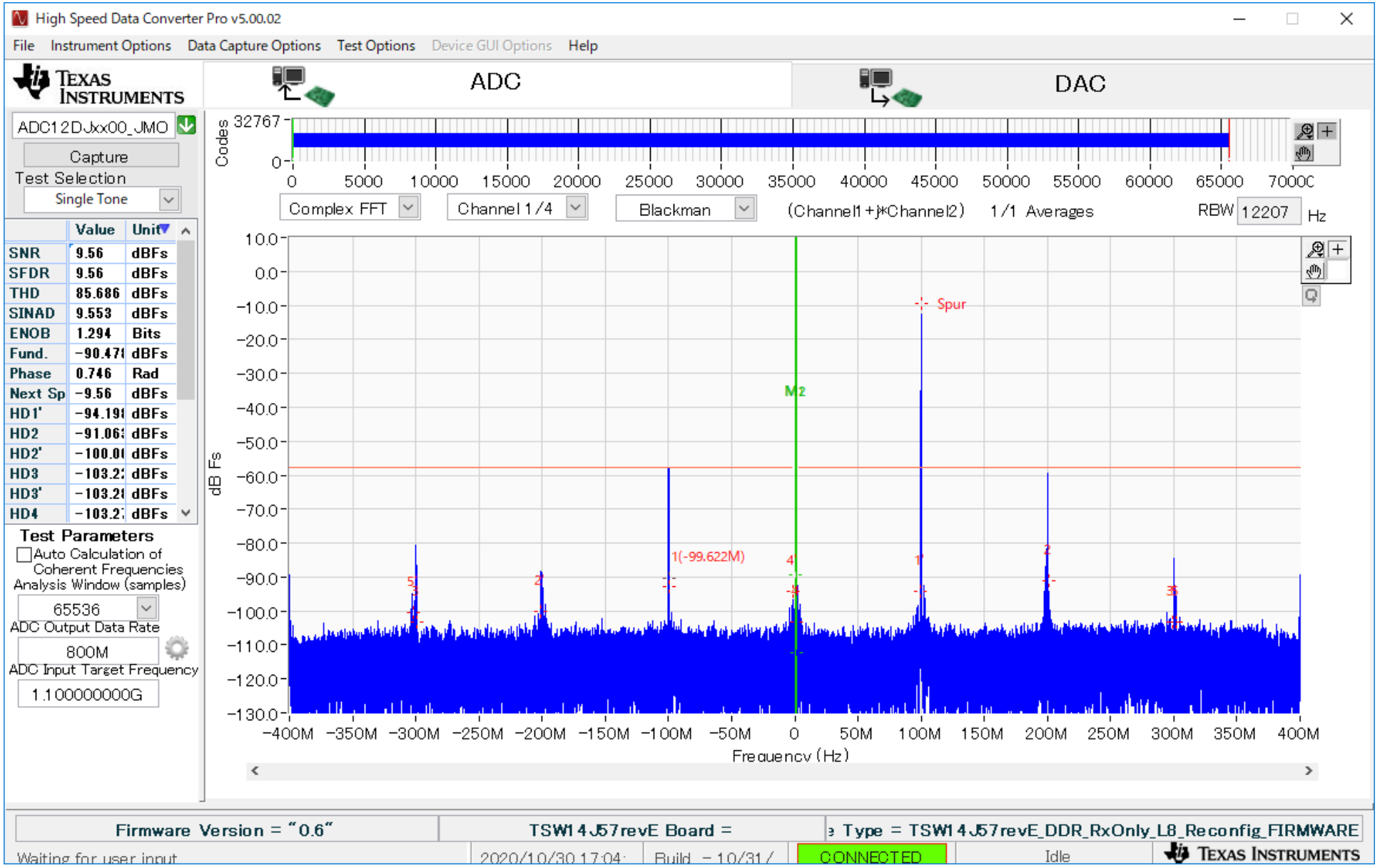
# HSDC_jmode11_fs3200M_fnco1200M_fin1050M

FFT results by MATLAB for IQ data exported from HSDC



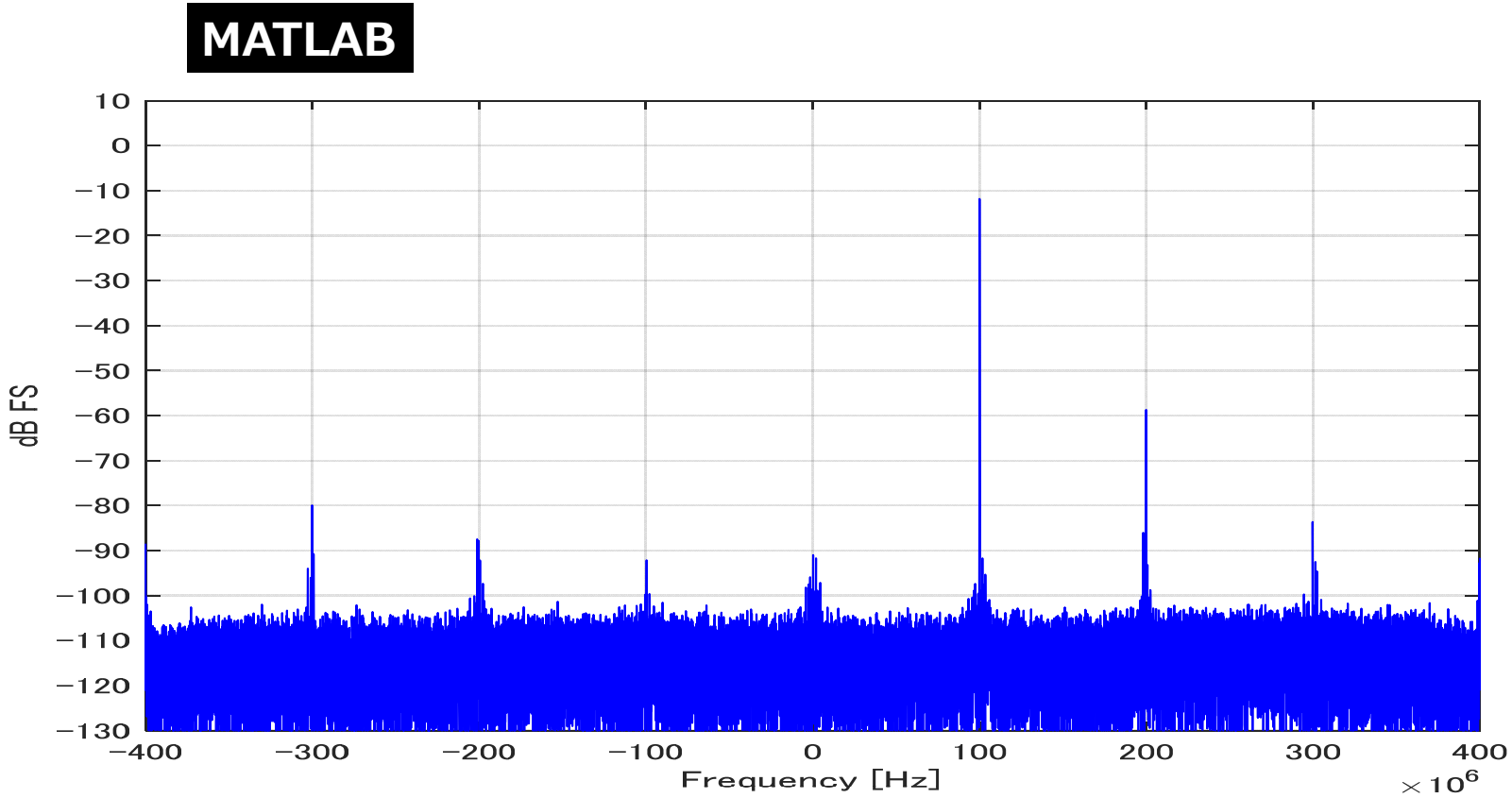

-60dBFS spurious around -150MHz disappears.

# HSDC_jmode11_fs3200M_fnco1200M_fin1100M



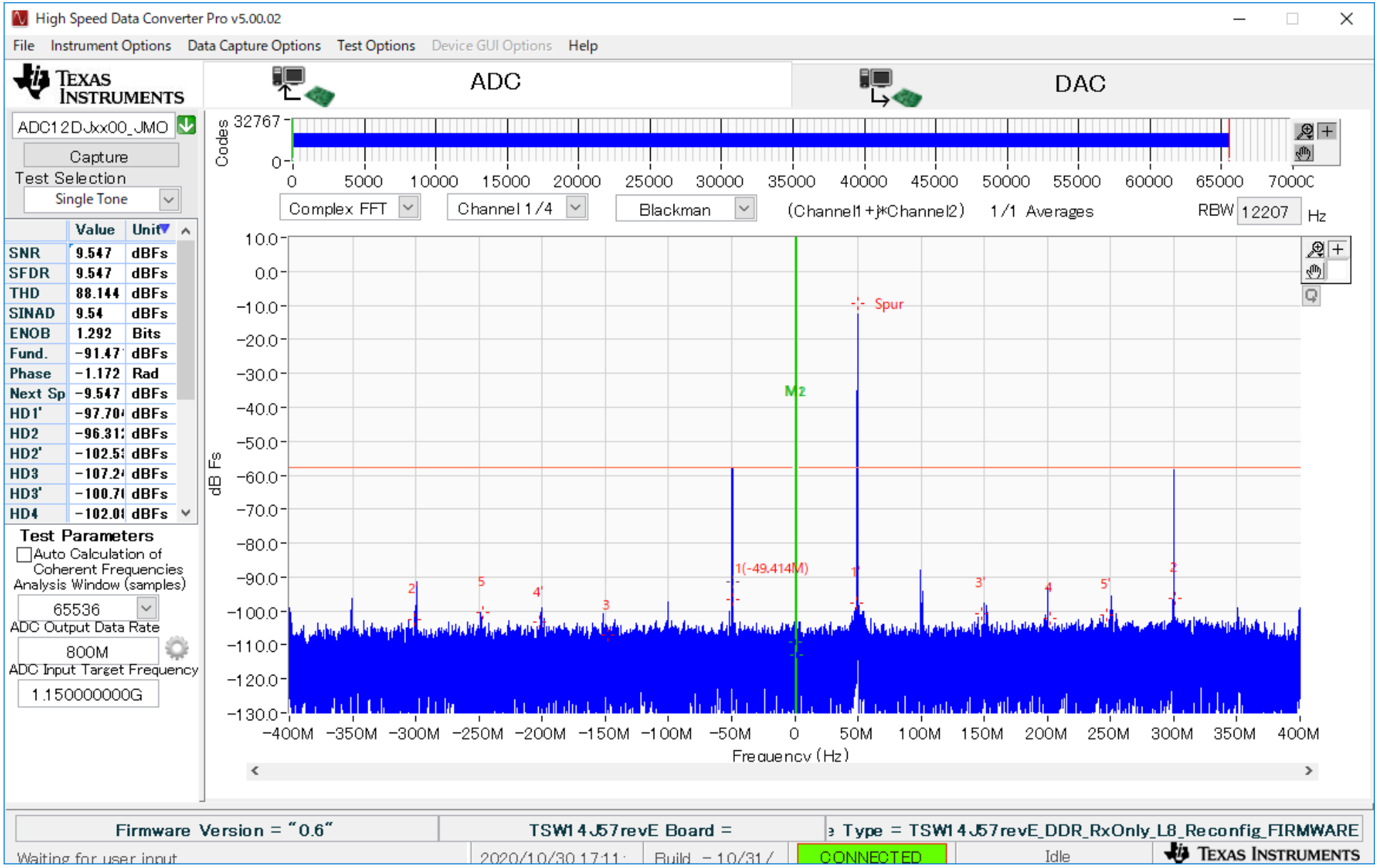
# HSDC_jmode11_fs3200M_fnco1200M_fin1100M

FFT results by MATLAB for IQ data exported from HSDC



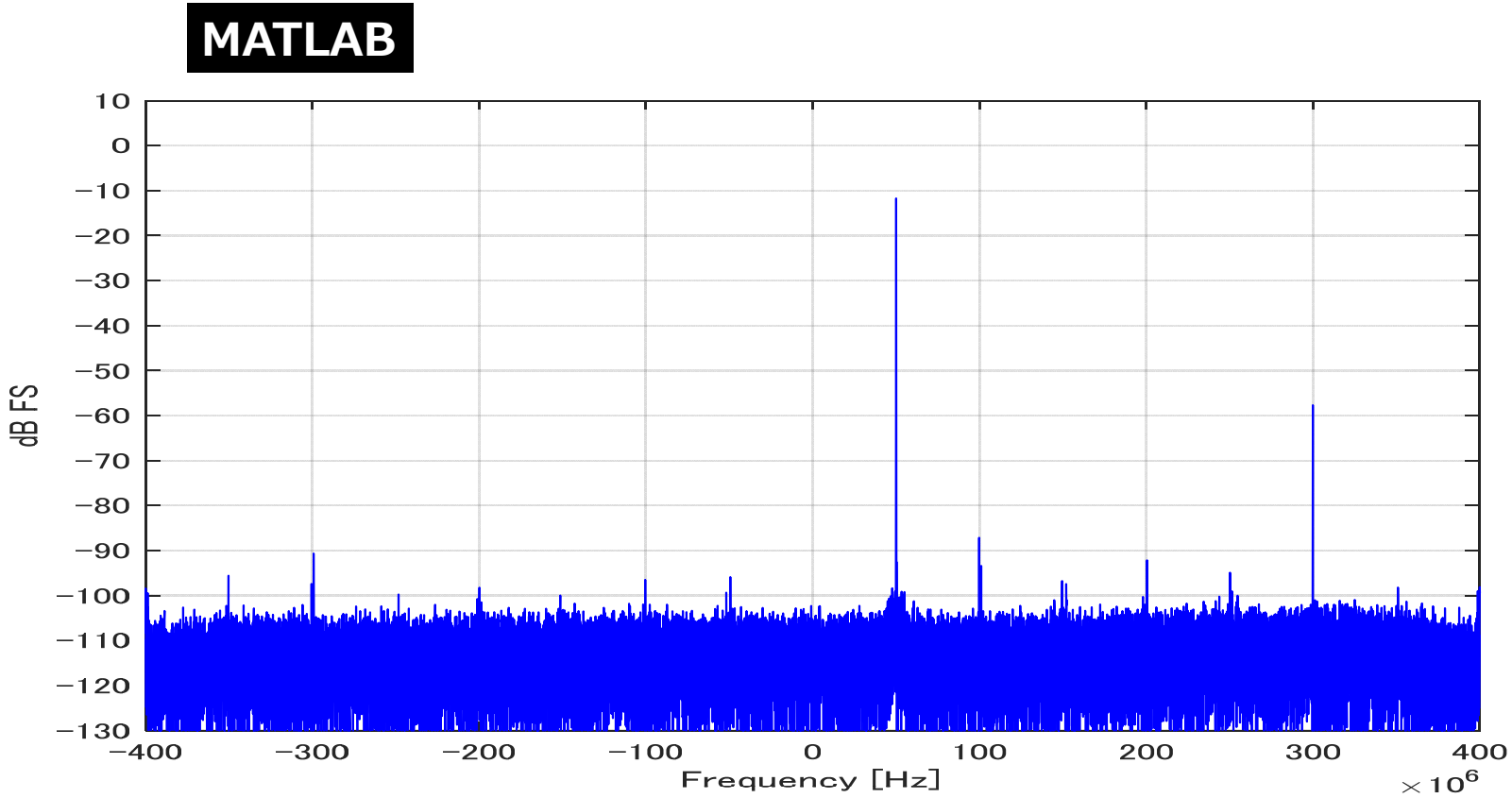

-60dBFS spurious around -100MHz disappears.

# HSDC_jmode11_fs3200M_fnco1200M_fin1150M



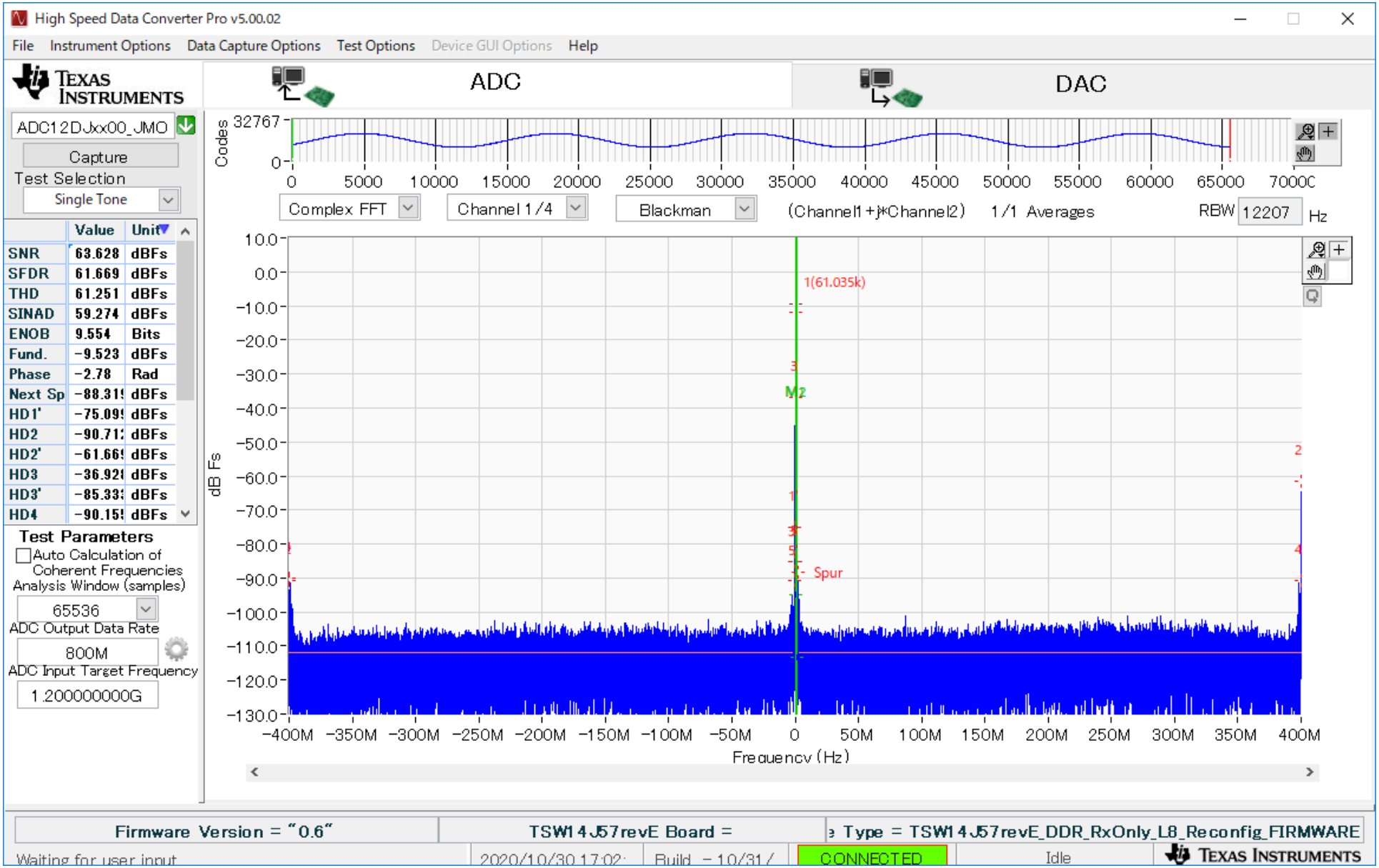
# HSDC_jmode11_fs3200M_fnco1200M_fin1150M

FFT results by MATLAB for IQ data exported from HSDC



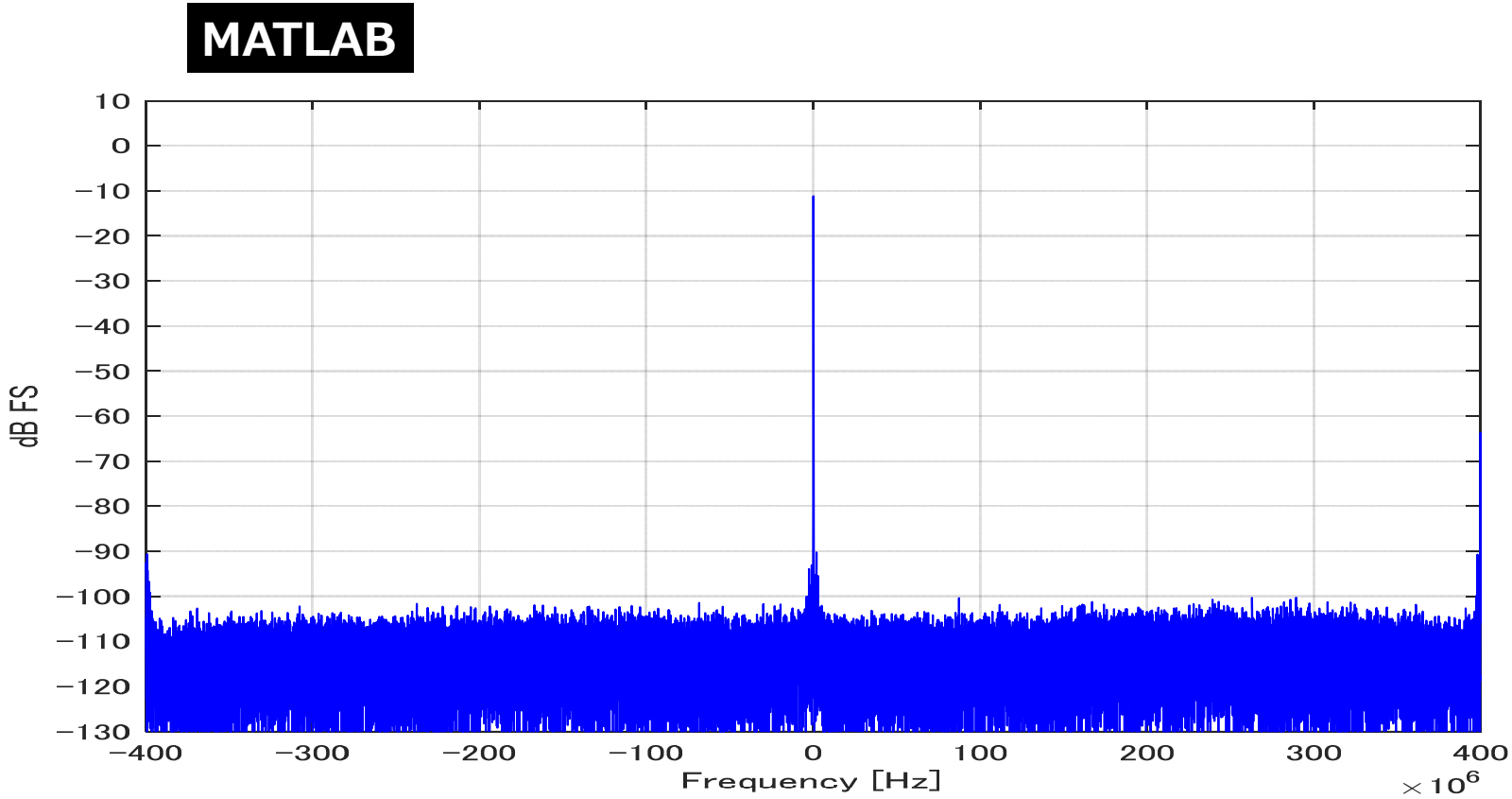

-60dBFS spurious around -50MHz disappears.

# HSDC_jmode11_fs3200M_fnco1200M_fin1200M



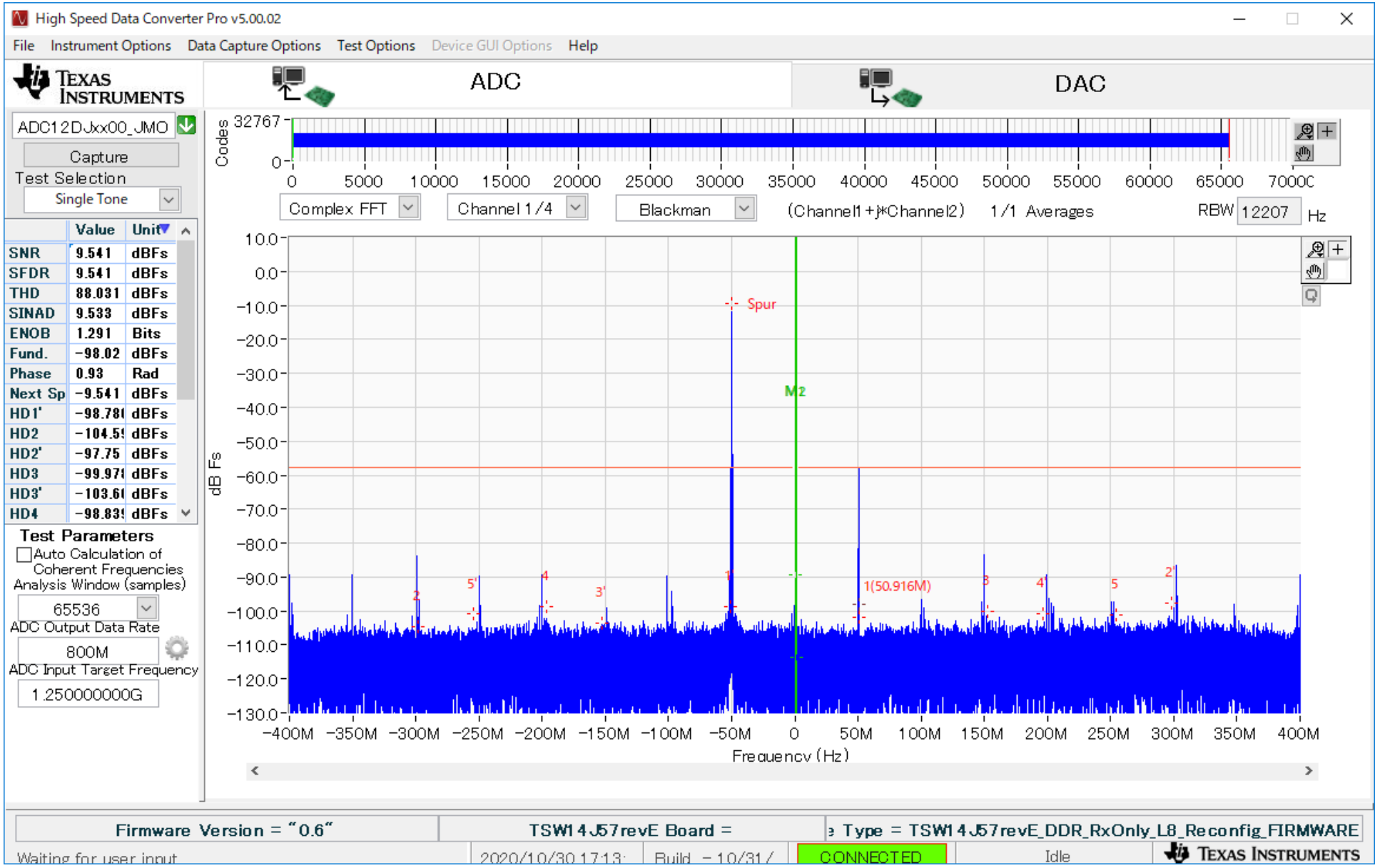
# HSDC_jmode11_fs3200M_fnco1200M_fin1200M

FFT results by MATLAB for IQ data exported from HSDC



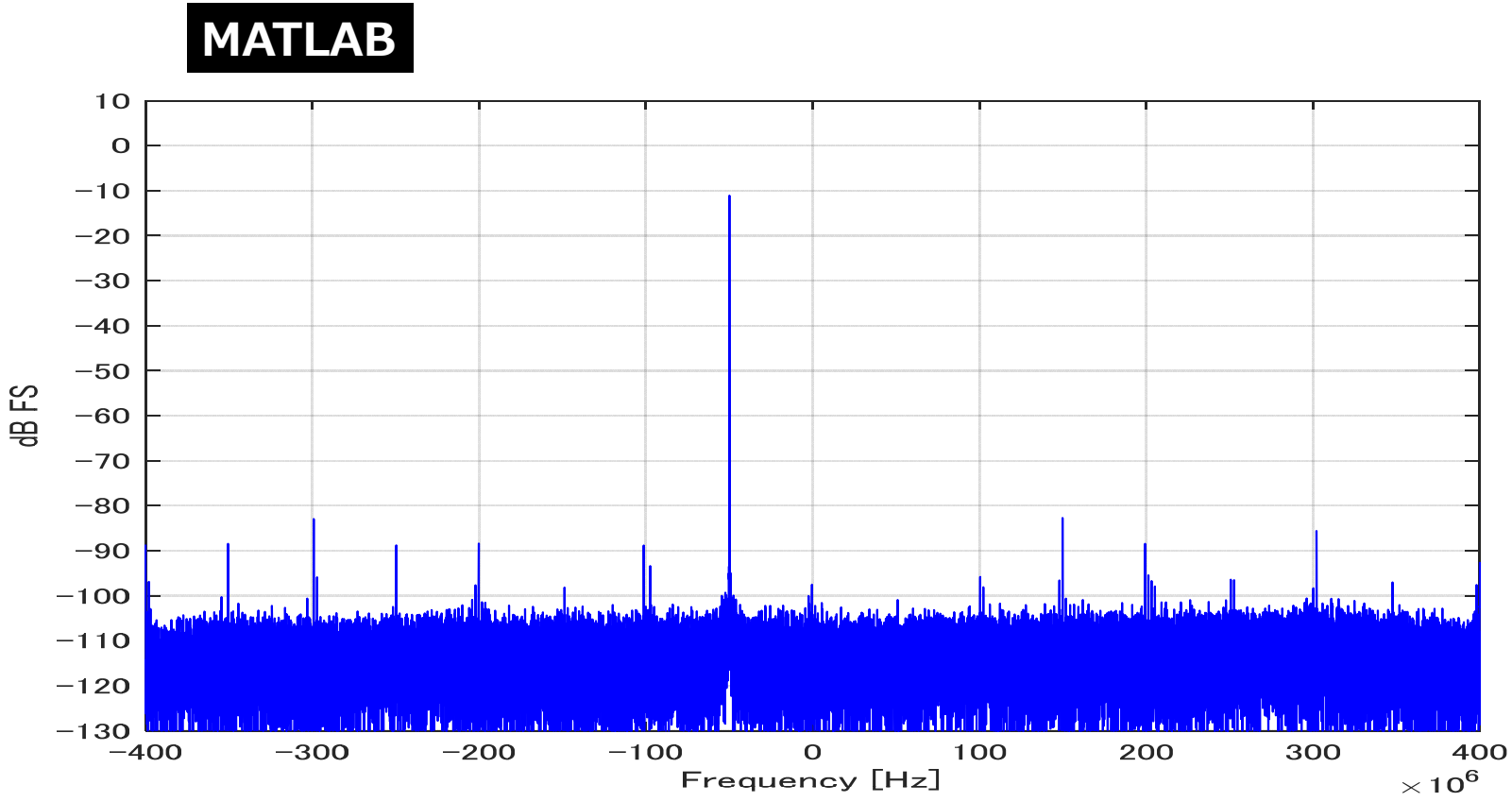

The results are very similar.

# HSDC_jmode11_fs3200M_fnco1200M_fin1250M



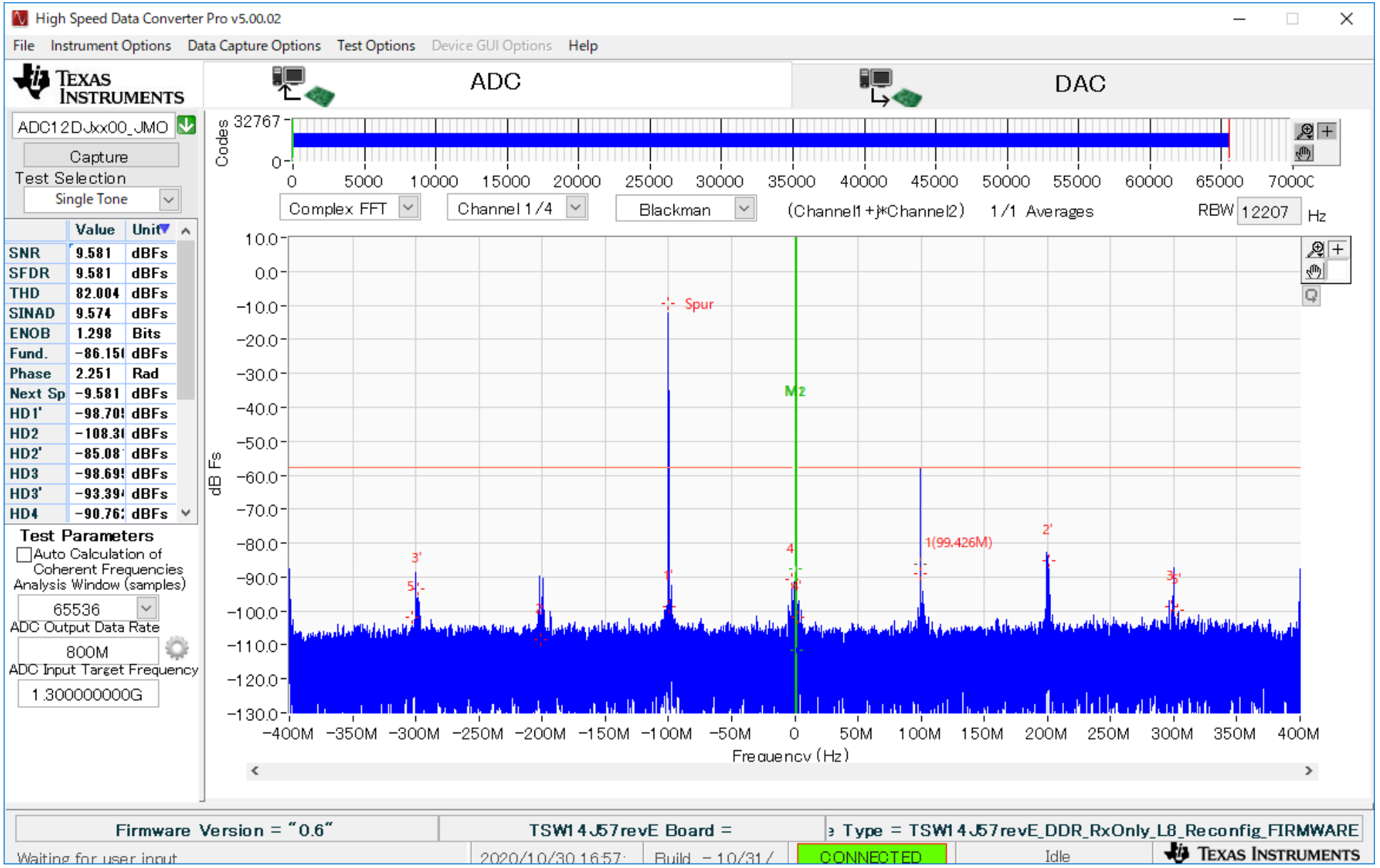
# HSDC_jmode11_fs3200M_fnco1200M_fin1250M

FFT results by MATLAB for IQ data exported from HSDC



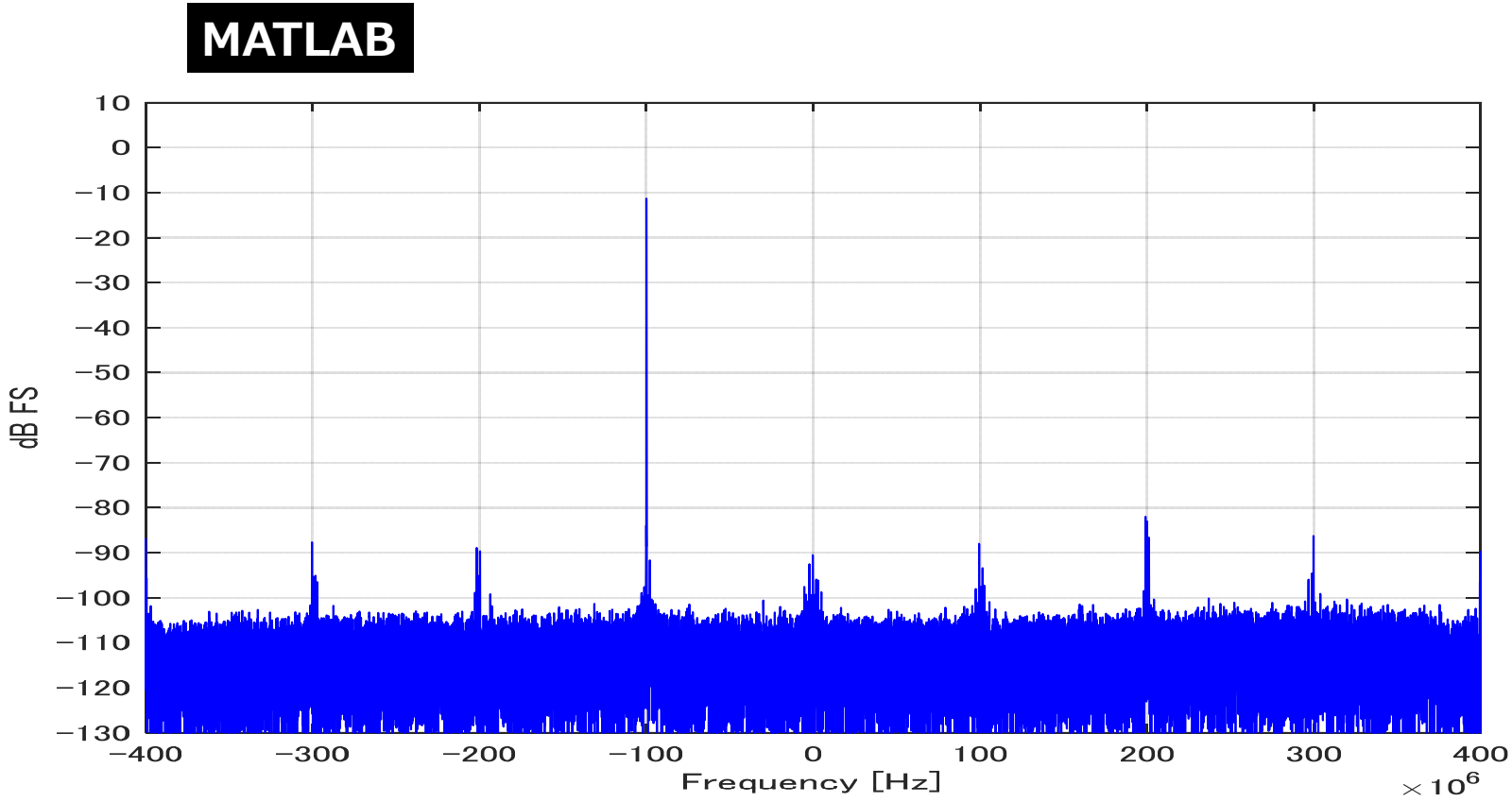

-60dBFS spurious around +50MHz disappears.

# HSDC_jmode11_fs3200M_fnco1200M_fin1300M



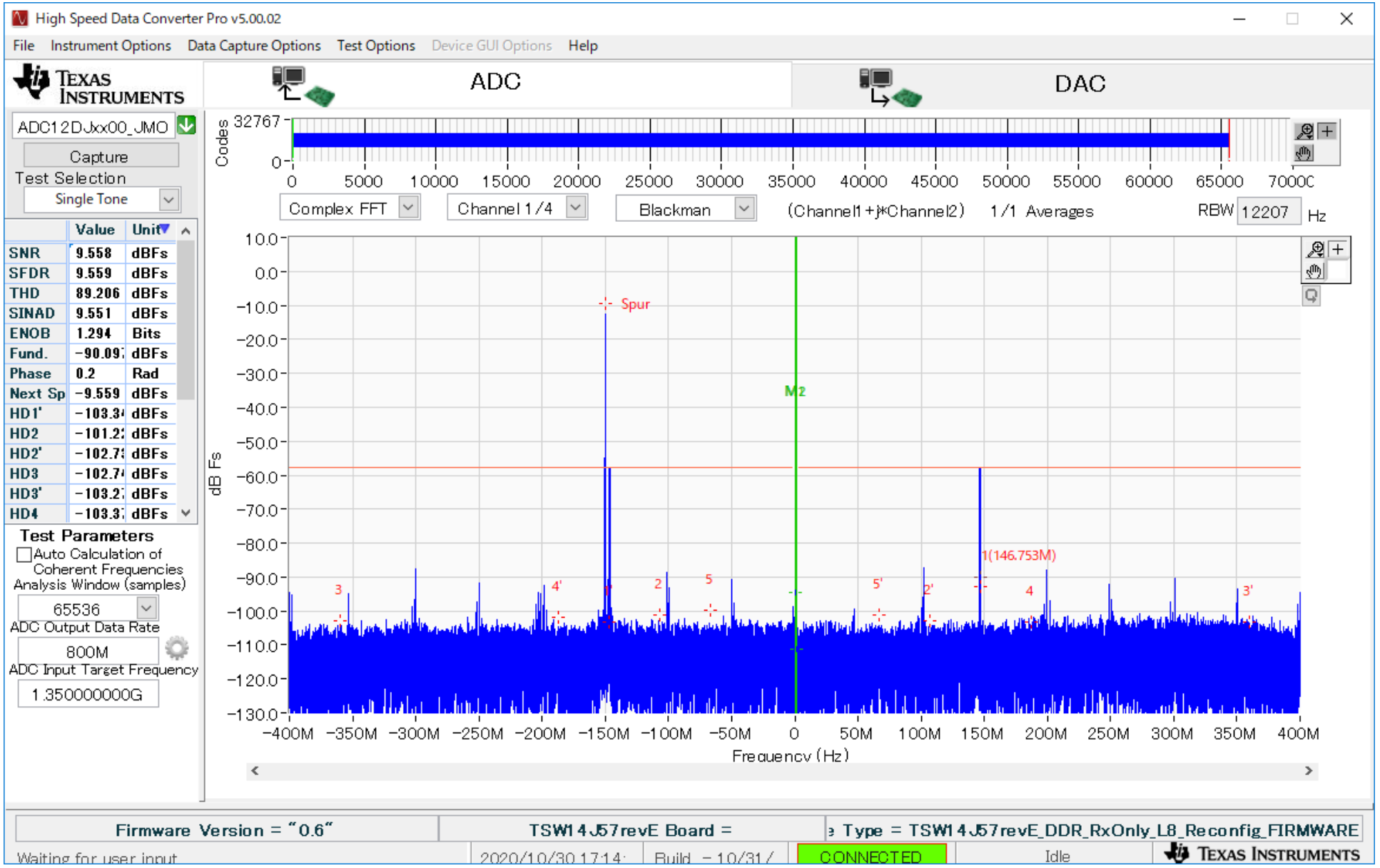
# HSDC_jmode11_fs3200M_fnco1200M_fin1300M

FFT results by MATLAB for IQ data exported from HSDC



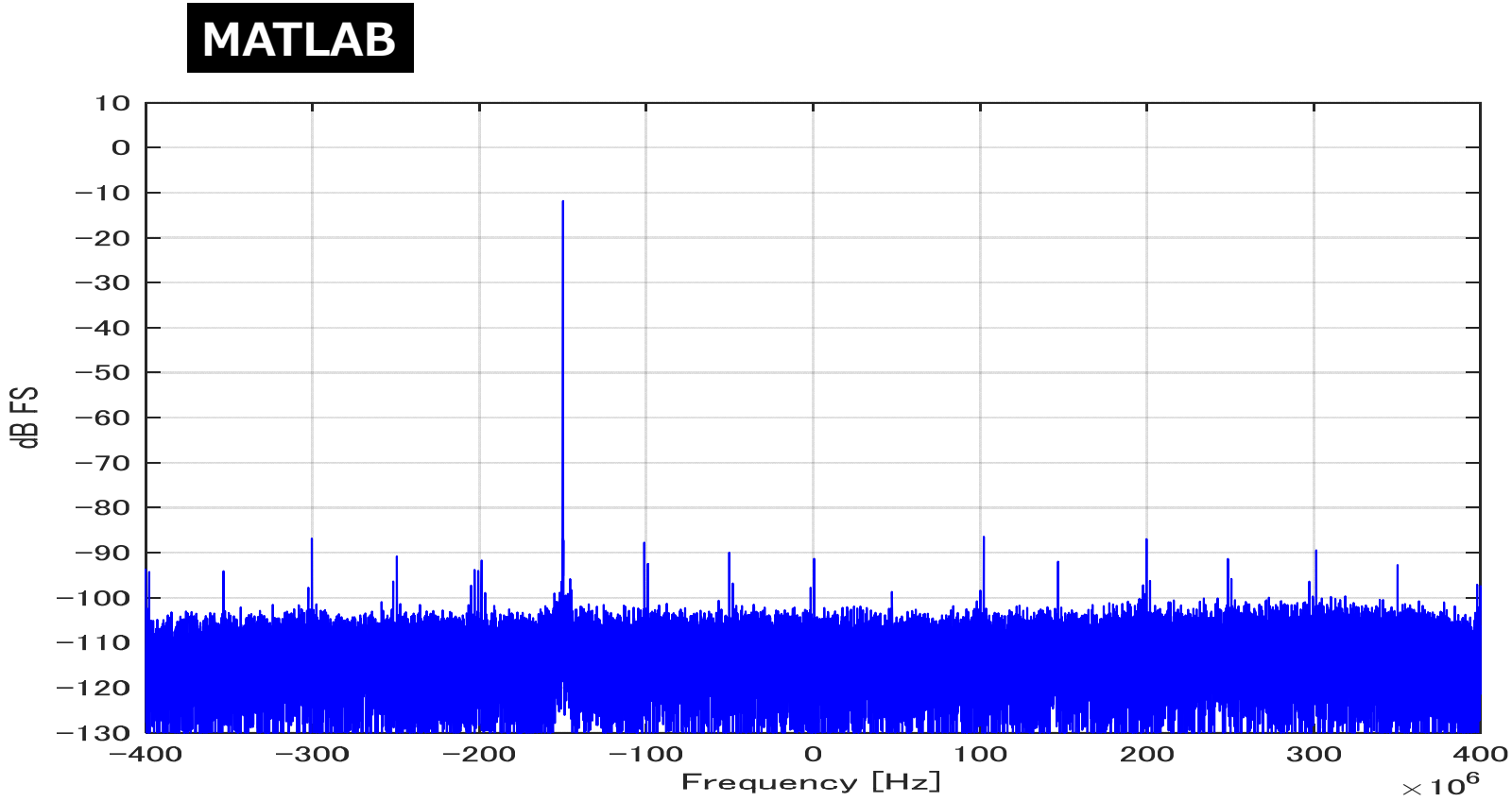

-60dBFS spurious around +100MHz disappears.

# HSDC_jmode11_fs3200M_fnco1200M_fin1350M



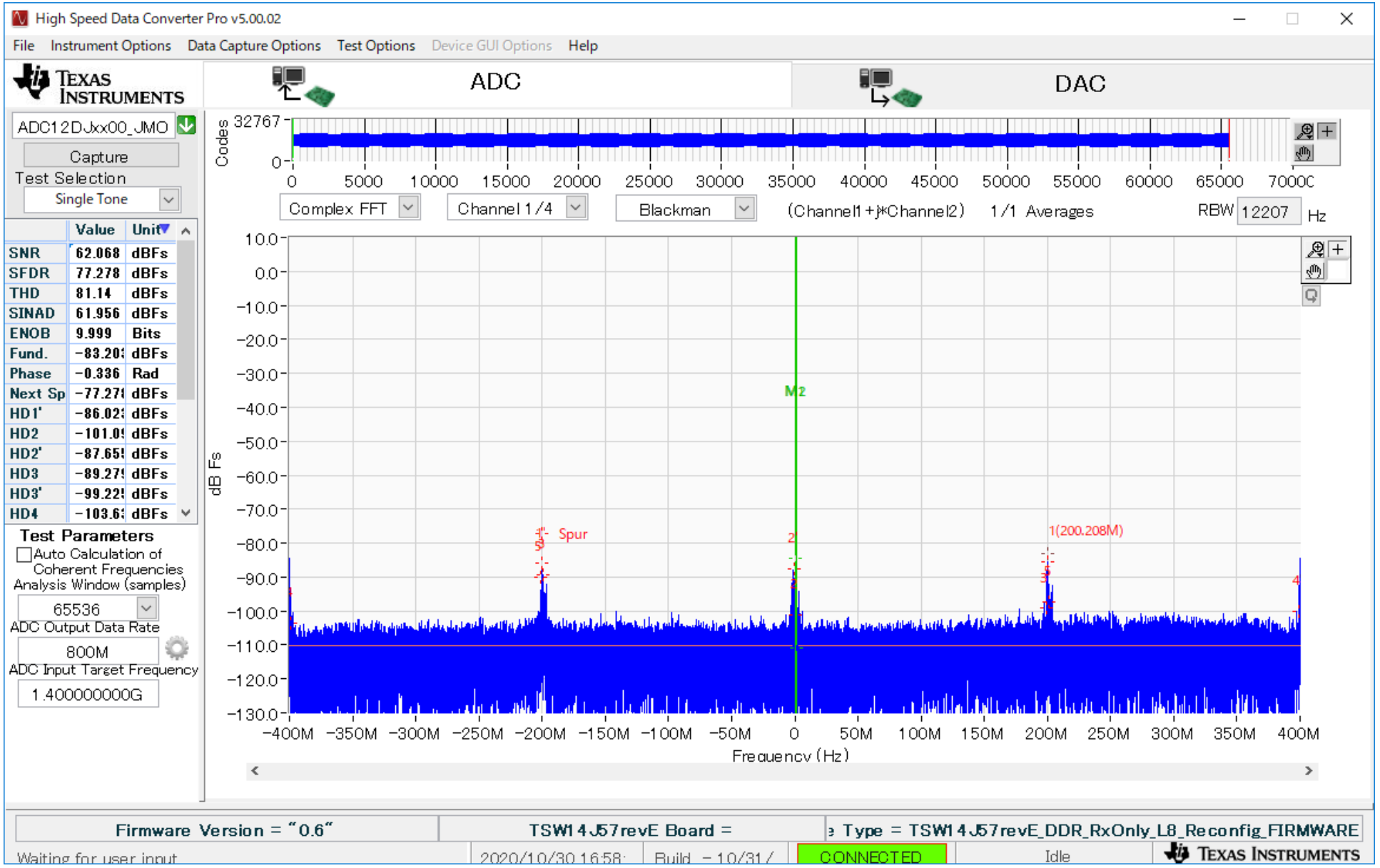
# HSDC_jmode11_fs3200M_fnco1200M_fin1350M

FFT results by MATLAB for IQ data exported from HSDC



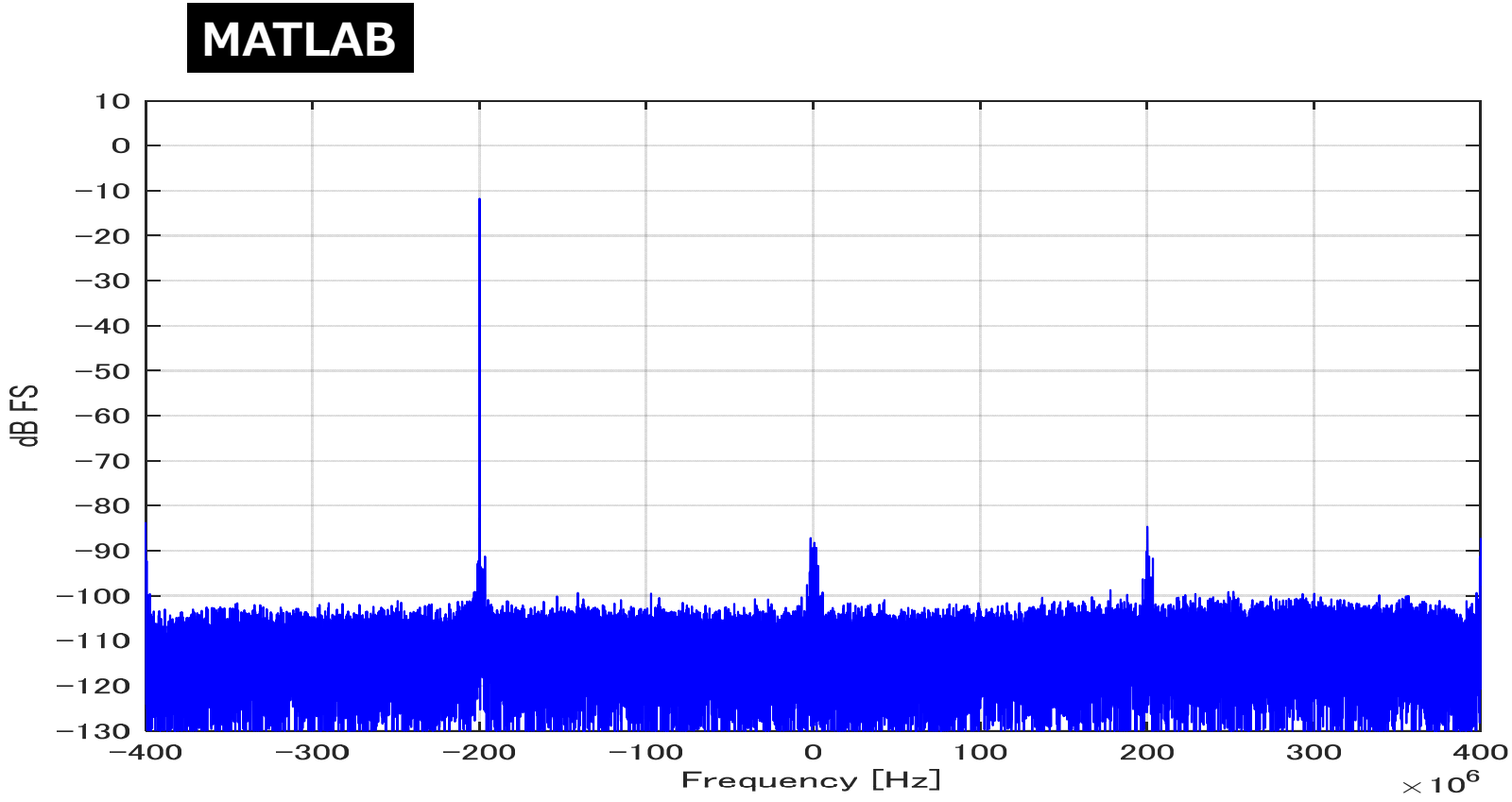

-60dBFS spurious around +150MHz disappears.

# HSDC_jmode11_fs3200M_fnco1200M_fin1400M



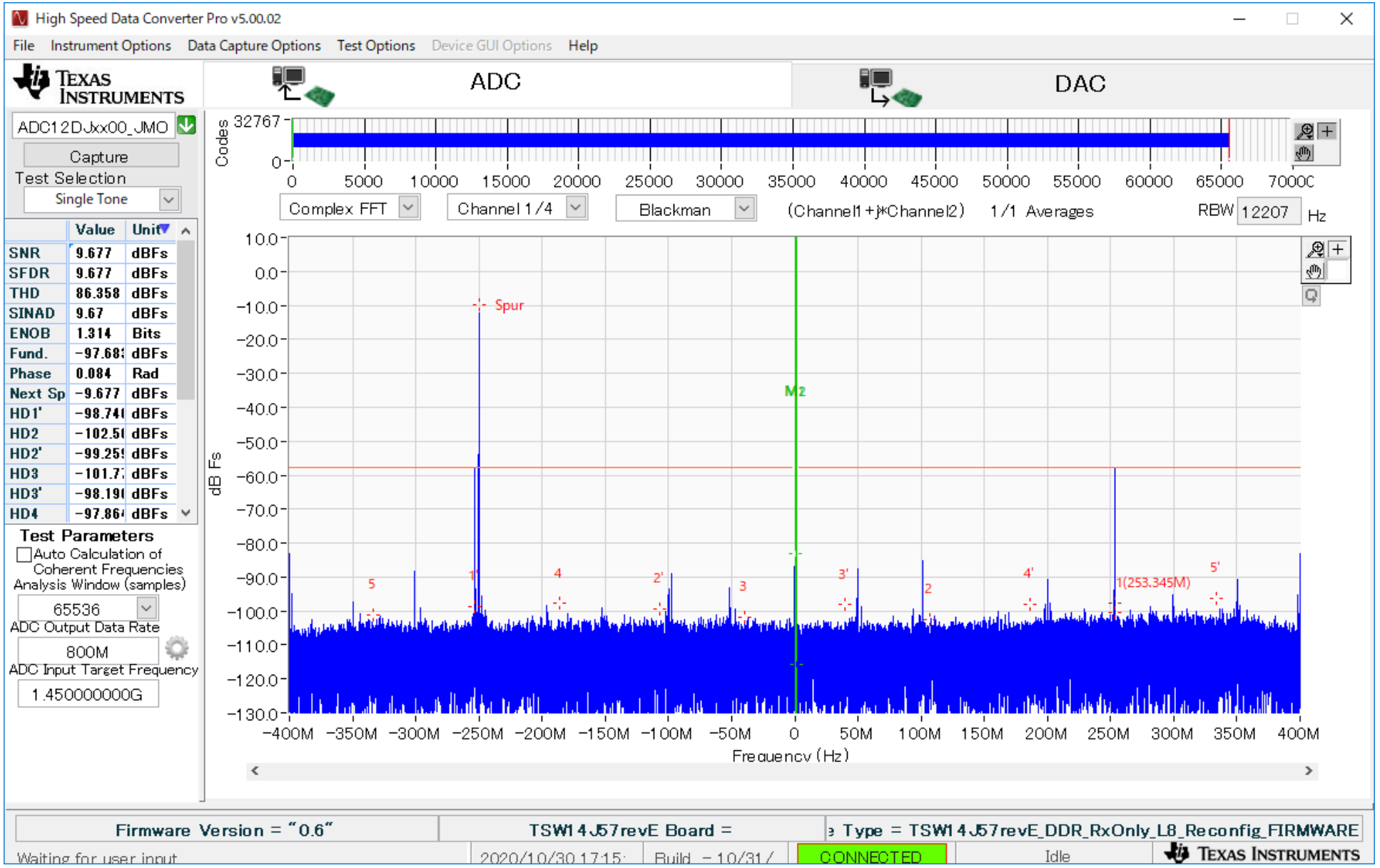
# HSDC_jmode11_fs3200M_fnco1200M_fin1400M

FFT results by MATLAB for IQ data exported from HSDC



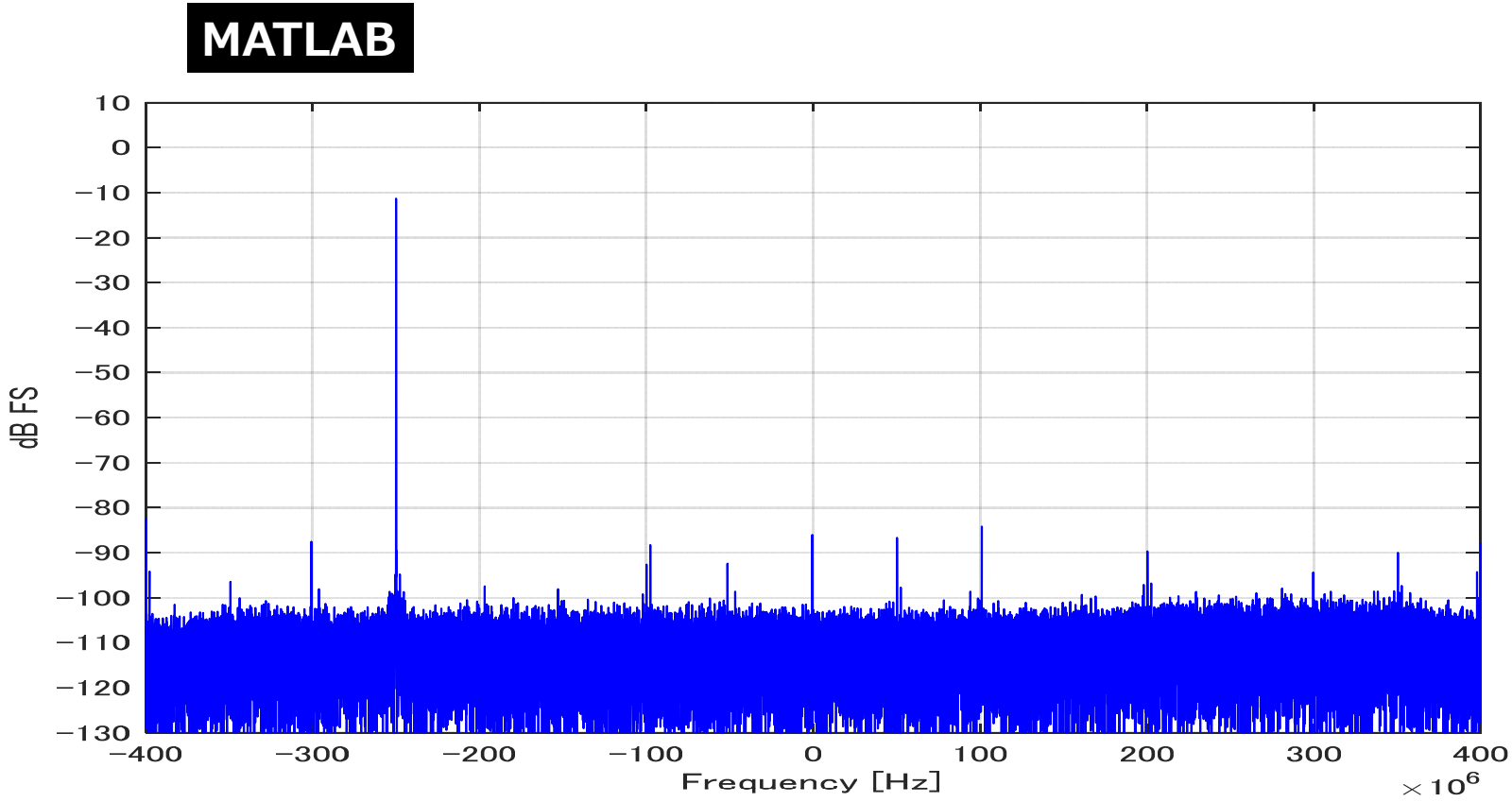

-10dBFS spectrum exists near -200MHz.

# HSDC_jmode11_fs3200M_fnco1200M_fin1450M



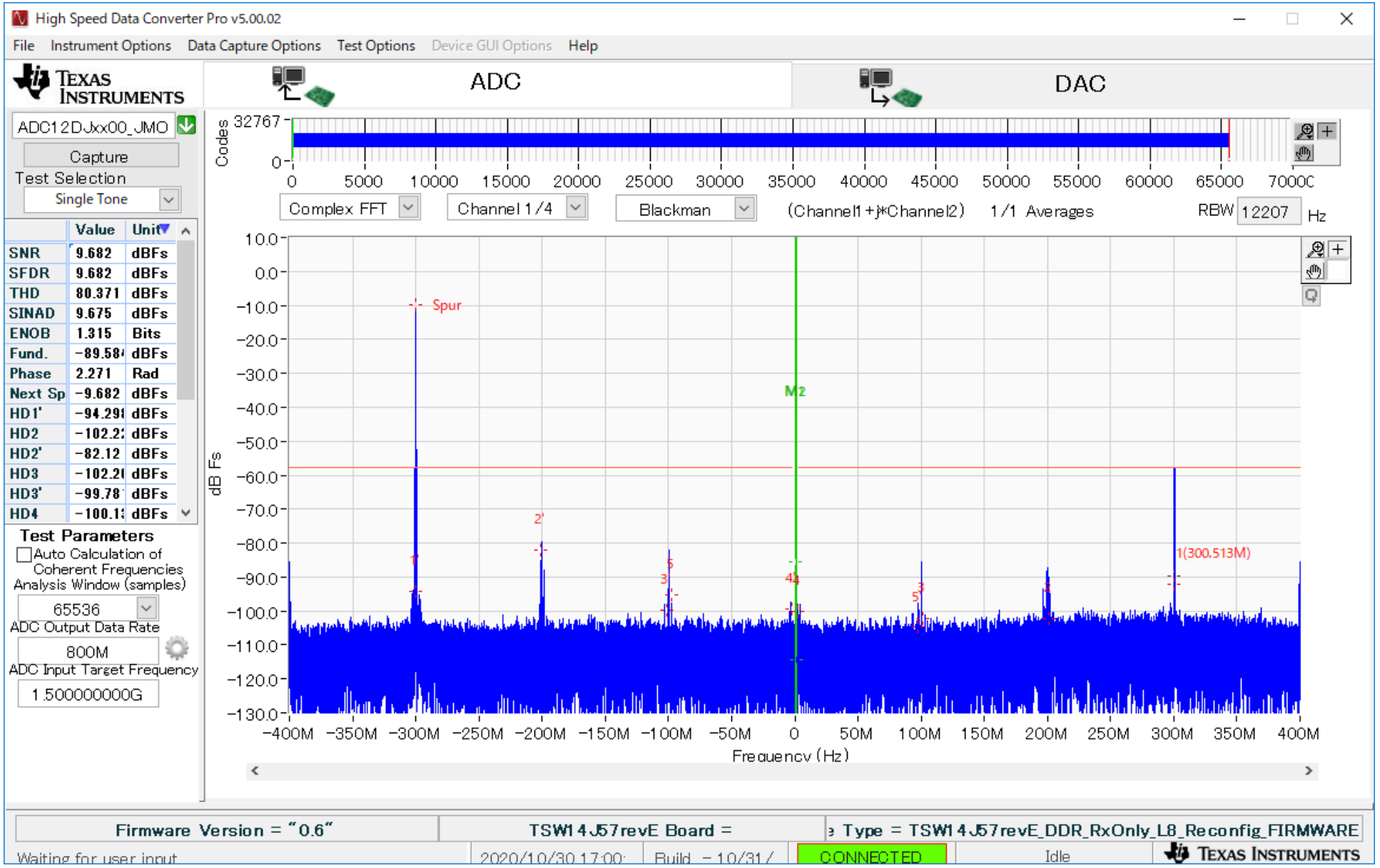
# HSDC_jmode11_fs3200M_fnco1200M_fin1450M

FFT results by MATLAB for IQ data exported from HSDC



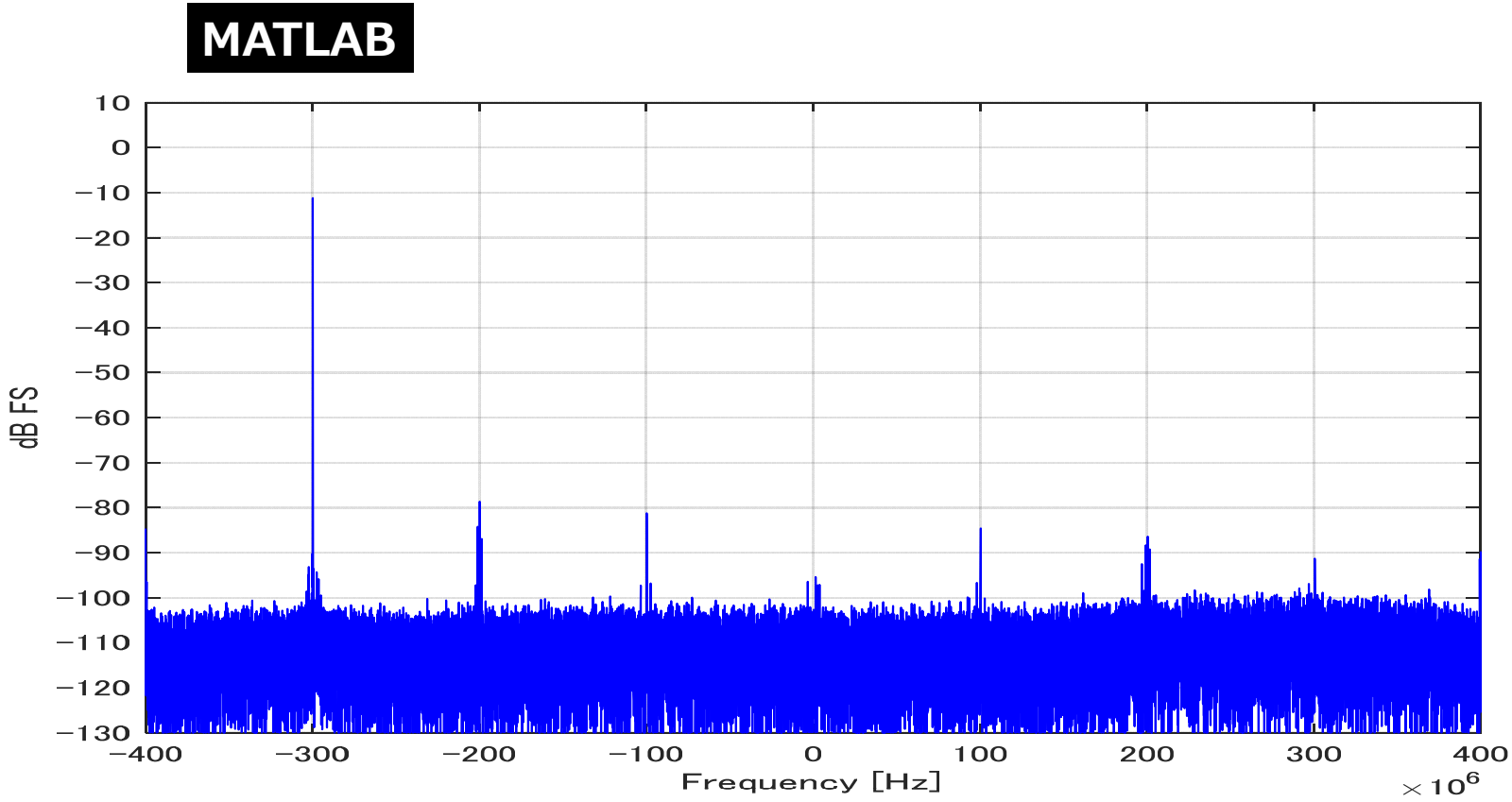

-60dBFS spurious around +250MHz disappears.

# HSDC_jmode11_fs3200M_fnco1200M_fin1500M



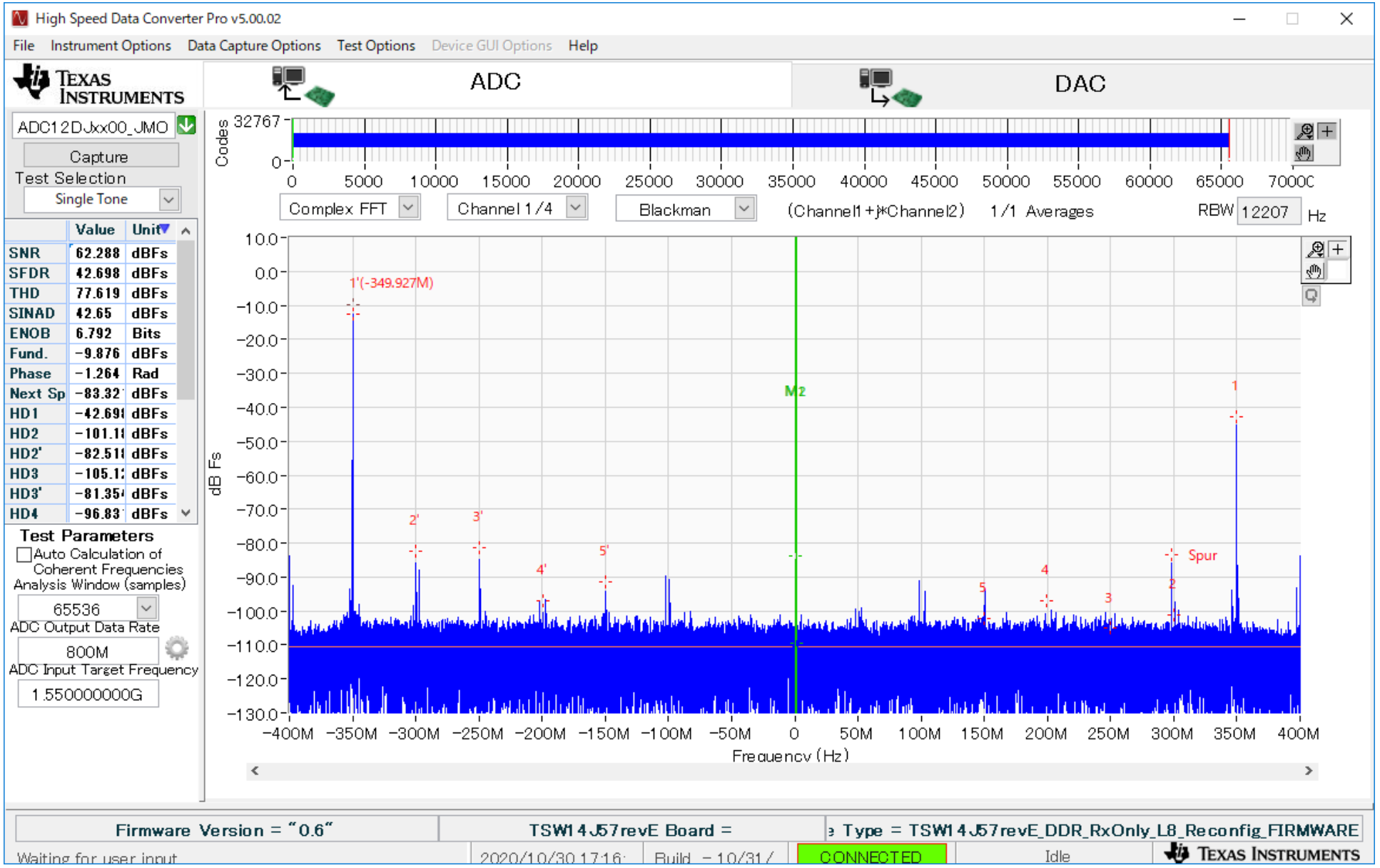
# HSDC_jmode11_fs3200M_fnco1200M_fin1500M

FFT results by MATLAB for IQ data exported from HSDC



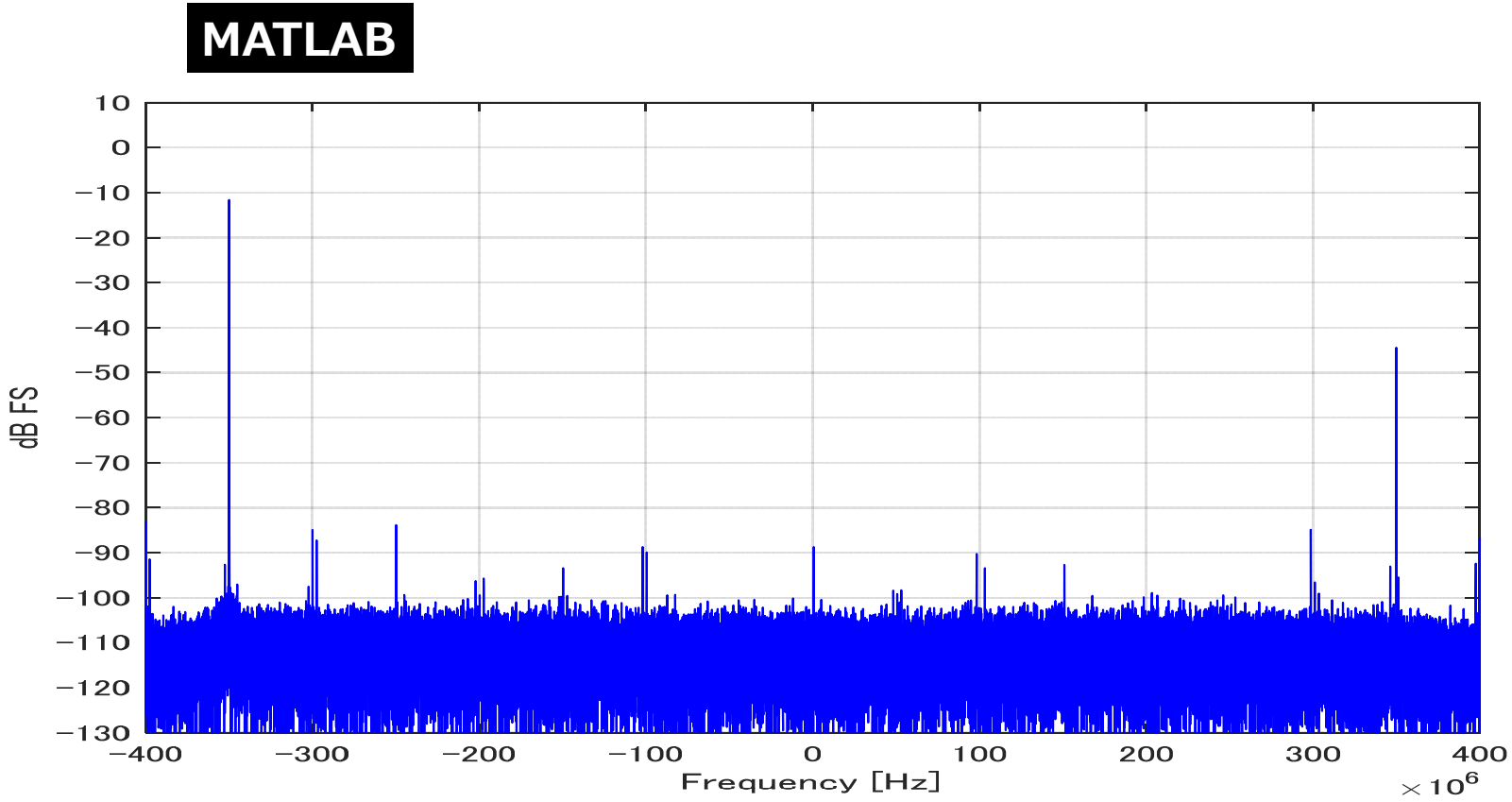

-60dBFS spurious around +300MHz disappears.

# HSDC_jmode11_fs3200M_fnco1200M_fin1550M



# HSDC_jmode11_fs3200M_fnco1200M_fin1550M

FFT results by MATLAB for IQ data exported from HSDC

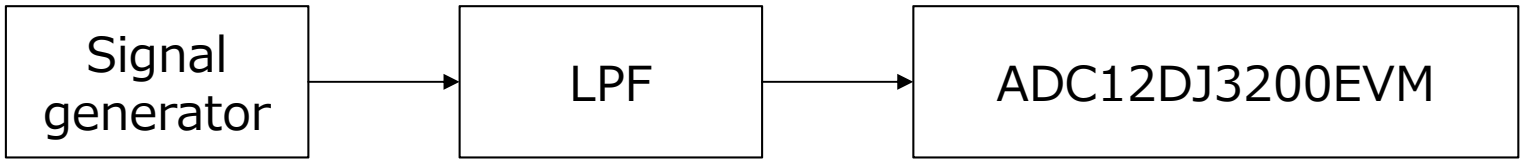



The results are very similar, but the marker index (primes) are reversed.

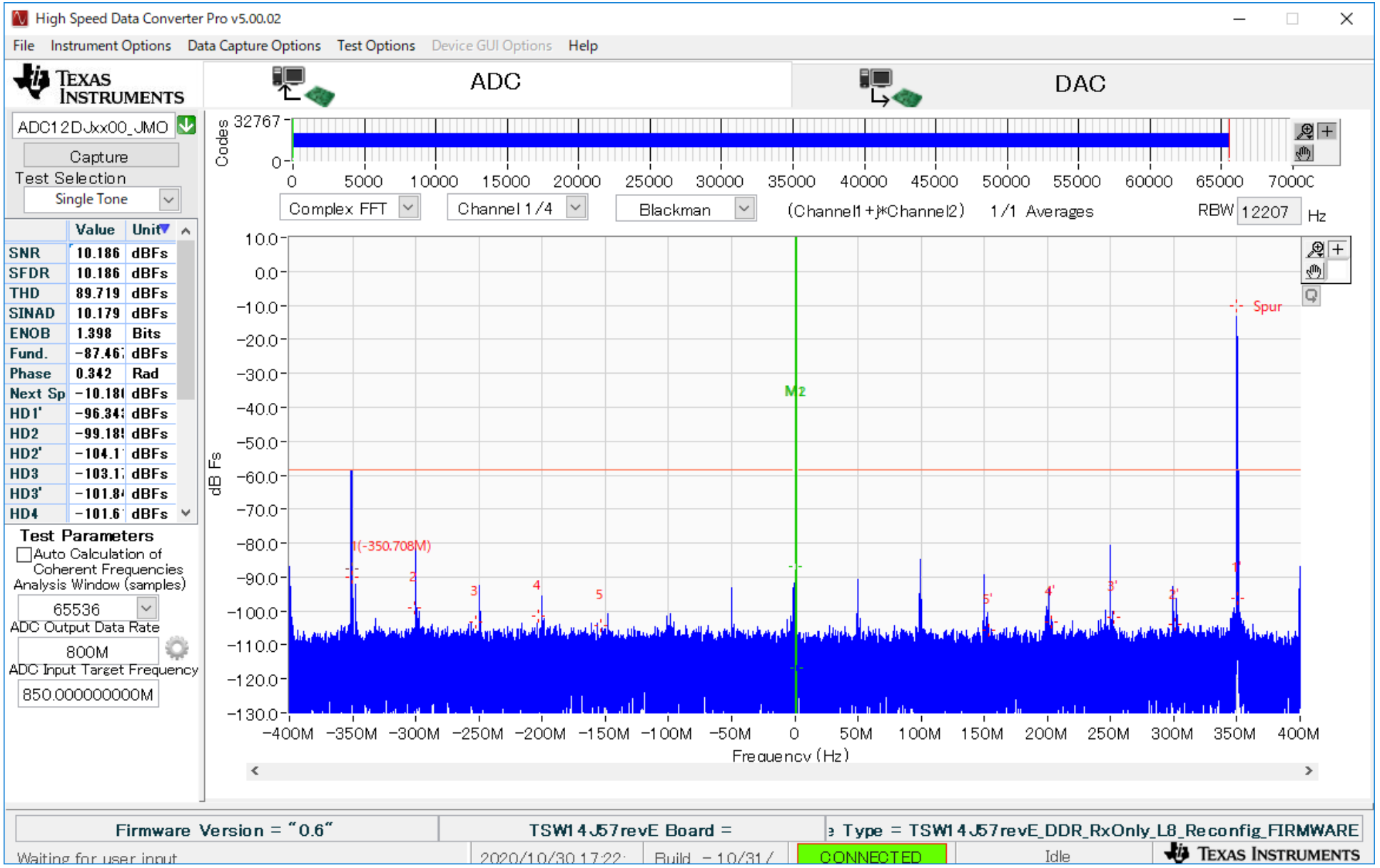
# 5

JMODE=11, Fs=3200MSPS,
NCO=1200MHz, Fin=850 to 1550MHz,
LPF was used, (1st Nyquist Zone)
IQ seemed to be swapping. The largest spectrum of the HSDC complex FFT was marked with the 1' marker. Sometimes the FFT results are different between HSDC and MATLAB.

# Evaluation with the harmonics < -70 dBc

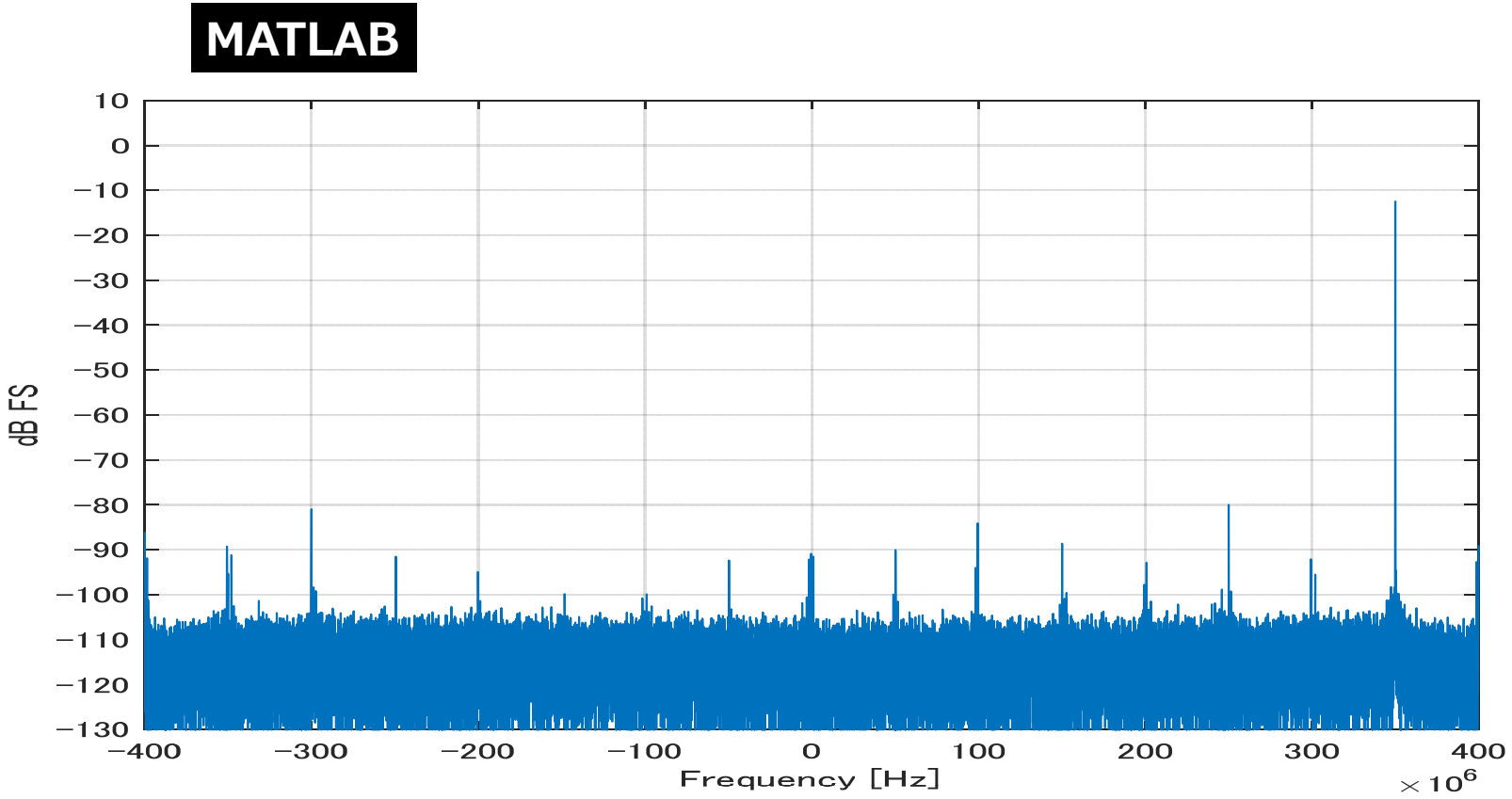


# HSDC_jmode11_fs3200M_fnco1200M_fin850M_LPF



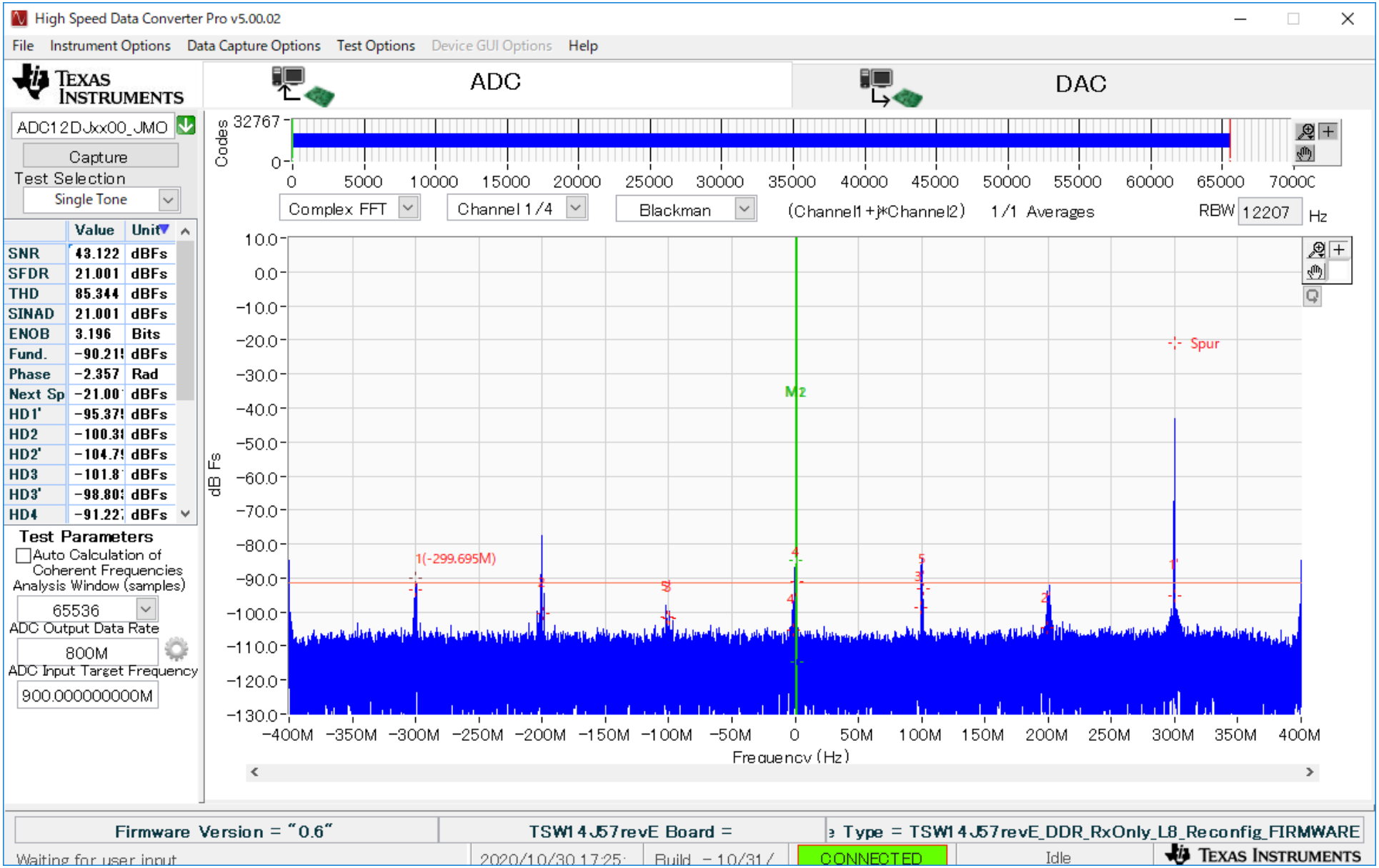
# HSDC_jmode11_fs3200M_fnco1200M_fin850M_LPF

FFT results by MATLAB for IQ data exported from HSDC



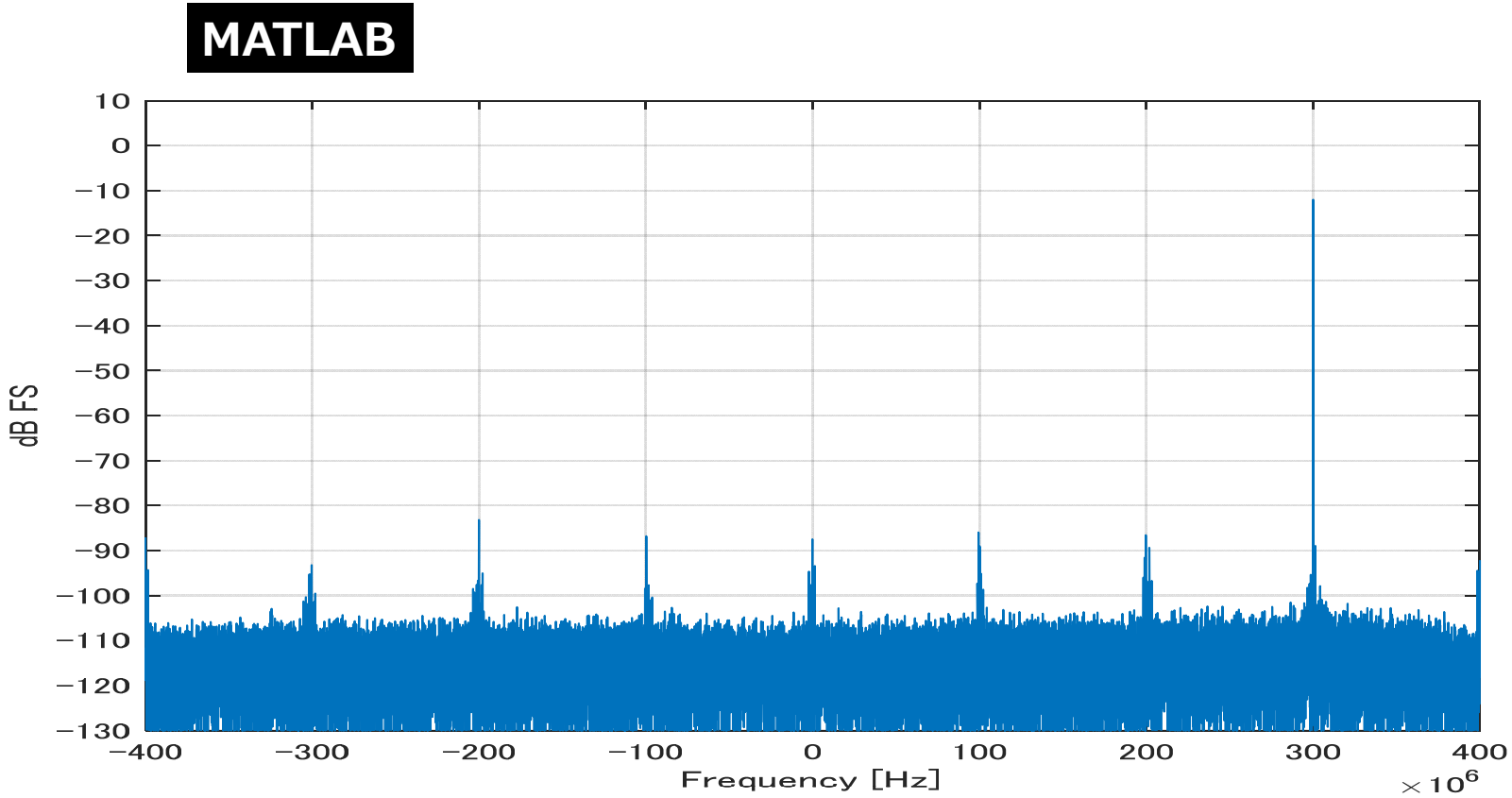

-60dBFS spurious around -350MHz disappears.

# HSDC_jmode11_fs3200M_fnco1200M_fin900M_LPF



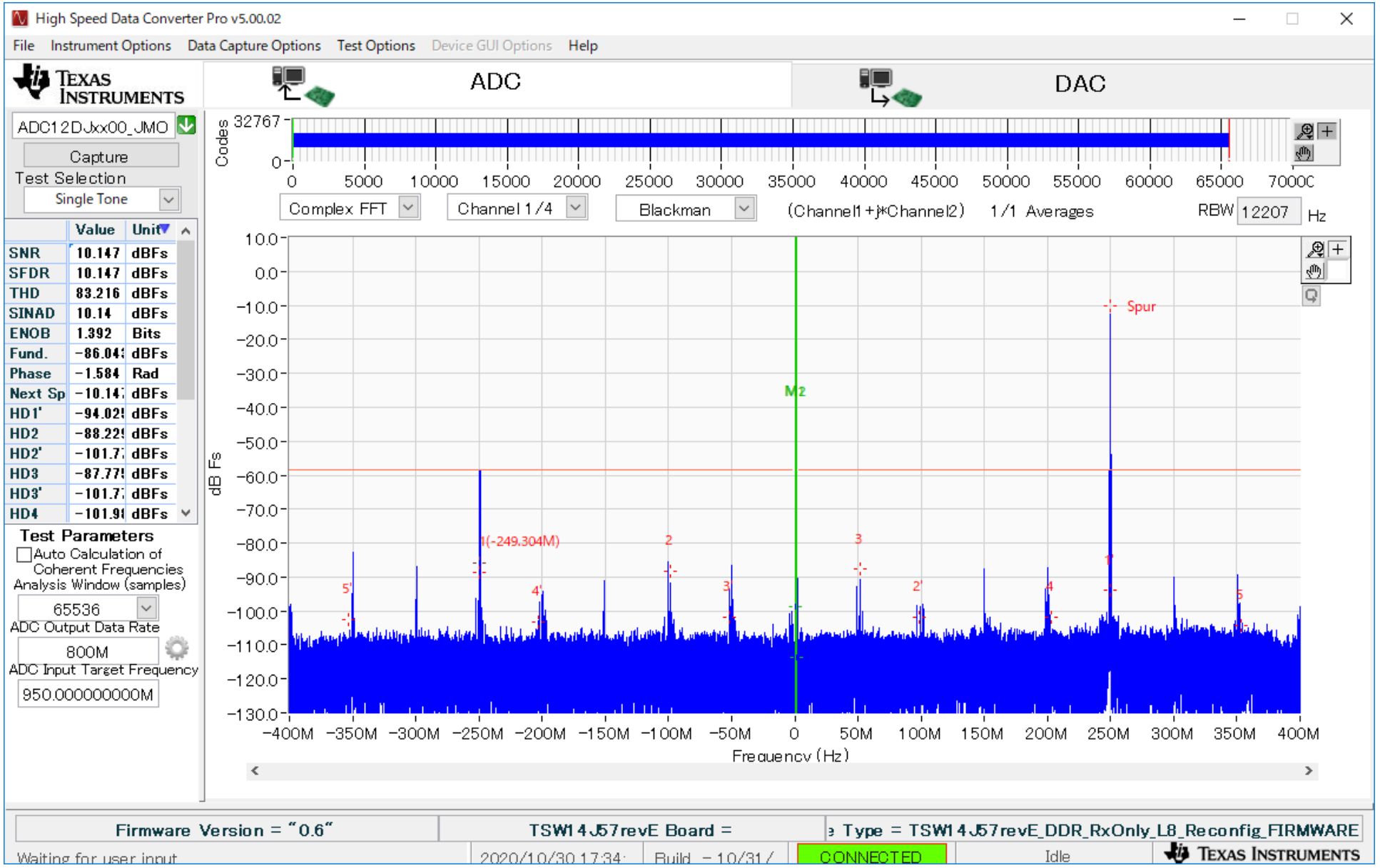
# HSDC_jmode11_fs3200M_fnco1200M_fin900M_LPF

FFT results by MATLAB for IQ data exported from HSDC



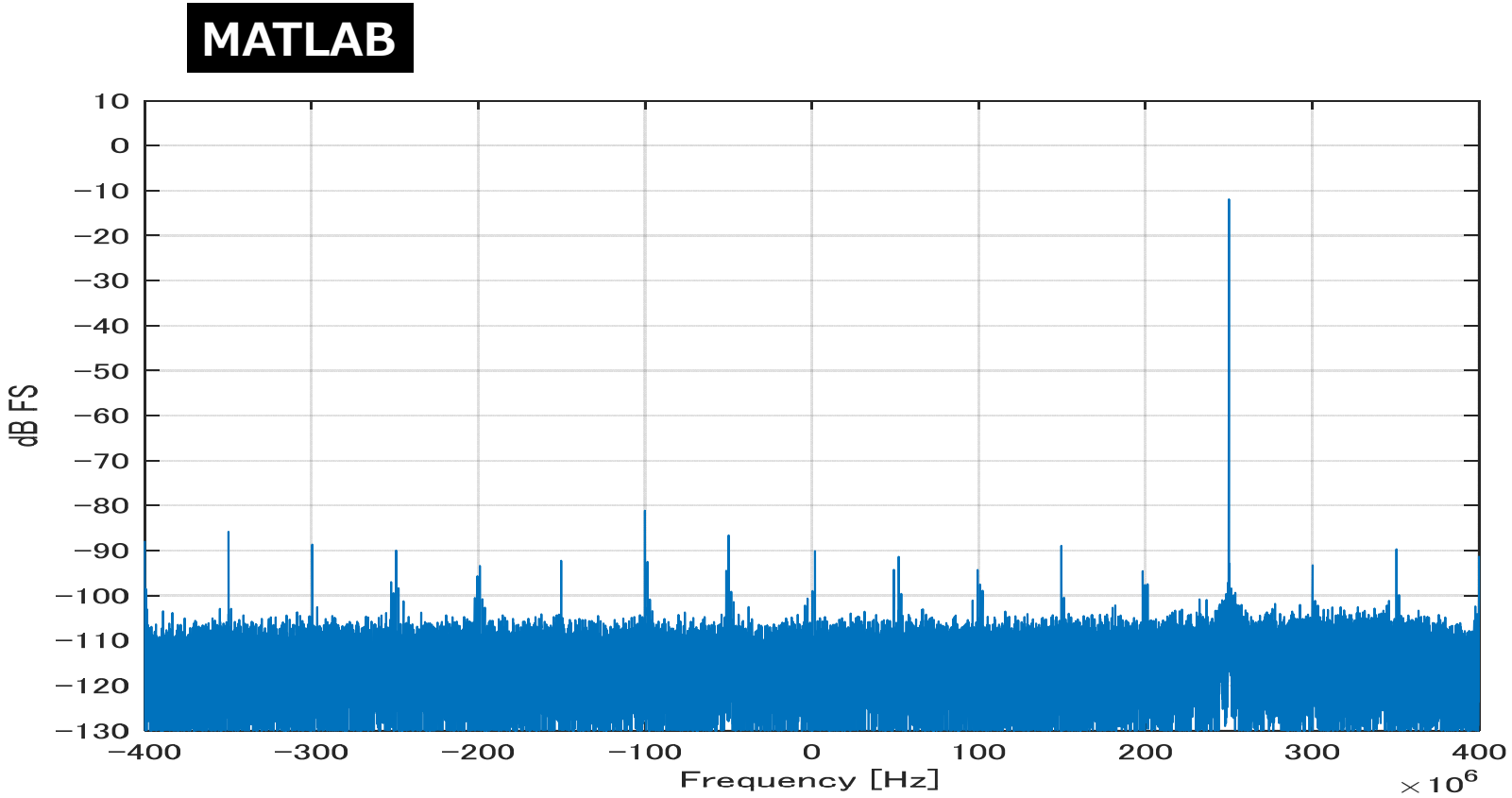

-20dBFS spectrum exists near 300MHz.

# HSDC_jmode11_fs3200M_fnco1200M_fin950M_LPF



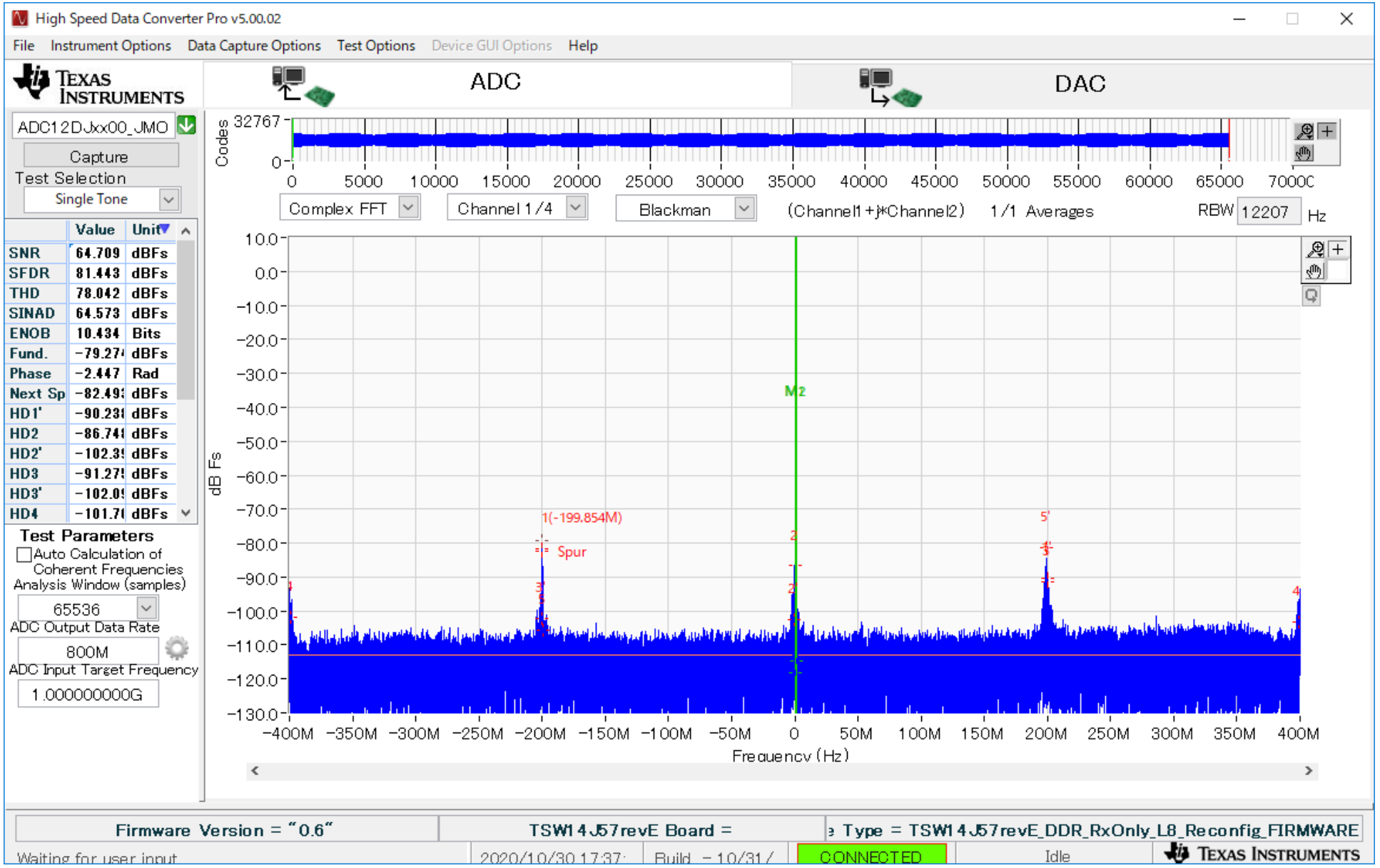
# HSDC_jmode11_fs3200M_fnco1200M_fin950M_LPF

FFT results by MATLAB for IQ data exported from HSDC



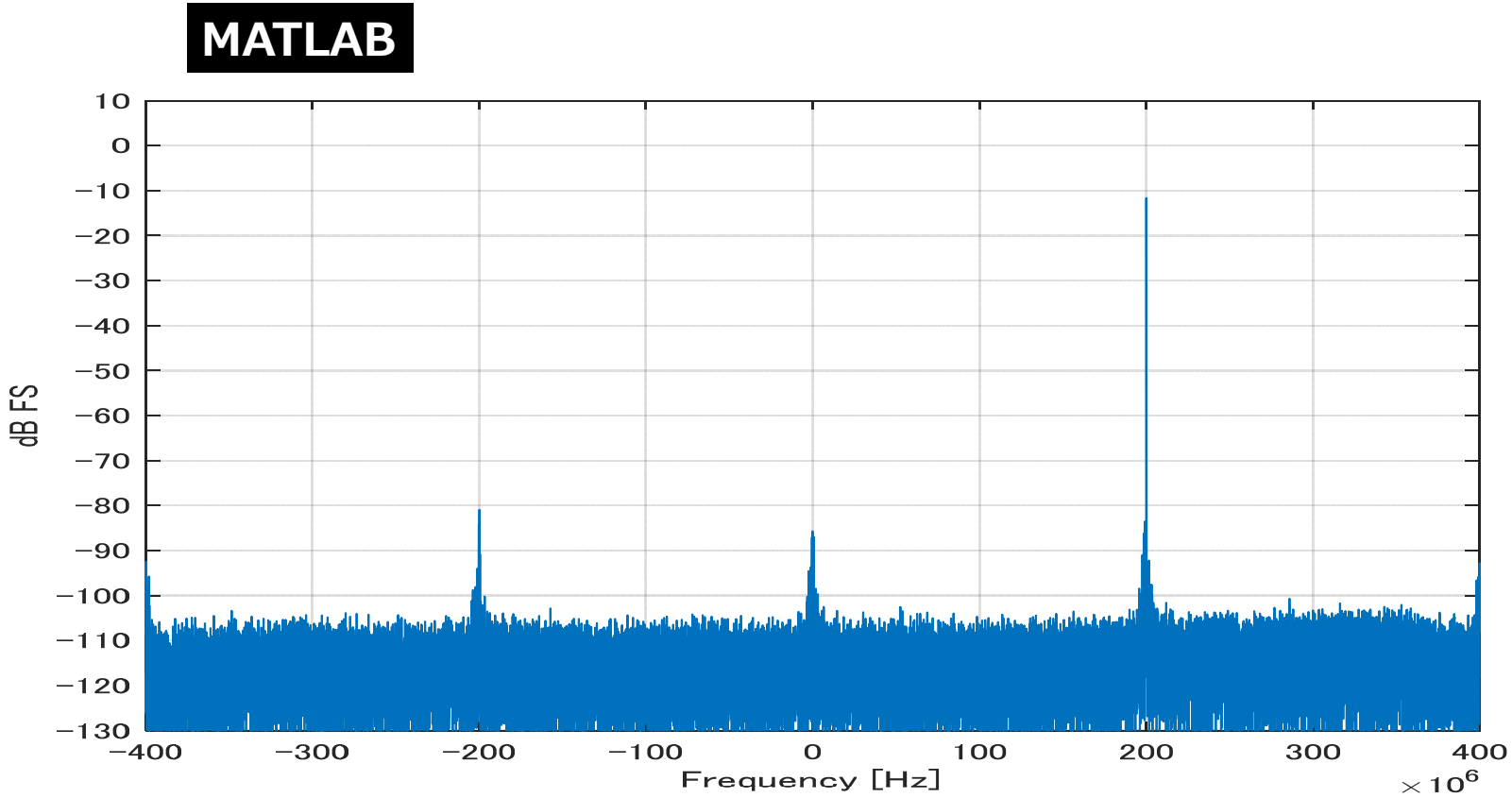

-60dBFS spurious around -250MHz disappears.

# HSDC_jmode11_fs3200M_fnco1200M_fin1000M_LPF



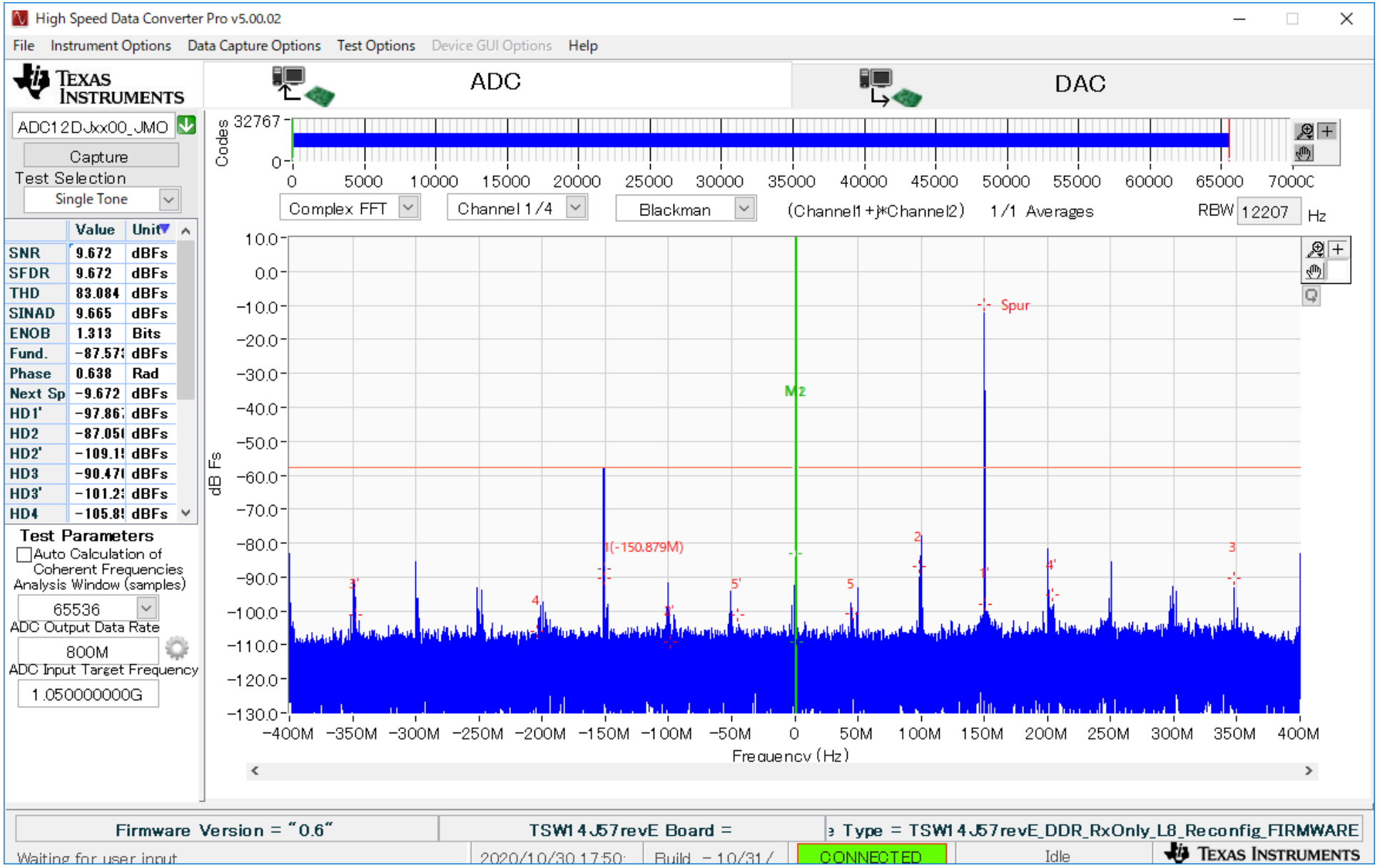
# HSDC_jmode11_fs3200M_fnco1200M_fin1000M_LPF

FFT results by MATLAB for IQ data exported from HSDC



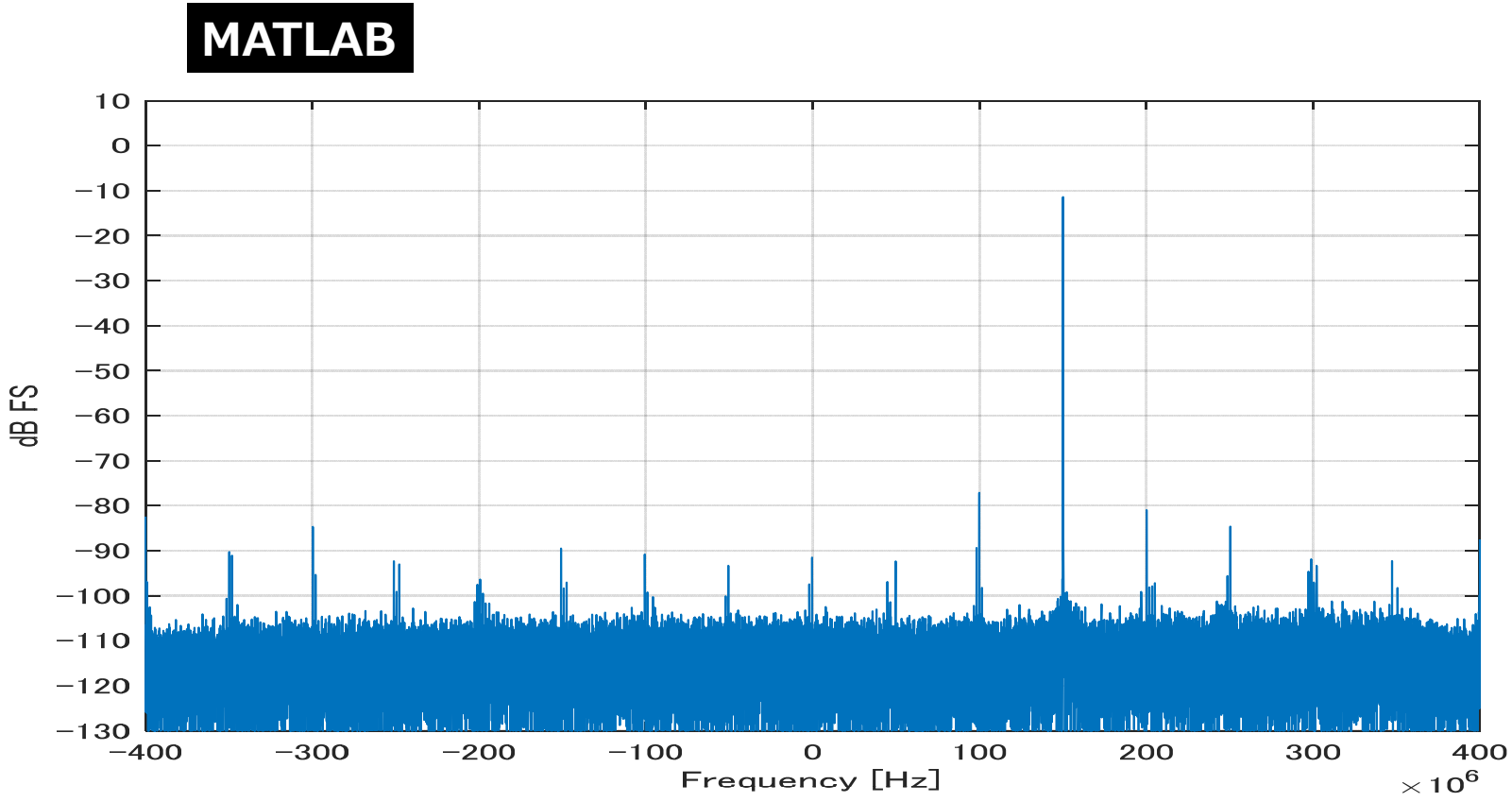

-10dBFS spectrum exists near +200MHz.

# HSDC_jmode11_fs3200M_fnco1200M_fin1050M_LPF



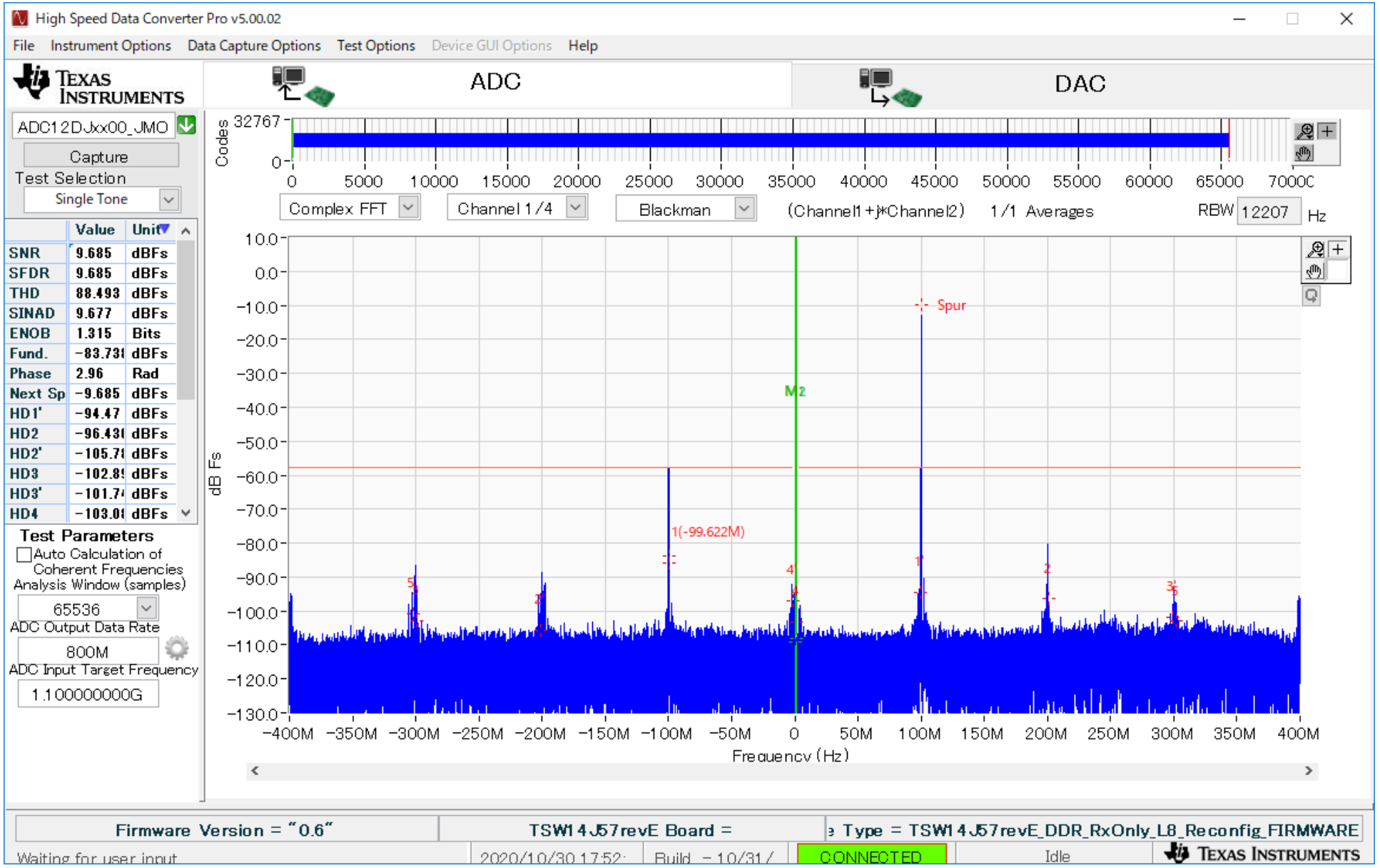
# HSDC_jmode11_fs3200M_fnco1200M_fin1050M_LPF

FFT results by MATLAB for IQ data exported from HSDC



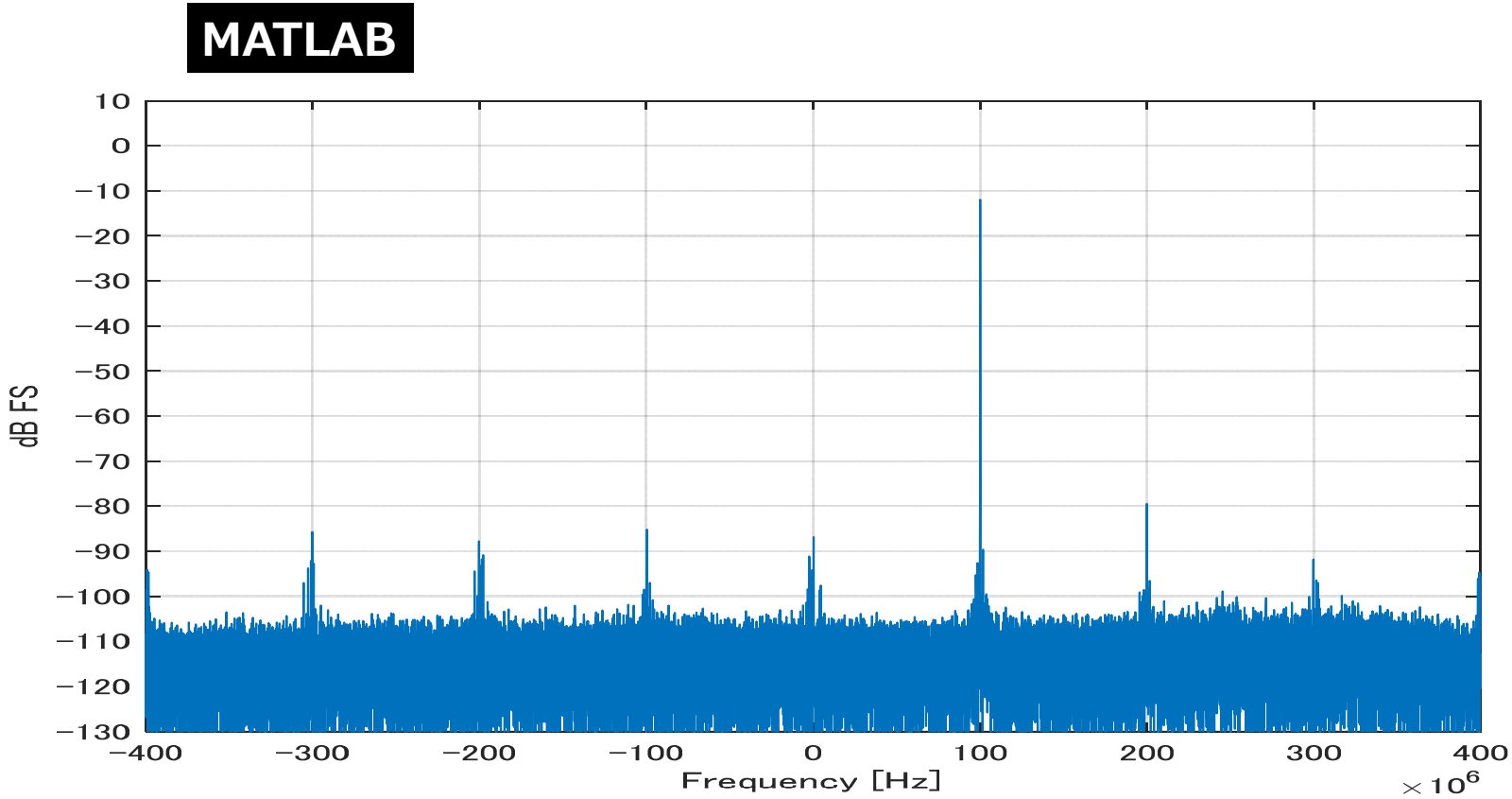

-60dBFS spurious around -150MHz disappears.

# HSDC_jmode11_fs3200M_fnco1200M_fin1100M_LPF



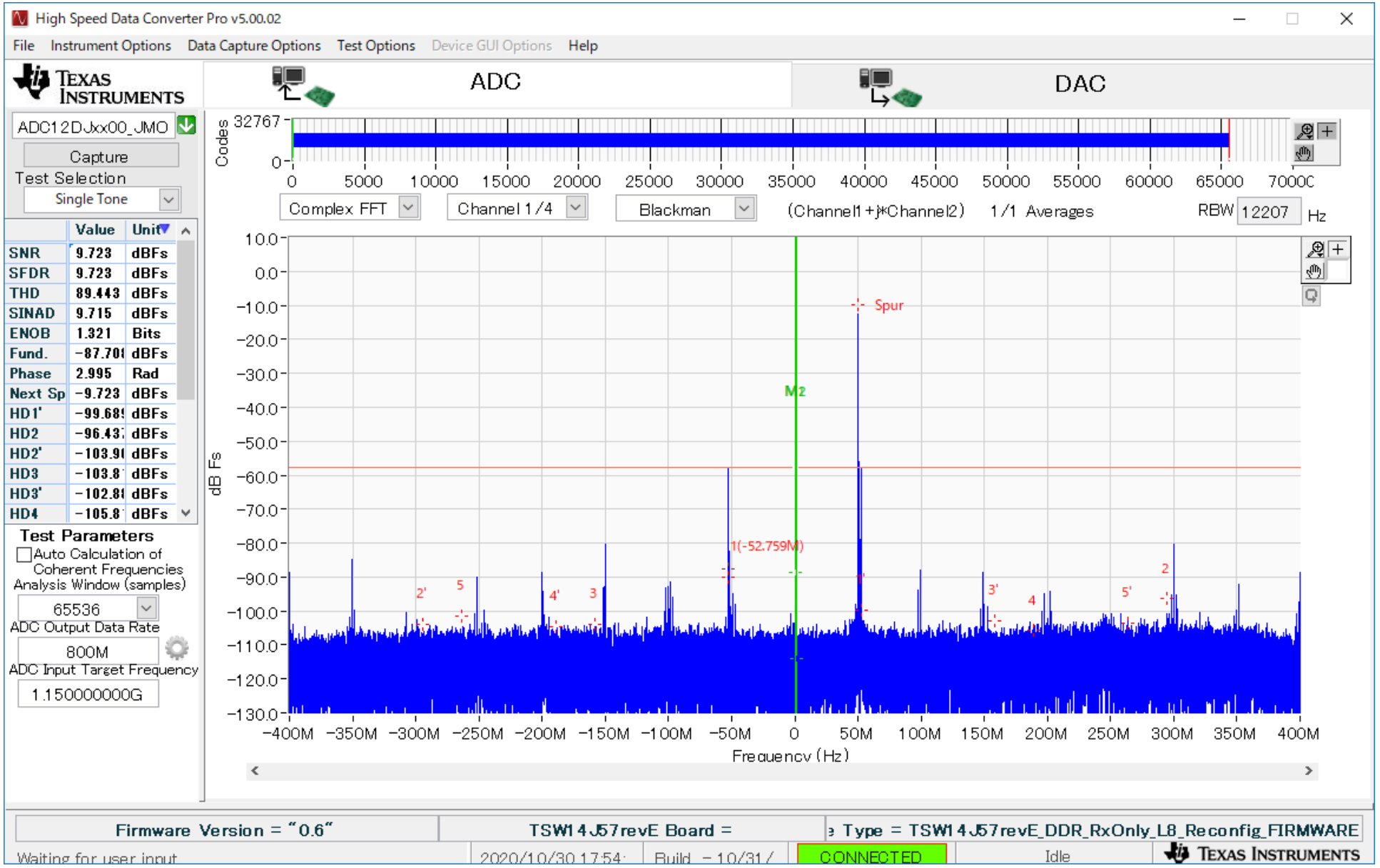
# HSDC_jmode11_fs3200M_fnco1200M_fin1100M_LPF

FFT results by MATLAB for IQ data exported from HSDC



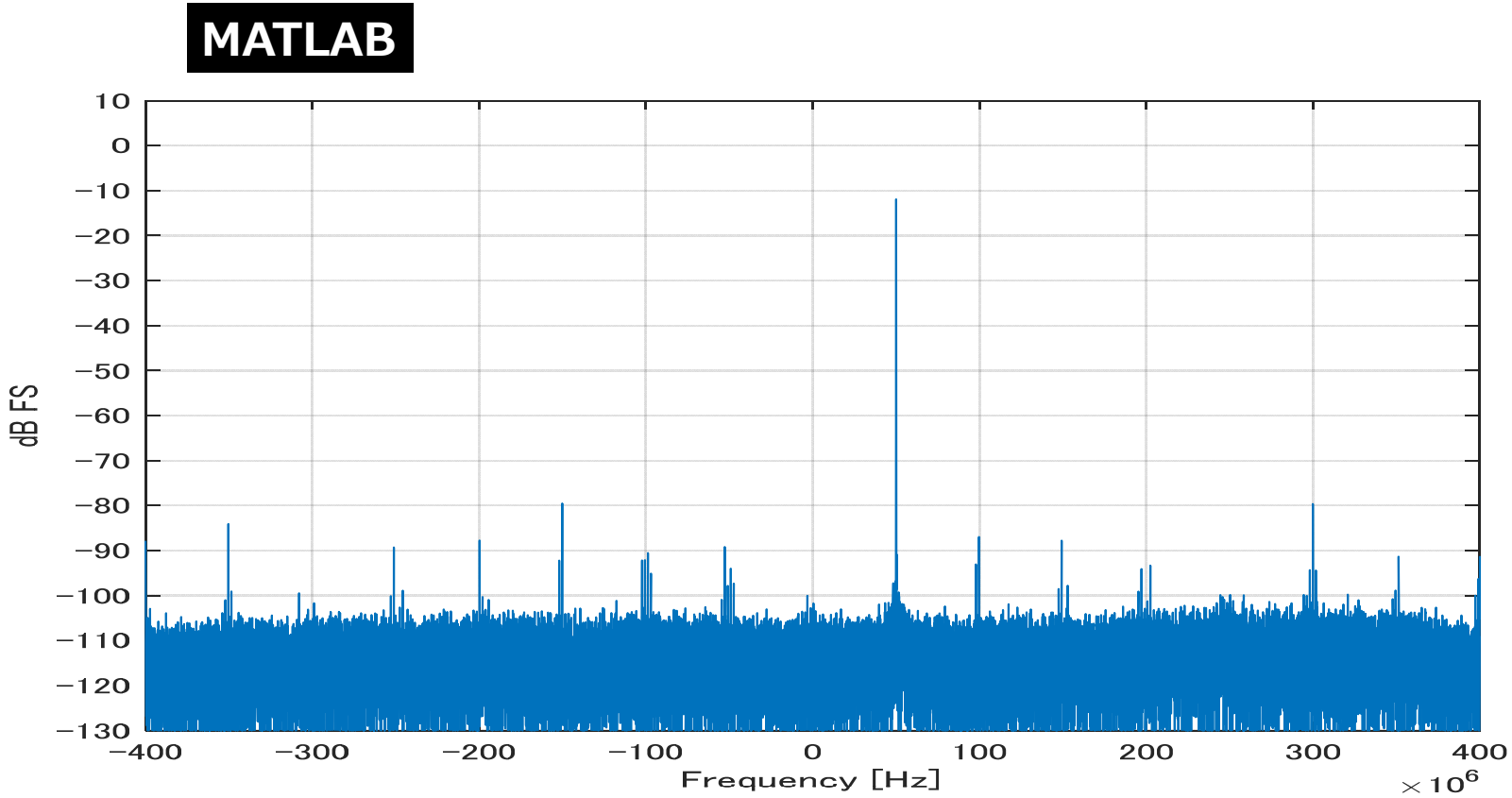

-60dBFS spurious around -100MHz disappears.

# HSDC_jmode11_fs3200M_fnco1200M_fin1150M_LPF



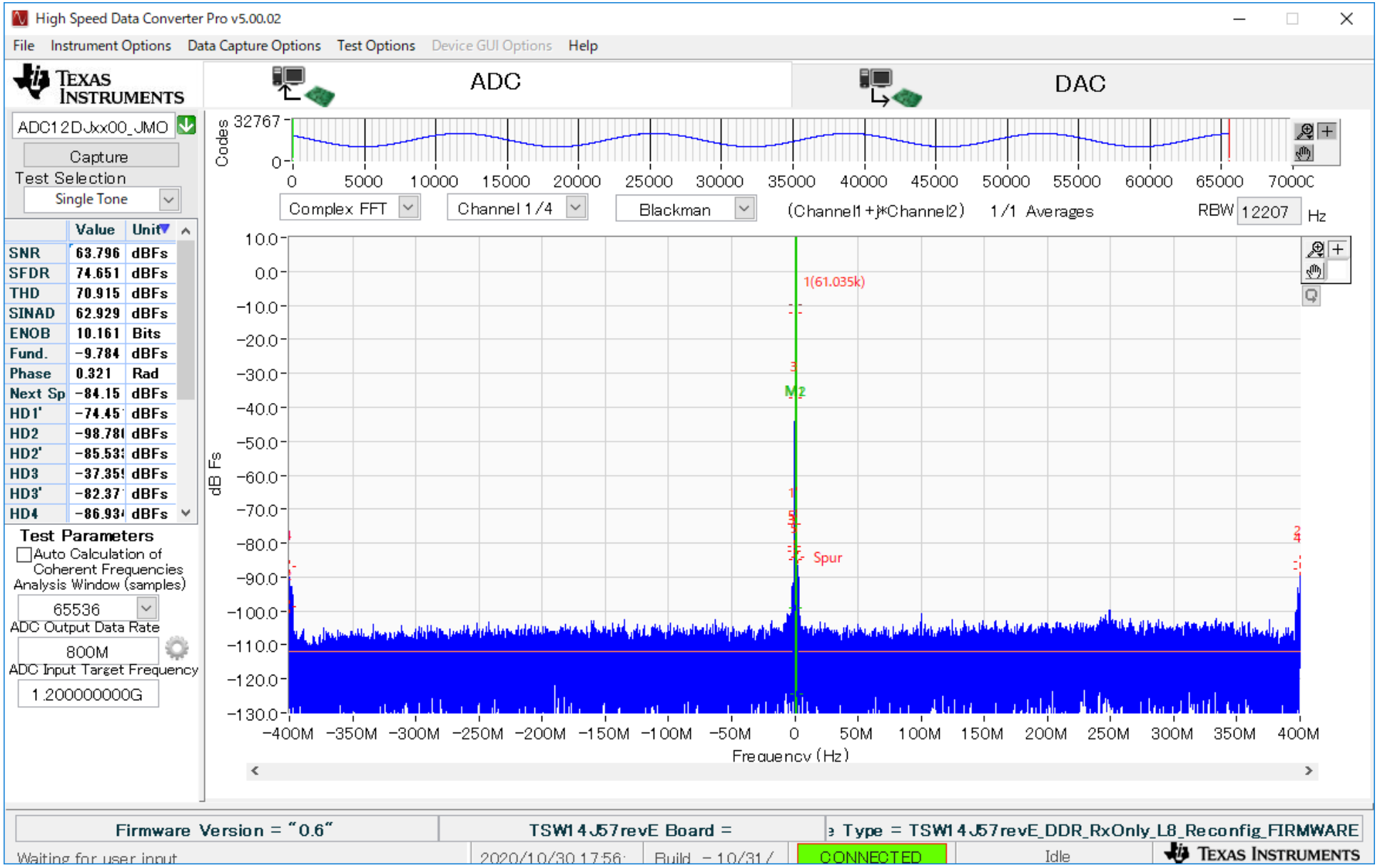
# HSDC_jmode11_fs3200M_fnco1200M_fin1150M_LPF

FFT results by MATLAB for IQ data exported from HSDC



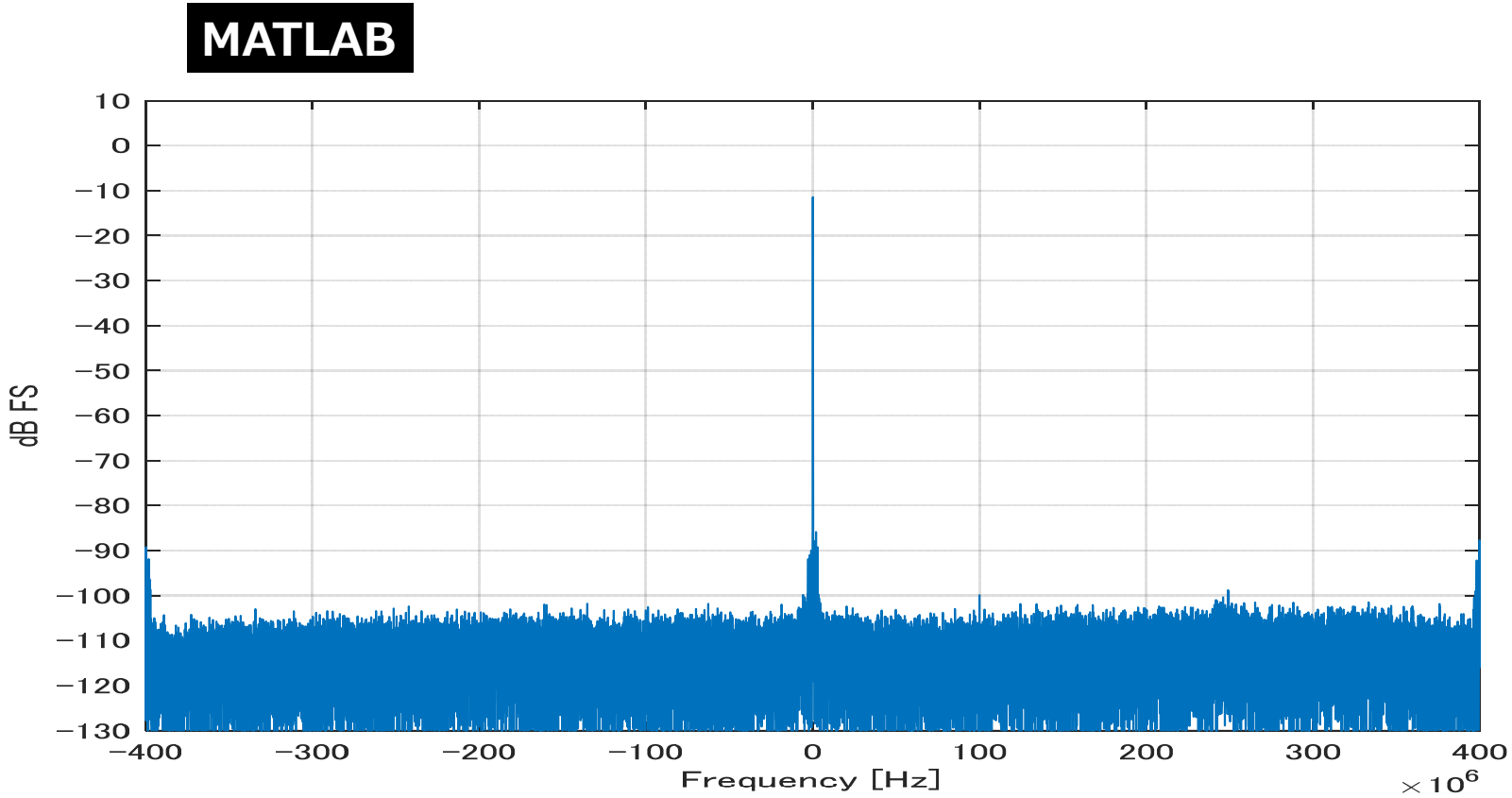

-60dBFS spurious around -50MHz disappears.

# HSDC_jmode11_fs3200M_fnco1200M_fin1200M_LPF

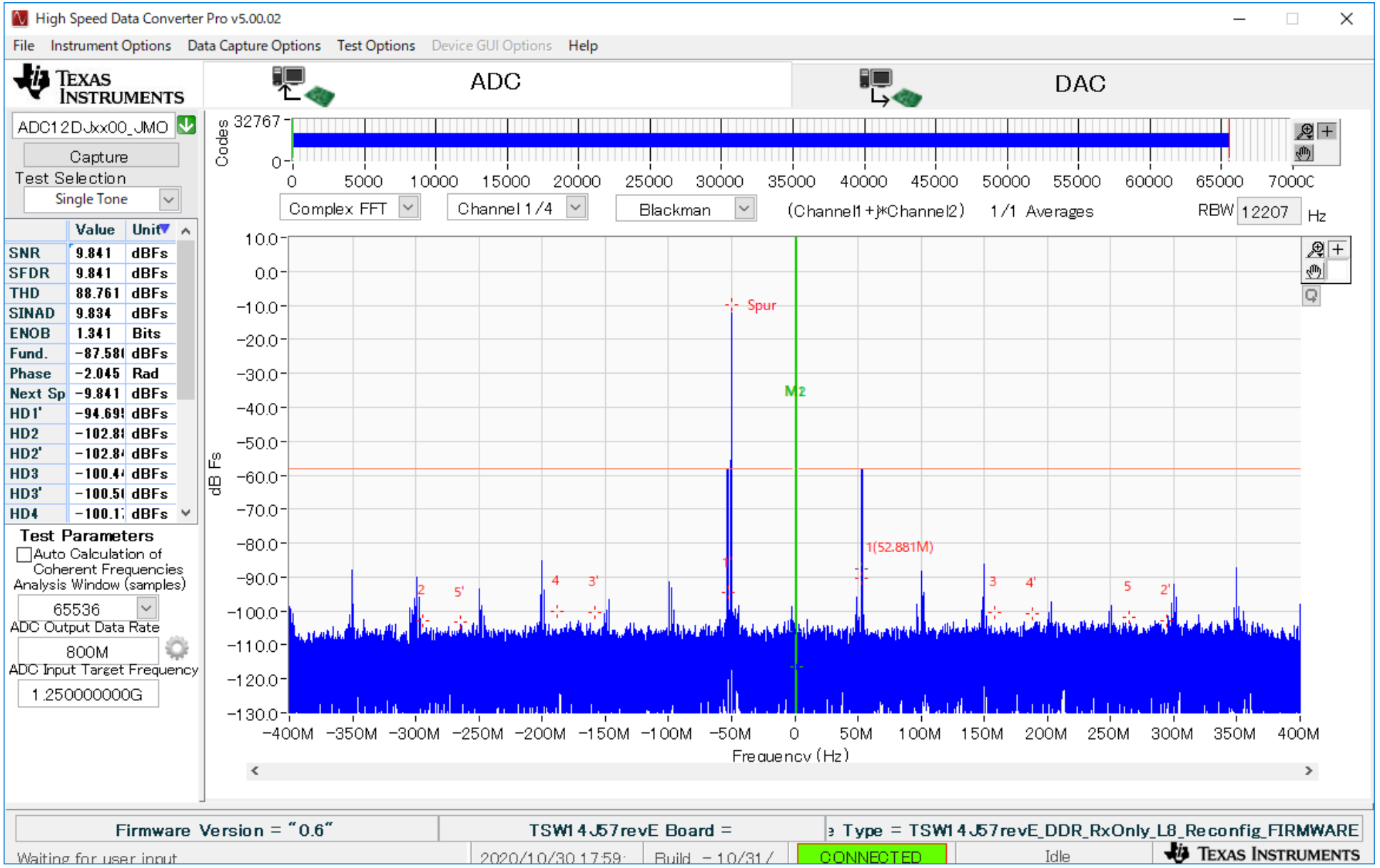


# HSDC_jmode11_fs3200M_fnco1200M_fin1200M_LPF

FFT results by MATLAB for IQ data exported from HSDC

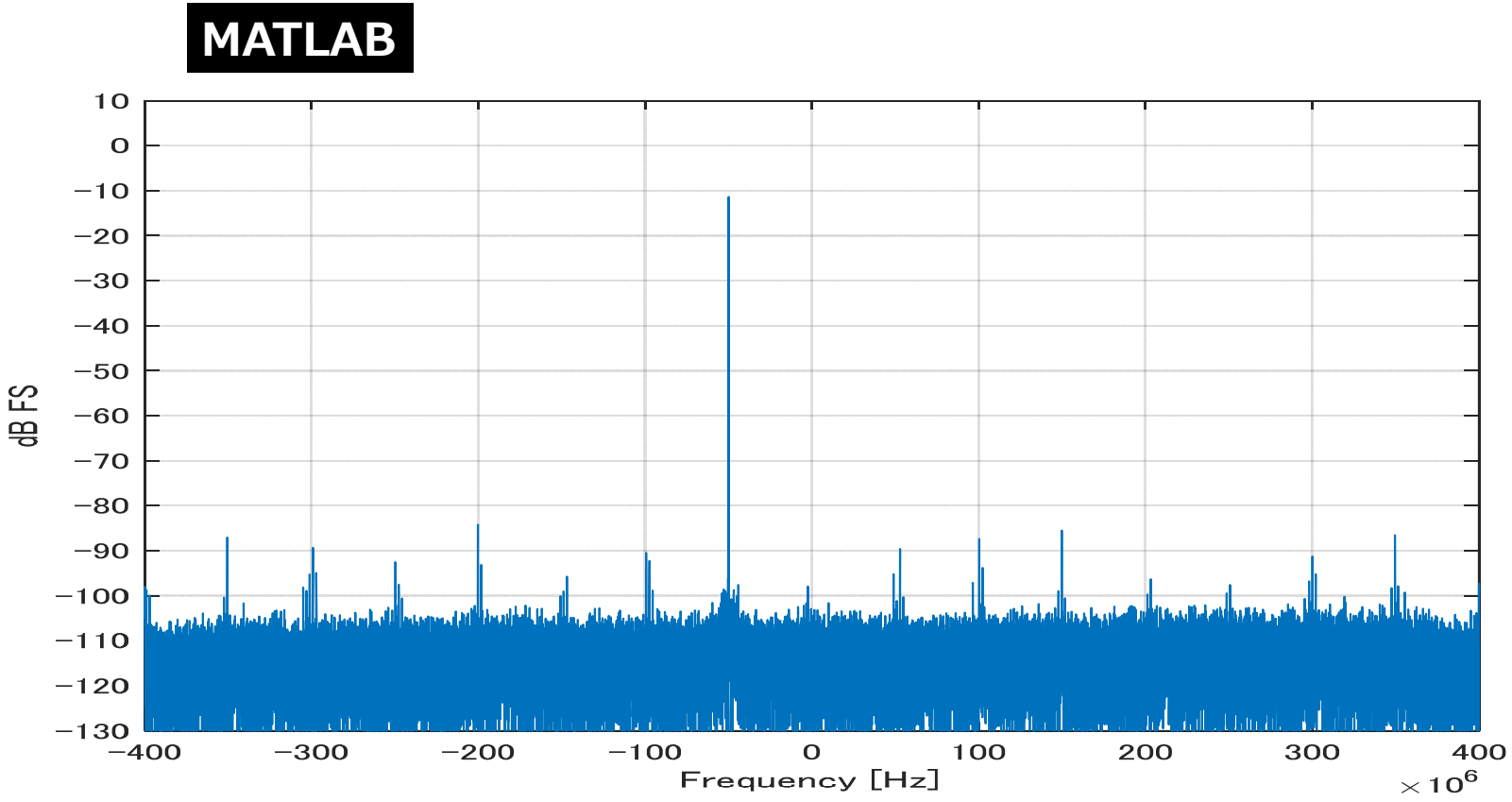


# HSDC_jmode11_fs3200M_fnco1200M_fin1250M_LPF



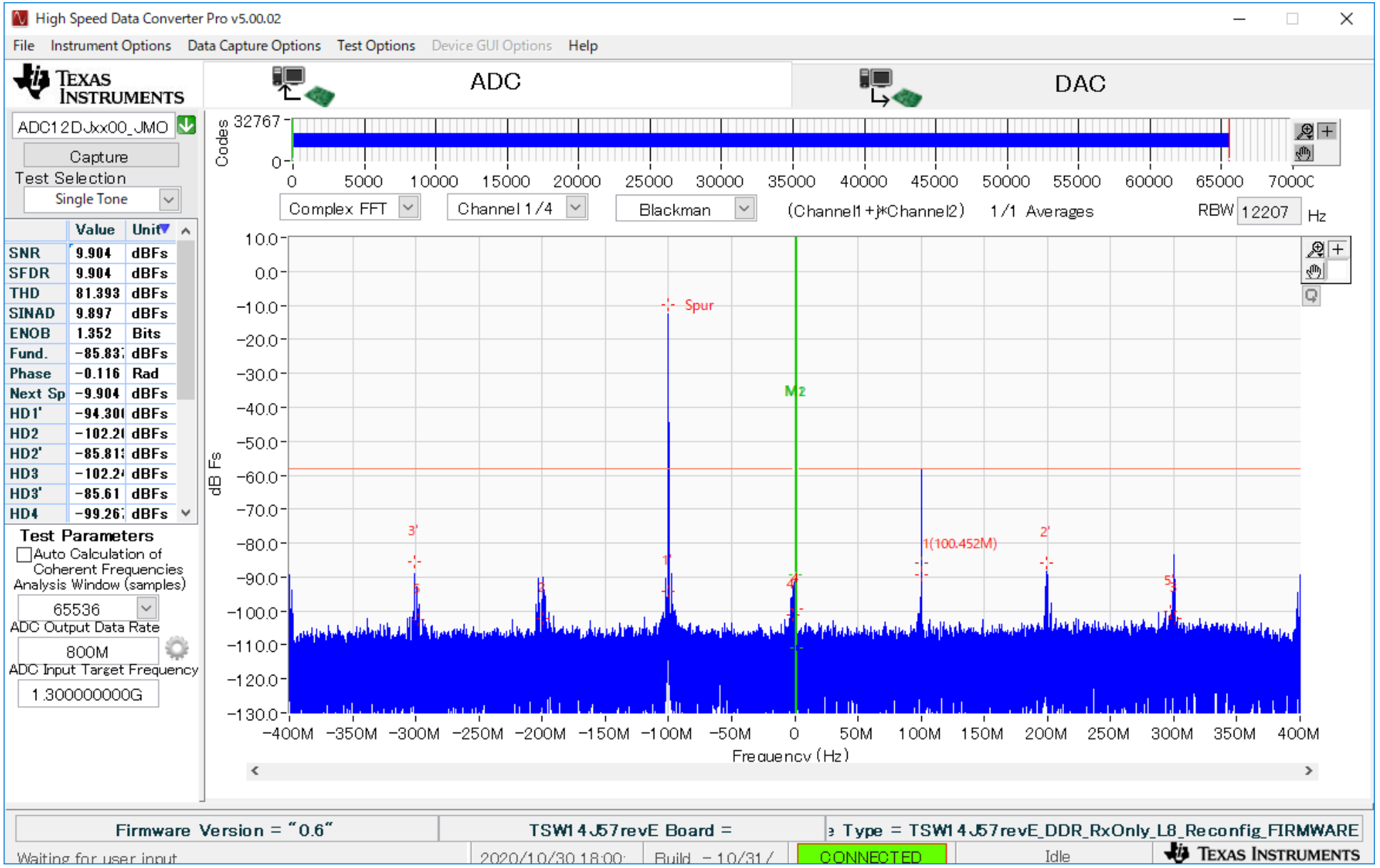
# HSDC_jmode11_fs3200M_fnco1200M_fin1250M_LPF

FFT results by MATLAB for IQ data exported from HSDC



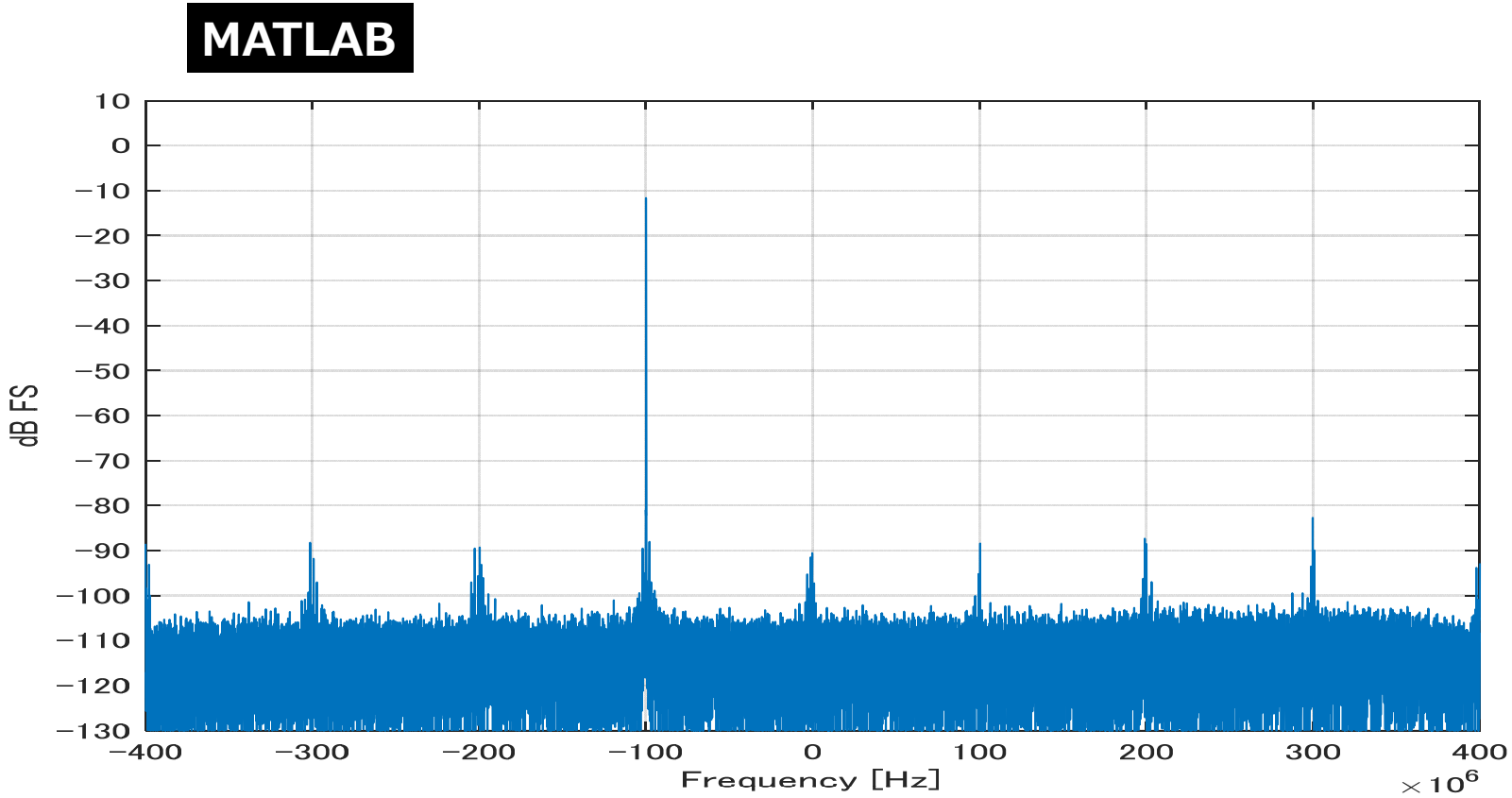

-60dBFS spurious around +50MHz disappears.

# HSDC_jmode11_fs3200M_fnco1200M_fin1300M_LPF



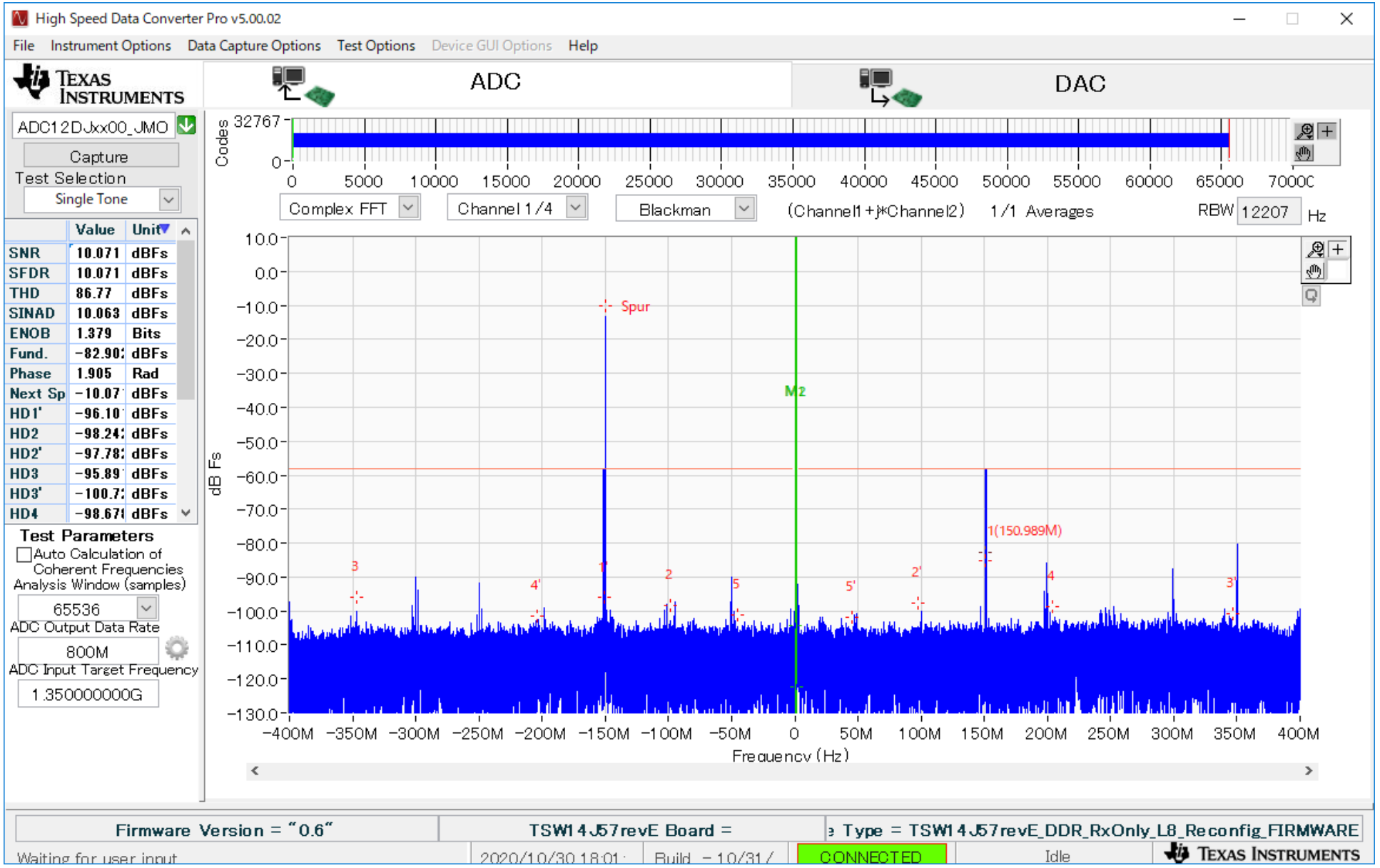
# HSDC_jmode11_fs3200M_fnco1200M_fin1300M_LPF

FFT results by MATLAB for IQ data exported from HSDC



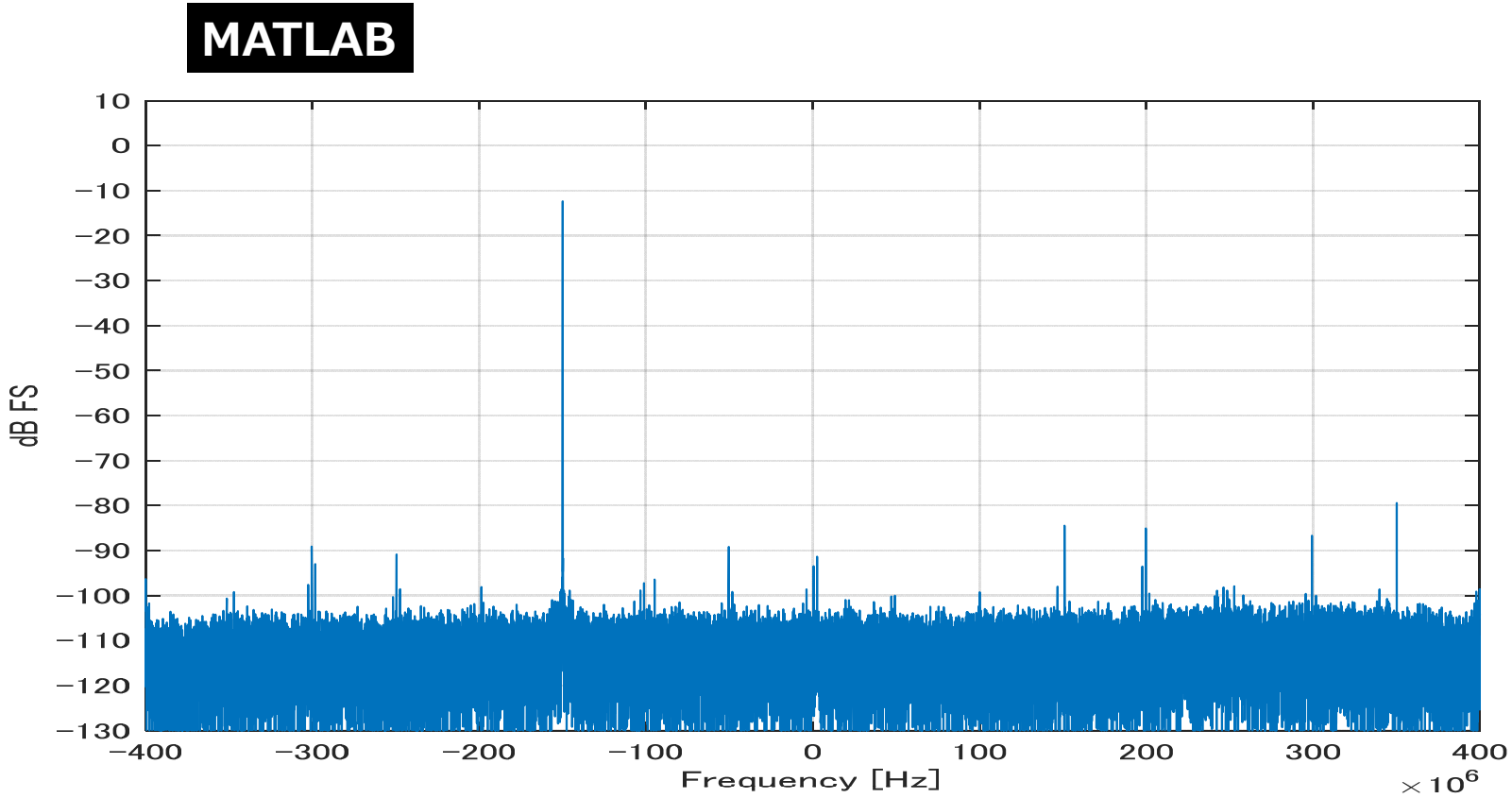

-60dBFS spurious around +100MHz disappears.

# HSDC_jmode11_fs3200M_fnco1200M_fin1350M_LPF



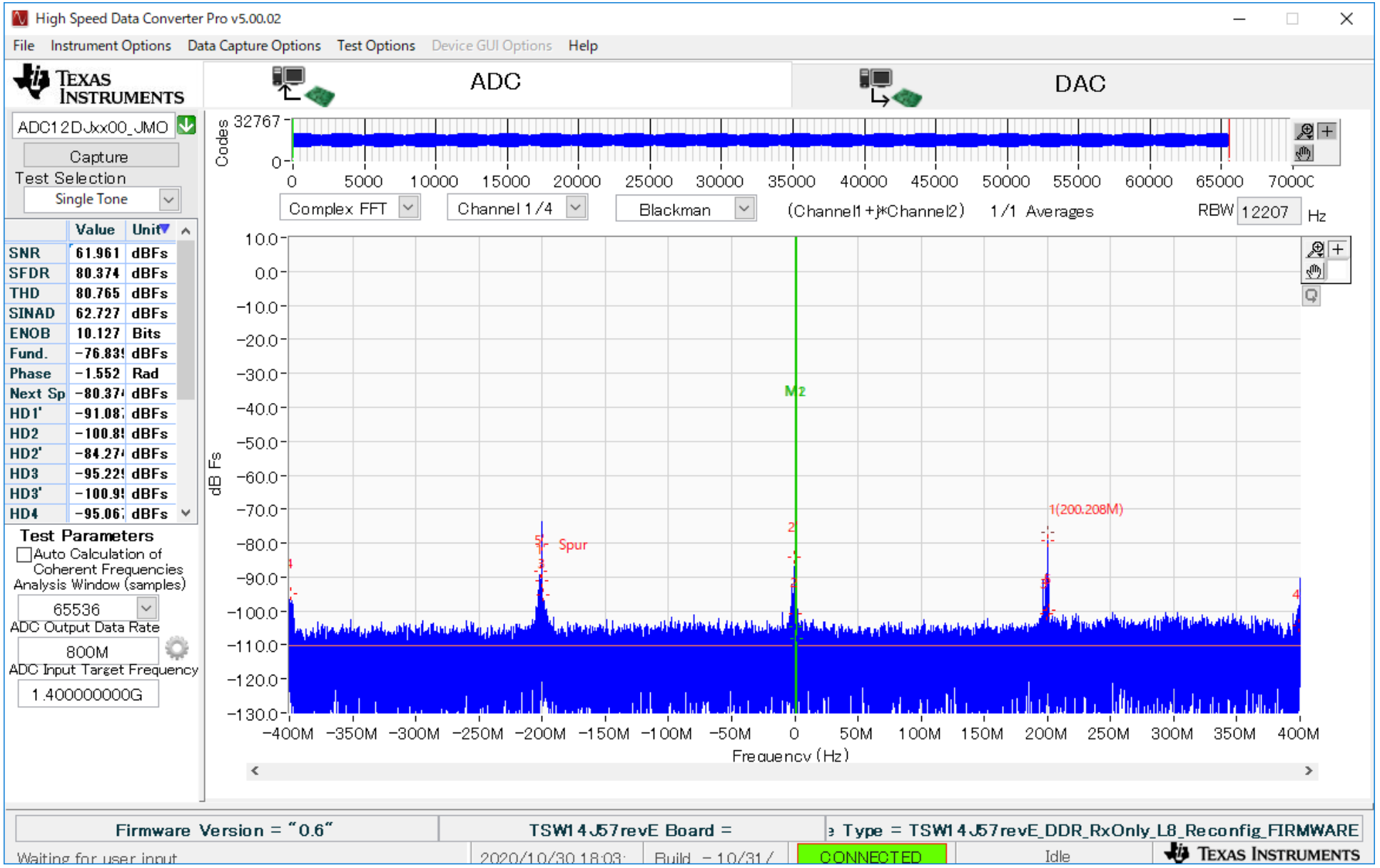
# HSDC_jmode11_fs3200M_fnco1200M_fin1350M_LPF

FFT results by MATLAB for IQ data exported from HSDC



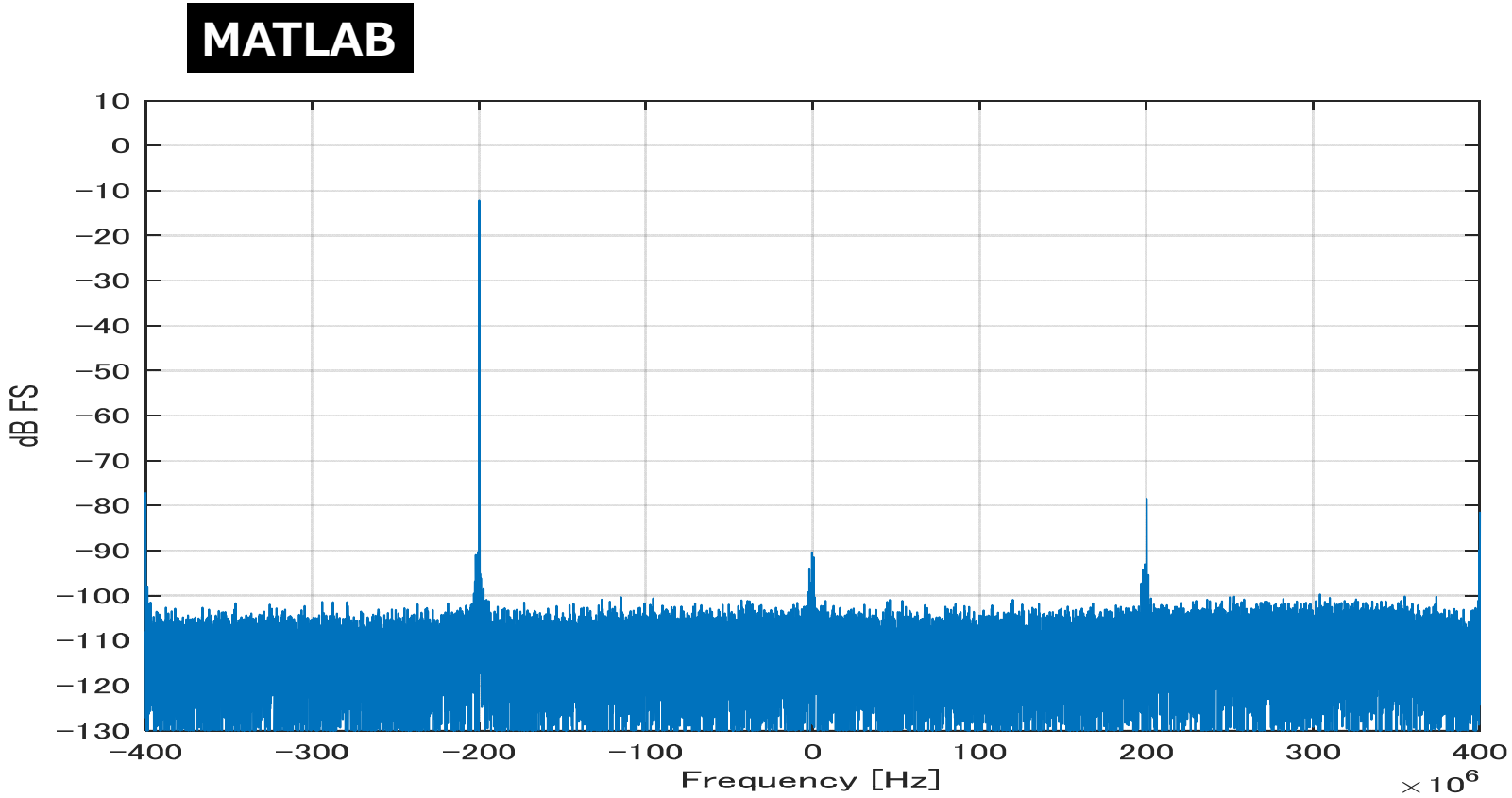

-60dBFS spurious around +150MHz disappears.

# HSDC_jmode11_fs3200M_fnco1200M_fin1400M_LPF



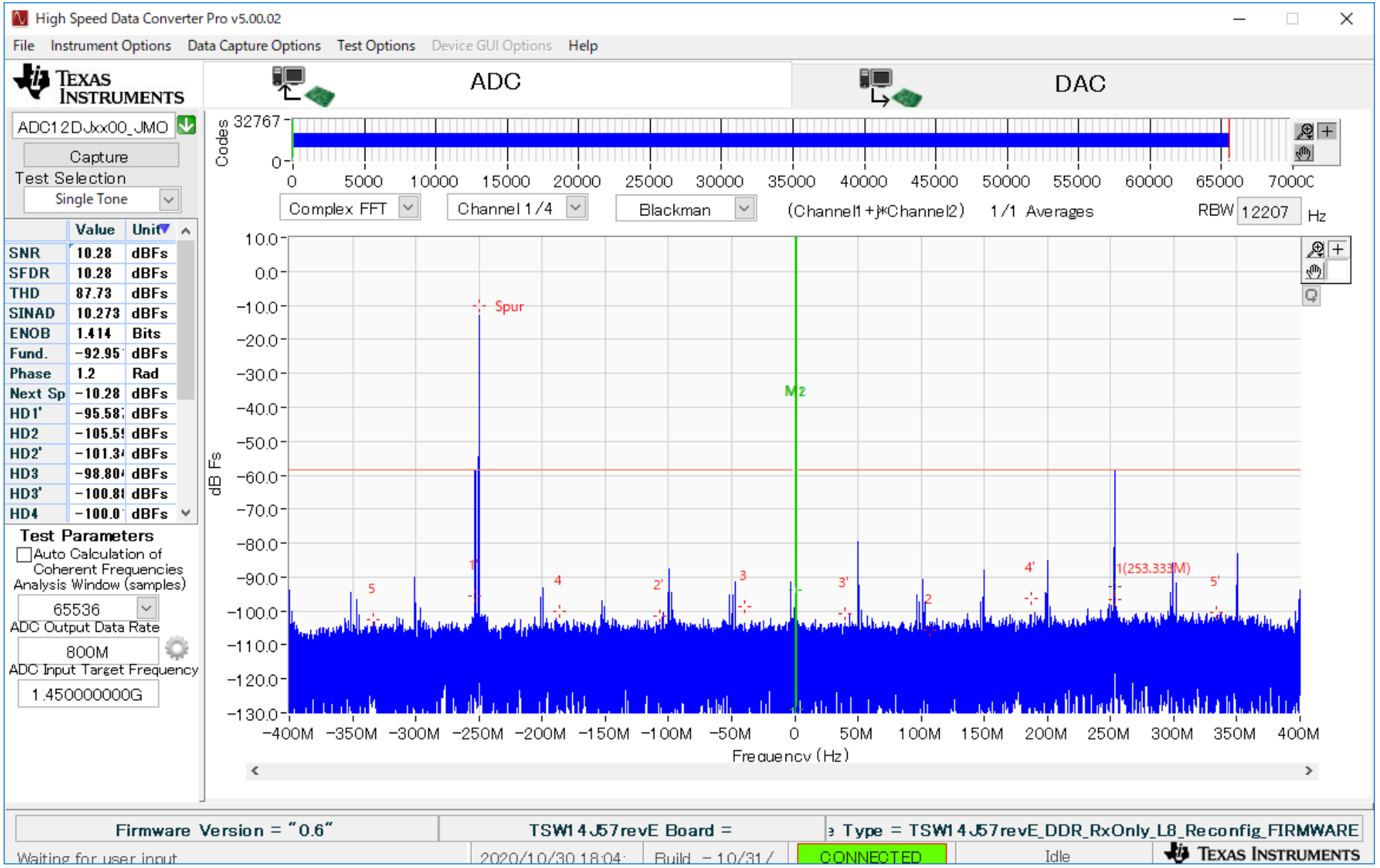
# HSDC_jmode11_fs3200M_fnco1200M_fin1400M_LPF

FFT results by MATLAB for IQ data exported from HSDC



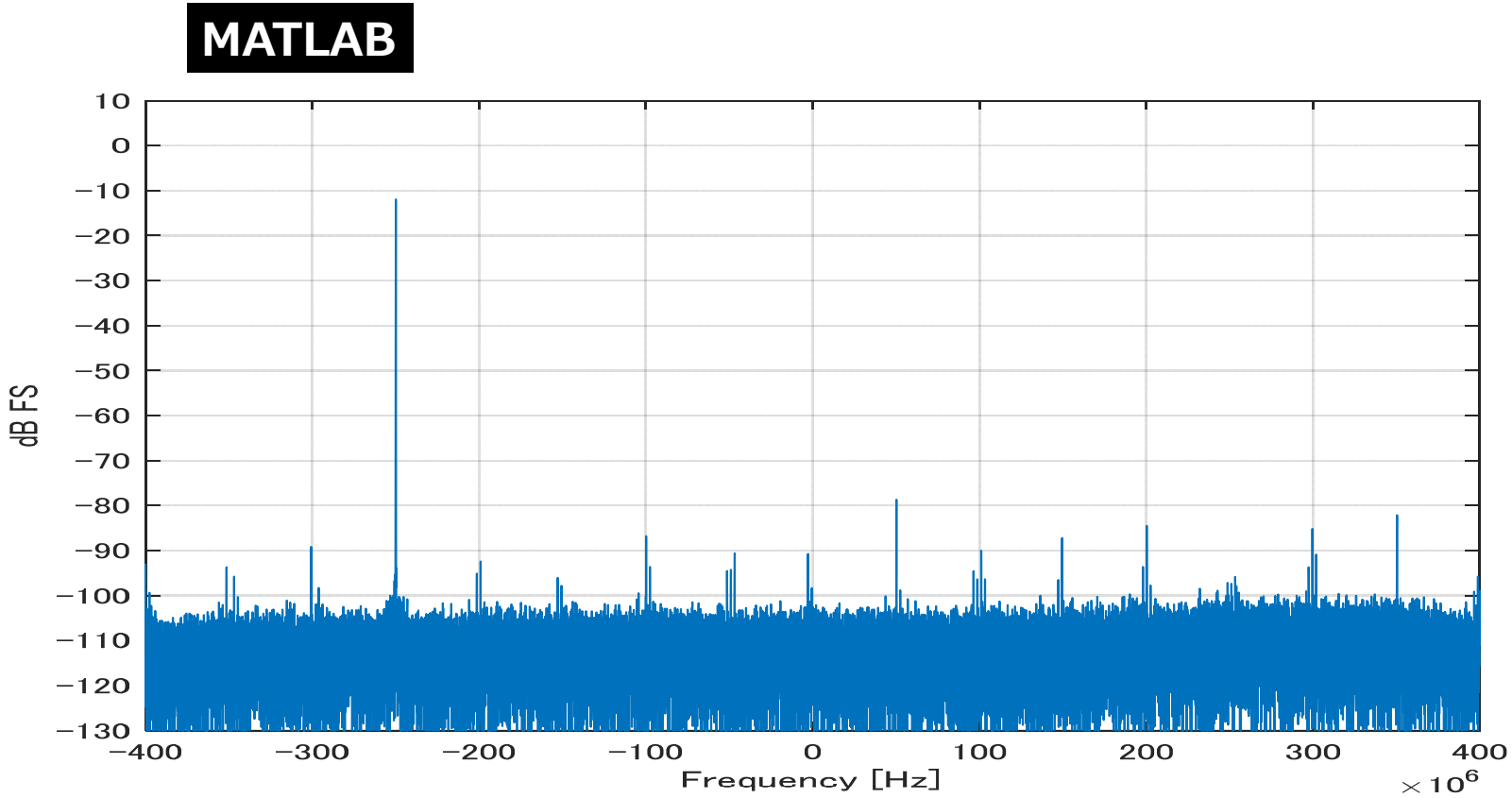

-10dBFS spectrum exists near -200MHz.

# HSDC_jmode11_fs3200M_fnco1200M_fin1450M_LPF



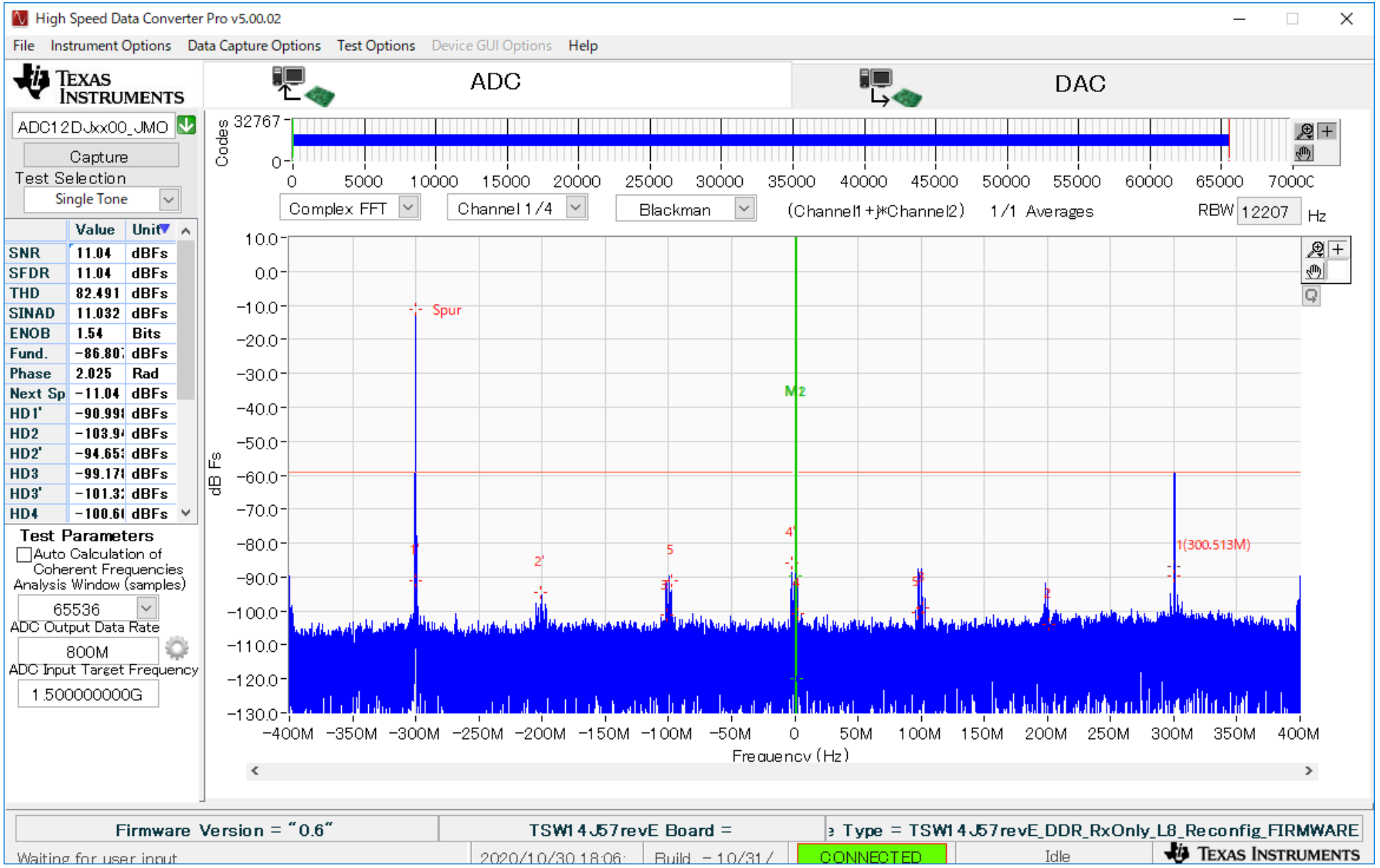
# HSDC_jmode11_fs3200M_fnco1200M_fin1450M_LPF

FFT results by MATLAB for IQ data exported from HSDC



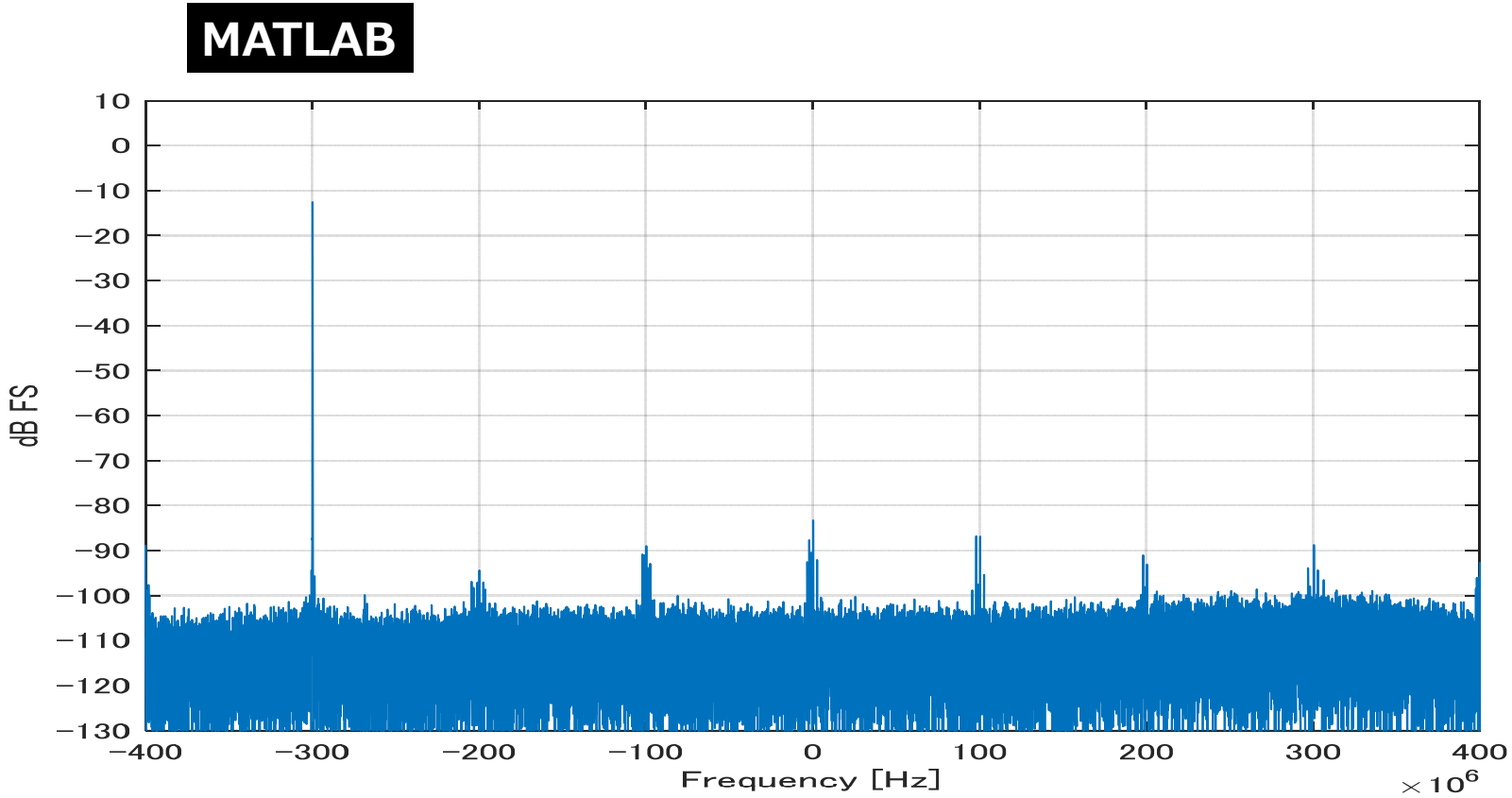

-60dBFS spurious around +250MHz disappears.

# HSDC_jmode11_fs3200M_fnco1200M_fin1500M_LPF



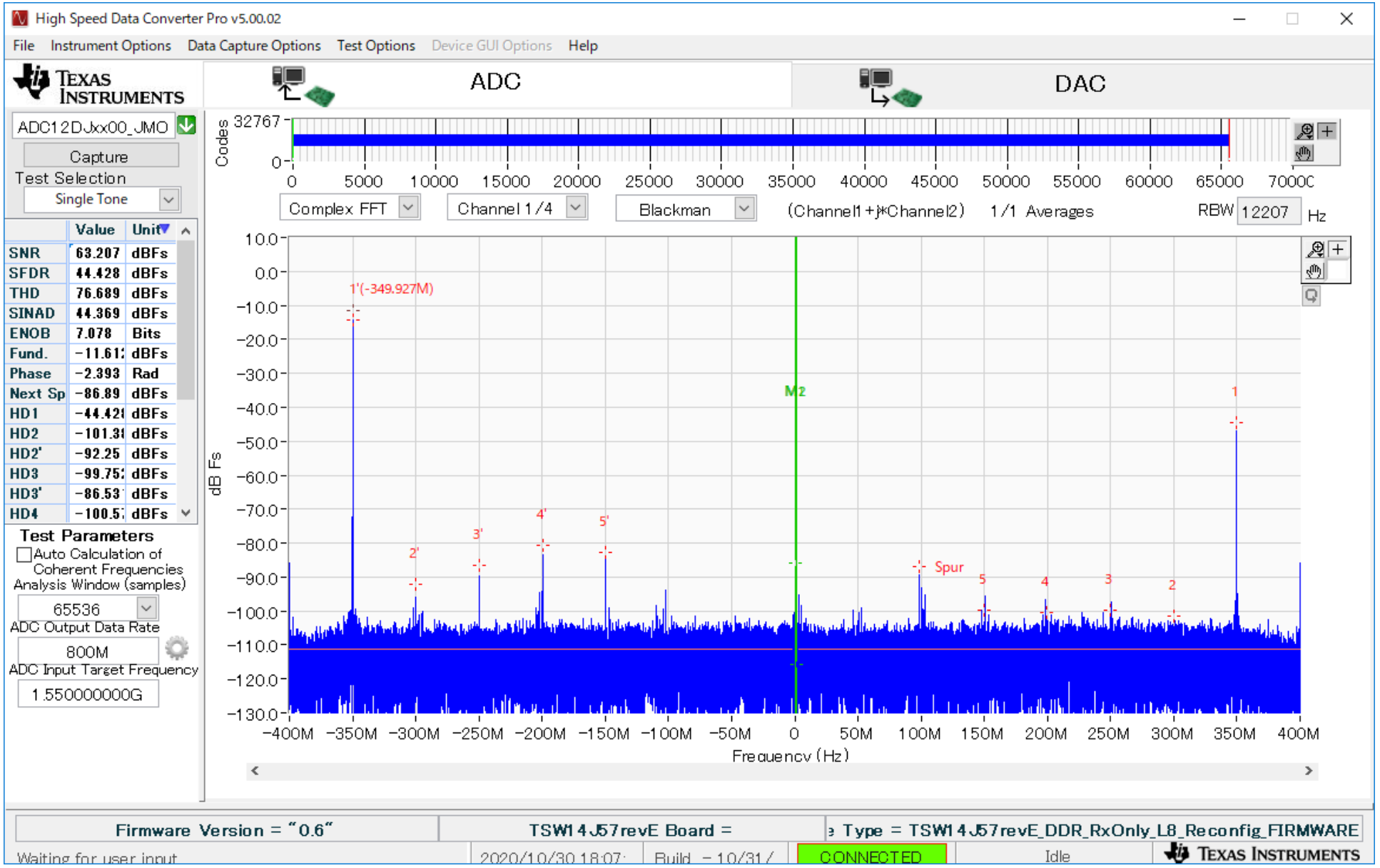
# HSDC_jmode11_fs3200M_fnco1200M_fin1500M_LPF

FFT results by MATLAB for IQ data exported from HSDC



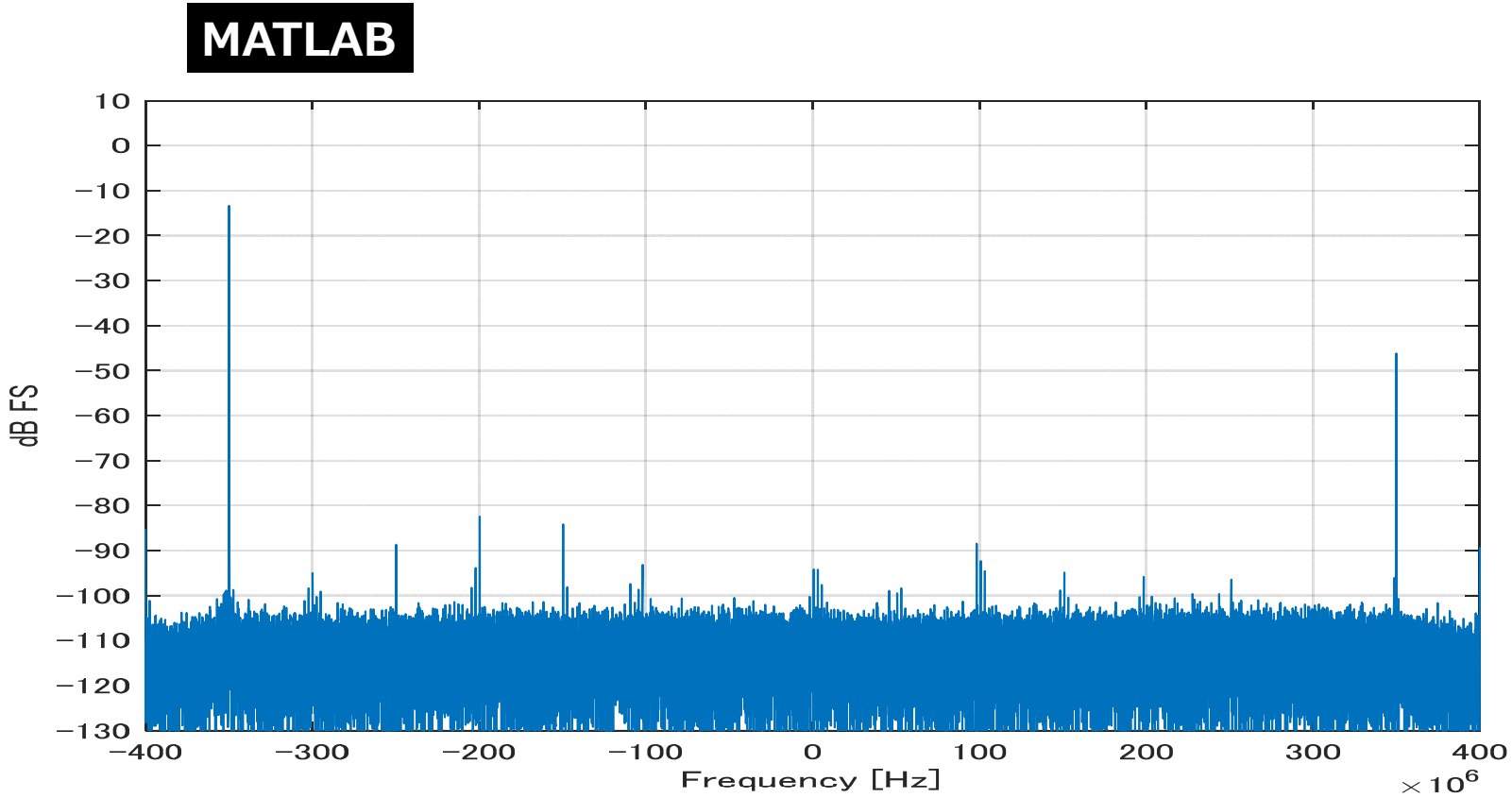

-60dBFS spurious around +300MHz disappears.

# HSDC_jmode11_fs3200M_fnco1200M_fin1550M_LPF



# HSDC_jmode11_fs3200M_fnco1200M_fin1550M_LPF

FFT results by MATLAB for IQ data exported from HSDC




The results are very similar, but the marker index (primes) are reversed.

# 6

# MATLAB code

# Validation of FFT results by MATLAB

```
clear
close all
pnt=65536;      % data samples
x=1:pnt;        % x-axis index vector
xf=(x-pnt/2)/(pnt/2)*400e6;     % frequency axis vector
a=csvread('HSDC_I32_codes.csv');     % read csv file
i=a(:,1)./16384;        % Normalize the I-ch signal (signed 15bit)
q=a(:,2)./16384;        % Normalize the Q-ch signal (signed 15bit)
c=(i+1j*q);             % Complex signal
w = blackman(pnt);          % Window function
f=20*log10(abs(fft(w.*c)./(pnt/2)));    % spectrum in dB
f2=circshift(f,(pnt/2));        % Shift DC to center
plot(xf,f2')
```