ECG 12 Channel Mainboard

Variant: [No Variations]

4/26/2024
V2.1

DESIGN CONSIDERATIONS

DESIGN NOTE:
Example text for informational design notes .

LAYOUT NOTE:
Example text for critical layout guidelines.

DESIGN NOTE:
Example text for critical design notes.

DESIGN NOTE:
Example text for debug notes.

DESIGN NOTE:
Stresses beyond those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability

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[Platform] TitleBlock

ECG 12 Channel Mainboard

(Block Diagram)

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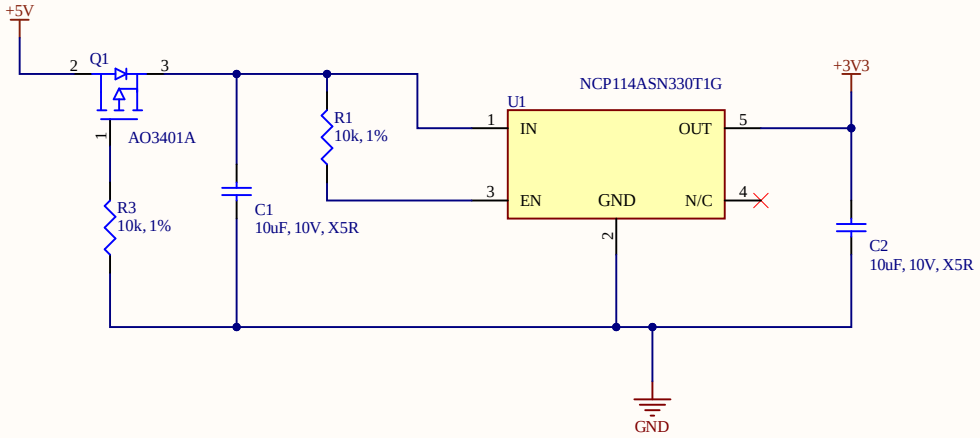
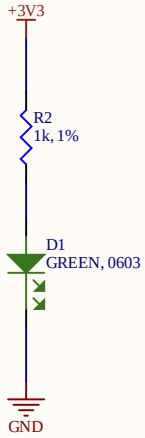
POWER, MECH, LED

LDO



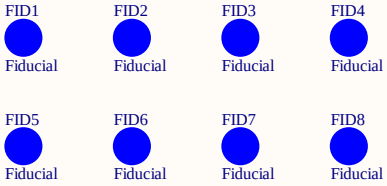
Power LED



Mounting Holes

Mounting holes 2mm pad 2mm drill
BOARD MOUNTING HOLES
4x ON THE CORNERS

Fiducials



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AFE, CONNECTOR

Connector to ECG Cable

J1 — AFC07-S12FCC-00
ELEC_RL, ELEC_V1, ELEC_V5, ELEC_V4, ELEC_V3, ELEC_V2, ELEC_LL, ELEC_LA, ELEC_RA, ELEC_V6
TP1 (+3V3), TP2 (+3V3_AFE_AVDD), TP3 (+3V3_AFE_DVDD), TP4

FB1 300mA, 0.52R; R4 1R, 1%
C9 10uF, 10V, X5R; C10 10uF, 10V, X5R; C11 10uF, 10V, X5R
pin A4 C3, pin A6 C4, pin B4 C5, pin B6 C6, pin C6 C7, pin A7 C8 — 100nF, 10V, X5R

FB2 300mA, 0.52R
pin D8 C12 1uF, 10V, X5R; pin D8 C13 100nF, 10V, X5R; pin C8 C14 1uF, 10V, X5R; pin C8 C15 100nF, 10V, X5R

Connector to Raspberry

J2 — AFC07-S10FCC-00
AFE_RESET, AFE_PWDN, AFE_START, AFE_SPI_CS, AFE_DRDY, AFE_SPI_MOSI, AFE_SPI_SCK, AFE_SPI_MISO

AFE

U2 — ADS1298RIZXGT

A4, A6, B4, B6, C6, A7	AVDD, AVDD1		
C8, D8	DVDD		
H1	IN1P	ECG_V6	
H2	IN1N		
G1	IN2P	ECG_LA	
G2	IN2N		
F1	IN3P	ECG_LL	
F2	IN3N	ECG_RA	
E1	IN4P	ECG_V2	
E2	IN4N		
D1	IN5P	ECG_V3	
D2	IN5N		
C1	IN6P	ECG_V4	
C2	IN6N		
B1	IN7P	ECG_V5	
B2	IN7N		
A1	IN8P	ECG_V1	
A2	IN8N		
D3	WCT	AFE_WCT	C35 1nF, 25V, X7R
F7	$\overline{CS}$	AFE_SPI_CS	
H8	DIN/MOSI	AFE_SPI_MOSI	
E8	DOUT/MISO	AFE_SPI_MISO	
F8	SCLK	AFE_SPI_SCK	
G7	START	AFE_START	
G6	$\overline{RESET}$	AFE_RESET	
G5	$\overline{PWDN}$	AFE_PWDN	
D6	$\overline{DRDY}$	AFE_DRDY	
H3	VREFP	AFE_VREFP	C24 100nF, 10V, X5R; C25 10uF, 10V, X5R
H4	VREFN		
G8	CLK		R21 1k, 1%
B8	CLKSEL	AFE_CLKSEL	
C3	RLDINV	AFE_RLDINV	C34 1.5nF, 16V, X5R; R26 1M, 1%
B3	RLDOUT	AFE_RLDOUT	0R R27 ECG_RL
A3	RLDIN		0R R28
C4	RLDREF		
F6	DAISY_IN		
E3	TESTP_PACE_OUT1		
F3	TESTN_PACE_OUT2		
F5	GPIO1		
E5	GPIO3		
E6	GPIO4		
G4	RESP_MODP		
F4	RESP_MODN		
E4	RESV1		
H5	VCAP1	AFE_VCAP1	
H6	VCAP2	AFE_VCAP2	
B7	VCAP3	AFE_VCAP3	
G3	VCAP4	AFE_VCAP4	C43 1uF, 10V, X5R; C44 1uF, 10V, X5R; C40 100nF, 10V, X5R; C41 1uF, 10V, X5R; C42 22uF, 10V, X5R
A8, A5, B5, C5, D4, D5	AVSS1, AVSS		
C7, D7, H7	DGND		

+3V3_AFE_DVDD: R9 10k, 1%; R10 10k, 1%; R11 10k, 1%; R12 10k, 1%

DESIGN NOTE:
VCAP1: AVSS + 1.2V
VCAP2: (AVDD+ AVSS)/2
VCAP3: AVDD + 1.3V

ELEC_V6, ELEC_LA, ELEC_LL, ELEC_RA, ELEC_V2, ELEC_V3, ELEC_V4, ELEC_V5, ELEC_V1, ELEC_RL

R5 22k, 1%	R6 10k, 1%	C16 47pF, 25V, C0G	C17 47pF, 25V, C0G
R7 22k, 1%	R8 10k, 1%	C18 47pF, 25V, C0G	C19 47pF, 25V, C0G
R13 22k, 1%	R14 10k, 1%	C20 47pF, 25V, C0G	C21 47pF, 25V, C0G
R15 22k, 1%	R16 10k, 1%	C22 47pF, 25V, C0G	C23 47pF, 25V, C0G
R17 22k, 1%	R18 10k, 1%	C26 47pF, 25V, C0G	C27 47pF, 25V, C0G
R19 22k, 1%	R20 10k, 1%	C28 47pF, 25V, C0G	C29 47pF, 25V, C0G
R22 22k, 1%	R23 10k, 1%	C30 47pF, 25V, C0G	C31 47pF, 25V, C0G
R24 22k, 1%	R25 10k, 1%	C32 47pF, 25V, C0G	C33 47pF, 25V, C0G
R29 22k, 1%	R30 10k, 1%	C36 47pF, 25V, C0G	C37 47pF, 25V, C0G
R31 22k, 1%	R32 10k, 1%	C38 47pF, 25V, C0G	C39 47pF, 25V, C0G — ECG_RL

D2, D3, D4 — RClamp0524PATCT

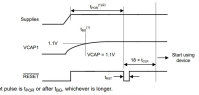
11.1 Power-Up Sequencing

Before device power up, all digital and analog inputs must be low. At the time of power up, keep all of these signals low until the power supplies have stabilized, as shown in Figure 105.

Allow time for the supply voltages to reach their final value, and then begin supplying the master clock signal to the CLK pin. Wait for time t_{POR}, then transmit a reset pulse using either the RESET pin or RESET command to initialize the digital portion of the chip. Issue the reset after t_{POR} or after the VCAP1 voltage is greater than 1.1 V, whichever time is longer. Note that:

- t_{POR} is described in Table 38.
- The VCAP1 pin charge time is set by the RC time constant; see Figure 31.

After releasing the RESET pin, program the configuration registers; see the *CONFIG1: Configuration Register 1 (address = 01h) (reset = 06h)* section for details. The power-up sequence timing is shown in Table 38.



(1) Timing to reset pulse is t_{POR} or after t_{RST}, whichever is longer.
(2) When using an external clock, t_{POR} timing does not start until CLK is valid.

Figure 105. Power-Up Timing Diagram

Table 38. Timing Requirements for Figure 105

		MIN	MAX	UNIT
t_{POR}	Wait after power up until reset	2^{16}		t_{CLK}
t_{RST}	Reset low duration	2		t_{CLK}

REVISION HISTORY

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Designator
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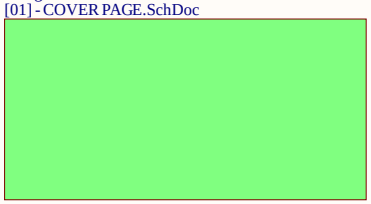
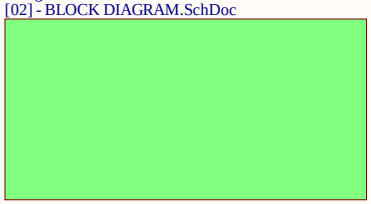


Designator
[02] - BLOCK DIAGRAM.SchDoc



Designator
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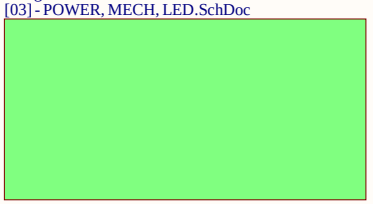
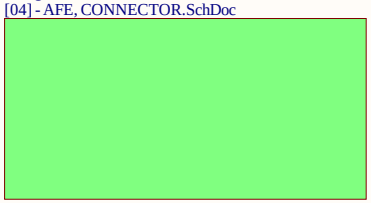
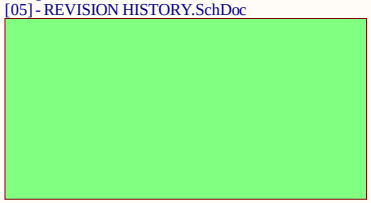


Designator
[04] - AFE, CONNECTOR.SchDoc



Designator
[05] - REVISION HISTORY.SchDoc



Mark Not Mount Components as

NF

NOTES

DRAFT - Very early stage of schematic, ignore details.

PRELIMINARY - Close to final schematic.

CHECKED - There should not be any mistakes. Tell the engineer if you find one.

RELEASED - A board with this schematic has been sent to production.

*

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