```
//START: Doing AFE Config


//Device Initialization for ChipVersion: 1.3


//**********System Parameters**********


//System Parameters:
//    FRef  =     368.64
//    FadcFb      =     2949.12
//    FadcRx      =     2949.12
//    Fdac  =     5898.24
//    LMFSHdFb    =     ['14810', '14810']
//    LMFSHdRx    =     ['181610', '181610', '181610', '181610']
//    LMFSHdTx    =     ['14810', '14810', '14810', '14810']
//    RRFMode     =     0
//    adcDataMuxEn      =     0
//    adcSelect0 =     [0, 1, 2]
//    adcSelect1 =     [0, 1, 2]
//    auxAdcEn    =     False
//    broadcastRxNcoSel     =     0
//    broadcastTxNcoSel     =     0
//    chipId      =     1
//    chipType    =     0
//    chipVersion       =     19
//    combineDucMode    =     [0, 0]
//    continuousSysref=     False
//    dacDataMuxEn      =     0
//    ddcFactorFb       =     [12, 12]
//    ddcFactorRx       =     [24, 24, 24, 24]
//    defaultFbDsa      =     [12, 12]
//    defaultRxDsa      =     [0, 0, 0, 0]
//    defaultTxDsa      =     [0, 0, 0, 0]
//    ducFactorTx       =     [24, 24, 24, 24]
//    enableDacInterleavedMode    =     False
//    enableReliabilityDetector   =     True
//    enableRxDsaCalibration      =     False
//    enableTxDsaCalibration      =     False
//    enableTxFbLoopbackLowLatencyMode =     [False, False]
//    executeLinkUpSequenceSeparately  =     True
//    externalClockRx =     False
//    externalClockTx =     False
//    fbChainSelForDsaCalib =     0
//    fbDataMux   =     [0, 1]
//    fbDsaPerTx =     [0, 0, 0, 0]
//    fbDsaPerTxEn      =     False
//    fbEnable    =     [False, True]
//    fbJesdTxK   =     [1, 1]
//    fbJesdTxScr       =     [False, False]
```

```
//    fbJesdTxSyncMux =     [0, 0]
//    fbNco0     =     [2139.84, 2139.84]
//    fbNco1     =     [2139.84, 2139.84]
//    fbNco2     =     [2139.84, 2139.84]
//    fbNco3     =     [2139.84, 2139.84]
//    gpioMapping = {       'K14' :'FBABTDD',
//                'R15' :['RXCTDD', 'RXDTDD'],
//                'P14' :'GLOBAL_PDN',
//                'V5'  :['TXCTDD', 'TXDTDD'],
//                'E7'  :['RXATDD', 'RXBTDD'],
//                'C6'  :'FB_NCOSEL_2',
//                'R6'  :'FBCDTDD',
//                'T6'  :'RXC_LNABYPASS_B0',
//                'H11' :'INTBIPI_SPIB1_SDI',
//                'H12' :['TXA_GSW', 'TXB_GSW', 'TXC_GSW',
'TXD_GSW', 'TX_NCOSEL_0'],
//                'T5'  :'RXD_LNABYPASS_B0',
//                'H15' :['TXATDD', 'TXBTDD'],
//                'H16' :'SPIB1_CSN',
//                'G16' :'SPIB1_CLK',
//                'G13' :['RXA_GSW', 'RX_NCOSEL_0'],
//                'G12' :'SPIB1_SDO',
//                'G10' :'RXB_LNABYPASS_B0',
//                'N13' :'RXB_GSW',
//                'H8'  :'ADC_SYNC0',
//                'H9'  :'DAC_SYNC0',
//                'N16' :'ALARM1',
//                'F6'  :'FB_NCOSEL_3',
//                'N15' :'ALARM2',
//                'D5'  :'RXA_LNABYPASS_B0',
//                }
//    gpioOverrideValSet    =     []
//    gpioPolarityInv =     []
//    halfRateModeFb  =     [False, False]
//    halfRateModeRx  =     [False, False]
//    halfRateModeTx  =     [False, False]
//    intPinsParams[0] = {       'SPI' :False,
//                'TXBPAP'   :True,
//                'TXCPAP'   :True,
//                'JESD'     :True,
//                'TXAPAP'   :True,
//                'PLL' :True,
//                'TXDPAP'   :True,
//                }
//
//    intPinsParams[1] = {       'SPI' :True,
//                'TXBPAP'   :False,
//                'TXCPAP'   :False,
//                'JESD'     :False,
//                'TXAPAP'   :False,
//                'PLL' :False,
//                'TXDPAP'   :False,
```

```
//              }
//
//    jesdABLvdsSync  =     False
//    jesdCDLvdsSync  =     False
//    jesdLoopbackEn  =     0
//    jesdRxK    =     [1, 1, 1, 1]
//    jesdRxLaneMux   =     [2, 1, 0, 4, 3, 5, 6, 7]
//    jesdRxProtocol  =     [2, 2]
//    jesdRxRbd  =     [4, 4]
//    jesdRxScr  =     [False, False, False, False]
//    jesdRxSyncMux   =     [0, 0, 0, 0]
//    jesdSendZeroesInTddOff      =     True
//    jesdSystemMode  =     [1, 1]
//    jesdTxIlaL =     [4, 4, 2, 4, 4, 2]
//    jesdTxIlaLid    =     [0, 1, 2, 3, 4, 5, 6, 7]
//    jesdTxIlaM =     [8, 8, 2, 8, 8, 2]
//    jesdTxLaneMux   =     [3, 1, 2, 0, 4, 5, 6, 7]
//    jesdTxProtocol  =     [2, 2]
//    libVersion =     '1.9'
//    modeTdd    =     0
//    ncoFbMode  =     1
//    ncoFreqMode     =     'FCW'
//    ncoRxMode  =     [5, 5]
//    ncoTxMode  =     [1, 1]
//    numBandsRx =     [0, 0, 0, 0]
//    numBandsTx =     [0, 0, 0, 0]
//    numFbNCO   =     4
//    numRxNCO   =     2
//    numRxNCOB0 =     [1, 1, 1, 1]
//    numRxNCOB1 =     [1, 1, 1, 1]
//    numTxNCO   =     2
//    numTxNCOB0 =     [1, 1, 1, 1]
//    numTxNCOB1 =     [1, 1, 1, 1]
//    papParams[0] = {      'hpfWindowCntr' :0,
//                'triggerToRampDown'   :50,
//                'triggerClearToRampUp'      :50,
//                'hpfNumSample'   :4,
//                'rampDownStartVal'    :128,
//                'enable'   :False,
//                'maNumSample'    :128,
//                'alarmPinDynamicMode' :1,
//                'waitCounter'    :200,
//                'maWindowCntrTh':1,
//                'alarmMask'      :64,
//                'detectInWaitState'   :0,
//                'maThreshB0'     :90.0,
//                'maThreshB1'     :90.0,
//                'hpfWindowCntrTh'     :0,
//                'hpfEnable'      :1,
//                'amplUpdateCycles'    :2,
//                'alarmChannelMask'    :14,
//                'maWindowCntr'   :1,
```

```
//              'rampStickyMode':0,
//              'gainStepSize'  :5,
//              'multMode' :0,
//              'alarmPulseGPIO':1000,
//              'hpfThreshComb' :30.0,
//              'maEnable' :1,
//              'attnStepSize'  :5,
//              'maThreshComb'  :90.0,
//              'hpfThreshB1'   :30.0,
//              'hpfThreshB0'   :30.0,
//              }
//
//   papParams[1] = {      'hpfWindowCntr' :0,
//              'triggerToRampDown'   :50,
//              'triggerClearToRampUp'      :50,
//              'hpfNumSample'  :4,
//              'rampDownStartVal'    :128,
//              'enable'   :False,
//              'maNumSample'   :128,
//              'alarmPinDynamicMode' :1,
//              'waitCounter'   :200,
//              'maWindowCntrTh':1,
//              'alarmMask'     :64,
//              'detectInWaitState'   :0,
//              'maThreshB0'    :90.0,
//              'maThreshB1'    :90.0,
//              'hpfWindowCntrTh'     :0,
//              'hpfEnable'     :1,
//              'amplUpdateCycles'    :2,
//              'alarmChannelMask'    :14,
//              'maWindowCntr'  :1,
//              'rampStickyMode':0,
//              'gainStepSize'  :5,
//              'multMode' :0,
//              'alarmPulseGPIO':1000,
//              'hpfThreshComb' :30.0,
//              'maEnable' :1,
//              'attnStepSize'  :5,
//              'maThreshComb'  :90.0,
//              'hpfThreshB1'   :30.0,
//              'hpfThreshB0'   :30.0,
//              }
//
//   papParams[2] = {      'hpfWindowCntr' :0,
//              'triggerToRampDown'   :50,
//              'triggerClearToRampUp'      :50,
//              'hpfNumSample'  :4,
//              'rampDownStartVal'    :128,
//              'enable'   :False,
//              'maNumSample'   :128,
//              'alarmPinDynamicMode' :1,
//              'waitCounter'   :200,
```

```
//                'maWindowCntrTh':1,
//                'alarmMask'     :64,
//                'detectInWaitState'   :0,
//                'maThreshB0'    :90.0,
//                'maThreshB1'    :90.0,
//                'hpfWindowCntrTh'     :0,
//                'hpfEnable'     :1,
//                'amplUpdateCycles'    :2,
//                'alarmChannelMask'    :14,
//                'maWindowCntr'  :1,
//                'rampStickyMode':0,
//                'gainStepSize'  :5,
//                'multMode' :0,
//                'alarmPulseGPIO':1000,
//                'hpfThreshComb' :30.0,
//                'maEnable' :1,
//                'attnStepSize'  :5,
//                'maThreshComb'  :90.0,
//                'hpfThreshB1'   :30.0,
//                'hpfThreshB0'   :30.0,
//                }
//
//    papParams[3] = {      'hpfWindowCntr' :0,
//                'triggerToRampDown'   :50,
//                'triggerClearToRampUp'      :50,
//                'hpfNumSample'  :4,
//                'rampDownStartVal'    :128,
//                'enable'   :False,
//                'maNumSample'   :128,
//                'alarmPinDynamicMode' :1,
//                'waitCounter'   :200,
//                'maWindowCntrTh':1,
//                'alarmMask'     :64,
//                'detectInWaitState'   :0,
//                'maThreshB0'    :90.0,
//                'maThreshB1'    :90.0,
//                'hpfWindowCntrTh'     :0,
//                'hpfEnable'     :1,
//                'amplUpdateCycles'    :2,
//                'alarmChannelMask'    :14,
//                'maWindowCntr'  :1,
//                'rampStickyMode':0,
//                'gainStepSize'  :5,
//                'multMode' :0,
//                'alarmPulseGPIO':1000,
//                'hpfThreshComb' :30.0,
//                'maEnable' :1,
//                'attnStepSize'  :5,
//                'maThreshComb'  :90.0,
//                'hpfThreshB1'   :30.0,
//                'hpfThreshB0'   :30.0,
//                }
```

```
//
//    pllGsmMode =     False
//    reliabilityDetectorDecayMode     =     1
//    rxChainSelForDsaCalib =     15
//    rxDataMux  =     [0, 1, 2, 3, 4, 5, 6, 7]
//    rxDsaBandCalibMode    =     0
//    rxDsaCalibMode  =     0
//    rxDsaGainRange  =     [0, 25]
//    rxEnable   =     [True, True, True, True]
//    rxJesdTxK  =     [1, 1, 1, 1]
//    rxJesdTxScr     =     [False, False, False, False]
//    rxJesdTxSyncMux =     [0, 0, 0, 0]
//    rxNco0     =     [[1949.84, 2600], [1949.84, 2600],
[1949.84, 2600], [1949.84, 2600]]
//    rxNco1     =     [[2139.84, 2600], [2139.84, 2600],
[2139.84, 2600], [2139.84, 2600]]
//    serdesFirmware  =     True
//    serdesManualCTLE =     [6, 6, 6, 6, 6, 6, 6, 6]
//    serdesManualCTLEEn    =     False
//    serdesRxLanePolarity  =     [False, False, False, False,
False, False, False, False]
//    serdesTxLanePolarity  =     [False, False, False, False,
False, False, False, False]
//    serdesTxMainCursor    =     [3, 0, 0, 0, 0, 0, 0, 3]
//    serdesTxPostCursor    =     [0, 0, 0, 0, 0, 0, 0, 0]
//    serdesTxPreCursor     =     [0, 0, 0, 0, 0, 0, 0, 0]
//    setIlaParams    =     True
//    spiMode    =     1
//    syncLoopBack    =     False
//    sysrefTermination     =     0
//    txDataMux  =     [0, 1, 2, 3, 4, 5, 6, 7]
//    txDsaBandCalibMode    =     0
//    txDsaCalibMode  =     0
//    txEnable   =     [True, True, True, True]
//    txNco0     =     [[2139.84, 2600], [2139.84, 2600],
[2139.84, 2600], [2139.84, 2600]]
//    txNco1     =     [[1949.84, 2600], [1949.84, 2600],
[1949.84, 2600], [1949.84, 2600]]
//    txToFbMode =     0
//    txdsaStartStop  =     [0, 29]
//    useLcmClkForSysrefLatch    =     True
//    useSpiSysref    =     False
//    useTxForCalib   =     0
//


//**********Configuration Starting**********
//


//EXTERNAL-ACTION: Toggle Hardware Reset
```

```
//STEP: rstDevice/step0

//START: Device Soft Reset and SPI Check

SPIWrite 0000,30,0,7  //global_soft_reset=0x0;
     Address(0x0[7:7])
SPIWrite 0000,b0,0,7  //global_soft_reset=0x1;
     Address(0x0[7:7])
SPIWrite 0000,30,0,7  //global_soft_reset=0x0;
     Address(0x0[7:7])
SPIWrite 0000,30,0,7  //global_4pin=0x1;    Address(0x0[7:4])
SPIWrite 0000,30,0,7  //global_ascend=0x1;  Address(0x0[7:5])
SPIReadCheck 0003,0,7,0a

//Read     chip_type=0xa;  Address(0x3[7:0],0x4[7:0])

SPIReadCheck 0004,0,7,78
SPIReadCheck 0005,0,7,00

//Read     chip_id=0x78;
     Address(0x4[7:0],0x5[7:0],0x5[7:0],0x6[7:0])

SPIReadCheck 0006,0,7,11

//Read     chip_ver=0x11;  Address(0x6[7:0],0x7[7:0])

SPIRead 0007,0,7
SPIRead 0008,0,7

//Read     vendor_id=0x451;
     Address(0x7[7:0],0x8[7:0],0x8[7:0],0x9[7:0])


//END: Device Soft Reset and SPI Check


//STEP: rstDevice/step1

//START: Waking up device

SPIWrite 0015,80,0,7  //timing_controller=0x1;
     Address(0x15[7:7])
SPIWrite 0191,00,0,7  //Property_170h_8_8=0x0;
     Address(0x191[7:0])
SPIWrite 0231,00,0,7  //Property_210h_8_8=0x0;
     Address(0x231[7:0])
SPIWrite 02d1,00,0,7  //Property_2b0h_8_8=0x0;
     Address(0x2d1[7:0])
SPIWrite 0371,00,0,7  //Property_350h_8_8=0x0;
     Address(0x371[7:0])
SPIWrite 042a,00,0,7  //Property_408h_16_16=0x0;
```

```
     Address(0x42a[7:0])
SPIWrite 04e2,00,0,7  //Property_4c0h_16_16=0x0;
     Address(0x4e2[7:0])
SPIWrite 059a,00,0,7  //Property_578h_16_16=0x0;
     Address(0x59a[7:0])
SPIWrite 0652,00,0,7  //Property_630h_16_16=0x0;
     Address(0x652[7:0])
SPIWrite 070a,00,0,7  //Property_6e8h_16_16=0x0;
     Address(0x70a[7:0])
SPIWrite 07c2,00,0,7  //Property_7a0h_16_16=0x0;
     Address(0x7c2[7:0])

//START: Setting TDD Pin in override state and setting override
values.

SPIWrite 00ec,01,0,7  //Property_cch_0_0=0x1;
     Address(0xec[7:0])
SPIWrite 00f4,01,0,7  //Property_d4h_0_0=0x1;
     Address(0xf4[7:0])
SPIWrite 00e4,01,0,7  //Property_c4h_0_0=0x1;
     Address(0xe4[7:0])
SPIWrite 00ed,00,0,7  //Property_cch_11_8=0x0;
     Address(0xed[7:0])
SPIWrite 00f5,00,0,7  //Property_d4h_9_8=0x0;
     Address(0xf5[7:0])
SPIWrite 00e5,00,0,7  //Property_c4h_11_8=0x0;
     Address(0xe5[7:0])

//END: Setting TDD Pin in override state and setting override
values.

SPIWrite 0015,00,0,7  //timing_controller=0x0;
     Address(0x15[7:7])
SPIWrite 0015,40,0,7  //digtop=0x1;    Address(0x15[7:6])
SPIWrite 0190,03,0,7  //misc_spi_global_pdn_ctrl=0x1;
     Address(0x190[7:0])
SPIWrite 0190,01,0,7  //misc_spi_global_pdn_sig=0x0;
     Address(0x190[7:1])
SPIWrite 0015,00,0,7  //digtop=0x0;    Address(0x15[7:6])

WAIT 0.005

//END: Done waking up device


//START: Changing termination to 100 ohm


//START: Requesting/releasing SPI Access to PLL Pages

SPIWrite 0015,40,0,7  //digtop=0x1;    Address(0x15[7:6])
SPIWrite 0170,01,0,7  //pll_reg_spi_req_a=0x1;
```

```
     Address(0x170[7:0])
SPIWrite 0540,00,0,7  //Property_520h_0_0=0x0;
     Address(0x540[7:0])

SPIPoll 0171,0,0,01
SPIRead 0171,0,0

//Read     pll_reg_spi_a_ack=0x1(Meaning: );;
     Address(0x171[7:0])


//END: Requesting/releasing SPI Access to PLL Pages

SPIWrite 0015,00,0,7  //digtop=0x0;    Address(0x15[7:6])
SPIWrite 0015,01,0,7  //pll=0x1;       Address(0x15[7:0])
SPIWrite 0054,81,0,7
SPIWrite 0015,00,0,7  //pll=0x0;       Address(0x15[7:0])

//START: Requesting/releasing SPI Access to PLL Pages

SPIWrite 0015,40,0,7  //digtop=0x1;    Address(0x15[7:6])
SPIWrite 0170,00,0,7  //pll_reg_spi_req_a=0x0;
     Address(0x170[7:0])
SPIWrite 0540,00,0,7  //Property_520h_0_0=0x0;
     Address(0x540[7:0])

WAIT 0.2

//END: Requesting/releasing SPI Access to PLL Pages


//END: Changing termination to 100 ohm


//START: Setting MCU Clock Div

SPIWrite 0015,00,0,7  //digtop=0x0;    Address(0x15[7:6])
SPIWrite 0015,02,0,7  //ana_4t4r=0x1;  Address(0x15[7:1])
SPIWrite 00c0,00,0,7  //Property_a0h_2_0=0x0;
     Address(0xc0[7:0])

//END: Setting MCU Clock Div

SPIWrite 0015,00,0,7  //ana_4t4r=0x0;  Address(0x15[7:1])

//STEP: efuseChain/step0

//START: Loading Efuse Chain

SPIWrite 0015,40,0,7  //digtop=0x1;    Address(0x15[7:6])
SPIWrite 08a8,02,0,7  //Property_888h_7_0=0x2;
     Address(0x8a8[7:0],0x8a9[7:0])
```

```
SPIWrite 0810,01,0,7  //Property_7f0h_0_0=0x1;
      Address(0x810[7:0])
SPIWrite 0830,01,0,7  //Property_810h_0_0=0x1;
      Address(0x830[7:0])
SPIWrite 0200,00,0,7  //Property_1e0h_2_0=0x0;
      Address(0x200[7:0])
SPIWrite 0210,00,0,7  //Property_1f0h_2_0=0x0;
      Address(0x210[7:0])
SPIWrite 0814,00,0,7  //Property_7f4h_1_0=0x0;
      Address(0x814[7:0])
SPIWrite 0834,00,0,7  //Property_814h_1_0=0x0;
      Address(0x834[7:0])
SPIWrite 0814,01,0,7  //Property_7f4h_1_0=0x1;
      Address(0x814[7:0])
SPIWrite 0834,01,0,7  //Property_814h_1_0=0x1;
      Address(0x834[7:0])
SPIWrite 0810,00,0,7  //Property_7f0h_0_0=0x0;
      Address(0x810[7:0])
SPIWrite 0830,00,0,7  //Property_810h_0_0=0x0;
      Address(0x830[7:0])
SPIWrite 0810,01,0,7  //Property_7f0h_0_0=0x1;
      Address(0x810[7:0])
SPIWrite 0830,01,0,7  //Property_810h_0_0=0x1;
      Address(0x830[7:0])
SPIWrite 0200,04,0,7  //Property_1e0h_2_0=0x4;
      Address(0x200[7:0])
SPIWrite 0210,00,0,7  //Property_1f0h_2_0=0x0;
      Address(0x210[7:0])
SPIWrite 0814,03,0,7  //Property_7f4h_1_0=0x3;
      Address(0x814[7:0])
SPIWrite 0834,03,0,7  //Property_814h_1_0=0x3;
      Address(0x834[7:0])
SPIWrite 0814,00,0,7  //Property_7f4h_1_0=0x0;
      Address(0x814[7:0])
SPIWrite 0834,00,0,7  //Property_814h_1_0=0x0;
      Address(0x834[7:0])
SPIWrite 0810,00,0,7  //Property_7f0h_0_0=0x0;
      Address(0x810[7:0])
SPIWrite 0830,00,0,7  //Property_810h_0_0=0x0;
      Address(0x830[7:0])
SPIWrite 0814,00,0,7  //Property_7f4h_5_2=0x0;
      Address(0x814[7:2])
SPIWrite 0834,00,0,7  //Property_814h_5_2=0x0;
      Address(0x834[7:2])
SPIWrite 0814,1c,0,7  //Property_7f4h_5_2=0x7;
      Address(0x814[7:2])
SPIWrite 0834,1c,0,7  //Property_814h_5_2=0x7;
      Address(0x834[7:2])
SPIWrite 0814,00,0,7  //Property_7f4h_5_2=0x0;
      Address(0x814[7:2])
SPIWrite 0834,00,0,7  //Property_814h_5_2=0x0;
      Address(0x834[7:2])
```

```
WAIT 0.05

//END: Loading Efuse Chain


//START: Checking for Efuse

SPIReadCheck 0150,0,3,0f

//Read     obs_func_spi_chain_autoload_done=0xf;
      Address(0x150[7:0])

SPIReadCheck 0150,4,7,00

//Read     obs_func_spi_chain_autoload_error=0x0;
      Address(0x150[7:4])


//END: Checking for Efuse


//START: enabling Efuse Clock

SPIWrite 0830,01,0,7  //Property_810h_0_0=0x1;
      Address(0x830[7:0])
SPIWrite 0810,01,0,7  //Property_7f0h_0_0=0x1;
      Address(0x810[7:0])
SPIWrite 0910,0f,0,7  //Property_8f0h_3_0=0xf;
      Address(0x910[7:0])
SPIWrite 0911,03,0,7  //Property_8f0h_9_8=0x3;
      Address(0x911[7:0])
SPIWrite 0912,0f,0,7  //Property_8f0h_19_16=0xf;
      Address(0x912[7:0])

//END: enabling Efuse Clock

SPIWrite 0015,00,0,7  //digtop=0x0;    Address(0x15[7:6])

//STEP: mcuWakeUp/step0
SPIWrite 0018,20,0,7  //macro=0x1;     Address(0x18[7:5])
SPIWrite 0140,01,0,7  //Property_120h_0_0=0x1;
      Address(0x140[7:0])
SPIWrite 0140,00,0,7  //Property_120h_0_0=0x0;
      Address(0x140[7:0])

WAIT 0.001
SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])
```

```
SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0x2;
     Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00,0,7
SPIWrite 00a1,00,0,7
SPIWrite 00a0,02,0,7
SPIWrite 0193,01,0,7  //MACRO_OPCODE=0x1;
     Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
     Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
     Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
     Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
```

```
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00fb,0,7
SPIRead 00fa,0,7
SPIRead 00f9,0,7
SPIRead 00f8,0,7

//Read     MACRO_RESULT_REG0=0x13070a01;
      Address(0xf8[7:0],0xf9[7:0],0xfa[7:0],0xfb[7:0],0xfc[7:0])

SPIReadCheck 00ff,0,7,00
SPIReadCheck 00fe,0,7,00
SPIReadCheck 00fd,0,7,2a
SPIReadCheck 00fc,0,7,f8

//Read     MACRO_RESULT_REG1=0x2af8;
      Address(0xfc[7:0],0xfd[7:0],0xfe[7:0],0xff[7:0],0x100[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0x0;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00,0,7
SPIWrite 00a1,00,0,7
SPIWrite 00a0,00,0,7
SPIWrite 0193,90,0,7  //MACRO_OPCODE=0x90;
      Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
```

```
      Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0; Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
      Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIWrite 0144,08,0,7  //Property_124h_4_2=0x2;
      Address(0x144[7:2])
SPIWrite 0018,00,0,7  //macro=0x0;     Address(0x18[7:5])
SPIWrite 0018,08,0,7  //Property_18h_3_3=0x1;
      Address(0x18[7:3])
SPIWrite 03bf,00,0,7
SPIWrite 03be,05,0,7
SPIWrite 03bd,a0,0,7
SPIWrite 03bc,00,0,7
SPIWrite 03c3,00,0,7
SPIWrite 03c2,04,0,7
SPIWrite 03c1,17,0,7
SPIWrite 03c0,46,0,7
SPIWrite 03d0,05,0,7
SPIWrite 03ac,1d,0,7
SPIWrite 03ad,1d,0,7
SPIWrite 1402,00,0,7
SPIWrite 1403,00,0,7
SPIWrite 1401,00,0,7
```

```
SPIWrite 0018,00,0,7  //Property_18h_3_3=0x0;
     Address(0x18[7:3])
SPIWrite 0018,20,0,7  //macro=0x1;    Address(0x18[7:5])
SPIWrite 0144,08,0,7  //Property_124h_4_2=0x2;
     Address(0x144[7:2])
SPIWrite 0018,00,0,7  //macro=0x0;    Address(0x18[7:5])
SPIWrite 0018,08,0,7  //Property_18h_3_3=0x1;
     Address(0x18[7:3])
SPIWrite 1ee8,00,0,7
SPIWrite 1ee9,00,0,7
SPIWrite 0018,00,0,7  //Property_18h_3_3=0x0;
     Address(0x18[7:3])
SPIWrite 0018,20,0,7  //macro=0x1;    Address(0x18[7:5])
SPIWrite 0144,08,0,7  //Property_124h_4_2=0x2;
     Address(0x144[7:2])
SPIWrite 0018,00,0,7  //macro=0x0;    Address(0x18[7:5])
SPIWrite 0018,08,0,7  //Property_18h_3_3=0x1;
     Address(0x18[7:3])
SPIWrite 1b5f,22,0,7
SPIWrite 0018,00,0,7  //Property_18h_3_3=0x0;
     Address(0x18[7:3])
SPIWrite 0018,20,0,7  //macro=0x1;    Address(0x18[7:5])
SPIWrite 0144,08,0,7  //Property_124h_4_2=0x2;
     Address(0x144[7:2])
SPIWrite 0018,00,0,7  //macro=0x0;    Address(0x18[7:5])
SPIWrite 0018,08,0,7  //Property_18h_3_3=0x1;
     Address(0x18[7:3])
SPIWrite 1b6f,07,0,7
SPIWrite 0018,00,0,7  //Property_18h_3_3=0x0;
     Address(0x18[7:3])
SPIWrite 0018,20,0,7  //macro=0x1;    Address(0x18[7:5])
SPIWrite 0144,08,0,7  //Property_124h_4_2=0x2;
     Address(0x144[7:2])
SPIWrite 0018,00,0,7  //macro=0x0;    Address(0x18[7:5])
SPIWrite 0018,08,0,7  //Property_18h_3_3=0x1;
     Address(0x18[7:3])
SPIWrite 1e7d,08,0,7
SPIWrite 0018,00,0,7  //Property_18h_3_3=0x0;
     Address(0x18[7:3])
SPIWrite 0018,20,0,7  //macro=0x1;    Address(0x18[7:5])
SPIWrite 0144,08,0,7  //Property_124h_4_2=0x2;
     Address(0x144[7:2])
SPIWrite 0018,00,0,7  //macro=0x0;    Address(0x18[7:5])
SPIWrite 0018,08,0,7  //Property_18h_3_3=0x1;
     Address(0x18[7:3])
SPIWrite 1a74,f0,0,7
SPIWrite 1a75,01,0,7
SPIWrite 0018,00,0,7  //Property_18h_3_3=0x0;
     Address(0x18[7:3])
SPIWrite 0018,20,0,7  //macro=0x1;    Address(0x18[7:5])
SPIWrite 0144,08,0,7  //Property_124h_4_2=0x2;
     Address(0x144[7:2])
```

```
SPIWrite 0018,00,0,7  //macro=0x0;     Address(0x18[7:5])
SPIWrite 0018,08,0,7  //Property_18h_3_3=0x1;
     Address(0x18[7:3])
SPIWrite 1b24,80,0,7
SPIWrite 1b25,01,0,7
SPIWrite 0018,00,0,7  //Property_18h_3_3=0x0;
     Address(0x18[7:3])
SPIWrite 0018,20,0,7  //macro=0x1;     Address(0x18[7:5])
SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0x1;
     Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00,0,7
SPIWrite 00a1,00,0,7
SPIWrite 00a0,01,0,7
SPIWrite 0193,90,0,7  //MACRO_OPCODE=0x90;
     Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
     Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
     Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])
```

```
SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIWrite 0018,00,0,7  //macro=0x0;     Address(0x18[7:5])

//STEP: mcuWakeUp/step1
SPIWrite 0018,20,0,7  //macro=0x1;     Address(0x18[7:5])
SPIWrite 0144,00,0,7  //Property_124h_4_2=0x0;
      Address(0x144[7:2])
SPIWrite 0018,00,0,7  //macro=0x0;     Address(0x18[7:5])
SPIWrite 0018,01,0,7  //Property_18h_0_0=0x1;
      Address(0x18[7:0])
SPIWrite 0020,00,0,7
SPIWrite 0021,00,0,7
SPIWrite 0022,00,0,7
SPIWrite 0023,00,0,7
SPIWrite 0024,59,0,7
SPIWrite 0025,14,0,7
SPIWrite 0026,03,0,7
SPIWrite 0027,00,0,7
SPIWrite 0028,b5,0,7
SPIWrite 0029,a4,0,7
SPIWrite 002a,6d,0,7
SPIWrite 002b,ea,0,7
SPIWrite 002c,7d,0,7
SPIWrite 002d,19,0,7
SPIWrite 002e,ce,0,7
SPIWrite 002f,ca,0,7
SPIWrite 0030,01,0,7
SPIWrite 0031,07,0,7
SPIWrite 0032,08,0,7
SPIWrite 0033,12,0,7
SPIWrite 0034,14,0,7
SPIWrite 0035,00,0,7
SPIWrite 0036,01,0,7
SPIWrite 0037,0a,0,7
```

```
SPIWrite 0038,07,0,7
SPIWrite 0039,13,0,7
SPIWrite 003a,f8,0,7
SPIWrite 003b,2a,0,7
SPIWrite 003c,01,0,7
SPIWrite 003d,0a,0,7
SPIWrite 003e,07,0,7
SPIWrite 003f,13,0,7
SPIWrite 0040,f8,0,7
SPIWrite 0041,2a,0,7
SPIWrite 0042,00,0,7
SPIWrite 0043,00,0,7
SPIWrite 0044,00,0,7
SPIWrite 0045,00,0,7
SPIWrite 0046,00,0,7
SPIWrite 0047,00,0,7
SPIWrite 0048,00,0,7
SPIWrite 0049,00,0,7
SPIWrite 004a,00,0,7
SPIWrite 004b,00,0,7
SPIWrite 004c,00,0,7
SPIWrite 004d,00,0,7
SPIWrite 004e,00,0,7
SPIWrite 004f,00,0,7
SPIWrite 0050,c7,0,7
SPIWrite 0051,4a,0,7
SPIWrite 0052,0c,0,7
SPIWrite 0053,23,0,7
SPIWrite 0054,10,0,7
SPIWrite 0055,fb,0,7
SPIWrite 0056,03,0,7
SPIWrite 0057,f0,0,7
SPIWrite 0058,00,0,7
SPIWrite 0059,eb,0,7
SPIWrite 005a,81,0,7
SPIWrite 005b,00,0,7
SPIWrite 005c,10,0,7
SPIWrite 005d,58,0,7
SPIWrite 005e,90,0,7
SPIWrite 005f,f8,0,7
SPIWrite 0060,b8,0,7
SPIWrite 0061,14,0,7
SPIWrite 0062,00,0,7
SPIWrite 0063,eb,0,7
SPIWrite 0064,41,0,7
SPIWrite 0065,00,0,7
SPIWrite 0066,b0,0,7
SPIWrite 0067,f8,0,7
SPIWrite 0068,bc,0,7
SPIWrite 0069,04,0,7
SPIWrite 006a,70,0,7
SPIWrite 006b,47,0,7
```

```
SPIWrite 006c,ac,0,7
SPIWrite 006d,4a,0,7
SPIWrite 006e,03,0,7
SPIWrite 006f,78,0,7
SPIWrite 0070,11,0,7
SPIWrite 0071,68,0,7
SPIWrite 0072,4b,0,7
SPIWrite 0073,40,0,7
SPIWrite 0074,03,0,7
SPIWrite 0075,f0,0,7
SPIWrite 0076,07,0,7
SPIWrite 0077,03,0,7
SPIWrite 0078,59,0,7
SPIWrite 0079,40,0,7
SPIWrite 007a,11,0,7
SPIWrite 007b,60,0,7
SPIWrite 007c,40,0,7
SPIWrite 007d,78,0,7
SPIWrite 007e,a2,0,7
SPIWrite 007f,f1,0,7
SPIWrite 0080,00,0,7
SPIWrite 0081,42,0,7
SPIWrite 0082,11,0,7
SPIWrite 0083,68,0,7
SPIWrite 0084,48,0,7
SPIWrite 0085,40,0,7
SPIWrite 0086,00,0,7
SPIWrite 0087,f0,0,7
SPIWrite 0088,07,0,7
SPIWrite 0089,00,0,7
SPIWrite 008a,48,0,7
SPIWrite 008b,40,0,7
SPIWrite 008c,10,0,7
SPIWrite 008d,60,0,7
SPIWrite 008e,70,0,7
SPIWrite 008f,47,0,7
SPIWrite 0090,38,0,7
SPIWrite 0091,b5,0,7
SPIWrite 0092,b7,0,7
SPIWrite 0093,4c,0,7
SPIWrite 0094,13,0,7
SPIWrite 0095,78,0,7
SPIWrite 0096,0c,0,7
SPIWrite 0097,25,0,7
SPIWrite 0098,10,0,7
SPIWrite 0099,fb,0,7
SPIWrite 009a,05,0,7
SPIWrite 009b,f0,0,7
SPIWrite 009c,00,0,7
SPIWrite 009d,eb,0,7
SPIWrite 009e,81,0,7
SPIWrite 009f,00,0,7
```

```
SPIWrite 00a0,20,0,7
SPIWrite 00a1,58,0,7
SPIWrite 00a2,80,0,7
SPIWrite 00a3,f8,0,7
SPIWrite 00a4,aa,0,7
SPIWrite 00a5,34,0,7
SPIWrite 00a6,51,0,7
SPIWrite 00a7,78,0,7
SPIWrite 00a8,d0,0,7
SPIWrite 00a9,f8,0,7
SPIWrite 00aa,14,0,7
SPIWrite 00ab,2b,0,7
SPIWrite 00ac,61,0,7
SPIWrite 00ad,f3,0,7
SPIWrite 00ae,8b,0,7
SPIWrite 00af,22,0,7
SPIWrite 00b0,c0,0,7
SPIWrite 00b1,f8,0,7
SPIWrite 00b2,14,0,7
SPIWrite 00b3,2b,0,7
SPIWrite 00b4,38,0,7
SPIWrite 00b5,bd,0,7
SPIWrite 00b6,f8,0,7
SPIWrite 00b7,b5,0,7
SPIWrite 00b8,ad,0,7
SPIWrite 00b9,4c,0,7
SPIWrite 00ba,ae,0,7
SPIWrite 00bb,4b,0,7
SPIWrite 00bc,0c,0,7
SPIWrite 00bd,25,0,7
SPIWrite 00be,4f,0,7
SPIWrite 00bf,f4,0,7
SPIWrite 00c0,25,0,7
SPIWrite 00c1,77,0,7
SPIWrite 00c2,dc,0,7
SPIWrite 00c3,26,0,7
SPIWrite 00c4,10,0,7
SPIWrite 00c5,fb,0,7
SPIWrite 00c6,05,0,7
SPIWrite 00c7,f5,0,7
SPIWrite 00c8,10,0,7
SPIWrite 00c9,fb,0,7
SPIWrite 00ca,07,0,7
SPIWrite 00cb,f7,0,7
SPIWrite 00cc,05,0,7
SPIWrite 00cd,eb,0,7
SPIWrite 00ce,81,0,7
SPIWrite 00cf,00,0,7
SPIWrite 00d0,11,0,7
SPIWrite 00d1,fb,0,7
SPIWrite 00d2,06,0,7
SPIWrite 00d3,71,0,7
```

```
SPIWrite 00d4,20,0,7
SPIWrite 00d5,58,0,7
SPIWrite 00d6,59,0,7
SPIWrite 00d7,5c,0,7
SPIWrite 00d8,0b,0,7
SPIWrite 00d9,09,0,7
SPIWrite 00da,24,0,7
SPIWrite 00db,bf,0,7
SPIWrite 00dc,13,0,7
SPIWrite 00dd,88,0,7
SPIWrite 00de,a0,0,7
SPIWrite 00df,f8,0,7
SPIWrite 00e0,38,0,7
SPIWrite 00e1,34,0,7
SPIWrite 00e2,cb,0,7
SPIWrite 00e3,08,0,7
SPIWrite 00e4,24,0,7
SPIWrite 00e5,bf,0,7
SPIWrite 00e6,53,0,7
SPIWrite 00e7,88,0,7
SPIWrite 00e8,a0,0,7
SPIWrite 00e9,f8,0,7
SPIWrite 00ea,34,0,7
SPIWrite 00eb,34,0,7
SPIWrite 00ec,89,0,7
SPIWrite 00ed,09,0,7
SPIWrite 00ee,24,0,7
SPIWrite 00ef,bf,0,7
SPIWrite 00f0,91,0,7
SPIWrite 00f1,88,0,7
SPIWrite 00f2,a0,0,7
SPIWrite 00f3,f8,0,7
SPIWrite 00f4,3e,0,7
SPIWrite 00f5,14,0,7
SPIWrite 00f6,91,0,7
SPIWrite 00f7,79,0,7
SPIWrite 00f8,80,0,7
SPIWrite 00f9,f8,0,7
SPIWrite 00fa,a0,0,7
SPIWrite 00fb,14,0,7
SPIWrite 00fc,f8,0,7
SPIWrite 00fd,bd,0,7
SPIWrite 00fe,2d,0,7
SPIWrite 00ff,e9,0,7
SPIWrite 0100,f0,0,7
SPIWrite 0101,47,0,7
SPIWrite 0102,08,0,7
SPIWrite 0103,af,0,7
SPIWrite 0104,3c,0,7
SPIWrite 0105,79,0,7
SPIWrite 0106,99,0,7
SPIWrite 0107,46,0,7
```

```
SPIWrite 0108,15,0,7
SPIWrite 0109,46,0,7
SPIWrite 010a,8a,0,7
SPIWrite 010b,46,0,7
SPIWrite 010c,06,0,7
SPIWrite 010d,46,0,7
SPIWrite 010e,8c,0,7
SPIWrite 010f,b9,0,7
SPIWrite 0110,36,0,7
SPIWrite 0111,01,0,7
SPIWrite 0112,30,0,7
SPIWrite 0113,46,0,7
SPIWrite 0114,eb,0,7
SPIWrite 0115,f7,0,7
SPIWrite 0116,99,0,7
SPIWrite 0117,fc,0,7
SPIWrite 0118,80,0,7
SPIWrite 0119,46,0,7
SPIWrite 011a,30,0,7
SPIWrite 011b,46,0,7
SPIWrite 011c,eb,0,7
SPIWrite 011d,f7,0,7
SPIWrite 011e,95,0,7
SPIWrite 011f,fc,0,7
SPIWrite 0120,08,0,7
SPIWrite 0121,eb,0,7
SPIWrite 0122,88,0,7
SPIWrite 0123,08,0,7
SPIWrite 0124,05,0,7
SPIWrite 0125,21,0,7
SPIWrite 0126,10,0,7
SPIWrite 0127,fb,0,7
SPIWrite 0128,01,0,7
SPIWrite 0129,f0,0,7
SPIWrite 012a,c0,0,7
SPIWrite 012b,f3,0,7
SPIWrite 012c,00,0,7
SPIWrite 012d,21,0,7
SPIWrite 012e,01,0,7
SPIWrite 012f,eb,0,7
SPIWrite 0130,68,0,7
SPIWrite 0131,21,0,7
SPIWrite 0132,0e,0,7
SPIWrite 0133,e0,0,7
SPIWrite 0134,eb,0,7
SPIWrite 0135,f7,0,7
SPIWrite 0136,89,0,7
SPIWrite 0137,fc,0,7
SPIWrite 0138,80,0,7
SPIWrite 0139,46,0,7
SPIWrite 013a,30,0,7
SPIWrite 013b,46,0,7
```

```
SPIWrite 013c,eb,0,7
SPIWrite 013d,f7,0,7
SPIWrite 013e,85,0,7
SPIWrite 013f,fc,0,7
SPIWrite 0140,08,0,7
SPIWrite 0141,eb,0,7
SPIWrite 0142,88,0,7
SPIWrite 0143,08,0,7
SPIWrite 0144,05,0,7
SPIWrite 0145,21,0,7
SPIWrite 0146,10,0,7
SPIWrite 0147,fb,0,7
SPIWrite 0148,01,0,7
SPIWrite 0149,f0,0,7
SPIWrite 014a,c0,0,7
SPIWrite 014b,f3,0,7
SPIWrite 014c,40,0,7
SPIWrite 014d,21,0,7
SPIWrite 014e,01,0,7
SPIWrite 014f,eb,0,7
SPIWrite 0150,a8,0,7
SPIWrite 0151,21,0,7
SPIWrite 0152,38,0,7
SPIWrite 0153,78,0,7
SPIWrite 0154,a5,0,7
SPIWrite 0155,eb,0,7
SPIWrite 0156,09,0,7
SPIWrite 0157,05,0,7
SPIWrite 0158,09,0,7
SPIWrite 0159,b2,0,7
SPIWrite 015a,40,0,7
SPIWrite 015b,19,0,7
SPIWrite 015c,a1,0,7
SPIWrite 015d,eb,0,7
SPIWrite 015e,00,0,7
SPIWrite 015f,10,0,7
SPIWrite 0160,a0,0,7
SPIWrite 0161,eb,0,7
SPIWrite 0162,0a,0,7
SPIWrite 0163,00,0,7
SPIWrite 0164,00,0,7
SPIWrite 0165,b2,0,7
SPIWrite 0166,41,0,7
SPIWrite 0167,42,0,7
SPIWrite 0168,c1,0,7
SPIWrite 0169,f3,0,7
SPIWrite 016a,80,0,7
SPIWrite 016b,00,0,7
SPIWrite 016c,00,0,7
SPIWrite 016d,eb,0,7
SPIWrite 016e,e1,0,7
SPIWrite 016f,00,0,7
```

```
SPIWrite 0170,80,0,7
SPIWrite 0171,b2,0,7
SPIWrite 0172,b0,0,7
SPIWrite 0173,f5,0,7
SPIWrite 0174,80,0,7
SPIWrite 0175,7f,0,7
SPIWrite 0176,a8,0,7
SPIWrite 0177,bf,0,7
SPIWrite 0178,ff,0,7
SPIWrite 0179,20,0,7
SPIWrite 017a,00,0,7
SPIWrite 017b,2c,0,7
SPIWrite 017c,19,0,7
SPIWrite 017d,bf,0,7
SPIWrite 017e,69,0,7
SPIWrite 017f,49,0,7
SPIWrite 0180,31,0,7
SPIWrite 0181,f8,0,7
SPIWrite 0182,10,0,7
SPIWrite 0183,00,0,7
SPIWrite 0184,c8,0,7
SPIWrite 0185,49,0,7
SPIWrite 0186,31,0,7
SPIWrite 0187,f8,0,7
SPIWrite 0188,10,0,7
SPIWrite 0189,00,0,7
SPIWrite 018a,bd,0,7
SPIWrite 018b,e8,0,7
SPIWrite 018c,f0,0,7
SPIWrite 018d,87,0,7
SPIWrite 018e,2d,0,7
SPIWrite 018f,e9,0,7
SPIWrite 0190,f0,0,7
SPIWrite 0191,4f,0,7
SPIWrite 0192,78,0,7
SPIWrite 0193,4c,0,7
SPIWrite 0194,4f,0,7
SPIWrite 0195,f4,0,7
SPIWrite 0196,25,0,7
SPIWrite 0197,7c,0,7
SPIWrite 0198,82,0,7
SPIWrite 0199,46,0,7
SPIWrite 019a,dc,0,7
SPIWrite 019b,26,0,7
SPIWrite 019c,89,0,7
SPIWrite 019d,46,0,7
SPIWrite 019e,1a,0,7
SPIWrite 019f,fb,0,7
SPIWrite 01a0,0c,0,7
SPIWrite 01a1,f0,0,7
SPIWrite 01a2,19,0,7
SPIWrite 01a3,fb,0,7
```

```
SPIWrite 01a4,06,0,7
SPIWrite 01a5,00,0,7
SPIWrite 01a6,25,0,7
SPIWrite 01a7,18,0,7
SPIWrite 01a8,28,0,7
SPIWrite 01a9,89,0,7
SPIWrite 01aa,ad,0,7
SPIWrite 01ab,f1,0,7
SPIWrite 01ac,24,0,7
SPIWrite 01ad,0d,0,7
SPIWrite 01ae,02,0,7
SPIWrite 01af,90,0,7
SPIWrite 01b0,e8,0,7
SPIWrite 01b1,88,0,7
SPIWrite 01b2,03,0,7
SPIWrite 01b3,90,0,7
SPIWrite 01b4,a8,0,7
SPIWrite 01b5,89,0,7
SPIWrite 01b6,04,0,7
SPIWrite 01b7,90,0,7
SPIWrite 01b8,95,0,7
SPIWrite 01b9,f8,0,7
SPIWrite 01ba,38,0,7
SPIWrite 01bb,00,0,7
SPIWrite 01bc,95,0,7
SPIWrite 01bd,f8,0,7
SPIWrite 01be,3d,0,7
SPIWrite 01bf,70,0,7
SPIWrite 01c0,05,0,7
SPIWrite 01c1,90,0,7
SPIWrite 01c2,50,0,7
SPIWrite 01c3,46,0,7
SPIWrite 01c4,ff,0,7
SPIWrite 01c5,f7,0,7
SPIWrite 01c6,44,0,7
SPIWrite 01c7,ff,0,7
SPIWrite 01c8,4f,0,7
SPIWrite 01c9,f0,0,7
SPIWrite 01ca,00,0,7
SPIWrite 01cb,08,0,7
SPIWrite 01cc,06,0,7
SPIWrite 01cd,21,0,7
SPIWrite 01ce,43,0,7
SPIWrite 01cf,46,0,7
SPIWrite 01d0,b6,0,7
SPIWrite 01d1,4a,0,7
SPIWrite 01d2,06,0,7
SPIWrite 01d3,90,0,7
SPIWrite 01d4,1a,0,7
SPIWrite 01d5,fb,0,7
SPIWrite 01d6,01,0,7
SPIWrite 01d7,f1,0,7
```

```
SPIWrite 01d8,cd,0,7
SPIWrite 01d9,f8,0,7
SPIWrite 01da,1c,0,7
SPIWrite 01db,80,0,7
SPIWrite 01dc,0f,0,7
SPIWrite 01dd,30,0,7
SPIWrite 01de,08,0,7
SPIWrite 01df,93,0,7
SPIWrite 01e0,01,0,7
SPIWrite 01e1,eb,0,7
SPIWrite 01e2,49,0,7
SPIWrite 01e3,01,0,7
SPIWrite 01e4,4f,0,7
SPIWrite 01e5,ea,0,7
SPIWrite 01e6,20,0,7
SPIWrite 01e7,1b,0,7
SPIWrite 01e8,02,0,7
SPIWrite 01e9,eb,0,7
SPIWrite 01ea,c1,0,7
SPIWrite 01eb,04,0,7
SPIWrite 01ec,b8,0,7
SPIWrite 01ed,f1,0,7
SPIWrite 01ee,01,0,7
SPIWrite 01ef,0f,0,7
SPIWrite 01f0,40,0,7
SPIWrite 01f1,d1,0,7
SPIWrite 01f2,28,0,7
SPIWrite 01f3,78,0,7
SPIWrite 01f4,95,0,7
SPIWrite 01f5,f8,0,7
SPIWrite 01f6,3c,0,7
SPIWrite 01f7,60,0,7
SPIWrite 01f8,c1,0,7
SPIWrite 01f9,08,0,7
SPIWrite 01fa,13,0,7
SPIWrite 01fb,d3,0,7
SPIWrite 01fc,00,0,7
SPIWrite 01fd,96,0,7
SPIWrite 01fe,07,0,7
SPIWrite 01ff,98,0,7
SPIWrite 0200,01,0,7
SPIWrite 0201,90,0,7
SPIWrite 0202,06,0,7
SPIWrite 0203,99,0,7
SPIWrite 0204,05,0,7
SPIWrite 0205,9a,0,7
SPIWrite 0206,03,0,7
SPIWrite 0207,98,0,7
SPIWrite 0208,3b,0,7
SPIWrite 0209,46,0,7
SPIWrite 020a,ff,0,7
SPIWrite 020b,f7,0,7
```

```
SPIWrite 020c,78,0,7
SPIWrite 020d,ff,0,7
SPIWrite 020e,59,0,7
SPIWrite 020f,4d,0,7
SPIWrite 0210,03,0,7
SPIWrite 0211,90,0,7
SPIWrite 0212,dc,0,7
SPIWrite 0213,21,0,7
SPIWrite 0214,4f,0,7
SPIWrite 0215,f4,0,7
SPIWrite 0216,25,0,7
SPIWrite 0217,70,0,7
SPIWrite 0218,1a,0,7
SPIWrite 0219,fb,0,7
SPIWrite 021a,00,0,7
SPIWrite 021b,f0,0,7
SPIWrite 021c,19,0,7
SPIWrite 021d,fb,0,7
SPIWrite 021e,01,0,7
SPIWrite 021f,00,0,7
SPIWrite 0220,2d,0,7
SPIWrite 0221,18,0,7
SPIWrite 0222,28,0,7
SPIWrite 0223,78,0,7
SPIWrite 0224,01,0,7
SPIWrite 0225,09,0,7
SPIWrite 0226,12,0,7
SPIWrite 0227,d3,0,7
SPIWrite 0228,00,0,7
SPIWrite 0229,96,0,7
SPIWrite 022a,08,0,7
SPIWrite 022b,98,0,7
SPIWrite 022c,01,0,7
SPIWrite 022d,90,0,7
SPIWrite 022e,06,0,7
SPIWrite 022f,99,0,7
SPIWrite 0230,05,0,7
SPIWrite 0231,9a,0,7
SPIWrite 0232,02,0,7
SPIWrite 0233,98,0,7
SPIWrite 0234,3b,0,7
SPIWrite 0235,46,0,7
SPIWrite 0236,ff,0,7
SPIWrite 0237,f7,0,7
SPIWrite 0238,62,0,7
SPIWrite 0239,ff,0,7
SPIWrite 023a,4e,0,7
SPIWrite 023b,4b,0,7
SPIWrite 023c,02,0,7
SPIWrite 023d,90,0,7
SPIWrite 023e,dc,0,7
SPIWrite 023f,21,0,7
```

```
SPIWrite 0240,4f,0,7
SPIWrite 0241,f4,0,7
SPIWrite 0242,25,0,7
SPIWrite 0243,70,0,7
SPIWrite 0244,1a,0,7
SPIWrite 0245,fb,0,7
SPIWrite 0246,00,0,7
SPIWrite 0247,f0,0,7
SPIWrite 0248,19,0,7
SPIWrite 0249,fb,0,7
SPIWrite 024a,01,0,7
SPIWrite 024b,00,0,7
SPIWrite 024c,18,0,7
SPIWrite 024d,5c,0,7
SPIWrite 024e,80,0,7
SPIWrite 024f,09,0,7
SPIWrite 0250,09,0,7
SPIWrite 0251,d3,0,7
SPIWrite 0252,00,0,7
SPIWrite 0253,96,0,7
SPIWrite 0254,01,0,7
SPIWrite 0255,20,0,7
SPIWrite 0256,01,0,7
SPIWrite 0257,90,0,7
SPIWrite 0258,06,0,7
SPIWrite 0259,99,0,7
SPIWrite 025a,05,0,7
SPIWrite 025b,9a,0,7
SPIWrite 025c,04,0,7
SPIWrite 025d,98,0,7
SPIWrite 025e,3b,0,7
SPIWrite 025f,46,0,7
SPIWrite 0260,ff,0,7
SPIWrite 0261,f7,0,7
SPIWrite 0262,4d,0,7
SPIWrite 0263,ff,0,7
SPIWrite 0264,04,0,7
SPIWrite 0265,90,0,7
SPIWrite 0266,0b,0,7
SPIWrite 0267,eb,0,7
SPIWrite 0268,06,0,7
SPIWrite 0269,00,0,7
SPIWrite 026a,40,0,7
SPIWrite 026b,1c,0,7
SPIWrite 026c,c7,0,7
SPIWrite 026d,b2,0,7
SPIWrite 026e,40,0,7
SPIWrite 026f,2f,0,7
SPIWrite 0270,a8,0,7
SPIWrite 0271,bf,0,7
SPIWrite 0272,3f,0,7
SPIWrite 0273,27,0,7
```

```
SPIWrite 0274,02,0,7
SPIWrite 0275,98,0,7
SPIWrite 0276,03,0,7
SPIWrite 0277,9e,0,7
SPIWrite 0278,a7,0,7
SPIWrite 0279,71,0,7
SPIWrite 027a,08,0,7
SPIWrite 027b,f1,0,7
SPIWrite 027c,01,0,7
SPIWrite 027d,08,0,7
SPIWrite 027e,20,0,7
SPIWrite 027f,80,0,7
SPIWrite 0280,04,0,7
SPIWrite 0281,9b,0,7
SPIWrite 0282,66,0,7
SPIWrite 0283,80,0,7
SPIWrite 0284,b8,0,7
SPIWrite 0285,f1,0,7
SPIWrite 0286,02,0,7
SPIWrite 0287,0f,0,7
SPIWrite 0288,a3,0,7
SPIWrite 0289,80,0,7
SPIWrite 028a,04,0,7
SPIWrite 028b,f1,0,7
SPIWrite 028c,08,0,7
SPIWrite 028d,04,0,7
SPIWrite 028e,ad,0,7
SPIWrite 028f,db,0,7
SPIWrite 0290,09,0,7
SPIWrite 0291,b0,0,7
SPIWrite 0292,bd,0,7
SPIWrite 0293,e8,0,7
SPIWrite 0294,f0,0,7
SPIWrite 0295,8f,0,7
SPIWrite 0296,f8,0,7
SPIWrite 0297,b5,0,7
SPIWrite 0298,b9,0,7
SPIWrite 0299,4b,0,7
SPIWrite 029a,35,0,7
SPIWrite 029b,4a,0,7
SPIWrite 029c,84,0,7
SPIWrite 029d,46,0,7
SPIWrite 029e,0c,0,7
SPIWrite 029f,24,0,7
SPIWrite 02a0,88,0,7
SPIWrite 02a1,00,0,7
SPIWrite 02a2,1c,0,7
SPIWrite 02a3,fb,0,7
SPIWrite 02a4,04,0,7
SPIWrite 02a5,04,0,7
SPIWrite 02a6,1f,0,7
SPIWrite 02a7,78,0,7
```

```
SPIWrite 02a8,12,0,7
SPIWrite 02a9,59,0,7
SPIWrite 02aa,00,0,7
SPIWrite 02ab,26,0,7
SPIWrite 02ac,00,0,7
SPIWrite 02ad,2f,0,7
SPIWrite 02ae,08,0,7
SPIWrite 02af,bf,0,7
SPIWrite 02b0,35,0,7
SPIWrite 02b1,1c,0,7
SPIWrite 02b2,0c,0,7
SPIWrite 02b3,d0,0,7
SPIWrite 02b4,d2,0,7
SPIWrite 02b5,f8,0,7
SPIWrite 02b6,e8,0,7
SPIWrite 02b7,35,0,7
SPIWrite 02b8,d2,0,7
SPIWrite 02b9,f8,0,7
SPIWrite 02ba,e8,0,7
SPIWrite 02bb,45,0,7
SPIWrite 02bc,c4,0,7
SPIWrite 02bd,f3,0,7
SPIWrite 02be,80,0,7
SPIWrite 02bf,15,0,7
SPIWrite 02c0,c3,0,7
SPIWrite 02c1,f3,0,7
SPIWrite 02c2,80,0,7
SPIWrite 02c3,13,0,7
SPIWrite 02c4,ab,0,7
SPIWrite 02c5,42,0,7
SPIWrite 02c6,18,0,7
SPIWrite 02c7,bf,0,7
SPIWrite 02c8,b7,0,7
SPIWrite 02c9,f1,0,7
SPIWrite 02ca,01,0,7
SPIWrite 02cb,07,0,7
SPIWrite 02cc,f2,0,7
SPIWrite 02cd,d1,0,7
SPIWrite 02ce,bd,0,7
SPIWrite 02cf,4c,0,7
SPIWrite 02d0,03,0,7
SPIWrite 02d1,22,0,7
SPIWrite 02d2,1c,0,7
SPIWrite 02d3,fb,0,7
SPIWrite 02d4,02,0,7
SPIWrite 02d5,f3,0,7
SPIWrite 02d6,ca,0,7
SPIWrite 02d7,18,0,7
SPIWrite 02d8,a4,0,7
SPIWrite 02d9,18,0,7
SPIWrite 02da,22,0,7
SPIWrite 02db,78,0,7
```

```
SPIWrite 02dc,95,0,7
SPIWrite 02dd,42,0,7
SPIWrite 02de,1d,0,7
SPIWrite 02df,d0,0,7
SPIWrite 02e0,c5,0,7
SPIWrite 02e1,4a,0,7
SPIWrite 02e2,12,0,7
SPIWrite 02e3,78,0,7
SPIWrite 02e4,01,0,7
SPIWrite 02e5,26,0,7
SPIWrite 02e6,01,0,7
SPIWrite 02e7,2a,0,7
SPIWrite 02e8,0e,0,7
SPIWrite 02e9,d0,0,7
SPIWrite 02ea,c4,0,7
SPIWrite 02eb,4a,0,7
SPIWrite 02ec,12,0,7
SPIWrite 02ed,78,0,7
SPIWrite 02ee,01,0,7
SPIWrite 02ef,2a,0,7
SPIWrite 02f0,13,0,7
SPIWrite 02f1,d1,0,7
SPIWrite 02f2,c3,0,7
SPIWrite 02f3,4a,0,7
SPIWrite 02f4,05,0,7
SPIWrite 02f5,eb,0,7
SPIWrite 02f6,43,0,7
SPIWrite 02f7,03,0,7
SPIWrite 02f8,00,0,7
SPIWrite 02f9,eb,0,7
SPIWrite 02fa,43,0,7
SPIWrite 02fb,00,0,7
SPIWrite 02fc,2b,0,7
SPIWrite 02fd,46,0,7
SPIWrite 02fe,12,0,7
SPIWrite 02ff,18,0,7
SPIWrite 0300,60,0,7
SPIWrite 0301,46,0,7
SPIWrite 0302,00,0,7
SPIWrite 0303,f0,0,7
SPIWrite 0304,05,0,7
SPIWrite 0305,fc,0,7
SPIWrite 0306,08,0,7
SPIWrite 0307,e0,0,7
SPIWrite 0308,68,0,7
SPIWrite 0309,4a,0,7
SPIWrite 030a,c8,0,7
SPIWrite 030b,18,0,7
SPIWrite 030c,05,0,7
SPIWrite 030d,eb,0,7
SPIWrite 030e,40,0,7
SPIWrite 030f,00,0,7
```

```
SPIWrite 0310,02,0,7
SPIWrite 0311,eb,0,7
SPIWrite 0312,c0,0,7
SPIWrite 0313,02,0,7
SPIWrite 0314,60,0,7
SPIWrite 0315,46,0,7
SPIWrite 0316,ff,0,7
SPIWrite 0317,f7,0,7
SPIWrite 0318,ce,0,7
SPIWrite 0319,fe,0,7
SPIWrite 031a,25,0,7
SPIWrite 031b,70,0,7
SPIWrite 031c,30,0,7
SPIWrite 031d,46,0,7
SPIWrite 031e,f8,0,7
SPIWrite 031f,bd,0,7
SPIWrite 0320,44,0,7
SPIWrite 0321,27,0,7
SPIWrite 0322,10,0,7
SPIWrite 0323,68,0,7
SPIWrite 0324,18,0,7
SPIWrite 0325,70,0,7
SPIWrite 0326,02,0,7
SPIWrite 0327,00,0,7
SPIWrite 0328,b3,0,7
SPIWrite 0329,48,0,7
SPIWrite 032a,2d,0,7
SPIWrite 032b,e9,0,7
SPIWrite 032c,f0,0,7
SPIWrite 032d,4f,0,7
SPIWrite 032e,00,0,7
SPIWrite 032f,78,0,7
SPIWrite 0330,ad,0,7
SPIWrite 0331,f1,0,7
SPIWrite 0332,34,0,7
SPIWrite 0333,0d,0,7
SPIWrite 0334,06,0,7
SPIWrite 0335,90,0,7
SPIWrite 0336,00,0,7
SPIWrite 0337,20,0,7
SPIWrite 0338,07,0,7
SPIWrite 0339,90,0,7
SPIWrite 033a,0d,0,7
SPIWrite 033b,f1,0,7
SPIWrite 033c,0f,0,7
SPIWrite 033d,07,0,7
SPIWrite 033e,08,0,7
SPIWrite 033f,90,0,7
SPIWrite 0340,84,0,7
SPIWrite 0341,46,0,7
SPIWrite 0342,09,0,7
SPIWrite 0343,90,0,7
```

```
SPIWrite 0344,9f,0,7
SPIWrite 0345,49,0,7
SPIWrite 0346,0a,0,7
SPIWrite 0347,48,0,7
SPIWrite 0348,08,0,7
SPIWrite 0349,9a,0,7
SPIWrite 034a,0a,0,7
SPIWrite 034b,4c,0,7
SPIWrite 034c,07,0,7
SPIWrite 034d,9e,0,7
SPIWrite 034e,00,0,7
SPIWrite 034f,25,0,7
SPIWrite 0350,2b,0,7
SPIWrite 0351,46,0,7
SPIWrite 0352,61,0,7
SPIWrite 0353,44,0,7
SPIWrite 0354,80,0,7
SPIWrite 0355,18,0,7
SPIWrite 0356,07,0,7
SPIWrite 0357,f8,0,7
SPIWrite 0358,01,0,7
SPIWrite 0359,3f,0,7
SPIWrite 035a,49,0,7
SPIWrite 035b,1e,0,7
SPIWrite 035c,a0,0,7
SPIWrite 035d,f1,0,7
SPIWrite 035e,04,0,7
SPIWrite 035f,0b,0,7
SPIWrite 0360,a4,0,7
SPIWrite 0361,19,0,7
SPIWrite 0362,be,0,7
SPIWrite 0363,48,0,7
SPIWrite 0364,05,0,7
SPIWrite 0365,91,0,7
SPIWrite 0366,dc,0,7
SPIWrite 0367,3c,0,7
SPIWrite 0368,0c,0,7
SPIWrite 0369,eb,0,7
SPIWrite 036a,00,0,7
SPIWrite 036b,06,0,7
SPIWrite 036c,04,0,7
SPIWrite 036d,e0,0,7
SPIWrite 036e,c0,0,7
SPIWrite 036f,46,0,7
SPIWrite 0370,a8,0,7
SPIWrite 0371,75,0,7
SPIWrite 0372,02,0,7
SPIWrite 0373,00,0,7
SPIWrite 0374,e0,0,7
SPIWrite 0375,ab,0,7
SPIWrite 0376,00,0,7
SPIWrite 0377,20,0,7
```

```
SPIWrite 0378,dc,0,7
SPIWrite 0379,34,0,7
SPIWrite 037a,5b,0,7
SPIWrite 037b,f8,0,7
SPIWrite 037c,04,0,7
SPIWrite 037d,0f,0,7
SPIWrite 037e,94,0,7
SPIWrite 037f,f8,0,7
SPIWrite 0380,3d,0,7
SPIWrite 0381,10,0,7
SPIWrite 0382,d0,0,7
SPIWrite 0383,f8,0,7
SPIWrite 0384,98,0,7
SPIWrite 0385,a4,0,7
SPIWrite 0386,05,0,7
SPIWrite 0387,9a,0,7
SPIWrite 0388,94,0,7
SPIWrite 0389,f8,0,7
SPIWrite 038a,38,0,7
SPIWrite 038b,30,0,7
SPIWrite 038c,94,0,7
SPIWrite 038d,f8,0,7
SPIWrite 038e,3c,0,7
SPIWrite 038f,90,0,7
SPIWrite 0390,94,0,7
SPIWrite 0391,f8,0,7
SPIWrite 0392,7a,0,7
SPIWrite 0393,80,0,7
SPIWrite 0394,0a,0,7
SPIWrite 0395,91,0,7
SPIWrite 0396,ff,0,7
SPIWrite 0397,20,0,7
SPIWrite 0398,0b,0,7
SPIWrite 0399,93,0,7
SPIWrite 039a,29,0,7
SPIWrite 039b,46,0,7
SPIWrite 039c,02,0,7
SPIWrite 039d,f8,0,7
SPIWrite 039e,01,0,7
SPIWrite 039f,0f,0,7
SPIWrite 03a0,09,0,7
SPIWrite 03a1,98,0,7
SPIWrite 03a2,05,0,7
SPIWrite 03a3,92,0,7
SPIWrite 03a4,ff,0,7
SPIWrite 03a5,f7,0,7
SPIWrite 03a6,54,0,7
SPIWrite 03a7,fe,0,7
SPIWrite 03a8,06,0,7
SPIWrite 03a9,99,0,7
SPIWrite 03aa,0a,0,7
SPIWrite 03ab,f0,0,7
```

```
SPIWrite 03ac,01,0,7
SPIWrite 03ad,02,0,7
SPIWrite 03ae,11,0,7
SPIWrite 03af,40,0,7
SPIWrite 03b0,01,0,7
SPIWrite 03b1,29,0,7
SPIWrite 03b2,0d,0,7
SPIWrite 03b3,d1,0,7
SPIWrite 03b4,b8,0,7
SPIWrite 03b5,f1,0,7
SPIWrite 03b6,00,0,7
SPIWrite 03b7,0f,0,7
SPIWrite 03b8,0a,0,7
SPIWrite 03b9,d1,0,7
SPIWrite 03ba,0a,0,7
SPIWrite 03bb,9a,0,7
SPIWrite 03bc,0b,0,7
SPIWrite 03bd,9b,0,7
SPIWrite 03be,0f,0,7
SPIWrite 03bf,30,0,7
SPIWrite 03c0,a2,0,7
SPIWrite 03c1,eb,0,7
SPIWrite 03c2,09,0,7
SPIWrite 03c3,02,0,7
SPIWrite 03c4,03,0,7
SPIWrite 03c5,eb,0,7
SPIWrite 03c6,20,0,7
SPIWrite 03c7,10,0,7
SPIWrite 03c8,90,0,7
SPIWrite 03c9,42,0,7
SPIWrite 03ca,a8,0,7
SPIWrite 03cb,bf,0,7
SPIWrite 03cc,01,0,7
SPIWrite 03cd,20,0,7
SPIWrite 03ce,00,0,7
SPIWrite 03cf,da,0,7
SPIWrite 03d0,00,0,7
SPIWrite 03d1,20,0,7
SPIWrite 03d2,01,0,7
SPIWrite 03d3,29,0,7
SPIWrite 03d4,30,0,7
SPIWrite 03d5,70,0,7
SPIWrite 03d6,04,0,7
SPIWrite 03d7,d1,0,7
SPIWrite 03d8,39,0,7
SPIWrite 03d9,78,0,7
SPIWrite 03da,01,0,7
SPIWrite 03db,20,0,7
SPIWrite 03dc,a8,0,7
SPIWrite 03dd,40,0,7
SPIWrite 03de,08,0,7
SPIWrite 03df,43,0,7
```

```
SPIWrite 03e0,38,0,7
SPIWrite 03e1,70,0,7
SPIWrite 03e2,6d,0,7
SPIWrite 03e3,1c,0,7
SPIWrite 03e4,76,0,7
SPIWrite 03e5,1c,0,7
SPIWrite 03e6,03,0,7
SPIWrite 03e7,2d,0,7
SPIWrite 03e8,c6,0,7
SPIWrite 03e9,db,0,7
SPIWrite 03ea,08,0,7
SPIWrite 03eb,99,0,7
SPIWrite 03ec,09,0,7
SPIWrite 03ed,98,0,7
SPIWrite 03ee,07,0,7
SPIWrite 03ef,9e,0,7
SPIWrite 03f0,0c,0,7
SPIWrite 03f1,31,0,7
SPIWrite 03f2,0c,0,7
SPIWrite 03f3,f1,0,7
SPIWrite 03f4,03,0,7
SPIWrite 03f5,0c,0,7
SPIWrite 03f6,40,0,7
SPIWrite 03f7,1c,0,7
SPIWrite 03f8,08,0,7
SPIWrite 03f9,91,0,7
SPIWrite 03fa,02,0,7
SPIWrite 03fb,28,0,7
SPIWrite 03fc,09,0,7
SPIWrite 03fd,90,0,7
SPIWrite 03fe,06,0,7
SPIWrite 03ff,f5,0,7
SPIWrite 0400,25,0,7
SPIWrite 0401,71,0,7
SPIWrite 0402,07,0,7
SPIWrite 0403,91,0,7
SPIWrite 0404,9e,0,7
SPIWrite 0405,db,0,7
SPIWrite 0406,04,0,7
SPIWrite 0407,a8,0,7
SPIWrite 0408,ff,0,7
SPIWrite 0409,f7,0,7
SPIWrite 040a,30,0,7
SPIWrite 040b,fe,0,7
SPIWrite 040c,00,0,7
SPIWrite 040d,25,0,7
SPIWrite 040e,4f,0,7
SPIWrite 040f,f0,0,7
SPIWrite 0410,dc,0,7
SPIWrite 0411,09,0,7
SPIWrite 0412,2e,0,7
SPIWrite 0413,46,0,7
```

```
SPIWrite 0414,df,0,7
SPIWrite 0415,f8,0,7
SPIWrite 0416,48,0,7
SPIWrite 0417,82,0,7
SPIWrite 0418,90,0,7
SPIWrite 0419,48,0,7
SPIWrite 041a,00,0,7
SPIWrite 041b,24,0,7
SPIWrite 041c,2f,0,7
SPIWrite 041d,18,0,7
SPIWrite 041e,17,0,7
SPIWrite 041f,f8,0,7
SPIWrite 0420,01,0,7
SPIWrite 0421,0b,0,7
SPIWrite 0422,18,0,7
SPIWrite 0423,bb,0,7
SPIWrite 0424,01,0,7
SPIWrite 0425,21,0,7
SPIWrite 0426,06,0,7
SPIWrite 0427,eb,0,7
SPIWrite 0428,46,0,7
SPIWrite 0429,00,0,7
SPIWrite 042a,8d,0,7
SPIWrite 042b,f8,0,7
SPIWrite 042c,01,0,7
SPIWrite 042d,10,0,7
SPIWrite 042e,20,0,7
SPIWrite 042f,18,0,7
SPIWrite 0430,09,0,7
SPIWrite 0431,fb,0,7
SPIWrite 0432,00,0,7
SPIWrite 0433,80,0,7
SPIWrite 0434,c3,0,7
SPIWrite 0435,88,0,7
SPIWrite 0436,01,0,7
SPIWrite 0437,89,0,7
SPIWrite 0438,ad,0,7
SPIWrite 0439,f8,0,7
SPIWrite 043a,0a,0,7
SPIWrite 043b,30,0,7
SPIWrite 043c,83,0,7
SPIWrite 043d,89,0,7
SPIWrite 043e,ad,0,7
SPIWrite 043f,f8,0,7
SPIWrite 0440,08,0,7
SPIWrite 0441,10,0,7
SPIWrite 0442,6a,0,7
SPIWrite 0443,46,0,7
SPIWrite 0444,ad,0,7
SPIWrite 0445,f8,0,7
SPIWrite 0446,0c,0,7
SPIWrite 0447,30,0,7
```

```
SPIWrite 0448,90,0,7
SPIWrite 0449,f8,0,7
SPIWrite 044a,3d,0,7
SPIWrite 044b,30,0,7
SPIWrite 044c,90,0,7
SPIWrite 044d,f8,0,7
SPIWrite 044e,38,0,7
SPIWrite 044f,00,0,7
SPIWrite 0450,8d,0,7
SPIWrite 0451,f8,0,7
SPIWrite 0452,0e,0,7
SPIWrite 0453,30,0,7
SPIWrite 0454,21,0,7
SPIWrite 0455,46,0,7
SPIWrite 0456,8d,0,7
SPIWrite 0457,f8,0,7
SPIWrite 0458,00,0,7
SPIWrite 0459,00,0,7
SPIWrite 045a,30,0,7
SPIWrite 045b,46,0,7
SPIWrite 045c,ff,0,7
SPIWrite 045d,f7,0,7
SPIWrite 045e,18,0,7
SPIWrite 045f,fe,0,7
SPIWrite 0460,02,0,7
SPIWrite 0461,aa,0,7
SPIWrite 0462,30,0,7
SPIWrite 0463,46,0,7
SPIWrite 0464,21,0,7
SPIWrite 0465,46,0,7
SPIWrite 0466,ff,0,7
SPIWrite 0467,f7,0,7
SPIWrite 0468,26,0,7
SPIWrite 0469,fe,0,7
SPIWrite 046a,12,0,7
SPIWrite 046b,e0,0,7
SPIWrite 046c,30,0,7
SPIWrite 046d,46,0,7
SPIWrite 046e,21,0,7
SPIWrite 046f,46,0,7
SPIWrite 0470,ff,0,7
SPIWrite 0471,f7,0,7
SPIWrite 0472,8d,0,7
SPIWrite 0473,fe,0,7
SPIWrite 0474,00,0,7
SPIWrite 0475,20,0,7
SPIWrite 0476,21,0,7
SPIWrite 0477,46,0,7
SPIWrite 0478,6a,0,7
SPIWrite 0479,46,0,7
SPIWrite 047a,8d,0,7
SPIWrite 047b,f8,0,7
```

```
SPIWrite 047c,00,0,7
SPIWrite 047d,00,0,7
SPIWrite 047e,03,0,7
SPIWrite 047f,46,0,7
SPIWrite 0480,8d,0,7
SPIWrite 0481,f8,0,7
SPIWrite 0482,01,0,7
SPIWrite 0483,30,0,7
SPIWrite 0484,30,0,7
SPIWrite 0485,46,0,7
SPIWrite 0486,ff,0,7
SPIWrite 0487,f7,0,7
SPIWrite 0488,03,0,7
SPIWrite 0489,fe,0,7
SPIWrite 048a,30,0,7
SPIWrite 048b,46,0,7
SPIWrite 048c,21,0,7
SPIWrite 048d,46,0,7
SPIWrite 048e,ff,0,7
SPIWrite 048f,f7,0,7
SPIWrite 0490,02,0,7
SPIWrite 0491,ff,0,7
SPIWrite 0492,64,0,7
SPIWrite 0493,1c,0,7
SPIWrite 0494,03,0,7
SPIWrite 0495,2c,0,7
SPIWrite 0496,c2,0,7
SPIWrite 0497,db,0,7
SPIWrite 0498,76,0,7
SPIWrite 0499,1c,0,7
SPIWrite 049a,ed,0,7
SPIWrite 049b,1c,0,7
SPIWrite 049c,02,0,7
SPIWrite 049d,2e,0,7
SPIWrite 049e,bb,0,7
SPIWrite 049f,db,0,7
SPIWrite 04a0,0d,0,7
SPIWrite 04a1,b0,0,7
SPIWrite 04a2,bd,0,7
SPIWrite 04a3,e8,0,7
SPIWrite 04a4,f0,0,7
SPIWrite 04a5,8f,0,7
SPIWrite 04a6,c0,0,7
SPIWrite 04a7,46,0,7
SPIWrite 04a8,18,0,7
SPIWrite 04a9,6e,0,7
SPIWrite 04aa,02,0,7
SPIWrite 04ab,00,0,7
SPIWrite 04ac,2c,0,7
SPIWrite 04ad,22,0,7
SPIWrite 04ae,01,0,7
SPIWrite 04af,20,0,7
```

```
SPIWrite 04b0,2d,0,7
SPIWrite 04b1,e9,0,7
SPIWrite 04b2,b8,0,7
SPIWrite 04b3,41,0,7
SPIWrite 04b4,51,0,7
SPIWrite 04b5,48,0,7
SPIWrite 04b6,6b,0,7
SPIWrite 04b7,4a,0,7
SPIWrite 04b8,77,0,7
SPIWrite 04b9,4c,0,7
SPIWrite 04ba,6b,0,7
SPIWrite 04bb,4d,0,7
SPIWrite 04bc,df,0,7
SPIWrite 04bd,f8,0,7
SPIWrite 04be,b0,0,7
SPIWrite 04bf,81,0,7
SPIWrite 04c0,07,0,7
SPIWrite 04c1,78,0,7
SPIWrite 04c2,12,0,7
SPIWrite 04c3,78,0,7
SPIWrite 04c4,4c,0,7
SPIWrite 04c5,48,0,7
SPIWrite 04c6,52,0,7
SPIWrite 04c7,08,0,7
SPIWrite 04c8,18,0,7
SPIWrite 04c9,d2,0,7
SPIWrite 04ca,00,0,7
SPIWrite 04cb,21,0,7
SPIWrite 04cc,01,0,7
SPIWrite 04cd,70,0,7
SPIWrite 04ce,5f,0,7
SPIWrite 04cf,b9,0,7
SPIWrite 04d0,4f,0,7
SPIWrite 04d1,f0,0,7
SPIWrite 04d2,00,0,7
SPIWrite 04d3,70,0,7
SPIWrite 04d4,80,0,7
SPIWrite 04d5,34,0,7
SPIWrite 04d6,20,0,7
SPIWrite 04d7,60,0,7
SPIWrite 04d8,66,0,7
SPIWrite 04d9,49,0,7
SPIWrite 04da,c8,0,7
SPIWrite 04db,f8,0,7
SPIWrite 04dc,7c,0,7
SPIWrite 04dd,11,0,7
SPIWrite 04de,66,0,7
SPIWrite 04df,4a,0,7
SPIWrite 04e0,c8,0,7
SPIWrite 04e1,f8,0,7
SPIWrite 04e2,a0,0,7
SPIWrite 04e3,21,0,7
```

```
SPIWrite 04e4,61,0,7
SPIWrite 04e5,4f,0,7
SPIWrite 04e6,2f,0,7
SPIWrite 04e7,60,0,7
SPIWrite 04e8,64,0,7
SPIWrite 04e9,48,0,7
SPIWrite 04ea,c8,0,7
SPIWrite 04eb,f8,0,7
SPIWrite 04ec,98,0,7
SPIWrite 04ed,01,0,7
SPIWrite 04ee,64,0,7
SPIWrite 04ef,48,0,7
SPIWrite 04f0,c8,0,7
SPIWrite 04f1,f8,0,7
SPIWrite 04f2,b8,0,7
SPIWrite 04f3,01,0,7
SPIWrite 04f4,ff,0,7
SPIWrite 04f5,f7,0,7
SPIWrite 04f6,18,0,7
SPIWrite 04f7,ff,0,7
SPIWrite 04f8,bd,0,7
SPIWrite 04f9,e8,0,7
SPIWrite 04fa,b8,0,7
SPIWrite 04fb,81,0,7
SPIWrite 04fc,01,0,7
SPIWrite 04fd,2f,0,7
SPIWrite 04fe,16,0,7
SPIWrite 04ff,d0,0,7
SPIWrite 0500,01,0,7
SPIWrite 0501,21,0,7
SPIWrite 0502,01,0,7
SPIWrite 0503,70,0,7
SPIWrite 0504,ff,0,7
SPIWrite 0505,f7,0,7
SPIWrite 0506,10,0,7
SPIWrite 0507,ff,0,7
SPIWrite 0508,5e,0,7
SPIWrite 0509,48,0,7
SPIWrite 050a,28,0,7
SPIWrite 050b,60,0,7
SPIWrite 050c,5f,0,7
SPIWrite 050d,4f,0,7
SPIWrite 050e,c8,0,7
SPIWrite 050f,f8,0,7
SPIWrite 0510,a0,0,7
SPIWrite 0511,71,0,7
SPIWrite 0512,5d,0,7
SPIWrite 0513,49,0,7
SPIWrite 0514,c8,0,7
SPIWrite 0515,f8,0,7
SPIWrite 0516,7c,0,7
SPIWrite 0517,11,0,7
```

```
SPIWrite 0518,5d,0,7
SPIWrite 0519,4b,0,7
SPIWrite 051a,c8,0,7
SPIWrite 051b,f8,0,7
SPIWrite 051c,98,0,7
SPIWrite 051d,31,0,7
SPIWrite 051e,5d,0,7
SPIWrite 051f,4a,0,7
SPIWrite 0520,c8,0,7
SPIWrite 0521,f8,0,7
SPIWrite 0522,b8,0,7
SPIWrite 0523,21,0,7
SPIWrite 0524,4f,0,7
SPIWrite 0525,f0,0,7
SPIWrite 0526,00,0,7
SPIWrite 0527,75,0,7
SPIWrite 0528,25,0,7
SPIWrite 0529,60,0,7
SPIWrite 052a,bd,0,7
SPIWrite 052b,e8,0,7
SPIWrite 052c,b8,0,7
SPIWrite 052d,81,0,7
SPIWrite 052e,08,0,7
SPIWrite 052f,20,0,7
SPIWrite 0530,08,0,7
SPIWrite 0531,70,0,7
SPIWrite 0532,bd,0,7
SPIWrite 0533,e8,0,7
SPIWrite 0534,b8,0,7
SPIWrite 0535,81,0,7
SPIWrite 0536,38,0,7
SPIWrite 0537,b5,0,7
SPIWrite 0538,0d,0,7
SPIWrite 0539,46,0,7
SPIWrite 053a,d2,0,7
SPIWrite 053b,f7,0,7
SPIWrite 053c,df,0,7
SPIWrite 053d,ff,0,7
SPIWrite 053e,2e,0,7
SPIWrite 053f,48,0,7
SPIWrite 0540,48,0,7
SPIWrite 0541,49,0,7
SPIWrite 0542,00,0,7
SPIWrite 0543,78,0,7
SPIWrite 0544,0c,0,7
SPIWrite 0545,78,0,7
SPIWrite 0546,01,0,7
SPIWrite 0547,28,0,7
SPIWrite 0548,0a,0,7
SPIWrite 0549,d0,0,7
SPIWrite 054a,2c,0,7
SPIWrite 054b,48,0,7
```

```
SPIWrite 054c,00,0,7
SPIWrite 054d,78,0,7
SPIWrite 054e,01,0,7
SPIWrite 054f,28,0,7
SPIWrite 0550,08,0,7
SPIWrite 0551,d1,0,7
SPIWrite 0552,00,0,7
SPIWrite 0553,f0,0,7
SPIWrite 0554,28,0,7
SPIWrite 0555,fb,0,7
SPIWrite 0556,20,0,7
SPIWrite 0557,46,0,7
SPIWrite 0558,29,0,7
SPIWrite 0559,46,0,7
SPIWrite 055a,00,0,7
SPIWrite 055b,f0,0,7
SPIWrite 055c,d1,0,7
SPIWrite 055d,fb,0,7
SPIWrite 055e,38,0,7
SPIWrite 055f,bd,0,7
SPIWrite 0560,ff,0,7
SPIWrite 0561,f7,0,7
SPIWrite 0562,e2,0,7
SPIWrite 0563,fe,0,7
SPIWrite 0564,38,0,7
SPIWrite 0565,bd,0,7
SPIWrite 0566,08,0,7
SPIWrite 0567,b5,0,7
SPIWrite 0568,d3,0,7
SPIWrite 0569,f7,0,7
SPIWrite 056a,be,0,7
SPIWrite 056b,fa,0,7
SPIWrite 056c,ff,0,7
SPIWrite 056d,f7,0,7
SPIWrite 056e,dc,0,7
SPIWrite 056f,fe,0,7
SPIWrite 0570,08,0,7
SPIWrite 0571,bd,0,7
SPIWrite 0572,08,0,7
SPIWrite 0573,b5,0,7
SPIWrite 0574,d3,0,7
SPIWrite 0575,f7,0,7
SPIWrite 0576,32,0,7
SPIWrite 0577,fb,0,7
SPIWrite 0578,ff,0,7
SPIWrite 0579,f7,0,7
SPIWrite 057a,d6,0,7
SPIWrite 057b,fe,0,7
SPIWrite 057c,08,0,7
SPIWrite 057d,bd,0,7
SPIWrite 057e,c0,0,7
SPIWrite 057f,46,0,7
```

```
SPIWrite 0580,2b,0,7
SPIWrite 0581,22,0,7
SPIWrite 0582,01,0,7
SPIWrite 0583,20,0,7
SPIWrite 0584,f8,0,7
SPIWrite 0585,b5,0,7
SPIWrite 0586,0c,0,7
SPIWrite 0587,46,0,7
SPIWrite 0588,d3,0,7
SPIWrite 0589,f7,0,7
SPIWrite 058a,d2,0,7
SPIWrite 058b,fc,0,7
SPIWrite 058c,4f,0,7
SPIWrite 058d,f0,0,7
SPIWrite 058e,22,0,7
SPIWrite 058f,40,0,7
SPIWrite 0590,90,0,7
SPIWrite 0591,f8,0,7
SPIWrite 0592,b4,0,7
SPIWrite 0593,e3,0,7
SPIWrite 0594,41,0,7
SPIWrite 0595,4b,0,7
SPIWrite 0596,90,0,7
SPIWrite 0597,f8,0,7
SPIWrite 0598,b5,0,7
SPIWrite 0599,c3,0,7
SPIWrite 059a,01,0,7
SPIWrite 059b,25,0,7
SPIWrite 059c,08,0,7
SPIWrite 059d,22,0,7
SPIWrite 059e,00,0,7
SPIWrite 059f,20,0,7
SPIWrite 05a0,01,0,7
SPIWrite 05a1,46,0,7
SPIWrite 05a2,05,0,7
SPIWrite 05a3,fa,0,7
SPIWrite 05a4,00,0,7
SPIWrite 05a5,f6,0,7
SPIWrite 05a6,1e,0,7
SPIWrite 05a7,ea,0,7
SPIWrite 05a8,06,0,7
SPIWrite 05a9,0f,0,7
SPIWrite 05aa,07,0,7
SPIWrite 05ab,d0,0,7
SPIWrite 05ac,bc,0,7
SPIWrite 05ad,f1,0,7
SPIWrite 05ae,01,0,7
SPIWrite 05af,0f,0,7
SPIWrite 05b0,03,0,7
SPIWrite 05b1,d1,0,7
SPIWrite 05b2,1f,0,7
SPIWrite 05b3,5c,0,7
```

```
SPIWrite 05b4,07,0,7
SPIWrite 05b5,b9,0,7
SPIWrite 05b6,22,0,7
SPIWrite 05b7,70,0,7
SPIWrite 05b8,00,0,7
SPIWrite 05b9,e0,0,7
SPIWrite 05ba,21,0,7
SPIWrite 05bb,70,0,7
SPIWrite 05bc,40,0,7
SPIWrite 05bd,1c,0,7
SPIWrite 05be,04,0,7
SPIWrite 05bf,28,0,7
SPIWrite 05c0,ef,0,7
SPIWrite 05c1,db,0,7
SPIWrite 05c2,f8,0,7
SPIWrite 05c3,bd,0,7
SPIWrite 05c4,d4,0,7
SPIWrite 05c5,22,0,7
SPIWrite 05c6,01,0,7
SPIWrite 05c7,20,0,7
SPIWrite 05c8,38,0,7
SPIWrite 05c9,b5,0,7
SPIWrite 05ca,0d,0,7
SPIWrite 05cb,46,0,7
SPIWrite 05cc,d4,0,7
SPIWrite 05cd,f7,0,7
SPIWrite 05ce,bc,0,7
SPIWrite 05cf,f8,0,7
SPIWrite 05d0,09,0,7
SPIWrite 05d1,48,0,7
SPIWrite 05d2,24,0,7
SPIWrite 05d3,49,0,7
SPIWrite 05d4,00,0,7
SPIWrite 05d5,78,0,7
SPIWrite 05d6,0c,0,7
SPIWrite 05d7,78,0,7
SPIWrite 05d8,01,0,7
SPIWrite 05d9,28,0,7
SPIWrite 05da,0a,0,7
SPIWrite 05db,d0,0,7
SPIWrite 05dc,07,0,7
SPIWrite 05dd,48,0,7
SPIWrite 05de,00,0,7
SPIWrite 05df,78,0,7
SPIWrite 05e0,01,0,7
SPIWrite 05e1,28,0,7
SPIWrite 05e2,08,0,7
SPIWrite 05e3,d1,0,7
SPIWrite 05e4,00,0,7
SPIWrite 05e5,f0,0,7
SPIWrite 05e6,df,0,7
SPIWrite 05e7,fa,0,7
```

```
SPIWrite 05e8,20,0,7
SPIWrite 05e9,46,0,7
SPIWrite 05ea,29,0,7
SPIWrite 05eb,46,0,7
SPIWrite 05ec,00,0,7
SPIWrite 05ed,f0,0,7
SPIWrite 05ee,88,0,7
SPIWrite 05ef,fb,0,7
SPIWrite 05f0,38,0,7
SPIWrite 05f1,bd,0,7
SPIWrite 05f2,ff,0,7
SPIWrite 05f3,f7,0,7
SPIWrite 05f4,99,0,7
SPIWrite 05f5,fe,0,7
SPIWrite 05f6,38,0,7
SPIWrite 05f7,bd,0,7
SPIWrite 05f8,f3,0,7
SPIWrite 05f9,22,0,7
SPIWrite 05fa,01,0,7
SPIWrite 05fb,20,0,7
SPIWrite 05fc,f2,0,7
SPIWrite 05fd,22,0,7
SPIWrite 05fe,01,0,7
SPIWrite 05ff,20,0,7
SPIWrite 0600,8c,0,7
SPIWrite 0601,22,0,7
SPIWrite 0602,01,0,7
SPIWrite 0603,20,0,7
SPIWrite 0604,2d,0,7
SPIWrite 0605,e9,0,7
SPIWrite 0606,f0,0,7
SPIWrite 0607,47,0,7
SPIWrite 0608,df,0,7
SPIWrite 0609,f8,0,7
SPIWrite 060a,50,0,7
SPIWrite 060b,a0,0,7
SPIWrite 060c,4f,0,7
SPIWrite 060d,f0,0,7
SPIWrite 060e,00,0,7
SPIWrite 060f,09,0,7
SPIWrite 0610,c8,0,7
SPIWrite 0611,46,0,7
SPIWrite 0612,1e,0,7
SPIWrite 0613,e0,0,7
SPIWrite 0614,00,0,7
SPIWrite 0615,26,0,7
SPIWrite 0616,4f,0,7
SPIWrite 0617,f0,0,7
SPIWrite 0618,01,0,7
SPIWrite 0619,09,0,7
SPIWrite 061a,37,0,7
SPIWrite 061b,46,0,7
```

```
SPIWrite 061c,0a,0,7
SPIWrite 061d,eb,0,7
SPIWrite 061e,06,0,7
SPIWrite 061f,04,0,7
SPIWrite 0620,00,0,7
SPIWrite 0621,25,0,7
SPIWrite 0622,64,0,7
SPIWrite 0623,1e,0,7
SPIWrite 0624,14,0,7
SPIWrite 0625,f8,0,7
SPIWrite 0626,01,0,7
SPIWrite 0627,0f,0,7
SPIWrite 0628,01,0,7
SPIWrite 0629,28,0,7
SPIWrite 062a,07,0,7
SPIWrite 062b,d1,0,7
SPIWrite 062c,38,0,7
SPIWrite 062d,46,0,7
SPIWrite 062e,29,0,7
SPIWrite 062f,46,0,7
SPIWrite 0630,ff,0,7
SPIWrite 0631,f7,0,7
SPIWrite 0632,31,0,7
SPIWrite 0633,fe,0,7
SPIWrite 0634,01,0,7
SPIWrite 0635,28,0,7
SPIWrite 0636,08,0,7
SPIWrite 0637,bf,0,7
SPIWrite 0638,4f,0,7
SPIWrite 0639,f0,0,7
SPIWrite 063a,00,0,7
SPIWrite 063b,09,0,7
SPIWrite 063c,6d,0,7
SPIWrite 063d,1c,0,7
SPIWrite 063e,03,0,7
SPIWrite 063f,2d,0,7
SPIWrite 0640,f0,0,7
SPIWrite 0641,db,0,7
SPIWrite 0642,7f,0,7
SPIWrite 0643,1c,0,7
SPIWrite 0644,f6,0,7
SPIWrite 0645,1c,0,7
SPIWrite 0646,02,0,7
SPIWrite 0647,2f,0,7
SPIWrite 0648,e8,0,7
SPIWrite 0649,db,0,7
SPIWrite 064a,08,0,7
SPIWrite 064b,f1,0,7
SPIWrite 064c,01,0,7
SPIWrite 064d,00,0,7
SPIWrite 064e,5f,0,7
SPIWrite 064f,fa,0,7
```

```
SPIWrite 0650,80,0,7
SPIWrite 0651,f8,0,7
SPIWrite 0652,58,0,7
SPIWrite 0653,ea,0,7
SPIWrite 0654,09,0,7
SPIWrite 0655,00,0,7
SPIWrite 0656,dd,0,7
SPIWrite 0657,d0,0,7
SPIWrite 0658,bd,0,7
SPIWrite 0659,e8,0,7
SPIWrite 065a,f0,0,7
SPIWrite 065b,87,0,7
SPIWrite 065c,cc,0,7
SPIWrite 065d,22,0,7
SPIWrite 065e,01,0,7
SPIWrite 065f,20,0,7
SPIWrite 0660,e0,0,7
SPIWrite 0661,ab,0,7
SPIWrite 0662,00,0,7
SPIWrite 0663,20,0,7
SPIWrite 0664,b4,0,7
SPIWrite 0665,03,0,7
SPIWrite 0666,00,0,7
SPIWrite 0667,a2,0,7
SPIWrite 0668,68,0,7
SPIWrite 0669,da,0,7
SPIWrite 066a,00,0,7
SPIWrite 066b,20,0,7
SPIWrite 066c,2b,0,7
SPIWrite 066d,fd,0,7
SPIWrite 066e,01,0,7
SPIWrite 066f,00,0,7
SPIWrite 0670,d4,0,7
SPIWrite 0671,f7,0,7
SPIWrite 0672,00,0,7
SPIWrite 0673,20,0,7
SPIWrite 0674,dd,0,7
SPIWrite 0675,34,0,7
SPIWrite 0676,00,0,7
SPIWrite 0677,00,0,7
SPIWrite 0678,29,0,7
SPIWrite 0679,47,0,7
SPIWrite 067a,00,0,7
SPIWrite 067b,00,0,7
SPIWrite 067c,bd,0,7
SPIWrite 067d,3b,0,7
SPIWrite 067e,00,0,7
SPIWrite 067f,00,0,7
SPIWrite 0680,c9,0,7
SPIWrite 0681,3a,0,7
SPIWrite 0682,00,0,7
SPIWrite 0683,00,0,7
```

```
SPIWrite 0684,e5,0,7
SPIWrite 0685,05,0,7
SPIWrite 0686,03,0,7
SPIWrite 0687,00,0,7
SPIWrite 0688,17,0,7
SPIWrite 0689,05,0,7
SPIWrite 068a,03,0,7
SPIWrite 068b,00,0,7
SPIWrite 068c,a9,0,7
SPIWrite 068d,05,0,7
SPIWrite 068e,03,0,7
SPIWrite 068f,00,0,7
SPIWrite 0690,53,0,7
SPIWrite 0691,05,0,7
SPIWrite 0692,03,0,7
SPIWrite 0693,00,0,7
SPIWrite 0694,47,0,7
SPIWrite 0695,05,0,7
SPIWrite 0696,03,0,7
SPIWrite 0697,00,0,7
SPIWrite 0698,00,0,7
SPIWrite 0699,e1,0,7
SPIWrite 069a,00,0,7
SPIWrite 069b,e0,0,7
SPIWrite 069c,22,0,7
SPIWrite 069d,02,0,7
SPIWrite 069e,01,0,7
SPIWrite 069f,20,0,7
SPIWrite 06a0,f8,0,7
SPIWrite 06a1,b5,0,7
SPIWrite 06a2,76,0,7
SPIWrite 06a3,48,0,7
SPIWrite 06a4,77,0,7
SPIWrite 06a5,4b,0,7
SPIWrite 06a6,04,0,7
SPIWrite 06a7,68,0,7
SPIWrite 06a8,44,0,7
SPIWrite 06a9,f0,0,7
SPIWrite 06aa,40,0,7
SPIWrite 06ab,01,0,7
SPIWrite 06ac,d2,0,7
SPIWrite 06ad,4f,0,7
SPIWrite 06ae,01,0,7
SPIWrite 06af,60,0,7
SPIWrite 06b0,1e,0,7
SPIWrite 06b1,68,0,7
SPIWrite 06b2,50,0,7
SPIWrite 06b3,f8,0,7
SPIWrite 06b4,c0,0,7
SPIWrite 06b5,1c,0,7
SPIWrite 06b6,72,0,7
SPIWrite 06b7,48,0,7
```

```
SPIWrite 06b8,00,0,7
SPIWrite 06b9,91,0,7
SPIWrite 06ba,01,0,7
SPIWrite 06bb,68,0,7
SPIWrite 06bc,41,0,7
SPIWrite 06bd,f0,0,7
SPIWrite 06be,01,0,7
SPIWrite 06bf,01,0,7
SPIWrite 06c0,01,0,7
SPIWrite 06c1,60,0,7
SPIWrite 06c2,01,0,7
SPIWrite 06c3,68,0,7
SPIWrite 06c4,00,0,7
SPIWrite 06c5,25,0,7
SPIWrite 06c6,21,0,7
SPIWrite 06c7,f0,0,7
SPIWrite 06c8,02,0,7
SPIWrite 06c9,01,0,7
SPIWrite 06ca,01,0,7
SPIWrite 06cb,60,0,7
SPIWrite 06cc,02,0,7
SPIWrite 06cd,68,0,7
SPIWrite 06ce,3c,0,7
SPIWrite 06cf,60,0,7
SPIWrite 06d0,c6,0,7
SPIWrite 06d1,f3,0,7
SPIWrite 06d2,40,0,7
SPIWrite 06d3,11,0,7
SPIWrite 06d4,01,0,7
SPIWrite 06d5,eb,0,7
SPIWrite 06d6,96,0,7
SPIWrite 06d7,11,0,7
SPIWrite 06d8,42,0,7
SPIWrite 06d9,f0,0,7
SPIWrite 06da,08,0,7
SPIWrite 06db,02,0,7
SPIWrite 06dc,02,0,7
SPIWrite 06dd,60,0,7
SPIWrite 06de,0f,0,7
SPIWrite 06df,e0,0,7
SPIWrite 06e0,21,0,7
SPIWrite 06e1,46,0,7
SPIWrite 06e2,49,0,7
SPIWrite 06e3,1e,0,7
SPIWrite 06e4,fd,0,7
SPIWrite 06e5,d1,0,7
SPIWrite 06e6,00,0,7
SPIWrite 06e7,bf,0,7
SPIWrite 06e8,5b,0,7
SPIWrite 06e9,1c,0,7
SPIWrite 06ea,20,0,7
SPIWrite 06eb,e0,0,7
```

```
SPIWrite 06ec,22,0,7
SPIWrite 06ed,46,0,7
SPIWrite 06ee,52,0,7
SPIWrite 06ef,1e,0,7
SPIWrite 06f0,fd,0,7
SPIWrite 06f1,d1,0,7
SPIWrite 06f2,00,0,7
SPIWrite 06f3,bf,0,7
SPIWrite 06f4,6d,0,7
SPIWrite 06f5,1c,0,7
SPIWrite 06f6,0d,0,7
SPIWrite 06f7,e0,0,7
SPIWrite 06f8,64,0,7
SPIWrite 06f9,1e,0,7
SPIWrite 06fa,fd,0,7
SPIWrite 06fb,d1,0,7
SPIWrite 06fc,00,0,7
SPIWrite 06fd,bf,0,7
SPIWrite 06fe,6d,0,7
SPIWrite 06ff,1c,0,7
SPIWrite 0700,13,0,7
SPIWrite 0701,24,0,7
SPIWrite 0702,a9,0,7
SPIWrite 0703,42,0,7
SPIWrite 0704,c0,0,7
SPIWrite 0705,f2,0,7
SPIWrite 0706,00,0,7
SPIWrite 0707,04,0,7
SPIWrite 0708,f6,0,7
SPIWrite 0709,d8,0,7
SPIWrite 070a,02,0,7
SPIWrite 070b,68,0,7
SPIWrite 070c,00,0,7
SPIWrite 070d,25,0,7
SPIWrite 070e,22,0,7
SPIWrite 070f,f0,0,7
SPIWrite 0710,08,0,7
SPIWrite 0711,02,0,7
SPIWrite 0712,02,0,7
SPIWrite 0713,60,0,7
SPIWrite 0714,a9,0,7
SPIWrite 0715,42,0,7
SPIWrite 0716,e9,0,7
SPIWrite 0717,d8,0,7
SPIWrite 0718,08,0,7
SPIWrite 0719,33,0,7
SPIWrite 071a,01,0,7
SPIWrite 071b,68,0,7
SPIWrite 071c,1d,0,7
SPIWrite 071d,68,0,7
SPIWrite 071e,41,0,7
SPIWrite 071f,f0,0,7
```

```
SPIWrite 0720,02,0,7
SPIWrite 0721,01,0,7
SPIWrite 0722,c5,0,7
SPIWrite 0723,f3,0,7
SPIWrite 0724,40,0,7
SPIWrite 0725,12,0,7
SPIWrite 0726,00,0,7
SPIWrite 0727,23,0,7
SPIWrite 0728,01,0,7
SPIWrite 0729,60,0,7
SPIWrite 072a,02,0,7
SPIWrite 072b,eb,0,7
SPIWrite 072c,95,0,7
SPIWrite 072d,10,0,7
SPIWrite 072e,98,0,7
SPIWrite 072f,42,0,7
SPIWrite 0730,d6,0,7
SPIWrite 0731,d8,0,7
SPIWrite 0732,f8,0,7
SPIWrite 0733,bd,0,7
SPIWrite 0734,52,0,7
SPIWrite 0735,4a,0,7
SPIWrite 0736,c9,0,7
SPIWrite 0737,4b,0,7
SPIWrite 0738,11,0,7
SPIWrite 0739,68,0,7
SPIWrite 073a,06,0,7
SPIWrite 073b,20,0,7
SPIWrite 073c,21,0,7
SPIWrite 073d,f0,0,7
SPIWrite 073e,01,0,7
SPIWrite 073f,01,0,7
SPIWrite 0740,11,0,7
SPIWrite 0741,60,0,7
SPIWrite 0742,53,0,7
SPIWrite 0743,f8,0,7
SPIWrite 0744,04,0,7
SPIWrite 0745,2b,0,7
SPIWrite 0746,d2,0,7
SPIWrite 0747,f8,0,7
SPIWrite 0748,18,0,7
SPIWrite 0749,11,0,7
SPIWrite 074a,40,0,7
SPIWrite 074b,1e,0,7
SPIWrite 074c,21,0,7
SPIWrite 074d,f4,0,7
SPIWrite 074e,00,0,7
SPIWrite 074f,71,0,7
SPIWrite 0750,c2,0,7
SPIWrite 0751,f8,0,7
SPIWrite 0752,18,0,7
SPIWrite 0753,11,0,7
```

```
SPIWrite 0754,f5,0,7
SPIWrite 0755,d1,0,7
SPIWrite 0756,d8,0,7
SPIWrite 0757,48,0,7
SPIWrite 0758,01,0,7
SPIWrite 0759,68,0,7
SPIWrite 075a,4a,0,7
SPIWrite 075b,4a,0,7
SPIWrite 075c,d1,0,7
SPIWrite 075d,f8,0,7
SPIWrite 075e,04,0,7
SPIWrite 075f,05,0,7
SPIWrite 0760,20,0,7
SPIWrite 0761,f0,0,7
SPIWrite 0762,3f,0,7
SPIWrite 0763,00,0,7
SPIWrite 0764,c1,0,7
SPIWrite 0765,f8,0,7
SPIWrite 0766,04,0,7
SPIWrite 0767,05,0,7
SPIWrite 0768,12,0,7
SPIWrite 0769,68,0,7
SPIWrite 076a,00,0,7
SPIWrite 076b,21,0,7
SPIWrite 076c,c2,0,7
SPIWrite 076d,f3,0,7
SPIWrite 076e,40,0,7
SPIWrite 076f,10,0,7
SPIWrite 0770,00,0,7
SPIWrite 0771,eb,0,7
SPIWrite 0772,92,0,7
SPIWrite 0773,10,0,7
SPIWrite 0774,06,0,7
SPIWrite 0775,e0,0,7
SPIWrite 0776,13,0,7
SPIWrite 0777,22,0,7
SPIWrite 0778,c0,0,7
SPIWrite 0779,f2,0,7
SPIWrite 077a,00,0,7
SPIWrite 077b,02,0,7
SPIWrite 077c,52,0,7
SPIWrite 077d,1e,0,7
SPIWrite 077e,fd,0,7
SPIWrite 077f,d1,0,7
SPIWrite 0780,00,0,7
SPIWrite 0781,bf,0,7
SPIWrite 0782,49,0,7
SPIWrite 0783,1c,0,7
SPIWrite 0784,88,0,7
SPIWrite 0785,42,0,7
SPIWrite 0786,f6,0,7
SPIWrite 0787,d8,0,7
```

```
SPIWrite 0788,9b,0,7
SPIWrite 0789,48,0,7
SPIWrite 078a,3c,0,7
SPIWrite 078b,49,0,7
SPIWrite 078c,00,0,7
SPIWrite 078d,68,0,7
SPIWrite 078e,08,0,7
SPIWrite 078f,60,0,7
SPIWrite 0790,70,0,7
SPIWrite 0791,47,0,7
SPIWrite 0792,3b,0,7
SPIWrite 0793,49,0,7
SPIWrite 0794,01,0,7
SPIWrite 0795,28,0,7
SPIWrite 0796,f8,0,7
SPIWrite 0797,b5,0,7
SPIWrite 0798,09,0,7
SPIWrite 0799,d0,0,7
SPIWrite 079a,0a,0,7
SPIWrite 079b,68,0,7
SPIWrite 079c,22,0,7
SPIWrite 079d,f4,0,7
SPIWrite 079e,60,0,7
SPIWrite 079f,02,0,7
SPIWrite 07a0,02,0,7
SPIWrite 07a1,f5,0,7
SPIWrite 07a2,00,0,7
SPIWrite 07a3,12,0,7
SPIWrite 07a4,0a,0,7
SPIWrite 07a5,60,0,7
SPIWrite 07a6,0a,0,7
SPIWrite 07a7,68,0,7
SPIWrite 07a8,22,0,7
SPIWrite 07a9,f4,0,7
SPIWrite 07aa,e0,0,7
SPIWrite 07ab,12,0,7
SPIWrite 07ac,08,0,7
SPIWrite 07ad,e0,0,7
SPIWrite 07ae,0a,0,7
SPIWrite 07af,68,0,7
SPIWrite 07b0,22,0,7
SPIWrite 07b1,f4,0,7
SPIWrite 07b2,60,0,7
SPIWrite 07b3,02,0,7
SPIWrite 07b4,0a,0,7
SPIWrite 07b5,60,0,7
SPIWrite 07b6,0a,0,7
SPIWrite 07b7,68,0,7
SPIWrite 07b8,22,0,7
SPIWrite 07b9,f4,0,7
SPIWrite 07ba,e0,0,7
SPIWrite 07bb,12,0,7
```

```
SPIWrite 07bc,02,0,7
SPIWrite 07bd,f5,0,7
SPIWrite 07be,80,0,7
SPIWrite 07bf,22,0,7
SPIWrite 07c0,30,0,7
SPIWrite 07c1,4d,0,7
SPIWrite 07c2,0a,0,7
SPIWrite 07c3,60,0,7
SPIWrite 07c4,00,0,7
SPIWrite 07c5,23,0,7
SPIWrite 07c6,2a,0,7
SPIWrite 07c7,1d,0,7
SPIWrite 07c8,0b,0,7
SPIWrite 07c9,75,0,7
SPIWrite 07ca,16,0,7
SPIWrite 07cb,68,0,7
SPIWrite 07cc,0c,0,7
SPIWrite 07cd,68,0,7
SPIWrite 07ce,1f,0,7
SPIWrite 07cf,46,0,7
SPIWrite 07d0,c6,0,7
SPIWrite 07d1,f3,0,7
SPIWrite 07d2,40,0,7
SPIWrite 07d3,12,0,7
SPIWrite 07d4,24,0,7
SPIWrite 07d5,f0,0,7
SPIWrite 07d6,02,0,7
SPIWrite 07d7,04,0,7
SPIWrite 07d8,02,0,7
SPIWrite 07d9,eb,0,7
SPIWrite 07da,96,0,7
SPIWrite 07db,12,0,7
SPIWrite 07dc,0c,0,7
SPIWrite 07dd,60,0,7
SPIWrite 07de,0f,0,7
SPIWrite 07df,e0,0,7
SPIWrite 07e0,34,0,7
SPIWrite 07e1,46,0,7
SPIWrite 07e2,64,0,7
SPIWrite 07e3,1e,0,7
SPIWrite 07e4,fd,0,7
SPIWrite 07e5,d1,0,7
SPIWrite 07e6,00,0,7
SPIWrite 07e7,bf,0,7
SPIWrite 07e8,5b,0,7
SPIWrite 07e9,1c,0,7
SPIWrite 07ea,1d,0,7
SPIWrite 07eb,e0,0,7
SPIWrite 07ec,37,0,7
SPIWrite 07ed,46,0,7
SPIWrite 07ee,7f,0,7
SPIWrite 07ef,1e,0,7
```

```
SPIWrite 07f0,fd,0,7
SPIWrite 07f1,d1,0,7
SPIWrite 07f2,00,0,7
SPIWrite 07f3,bf,0,7
SPIWrite 07f4,6d,0,7
SPIWrite 07f5,1c,0,7
SPIWrite 07f6,13,0,7
SPIWrite 07f7,e0,0,7
SPIWrite 07f8,76,0,7
SPIWrite 07f9,1e,0,7
SPIWrite 07fa,fd,0,7
SPIWrite 07fb,d1,0,7
SPIWrite 07fc,00,0,7
SPIWrite 07fd,bf,0,7
SPIWrite 07fe,7f,0,7
SPIWrite 07ff,1c,0,7
SPIWrite 0800,13,0,7
SPIWrite 0801,26,0,7
SPIWrite 0802,ba,0,7
SPIWrite 0803,42,0,7
SPIWrite 0804,c0,0,7
SPIWrite 0805,f2,0,7
SPIWrite 0806,00,0,7
SPIWrite 0807,06,0,7
SPIWrite 0808,f6,0,7
SPIWrite 0809,d8,0,7
SPIWrite 080a,08,0,7
SPIWrite 080b,35,0,7
SPIWrite 080c,0c,0,7
SPIWrite 080d,68,0,7
SPIWrite 080e,2f,0,7
SPIWrite 080f,68,0,7
SPIWrite 0810,44,0,7
SPIWrite 0811,f0,0,7
SPIWrite 0812,02,0,7
SPIWrite 0813,04,0,7
SPIWrite 0814,c7,0,7
SPIWrite 0815,f3,0,7
SPIWrite 0816,40,0,7
SPIWrite 0817,1c,0,7
SPIWrite 0818,1d,0,7
SPIWrite 0819,46,0,7
SPIWrite 081a,0c,0,7
SPIWrite 081b,60,0,7
SPIWrite 081c,0c,0,7
SPIWrite 081d,eb,0,7
SPIWrite 081e,97,0,7
SPIWrite 081f,14,0,7
SPIWrite 0018,00,0,7  //Property_18h_0_0=0x0;
     Address(0x18[7:0])
SPIWrite 0018,20,0,7  //macro=0x1;     Address(0x18[7:5])
SPIRead 00f0,0,0
```

```
//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,08,0,7  //MACRO_OPERAND_REG0=0x8000000;
     Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00,0,7
SPIWrite 00a1,00,0,7
SPIWrite 00a0,00,0,7
SPIWrite 00a7,00,0,7  //MACRO_OPERAND_REG1=0x0;
     Address(0xa4[7:0],0xa5[7:0],0xa6[7:0],0xa7[7:0],0xa8[7:0])
SPIWrite 00a6,00,0,7
SPIWrite 00a5,00,0,7
SPIWrite 00a4,00,0,7
SPIWrite 0193,78,0,7  //MACRO_OPCODE=0x78;
     Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
     Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
     Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])
```

```
SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIWrite 0144,00,0,7  //Property_124h_4_2=0x0;
      Address(0x144[7:2])
SPIWrite 0018,00,0,7  //macro=0x0;     Address(0x18[7:5])
SPIWrite 0018,01,0,7  //Property_18h_0_0=0x1;
      Address(0x18[7:0])
SPIWrite 0020,ac,0,7
SPIWrite 0021,42,0,7
SPIWrite 0022,e3,0,7
SPIWrite 0023,d8,0,7
SPIWrite 0024,01,0,7
SPIWrite 0025,24,0,7
SPIWrite 0026,0c,0,7
SPIWrite 0027,75,0,7
SPIWrite 0028,9a,0,7
SPIWrite 0029,42,0,7
SPIWrite 002a,d9,0,7
SPIWrite 002b,d8,0,7
SPIWrite 002c,b1,0,7
SPIWrite 002d,f9,0,7
SPIWrite 002e,10,0,7
SPIWrite 002f,10,0,7
SPIWrite 0030,01,0,7
SPIWrite 0031,28,0,7
SPIWrite 0032,0c,0,7
SPIWrite 0033,bf,0,7
SPIWrite 0034,c1,0,7
SPIWrite 0035,f5,0,7
SPIWrite 0036,40,0,7
SPIWrite 0037,61,0,7
SPIWrite 0038,a1,0,7
SPIWrite 0039,f5,0,7
SPIWrite 003a,80,0,7
SPIWrite 003b,61,0,7
SPIWrite 003c,08,0,7
SPIWrite 003d,b2,0,7
SPIWrite 003e,f8,0,7
SPIWrite 003f,bd,0,7
```

```
SPIWrite 0040,af,0,7
SPIWrite 0041,4a,0,7
SPIWrite 0042,b2,0,7
SPIWrite 0043,f9,0,7
SPIWrite 0044,00,0,7
SPIWrite 0045,20,0,7
SPIWrite 0046,48,0,7
SPIWrite 0047,43,0,7
SPIWrite 0048,00,0,7
SPIWrite 0049,28,0,7
SPIWrite 004a,cc,0,7
SPIWrite 004b,bf,0,7
SPIWrite 004c,00,0,7
SPIWrite 004d,eb,0,7
SPIWrite 004e,62,0,7
SPIWrite 004f,00,0,7
SPIWrite 0050,a0,0,7
SPIWrite 0051,eb,0,7
SPIWrite 0052,62,0,7
SPIWrite 0053,00,0,7
SPIWrite 0054,90,0,7
SPIWrite 0055,fb,0,7
SPIWrite 0056,f2,0,7
SPIWrite 0057,f0,0,7
SPIWrite 0058,70,0,7
SPIWrite 0059,47,0,7
SPIWrite 005a,03,0,7
SPIWrite 005b,46,0,7
SPIWrite 005c,00,0,7
SPIWrite 005d,28,0,7
SPIWrite 005e,b8,0,7
SPIWrite 005f,bf,0,7
SPIWrite 0060,40,0,7
SPIWrite 0061,42,0,7
SPIWrite 0062,49,0,7
SPIWrite 0063,b2,0,7
SPIWrite 0064,01,0,7
SPIWrite 0065,22,0,7
SPIWrite 0066,49,0,7
SPIWrite 0067,1e,0,7
SPIWrite 0068,c9,0,7
SPIWrite 0069,b2,0,7
SPIWrite 006a,8a,0,7
SPIWrite 006b,40,0,7
SPIWrite 006c,51,0,7
SPIWrite 006d,1e,0,7
SPIWrite 006e,81,0,7
SPIWrite 006f,42,0,7
SPIWrite 0070,38,0,7
SPIWrite 0071,bf,0,7
SPIWrite 0072,08,0,7
SPIWrite 0073,1c,0,7
```

```
SPIWrite 0074,00,0,7
SPIWrite 0075,2b,0,7
SPIWrite 0076,48,0,7
SPIWrite 0077,bf,0,7
SPIWrite 0078,10,0,7
SPIWrite 0079,44,0,7
SPIWrite 007a,70,0,7
SPIWrite 007b,47,0,7
SPIWrite 007c,c0,0,7
SPIWrite 007d,00,0,7
SPIWrite 007e,03,0,7
SPIWrite 007f,ad,0,7
SPIWrite 0080,00,0,7
SPIWrite 0081,05,0,7
SPIWrite 0082,02,0,7
SPIWrite 0083,ac,0,7
SPIWrite 0084,ac,0,7
SPIWrite 0085,22,0,7
SPIWrite 0086,01,0,7
SPIWrite 0087,20,0,7
SPIWrite 0088,2d,0,7
SPIWrite 0089,e9,0,7
SPIWrite 008a,f0,0,7
SPIWrite 008b,4f,0,7
SPIWrite 008c,df,0,7
SPIWrite 008d,f8,0,7
SPIWrite 008e,74,0,7
SPIWrite 008f,82,0,7
SPIWrite 0090,d8,0,7
SPIWrite 0091,f8,0,7
SPIWrite 0092,00,0,7
SPIWrite 0093,32,0,7
SPIWrite 0094,0c,0,7
SPIWrite 0095,46,0,7
SPIWrite 0096,81,0,7
SPIWrite 0097,46,0,7
SPIWrite 0098,01,0,7
SPIWrite 0099,21,0,7
SPIWrite 009a,00,0,7
SPIWrite 009b,20,0,7
SPIWrite 009c,0a,0,7
SPIWrite 009d,46,0,7
SPIWrite 009e,ad,0,7
SPIWrite 009f,f1,0,7
SPIWrite 00a0,1c,0,7
SPIWrite 00a1,0d,0,7
SPIWrite 00a2,98,0,7
SPIWrite 00a3,47,0,7
SPIWrite 00a4,ff,0,7
SPIWrite 00a5,f7,0,7
SPIWrite 00a6,fc,0,7
SPIWrite 00a7,fe,0,7
```

```
SPIWrite 00a8,48,0,7
SPIWrite 00a9,46,0,7
SPIWrite 00aa,00,0,7
SPIWrite 00ab,2c,0,7
SPIWrite 00ac,05,0,7
SPIWrite 00ad,94,0,7
SPIWrite 00ae,00,0,7
SPIWrite 00af,f0,0,7
SPIWrite 00b0,f7,0,7
SPIWrite 00b1,80,0,7
SPIWrite 00b2,df,0,7
SPIWrite 00b3,f8,0,7
SPIWrite 00b4,54,0,7
SPIWrite 00b5,82,0,7
SPIWrite 00b6,95,0,7
SPIWrite 00b7,4f,0,7
SPIWrite 00b8,40,0,7
SPIWrite 00b9,1e,0,7
SPIWrite 00ba,4f,0,7
SPIWrite 00bb,f0,0,7
SPIWrite 00bc,00,0,7
SPIWrite 00bd,0b,0,7
SPIWrite 00be,04,0,7
SPIWrite 00bf,90,0,7
SPIWrite 00c0,04,0,7
SPIWrite 00c1,98,0,7
SPIWrite 00c2,66,0,7
SPIWrite 00c3,4b,0,7
SPIWrite 00c4,03,0,7
SPIWrite 00c5,25,0,7
SPIWrite 00c6,06,0,7
SPIWrite 00c7,26,0,7
SPIWrite 00c8,10,0,7
SPIWrite 00c9,f8,0,7
SPIWrite 00ca,01,0,7
SPIWrite 00cb,cf,0,7
SPIWrite 00cc,04,0,7
SPIWrite 00cd,90,0,7
SPIWrite 00ce,9c,0,7
SPIWrite 00cf,fb,0,7
SPIWrite 00d0,f5,0,7
SPIWrite 00d1,f2,0,7
SPIWrite 00d2,53,0,7
SPIWrite 00d3,f8,0,7
SPIWrite 00d4,04,0,7
SPIWrite 00d5,1b,0,7
SPIWrite 00d6,d1,0,7
SPIWrite 00d7,f8,0,7
SPIWrite 00d8,18,0,7
SPIWrite 00d9,01,0,7
SPIWrite 00da,20,0,7
SPIWrite 00db,f4,0,7
```

```
SPIWrite 00dc,00,0,7
SPIWrite 00dd,70,0,7
SPIWrite 00de,c1,0,7
SPIWrite 00df,f8,0,7
SPIWrite 00e0,18,0,7
SPIWrite 00e1,01,0,7
SPIWrite 00e2,08,0,7
SPIWrite 00e3,6e,0,7
SPIWrite 00e4,76,0,7
SPIWrite 00e5,1e,0,7
SPIWrite 00e6,20,0,7
SPIWrite 00e7,f0,0,7
SPIWrite 00e8,00,0,7
SPIWrite 00e9,70,0,7
SPIWrite 00ea,08,0,7
SPIWrite 00eb,66,0,7
SPIWrite 00ec,f1,0,7
SPIWrite 00ed,d1,0,7
SPIWrite 00ee,5b,0,7
SPIWrite 00ef,48,0,7
SPIWrite 00f0,50,0,7
SPIWrite 00f1,f8,0,7
SPIWrite 00f2,2c,0,7
SPIWrite 00f3,40,0,7
SPIWrite 00f4,d4,0,7
SPIWrite 00f5,f8,0,7
SPIWrite 00f6,18,0,7
SPIWrite 00f7,01,0,7
SPIWrite 00f8,40,0,7
SPIWrite 00f9,f4,0,7
SPIWrite 00fa,00,0,7
SPIWrite 00fb,70,0,7
SPIWrite 00fc,c4,0,7
SPIWrite 00fd,f8,0,7
SPIWrite 00fe,18,0,7
SPIWrite 00ff,01,0,7
SPIWrite 0100,20,0,7
SPIWrite 0101,6e,0,7
SPIWrite 0102,40,0,7
SPIWrite 0103,f0,0,7
SPIWrite 0104,80,0,7
SPIWrite 0105,60,0,7
SPIWrite 0106,20,0,7
SPIWrite 0107,66,0,7
SPIWrite 0108,20,0,7
SPIWrite 0109,68,0,7
SPIWrite 010a,01,0,7
SPIWrite 010b,2a,0,7
SPIWrite 010c,00,0,7
SPIWrite 010d,90,0,7
SPIWrite 010e,0c,0,7
SPIWrite 010f,d0,0,7
```

```
SPIWrite 0110,d8,0,7
SPIWrite 0111,f8,0,7
SPIWrite 0112,00,0,7
SPIWrite 0113,00,0,7
SPIWrite 0114,20,0,7
SPIWrite 0115,f0,0,7
SPIWrite 0116,38,0,7
SPIWrite 0117,00,0,7
SPIWrite 0118,38,0,7
SPIWrite 0119,30,0,7
SPIWrite 011a,c8,0,7
SPIWrite 011b,f8,0,7
SPIWrite 011c,00,0,7
SPIWrite 011d,00,0,7
SPIWrite 011e,d8,0,7
SPIWrite 011f,f8,0,7
SPIWrite 0120,00,0,7
SPIWrite 0121,00,0,7
SPIWrite 0122,20,0,7
SPIWrite 0123,f0,0,7
SPIWrite 0124,07,0,7
SPIWrite 0125,00,0,7
SPIWrite 0126,c0,0,7
SPIWrite 0127,1d,0,7
SPIWrite 0128,0b,0,7
SPIWrite 0129,e0,0,7
SPIWrite 012a,d8,0,7
SPIWrite 012b,f8,0,7
SPIWrite 012c,00,0,7
SPIWrite 012d,00,0,7
SPIWrite 012e,20,0,7
SPIWrite 012f,f0,0,7
SPIWrite 0130,38,0,7
SPIWrite 0131,00,0,7
SPIWrite 0132,30,0,7
SPIWrite 0133,30,0,7
SPIWrite 0134,c8,0,7
SPIWrite 0135,f8,0,7
SPIWrite 0136,00,0,7
SPIWrite 0137,00,0,7
SPIWrite 0138,d8,0,7
SPIWrite 0139,f8,0,7
SPIWrite 013a,00,0,7
SPIWrite 013b,00,0,7
SPIWrite 013c,20,0,7
SPIWrite 013d,f0,0,7
SPIWrite 013e,07,0,7
SPIWrite 013f,00,0,7
SPIWrite 0140,80,0,7
SPIWrite 0141,1d,0,7
SPIWrite 0142,c8,0,7
SPIWrite 0143,f8,0,7
```

```
SPIWrite 0144,00,0,7
SPIWrite 0145,00,0,7
SPIWrite 0146,00,0,7
SPIWrite 0147,20,0,7
SPIWrite 0148,ff,0,7
SPIWrite 0149,f7,0,7
SPIWrite 014a,23,0,7
SPIWrite 014b,ff,0,7
SPIWrite 014c,05,0,7
SPIWrite 014d,46,0,7
SPIWrite 014e,01,0,7
SPIWrite 014f,20,0,7
SPIWrite 0150,ff,0,7
SPIWrite 0151,f7,0,7
SPIWrite 0152,1f,0,7
SPIWrite 0153,ff,0,7
SPIWrite 0154,28,0,7
SPIWrite 0155,49,0,7
SPIWrite 0156,4d,0,7
SPIWrite 0157,60,0,7
SPIWrite 0158,0e,0,7
SPIWrite 0159,46,0,7
SPIWrite 015a,b0,0,7
SPIWrite 015b,60,0,7
SPIWrite 015c,21,0,7
SPIWrite 015d,6e,0,7
SPIWrite 015e,21,0,7
SPIWrite 015f,f0,0,7
SPIWrite 0160,80,0,7
SPIWrite 0161,61,0,7
SPIWrite 0162,21,0,7
SPIWrite 0163,66,0,7
SPIWrite 0164,21,0,7
SPIWrite 0165,6e,0,7
SPIWrite 0166,41,0,7
SPIWrite 0167,f0,0,7
SPIWrite 0168,00,0,7
SPIWrite 0169,71,0,7
SPIWrite 016a,21,0,7
SPIWrite 016b,66,0,7
SPIWrite 016c,61,0,7
SPIWrite 016d,6e,0,7
SPIWrite 016e,43,0,7
SPIWrite 016f,19,0,7
SPIWrite 0170,4f,0,7
SPIWrite 0171,ea,0,7
SPIWrite 0172,63,0,7
SPIWrite 0173,0a,0,7
SPIWrite 0174,00,0,7
SPIWrite 0175,26,0,7
SPIWrite 0176,c1,0,7
SPIWrite 0177,f3,0,7
```

```
SPIWrite 0178,c0,0,7
SPIWrite 0179,45,0,7
SPIWrite 017a,00,0,7
SPIWrite 017b,2d,0,7
SPIWrite 017c,5d,0,7
SPIWrite 017d,d1,0,7
SPIWrite 017e,35,0,7
SPIWrite 017f,46,0,7
SPIWrite 0180,b1,0,7
SPIWrite 0181,46,0,7
SPIWrite 0182,23,0,7
SPIWrite 0183,e0,0,7
SPIWrite 0184,28,0,7
SPIWrite 0185,46,0,7
SPIWrite 0186,ff,0,7
SPIWrite 0187,f7,0,7
SPIWrite 0188,04,0,7
SPIWrite 0189,ff,0,7
SPIWrite 018a,b7,0,7
SPIWrite 018b,f9,0,7
SPIWrite 018c,00,0,7
SPIWrite 018d,10,0,7
SPIWrite 018e,aa,0,7
SPIWrite 018f,eb,0,7
SPIWrite 0190,00,0,7
SPIWrite 0191,00,0,7
SPIWrite 0192,ff,0,7
SPIWrite 0193,f7,0,7
SPIWrite 0194,55,0,7
SPIWrite 0195,ff,0,7
SPIWrite 0196,36,0,7
SPIWrite 0197,1a,0,7
SPIWrite 0198,03,0,7
SPIWrite 0199,d4,0,7
SPIWrite 019a,10,0,7
SPIWrite 019b,2e,0,7
SPIWrite 019c,a8,0,7
SPIWrite 019d,bf,0,7
SPIWrite 019e,0f,0,7
SPIWrite 019f,26,0,7
SPIWrite 01a0,04,0,7
SPIWrite 01a1,e0,0,7
SPIWrite 01a2,16,0,7
SPIWrite 01a3,f1,0,7
SPIWrite 01a4,0f,0,7
SPIWrite 01a5,0f,0,7
SPIWrite 01a6,b8,0,7
SPIWrite 01a7,bf,0,7
SPIWrite 01a8,6f,0,7
SPIWrite 01a9,f0,0,7
SPIWrite 01aa,0e,0,7
SPIWrite 01ab,06,0,7
```

```
SPIWrite 01ac,30,0,7
SPIWrite 01ad,46,0,7
SPIWrite 01ae,05,0,7
SPIWrite 01af,21,0,7
SPIWrite 01b0,ff,0,7
SPIWrite 01b1,f7,0,7
SPIWrite 01b2,53,0,7
SPIWrite 01b3,ff,0,7
SPIWrite 01b4,d4,0,7
SPIWrite 01b5,f8,0,7
SPIWrite 01b6,80,0,7
SPIWrite 01b7,10,0,7
SPIWrite 01b8,60,0,7
SPIWrite 01b9,f3,0,7
SPIWrite 01ba,1c,0,7
SPIWrite 01bb,61,0,7
SPIWrite 01bc,c4,0,7
SPIWrite 01bd,f8,0,7
SPIWrite 01be,80,0,7
SPIWrite 01bf,10,0,7
SPIWrite 01c0,20,0,7
SPIWrite 01c1,68,0,7
SPIWrite 01c2,09,0,7
SPIWrite 01c3,f1,0,7
SPIWrite 01c4,01,0,7
SPIWrite 01c5,03,0,7
SPIWrite 01c6,5f,0,7
SPIWrite 01c7,fa,0,7
SPIWrite 01c8,83,0,7
SPIWrite 01c9,f9,0,7
SPIWrite 01ca,01,0,7
SPIWrite 01cb,90,0,7
SPIWrite 01cc,b8,0,7
SPIWrite 01cd,79,0,7
SPIWrite 01ce,48,0,7
SPIWrite 01cf,45,0,7
SPIWrite 01d0,d8,0,7
SPIWrite 01d1,dc,0,7
SPIWrite 01d2,2e,0,7
SPIWrite 01d3,46,0,7
SPIWrite 01d4,b0,0,7
SPIWrite 01d5,42,0,7
SPIWrite 01d6,59,0,7
SPIWrite 01d7,dd,0,7
SPIWrite 01d8,01,0,7
SPIWrite 01d9,20,0,7
SPIWrite 01da,ff,0,7
SPIWrite 01db,f7,0,7
SPIWrite 01dc,da,0,7
SPIWrite 01dd,fe,0,7
SPIWrite 01de,b7,0,7
SPIWrite 01df,f9,0,7
```

```
SPIWrite 01e0,02,0,7
SPIWrite 01e1,10,0,7
SPIWrite 01e2,aa,0,7
SPIWrite 01e3,eb,0,7
SPIWrite 01e4,00,0,7
SPIWrite 01e5,00,0,7
SPIWrite 01e6,ff,0,7
SPIWrite 01e7,f7,0,7
SPIWrite 01e8,2b,0,7
SPIWrite 01e9,ff,0,7
SPIWrite 01ea,45,0,7
SPIWrite 01eb,19,0,7
SPIWrite 01ec,06,0,7
SPIWrite 01ed,d4,0,7
SPIWrite 01ee,08,0,7
SPIWrite 01ef,2d,0,7
SPIWrite 01f0,a8,0,7
SPIWrite 01f1,bf,0,7
SPIWrite 01f2,07,0,7
SPIWrite 01f3,25,0,7
SPIWrite 01f4,07,0,7
SPIWrite 01f5,e0,0,7
SPIWrite 01f6,c0,0,7
SPIWrite 01f7,46,0,7
SPIWrite 01f8,b8,0,7
SPIWrite 01f9,22,0,7
SPIWrite 01fa,01,0,7
SPIWrite 01fb,20,0,7
SPIWrite 01fc,15,0,7
SPIWrite 01fd,f1,0,7
SPIWrite 01fe,07,0,7
SPIWrite 01ff,0f,0,7
SPIWrite 0200,b8,0,7
SPIWrite 0201,bf,0,7
SPIWrite 0202,6f,0,7
SPIWrite 0203,f0,0,7
SPIWrite 0204,06,0,7
SPIWrite 0205,05,0,7
SPIWrite 0206,00,0,7
SPIWrite 0207,21,0,7
SPIWrite 0208,00,0,7
SPIWrite 0209,2d,0,7
SPIWrite 020a,d8,0,7
SPIWrite 020b,bf,0,7
SPIWrite 020c,01,0,7
SPIWrite 020d,21,0,7
SPIWrite 020e,20,0,7
SPIWrite 020f,6f,0,7
SPIWrite 0210,20,0,7
SPIWrite 0211,f4,0,7
SPIWrite 0212,00,0,7
SPIWrite 0213,50,0,7
```

```
SPIWrite 0214,40,0,7
SPIWrite 0215,ea,0,7
SPIWrite 0216,41,0,7
SPIWrite 0217,30,0,7
SPIWrite 0218,20,0,7
SPIWrite 0219,67,0,7
SPIWrite 021a,29,0,7
SPIWrite 021b,46,0,7
SPIWrite 021c,00,0,7
SPIWrite 021d,29,0,7
SPIWrite 021e,b8,0,7
SPIWrite 021f,bf,0,7
SPIWrite 0220,49,0,7
SPIWrite 0221,42,0,7
SPIWrite 0222,d4,0,7
SPIWrite 0223,f8,0,7
SPIWrite 0224,84,0,7
SPIWrite 0225,00,0,7
SPIWrite 0226,61,0,7
SPIWrite 0227,f3,0,7
SPIWrite 0228,8c,0,7
SPIWrite 0229,20,0,7
SPIWrite 022a,c4,0,7
SPIWrite 022b,f8,0,7
SPIWrite 022c,84,0,7
SPIWrite 022d,00,0,7
SPIWrite 022e,b8,0,7
SPIWrite 022f,79,0,7
SPIWrite 0230,21,0,7
SPIWrite 0231,68,0,7
SPIWrite 0232,76,0,7
SPIWrite 0233,1c,0,7
SPIWrite 0234,f6,0,7
SPIWrite 0235,b2,0,7
SPIWrite 0236,02,0,7
SPIWrite 0237,91,0,7
SPIWrite 0238,cc,0,7
SPIWrite 0239,e7,0,7
SPIWrite 023a,35,0,7
SPIWrite 023b,46,0,7
SPIWrite 023c,23,0,7
SPIWrite 023d,e0,0,7
SPIWrite 023e,01,0,7
SPIWrite 023f,20,0,7
SPIWrite 0240,ff,0,7
SPIWrite 0241,f7,0,7
SPIWrite 0242,a7,0,7
SPIWrite 0243,fe,0,7
SPIWrite 0244,b7,0,7
SPIWrite 0245,f9,0,7
SPIWrite 0246,00,0,7
SPIWrite 0247,10,0,7
```

```
SPIWrite 0248,aa,0,7
SPIWrite 0249,eb,0,7
SPIWrite 024a,00,0,7
SPIWrite 024b,00,0,7
SPIWrite 024c,ff,0,7
SPIWrite 024d,f7,0,7
SPIWrite 024e,f8,0,7
SPIWrite 024f,fe,0,7
SPIWrite 0250,36,0,7
SPIWrite 0251,1a,0,7
SPIWrite 0252,05,0,7
SPIWrite 0253,d4,0,7
SPIWrite 0254,10,0,7
SPIWrite 0255,2e,0,7
SPIWrite 0256,a8,0,7
SPIWrite 0257,bf,0,7
SPIWrite 0258,0f,0,7
SPIWrite 0259,26,0,7
SPIWrite 025a,06,0,7
SPIWrite 025b,e0,0,7
SPIWrite 025c,c0,0,7
SPIWrite 025d,75,0,7
SPIWrite 025e,02,0,7
SPIWrite 025f,00,0,7
SPIWrite 0260,16,0,7
SPIWrite 0261,f1,0,7
SPIWrite 0262,0f,0,7
SPIWrite 0263,0f,0,7
SPIWrite 0264,b8,0,7
SPIWrite 0265,bf,0,7
SPIWrite 0266,6f,0,7
SPIWrite 0267,f0,0,7
SPIWrite 0268,0e,0,7
SPIWrite 0269,06,0,7
SPIWrite 026a,30,0,7
SPIWrite 026b,46,0,7
SPIWrite 026c,05,0,7
SPIWrite 026d,21,0,7
SPIWrite 026e,ff,0,7
SPIWrite 026f,f7,0,7
SPIWrite 0270,f4,0,7
SPIWrite 0271,fe,0,7
SPIWrite 0272,d4,0,7
SPIWrite 0273,f8,0,7
SPIWrite 0274,80,0,7
SPIWrite 0275,10,0,7
SPIWrite 0276,60,0,7
SPIWrite 0277,f3,0,7
SPIWrite 0278,1c,0,7
SPIWrite 0279,61,0,7
SPIWrite 027a,c4,0,7
SPIWrite 027b,f8,0,7
```

```
SPIWrite 027c,80,0,7
SPIWrite 027d,10,0,7
SPIWrite 027e,20,0,7
SPIWrite 027f,68,0,7
SPIWrite 0280,6d,0,7
SPIWrite 0281,1c,0,7
SPIWrite 0282,ed,0,7
SPIWrite 0283,b2,0,7
SPIWrite 0284,03,0,7
SPIWrite 0285,90,0,7
SPIWrite 0286,b8,0,7
SPIWrite 0287,79,0,7
SPIWrite 0288,a8,0,7
SPIWrite 0289,42,0,7
SPIWrite 028a,d8,0,7
SPIWrite 028b,dc,0,7
SPIWrite 028c,20,0,7
SPIWrite 028d,6e,0,7
SPIWrite 028e,05,0,7
SPIWrite 028f,9e,0,7
SPIWrite 0290,0b,0,7
SPIWrite 0291,f1,0,7
SPIWrite 0292,01,0,7
SPIWrite 0293,0b,0,7
SPIWrite 0294,20,0,7
SPIWrite 0295,f0,0,7
SPIWrite 0296,00,0,7
SPIWrite 0297,70,0,7
SPIWrite 0298,5e,0,7
SPIWrite 0299,45,0,7
SPIWrite 029a,20,0,7
SPIWrite 029b,66,0,7
SPIWrite 029c,3f,0,7
SPIWrite 029d,f7,0,7
SPIWrite 029e,10,0,7
SPIWrite 029f,af,0,7
SPIWrite 02a0,ff,0,7
SPIWrite 02a1,f7,0,7
SPIWrite 02a2,48,0,7
SPIWrite 02a3,fe,0,7
SPIWrite 02a4,17,0,7
SPIWrite 02a5,48,0,7
SPIWrite 02a6,d0,0,7
SPIWrite 02a7,f8,0,7
SPIWrite 02a8,04,0,7
SPIWrite 02a9,32,0,7
SPIWrite 02aa,01,0,7
SPIWrite 02ab,21,0,7
SPIWrite 02ac,0a,0,7
SPIWrite 02ad,46,0,7
SPIWrite 02ae,00,0,7
SPIWrite 02af,20,0,7
```

```
SPIWrite 02b0,98,0,7
SPIWrite 02b1,47,0,7
SPIWrite 02b2,07,0,7
SPIWrite 02b3,b0,0,7
SPIWrite 02b4,bd,0,7
SPIWrite 02b5,e8,0,7
SPIWrite 02b6,f0,0,7
SPIWrite 02b7,8f,0,7
SPIWrite 02b8,ec,0,7
SPIWrite 02b9,22,0,7
SPIWrite 02ba,01,0,7
SPIWrite 02bb,20,0,7
SPIWrite 02bc,01,0,7
SPIWrite 02bd,22,0,7
SPIWrite 02be,49,0,7
SPIWrite 02bf,1e,0,7
SPIWrite 02c0,8a,0,7
SPIWrite 02c1,40,0,7
SPIWrite 02c2,01,0,7
SPIWrite 02c3,46,0,7
SPIWrite 02c4,50,0,7
SPIWrite 02c5,1e,0,7
SPIWrite 02c6,11,0,7
SPIWrite 02c7,42,0,7
SPIWrite 02c8,01,0,7
SPIWrite 02c9,ea,0,7
SPIWrite 02ca,00,0,7
SPIWrite 02cb,00,0,7
SPIWrite 02cc,18,0,7
SPIWrite 02cd,bf,0,7
SPIWrite 02ce,40,0,7
SPIWrite 02cf,42,0,7
SPIWrite 02d0,70,0,7
SPIWrite 02d1,47,0,7
SPIWrite 02d2,01,0,7
SPIWrite 02d3,46,0,7
SPIWrite 02d4,1c,0,7
SPIWrite 02d5,b5,0,7
SPIWrite 02d6,00,0,7
SPIWrite 02d7,20,0,7
SPIWrite 02d8,01,0,7
SPIWrite 02d9,24,0,7
SPIWrite 02da,02,0,7
SPIWrite 02db,46,0,7
SPIWrite 02dc,04,0,7
SPIWrite 02dd,fa,0,7
SPIWrite 02de,02,0,7
SPIWrite 02df,f3,0,7
SPIWrite 02e0,19,0,7
SPIWrite 02e1,42,0,7
SPIWrite 02e2,03,0,7
SPIWrite 02e3,d0,0,7
```

```
SPIWrite 02e4,43,0,7
SPIWrite 02e5,1c,0,7
SPIWrite 02e6,00,0,7
SPIWrite 02e7,f8,0,7
SPIWrite 02e8,0d,0,7
SPIWrite 02e9,20,0,7
SPIWrite 02ea,d8,0,7
SPIWrite 02eb,b2,0,7
SPIWrite 02ec,52,0,7
SPIWrite 02ed,1c,0,7
SPIWrite 02ee,06,0,7
SPIWrite 02ef,2a,0,7
SPIWrite 02f0,f4,0,7
SPIWrite 02f1,db,0,7
SPIWrite 02f2,18,0,7
SPIWrite 02f3,b1,0,7
SPIWrite 02f4,01,0,7
SPIWrite 02f5,46,0,7
SPIWrite 02f6,68,0,7
SPIWrite 02f7,46,0,7
SPIWrite 02f8,ff,0,7
SPIWrite 02f9,f7,0,7
SPIWrite 02fa,c6,0,7
SPIWrite 02fb,fe,0,7
SPIWrite 02fc,1c,0,7
SPIWrite 02fd,bd,0,7
SPIWrite 02fe,c0,0,7
SPIWrite 02ff,46,0,7
SPIWrite 0300,a8,0,7
SPIWrite 0301,22,0,7
SPIWrite 0302,01,0,7
SPIWrite 0303,20,0,7
SPIWrite 0304,90,0,7
SPIWrite 0305,d6,0,7
SPIWrite 0306,00,0,7
SPIWrite 0307,20,0,7
SPIWrite 0308,04,0,7
SPIWrite 0309,05,0,7
SPIWrite 030a,02,0,7
SPIWrite 030b,ac,0,7
SPIWrite 030c,a4,0,7
SPIWrite 030d,22,0,7
SPIWrite 030e,01,0,7
SPIWrite 030f,20,0,7
SPIWrite 0310,38,0,7
SPIWrite 0311,b5,0,7
SPIWrite 0312,ce,0,7
SPIWrite 0313,4c,0,7
SPIWrite 0314,0c,0,7
SPIWrite 0315,25,0,7
SPIWrite 0316,10,0,7
SPIWrite 0317,fb,0,7
```

```
SPIWrite 0318,05,0,7
SPIWrite 0319,f0,0,7
SPIWrite 031a,00,0,7
SPIWrite 031b,eb,0,7
SPIWrite 031c,81,0,7
SPIWrite 031d,00,0,7
SPIWrite 031e,20,0,7
SPIWrite 031f,58,0,7
SPIWrite 0320,01,0,7
SPIWrite 0321,2b,0,7
SPIWrite 0322,06,0,7
SPIWrite 0323,d0,0,7
SPIWrite 0324,51,0,7
SPIWrite 0325,78,0,7
SPIWrite 0326,80,0,7
SPIWrite 0327,f8,0,7
SPIWrite 0328,a0,0,7
SPIWrite 0329,14,0,7
SPIWrite 032a,11,0,7
SPIWrite 032b,78,0,7
SPIWrite 032c,80,0,7
SPIWrite 032d,f8,0,7
SPIWrite 032e,aa,0,7
SPIWrite 032f,14,0,7
SPIWrite 0330,38,0,7
SPIWrite 0331,bd,0,7
SPIWrite 0332,11,0,7
SPIWrite 0333,78,0,7
SPIWrite 0334,80,0,7
SPIWrite 0335,f8,0,7
SPIWrite 0336,aa,0,7
SPIWrite 0337,14,0,7
SPIWrite 0338,51,0,7
SPIWrite 0339,78,0,7
SPIWrite 033a,80,0,7
SPIWrite 033b,f8,0,7
SPIWrite 033c,a0,0,7
SPIWrite 033d,14,0,7
SPIWrite 033e,38,0,7
SPIWrite 033f,bd,0,7
SPIWrite 0340,84,0,7
SPIWrite 0341,46,0,7
SPIWrite 0342,f8,0,7
SPIWrite 0343,b5,0,7
SPIWrite 0344,c3,0,7
SPIWrite 0345,48,0,7
SPIWrite 0346,df,0,7
SPIWrite 0347,f8,0,7
SPIWrite 0348,08,0,7
SPIWrite 0349,e3,0,7
SPIWrite 034a,4f,0,7
SPIWrite 034b,f4,0,7
```

```
SPIWrite 034c,25,0,7
SPIWrite 034d,73,0,7
SPIWrite 034e,dc,0,7
SPIWrite 034f,22,0,7
SPIWrite 0350,1c,0,7
SPIWrite 0351,fb,0,7
SPIWrite 0352,03,0,7
SPIWrite 0353,f3,0,7
SPIWrite 0354,11,0,7
SPIWrite 0355,fb,0,7
SPIWrite 0356,02,0,7
SPIWrite 0357,32,0,7
SPIWrite 0358,80,0,7
SPIWrite 0359,18,0,7
SPIWrite 035a,90,0,7
SPIWrite 035b,f8,0,7
SPIWrite 035c,38,0,7
SPIWrite 035d,60,0,7
SPIWrite 035e,90,0,7
SPIWrite 035f,f8,0,7
SPIWrite 0360,3d,0,7
SPIWrite 0361,70,0,7
SPIWrite 0362,bd,0,7
SPIWrite 0363,4a,0,7
SPIWrite 0364,00,0,7
SPIWrite 0365,23,0,7
SPIWrite 0366,06,0,7
SPIWrite 0367,20,0,7
SPIWrite 0368,1c,0,7
SPIWrite 0369,fb,0,7
SPIWrite 036a,00,0,7
SPIWrite 036b,f4,0,7
SPIWrite 036c,04,0,7
SPIWrite 036d,eb,0,7
SPIWrite 036e,41,0,7
SPIWrite 036f,04,0,7
SPIWrite 0370,03,0,7
SPIWrite 0371,20,0,7
SPIWrite 0372,02,0,7
SPIWrite 0373,eb,0,7
SPIWrite 0374,44,0,7
SPIWrite 0375,02,0,7
SPIWrite 0376,01,0,7
SPIWrite 0377,2b,0,7
SPIWrite 0378,0b,0,7
SPIWrite 0379,d0,0,7
SPIWrite 037a,1c,0,7
SPIWrite 037b,fb,0,7
SPIWrite 037c,00,0,7
SPIWrite 037d,14,0,7
SPIWrite 037e,1e,0,7
SPIWrite 037f,f8,0,7
```

```
SPIWrite 0380,04,0,7
SPIWrite 0381,40,0,7
SPIWrite 0382,f5,0,7
SPIWrite 0383,1b,0,7
SPIWrite 0384,65,0,7
SPIWrite 0385,19,0,7
SPIWrite 0386,6d,0,7
SPIWrite 0387,b2,0,7
SPIWrite 0388,00,0,7
SPIWrite 0389,2d,0,7
SPIWrite 038a,48,0,7
SPIWrite 038b,bf,0,7
SPIWrite 038c,00,0,7
SPIWrite 038d,25,0,7
SPIWrite 038e,ed,0,7
SPIWrite 038f,b2,0,7
SPIWrite 0390,01,0,7
SPIWrite 0391,e0,0,7
SPIWrite 0392,3c,0,7
SPIWrite 0393,46,0,7
SPIWrite 0394,35,0,7
SPIWrite 0395,46,0,7
SPIWrite 0396,15,0,7
SPIWrite 0397,70,0,7
SPIWrite 0398,5b,0,7
SPIWrite 0399,1c,0,7
SPIWrite 039a,54,0,7
SPIWrite 039b,70,0,7
SPIWrite 039c,02,0,7
SPIWrite 039d,2b,0,7
SPIWrite 039e,02,0,7
SPIWrite 039f,f1,0,7
SPIWrite 03a0,02,0,7
SPIWrite 03a1,02,0,7
SPIWrite 03a2,e8,0,7
SPIWrite 03a3,db,0,7
SPIWrite 03a4,f8,0,7
SPIWrite 03a5,bd,0,7
SPIWrite 03a6,2d,0,7
SPIWrite 03a7,e9,0,7
SPIWrite 03a8,fe,0,7
SPIWrite 03a9,4f,0,7
SPIWrite 03aa,ac,0,7
SPIWrite 03ab,48,0,7
SPIWrite 03ac,df,0,7
SPIWrite 03ad,f8,0,7
SPIWrite 03ae,a4,0,7
SPIWrite 03af,92,0,7
SPIWrite 03b0,90,0,7
SPIWrite 03b1,f8,0,7
SPIWrite 03b2,00,0,7
SPIWrite 03b3,a0,0,7
```

```
SPIWrite 03b4,4f,0,7
SPIWrite 03b5,f0,0,7
SPIWrite 03b6,00,0,7
SPIWrite 03b7,0e,0,7
SPIWrite 03b8,4f,0,7
SPIWrite 03b9,f0,0,7
SPIWrite 03ba,01,0,7
SPIWrite 03bb,08,0,7
SPIWrite 03bc,0d,0,7
SPIWrite 03bd,f1,0,7
SPIWrite 03be,01,0,7
SPIWrite 03bf,04,0,7
SPIWrite 03c0,76,0,7
SPIWrite 03c1,46,0,7
SPIWrite 03c2,35,0,7
SPIWrite 03c3,46,0,7
SPIWrite 03c4,00,0,7
SPIWrite 03c5,20,0,7
SPIWrite 03c6,a6,0,7
SPIWrite 03c7,4f,0,7
SPIWrite 03c8,a6,0,7
SPIWrite 03c9,4a,0,7
SPIWrite 03ca,a0,0,7
SPIWrite 03cb,49,0,7
SPIWrite 03cc,04,0,7
SPIWrite 03cd,f8,0,7
SPIWrite 03ce,01,0,7
SPIWrite 03cf,0f,0,7
SPIWrite 03d0,f3,0,7
SPIWrite 03d1,19,0,7
SPIWrite 03d2,92,0,7
SPIWrite 03d3,19,0,7
SPIWrite 03d4,71,0,7
SPIWrite 03d5,44,0,7
SPIWrite 03d6,a2,0,7
SPIWrite 03d7,f1,0,7
SPIWrite 03d8,01,0,7
SPIWrite 03d9,0c,0,7
SPIWrite 03da,09,0,7
SPIWrite 03db,1f,0,7
SPIWrite 03dc,51,0,7
SPIWrite 03dd,f8,0,7
SPIWrite 03de,04,0,7
SPIWrite 03df,2f,0,7
SPIWrite 03e0,d2,0,7
SPIWrite 03e1,f8,0,7
SPIWrite 03e2,98,0,7
SPIWrite 03e3,24,0,7
SPIWrite 03e4,02,0,7
SPIWrite 03e5,f0,0,7
SPIWrite 03e6,01,0,7
SPIWrite 03e7,02,0,7
```

```
SPIWrite 03e8,0a,0,7
SPIWrite 03e9,ea,0,7
SPIWrite 03ea,02,0,7
SPIWrite 03eb,07,0,7
SPIWrite 03ec,ff,0,7
SPIWrite 03ed,22,0,7
SPIWrite 03ee,01,0,7
SPIWrite 03ef,2f,0,7
SPIWrite 03f0,0c,0,7
SPIWrite 03f1,f8,0,7
SPIWrite 03f2,01,0,7
SPIWrite 03f3,2f,0,7
SPIWrite 03f4,0d,0,7
SPIWrite 03f5,d1,0,7
SPIWrite 03f6,dc,0,7
SPIWrite 03f7,22,0,7
SPIWrite 03f8,4f,0,7
SPIWrite 03f9,f4,0,7
SPIWrite 03fa,25,0,7
SPIWrite 03fb,7b,0,7
SPIWrite 03fc,42,0,7
SPIWrite 03fd,43,0,7
SPIWrite 03fe,0b,0,7
SPIWrite 03ff,fb,0,7
SPIWrite 0400,05,0,7
SPIWrite 0401,22,0,7
SPIWrite 0402,4a,0,7
SPIWrite 0403,44,0,7
SPIWrite 0404,92,0,7
SPIWrite 0405,f8,0,7
SPIWrite 0406,7a,0,7
SPIWrite 0407,20,0,7
SPIWrite 0408,00,0,7
SPIWrite 0409,2a,0,7
SPIWrite 040a,08,0,7
SPIWrite 040b,bf,0,7
SPIWrite 040c,83,0,7
SPIWrite 040d,f8,0,7
SPIWrite 040e,00,0,7
SPIWrite 040f,80,0,7
SPIWrite 0410,01,0,7
SPIWrite 0411,d0,0,7
SPIWrite 0412,00,0,7
SPIWrite 0413,22,0,7
SPIWrite 0414,1a,0,7
SPIWrite 0415,70,0,7
SPIWrite 0416,01,0,7
SPIWrite 0417,2f,0,7
SPIWrite 0418,04,0,7
SPIWrite 0419,d1,0,7
SPIWrite 041a,27,0,7
SPIWrite 041b,78,0,7
```

```
SPIWrite 041c,08,0,7
SPIWrite 041d,fa,0,7
SPIWrite 041e,00,0,7
SPIWrite 041f,f2,0,7
SPIWrite 0420,3a,0,7
SPIWrite 0421,43,0,7
SPIWrite 0422,22,0,7
SPIWrite 0423,70,0,7
SPIWrite 0424,40,0,7
SPIWrite 0425,1c,0,7
SPIWrite 0426,5b,0,7
SPIWrite 0427,1c,0,7
SPIWrite 0428,03,0,7
SPIWrite 0429,28,0,7
SPIWrite 042a,d7,0,7
SPIWrite 042b,db,0,7
SPIWrite 042c,6d,0,7
SPIWrite 042d,1c,0,7
SPIWrite 042e,f6,0,7
SPIWrite 042f,1c,0,7
SPIWrite 0430,0e,0,7
SPIWrite 0431,f1,0,7
SPIWrite 0432,0c,0,7
SPIWrite 0433,0e,0,7
SPIWrite 0434,02,0,7
SPIWrite 0435,2d,0,7
SPIWrite 0436,c5,0,7
SPIWrite 0437,db,0,7
SPIWrite 0438,0d,0,7
SPIWrite 0439,f1,0,7
SPIWrite 043a,02,0,7
SPIWrite 043b,00,0,7
SPIWrite 043c,ff,0,7
SPIWrite 043d,f7,0,7
SPIWrite 043e,16,0,7
SPIWrite 043f,fa,0,7
SPIWrite 0440,00,0,7
SPIWrite 0441,25,0,7
SPIWrite 0442,4f,0,7
SPIWrite 0443,f0,0,7
SPIWrite 0444,dc,0,7
SPIWrite 0445,08,0,7
SPIWrite 0446,2e,0,7
SPIWrite 0447,46,0,7
SPIWrite 0448,85,0,7
SPIWrite 0449,48,0,7
SPIWrite 044a,00,0,7
SPIWrite 044b,24,0,7
SPIWrite 044c,2f,0,7
SPIWrite 044d,18,0,7
SPIWrite 044e,17,0,7
SPIWrite 044f,f8,0,7
```

```
SPIWrite 0450,01,0,7
SPIWrite 0451,0b,0,7
SPIWrite 0452,98,0,7
SPIWrite 0453,b9,0,7
SPIWrite 0454,06,0,7
SPIWrite 0455,eb,0,7
SPIWrite 0456,46,0,7
SPIWrite 0457,00,0,7
SPIWrite 0458,20,0,7
SPIWrite 0459,18,0,7
SPIWrite 045a,08,0,7
SPIWrite 045b,fb,0,7
SPIWrite 045c,00,0,7
SPIWrite 045d,90,0,7
SPIWrite 045e,6a,0,7
SPIWrite 045f,46,0,7
SPIWrite 0460,90,0,7
SPIWrite 0461,f8,0,7
SPIWrite 0462,3d,0,7
SPIWrite 0463,10,0,7
SPIWrite 0464,90,0,7
SPIWrite 0465,f8,0,7
SPIWrite 0466,38,0,7
SPIWrite 0467,00,0,7
SPIWrite 0468,8d,0,7
SPIWrite 0469,f8,0,7
SPIWrite 046a,01,0,7
SPIWrite 046b,10,0,7
SPIWrite 046c,00,0,7
SPIWrite 046d,23,0,7
SPIWrite 046e,8d,0,7
SPIWrite 046f,f8,0,7
SPIWrite 0470,00,0,7
SPIWrite 0471,00,0,7
SPIWrite 0472,21,0,7
SPIWrite 0473,46,0,7
SPIWrite 0474,30,0,7
SPIWrite 0475,46,0,7
SPIWrite 0476,ff,0,7
SPIWrite 0477,f7,0,7
SPIWrite 0478,4b,0,7
SPIWrite 0479,ff,0,7
SPIWrite 047a,06,0,7
SPIWrite 047b,e0,0,7
SPIWrite 047c,30,0,7
SPIWrite 047d,46,0,7
SPIWrite 047e,21,0,7
SPIWrite 047f,46,0,7
SPIWrite 0480,ff,0,7
SPIWrite 0481,f7,0,7
SPIWrite 0482,5e,0,7
SPIWrite 0483,ff,0,7
```

```
SPIWrite 0484,30,0,7
SPIWrite 0485,46,0,7
SPIWrite 0486,ff,0,7
SPIWrite 0487,f7,0,7
SPIWrite 0488,06,0,7
SPIWrite 0489,fb,0,7
SPIWrite 048a,64,0,7
SPIWrite 048b,1c,0,7
SPIWrite 048c,03,0,7
SPIWrite 048d,2c,0,7
SPIWrite 048e,de,0,7
SPIWrite 048f,db,0,7
SPIWrite 0490,76,0,7
SPIWrite 0491,1c,0,7
SPIWrite 0492,ed,0,7
SPIWrite 0493,1c,0,7
SPIWrite 0494,02,0,7
SPIWrite 0495,2e,0,7
SPIWrite 0496,d7,0,7
SPIWrite 0497,db,0,7
SPIWrite 0498,bd,0,7
SPIWrite 0499,e8,0,7
SPIWrite 049a,fe,0,7
SPIWrite 049b,8f,0,7
SPIWrite 049c,f8,0,7
SPIWrite 049d,b5,0,7
SPIWrite 049e,72,0,7
SPIWrite 049f,48,0,7
SPIWrite 04a0,72,0,7
SPIWrite 04a1,4a,0,7
SPIWrite 04a2,7b,0,7
SPIWrite 04a3,4c,0,7
SPIWrite 04a4,72,0,7
SPIWrite 04a5,4e,0,7
SPIWrite 04a6,74,0,7
SPIWrite 04a7,4d,0,7
SPIWrite 04a8,07,0,7
SPIWrite 04a9,78,0,7
SPIWrite 04aa,12,0,7
SPIWrite 04ab,78,0,7
SPIWrite 04ac,6b,0,7
SPIWrite 04ad,48,0,7
SPIWrite 04ae,52,0,7
SPIWrite 04af,08,0,7
SPIWrite 04b0,11,0,7
SPIWrite 04b1,d2,0,7
SPIWrite 04b2,00,0,7
SPIWrite 04b3,21,0,7
SPIWrite 04b4,01,0,7
SPIWrite 04b5,70,0,7
SPIWrite 04b6,5f,0,7
SPIWrite 04b7,b9,0,7
```

```
SPIWrite 04b8,4f,0,7
SPIWrite 04b9,f0,0,7
SPIWrite 04ba,00,0,7
SPIWrite 04bb,70,0,7
SPIWrite 04bc,80,0,7
SPIWrite 04bd,34,0,7
SPIWrite 04be,20,0,7
SPIWrite 04bf,60,0,7
SPIWrite 04c0,6e,0,7
SPIWrite 04c1,49,0,7
SPIWrite 04c2,c5,0,7
SPIWrite 04c3,f8,0,7
SPIWrite 04c4,7c,0,7
SPIWrite 04c5,11,0,7
SPIWrite 04c6,6e,0,7
SPIWrite 04c7,4a,0,7
SPIWrite 04c8,c5,0,7
SPIWrite 04c9,f8,0,7
SPIWrite 04ca,a0,0,7
SPIWrite 04cb,21,0,7
SPIWrite 04cc,69,0,7
SPIWrite 04cd,4f,0,7
SPIWrite 04ce,37,0,7
SPIWrite 04cf,60,0,7
SPIWrite 04d0,ff,0,7
SPIWrite 04d1,f7,0,7
SPIWrite 04d2,69,0,7
SPIWrite 04d3,ff,0,7
SPIWrite 04d4,f8,0,7
SPIWrite 04d5,bd,0,7
SPIWrite 04d6,01,0,7
SPIWrite 04d7,2f,0,7
SPIWrite 04d8,0f,0,7
SPIWrite 04d9,d0,0,7
SPIWrite 04da,01,0,7
SPIWrite 04db,21,0,7
SPIWrite 04dc,01,0,7
SPIWrite 04dd,70,0,7
SPIWrite 04de,ff,0,7
SPIWrite 04df,f7,0,7
SPIWrite 04e0,62,0,7
SPIWrite 04e1,ff,0,7
SPIWrite 04e2,6a,0,7
SPIWrite 04e3,4f,0,7
SPIWrite 04e4,c5,0,7
SPIWrite 04e5,f8,0,7
SPIWrite 04e6,a0,0,7
SPIWrite 04e7,71,0,7
SPIWrite 04e8,66,0,7
SPIWrite 04e9,48,0,7
SPIWrite 04ea,30,0,7
SPIWrite 04eb,60,0,7
```

```
SPIWrite 04ec,66,0,7
SPIWrite 04ed,49,0,7
SPIWrite 04ee,c5,0,7
SPIWrite 04ef,f8,0,7
SPIWrite 04f0,7c,0,7
SPIWrite 04f1,11,0,7
SPIWrite 04f2,4f,0,7
SPIWrite 04f3,f0,0,7
SPIWrite 04f4,00,0,7
SPIWrite 04f5,73,0,7
SPIWrite 04f6,23,0,7
SPIWrite 04f7,60,0,7
SPIWrite 04f8,f8,0,7
SPIWrite 04f9,bd,0,7
SPIWrite 04fa,08,0,7
SPIWrite 04fb,20,0,7
SPIWrite 04fc,08,0,7
SPIWrite 04fd,70,0,7
SPIWrite 04fe,f8,0,7
SPIWrite 04ff,bd,0,7
SPIWrite 0500,2d,0,7
SPIWrite 0501,e9,0,7
SPIWrite 0502,f8,0,7
SPIWrite 0503,4f,0,7
SPIWrite 0504,df,0,7
SPIWrite 0505,f8,0,7
SPIWrite 0506,8c,0,7
SPIWrite 0507,b1,0,7
SPIWrite 0508,df,0,7
SPIWrite 0509,f8,0,7
SPIWrite 050a,40,0,7
SPIWrite 050b,a1,0,7
SPIWrite 050c,df,0,7
SPIWrite 050d,f8,0,7
SPIWrite 050e,44,0,7
SPIWrite 050f,81,0,7
SPIWrite 0510,df,0,7
SPIWrite 0511,f8,0,7
SPIWrite 0512,3c,0,7
SPIWrite 0513,91,0,7
SPIWrite 0514,02,0,7
SPIWrite 0515,46,0,7
SPIWrite 0516,4f,0,7
SPIWrite 0517,f0,0,7
SPIWrite 0518,dc,0,7
SPIWrite 0519,0c,0,7
SPIWrite 051a,01,0,7
SPIWrite 051b,23,0,7
SPIWrite 051c,00,0,7
SPIWrite 051d,24,0,7
SPIWrite 051e,4f,0,7
SPIWrite 051f,f4,0,7
```

```
SPIWrite 0520,25,0,7
SPIWrite 0521,7e,0,7
SPIWrite 0522,04,0,7
SPIWrite 0523,20,0,7
SPIWrite 0524,00,0,7
SPIWrite 0525,92,0,7
SPIWrite 0526,00,0,7
SPIWrite 0527,9d,0,7
SPIWrite 0528,03,0,7
SPIWrite 0529,fa,0,7
SPIWrite 052a,04,0,7
SPIWrite 052b,f2,0,7
SPIWrite 052c,15,0,7
SPIWrite 052d,42,0,7
SPIWrite 052e,1e,0,7
SPIWrite 052f,d0,0,7
SPIWrite 0530,1b,0,7
SPIWrite 0531,f8,0,7
SPIWrite 0532,14,0,7
SPIWrite 0533,20,0,7
SPIWrite 0534,04,0,7
SPIWrite 0535,2a,0,7
SPIWrite 0536,1a,0,7
SPIWrite 0537,d0,0,7
SPIWrite 0538,65,0,7
SPIWrite 0539,10,0,7
SPIWrite 053a,05,0,7
SPIWrite 053b,eb,0,7
SPIWrite 053c,45,0,7
SPIWrite 053d,06,0,7
SPIWrite 053e,96,0,7
SPIWrite 053f,19,0,7
SPIWrite 0540,5a,0,7
SPIWrite 0541,f8,0,7
SPIWrite 0542,26,0,7
SPIWrite 0543,70,0,7
SPIWrite 0544,d7,0,7
SPIWrite 0545,f8,0,7
SPIWrite 0546,98,0,7
SPIWrite 0547,74,0,7
SPIWrite 0548,7f,0,7
SPIWrite 0549,08,0,7
SPIWrite 054a,10,0,7
SPIWrite 054b,d3,0,7
SPIWrite 054c,19,0,7
SPIWrite 054d,f8,0,7
SPIWrite 054e,06,0,7
SPIWrite 054f,60,0,7
SPIWrite 0550,12,0,7
SPIWrite 0551,fb,0,7
SPIWrite 0552,0c,0,7
SPIWrite 0553,f2,0,7
```

```
SPIWrite 0554,0e,0,7
SPIWrite 0555,fb,0,7
SPIWrite 0556,05,0,7
SPIWrite 0557,22,0,7
SPIWrite 0558,08,0,7
SPIWrite 0559,eb,0,7
SPIWrite 055a,02,0,7
SPIWrite 055b,05,0,7
SPIWrite 055c,95,0,7
SPIWrite 055d,f8,0,7
SPIWrite 055e,3d,0,7
SPIWrite 055f,20,0,7
SPIWrite 0560,95,0,7
SPIWrite 0561,f8,0,7
SPIWrite 0562,38,0,7
SPIWrite 0563,50,0,7
SPIWrite 0564,92,0,7
SPIWrite 0565,1b,0,7
SPIWrite 0566,95,0,7
SPIWrite 0567,42,0,7
SPIWrite 0568,bc,0,7
SPIWrite 0569,bf,0,7
SPIWrite 056a,08,0,7
SPIWrite 056b,70,0,7
SPIWrite 056c,4b,0,7
SPIWrite 056d,80,0,7
SPIWrite 056e,64,0,7
SPIWrite 056f,1c,0,7
SPIWrite 0570,04,0,7
SPIWrite 0571,2c,0,7
SPIWrite 0572,d8,0,7
SPIWrite 0573,db,0,7
SPIWrite 0574,df,0,7
SPIWrite 0575,f8,0,7
SPIWrite 0576,24,0,7
SPIWrite 0577,b1,0,7
SPIWrite 0578,00,0,7
SPIWrite 0579,24,0,7
SPIWrite 057a,00,0,7
SPIWrite 057b,9d,0,7
SPIWrite 057c,22,0,7
SPIWrite 057d,1d,0,7
SPIWrite 057e,03,0,7
SPIWrite 057f,fa,0,7
SPIWrite 0580,02,0,7
SPIWrite 0581,f2,0,7
SPIWrite 0582,15,0,7
SPIWrite 0583,42,0,7
SPIWrite 0584,1f,0,7
SPIWrite 0585,d0,0,7
SPIWrite 0586,44,0,7
SPIWrite 0587,4a,0,7
```

```
SPIWrite 0588,17,0,7
SPIWrite 0589,5d,0,7
SPIWrite 058a,e7,0,7
SPIWrite 058b,b9,0,7
SPIWrite 058c,1b,0,7
SPIWrite 058d,f8,0,7
SPIWrite 058e,14,0,7
SPIWrite 058f,50,0,7
SPIWrite 0590,04,0,7
SPIWrite 0591,2d,0,7
SPIWrite 0592,18,0,7
SPIWrite 0593,d0,0,7
SPIWrite 0594,04,0,7
SPIWrite 0595,eb,0,7
SPIWrite 0596,44,0,7
SPIWrite 0597,02,0,7
SPIWrite 0598,aa,0,7
SPIWrite 0599,18,0,7
SPIWrite 059a,5a,0,7
SPIWrite 059b,f8,0,7
SPIWrite 059c,22,0,7
SPIWrite 059d,60,0,7
SPIWrite 059e,d6,0,7
SPIWrite 059f,f8,0,7
SPIWrite 05a0,98,0,7
SPIWrite 05a1,64,0,7
SPIWrite 05a2,76,0,7
SPIWrite 05a3,08,0,7
SPIWrite 05a4,0f,0,7
SPIWrite 05a5,d3,0,7
SPIWrite 05a6,19,0,7
SPIWrite 05a7,f8,0,7
SPIWrite 05a8,02,0,7
SPIWrite 05a9,60,0,7
SPIWrite 05aa,15,0,7
SPIWrite 05ab,fb,0,7
SPIWrite 05ac,0c,0,7
SPIWrite 05ad,f5,0,7
SPIWrite 05ae,0e,0,7
SPIWrite 05af,fb,0,7
SPIWrite 05b0,04,0,7
SPIWrite 05b1,55,0,7
SPIWrite 05b2,45,0,7
SPIWrite 05b3,44,0,7
SPIWrite 05b4,95,0,7
SPIWrite 05b5,f8,0,7
SPIWrite 05b6,3d,0,7
SPIWrite 05b7,20,0,7
SPIWrite 05b8,95,0,7
SPIWrite 05b9,f8,0,7
SPIWrite 05ba,38,0,7
SPIWrite 05bb,50,0,7
```

```
SPIWrite 05bc,92,0,7
SPIWrite 05bd,1b,0,7
SPIWrite 05be,95,0,7
SPIWrite 05bf,42,0,7
SPIWrite 05c0,bc,0,7
SPIWrite 05c1,bf,0,7
SPIWrite 05c2,08,0,7
SPIWrite 05c3,70,0,7
SPIWrite 05c4,4b,0,7
SPIWrite 05c5,80,0,7
SPIWrite 05c6,64,0,7
SPIWrite 05c7,1c,0,7
SPIWrite 05c8,02,0,7
SPIWrite 05c9,2c,0,7
SPIWrite 05ca,d6,0,7
SPIWrite 05cb,db,0,7
SPIWrite 05cc,bd,0,7
SPIWrite 05cd,e8,0,7
SPIWrite 05ce,f8,0,7
SPIWrite 05cf,8f,0,7
SPIWrite 05d0,2d,0,7
SPIWrite 05d1,e9,0,7
SPIWrite 05d2,f8,0,7
SPIWrite 05d3,43,0,7
SPIWrite 05d4,89,0,7
SPIWrite 05d5,46,0,7
SPIWrite 05d6,25,0,7
SPIWrite 05d7,4c,0,7
SPIWrite 05d8,df,0,7
SPIWrite 05d9,f8,0,7
SPIWrite 05da,b8,0,7
SPIWrite 05db,c0,0,7
SPIWrite 05dc,1c,0,7
SPIWrite 05dd,49,0,7
SPIWrite 05de,20,0,7
SPIWrite 05df,78,0,7
SPIWrite 05e0,01,0,7
SPIWrite 05e1,22,0,7
SPIWrite 05e2,00,0,7
SPIWrite 05e3,26,0,7
SPIWrite 05e4,02,0,7
SPIWrite 05e5,fa,0,7
SPIWrite 05e6,06,0,7
SPIWrite 05e7,f3,0,7
SPIWrite 05e8,18,0,7
SPIWrite 05e9,42,0,7
SPIWrite 05ea,09,0,7
SPIWrite 05eb,d0,0,7
SPIWrite 05ec,1c,0,7
SPIWrite 05ed,f8,0,7
SPIWrite 05ee,16,0,7
SPIWrite 05ef,50,0,7
```

```
SPIWrite 05f0,04,0,7
SPIWrite 05f1,2d,0,7
SPIWrite 05f2,05,0,7
SPIWrite 05f3,d0,0,7
SPIWrite 05f4,67,0,7
SPIWrite 05f5,78,0,7
SPIWrite 05f6,73,0,7
SPIWrite 05f7,10,0,7
SPIWrite 05f8,03,0,7
SPIWrite 05f9,eb,0,7
SPIWrite 05fa,43,0,7
SPIWrite 05fb,03,0,7
SPIWrite 05fc,ed,0,7
SPIWrite 05fd,18,0,7
SPIWrite 05fe,4f,0,7
SPIWrite 05ff,55,0,7
SPIWrite 0600,76,0,7
SPIWrite 0601,1c,0,7
SPIWrite 0602,04,0,7
SPIWrite 0603,2e,0,7
SPIWrite 0604,ee,0,7
SPIWrite 0605,db,0,7
SPIWrite 0606,df,0,7
SPIWrite 0607,f8,0,7
SPIWrite 0608,90,0,7
SPIWrite 0609,80,0,7
SPIWrite 060a,df,0,7
SPIWrite 060b,f8,0,7
SPIWrite 060c,90,0,7
SPIWrite 060d,e0,0,7
SPIWrite 060e,00,0,7
SPIWrite 060f,23,0,7
SPIWrite 0610,94,0,7
SPIWrite 0611,46,0,7
SPIWrite 0612,08,0,7
SPIWrite 0613,25,0,7
SPIWrite 0614,1a,0,7
SPIWrite 0615,1d,0,7
SPIWrite 0616,0c,0,7
SPIWrite 0617,fa,0,7
SPIWrite 0618,02,0,7
SPIWrite 0619,f2,0,7
SPIWrite 061a,10,0,7
SPIWrite 061b,42,0,7
SPIWrite 061c,0e,0,7
SPIWrite 061d,d0,0,7
SPIWrite 061e,18,0,7
SPIWrite 061f,f8,0,7
SPIWrite 0620,03,0,7
SPIWrite 0621,70,0,7
SPIWrite 0622,4f,0,7
SPIWrite 0623,b9,0,7
```

```
SPIWrite 0624,1e,0,7
SPIWrite 0625,f8,0,7
SPIWrite 0626,13,0,7
SPIWrite 0627,20,0,7
SPIWrite 0628,04,0,7
SPIWrite 0629,2a,0,7
SPIWrite 062a,07,0,7
SPIWrite 062b,d0,0,7
SPIWrite 062c,66,0,7
SPIWrite 062d,78,0,7
SPIWrite 062e,03,0,7
SPIWrite 062f,eb,0,7
SPIWrite 0630,43,0,7
SPIWrite 0631,07,0,7
SPIWrite 0632,d2,0,7
SPIWrite 0633,19,0,7
SPIWrite 0634,8e,0,7
SPIWrite 0635,54,0,7
SPIWrite 0636,01,0,7
SPIWrite 0637,e0,0,7
SPIWrite 0638,89,0,7
SPIWrite 0639,f8,0,7
SPIWrite 063a,00,0,7
SPIWrite 063b,50,0,7
SPIWrite 063c,5b,0,7
SPIWrite 063d,1c,0,7
SPIWrite 063e,02,0,7
SPIWrite 063f,2b,0,7
SPIWrite 0640,e8,0,7
SPIWrite 0641,db,0,7
SPIWrite 0642,49,0,7
SPIWrite 0643,46,0,7
SPIWrite 0644,ff,0,7
SPIWrite 0645,f7,0,7
SPIWrite 0646,5c,0,7
SPIWrite 0647,ff,0,7
SPIWrite 0648,bd,0,7
SPIWrite 0649,e8,0,7
SPIWrite 064a,f8,0,7
SPIWrite 064b,83,0,7
SPIWrite 064c,a8,0,7
SPIWrite 064d,75,0,7
SPIWrite 064e,02,0,7
SPIWrite 064f,00,0,7
SPIWrite 0650,c4,0,7
SPIWrite 0651,22,0,7
SPIWrite 0652,01,0,7
SPIWrite 0653,20,0,7
SPIWrite 0654,e0,0,7
SPIWrite 0655,ab,0,7
SPIWrite 0656,00,0,7
SPIWrite 0657,20,0,7
```

```
SPIWrite 0658,8c,0,7
SPIWrite 0659,22,0,7
SPIWrite 065a,01,0,7
SPIWrite 065b,20,0,7
SPIWrite 065c,f2,0,7
SPIWrite 065d,22,0,7
SPIWrite 065e,01,0,7
SPIWrite 065f,20,0,7
SPIWrite 0660,cc,0,7
SPIWrite 0661,22,0,7
SPIWrite 0662,01,0,7
SPIWrite 0663,20,0,7
SPIWrite 0664,d4,0,7
SPIWrite 0665,22,0,7
SPIWrite 0666,01,0,7
SPIWrite 0667,20,0,7
SPIWrite 0668,f3,0,7
SPIWrite 0669,22,0,7
SPIWrite 066a,01,0,7
SPIWrite 066b,20,0,7
SPIWrite 066c,b4,0,7
SPIWrite 066d,03,0,7
SPIWrite 066e,00,0,7
SPIWrite 066f,a2,0,7
SPIWrite 0670,68,0,7
SPIWrite 0671,da,0,7
SPIWrite 0672,00,0,7
SPIWrite 0673,20,0,7
SPIWrite 0674,2b,0,7
SPIWrite 0675,fd,0,7
SPIWrite 0676,01,0,7
SPIWrite 0677,00,0,7
SPIWrite 0678,d4,0,7
SPIWrite 0679,f7,0,7
SPIWrite 067a,00,0,7
SPIWrite 067b,20,0,7
SPIWrite 067c,dd,0,7
SPIWrite 067d,34,0,7
SPIWrite 067e,00,0,7
SPIWrite 067f,00,0,7
SPIWrite 0680,29,0,7
SPIWrite 0681,47,0,7
SPIWrite 0682,00,0,7
SPIWrite 0683,00,0,7
SPIWrite 0684,e5,0,7
SPIWrite 0685,05,0,7
SPIWrite 0686,03,0,7
SPIWrite 0687,00,0,7
SPIWrite 0688,17,0,7
SPIWrite 0689,05,0,7
SPIWrite 068a,03,0,7
SPIWrite 068b,00,0,7
```

```
SPIWrite 068c,a9,0,7
SPIWrite 068d,05,0,7
SPIWrite 068e,03,0,7
SPIWrite 068f,00,0,7
SPIWrite 0690,00,0,7
SPIWrite 0691,e1,0,7
SPIWrite 0692,00,0,7
SPIWrite 0693,e0,0,7
SPIWrite 0694,06,0,7
SPIWrite 0695,d6,0,7
SPIWrite 0696,00,0,7
SPIWrite 0697,20,0,7
SPIWrite 0698,9e,0,7
SPIWrite 0699,13,0,7
SPIWrite 069a,01,0,7
SPIWrite 069b,20,0,7
SPIWrite 069c,64,0,7
SPIWrite 069d,d6,0,7
SPIWrite 069e,00,0,7
SPIWrite 069f,20,0,7
SPIWrite 06a0,10,0,7
SPIWrite 06a1,b5,0,7
SPIWrite 06a2,b7,0,7
SPIWrite 06a3,4b,0,7
SPIWrite 06a4,b5,0,7
SPIWrite 06a5,4c,0,7
SPIWrite 06a6,03,0,7
SPIWrite 06a7,22,0,7
SPIWrite 06a8,10,0,7
SPIWrite 06a9,fb,0,7
SPIWrite 06aa,02,0,7
SPIWrite 06ab,10,0,7
SPIWrite 06ac,18,0,7
SPIWrite 06ad,5c,0,7
SPIWrite 06ae,20,0,7
SPIWrite 06af,5c,0,7
SPIWrite 06b0,80,0,7
SPIWrite 06b1,00,0,7
SPIWrite 06b2,c0,0,7
SPIWrite 06b3,b2,0,7
SPIWrite 06b4,10,0,7
SPIWrite 06b5,bd,0,7
SPIWrite 06b6,2d,0,7
SPIWrite 06b7,e9,0,7
SPIWrite 06b8,f0,0,7
SPIWrite 06b9,4f,0,7
SPIWrite 06ba,ad,0,7
SPIWrite 06bb,f1,0,7
SPIWrite 06bc,34,0,7
SPIWrite 06bd,0d,0,7
SPIWrite 06be,08,0,7
SPIWrite 06bf,90,0,7
```

```
SPIWrite 06c0,e7,0,7
SPIWrite 06c1,f7,0,7
SPIWrite 06c2,3c,0,7
SPIWrite 06c3,ff,0,7
SPIWrite 06c4,af,0,7
SPIWrite 06c5,4a,0,7
SPIWrite 06c6,06,0,7
SPIWrite 06c7,27,0,7
SPIWrite 06c8,10,0,7
SPIWrite 06c9,46,0,7
SPIWrite 06ca,00,0,7
SPIWrite 06cb,21,0,7
SPIWrite 06cc,7f,0,7
SPIWrite 06cd,1e,0,7
SPIWrite 06ce,00,0,7
SPIWrite 06cf,f8,0,7
SPIWrite 06d0,01,0,7
SPIWrite 06d1,1b,0,7
SPIWrite 06d2,fa,0,7
SPIWrite 06d3,d1,0,7
SPIWrite 06d4,aa,0,7
SPIWrite 06d5,49,0,7
SPIWrite 06d6,08,0,7
SPIWrite 06d7,98,0,7
SPIWrite 06d8,ac,0,7
SPIWrite 06d9,4c,0,7
SPIWrite 06da,89,0,7
SPIWrite 06db,1f,0,7
SPIWrite 06dc,08,0,7
SPIWrite 06dd,18,0,7
SPIWrite 06de,80,0,7
SPIWrite 06df,78,0,7
SPIWrite 06e0,b1,0,7
SPIWrite 06e1,f8,0,7
SPIWrite 06e2,9e,0,7
SPIWrite 06e3,31,0,7
SPIWrite 06e4,20,0,7
SPIWrite 06e5,5c,0,7
SPIWrite 06e6,4f,0,7
SPIWrite 06e7,f0,0,7
SPIWrite 06e8,01,0,7
SPIWrite 06e9,0a,0,7
SPIWrite 06ea,89,0,7
SPIWrite 06eb,46,0,7
SPIWrite 06ec,58,0,7
SPIWrite 06ed,43,0,7
SPIWrite 06ee,09,0,7
SPIWrite 06ef,90,0,7
SPIWrite 06f0,a8,0,7
SPIWrite 06f1,48,0,7
SPIWrite 06f2,d0,0,7
SPIWrite 06f3,f8,0,7
```

```
SPIWrite 06f4,d8,0,7
SPIWrite 06f5,31,0,7
SPIWrite 06f6,04,0,7
SPIWrite 06f7,27,0,7
SPIWrite 06f8,51,0,7
SPIWrite 06f9,46,0,7
SPIWrite 06fa,6a,0,7
SPIWrite 06fb,46,0,7
SPIWrite 06fc,08,0,7
SPIWrite 06fd,98,0,7
SPIWrite 06fe,8d,0,7
SPIWrite 06ff,f8,0,7
SPIWrite 0700,00,0,7
SPIWrite 0701,70,0,7
SPIWrite 0702,98,0,7
SPIWrite 0703,47,0,7
SPIWrite 0704,ad,0,7
SPIWrite 0705,f1,0,7
SPIWrite 0706,01,0,7
SPIWrite 0707,06,0,7
SPIWrite 0708,02,0,7
SPIWrite 0709,96,0,7
SPIWrite 070a,02,0,7
SPIWrite 070b,20,0,7
SPIWrite 070c,06,0,7
SPIWrite 070d,90,0,7
SPIWrite 070e,02,0,7
SPIWrite 070f,98,0,7
SPIWrite 0710,10,0,7
SPIWrite 0711,f8,0,7
SPIWrite 0712,01,0,7
SPIWrite 0713,1f,0,7
SPIWrite 0714,04,0,7
SPIWrite 0715,29,0,7
SPIWrite 0716,02,0,7
SPIWrite 0717,90,0,7
SPIWrite 0718,00,0,7
SPIWrite 0719,f0,0,7
SPIWrite 071a,90,0,7
SPIWrite 071b,80,0,7
SPIWrite 071c,9d,0,7
SPIWrite 071d,48,0,7
SPIWrite 071e,08,0,7
SPIWrite 071f,9c,0,7
SPIWrite 0720,d0,0,7
SPIWrite 0721,f8,0,7
SPIWrite 0722,f8,0,7
SPIWrite 0723,21,0,7
SPIWrite 0724,20,0,7
SPIWrite 0725,46,0,7
SPIWrite 0726,90,0,7
SPIWrite 0727,47,0,7
```

```
SPIWrite 0728,4f,0,7
SPIWrite 0729,f0,0,7
SPIWrite 072a,0d,0,7
SPIWrite 072b,0b,0,7
SPIWrite 072c,98,0,7
SPIWrite 072d,49,0,7
SPIWrite 072e,0a,0,7
SPIWrite 072f,90,0,7
SPIWrite 0730,0b,0,7
SPIWrite 0731,fb,0,7
SPIWrite 0732,00,0,7
SPIWrite 0733,fb,0,7
SPIWrite 0734,40,0,7
SPIWrite 0735,18,0,7
SPIWrite 0736,80,0,7
SPIWrite 0737,7a,0,7
SPIWrite 0738,0f,0,7
SPIWrite 0739,46,0,7
SPIWrite 073a,0b,0,7
SPIWrite 073b,eb,0,7
SPIWrite 073c,07,0,7
SPIWrite 073d,01,0,7
SPIWrite 073e,0b,0,7
SPIWrite 073f,90,0,7
SPIWrite 0740,91,0,7
SPIWrite 0741,f8,0,7
SPIWrite 0742,22,0,7
SPIWrite 0743,00,0,7
SPIWrite 0744,ba,0,7
SPIWrite 0745,f1,0,7
SPIWrite 0746,01,0,7
SPIWrite 0747,0f,0,7
SPIWrite 0748,0c,0,7
SPIWrite 0749,90,0,7
SPIWrite 074a,4f,0,7
SPIWrite 074b,ea,0,7
SPIWrite 074c,44,0,7
SPIWrite 074d,00,0,7
SPIWrite 074e,0a,0,7
SPIWrite 074f,eb,0,7
SPIWrite 0750,00,0,7
SPIWrite 0751,02,0,7
SPIWrite 0752,0a,0,7
SPIWrite 0753,eb,0,7
SPIWrite 0754,00,0,7
SPIWrite 0755,01,0,7
SPIWrite 0756,a2,0,7
SPIWrite 0757,f1,0,7
SPIWrite 0758,01,0,7
SPIWrite 0759,02,0,7
SPIWrite 075a,a1,0,7
SPIWrite 075b,f1,0,7
```

```
SPIWrite 075c,01,0,7
SPIWrite 075d,01,0,7
SPIWrite 075e,d3,0,7
SPIWrite 075f,b2,0,7
SPIWrite 0760,c9,0,7
SPIWrite 0761,b2,0,7
SPIWrite 0762,4f,0,7
SPIWrite 0763,ea,0,7
SPIWrite 0764,61,0,7
SPIWrite 0765,02,0,7
SPIWrite 0766,0c,0,7
SPIWrite 0767,bf,0,7
SPIWrite 0768,02,0,7
SPIWrite 0769,21,0,7
SPIWrite 076a,01,0,7
SPIWrite 076b,21,0,7
SPIWrite 076c,8d,0,7
SPIWrite 076d,f8,0,7
SPIWrite 076e,04,0,7
SPIWrite 076f,30,0,7
SPIWrite 0770,09,0,7
SPIWrite 0771,18,0,7
SPIWrite 0772,49,0,7
SPIWrite 0773,1e,0,7
SPIWrite 0774,09,0,7
SPIWrite 0775,eb,0,7
SPIWrite 0776,02,0,7
SPIWrite 0777,00,0,7
SPIWrite 0778,90,0,7
SPIWrite 0779,f8,0,7
SPIWrite 077a,ed,0,7
SPIWrite 077b,70,0,7
SPIWrite 077c,8d,0,7
SPIWrite 077d,f8,0,7
SPIWrite 077e,05,0,7
SPIWrite 077f,10,0,7
SPIWrite 0780,00,0,7
SPIWrite 0781,2f,0,7
SPIWrite 0782,0c,0,7
SPIWrite 0783,bf,0,7
SPIWrite 0784,01,0,7
SPIWrite 0785,20,0,7
SPIWrite 0786,02,0,7
SPIWrite 0787,20,0,7
SPIWrite 0788,07,0,7
SPIWrite 0789,90,0,7
SPIWrite 078a,0d,0,7
SPIWrite 078b,f1,0,7
SPIWrite 078c,03,0,7
SPIWrite 078d,00,0,7
SPIWrite 078e,03,0,7
SPIWrite 078f,90,0,7
```

```
SPIWrite 0790,03,0,7
SPIWrite 0791,98,0,7
SPIWrite 0792,10,0,7
SPIWrite 0793,f8,0,7
SPIWrite 0794,01,0,7
SPIWrite 0795,6f,0,7
SPIWrite 0796,03,0,7
SPIWrite 0797,90,0,7
SPIWrite 0798,06,0,7
SPIWrite 0799,eb,0,7
SPIWrite 079a,09,0,7
SPIWrite 079b,01,0,7
SPIWrite 079c,91,0,7
SPIWrite 079d,f8,0,7
SPIWrite 079e,6e,0,7
SPIWrite 079f,00,0,7
SPIWrite 07a0,40,0,7
SPIWrite 07a1,1c,0,7
SPIWrite 07a2,c7,0,7
SPIWrite 07a3,b2,0,7
SPIWrite 07a4,00,0,7
SPIWrite 07a5,2f,0,7
SPIWrite 07a6,45,0,7
SPIWrite 07a7,d0,0,7
SPIWrite 07a8,7b,0,7
SPIWrite 07a9,48,0,7
SPIWrite 07aa,dd,0,7
SPIWrite 07ab,f8,0,7
SPIWrite 07ac,28,0,7
SPIWrite 07ad,80,0,7
SPIWrite 07ae,75,0,7
SPIWrite 07af,4d,0,7
SPIWrite 07b0,e1,0,7
SPIWrite 07b1,31,0,7
SPIWrite 07b2,00,0,7
SPIWrite 07b3,24,0,7
SPIWrite 07b4,04,0,7
SPIWrite 07b5,91,0,7
SPIWrite 07b6,30,0,7
SPIWrite 07b7,18,0,7
SPIWrite 07b8,11,0,7
SPIWrite 07b9,30,0,7
SPIWrite 07ba,a8,0,7
SPIWrite 07bb,44,0,7
SPIWrite 07bc,05,0,7
SPIWrite 07bd,90,0,7
SPIWrite 07be,05,0,7
SPIWrite 07bf,98,0,7
SPIWrite 07c0,04,0,7
SPIWrite 07c1,99,0,7
SPIWrite 07c2,03,0,7
SPIWrite 07c3,78,0,7
```

```
SPIWrite 07c4,98,0,7
SPIWrite 07c5,f8,0,7
SPIWrite 07c6,00,0,7
SPIWrite 07c7,50,0,7
SPIWrite 07c8,08,0,7
SPIWrite 07c9,78,0,7
SPIWrite 07ca,23,0,7
SPIWrite 07cb,b1,0,7
SPIWrite 07cc,72,0,7
SPIWrite 07cd,48,0,7
SPIWrite 07ce,04,0,7
SPIWrite 07cf,eb,0,7
SPIWrite 07d0,46,0,7
SPIWrite 07d1,01,0,7
SPIWrite 07d2,40,0,7
SPIWrite 07d3,18,0,7
SPIWrite 07d4,40,0,7
SPIWrite 07d5,7d,0,7
SPIWrite 07d6,0c,0,7
SPIWrite 07d7,99,0,7
SPIWrite 07d8,a9,0,7
SPIWrite 07d9,42,0,7
SPIWrite 07da,27,0,7
SPIWrite 07db,dd,0,7
SPIWrite 07dc,0b,0,7
SPIWrite 07dd,99,0,7
SPIWrite 07de,81,0,7
SPIWrite 07df,42,0,7
SPIWrite 07e0,24,0,7
SPIWrite 07e1,d1,0,7
SPIWrite 07e2,6c,0,7
SPIWrite 07e3,49,0,7
SPIWrite 07e4,d1,0,7
SPIWrite 07e5,f8,0,7
SPIWrite 07e6,2c,0,7
SPIWrite 07e7,c4,0,7
SPIWrite 07e8,99,0,7
SPIWrite 07e9,f8,0,7
SPIWrite 07ea,cc,0,7
SPIWrite 07eb,30,0,7
SPIWrite 07ec,0b,0,7
SPIWrite 07ed,9a,0,7
SPIWrite 07ee,e0,0,7
SPIWrite 07ef,00,0,7
SPIWrite 07f0,00,0,7
SPIWrite 07f1,eb,0,7
SPIWrite 07f2,06,0,7
SPIWrite 07f3,10,0,7
SPIWrite 07f4,48,0,7
SPIWrite 07f5,44,0,7
SPIWrite 07f6,09,0,7
SPIWrite 07f7,99,0,7
```

```
SPIWrite 07f8,c0,0,7
SPIWrite 07f9,68,0,7
SPIWrite 07fa,e0,0,7
SPIWrite 07fb,47,0,7
SPIWrite 07fc,64,0,7
SPIWrite 07fd,49,0,7
SPIWrite 07fe,4f,0,7
SPIWrite 07ff,f4,0,7
SPIWrite 0800,7a,0,7
SPIWrite 0801,72,0,7
SPIWrite 0802,b0,0,7
SPIWrite 0803,fb,0,7
SPIWrite 0804,f2,0,7
SPIWrite 0805,f0,0,7
SPIWrite 0806,59,0,7
SPIWrite 0807,44,0,7
SPIWrite 0808,01,0,7
SPIWrite 0809,eb,0,7
SPIWrite 080a,45,0,7
SPIWrite 080b,01,0,7
SPIWrite 080c,a1,0,7
SPIWrite 080d,f8,0,7
SPIWrite 080e,23,0,7
SPIWrite 080f,00,0,7
SPIWrite 0810,08,0,7
SPIWrite 0811,98,0,7
SPIWrite 0812,51,0,7
SPIWrite 0813,46,0,7
SPIWrite 0814,ff,0,7
SPIWrite 0815,f7,0,7
SPIWrite 0816,44,0,7
SPIWrite 0817,ff,0,7
SPIWrite 0818,5d,0,7
SPIWrite 0819,49,0,7
SPIWrite 081a,98,0,7
SPIWrite 081b,f8,0,7
SPIWrite 081c,00,0,7
SPIWrite 081d,30,0,7
SPIWrite 081e,59,0,7
SPIWrite 081f,44,0,7
SPIWrite 0018,00,0,7  //Property_18h_0_0=0x0;
     Address(0x18[7:0])
SPIWrite 0018,20,0,7  //macro=0x1;    Address(0x18[7:5])
SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,08,0,7  //MACRO_OPERAND_REG0=0x8000000;
     Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
```

```
SPIWrite 00a2,00,0,7
SPIWrite 00a1,00,0,7
SPIWrite 00a0,00,0,7
SPIWrite 00a7,00,0,7  //MACRO_OPERAND_REG1=0x800;
     Address(0xa4[7:0],0xa5[7:0],0xa6[7:0],0xa7[7:0],0xa8[7:0])
SPIWrite 00a6,00,0,7
SPIWrite 00a5,08,0,7
SPIWrite 00a4,00,0,7
SPIWrite 0193,78,0,7  //MACRO_OPCODE=0x78;
     Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
     Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
     Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
     Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
```

```
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIWrite 0144,00,0,7  //Property_124h_4_2=0x0;
      Address(0x144[7:2])
SPIWrite 0018,00,0,7  //macro=0x0;     Address(0x18[7:5])
SPIWrite 0018,01,0,7  //Property_18h_0_0=0x1;
      Address(0x18[7:0])
SPIWrite 0020,6d,0,7
SPIWrite 0021,18,0,7
SPIWrite 0022,85,0,7
SPIWrite 0023,f8,0,7
SPIWrite 0024,2b,0,7
SPIWrite 0025,00,0,7
SPIWrite 0026,59,0,7
SPIWrite 0027,1c,0,7
SPIWrite 0028,88,0,7
SPIWrite 0029,f8,0,7
SPIWrite 002a,00,0,7
SPIWrite 002b,10,0,7
SPIWrite 002c,7f,0,7
SPIWrite 002d,1e,0,7
SPIWrite 002e,04,0,7
SPIWrite 002f,f1,0,7
SPIWrite 0030,01,0,7
SPIWrite 0031,04,0,7
SPIWrite 0032,c4,0,7
SPIWrite 0033,d1,0,7
SPIWrite 0034,07,0,7
SPIWrite 0035,98,0,7
SPIWrite 0036,40,0,7
SPIWrite 0037,1e,0,7
SPIWrite 0038,07,0,7
SPIWrite 0039,90,0,7
SPIWrite 003a,a9,0,7
SPIWrite 003b,d1,0,7
SPIWrite 003c,06,0,7
SPIWrite 003d,98,0,7
SPIWrite 003e,40,0,7
SPIWrite 003f,1e,0,7
SPIWrite 0040,06,0,7
SPIWrite 0041,90,0,7
SPIWrite 0042,7f,0,7
SPIWrite 0043,f4,0,7
SPIWrite 0044,64,0,7
SPIWrite 0045,af,0,7
SPIWrite 0046,0a,0,7
SPIWrite 0047,f1,0,7
```

```
SPIWrite 0048,01,0,7
SPIWrite 0049,0a,0,7
SPIWrite 004a,ba,0,7
SPIWrite 004b,f1,0,7
SPIWrite 004c,03,0,7
SPIWrite 004d,0f,0,7
SPIWrite 004e,ff,0,7
SPIWrite 004f,f6,0,7
SPIWrite 0050,4f,0,7
SPIWrite 0051,af,0,7
SPIWrite 0052,0d,0,7
SPIWrite 0053,b0,0,7
SPIWrite 0054,bd,0,7
SPIWrite 0055,e8,0,7
SPIWrite 0056,f0,0,7
SPIWrite 0057,8f,0,7
SPIWrite 0058,2d,0,7
SPIWrite 0059,e9,0,7
SPIWrite 005a,f0,0,7
SPIWrite 005b,4f,0,7
SPIWrite 005c,81,0,7
SPIWrite 005d,46,0,7
SPIWrite 005e,ad,0,7
SPIWrite 005f,f1,0,7
SPIWrite 0060,24,0,7
SPIWrite 0061,0d,0,7
SPIWrite 0062,e7,0,7
SPIWrite 0063,f7,0,7
SPIWrite 0064,61,0,7
SPIWrite 0065,ff,0,7
SPIWrite 0066,48,0,7
SPIWrite 0067,4c,0,7
SPIWrite 0068,4a,0,7
SPIWrite 0069,4f,0,7
SPIWrite 006a,48,0,7
SPIWrite 006b,4a,0,7
SPIWrite 006c,05,0,7
SPIWrite 006d,90,0,7
SPIWrite 006e,04,0,7
SPIWrite 006f,eb,0,7
SPIWrite 0070,09,0,7
SPIWrite 0071,00,0,7
SPIWrite 0072,d7,0,7
SPIWrite 0073,f8,0,7
SPIWrite 0074,d8,0,7
SPIWrite 0075,31,0,7
SPIWrite 0076,b4,0,7
SPIWrite 0077,f8,0,7
SPIWrite 0078,9e,0,7
SPIWrite 0079,61,0,7
SPIWrite 007a,01,0,7
SPIWrite 007b,79,0,7
```

```
SPIWrite 007c,04,0,7
SPIWrite 007d,20,0,7
SPIWrite 007e,55,0,7
SPIWrite 007f,5c,0,7
SPIWrite 0080,8d,0,7
SPIWrite 0081,f8,0,7
SPIWrite 0082,00,0,7
SPIWrite 0083,00,0,7
SPIWrite 0084,00,0,7
SPIWrite 0085,21,0,7
SPIWrite 0086,48,0,7
SPIWrite 0087,46,0,7
SPIWrite 0088,6a,0,7
SPIWrite 0089,46,0,7
SPIWrite 008a,98,0,7
SPIWrite 008b,47,0,7
SPIWrite 008c,4f,0,7
SPIWrite 008d,f0,0,7
SPIWrite 008e,02,0,7
SPIWrite 008f,0b,0,7
SPIWrite 0090,75,0,7
SPIWrite 0091,43,0,7
SPIWrite 0092,ad,0,7
SPIWrite 0093,f1,0,7
SPIWrite 0094,01,0,7
SPIWrite 0095,00,0,7
SPIWrite 0096,06,0,7
SPIWrite 0097,95,0,7
SPIWrite 0098,df,0,7
SPIWrite 0099,f8,0,7
SPIWrite 009a,f4,0,7
SPIWrite 009b,a0,0,7
SPIWrite 009c,01,0,7
SPIWrite 009d,90,0,7
SPIWrite 009e,09,0,7
SPIWrite 009f,eb,0,7
SPIWrite 00a0,04,0,7
SPIWrite 00a1,00,0,7
SPIWrite 00a2,02,0,7
SPIWrite 00a3,90,0,7
SPIWrite 00a4,01,0,7
SPIWrite 00a5,98,0,7
SPIWrite 00a6,10,0,7
SPIWrite 00a7,f8,0,7
SPIWrite 00a8,01,0,7
SPIWrite 00a9,1f,0,7
SPIWrite 00aa,04,0,7
SPIWrite 00ab,29,0,7
SPIWrite 00ac,01,0,7
SPIWrite 00ad,90,0,7
SPIWrite 00ae,5e,0,7
SPIWrite 00af,d0,0,7
```

```
SPIWrite 00b0,38,0,7
SPIWrite 00b1,48,0,7
SPIWrite 00b2,d0,0,7
SPIWrite 00b3,f8,0,7
SPIWrite 00b4,f8,0,7
SPIWrite 00b5,21,0,7
SPIWrite 00b6,48,0,7
SPIWrite 00b7,46,0,7
SPIWrite 00b8,90,0,7
SPIWrite 00b9,47,0,7
SPIWrite 00ba,01,0,7
SPIWrite 00bb,46,0,7
SPIWrite 00bc,02,0,7
SPIWrite 00bd,98,0,7
SPIWrite 00be,4f,0,7
SPIWrite 00bf,f0,0,7
SPIWrite 00c0,0d,0,7
SPIWrite 00c1,08,0,7
SPIWrite 00c2,01,0,7
SPIWrite 00c3,eb,0,7
SPIWrite 00c4,0a,0,7
SPIWrite 00c5,03,0,7
SPIWrite 00c6,08,0,7
SPIWrite 00c7,fb,0,7
SPIWrite 00c8,01,0,7
SPIWrite 00c9,f8,0,7
SPIWrite 00ca,08,0,7
SPIWrite 00cb,eb,0,7
SPIWrite 00cc,0a,0,7
SPIWrite 00cd,02,0,7
SPIWrite 00ce,9b,0,7
SPIWrite 00cf,7a,0,7
SPIWrite 00d0,90,0,7
SPIWrite 00d1,f8,0,7
SPIWrite 00d2,df,0,7
SPIWrite 00d3,00,0,7
SPIWrite 00d4,92,0,7
SPIWrite 00d5,f8,0,7
SPIWrite 00d6,22,0,7
SPIWrite 00d7,20,0,7
SPIWrite 00d8,07,0,7
SPIWrite 00d9,93,0,7
SPIWrite 00da,40,0,7
SPIWrite 00db,1c,0,7
SPIWrite 00dc,c7,0,7
SPIWrite 00dd,b2,0,7
SPIWrite 00de,08,0,7
SPIWrite 00df,92,0,7
SPIWrite 00e0,00,0,7
SPIWrite 00e1,2f,0,7
SPIWrite 00e2,44,0,7
SPIWrite 00e3,d0,0,7
```

```
SPIWrite 00e4,02,0,7
SPIWrite 00e5,9a,0,7
SPIWrite 00e6,2c,0,7
SPIWrite 00e7,48,0,7
SPIWrite 00e8,26,0,7
SPIWrite 00e9,4d,0,7
SPIWrite 00ea,00,0,7
SPIWrite 00eb,26,0,7
SPIWrite 00ec,e5,0,7
SPIWrite 00ed,32,0,7
SPIWrite 00ee,48,0,7
SPIWrite 00ef,44,0,7
SPIWrite 00f0,6d,0,7
SPIWrite 00f1,18,0,7
SPIWrite 00f2,03,0,7
SPIWrite 00f3,92,0,7
SPIWrite 00f4,21,0,7
SPIWrite 00f5,30,0,7
SPIWrite 00f6,04,0,7
SPIWrite 00f7,90,0,7
SPIWrite 00f8,04,0,7
SPIWrite 00f9,98,0,7
SPIWrite 00fa,03,0,7
SPIWrite 00fb,9a,0,7
SPIWrite 00fc,03,0,7
SPIWrite 00fd,78,0,7
SPIWrite 00fe,2c,0,7
SPIWrite 00ff,78,0,7
SPIWrite 0100,10,0,7
SPIWrite 0101,78,0,7
SPIWrite 0102,2b,0,7
SPIWrite 0103,b1,0,7
SPIWrite 0104,24,0,7
SPIWrite 0105,48,0,7
SPIWrite 0106,06,0,7
SPIWrite 0107,eb,0,7
SPIWrite 0108,89,0,7
SPIWrite 0109,01,0,7
SPIWrite 010a,40,0,7
SPIWrite 010b,18,0,7
SPIWrite 010c,90,0,7
SPIWrite 010d,f8,0,7
SPIWrite 010e,23,0,7
SPIWrite 010f,00,0,7
SPIWrite 0110,08,0,7
SPIWrite 0111,99,0,7
SPIWrite 0112,a1,0,7
SPIWrite 0113,42,0,7
SPIWrite 0114,27,0,7
SPIWrite 0115,dd,0,7
SPIWrite 0116,07,0,7
SPIWrite 0117,99,0,7
```

```
SPIWrite 0118,81,0,7
SPIWrite 0119,42,0,7
SPIWrite 011a,24,0,7
SPIWrite 011b,d1,0,7
SPIWrite 011c,1d,0,7
SPIWrite 011d,4b,0,7
SPIWrite 011e,1a,0,7
SPIWrite 011f,48,0,7
SPIWrite 0120,d3,0,7
SPIWrite 0121,f8,0,7
SPIWrite 0122,2c,0,7
SPIWrite 0123,c4,0,7
SPIWrite 0124,07,0,7
SPIWrite 0125,9a,0,7
SPIWrite 0126,b1,0,7
SPIWrite 0127,00,0,7
SPIWrite 0128,01,0,7
SPIWrite 0129,eb,0,7
SPIWrite 012a,09,0,7
SPIWrite 012b,11,0,7
SPIWrite 012c,40,0,7
SPIWrite 012d,18,0,7
SPIWrite 012e,16,0,7
SPIWrite 012f,49,0,7
SPIWrite 0130,c0,0,7
SPIWrite 0131,6c,0,7
SPIWrite 0132,91,0,7
SPIWrite 0133,f8,0,7
SPIWrite 0134,ce,0,7
SPIWrite 0135,30,0,7
SPIWrite 0136,06,0,7
SPIWrite 0137,99,0,7
SPIWrite 0138,e0,0,7
SPIWrite 0139,47,0,7
SPIWrite 013a,08,0,7
SPIWrite 013b,eb,0,7
SPIWrite 013c,0a,0,7
SPIWrite 013d,01,0,7
SPIWrite 013e,4f,0,7
SPIWrite 013f,f4,0,7
SPIWrite 0140,7a,0,7
SPIWrite 0141,72,0,7
SPIWrite 0142,01,0,7
SPIWrite 0143,eb,0,7
SPIWrite 0144,44,0,7
SPIWrite 0145,01,0,7
SPIWrite 0146,b0,0,7
SPIWrite 0147,fb,0,7
SPIWrite 0148,f2,0,7
SPIWrite 0149,f0,0,7
SPIWrite 014a,a1,0,7
SPIWrite 014b,f8,0,7
```

```
SPIWrite 014c,23,0,7
SPIWrite 014d,00,0,7
SPIWrite 014e,00,0,7
SPIWrite 014f,21,0,7
SPIWrite 0150,48,0,7
SPIWrite 0151,46,0,7
SPIWrite 0152,ff,0,7
SPIWrite 0153,f7,0,7
SPIWrite 0154,a5,0,7
SPIWrite 0155,fe,0,7
SPIWrite 0156,2b,0,7
SPIWrite 0157,78,0,7
SPIWrite 0158,08,0,7
SPIWrite 0159,eb,0,7
SPIWrite 015a,0a,0,7
SPIWrite 015b,01,0,7
SPIWrite 015c,64,0,7
SPIWrite 015d,18,0,7
SPIWrite 015e,84,0,7
SPIWrite 015f,f8,0,7
SPIWrite 0160,2b,0,7
SPIWrite 0161,00,0,7
SPIWrite 0162,59,0,7
SPIWrite 0163,1c,0,7
SPIWrite 0164,29,0,7
SPIWrite 0165,70,0,7
SPIWrite 0166,7f,0,7
SPIWrite 0167,1e,0,7
SPIWrite 0168,06,0,7
SPIWrite 0169,f1,0,7
SPIWrite 016a,01,0,7
SPIWrite 016b,06,0,7
SPIWrite 016c,c4,0,7
SPIWrite 016d,d1,0,7
SPIWrite 016e,bb,0,7
SPIWrite 016f,f1,0,7
SPIWrite 0170,01,0,7
SPIWrite 0171,0b,0,7
SPIWrite 0172,97,0,7
SPIWrite 0173,d1,0,7
SPIWrite 0174,05,0,7
SPIWrite 0175,98,0,7
SPIWrite 0176,09,0,7
SPIWrite 0177,b0,0,7
SPIWrite 0178,bd,0,7
SPIWrite 0179,e8,0,7
SPIWrite 017a,f0,0,7
SPIWrite 017b,8f,0,7
SPIWrite 017c,31,0,7
SPIWrite 017d,78,0,7
SPIWrite 017e,02,0,7
SPIWrite 017f,00,0,7
```

```
SPIWrite 0180,ba,0,7
SPIWrite 0181,01,0,7
SPIWrite 0182,01,0,7
SPIWrite 0183,20,0,7
SPIWrite 0184,e4,0,7
SPIWrite 0185,22,0,7
SPIWrite 0186,01,0,7
SPIWrite 0187,20,0,7
SPIWrite 0188,b4,0,7
SPIWrite 0189,01,0,7
SPIWrite 018a,01,0,7
SPIWrite 018b,20,0,7
SPIWrite 018c,ac,0,7
SPIWrite 018d,78,0,7
SPIWrite 018e,02,0,7
SPIWrite 018f,00,0,7
SPIWrite 0190,98,0,7
SPIWrite 0191,0e,0,7
SPIWrite 0192,01,0,7
SPIWrite 0193,20,0,7
SPIWrite 0194,90,0,7
SPIWrite 0195,d6,0,7
SPIWrite 0196,00,0,7
SPIWrite 0197,20,0,7
SPIWrite 0198,a0,0,7
SPIWrite 0199,13,0,7
SPIWrite 019a,01,0,7
SPIWrite 019b,20,0,7
SPIWrite 019c,2d,0,7
SPIWrite 019d,e9,0,7
SPIWrite 019e,f8,0,7
SPIWrite 019f,4f,0,7
SPIWrite 01a0,89,0,7
SPIWrite 01a1,46,0,7
SPIWrite 01a2,a5,0,7
SPIWrite 01a3,4a,0,7
SPIWrite 01a4,a5,0,7
SPIWrite 01a5,49,0,7
SPIWrite 01a6,80,0,7
SPIWrite 01a7,46,0,7
SPIWrite 01a8,4f,0,7
SPIWrite 01a9,ea,0,7
SPIWrite 01aa,68,0,7
SPIWrite 01ab,00,0,7
SPIWrite 01ac,a1,0,7
SPIWrite 01ad,4b,0,7
SPIWrite 01ae,12,0,7
SPIWrite 01af,5c,0,7
SPIWrite 01b0,09,0,7
SPIWrite 01b1,88,0,7
SPIWrite 01b2,a4,0,7
SPIWrite 01b3,48,0,7
```

```
SPIWrite 01b4,9c,0,7
SPIWrite 01b5,5c,0,7
SPIWrite 01b6,00,0,7
SPIWrite 01b7,68,0,7
SPIWrite 01b8,a1,0,7
SPIWrite 01b9,4a,0,7
SPIWrite 01ba,03,0,7
SPIWrite 01bb,46,0,7
SPIWrite 01bc,4c,0,7
SPIWrite 01bd,43,0,7
SPIWrite 01be,02,0,7
SPIWrite 01bf,eb,0,7
SPIWrite 01c0,c8,0,7
SPIWrite 01c1,02,0,7
SPIWrite 01c2,01,0,7
SPIWrite 01c3,20,0,7
SPIWrite 01c4,21,0,7
SPIWrite 01c5,46,0,7
SPIWrite 01c6,98,0,7
SPIWrite 01c7,47,0,7
SPIWrite 01c8,df,0,7
SPIWrite 01c9,f8,0,7
SPIWrite 01ca,7c,0,7
SPIWrite 01cb,c2,0,7
SPIWrite 01cc,4f,0,7
SPIWrite 01cd,ea,0,7
SPIWrite 01ce,08,0,7
SPIWrite 01cf,1a,0,7
SPIWrite 01d0,00,0,7
SPIWrite 01d1,25,0,7
SPIWrite 01d2,56,0,7
SPIWrite 01d3,46,0,7
SPIWrite 01d4,22,0,7
SPIWrite 01d5,46,0,7
SPIWrite 01d6,02,0,7
SPIWrite 01d7,24,0,7
SPIWrite 01d8,4f,0,7
SPIWrite 01d9,ea,0,7
SPIWrite 01da,12,0,7
SPIWrite 01db,1e,0,7
SPIWrite 01dc,0a,0,7
SPIWrite 01dd,eb,0,7
SPIWrite 01de,05,0,7
SPIWrite 01df,03,0,7
SPIWrite 01e0,06,0,7
SPIWrite 01e1,eb,0,7
SPIWrite 01e2,0c,0,7
SPIWrite 01e3,00,0,7
SPIWrite 01e4,02,0,7
SPIWrite 01e5,27,0,7
SPIWrite 01e6,63,0,7
SPIWrite 01e7,44,0,7
```

```
SPIWrite 01e8,90,0,7
SPIWrite 01e9,30,0,7
SPIWrite 01ea,03,0,7
SPIWrite 01eb,f5,0,7
SPIWrite 01ec,20,0,7
SPIWrite 01ed,7b,0,7
SPIWrite 01ee,50,0,7
SPIWrite 01ef,f8,0,7
SPIWrite 01f0,04,0,7
SPIWrite 01f1,3b,0,7
SPIWrite 01f2,19,0,7
SPIWrite 01f3,01,0,7
SPIWrite 01f4,7f,0,7
SPIWrite 01f5,1e,0,7
SPIWrite 01f6,b1,0,7
SPIWrite 01f7,fb,0,7
SPIWrite 01f8,f2,0,7
SPIWrite 01f9,f1,0,7
SPIWrite 01fa,0e,0,7
SPIWrite 01fb,fb,0,7
SPIWrite 01fc,11,0,7
SPIWrite 01fd,31,0,7
SPIWrite 01fe,4b,0,7
SPIWrite 01ff,f8,0,7
SPIWrite 0200,08,0,7
SPIWrite 0201,1b,0,7
SPIWrite 0202,f4,0,7
SPIWrite 0203,d1,0,7
SPIWrite 0204,64,0,7
SPIWrite 0205,1e,0,7
SPIWrite 0206,06,0,7
SPIWrite 0207,f1,0,7
SPIWrite 0208,08,0,7
SPIWrite 0209,06,0,7
SPIWrite 020a,05,0,7
SPIWrite 020b,f1,0,7
SPIWrite 020c,04,0,7
SPIWrite 020d,05,0,7
SPIWrite 020e,e5,0,7
SPIWrite 020f,d1,0,7
SPIWrite 0210,40,0,7
SPIWrite 0211,46,0,7
SPIWrite 0212,49,0,7
SPIWrite 0213,46,0,7
SPIWrite 0214,e1,0,7
SPIWrite 0215,f7,0,7
SPIWrite 0216,8c,0,7
SPIWrite 0217,fc,0,7
SPIWrite 0218,bd,0,7
SPIWrite 0219,e8,0,7
SPIWrite 021a,f8,0,7
SPIWrite 021b,8f,0,7
```

```
SPIWrite 021c,70,0,7
SPIWrite 021d,b5,0,7
SPIWrite 021e,02,0,7
SPIWrite 021f,46,0,7
SPIWrite 0220,d2,0,7
SPIWrite 0221,f8,0,7
SPIWrite 0222,a4,0,7
SPIWrite 0223,60,0,7
SPIWrite 0224,d2,0,7
SPIWrite 0225,f8,0,7
SPIWrite 0226,44,0,7
SPIWrite 0227,51,0,7
SPIWrite 0228,d2,0,7
SPIWrite 0229,f8,0,7
SPIWrite 022a,04,0,7
SPIWrite 022b,41,0,7
SPIWrite 022c,08,0,7
SPIWrite 022d,46,0,7
SPIWrite 022e,02,0,7
SPIWrite 022f,28,0,7
SPIWrite 0230,0d,0,7
SPIWrite 0231,db,0,7
SPIWrite 0232,40,0,7
SPIWrite 0233,1e,0,7
SPIWrite 0234,01,0,7
SPIWrite 0235,21,0,7
SPIWrite 0236,02,0,7
SPIWrite 0237,eb,0,7
SPIWrite 0238,81,0,7
SPIWrite 0239,03,0,7
SPIWrite 023a,c3,0,7
SPIWrite 023b,f8,0,7
SPIWrite 023c,a4,0,7
SPIWrite 023d,60,0,7
SPIWrite 023e,40,0,7
SPIWrite 023f,1e,0,7
SPIWrite 0240,c3,0,7
SPIWrite 0241,f8,0,7
SPIWrite 0242,44,0,7
SPIWrite 0243,51,0,7
SPIWrite 0244,01,0,7
SPIWrite 0245,f1,0,7
SPIWrite 0246,01,0,7
SPIWrite 0247,01,0,7
SPIWrite 0248,c3,0,7
SPIWrite 0249,f8,0,7
SPIWrite 024a,04,0,7
SPIWrite 024b,41,0,7
SPIWrite 024c,f3,0,7
SPIWrite 024d,d1,0,7
SPIWrite 024e,70,0,7
SPIWrite 024f,bd,0,7
```

```
SPIWrite 0250,10,0,7
SPIWrite 0251,b5,0,7
SPIWrite 0252,04,0,7
SPIWrite 0253,46,0,7
SPIWrite 0254,7d,0,7
SPIWrite 0255,48,0,7
SPIWrite 0256,04,0,7
SPIWrite 0257,70,0,7
SPIWrite 0258,20,0,7
SPIWrite 0259,46,0,7
SPIWrite 025a,e1,0,7
SPIWrite 025b,f7,0,7
SPIWrite 025c,ad,0,7
SPIWrite 025d,ff,0,7
SPIWrite 025e,7c,0,7
SPIWrite 025f,48,0,7
SPIWrite 0260,50,0,7
SPIWrite 0261,f8,0,7
SPIWrite 0262,24,0,7
SPIWrite 0263,00,0,7
SPIWrite 0264,0f,0,7
SPIWrite 0265,21,0,7
SPIWrite 0266,ff,0,7
SPIWrite 0267,f7,0,7
SPIWrite 0268,d9,0,7
SPIWrite 0269,ff,0,7
SPIWrite 026a,10,0,7
SPIWrite 026b,bd,0,7
SPIWrite 026c,70,0,7
SPIWrite 026d,b5,0,7
SPIWrite 026e,04,0,7
SPIWrite 026f,46,0,7
SPIWrite 0270,78,0,7
SPIWrite 0271,48,0,7
SPIWrite 0272,00,0,7
SPIWrite 0273,68,0,7
SPIWrite 0274,16,0,7
SPIWrite 0275,46,0,7
SPIWrite 0276,0d,0,7
SPIWrite 0277,46,0,7
SPIWrite 0278,80,0,7
SPIWrite 0279,47,0,7
SPIWrite 027a,01,0,7
SPIWrite 027b,28,0,7
SPIWrite 027c,31,0,7
SPIWrite 027d,46,0,7
SPIWrite 027e,3c,0,7
SPIWrite 027f,d1,0,7
SPIWrite 0280,4f,0,7
SPIWrite 0281,f0,0,7
SPIWrite 0282,29,0,7
SPIWrite 0283,42,0,7
```

```
SPIWrite 0284,92,0,7
SPIWrite 0285,f8,0,7
SPIWrite 0286,77,0,7
SPIWrite 0287,00,0,7
SPIWrite 0288,40,0,7
SPIWrite 0289,f0,0,7
SPIWrite 028a,08,0,7
SPIWrite 028b,00,0,7
SPIWrite 028c,82,0,7
SPIWrite 028d,f8,0,7
SPIWrite 028e,77,0,7
SPIWrite 028f,00,0,7
SPIWrite 0290,92,0,7
SPIWrite 0291,f8,0,7
SPIWrite 0292,82,0,7
SPIWrite 0293,00,0,7
SPIWrite 0294,00,0,7
SPIWrite 0295,f0,0,7
SPIWrite 0296,c3,0,7
SPIWrite 0297,00,0,7
SPIWrite 0298,0c,0,7
SPIWrite 0299,30,0,7
SPIWrite 029a,82,0,7
SPIWrite 029b,f8,0,7
SPIWrite 029c,82,0,7
SPIWrite 029d,00,0,7
SPIWrite 029e,05,0,7
SPIWrite 029f,eb,0,7
SPIWrite 02a0,04,0,7
SPIWrite 02a1,15,0,7
SPIWrite 02a2,82,0,7
SPIWrite 02a3,f8,0,7
SPIWrite 02a4,76,0,7
SPIWrite 02a5,50,0,7
SPIWrite 02a6,92,0,7
SPIWrite 02a7,f8,0,7
SPIWrite 02a8,77,0,7
SPIWrite 02a9,00,0,7
SPIWrite 02aa,01,0,7
SPIWrite 02ab,f0,0,7
SPIWrite 02ac,03,0,7
SPIWrite 02ad,01,0,7
SPIWrite 02ae,00,0,7
SPIWrite 02af,f0,0,7
SPIWrite 02b0,fc,0,7
SPIWrite 02b1,00,0,7
SPIWrite 02b2,01,0,7
SPIWrite 02b3,43,0,7
SPIWrite 02b4,82,0,7
SPIWrite 02b5,f8,0,7
SPIWrite 02b6,77,0,7
SPIWrite 02b7,10,0,7
```

```
SPIWrite 02b8,92,0,7
SPIWrite 02b9,f8,0,7
SPIWrite 02ba,77,0,7
SPIWrite 02bb,00,0,7
SPIWrite 02bc,00,0,7
SPIWrite 02bd,f0,0,7
SPIWrite 02be,fb,0,7
SPIWrite 02bf,00,0,7
SPIWrite 02c0,82,0,7
SPIWrite 02c1,f8,0,7
SPIWrite 02c2,77,0,7
SPIWrite 02c3,00,0,7
SPIWrite 02c4,92,0,7
SPIWrite 02c5,f8,0,7
SPIWrite 02c6,77,0,7
SPIWrite 02c7,00,0,7
SPIWrite 02c8,40,0,7
SPIWrite 02c9,f0,0,7
SPIWrite 02ca,04,0,7
SPIWrite 02cb,00,0,7
SPIWrite 02cc,82,0,7
SPIWrite 02cd,f8,0,7
SPIWrite 02ce,77,0,7
SPIWrite 02cf,00,0,7
SPIWrite 02d0,92,0,7
SPIWrite 02d1,f8,0,7
SPIWrite 02d2,77,0,7
SPIWrite 02d3,00,0,7
SPIWrite 02d4,00,0,7
SPIWrite 02d5,f0,0,7
SPIWrite 02d6,f7,0,7
SPIWrite 02d7,00,0,7
SPIWrite 02d8,82,0,7
SPIWrite 02d9,f8,0,7
SPIWrite 02da,77,0,7
SPIWrite 02db,00,0,7
SPIWrite 02dc,92,0,7
SPIWrite 02dd,f8,0,7
SPIWrite 02de,82,0,7
SPIWrite 02df,00,0,7
SPIWrite 02e0,00,0,7
SPIWrite 02e1,f0,0,7
SPIWrite 02e2,c3,0,7
SPIWrite 02e3,00,0,7
SPIWrite 02e4,82,0,7
SPIWrite 02e5,f8,0,7
SPIWrite 02e6,82,0,7
SPIWrite 02e7,00,0,7
SPIWrite 02e8,00,0,7
SPIWrite 02e9,26,0,7
SPIWrite 02ea,82,0,7
SPIWrite 02eb,f8,0,7
```

```
SPIWrite 02ec,76,0,7
SPIWrite 02ed,60,0,7
SPIWrite 02ee,92,0,7
SPIWrite 02ef,f8,0,7
SPIWrite 02f0,77,0,7
SPIWrite 02f1,00,0,7
SPIWrite 02f2,00,0,7
SPIWrite 02f3,f0,0,7
SPIWrite 02f4,fc,0,7
SPIWrite 02f5,00,0,7
SPIWrite 02f6,82,0,7
SPIWrite 02f7,f8,0,7
SPIWrite 02f8,77,0,7
SPIWrite 02f9,00,0,7
SPIWrite 02fa,57,0,7
SPIWrite 02fb,48,0,7
SPIWrite 02fc,d0,0,7
SPIWrite 02fd,f8,0,7
SPIWrite 02fe,18,0,7
SPIWrite 02ff,04,0,7
SPIWrite 0300,80,0,7
SPIWrite 0301,47,0,7
SPIWrite 0302,70,0,7
SPIWrite 0303,bd,0,7
SPIWrite 0304,70,0,7
SPIWrite 0305,b5,0,7
SPIWrite 0306,51,0,7
SPIWrite 0307,4c,0,7
SPIWrite 0308,54,0,7
SPIWrite 0309,4b,0,7
SPIWrite 030a,25,0,7
SPIWrite 030b,78,0,7
SPIWrite 030c,03,0,7
SPIWrite 030d,eb,0,7
SPIWrite 030e,65,0,7
SPIWrite 030f,04,0,7
SPIWrite 0310,a6,0,7
SPIWrite 0311,79,0,7
SPIWrite 0312,5b,0,7
SPIWrite 0313,19,0,7
SPIWrite 0314,9c,0,7
SPIWrite 0315,7a,0,7
SPIWrite 0316,52,0,7
SPIWrite 0317,4d,0,7
SPIWrite 0318,73,0,7
SPIWrite 0319,00,0,7
SPIWrite 031a,03,0,7
SPIWrite 031b,eb,0,7
SPIWrite 031c,c6,0,7
SPIWrite 031d,03,0,7
SPIWrite 031e,e4,0,7
SPIWrite 031f,18,0,7
```

```
SPIWrite 0320,2b,0,7
SPIWrite 0321,5d,0,7
SPIWrite 0322,06,0,7
SPIWrite 0323,2b,0,7
SPIWrite 0324,06,0,7
SPIWrite 0325,da,0,7
SPIWrite 0326,8a,0,7
SPIWrite 0327,00,0,7
SPIWrite 0328,83,0,7
SPIWrite 0329,08,0,7
SPIWrite 032a,b2,0,7
SPIWrite 032b,fb,0,7
SPIWrite 032c,f0,0,7
SPIWrite 032d,f0,0,7
SPIWrite 032e,03,0,7
SPIWrite 032f,fb,0,7
SPIWrite 0330,10,0,7
SPIWrite 0331,10,0,7
SPIWrite 0332,70,0,7
SPIWrite 0333,bd,0,7
SPIWrite 0334,e2,0,7
SPIWrite 0335,f7,0,7
SPIWrite 0336,5f,0,7
SPIWrite 0337,fa,0,7
SPIWrite 0338,70,0,7
SPIWrite 0339,bd,0,7
SPIWrite 033a,2d,0,7
SPIWrite 033b,e9,0,7
SPIWrite 033c,f0,0,7
SPIWrite 033d,43,0,7
SPIWrite 033e,4f,0,7
SPIWrite 033f,f0,0,7
SPIWrite 0340,00,0,7
SPIWrite 0341,08,0,7
SPIWrite 0342,04,0,7
SPIWrite 0343,46,0,7
SPIWrite 0344,15,0,7
SPIWrite 0345,46,0,7
SPIWrite 0346,ad,0,7
SPIWrite 0347,f1,0,7
SPIWrite 0348,14,0,7
SPIWrite 0349,0d,0,7
SPIWrite 034a,81,0,7
SPIWrite 034b,f8,0,7
SPIWrite 034c,00,0,7
SPIWrite 034d,80,0,7
SPIWrite 034e,e2,0,7
SPIWrite 034f,f7,0,7
SPIWrite 0350,6f,0,7
SPIWrite 0351,fa,0,7
SPIWrite 0352,42,0,7
SPIWrite 0353,4a,0,7
```

```
SPIWrite 0354,50,0,7
SPIWrite 0355,78,0,7
SPIWrite 0356,01,0,7
SPIWrite 0357,21,0,7
SPIWrite 0358,01,0,7
SPIWrite 0359,fa,0,7
SPIWrite 035a,04,0,7
SPIWrite 035b,f3,0,7
SPIWrite 035c,03,0,7
SPIWrite 035d,42,0,7
SPIWrite 035e,65,0,7
SPIWrite 035f,d0,0,7
SPIWrite 0360,42,0,7
SPIWrite 0361,4b,0,7
SPIWrite 0362,40,0,7
SPIWrite 0363,4e,0,7
SPIWrite 0364,14,0,7
SPIWrite 0365,20,0,7
SPIWrite 0366,17,0,7
SPIWrite 0367,19,0,7
SPIWrite 0368,14,0,7
SPIWrite 0369,fb,0,7
SPIWrite 036a,00,0,7
SPIWrite 036b,f0,0,7
SPIWrite 036c,1b,0,7
SPIWrite 036d,58,0,7
SPIWrite 036e,38,0,7
SPIWrite 036f,7a,0,7
SPIWrite 0370,3d,0,7
SPIWrite 0371,4f,0,7
SPIWrite 0372,30,0,7
SPIWrite 0373,5c,0,7
SPIWrite 0374,b7,0,7
SPIWrite 0375,f8,0,7
SPIWrite 0376,9e,0,7
SPIWrite 0377,61,0,7
SPIWrite 0378,70,0,7
SPIWrite 0379,43,0,7
SPIWrite 037a,18,0,7
SPIWrite 037b,26,0,7
SPIWrite 037c,14,0,7
SPIWrite 037d,fb,0,7
SPIWrite 037e,06,0,7
SPIWrite 037f,2c,0,7
SPIWrite 0380,0c,0,7
SPIWrite 0381,eb,0,7
SPIWrite 0382,c5,0,7
SPIWrite 0383,0e,0,7
SPIWrite 0384,de,0,7
SPIWrite 0385,f8,0,7
SPIWrite 0386,d0,0,7
SPIWrite 0387,60,0,7
```

```
SPIWrite 0388,b2,0,7
SPIWrite 0389,00,0,7
SPIWrite 038a,b2,0,7
SPIWrite 038b,fb,0,7
SPIWrite 038c,f0,0,7
SPIWrite 038d,f9,0,7
SPIWrite 038e,82,0,7
SPIWrite 038f,08,0,7
SPIWrite 0390,02,0,7
SPIWrite 0391,fb,0,7
SPIWrite 0392,19,0,7
SPIWrite 0393,66,0,7
SPIWrite 0394,00,0,7
SPIWrite 0395,96,0,7
SPIWrite 0396,de,0,7
SPIWrite 0397,f8,0,7
SPIWrite 0398,d4,0,7
SPIWrite 0399,60,0,7
SPIWrite 039a,4f,0,7
SPIWrite 039b,ea,0,7
SPIWrite 039c,86,0,7
SPIWrite 039d,0e,0,7
SPIWrite 039e,be,0,7
SPIWrite 039f,fb,0,7
SPIWrite 03a0,f0,0,7
SPIWrite 03a1,fe,0,7
SPIWrite 03a2,02,0,7
SPIWrite 03a3,fb,0,7
SPIWrite 03a4,1e,0,7
SPIWrite 03a5,66,0,7
SPIWrite 03a6,01,0,7
SPIWrite 03a7,96,0,7
SPIWrite 03a8,dc,0,7
SPIWrite 03a9,f8,0,7
SPIWrite 03aa,e0,0,7
SPIWrite 03ab,60,0,7
SPIWrite 03ac,4f,0,7
SPIWrite 03ad,ea,0,7
SPIWrite 03ae,86,0,7
SPIWrite 03af,0e,0,7
SPIWrite 03b0,be,0,7
SPIWrite 03b1,fb,0,7
SPIWrite 03b2,f0,0,7
SPIWrite 03b3,fe,0,7
SPIWrite 03b4,02,0,7
SPIWrite 03b5,fb,0,7
SPIWrite 03b6,1e,0,7
SPIWrite 03b7,66,0,7
SPIWrite 03b8,02,0,7
SPIWrite 03b9,96,0,7
SPIWrite 03ba,dc,0,7
SPIWrite 03bb,f8,0,7
```

```
SPIWrite 03bc,e4,0,7
SPIWrite 03bd,60,0,7
SPIWrite 03be,3f,0,7
SPIWrite 03bf,19,0,7
SPIWrite 03c0,4f,0,7
SPIWrite 03c1,ea,0,7
SPIWrite 03c2,86,0,7
SPIWrite 03c3,0c,0,7
SPIWrite 03c4,bc,0,7
SPIWrite 03c5,fb,0,7
SPIWrite 03c6,f0,0,7
SPIWrite 03c7,f0,0,7
SPIWrite 03c8,02,0,7
SPIWrite 03c9,fb,0,7
SPIWrite 03ca,10,0,7
SPIWrite 03cb,60,0,7
SPIWrite 03cc,03,0,7
SPIWrite 03cd,90,0,7
SPIWrite 03ce,97,0,7
SPIWrite 03cf,f8,0,7
SPIWrite 03d0,6c,0,7
SPIWrite 03d1,00,0,7
SPIWrite 03d2,0a,0,7
SPIWrite 03d3,46,0,7
SPIWrite 03d4,03,0,7
SPIWrite 03d5,28,0,7
SPIWrite 03d6,07,0,7
SPIWrite 03d7,d0,0,7
SPIWrite 03d8,0a,0,7
SPIWrite 03d9,28,0,7
SPIWrite 03da,05,0,7
SPIWrite 03db,d0,0,7
SPIWrite 03dc,0b,0,7
SPIWrite 03dd,28,0,7
SPIWrite 03de,03,0,7
SPIWrite 03df,d0,0,7
SPIWrite 03e0,0c,0,7
SPIWrite 03e1,28,0,7
SPIWrite 03e2,1c,0,7
SPIWrite 03e3,bf,0,7
SPIWrite 03e4,0d,0,7
SPIWrite 03e5,28,0,7
SPIWrite 03e6,42,0,7
SPIWrite 03e7,46,0,7
SPIWrite 03e8,12,0,7
SPIWrite 03e9,fb,0,7
SPIWrite 03ea,05,0,7
SPIWrite 03eb,f0,0,7
SPIWrite 03ec,4f,0,7
SPIWrite 03ed,f4,0,7
SPIWrite 03ee,80,0,7
SPIWrite 03ef,72,0,7
```

```
SPIWrite 03f0,04,0,7
SPIWrite 03f1,27,0,7
SPIWrite 03f2,ec,0,7
SPIWrite 03f3,46,0,7
SPIWrite 03f4,02,0,7
SPIWrite 03f5,eb,0,7
SPIWrite 03f6,40,0,7
SPIWrite 03f7,12,0,7
SPIWrite 03f8,96,0,7
SPIWrite 03f9,b2,0,7
SPIWrite 03fa,40,0,7
SPIWrite 03fb,46,0,7
SPIWrite 03fc,5c,0,7
SPIWrite 03fd,f8,0,7
SPIWrite 03fe,04,0,7
SPIWrite 03ff,2b,0,7
SPIWrite 0400,35,0,7
SPIWrite 0401,18,0,7
SPIWrite 0402,7f,0,7
SPIWrite 0403,1e,0,7
SPIWrite 0404,00,0,7
SPIWrite 0405,f1,0,7
SPIWrite 0406,04,0,7
SPIWrite 0407,00,0,7
SPIWrite 0408,5a,0,7
SPIWrite 0409,51,0,7
SPIWrite 040a,f7,0,7
SPIWrite 040b,d1,0,7
SPIWrite 040c,18,0,7
SPIWrite 040d,4a,0,7
SPIWrite 040e,15,0,7
SPIWrite 040f,20,0,7
SPIWrite 0410,14,0,7
SPIWrite 0411,fb,0,7
SPIWrite 0412,00,0,7
SPIWrite 0413,f0,0,7
SPIWrite 0414,10,0,7
SPIWrite 0415,5c,0,7
SPIWrite 0416,06,0,7
SPIWrite 0417,28,0,7
SPIWrite 0418,03,0,7
SPIWrite 0419,d0,0,7
SPIWrite 041a,40,0,7
SPIWrite 041b,08,0,7
SPIWrite 041c,2c,0,7
SPIWrite 041d,bf,0,7
SPIWrite 041e,0f,0,7
SPIWrite 041f,21,0,7
SPIWrite 0420,07,0,7
SPIWrite 0421,21,0,7
SPIWrite 0422,14,0,7
SPIWrite 0423,48,0,7
```

```
SPIWrite 0424,50,0,7
SPIWrite 0425,f8,0,7
SPIWrite 0426,24,0,7
SPIWrite 0427,00,0,7
SPIWrite 0428,ff,0,7
SPIWrite 0429,f7,0,7
SPIWrite 042a,f8,0,7
SPIWrite 042b,fe,0,7
SPIWrite 042c,05,0,7
SPIWrite 042d,b0,0,7
SPIWrite 042e,bd,0,7
SPIWrite 042f,e8,0,7
SPIWrite 0430,f0,0,7
SPIWrite 0431,83,0,7
SPIWrite 0432,c0,0,7
SPIWrite 0433,46,0,7
SPIWrite 0434,3b,0,7
SPIWrite 0435,78,0,7
SPIWrite 0436,02,0,7
SPIWrite 0437,00,0,7
SPIWrite 0438,17,0,7
SPIWrite 0439,01,0,7
SPIWrite 043a,01,0,7
SPIWrite 043b,20,0,7
SPIWrite 043c,52,0,7
SPIWrite 043d,03,0,7
SPIWrite 043e,01,0,7
SPIWrite 043f,20,0,7
SPIWrite 0440,34,0,7
SPIWrite 0441,fe,0,7
SPIWrite 0442,00,0,7
SPIWrite 0443,20,0,7
SPIWrite 0444,bc,0,7
SPIWrite 0445,dc,0,7
SPIWrite 0446,00,0,7
SPIWrite 0447,20,0,7
SPIWrite 0448,d4,0,7
SPIWrite 0449,fb,0,7
SPIWrite 044a,00,0,7
SPIWrite 044b,20,0,7
SPIWrite 044c,f5,0,7
SPIWrite 044d,22,0,7
SPIWrite 044e,01,0,7
SPIWrite 044f,20,0,7
SPIWrite 0450,9c,0,7
SPIWrite 0451,77,0,7
SPIWrite 0452,02,0,7
SPIWrite 0453,00,0,7
SPIWrite 0454,a4,0,7
SPIWrite 0455,da,0,7
SPIWrite 0456,00,0,7
SPIWrite 0457,20,0,7
```

```
SPIWrite 0458,90,0,7
SPIWrite 0459,d6,0,7
SPIWrite 045a,00,0,7
SPIWrite 045b,20,0,7
SPIWrite 045c,18,0,7
SPIWrite 045d,ff,0,7
SPIWrite 045e,00,0,7
SPIWrite 045f,20,0,7
SPIWrite 0460,b8,0,7
SPIWrite 0461,16,0,7
SPIWrite 0462,01,0,7
SPIWrite 0463,20,0,7
SPIWrite 0464,ac,0,7
SPIWrite 0465,78,0,7
SPIWrite 0466,02,0,7
SPIWrite 0467,00,0,7
SPIWrite 0468,b4,0,7
SPIWrite 0469,01,0,7
SPIWrite 046a,01,0,7
SPIWrite 046b,20,0,7
SPIWrite 046c,d8,0,7
SPIWrite 046d,74,0,7
SPIWrite 046e,02,0,7
SPIWrite 046f,00,0,7
SPIWrite 0470,32,0,7
SPIWrite 0471,d4,0,7
SPIWrite 0472,00,0,7
SPIWrite 0473,20,0,7
SPIWrite 0474,90,0,7
SPIWrite 0475,78,0,7
SPIWrite 0476,02,0,7
SPIWrite 0477,00,0,7
SPIWrite 0478,f8,0,7
SPIWrite 0479,b5,0,7
SPIWrite 047a,50,0,7
SPIWrite 047b,49,0,7
SPIWrite 047c,4e,0,7
SPIWrite 047d,4c,0,7
SPIWrite 047e,50,0,7
SPIWrite 047f,48,0,7
SPIWrite 0480,56,0,7
SPIWrite 0481,4b,0,7
SPIWrite 0482,c4,0,7
SPIWrite 0483,f8,0,7
SPIWrite 0484,fc,0,7
SPIWrite 0485,10,0,7
SPIWrite 0486,4f,0,7
SPIWrite 0487,49,0,7
SPIWrite 0488,c4,0,7
SPIWrite 0489,f8,0,7
SPIWrite 048a,c4,0,7
SPIWrite 048b,00,0,7
```

```
SPIWrite 048c,02,0,7
SPIWrite 048d,27,0,7
SPIWrite 048e,c4,0,7
SPIWrite 048f,f8,0,7
SPIWrite 0490,c0,0,7
SPIWrite 0491,10,0,7
SPIWrite 0492,4f,0,7
SPIWrite 0493,48,0,7
SPIWrite 0494,1f,0,7
SPIWrite 0495,70,0,7
SPIWrite 0496,4f,0,7
SPIWrite 0497,49,0,7
SPIWrite 0498,c4,0,7
SPIWrite 0499,f8,0,7
SPIWrite 049a,30,0,7
SPIWrite 049b,01,0,7
SPIWrite 049c,4e,0,7
SPIWrite 049d,48,0,7
SPIWrite 049e,c4,0,7
SPIWrite 049f,f8,0,7
SPIWrite 04a0,40,0,7
SPIWrite 04a1,11,0,7
SPIWrite 04a2,5b,0,7
SPIWrite 04a3,49,0,7
SPIWrite 04a4,c4,0,7
SPIWrite 04a5,f8,0,7
SPIWrite 04a6,38,0,7
SPIWrite 04a7,01,0,7
SPIWrite 04a8,5a,0,7
SPIWrite 04a9,48,0,7
SPIWrite 04aa,c4,0,7
SPIWrite 04ab,f8,0,7
SPIWrite 04ac,a8,0,7
SPIWrite 04ad,16,0,7
SPIWrite 04ae,5a,0,7
SPIWrite 04af,49,0,7
SPIWrite 04b0,c4,0,7
SPIWrite 04b1,f8,0,7
SPIWrite 04b2,ac,0,7
SPIWrite 04b3,06,0,7
SPIWrite 04b4,59,0,7
SPIWrite 04b5,48,0,7
SPIWrite 04b6,c4,0,7
SPIWrite 04b7,f8,0,7
SPIWrite 04b8,f4,0,7
SPIWrite 04b9,15,0,7
SPIWrite 04ba,59,0,7
SPIWrite 04bb,4a,0,7
SPIWrite 04bc,a0,0,7
SPIWrite 04bd,64,0,7
SPIWrite 04be,00,0,7
SPIWrite 04bf,26,0,7
```

```
SPIWrite 04c0,c4,0,7
SPIWrite 04c1,f8,0,7
SPIWrite 04c2,3c,0,7
SPIWrite 04c3,26,0,7
SPIWrite 04c4,46,0,7
SPIWrite 04c5,4a,0,7
SPIWrite 04c6,57,0,7
SPIWrite 04c7,49,0,7
SPIWrite 04c8,16,0,7
SPIWrite 04c9,70,0,7
SPIWrite 04ca,57,0,7
SPIWrite 04cb,48,0,7
SPIWrite 04cc,c4,0,7
SPIWrite 04cd,f8,0,7
SPIWrite 04ce,30,0,7
SPIWrite 04cf,16,0,7
SPIWrite 04d0,44,0,7
SPIWrite 04d1,49,0,7
SPIWrite 04d2,c4,0,7
SPIWrite 04d3,f8,0,7
SPIWrite 04d4,40,0,7
SPIWrite 04d5,06,0,7
SPIWrite 04d6,49,0,7
SPIWrite 04d7,48,0,7
SPIWrite 04d8,0e,0,7
SPIWrite 04d9,70,0,7
SPIWrite 04da,a6,0,7
SPIWrite 04db,22,0,7
SPIWrite 04dc,42,0,7
SPIWrite 04dd,80,0,7
SPIWrite 04de,40,0,7
SPIWrite 04df,f2,0,7
SPIWrite 04e0,b7,0,7
SPIWrite 04e1,51,0,7
SPIWrite 04e2,81,0,7
SPIWrite 04e3,80,0,7
SPIWrite 04e4,28,0,7
SPIWrite 04e5,23,0,7
SPIWrite 04e6,03,0,7
SPIWrite 04e7,80,0,7
SPIWrite 04e8,41,0,7
SPIWrite 04e9,f2,0,7
SPIWrite 04ea,88,0,7
SPIWrite 04eb,32,0,7
SPIWrite 04ec,47,0,7
SPIWrite 04ed,49,0,7
SPIWrite 04ee,c2,0,7
SPIWrite 04ef,60,0,7
SPIWrite 04f0,35,0,7
SPIWrite 04f1,4d,0,7
SPIWrite 04f2,0e,0,7
SPIWrite 04f3,70,0,7
```

```
SPIWrite 04f4,03,0,7
SPIWrite 04f5,23,0,7
SPIWrite 04f6,83,0,7
SPIWrite 04f7,71,0,7
SPIWrite 04f8,3b,0,7
SPIWrite 04f9,4a,0,7
SPIWrite 04fa,3c,0,7
SPIWrite 04fb,49,0,7
SPIWrite 04fc,c5,0,7
SPIWrite 04fd,f8,0,7
SPIWrite 04fe,f4,0,7
SPIWrite 04ff,21,0,7
SPIWrite 0500,32,0,7
SPIWrite 0501,4b,0,7
SPIWrite 0502,c5,0,7
SPIWrite 0503,f8,0,7
SPIWrite 0504,38,0,7
SPIWrite 0505,12,0,7
SPIWrite 0506,3a,0,7
SPIWrite 0507,4a,0,7
SPIWrite 0508,c5,0,7
SPIWrite 0509,f8,0,7
SPIWrite 050a,84,0,7
SPIWrite 050b,31,0,7
SPIWrite 050c,3a,0,7
SPIWrite 050d,49,0,7
SPIWrite 050e,c5,0,7
SPIWrite 050f,f8,0,7
SPIWrite 0510,3c,0,7
SPIWrite 0511,22,0,7
SPIWrite 0512,38,0,7
SPIWrite 0513,4a,0,7
SPIWrite 0514,11,0,7
SPIWrite 0515,60,0,7
SPIWrite 0516,3a,0,7
SPIWrite 0517,49,0,7
SPIWrite 0518,81,0,7
SPIWrite 0519,60,0,7
SPIWrite 051a,3a,0,7
SPIWrite 051b,49,0,7
SPIWrite 051c,01,0,7
SPIWrite 051d,61,0,7
SPIWrite 051e,3a,0,7
SPIWrite 051f,48,0,7
SPIWrite 0520,a8,0,7
SPIWrite 0521,65,0,7
SPIWrite 0522,42,0,7
SPIWrite 0523,48,0,7
SPIWrite 0524,c4,0,7
SPIWrite 0525,f8,0,7
SPIWrite 0526,34,0,7
SPIWrite 0527,06,0,7
```

```
SPIWrite 0528,00,0,7
SPIWrite 0529,f0,0,7
SPIWrite 052a,88,0,7
SPIWrite 052b,fd,0,7
SPIWrite 052c,00,0,7
SPIWrite 052d,f0,0,7
SPIWrite 052e,17,0,7
SPIWrite 052f,fa,0,7
SPIWrite 0530,3f,0,7
SPIWrite 0531,48,0,7
SPIWrite 0532,40,0,7
SPIWrite 0533,49,0,7
SPIWrite 0534,00,0,7
SPIWrite 0535,f0,0,7
SPIWrite 0536,b4,0,7
SPIWrite 0537,f9,0,7
SPIWrite 0538,40,0,7
SPIWrite 0539,48,0,7
SPIWrite 053a,c4,0,7
SPIWrite 053b,f8,0,7
SPIWrite 053c,70,0,7
SPIWrite 053d,09,0,7
SPIWrite 053e,41,0,7
SPIWrite 053f,49,0,7
SPIWrite 0540,c4,0,7
SPIWrite 0541,f8,0,7
SPIWrite 0542,4c,0,7
SPIWrite 0543,15,0,7
SPIWrite 0544,4a,0,7
SPIWrite 0545,4a,0,7
SPIWrite 0546,17,0,7
SPIWrite 0547,70,0,7
SPIWrite 0548,3f,0,7
SPIWrite 0549,48,0,7
SPIWrite 054a,c4,0,7
SPIWrite 054b,f8,0,7
SPIWrite 054c,38,0,7
SPIWrite 054d,06,0,7
SPIWrite 054e,3f,0,7
SPIWrite 054f,49,0,7
SPIWrite 0550,c4,0,7
SPIWrite 0551,f8,0,7
SPIWrite 0552,c4,0,7
SPIWrite 0553,14,0,7
SPIWrite 0554,3e,0,7
SPIWrite 0555,48,0,7
SPIWrite 0556,c4,0,7
SPIWrite 0557,f8,0,7
SPIWrite 0558,94,0,7
SPIWrite 0559,04,0,7
SPIWrite 055a,3e,0,7
SPIWrite 055b,49,0,7
```

```
SPIWrite 055c,c4,0,7
SPIWrite 055d,f8,0,7
SPIWrite 055e,98,0,7
SPIWrite 055f,14,0,7
SPIWrite 0560,3d,0,7
SPIWrite 0561,48,0,7
SPIWrite 0562,c4,0,7
SPIWrite 0563,f8,0,7
SPIWrite 0564,00,0,7
SPIWrite 0565,02,0,7
SPIWrite 0566,3d,0,7
SPIWrite 0567,49,0,7
SPIWrite 0568,c4,0,7
SPIWrite 0569,f8,0,7
SPIWrite 056a,04,0,7
SPIWrite 056b,12,0,7
SPIWrite 056c,3d,0,7
SPIWrite 056d,48,0,7
SPIWrite 056e,c4,0,7
SPIWrite 056f,f8,0,7
SPIWrite 0570,24,0,7
SPIWrite 0571,03,0,7
SPIWrite 0572,3d,0,7
SPIWrite 0573,49,0,7
SPIWrite 0574,c4,0,7
SPIWrite 0575,f8,0,7
SPIWrite 0576,94,0,7
SPIWrite 0577,11,0,7
SPIWrite 0578,3c,0,7
SPIWrite 0579,48,0,7
SPIWrite 057a,c4,0,7
SPIWrite 057b,f8,0,7
SPIWrite 057c,c4,0,7
SPIWrite 057d,02,0,7
SPIWrite 057e,30,0,7
SPIWrite 057f,48,0,7
SPIWrite 0580,3d,0,7
SPIWrite 0581,49,0,7
SPIWrite 0582,06,0,7
SPIWrite 0583,70,0,7
SPIWrite 0584,01,0,7
SPIWrite 0585,20,0,7
SPIWrite 0586,c4,0,7
SPIWrite 0587,f8,0,7
SPIWrite 0588,4c,0,7
SPIWrite 0589,14,0,7
SPIWrite 058a,3a,0,7
SPIWrite 058b,49,0,7
SPIWrite 058c,3b,0,7
SPIWrite 058d,4a,0,7
SPIWrite 058e,08,0,7
SPIWrite 058f,80,0,7
```

```
SPIWrite 0590,3c,0,7
SPIWrite 0591,48,0,7
SPIWrite 0592,16,0,7
SPIWrite 0593,70,0,7
SPIWrite 0594,16,0,7
SPIWrite 0595,21,0,7
SPIWrite 0596,41,0,7
SPIWrite 0597,70,0,7
SPIWrite 0598,07,0,7
SPIWrite 0599,21,0,7
SPIWrite 059a,81,0,7
SPIWrite 059b,70,0,7
SPIWrite 059c,14,0,7
SPIWrite 059d,21,0,7
SPIWrite 059e,c1,0,7
SPIWrite 059f,70,0,7
SPIWrite 05a0,a2,0,7
SPIWrite 05a1,21,0,7
SPIWrite 05a2,81,0,7
SPIWrite 05a3,80,0,7
SPIWrite 05a4,24,0,7
SPIWrite 05a5,48,0,7
SPIWrite 05a6,c5,0,7
SPIWrite 05a7,f8,0,7
SPIWrite 05a8,34,0,7
SPIWrite 05a9,02,0,7
SPIWrite 05aa,2d,0,7
SPIWrite 05ab,48,0,7
SPIWrite 05ac,c5,0,7
SPIWrite 05ad,f8,0,7
SPIWrite 05ae,f8,0,7
SPIWrite 05af,00,0,7
SPIWrite 05b0,33,0,7
SPIWrite 05b1,48,0,7
SPIWrite 05b2,c4,0,7
SPIWrite 05b3,f8,0,7
SPIWrite 05b4,c8,0,7
SPIWrite 05b5,04,0,7
SPIWrite 05b6,f8,0,7
SPIWrite 05b7,bd,0,7
SPIWrite 05b8,90,0,7
SPIWrite 05b9,d6,0,7
SPIWrite 05ba,00,0,7
SPIWrite 05bb,20,0,7
SPIWrite 05bc,d3,0,7
SPIWrite 05bd,1a,0,7
SPIWrite 05be,03,0,7
SPIWrite 05bf,00,0,7
SPIWrite 05c0,55,0,7
SPIWrite 05c1,1a,0,7
SPIWrite 05c2,03,0,7
SPIWrite 05c3,00,0,7
```

```
SPIWrite 05c4,d5,0,7
SPIWrite 05c5,19,0,7
SPIWrite 05c6,03,0,7
SPIWrite 05c7,00,0,7
SPIWrite 05c8,d4,0,7
SPIWrite 05c9,f7,0,7
SPIWrite 05ca,00,0,7
SPIWrite 05cb,20,0,7
SPIWrite 05cc,65,0,7
SPIWrite 05cd,05,0,7
SPIWrite 05ce,03,0,7
SPIWrite 05cf,00,0,7
SPIWrite 05d0,cf,0,7
SPIWrite 05d1,17,0,7
SPIWrite 05d2,03,0,7
SPIWrite 05d3,00,0,7
SPIWrite 05d4,6b,0,7
SPIWrite 05d5,16,0,7
SPIWrite 05d6,03,0,7
SPIWrite 05d7,00,0,7
SPIWrite 05d8,f9,0,7
SPIWrite 05d9,16,0,7
SPIWrite 05da,03,0,7
SPIWrite 05db,00,0,7
SPIWrite 05dc,2b,0,7
SPIWrite 05dd,22,0,7
SPIWrite 05de,01,0,7
SPIWrite 05df,20,0,7
SPIWrite 05e0,f2,0,7
SPIWrite 05e1,22,0,7
SPIWrite 05e2,01,0,7
SPIWrite 05e3,20,0,7
SPIWrite 05e4,f3,0,7
SPIWrite 05e5,22,0,7
SPIWrite 05e6,01,0,7
SPIWrite 05e7,20,0,7
SPIWrite 05e8,91,0,7
SPIWrite 05e9,04,0,7
SPIWrite 05ea,03,0,7
SPIWrite 05eb,00,0,7
SPIWrite 05ec,7d,0,7
SPIWrite 05ed,0c,0,7
SPIWrite 05ee,03,0,7
SPIWrite 05ef,00,0,7
SPIWrite 05f0,b1,0,7
SPIWrite 05f1,0d,0,7
SPIWrite 05f2,03,0,7
SPIWrite 05f3,00,0,7
SPIWrite 05f4,ec,0,7
SPIWrite 05f5,22,0,7
SPIWrite 05f6,01,0,7
SPIWrite 05f7,20,0,7
```

```
SPIWrite 05f8,00,0,7
SPIWrite 05f9,00,0,7
SPIWrite 05fa,02,0,7
SPIWrite 05fb,ac,0,7
SPIWrite 05fc,a4,0,7
SPIWrite 05fd,22,0,7
SPIWrite 05fe,01,0,7
SPIWrite 05ff,20,0,7
SPIWrite 0600,40,0,7
SPIWrite 0601,78,0,7
SPIWrite 0602,7d,0,7
SPIWrite 0603,01,0,7
SPIWrite 0604,48,0,7
SPIWrite 0605,e8,0,7
SPIWrite 0606,01,0,7
SPIWrite 0607,00,0,7
SPIWrite 0608,1d,0,7
SPIWrite 0609,1b,0,7
SPIWrite 060a,03,0,7
SPIWrite 060b,00,0,7
SPIWrite 060c,f4,0,7
SPIWrite 060d,22,0,7
SPIWrite 060e,01,0,7
SPIWrite 060f,20,0,7
SPIWrite 0610,6b,0,7
SPIWrite 0611,1e,0,7
SPIWrite 0612,03,0,7
SPIWrite 0613,00,0,7
SPIWrite 0614,5f,0,7
SPIWrite 0615,1e,0,7
SPIWrite 0616,03,0,7
SPIWrite 0617,00,0,7
SPIWrite 0618,85,0,7
SPIWrite 0619,1f,0,7
SPIWrite 061a,03,0,7
SPIWrite 061b,00,0,7
SPIWrite 061c,5f,0,7
SPIWrite 061d,1d,0,7
SPIWrite 061e,03,0,7
SPIWrite 061f,00,0,7
SPIWrite 0620,7d,0,7
SPIWrite 0621,11,0,7
SPIWrite 0622,03,0,7
SPIWrite 0623,00,0,7
SPIWrite 0624,31,0,7
SPIWrite 0625,12,0,7
SPIWrite 0626,03,0,7
SPIWrite 0627,00,0,7
SPIWrite 0628,e5,0,7
SPIWrite 0629,12,0,7
SPIWrite 062a,03,0,7
SPIWrite 062b,00,0,7
```

```
SPIWrite 062c,1b,0,7
SPIWrite 062d,13,0,7
SPIWrite 062e,03,0,7
SPIWrite 062f,00,0,7
SPIWrite 0630,4c,0,7
SPIWrite 0631,21,0,7
SPIWrite 0632,03,0,7
SPIWrite 0633,00,0,7
SPIWrite 0634,74,0,7
SPIWrite 0635,21,0,7
SPIWrite 0636,03,0,7
SPIWrite 0637,00,0,7
SPIWrite 0638,19,0,7
SPIWrite 0639,1c,0,7
SPIWrite 063a,03,0,7
SPIWrite 063b,00,0,7
SPIWrite 063c,7b,0,7
SPIWrite 063d,19,0,7
SPIWrite 063e,03,0,7
SPIWrite 063f,00,0,7
SPIWrite 0640,f6,0,7
SPIWrite 0641,22,0,7
SPIWrite 0642,01,0,7
SPIWrite 0643,20,0,7
SPIWrite 0644,e9,0,7
SPIWrite 0645,1e,0,7
SPIWrite 0646,03,0,7
SPIWrite 0647,00,0,7
SPIWrite 0648,05,0,7
SPIWrite 0649,19,0,7
SPIWrite 064a,03,0,7
SPIWrite 064b,00,0,7
SPIWrite 064c,09,0,7
SPIWrite 064d,20,0,7
SPIWrite 064e,03,0,7
SPIWrite 064f,00,0,7
SPIWrite 0650,97,0,7
SPIWrite 0651,0e,0,7
SPIWrite 0652,03,0,7
SPIWrite 0653,00,0,7
SPIWrite 0654,39,0,7
SPIWrite 0655,10,0,7
SPIWrite 0656,03,0,7
SPIWrite 0657,00,0,7
SPIWrite 0658,bd,0,7
SPIWrite 0659,1f,0,7
SPIWrite 065a,03,0,7
SPIWrite 065b,00,0,7
SPIWrite 065c,cb,0,7
SPIWrite 065d,1f,0,7
SPIWrite 065e,03,0,7
SPIWrite 065f,00,0,7
```

```
SPIWrite 0660,2f,0,7
SPIWrite 0661,1b,0,7
SPIWrite 0662,03,0,7
SPIWrite 0663,00,0,7
SPIWrite 0664,ed,0,7
SPIWrite 0665,1f,0,7
SPIWrite 0666,03,0,7
SPIWrite 0667,00,0,7
SPIWrite 0668,45,0,7
SPIWrite 0669,1f,0,7
SPIWrite 066a,03,0,7
SPIWrite 066b,00,0,7
SPIWrite 066c,b7,0,7
SPIWrite 066d,1e,0,7
SPIWrite 066e,03,0,7
SPIWrite 066f,00,0,7
SPIWrite 0670,f7,0,7
SPIWrite 0671,22,0,7
SPIWrite 0672,01,0,7
SPIWrite 0673,20,0,7
SPIWrite 0674,f0,0,7
SPIWrite 0675,22,0,7
SPIWrite 0676,01,0,7
SPIWrite 0677,20,0,7
SPIWrite 0678,45,0,7
SPIWrite 0679,1c,0,7
SPIWrite 067a,03,0,7
SPIWrite 067b,00,0,7
SPIWrite 067c,a1,0,7
SPIWrite 067d,13,0,7
SPIWrite 067e,01,0,7
SPIWrite 067f,20,0,7
SPIWrite 0680,0b,0,7
SPIWrite 0681,20,0,7
SPIWrite 0682,03,0,7
SPIWrite 0683,00,0,7
SPIWrite 0684,3c,0,7
SPIWrite 0685,d6,0,7
SPIWrite 0686,00,0,7
SPIWrite 0687,20,0,7
SPIWrite 0688,70,0,7
SPIWrite 0689,47,0,7
SPIWrite 068a,f8,0,7
SPIWrite 068b,b5,0,7
SPIWrite 068c,75,0,7
SPIWrite 068d,4c,0,7
SPIWrite 068e,84,0,7
SPIWrite 068f,46,0,7
SPIWrite 0690,e0,0,7
SPIWrite 0691,79,0,7
SPIWrite 0692,64,0,7
SPIWrite 0693,79,0,7
```

```
SPIWrite 0694,24,0,7
SPIWrite 0695,18,0,7
SPIWrite 0696,02,0,7
SPIWrite 0697,2c,0,7
SPIWrite 0698,3a,0,7
SPIWrite 0699,d1,0,7
SPIWrite 069a,57,0,7
SPIWrite 069b,78,0,7
SPIWrite 069c,37,0,7
SPIWrite 069d,f0,0,7
SPIWrite 069e,02,0,7
SPIWrite 069f,07,0,7
SPIWrite 06a0,36,0,7
SPIWrite 06a1,d1,0,7
SPIWrite 06a2,73,0,7
SPIWrite 06a3,4c,0,7
SPIWrite 06a4,71,0,7
SPIWrite 06a5,4a,0,7
SPIWrite 06a6,03,0,7
SPIWrite 06a7,27,0,7
SPIWrite 06a8,0c,0,7
SPIWrite 06a9,20,0,7
SPIWrite 06aa,1c,0,7
SPIWrite 06ab,fb,0,7
SPIWrite 06ac,07,0,7
SPIWrite 06ad,15,0,7
SPIWrite 06ae,1c,0,7
SPIWrite 06af,fb,0,7
SPIWrite 06b0,00,0,7
SPIWrite 06b1,f0,0,7
SPIWrite 06b2,00,0,7
SPIWrite 06b3,eb,0,7
SPIWrite 06b4,81,0,7
SPIWrite 06b5,00,0,7
SPIWrite 06b6,67,0,7
SPIWrite 06b7,5d,0,7
SPIWrite 06b8,12,0,7
SPIWrite 06b9,58,0,7
SPIWrite 06ba,6b,0,7
SPIWrite 06bb,48,0,7
SPIWrite 06bc,92,0,7
SPIWrite 06bd,f9,0,7
SPIWrite 06be,90,0,7
SPIWrite 06bf,54,0,7
SPIWrite 06c0,dc,0,7
SPIWrite 06c1,26,0,7
SPIWrite 06c2,4f,0,7
SPIWrite 06c3,f4,0,7
SPIWrite 06c4,25,0,7
SPIWrite 06c5,7e,0,7
SPIWrite 06c6,11,0,7
SPIWrite 06c7,fb,0,7
```

```
SPIWrite 06c8,06,0,7
SPIWrite 06c9,f6,0,7
SPIWrite 06ca,1c,0,7
SPIWrite 06cb,fb,0,7
SPIWrite 06cc,0e,0,7
SPIWrite 06cd,66,0,7
SPIWrite 06ce,94,0,7
SPIWrite 06cf,46,0,7
SPIWrite 06d0,80,0,7
SPIWrite 06d1,19,0,7
SPIWrite 06d2,90,0,7
SPIWrite 06d3,f9,0,7
SPIWrite 06d4,89,0,7
SPIWrite 06d5,10,0,7
SPIWrite 06d6,90,0,7
SPIWrite 06d7,f9,0,7
SPIWrite 06d8,87,0,7
SPIWrite 06d9,40,0,7
SPIWrite 06da,90,0,7
SPIWrite 06db,f9,0,7
SPIWrite 06dc,86,0,7
SPIWrite 06dd,20,0,7
SPIWrite 06de,9c,0,7
SPIWrite 06df,f9,0,7
SPIWrite 06e0,91,0,7
SPIWrite 06e1,64,0,7
SPIWrite 06e2,90,0,7
SPIWrite 06e3,f9,0,7
SPIWrite 06e4,88,0,7
SPIWrite 06e5,00,0,7
SPIWrite 06e6,4f,0,7
SPIWrite 06e7,b9,0,7
SPIWrite 06e8,86,0,7
SPIWrite 06e9,42,0,7
SPIWrite 06ea,0e,0,7
SPIWrite 06eb,bf,0,7
SPIWrite 06ec,a5,0,7
SPIWrite 06ed,42,0,7
SPIWrite 06ee,01,0,7
SPIWrite 06ef,21,0,7
SPIWrite 06f0,19,0,7
SPIWrite 06f1,70,0,7
SPIWrite 06f2,8c,0,7
SPIWrite 06f3,f8,0,7
SPIWrite 06f4,90,0,7
SPIWrite 06f5,44,0,7
SPIWrite 06f6,8c,0,7
SPIWrite 06f7,f8,0,7
SPIWrite 06f8,91,0,7
SPIWrite 06f9,04,0,7
SPIWrite 06fa,f8,0,7
SPIWrite 06fb,bd,0,7
```

```
SPIWrite 06fc,95,0,7
SPIWrite 06fd,42,0,7
SPIWrite 06fe,0e,0,7
SPIWrite 06ff,bf,0,7
SPIWrite 0700,8e,0,7
SPIWrite 0701,42,0,7
SPIWrite 0702,01,0,7
SPIWrite 0703,20,0,7
SPIWrite 0704,18,0,7
SPIWrite 0705,70,0,7
SPIWrite 0706,8c,0,7
SPIWrite 0707,f8,0,7
SPIWrite 0708,91,0,7
SPIWrite 0709,14,0,7
SPIWrite 070a,8c,0,7
SPIWrite 070b,f8,0,7
SPIWrite 070c,90,0,7
SPIWrite 070d,24,0,7
SPIWrite 070e,f8,0,7
SPIWrite 070f,bd,0,7
SPIWrite 0710,60,0,7
SPIWrite 0711,46,0,7
SPIWrite 0712,ec,0,7
SPIWrite 0713,f7,0,7
SPIWrite 0714,31,0,7
SPIWrite 0715,f8,0,7
SPIWrite 0716,f8,0,7
SPIWrite 0717,bd,0,7
SPIWrite 0718,2d,0,7
SPIWrite 0719,e9,0,7
SPIWrite 071a,fe,0,7
SPIWrite 071b,4f,0,7
SPIWrite 071c,0c,0,7
SPIWrite 071d,9e,0,7
SPIWrite 071e,82,0,7
SPIWrite 071f,46,0,7
SPIWrite 0720,89,0,7
SPIWrite 0721,46,0,7
SPIWrite 0722,14,0,7
SPIWrite 0723,46,0,7
SPIWrite 0724,0d,0,7
SPIWrite 0725,9f,0,7
SPIWrite 0726,00,0,7
SPIWrite 0727,96,0,7
SPIWrite 0728,1d,0,7
SPIWrite 0729,46,0,7
SPIWrite 072a,01,0,7
SPIWrite 072b,97,0,7
SPIWrite 072c,ec,0,7
SPIWrite 072d,f7,0,7
SPIWrite 072e,52,0,7
SPIWrite 072f,f9,0,7
```

```
SPIWrite 0730,df,0,7
SPIWrite 0731,f8,0,7
SPIWrite 0732,3c,0,7
SPIWrite 0733,b1,0,7
SPIWrite 0734,20,0,7
SPIWrite 0735,88,0,7
SPIWrite 0736,20,0,7
SPIWrite 0737,b9,0,7
SPIWrite 0738,60,0,7
SPIWrite 0739,88,0,7
SPIWrite 073a,00,0,7
SPIWrite 073b,28,0,7
SPIWrite 073c,4f,0,7
SPIWrite 073d,d0,0,7
SPIWrite 073e,01,0,7
SPIWrite 073f,20,0,7
SPIWrite 0740,4e,0,7
SPIWrite 0741,e0,0,7
SPIWrite 0742,63,0,7
SPIWrite 0743,88,0,7
SPIWrite 0744,00,0,7
SPIWrite 0745,2b,0,7
SPIWrite 0746,4a,0,7
SPIWrite 0747,d0,0,7
SPIWrite 0748,ea,0,7
SPIWrite 0749,f7,0,7
SPIWrite 074a,7f,0,7
SPIWrite 074b,f9,0,7
SPIWrite 074c,80,0,7
SPIWrite 074d,46,0,7
SPIWrite 074e,60,0,7
SPIWrite 074f,88,0,7
SPIWrite 0750,ea,0,7
SPIWrite 0751,f7,0,7
SPIWrite 0752,7b,0,7
SPIWrite 0753,f9,0,7
SPIWrite 0754,69,0,7
SPIWrite 0755,79,0,7
SPIWrite 0756,00,0,7
SPIWrite 0757,eb,0,7
SPIWrite 0758,80,0,7
SPIWrite 0759,00,0,7
SPIWrite 075a,08,0,7
SPIWrite 075b,eb,0,7
SPIWrite 075c,88,0,7
SPIWrite 075d,02,0,7
SPIWrite 075e,c0,0,7
SPIWrite 075f,13,0,7
SPIWrite 0760,d2,0,7
SPIWrite 0761,13,0,7
SPIWrite 0762,01,0,7
SPIWrite 0763,29,0,7
```

```
SPIWrite 0764,44,0,7
SPIWrite 0765,b2,0,7
SPIWrite 0766,53,0,7
SPIWrite 0767,b2,0,7
SPIWrite 0768,3f,0,7
SPIWrite 0769,d1,0,7
SPIWrite 076a,3f,0,7
SPIWrite 076b,48,0,7
SPIWrite 076c,dc,0,7
SPIWrite 076d,21,0,7
SPIWrite 076e,4f,0,7
SPIWrite 076f,f4,0,7
SPIWrite 0770,25,0,7
SPIWrite 0771,72,0,7
SPIWrite 0772,19,0,7
SPIWrite 0773,fb,0,7
SPIWrite 0774,01,0,7
SPIWrite 0775,f1,0,7
SPIWrite 0776,1a,0,7
SPIWrite 0777,fb,0,7
SPIWrite 0778,02,0,7
SPIWrite 0779,11,0,7
SPIWrite 077a,b2,0,7
SPIWrite 077b,78,0,7
SPIWrite 077c,40,0,7
SPIWrite 077d,18,0,7
SPIWrite 077e,71,0,7
SPIWrite 077f,78,0,7
SPIWrite 0780,b0,0,7
SPIWrite 0781,f9,0,7
SPIWrite 0782,5a,0,7
SPIWrite 0783,c0,0,7
SPIWrite 0784,b0,0,7
SPIWrite 0785,f9,0,7
SPIWrite 0786,5c,0,7
SPIWrite 0787,60,0,7
SPIWrite 0788,c2,0,7
SPIWrite 0789,f1,0,7
SPIWrite 078a,01,0,7
SPIWrite 078b,02,0,7
SPIWrite 078c,c1,0,7
SPIWrite 078d,f1,0,7
SPIWrite 078e,01,0,7
SPIWrite 078f,01,0,7
SPIWrite 0790,11,0,7
SPIWrite 0791,fb,0,7
SPIWrite 0792,0c,0,7
SPIWrite 0793,f0,0,7
SPIWrite 0794,c0,0,7
SPIWrite 0795,eb,0,7
SPIWrite 0796,43,0,7
SPIWrite 0797,10,0,7
```

```
SPIWrite 0798,12,0,7
SPIWrite 0799,fb,0,7
SPIWrite 079a,06,0,7
SPIWrite 079b,f1,0,7
SPIWrite 079c,40,0,7
SPIWrite 079d,11,0,7
SPIWrite 079e,c1,0,7
SPIWrite 079f,eb,0,7
SPIWrite 07a0,44,0,7
SPIWrite 07a1,11,0,7
SPIWrite 07a2,a0,0,7
SPIWrite 07a3,eb,0,7
SPIWrite 07a4,61,0,7
SPIWrite 07a5,10,0,7
SPIWrite 07a6,41,0,7
SPIWrite 07a7,b2,0,7
SPIWrite 07a8,08,0,7
SPIWrite 07a9,46,0,7
SPIWrite 07aa,00,0,7
SPIWrite 07ab,28,0,7
SPIWrite 07ac,b8,0,7
SPIWrite 07ad,bf,0,7
SPIWrite 07ae,40,0,7
SPIWrite 07af,42,0,7
SPIWrite 07b0,c2,0,7
SPIWrite 07b1,b2,0,7
SPIWrite 07b2,00,0,7
SPIWrite 07b3,29,0,7
SPIWrite 07b4,4f,0,7
SPIWrite 07b5,f0,0,7
SPIWrite 07b6,00,0,7
SPIWrite 07b7,00,0,7
SPIWrite 07b8,d8,0,7
SPIWrite 07b9,bf,0,7
SPIWrite 07ba,01,0,7
SPIWrite 07bb,20,0,7
SPIWrite 07bc,a9,0,7
SPIWrite 07bd,79,0,7
SPIWrite 07be,91,0,7
SPIWrite 07bf,42,0,7
SPIWrite 07c0,0e,0,7
SPIWrite 07c1,da,0,7
SPIWrite 07c2,2b,0,7
SPIWrite 07c3,78,0,7
SPIWrite 07c4,c9,0,7
SPIWrite 07c5,18,0,7
SPIWrite 07c6,91,0,7
SPIWrite 07c7,42,0,7
SPIWrite 07c8,0a,0,7
SPIWrite 07c9,db,0,7
SPIWrite 07ca,03,0,7
SPIWrite 07cb,22,0,7
```

```
SPIWrite 07cc,59,0,7
SPIWrite 07cd,46,0,7
SPIWrite 07ce,1a,0,7
SPIWrite 07cf,fb,0,7
SPIWrite 07d0,02,0,7
SPIWrite 07d1,92,0,7
SPIWrite 07d2,89,0,7
SPIWrite 07d3,5c,0,7
SPIWrite 07d4,81,0,7
SPIWrite 07d5,42,0,7
SPIWrite 07d6,1c,0,7
SPIWrite 07d7,bf,0,7
SPIWrite 07d8,01,0,7
SPIWrite 07d9,21,0,7
SPIWrite 07da,79,0,7
SPIWrite 07db,70,0,7
SPIWrite 07dc,00,0,7
SPIWrite 07dd,e0,0,7
SPIWrite 07de,00,0,7
SPIWrite 07df,20,0,7
SPIWrite 07e0,03,0,7
SPIWrite 07e1,22,0,7
SPIWrite 07e2,59,0,7
SPIWrite 07e3,46,0,7
SPIWrite 07e4,1a,0,7
SPIWrite 07e5,fb,0,7
SPIWrite 07e6,02,0,7
SPIWrite 07e7,92,0,7
SPIWrite 07e8,88,0,7
SPIWrite 07e9,54,0,7
SPIWrite 07ea,bd,0,7
SPIWrite 07eb,e8,0,7
SPIWrite 07ec,fe,0,7
SPIWrite 07ed,8f,0,7
SPIWrite 07ee,2d,0,7
SPIWrite 07ef,e9,0,7
SPIWrite 07f0,fe,0,7
SPIWrite 07f1,43,0,7
SPIWrite 07f2,21,0,7
SPIWrite 07f3,48,0,7
SPIWrite 07f4,1f,0,7
SPIWrite 07f5,49,0,7
SPIWrite 07f6,08,0,7
SPIWrite 07f7,60,0,7
SPIWrite 07f8,ec,0,7
SPIWrite 07f9,f7,0,7
SPIWrite 07fa,88,0,7
SPIWrite 07fb,fa,0,7
SPIWrite 07fc,00,0,7
SPIWrite 07fd,24,0,7
SPIWrite 07fe,1f,0,7
SPIWrite 07ff,4d,0,7
```

```
SPIWrite 0800,df,0,7
SPIWrite 0801,f8,0,7
SPIWrite 0802,80,0,7
SPIWrite 0803,80,0,7
SPIWrite 0804,20,0,7
SPIWrite 0805,4f,0,7
SPIWrite 0806,df,0,7
SPIWrite 0807,f8,0,7
SPIWrite 0808,78,0,7
SPIWrite 0809,90,0,7
SPIWrite 080a,18,0,7
SPIWrite 080b,4e,0,7
SPIWrite 080c,8d,0,7
SPIWrite 080d,f8,0,7
SPIWrite 080e,04,0,7
SPIWrite 080f,40,0,7
SPIWrite 0810,6d,0,7
SPIWrite 0811,1e,0,7
SPIWrite 0812,15,0,7
SPIWrite 0813,f8,0,7
SPIWrite 0814,01,0,7
SPIWrite 0815,0f,0,7
SPIWrite 0816,01,0,7
SPIWrite 0817,28,0,7
SPIWrite 0818,1f,0,7
SPIWrite 0819,d1,0,7
SPIWrite 081a,19,0,7
SPIWrite 081b,f8,0,7
SPIWrite 081c,04,0,7
SPIWrite 081d,00,0,7
SPIWrite 081e,e0,0,7
SPIWrite 081f,b9,0,7
SPIWrite 0018,00,0,7  //Property_18h_0_0=0x0;
     Address(0x18[7:0])
SPIWrite 0018,20,0,7  //macro=0x1;    Address(0x18[7:5])
SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,08,0,7  //MACRO_OPERAND_REG0=0x8000000;
     Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00,0,7
SPIWrite 00a1,00,0,7
SPIWrite 00a0,00,0,7
SPIWrite 00a7,00,0,7  //MACRO_OPERAND_REG1=0x1000;
     Address(0xa4[7:0],0xa5[7:0],0xa6[7:0],0xa7[7:0],0xa8[7:0])
SPIWrite 00a6,00,0,7
SPIWrite 00a5,10,0,7
SPIWrite 00a4,00,0,7
```

```
SPIWrite 0193,78,0,7  //MACRO_OPCODE=0x78;
     Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
     Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
     Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
     Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
     Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIWrite 0144,00,0,7  //Property_124h_4_2=0x0;
```

```
      Address(0x144[7:2])
SPIWrite 0018,00,0,7  //macro=0x0;     Address(0x18[7:5])
SPIWrite 0018,01,0,7  //Property_18h_0_0=0x1;
      Address(0x18[7:0])
SPIWrite 0020,18,0,7
SPIWrite 0021,f8,0,7
SPIWrite 0022,14,0,7
SPIWrite 0023,10,0,7
SPIWrite 0024,60,0,7
SPIWrite 0025,00,0,7
SPIWrite 0026,00,0,7
SPIWrite 0027,eb,0,7
SPIWrite 0028,84,0,7
SPIWrite 0029,00,0,7
SPIWrite 002a,3b,0,7
SPIWrite 002b,18,0,7
SPIWrite 002c,9a,0,7
SPIWrite 002d,78,0,7
SPIWrite 002e,60,0,7
SPIWrite 002f,10,0,7
SPIWrite 0030,01,0,7
SPIWrite 0031,2a,0,7
SPIWrite 0032,0c,0,7
SPIWrite 0033,d0,0,7
SPIWrite 0034,82,0,7
SPIWrite 0035,00,0,7
SPIWrite 0036,02,0,7
SPIWrite 0037,eb,0,7
SPIWrite 0038,c0,0,7
SPIWrite 0039,02,0,7
SPIWrite 003a,02,0,7
SPIWrite 003b,eb,0,7
SPIWrite 003c,81,0,7
SPIWrite 003d,02,0,7
SPIWrite 003e,b1,0,7
SPIWrite 003f,58,0,7
SPIWrite 0040,d1,0,7
SPIWrite 0041,f8,0,7
SPIWrite 0042,00,0,7
SPIWrite 0043,04,0,7
SPIWrite 0044,20,0,7
SPIWrite 0045,f4,0,7
SPIWrite 0046,80,0,7
SPIWrite 0047,70,0,7
SPIWrite 0048,c1,0,7
SPIWrite 0049,f8,0,7
SPIWrite 004a,00,0,7
SPIWrite 004b,04,0,7
SPIWrite 004c,05,0,7
SPIWrite 004d,e0,0,7
SPIWrite 004e,01,0,7
SPIWrite 004f,aa,0,7
```

```
SPIWrite 0050,00,0,7
SPIWrite 0051,92,0,7
SPIWrite 0052,da,0,7
SPIWrite 0053,78,0,7
SPIWrite 0054,1b,0,7
SPIWrite 0055,1d,0,7
SPIWrite 0056,eb,0,7
SPIWrite 0057,f7,0,7
SPIWrite 0058,45,0,7
SPIWrite 0059,ff,0,7
SPIWrite 005a,64,0,7
SPIWrite 005b,1c,0,7
SPIWrite 005c,04,0,7
SPIWrite 005d,2c,0,7
SPIWrite 005e,d8,0,7
SPIWrite 005f,db,0,7
SPIWrite 0060,bd,0,7
SPIWrite 0061,e8,0,7
SPIWrite 0062,fe,0,7
SPIWrite 0063,83,0,7
SPIWrite 0064,e6,0,7
SPIWrite 0065,1d,0,7
SPIWrite 0066,01,0,7
SPIWrite 0067,20,0,7
SPIWrite 0068,e0,0,7
SPIWrite 0069,ab,0,7
SPIWrite 006a,00,0,7
SPIWrite 006b,20,0,7
SPIWrite 006c,a8,0,7
SPIWrite 006d,75,0,7
SPIWrite 006e,02,0,7
SPIWrite 006f,00,0,7
SPIWrite 0070,dc,0,7
SPIWrite 0071,22,0,7
SPIWrite 0072,01,0,7
SPIWrite 0073,20,0,7
SPIWrite 0074,cc,0,7
SPIWrite 0075,d7,0,7
SPIWrite 0076,00,0,7
SPIWrite 0077,20,0,7
SPIWrite 0078,69,0,7
SPIWrite 0079,16,0,7
SPIWrite 007a,03,0,7
SPIWrite 007b,00,0,7
SPIWrite 007c,f0,0,7
SPIWrite 007d,1e,0,7
SPIWrite 007e,01,0,7
SPIWrite 007f,20,0,7
SPIWrite 0080,f4,0,7
SPIWrite 0081,1e,0,7
SPIWrite 0082,01,0,7
SPIWrite 0083,20,0,7
```

```
SPIWrite 0084,06,0,7
SPIWrite 0085,d6,0,7
SPIWrite 0086,00,0,7
SPIWrite 0087,20,0,7
SPIWrite 0088,6c,0,7
SPIWrite 0089,1a,0,7
SPIWrite 008a,01,0,7
SPIWrite 008b,20,0,7
SPIWrite 008c,3a,0,7
SPIWrite 008d,b1,0,7
SPIWrite 008e,03,0,7
SPIWrite 008f,46,0,7
SPIWrite 0090,10,0,7
SPIWrite 0091,46,0,7
SPIWrite 0092,13,0,7
SPIWrite 0093,f8,0,7
SPIWrite 0094,01,0,7
SPIWrite 0095,2b,0,7
SPIWrite 0096,40,0,7
SPIWrite 0097,1e,0,7
SPIWrite 0098,01,0,7
SPIWrite 0099,f8,0,7
SPIWrite 009a,01,0,7
SPIWrite 009b,2b,0,7
SPIWrite 009c,f9,0,7
SPIWrite 009d,d1,0,7
SPIWrite 009e,70,0,7
SPIWrite 009f,47,0,7
SPIWrite 00a0,38,0,7
SPIWrite 00a1,b5,0,7
SPIWrite 00a2,05,0,7
SPIWrite 00a3,46,0,7
SPIWrite 00a4,0c,0,7
SPIWrite 00a5,46,0,7
SPIWrite 00a6,28,0,7
SPIWrite 00a7,68,0,7
SPIWrite 00a8,21,0,7
SPIWrite 00a9,68,0,7
SPIWrite 00aa,0c,0,7
SPIWrite 00ab,22,0,7
SPIWrite 00ac,ff,0,7
SPIWrite 00ad,f7,0,7
SPIWrite 00ae,ee,0,7
SPIWrite 00af,ff,0,7
SPIWrite 00b0,68,0,7
SPIWrite 00b1,68,0,7
SPIWrite 00b2,61,0,7
SPIWrite 00b3,68,0,7
SPIWrite 00b4,05,0,7
SPIWrite 00b5,22,0,7
SPIWrite 00b6,ff,0,7
SPIWrite 00b7,f7,0,7
```

```
SPIWrite 00b8,e9,0,7
SPIWrite 00b9,ff,0,7
SPIWrite 00ba,a8,0,7
SPIWrite 00bb,68,0,7
SPIWrite 00bc,a1,0,7
SPIWrite 00bd,68,0,7
SPIWrite 00be,18,0,7
SPIWrite 00bf,22,0,7
SPIWrite 00c0,ff,0,7
SPIWrite 00c1,f7,0,7
SPIWrite 00c2,e4,0,7
SPIWrite 00c3,ff,0,7
SPIWrite 00c4,e8,0,7
SPIWrite 00c5,68,0,7
SPIWrite 00c6,e1,0,7
SPIWrite 00c7,68,0,7
SPIWrite 00c8,d2,0,7
SPIWrite 00c9,22,0,7
SPIWrite 00ca,ff,0,7
SPIWrite 00cb,f7,0,7
SPIWrite 00cc,df,0,7
SPIWrite 00cd,ff,0,7
SPIWrite 00ce,28,0,7
SPIWrite 00cf,69,0,7
SPIWrite 00d0,21,0,7
SPIWrite 00d1,69,0,7
SPIWrite 00d2,96,0,7
SPIWrite 00d3,22,0,7
SPIWrite 00d4,ff,0,7
SPIWrite 00d5,f7,0,7
SPIWrite 00d6,da,0,7
SPIWrite 00d7,ff,0,7
SPIWrite 00d8,38,0,7
SPIWrite 00d9,bd,0,7
SPIWrite 00da,b0,0,7
SPIWrite 00db,b5,0,7
SPIWrite 00dc,39,0,7
SPIWrite 00dd,49,0,7
SPIWrite 00de,3a,0,7
SPIWrite 00df,4d,0,7
SPIWrite 00e0,00,0,7
SPIWrite 00e1,f0,0,7
SPIWrite 00e2,01,0,7
SPIWrite 00e3,02,0,7
SPIWrite 00e4,04,0,7
SPIWrite 00e5,27,0,7
SPIWrite 00e6,12,0,7
SPIWrite 00e7,04,0,7
SPIWrite 00e8,08,0,7
SPIWrite 00e9,70,0,7
SPIWrite 00ea,55,0,7
SPIWrite 00eb,f8,0,7
```

```
SPIWrite 00ec,04,0,7
SPIWrite 00ed,4b,0,7
SPIWrite 00ee,d4,0,7
SPIWrite 00ef,f8,0,7
SPIWrite 00f0,80,0,7
SPIWrite 00f1,1b,0,7
SPIWrite 00f2,21,0,7
SPIWrite 00f3,f4,0,7
SPIWrite 00f4,80,0,7
SPIWrite 00f5,31,0,7
SPIWrite 00f6,11,0,7
SPIWrite 00f7,43,0,7
SPIWrite 00f8,c4,0,7
SPIWrite 00f9,f8,0,7
SPIWrite 00fa,80,0,7
SPIWrite 00fb,1b,0,7
SPIWrite 00fc,d4,0,7
SPIWrite 00fd,f8,0,7
SPIWrite 00fe,48,0,7
SPIWrite 00ff,3b,0,7
SPIWrite 0100,7f,0,7
SPIWrite 0101,1e,0,7
SPIWrite 0102,80,0,7
SPIWrite 0103,ea,0,7
SPIWrite 0104,03,0,7
SPIWrite 0105,01,0,7
SPIWrite 0106,01,0,7
SPIWrite 0107,f0,0,7
SPIWrite 0108,01,0,7
SPIWrite 0109,01,0,7
SPIWrite 010a,81,0,7
SPIWrite 010b,ea,0,7
SPIWrite 010c,03,0,7
SPIWrite 010d,01,0,7
SPIWrite 010e,c4,0,7
SPIWrite 010f,f8,0,7
SPIWrite 0110,48,0,7
SPIWrite 0111,1b,0,7
SPIWrite 0112,ea,0,7
SPIWrite 0113,d1,0,7
SPIWrite 0114,01,0,7
SPIWrite 0115,28,0,7
SPIWrite 0116,0c,0,7
SPIWrite 0117,bf,0,7
SPIWrite 0118,2c,0,7
SPIWrite 0119,48,0,7
SPIWrite 011a,2d,0,7
SPIWrite 011b,48,0,7
SPIWrite 011c,2d,0,7
SPIWrite 011d,49,0,7
SPIWrite 011e,ff,0,7
SPIWrite 011f,f7,0,7
```

```
SPIWrite 0120,bf,0,7
SPIWrite 0121,ff,0,7
SPIWrite 0122,b0,0,7
SPIWrite 0123,bd,0,7
SPIWrite 0124,8c,0,7
SPIWrite 0125,46,0,7
SPIWrite 0126,2c,0,7
SPIWrite 0127,49,0,7
SPIWrite 0128,f8,0,7
SPIWrite 0129,b5,0,7
SPIWrite 012a,09,0,7
SPIWrite 012b,5c,0,7
SPIWrite 012c,01,0,7
SPIWrite 012d,29,0,7
SPIWrite 012e,12,0,7
SPIWrite 012f,d1,0,7
SPIWrite 0130,2a,0,7
SPIWrite 0131,49,0,7
SPIWrite 0132,46,0,7
SPIWrite 0133,01,0,7
SPIWrite 0134,02,0,7
SPIWrite 0135,23,0,7
SPIWrite 0136,00,0,7
SPIWrite 0137,24,0,7
SPIWrite 0138,32,0,7
SPIWrite 0139,19,0,7
SPIWrite 013a,02,0,7
SPIWrite 013b,27,0,7
SPIWrite 013c,8a,0,7
SPIWrite 013d,18,0,7
SPIWrite 013e,b2,0,7
SPIWrite 013f,f9,0,7
SPIWrite 0140,00,0,7
SPIWrite 0141,50,0,7
SPIWrite 0142,7f,0,7
SPIWrite 0143,1e,0,7
SPIWrite 0144,4f,0,7
SPIWrite 0145,ea,0,7
SPIWrite 0146,45,0,7
SPIWrite 0147,05,0,7
SPIWrite 0148,22,0,7
SPIWrite 0149,f8,0,7
SPIWrite 014a,10,0,7
SPIWrite 014b,5b,0,7
SPIWrite 014c,f7,0,7
SPIWrite 014d,d1,0,7
SPIWrite 014e,5b,0,7
SPIWrite 014f,1e,0,7
SPIWrite 0150,04,0,7
SPIWrite 0151,f1,0,7
SPIWrite 0152,08,0,7
SPIWrite 0153,04,0,7
```

```
SPIWrite 0154,f0,0,7
SPIWrite 0155,d1,0,7
SPIWrite 0156,61,0,7
SPIWrite 0157,46,0,7
SPIWrite 0158,e1,0,7
SPIWrite 0159,f7,0,7
SPIWrite 015a,e6,0,7
SPIWrite 015b,f9,0,7
SPIWrite 015c,f8,0,7
SPIWrite 015d,bd,0,7
SPIWrite 015e,98,0,7
SPIWrite 015f,b5,0,7
SPIWrite 0160,1f,0,7
SPIWrite 0161,4c,0,7
SPIWrite 0162,00,0,7
SPIWrite 0163,21,0,7
SPIWrite 0164,84,0,7
SPIWrite 0165,f8,0,7
SPIWrite 0166,24,0,7
SPIWrite 0167,10,0,7
SPIWrite 0168,1f,0,7
SPIWrite 0169,48,0,7
SPIWrite 016a,84,0,7
SPIWrite 016b,f8,0,7
SPIWrite 016c,25,0,7
SPIWrite 016d,10,0,7
SPIWrite 016e,03,0,7
SPIWrite 016f,22,0,7
SPIWrite 0170,84,0,7
SPIWrite 0171,f8,0,7
SPIWrite 0172,29,0,7
SPIWrite 0173,10,0,7
SPIWrite 0174,1b,0,7
SPIWrite 0175,4b,0,7
SPIWrite 0176,84,0,7
SPIWrite 0177,f8,0,7
SPIWrite 0178,2a,0,7
SPIWrite 0179,10,0,7
SPIWrite 017a,0a,0,7
SPIWrite 017b,21,0,7
SPIWrite 017c,40,0,7
SPIWrite 017d,1e,0,7
SPIWrite 017e,10,0,7
SPIWrite 017f,f8,0,7
SPIWrite 0180,01,0,7
SPIWrite 0181,4f,0,7
SPIWrite 0182,05,0,7
SPIWrite 0183,27,0,7
SPIWrite 0184,7f,0,7
SPIWrite 0185,1e,0,7
SPIWrite 0186,03,0,7
SPIWrite 0187,f8,0,7
```

```
SPIWrite 0188,01,0,7
SPIWrite 0189,4b,0,7
SPIWrite 018a,fb,0,7
SPIWrite 018b,d1,0,7
SPIWrite 018c,49,0,7
SPIWrite 018d,1e,0,7
SPIWrite 018e,f6,0,7
SPIWrite 018f,d1,0,7
SPIWrite 0190,52,0,7
SPIWrite 0191,1e,0,7
SPIWrite 0192,00,0,7
SPIWrite 0193,f1,0,7
SPIWrite 0194,01,0,7
SPIWrite 0195,00,0,7
SPIWrite 0196,f0,0,7
SPIWrite 0197,d1,0,7
SPIWrite 0198,98,0,7
SPIWrite 0199,bd,0,7
SPIWrite 019a,0a,0,7
SPIWrite 019b,4a,0,7
SPIWrite 019c,80,0,7
SPIWrite 019d,b5,0,7
SPIWrite 019e,12,0,7
SPIWrite 019f,78,0,7
SPIWrite 01a0,01,0,7
SPIWrite 01a1,2a,0,7
SPIWrite 01a2,0c,0,7
SPIWrite 01a3,d1,0,7
SPIWrite 01a4,11,0,7
SPIWrite 01a5,4b,0,7
SPIWrite 01a6,42,0,7
SPIWrite 01a7,10,0,7
SPIWrite 01a8,9a,0,7
SPIWrite 01a9,5c,0,7
SPIWrite 01aa,92,0,7
SPIWrite 01ab,1e,0,7
SPIWrite 01ac,d7,0,7
SPIWrite 01ad,b2,0,7
SPIWrite 01ae,1f,0,7
SPIWrite 01af,b1,0,7
SPIWrite 01b0,01,0,7
SPIWrite 01b1,2f,0,7
SPIWrite 01b2,04,0,7
SPIWrite 01b3,d1,0,7
SPIWrite 01b4,05,0,7
SPIWrite 01b5,22,0,7
SPIWrite 01b6,00,0,7
SPIWrite 01b7,e0,0,7
SPIWrite 01b8,07,0,7
SPIWrite 01b9,22,0,7
SPIWrite 01ba,0d,0,7
SPIWrite 01bb,4b,0,7
```

```
SPIWrite 01bc,1a,0,7
SPIWrite 01bd,70,0,7
SPIWrite 01be,d7,0,7
SPIWrite 01bf,f7,0,7
SPIWrite 01c0,b1,0,7
SPIWrite 01c1,ff,0,7
SPIWrite 01c2,80,0,7
SPIWrite 01c3,bd,0,7
SPIWrite 01c4,f6,0,7
SPIWrite 01c5,22,0,7
SPIWrite 01c6,01,0,7
SPIWrite 01c7,20,0,7
SPIWrite 01c8,bc,0,7
SPIWrite 01c9,77,0,7
SPIWrite 01ca,02,0,7
SPIWrite 01cb,00,0,7
SPIWrite 01cc,60,0,7
SPIWrite 01cd,21,0,7
SPIWrite 01ce,03,0,7
SPIWrite 01cf,00,0,7
SPIWrite 01d0,74,0,7
SPIWrite 01d1,21,0,7
SPIWrite 01d2,03,0,7
SPIWrite 01d3,00,0,7
SPIWrite 01d4,4c,0,7
SPIWrite 01d5,21,0,7
SPIWrite 01d6,03,0,7
SPIWrite 01d7,00,0,7
SPIWrite 01d8,ac,0,7
SPIWrite 01d9,fe,0,7
SPIWrite 01da,00,0,7
SPIWrite 01db,20,0,7
SPIWrite 01dc,28,0,7
SPIWrite 01dd,fd,0,7
SPIWrite 01de,00,0,7
SPIWrite 01df,20,0,7
SPIWrite 01e0,4a,0,7
SPIWrite 01e1,0c,0,7
SPIWrite 01e2,01,0,7
SPIWrite 01e3,20,0,7
SPIWrite 01e4,fb,0,7
SPIWrite 01e5,20,0,7
SPIWrite 01e6,01,0,7
SPIWrite 01e7,20,0,7
SPIWrite 01e8,2b,0,7
SPIWrite 01e9,21,0,7
SPIWrite 01ea,03,0,7
SPIWrite 01eb,00,0,7
SPIWrite 01ec,a2,0,7
SPIWrite 01ed,01,0,7
SPIWrite 01ee,01,0,7
SPIWrite 01ef,20,0,7
```

```
SPIWrite 01f0,d4,0,7
SPIWrite 01f1,1e,0,7
SPIWrite 01f2,01,0,7
SPIWrite 01f3,20,0,7
SPIWrite 01f4,2d,0,7
SPIWrite 01f5,e9,0,7
SPIWrite 01f6,f0,0,7
SPIWrite 01f7,41,0,7
SPIWrite 01f8,04,0,7
SPIWrite 01f9,46,0,7
SPIWrite 01fa,4a,0,7
SPIWrite 01fb,48,0,7
SPIWrite 01fc,0d,0,7
SPIWrite 01fd,46,0,7
SPIWrite 01fe,a7,0,7
SPIWrite 01ff,00,0,7
SPIWrite 0200,c1,0,7
SPIWrite 0201,5d,0,7
SPIWrite 0202,1e,0,7
SPIWrite 0203,46,0,7
SPIWrite 0204,8d,0,7
SPIWrite 0205,42,0,7
SPIWrite 0206,07,0,7
SPIWrite 0207,44,0,7
SPIWrite 0208,08,0,7
SPIWrite 0209,d0,0,7
SPIWrite 020a,b9,0,7
SPIWrite 020b,78,0,7
SPIWrite 020c,8d,0,7
SPIWrite 020d,42,0,7
SPIWrite 020e,18,0,7
SPIWrite 020f,bf,0,7
SPIWrite 0210,04,0,7
SPIWrite 0211,27,0,7
SPIWrite 0212,13,0,7
SPIWrite 0213,d1,0,7
SPIWrite 0214,01,0,7
SPIWrite 0215,21,0,7
SPIWrite 0216,01,0,7
SPIWrite 0217,eb,0,7
SPIWrite 0218,44,0,7
SPIWrite 0219,01,0,7
SPIWrite 021a,00,0,7
SPIWrite 021b,e0,0,7
SPIWrite 021c,61,0,7
SPIWrite 021d,00,0,7
SPIWrite 021e,cf,0,7
SPIWrite 021f,b2,0,7
SPIWrite 0220,04,0,7
SPIWrite 0221,2f,0,7
SPIWrite 0222,0b,0,7
SPIWrite 0223,d0,0,7
```

```
SPIWrite 0224,40,0,7
SPIWrite 0225,49,0,7
SPIWrite 0226,00,0,7
SPIWrite 0227,eb,0,7
SPIWrite 0228,47,0,7
SPIWrite 0229,00,0,7
SPIWrite 022a,0a,0,7
SPIWrite 022b,5d,0,7
SPIWrite 022c,41,0,7
SPIWrite 022d,78,0,7
SPIWrite 022e,90,0,7
SPIWrite 022f,46,0,7
SPIWrite 0230,04,0,7
SPIWrite 0231,29,0,7
SPIWrite 0232,04,0,7
SPIWrite 0233,d0,0,7
SPIWrite 0234,20,0,7
SPIWrite 0235,46,0,7
SPIWrite 0236,dd,0,7
SPIWrite 0237,f7,0,7
SPIWrite 0238,0b,0,7
SPIWrite 0239,fe,0,7
SPIWrite 023a,00,0,7
SPIWrite 023b,e0,0,7
SPIWrite 023c,90,0,7
SPIWrite 023d,46,0,7
SPIWrite 023e,20,0,7
SPIWrite 023f,46,0,7
SPIWrite 0240,29,0,7
SPIWrite 0241,46,0,7
SPIWrite 0242,33,0,7
SPIWrite 0243,46,0,7
SPIWrite 0244,42,0,7
SPIWrite 0245,46,0,7
SPIWrite 0246,dd,0,7
SPIWrite 0247,f7,0,7
SPIWrite 0248,03,0,7
SPIWrite 0249,fe,0,7
SPIWrite 024a,04,0,7
SPIWrite 024b,2f,0,7
SPIWrite 024c,10,0,7
SPIWrite 024d,d0,0,7
SPIWrite 024e,38,0,7
SPIWrite 024f,4b,0,7
SPIWrite 0250,36,0,7
SPIWrite 0251,49,0,7
SPIWrite 0252,0c,0,7
SPIWrite 0253,20,0,7
SPIWrite 0254,14,0,7
SPIWrite 0255,fb,0,7
SPIWrite 0256,00,0,7
SPIWrite 0257,f0,0,7
```

```
SPIWrite 0258,00,0,7
SPIWrite 0259,eb,0,7
SPIWrite 025a,85,0,7
SPIWrite 025b,02,0,7
SPIWrite 025c,13,0,7
SPIWrite 025d,f8,0,7
SPIWrite 025e,17,0,7
SPIWrite 025f,30,0,7
SPIWrite 0260,8a,0,7
SPIWrite 0261,58,0,7
SPIWrite 0262,00,0,7
SPIWrite 0263,eb,0,7
SPIWrite 0264,83,0,7
SPIWrite 0265,00,0,7
SPIWrite 0266,92,0,7
SPIWrite 0267,f8,0,7
SPIWrite 0268,02,0,7
SPIWrite 0269,26,0,7
SPIWrite 026a,08,0,7
SPIWrite 026b,58,0,7
SPIWrite 026c,80,0,7
SPIWrite 026d,f8,0,7
SPIWrite 026e,02,0,7
SPIWrite 026f,26,0,7
SPIWrite 0270,bd,0,7
SPIWrite 0271,e8,0,7
SPIWrite 0272,f0,0,7
SPIWrite 0273,81,0,7
SPIWrite 0274,70,0,7
SPIWrite 0275,b5,0,7
SPIWrite 0276,05,0,7
SPIWrite 0277,46,0,7
SPIWrite 0278,0c,0,7
SPIWrite 0279,46,0,7
SPIWrite 027a,de,0,7
SPIWrite 027b,f7,0,7
SPIWrite 027c,99,0,7
SPIWrite 027d,fa,0,7
SPIWrite 027e,2d,0,7
SPIWrite 027f,48,0,7
SPIWrite 0280,2a,0,7
SPIWrite 0281,4a,0,7
SPIWrite 0282,4f,0,7
SPIWrite 0283,f4,0,7
SPIWrite 0284,25,0,7
SPIWrite 0285,76,0,7
SPIWrite 0286,15,0,7
SPIWrite 0287,fb,0,7
SPIWrite 0288,06,0,7
SPIWrite 0289,f6,0,7
SPIWrite 028a,0c,0,7
SPIWrite 028b,21,0,7
```

```
SPIWrite 028c,dc,0,7
SPIWrite 028d,23,0,7
SPIWrite 028e,15,0,7
SPIWrite 028f,fb,0,7
SPIWrite 0290,01,0,7
SPIWrite 0291,f1,0,7
SPIWrite 0292,14,0,7
SPIWrite 0293,fb,0,7
SPIWrite 0294,03,0,7
SPIWrite 0295,63,0,7
SPIWrite 0296,01,0,7
SPIWrite 0297,eb,0,7
SPIWrite 0298,84,0,7
SPIWrite 0299,01,0,7
SPIWrite 029a,c0,0,7
SPIWrite 029b,18,0,7
SPIWrite 029c,54,0,7
SPIWrite 029d,58,0,7
SPIWrite 029e,90,0,7
SPIWrite 029f,f8,0,7
SPIWrite 02a0,74,0,7
SPIWrite 02a1,10,0,7
SPIWrite 02a2,90,0,7
SPIWrite 02a3,f8,0,7
SPIWrite 02a4,42,0,7
SPIWrite 02a5,20,0,7
SPIWrite 02a6,d4,0,7
SPIWrite 02a7,f8,0,7
SPIWrite 02a8,3c,0,7
SPIWrite 02a9,66,0,7
SPIWrite 02aa,52,0,7
SPIWrite 02ab,18,0,7
SPIWrite 02ac,92,0,7
SPIWrite 02ad,1e,0,7
SPIWrite 02ae,06,0,7
SPIWrite 02af,21,0,7
SPIWrite 02b0,d2,0,7
SPIWrite 02b1,b2,0,7
SPIWrite 02b2,0d,0,7
SPIWrite 02b3,46,0,7
SPIWrite 02b4,b2,0,7
SPIWrite 02b5,fb,0,7
SPIWrite 02b6,f1,0,7
SPIWrite 02b7,f1,0,7
SPIWrite 02b8,11,0,7
SPIWrite 02b9,fb,0,7
SPIWrite 02ba,05,0,7
SPIWrite 02bb,f3,0,7
SPIWrite 02bc,d2,0,7
SPIWrite 02bd,1a,0,7
SPIWrite 02be,6f,0,7
SPIWrite 02bf,f0,0,7
```

```
SPIWrite 02c0,02,0,7
SPIWrite 02c1,03,0,7
SPIWrite 02c2,d2,0,7
SPIWrite 02c3,b2,0,7
SPIWrite 02c4,9b,0,7
SPIWrite 02c5,1a,0,7
SPIWrite 02c6,63,0,7
SPIWrite 02c7,f3,0,7
SPIWrite 02c8,12,0,7
SPIWrite 02c9,46,0,7
SPIWrite 02ca,c4,0,7
SPIWrite 02cb,f8,0,7
SPIWrite 02cc,3c,0,7
SPIWrite 02cd,66,0,7
SPIWrite 02ce,90,0,7
SPIWrite 02cf,f8,0,7
SPIWrite 02d0,42,0,7
SPIWrite 02d1,00,0,7
SPIWrite 02d2,d4,0,7
SPIWrite 02d3,f8,0,7
SPIWrite 02d4,3c,0,7
SPIWrite 02d5,26,0,7
SPIWrite 02d6,00,0,7
SPIWrite 02d7,1d,0,7
SPIWrite 02d8,90,0,7
SPIWrite 02d9,fb,0,7
SPIWrite 02da,f5,0,7
SPIWrite 02db,f3,0,7
SPIWrite 02dc,4f,0,7
SPIWrite 02dd,f4,0,7
SPIWrite 02de,00,0,7
SPIWrite 02df,20,0,7
SPIWrite 02e0,c9,0,7
SPIWrite 02e1,1a,0,7
SPIWrite 02e2,00,0,7
SPIWrite 02e3,eb,0,7
SPIWrite 02e4,c1,0,7
SPIWrite 02e5,40,0,7
SPIWrite 02e6,c0,0,7
SPIWrite 02e7,0c,0,7
SPIWrite 02e8,60,0,7
SPIWrite 02e9,f3,0,7
SPIWrite 02ea,d7,0,7
SPIWrite 02eb,42,0,7
SPIWrite 02ec,c4,0,7
SPIWrite 02ed,f8,0,7
SPIWrite 02ee,3c,0,7
SPIWrite 02ef,26,0,7
SPIWrite 02f0,70,0,7
SPIWrite 02f1,bd,0,7
SPIWrite 02f2,38,0,7
SPIWrite 02f3,b5,0,7
```

```
SPIWrite 02f4,0f,0,7
SPIWrite 02f5,4a,0,7
SPIWrite 02f6,10,0,7
SPIWrite 02f7,4c,0,7
SPIWrite 02f8,4f,0,7
SPIWrite 02f9,f4,0,7
SPIWrite 02fa,25,0,7
SPIWrite 02fb,75,0,7
SPIWrite 02fc,dc,0,7
SPIWrite 02fd,23,0,7
SPIWrite 02fe,10,0,7
SPIWrite 02ff,fb,0,7
SPIWrite 0300,05,0,7
SPIWrite 0301,f5,0,7
SPIWrite 0302,b1,0,7
SPIWrite 0303,32,0,7
SPIWrite 0304,11,0,7
SPIWrite 0305,fb,0,7
SPIWrite 0306,03,0,7
SPIWrite 0307,53,0,7
SPIWrite 0308,d2,0,7
SPIWrite 0309,5c,0,7
SPIWrite 030a,94,0,7
SPIWrite 030b,f9,0,7
SPIWrite 030c,01,0,7
SPIWrite 030d,50,0,7
SPIWrite 030e,03,0,7
SPIWrite 030f,2a,0,7
SPIWrite 0310,03,0,7
SPIWrite 0311,d0,0,7
SPIWrite 0312,94,0,7
SPIWrite 0313,f9,0,7
SPIWrite 0314,01,0,7
SPIWrite 0315,20,0,7
SPIWrite 0316,92,0,7
SPIWrite 0317,1f,0,7
SPIWrite 0318,62,0,7
SPIWrite 0319,70,0,7
SPIWrite 031a,de,0,7
SPIWrite 031b,f7,0,7
SPIWrite 031c,8f,0,7
SPIWrite 031d,fc,0,7
SPIWrite 031e,65,0,7
SPIWrite 031f,70,0,7
SPIWrite 0320,38,0,7
SPIWrite 0321,bd,0,7
SPIWrite 0322,c0,0,7
SPIWrite 0323,46,0,7
SPIWrite 0324,fe,0,7
SPIWrite 0325,d5,0,7
SPIWrite 0326,00,0,7
SPIWrite 0327,20,0,7
```

```
SPIWrite 0328,b6,0,7
SPIWrite 0329,01,0,7
SPIWrite 032a,01,0,7
SPIWrite 032b,20,0,7
SPIWrite 032c,a8,0,7
SPIWrite 032d,75,0,7
SPIWrite 032e,02,0,7
SPIWrite 032f,00,0,7
SPIWrite 0330,06,0,7
SPIWrite 0331,d6,0,7
SPIWrite 0332,00,0,7
SPIWrite 0333,20,0,7
SPIWrite 0334,e0,0,7
SPIWrite 0335,ab,0,7
SPIWrite 0336,00,0,7
SPIWrite 0337,20,0,7
SPIWrite 0338,36,0,7
SPIWrite 0339,d6,0,7
SPIWrite 033a,00,0,7
SPIWrite 033b,20,0,7
SPIWrite 033c,43,0,7
SPIWrite 033d,48,0,7
SPIWrite 033e,10,0,7
SPIWrite 033f,b5,0,7
SPIWrite 0340,00,0,7
SPIWrite 0341,78,0,7
SPIWrite 0342,0c,0,7
SPIWrite 0343,46,0,7
SPIWrite 0344,fe,0,7
SPIWrite 0345,f7,0,7
SPIWrite 0346,c5,0,7
SPIWrite 0347,ff,0,7
SPIWrite 0348,00,0,7
SPIWrite 0349,20,0,7
SPIWrite 034a,20,0,7
SPIWrite 034b,70,0,7
SPIWrite 034c,10,0,7
SPIWrite 034d,bd,0,7
SPIWrite 034e,3f,0,7
SPIWrite 034f,48,0,7
SPIWrite 0350,2d,0,7
SPIWrite 0351,e9,0,7
SPIWrite 0352,f0,0,7
SPIWrite 0353,41,0,7
SPIWrite 0354,05,0,7
SPIWrite 0355,78,0,7
SPIWrite 0356,3f,0,7
SPIWrite 0357,4f,0,7
SPIWrite 0358,3d,0,7
SPIWrite 0359,48,0,7
SPIWrite 035a,00,0,7
SPIWrite 035b,22,0,7
```

```
SPIWrite 035c,0c,0,7
SPIWrite 035d,46,0,7
SPIWrite 035e,2e,0,7
SPIWrite 035f,01,0,7
SPIWrite 0360,c7,0,7
SPIWrite 0361,eb,0,7
SPIWrite 0362,82,0,7
SPIWrite 0363,01,0,7
SPIWrite 0364,0b,0,7
SPIWrite 0365,68,0,7
SPIWrite 0366,02,0,7
SPIWrite 0367,f0,0,7
SPIWrite 0368,01,0,7
SPIWrite 0369,0c,0,7
SPIWrite 036a,42,0,7
SPIWrite 036b,f3,0,7
SPIWrite 036c,5d,0,7
SPIWrite 036d,01,0,7
SPIWrite 036e,52,0,7
SPIWrite 036f,1c,0,7
SPIWrite 0370,89,0,7
SPIWrite 0371,00,0,7
SPIWrite 0372,04,0,7
SPIWrite 0373,2a,0,7
SPIWrite 0374,01,0,7
SPIWrite 0375,eb,0,7
SPIWrite 0376,cc,0,7
SPIWrite 0377,01,0,7
SPIWrite 0378,31,0,7
SPIWrite 0379,44,0,7
SPIWrite 037a,01,0,7
SPIWrite 037b,44,0,7
SPIWrite 037c,cb,0,7
SPIWrite 037d,67,0,7
SPIWrite 037e,ef,0,7
SPIWrite 037f,db,0,7
SPIWrite 0380,df,0,7
SPIWrite 0381,f8,0,7
SPIWrite 0382,d8,0,7
SPIWrite 0383,80,0,7
SPIWrite 0384,34,0,7
SPIWrite 0385,4f,0,7
SPIWrite 0386,90,0,7
SPIWrite 0387,f8,0,7
SPIWrite 0388,c2,0,7
SPIWrite 0389,20,0,7
SPIWrite 038a,d8,0,7
SPIWrite 038b,f8,0,7
SPIWrite 038c,50,0,7
SPIWrite 038d,37,0,7
SPIWrite 038e,39,0,7
SPIWrite 038f,46,0,7
```

```
SPIWrite 0390,98,0,7
SPIWrite 0391,47,0,7
SPIWrite 0392,33,0,7
SPIWrite 0393,4e,0,7
SPIWrite 0394,d8,0,7
SPIWrite 0395,f8,0,7
SPIWrite 0396,68,0,7
SPIWrite 0397,39,0,7
SPIWrite 0398,28,0,7
SPIWrite 0399,46,0,7
SPIWrite 039a,39,0,7
SPIWrite 039b,46,0,7
SPIWrite 039c,32,0,7
SPIWrite 039d,46,0,7
SPIWrite 039e,98,0,7
SPIWrite 039f,47,0,7
SPIWrite 03a0,a8,0,7
SPIWrite 03a1,19,0,7
SPIWrite 03a2,00,0,7
SPIWrite 03a3,f5,0,7
SPIWrite 03a4,33,0,7
SPIWrite 03a5,70,0,7
SPIWrite 03a6,07,0,7
SPIWrite 03a7,78,0,7
SPIWrite 03a8,00,0,7
SPIWrite 03a9,2f,0,7
SPIWrite 03aa,31,0,7
SPIWrite 03ab,d1,0,7
SPIWrite 03ac,d8,0,7
SPIWrite 03ad,f8,0,7
SPIWrite 03ae,60,0,7
SPIWrite 03af,29,0,7
SPIWrite 03b0,28,0,7
SPIWrite 03b1,46,0,7
SPIWrite 03b2,21,0,7
SPIWrite 03b3,46,0,7
SPIWrite 03b4,90,0,7
SPIWrite 03b5,47,0,7
SPIWrite 03b6,20,0,7
SPIWrite 03b7,78,0,7
SPIWrite 03b8,00,0,7
SPIWrite 03b9,28,0,7
SPIWrite 03ba,3b,0,7
SPIWrite 03bb,d1,0,7
SPIWrite 03bc,d8,0,7
SPIWrite 03bd,f8,0,7
SPIWrite 03be,70,0,7
SPIWrite 03bf,29,0,7
SPIWrite 03c0,28,0,7
SPIWrite 03c1,46,0,7
SPIWrite 03c2,21,0,7
SPIWrite 03c3,46,0,7
```

```
SPIWrite 03c4,90,0,7
SPIWrite 03c5,47,0,7
SPIWrite 03c6,20,0,7
SPIWrite 03c7,78,0,7
SPIWrite 03c8,a0,0,7
SPIWrite 03c9,bb,0,7
SPIWrite 03ca,d8,0,7
SPIWrite 03cb,f8,0,7
SPIWrite 03cc,38,0,7
SPIWrite 03cd,26,0,7
SPIWrite 03ce,28,0,7
SPIWrite 03cf,46,0,7
SPIWrite 03d0,21,0,7
SPIWrite 03d1,46,0,7
SPIWrite 03d2,90,0,7
SPIWrite 03d3,47,0,7
SPIWrite 03d4,20,0,7
SPIWrite 03d5,78,0,7
SPIWrite 03d6,68,0,7
SPIWrite 03d7,bb,0,7
SPIWrite 03d8,d8,0,7
SPIWrite 03d9,f8,0,7
SPIWrite 03da,3c,0,7
SPIWrite 03db,26,0,7
SPIWrite 03dc,28,0,7
SPIWrite 03dd,46,0,7
SPIWrite 03de,21,0,7
SPIWrite 03df,46,0,7
SPIWrite 03e0,90,0,7
SPIWrite 03e1,47,0,7
SPIWrite 03e2,20,0,7
SPIWrite 03e3,78,0,7
SPIWrite 03e4,30,0,7
SPIWrite 03e5,bb,0,7
SPIWrite 03e6,d8,0,7
SPIWrite 03e7,f8,0,7
SPIWrite 03e8,50,0,7
SPIWrite 03e9,16,0,7
SPIWrite 03ea,28,0,7
SPIWrite 03eb,46,0,7
SPIWrite 03ec,88,0,7
SPIWrite 03ed,47,0,7
SPIWrite 03ee,d8,0,7
SPIWrite 03ef,f8,0,7
SPIWrite 03f0,54,0,7
SPIWrite 03f1,16,0,7
SPIWrite 03f2,28,0,7
SPIWrite 03f3,46,0,7
SPIWrite 03f4,88,0,7
SPIWrite 03f5,47,0,7
SPIWrite 03f6,d8,0,7
SPIWrite 03f7,f8,0,7
```

```
SPIWrite 03f8,58,0,7
SPIWrite 03f9,16,0,7
SPIWrite 03fa,28,0,7
SPIWrite 03fb,46,0,7
SPIWrite 03fc,88,0,7
SPIWrite 03fd,47,0,7
SPIWrite 03fe,01,0,7
SPIWrite 03ff,20,0,7
SPIWrite 0400,00,0,7
SPIWrite 0401,21,0,7
SPIWrite 0402,a8,0,7
SPIWrite 0403,40,0,7
SPIWrite 0404,0a,0,7
SPIWrite 0405,46,0,7
SPIWrite 0406,c0,0,7
SPIWrite 0407,b2,0,7
SPIWrite 0408,ff,0,7
SPIWrite 0409,f7,0,7
SPIWrite 040a,30,0,7
SPIWrite 040b,fb,0,7
SPIWrite 040c,bd,0,7
SPIWrite 040d,e8,0,7
SPIWrite 040e,f0,0,7
SPIWrite 040f,81,0,7
SPIWrite 0410,62,0,7
SPIWrite 0411,88,0,7
SPIWrite 0412,08,0,7
SPIWrite 0413,23,0,7
SPIWrite 0414,01,0,7
SPIWrite 0415,21,0,7
SPIWrite 0416,66,0,7
SPIWrite 0417,68,0,7
SPIWrite 0418,23,0,7
SPIWrite 0419,70,0,7
SPIWrite 041a,42,0,7
SPIWrite 041b,f4,0,7
SPIWrite 041c,80,0,7
SPIWrite 041d,42,0,7
SPIWrite 041e,01,0,7
SPIWrite 041f,fa,0,7
SPIWrite 0420,05,0,7
SPIWrite 0421,f3,0,7
SPIWrite 0422,62,0,7
SPIWrite 0423,80,0,7
SPIWrite 0424,33,0,7
SPIWrite 0425,43,0,7
SPIWrite 0426,63,0,7
SPIWrite 0427,60,0,7
SPIWrite 0428,00,0,7
SPIWrite 0429,78,0,7
SPIWrite 042a,62,0,7
SPIWrite 042b,68,0,7
```

```
SPIWrite 042c,00,0,7
SPIWrite 042d,1d,0,7
SPIWrite 042e,81,0,7
SPIWrite 042f,40,0,7
SPIWrite 0430,11,0,7
SPIWrite 0431,43,0,7
SPIWrite 0432,61,0,7
SPIWrite 0433,60,0,7
SPIWrite 0434,bd,0,7
SPIWrite 0435,e8,0,7
SPIWrite 0436,f0,0,7
SPIWrite 0437,81,0,7
SPIWrite 0438,04,0,7
SPIWrite 0439,48,0,7
SPIWrite 043a,00,0,7
SPIWrite 043b,78,0,7
SPIWrite 043c,02,0,7
SPIWrite 043d,28,0,7
SPIWrite 043e,a4,0,7
SPIWrite 043f,bf,0,7
SPIWrite 0440,04,0,7
SPIWrite 0441,20,0,7
SPIWrite 0442,08,0,7
SPIWrite 0443,70,0,7
SPIWrite 0444,01,0,7
SPIWrite 0445,da,0,7
SPIWrite 0446,ff,0,7
SPIWrite 0447,f7,0,7
SPIWrite 0448,48,0,7
SPIWrite 0449,be,0,7
SPIWrite 044a,70,0,7
SPIWrite 044b,47,0,7
SPIWrite 044c,b4,0,7
SPIWrite 044d,03,0,7
SPIWrite 044e,00,0,7
SPIWrite 044f,a2,0,7
SPIWrite 0450,b4,0,7
SPIWrite 0451,01,0,7
SPIWrite 0452,01,0,7
SPIWrite 0453,20,0,7
SPIWrite 0454,4b,0,7
SPIWrite 0455,fc,0,7
SPIWrite 0456,ff,0,7
SPIWrite 0457,5d,0,7
SPIWrite 0458,18,0,7
SPIWrite 0459,ff,0,7
SPIWrite 045a,00,0,7
SPIWrite 045b,20,0,7
SPIWrite 045c,90,0,7
SPIWrite 045d,d6,0,7
SPIWrite 045e,00,0,7
SPIWrite 045f,20,0,7
```

```
SPIWrite 0460,d4,0,7
SPIWrite 0461,fb,0,7
SPIWrite 0462,00,0,7
SPIWrite 0463,20,0,7
SPIWrite 0464,0a,0,7
SPIWrite 0465,46,0,7
SPIWrite 0466,2d,0,7
SPIWrite 0467,e9,0,7
SPIWrite 0468,f8,0,7
SPIWrite 0469,4f,0,7
SPIWrite 046a,01,0,7
SPIWrite 046b,46,0,7
SPIWrite 046c,4f,0,7
SPIWrite 046d,f0,0,7
SPIWrite 046e,aa,0,7
SPIWrite 046f,0a,0,7
SPIWrite 0470,00,0,7
SPIWrite 0471,20,0,7
SPIWrite 0472,a1,0,7
SPIWrite 0473,f1,0,7
SPIWrite 0474,aa,0,7
SPIWrite 0475,08,0,7
SPIWrite 0476,d3,0,7
SPIWrite 0477,46,0,7
SPIWrite 0478,04,0,7
SPIWrite 0479,46,0,7
SPIWrite 047a,00,0,7
SPIWrite 047b,92,0,7
SPIWrite 047c,08,0,7
SPIWrite 047d,f1,0,7
SPIWrite 047e,aa,0,7
SPIWrite 047f,08,0,7
SPIWrite 0480,98,0,7
SPIWrite 0481,f8,0,7
SPIWrite 0482,a6,0,7
SPIWrite 0483,20,0,7
SPIWrite 0484,04,0,7
SPIWrite 0485,2a,0,7
SPIWrite 0486,56,0,7
SPIWrite 0487,da,0,7
SPIWrite 0488,98,0,7
SPIWrite 0489,f8,0,7
SPIWrite 048a,04,0,7
SPIWrite 048b,70,0,7
SPIWrite 048c,00,0,7
SPIWrite 048d,2f,0,7
SPIWrite 048e,52,0,7
SPIWrite 048f,d0,0,7
SPIWrite 0490,7f,0,7
SPIWrite 0491,1e,0,7
SPIWrite 0492,7a,0,7
SPIWrite 0493,1c,0,7
```

```
SPIWrite 0494,5f,0,7
SPIWrite 0495,fa,0,7
SPIWrite 0496,87,0,7
SPIWrite 0497,f9,0,7
SPIWrite 0498,d2,0,7
SPIWrite 0499,b2,0,7
SPIWrite 049a,06,0,7
SPIWrite 049b,2a,0,7
SPIWrite 049c,48,0,7
SPIWrite 049d,da,0,7
SPIWrite 049e,5b,0,7
SPIWrite 049f,46,0,7
SPIWrite 04a0,03,0,7
SPIWrite 04a1,fb,0,7
SPIWrite 04a2,04,0,7
SPIWrite 04a3,13,0,7
SPIWrite 04a4,1d,0,7
SPIWrite 04a5,7c,0,7
SPIWrite 04a6,00,0,7
SPIWrite 04a7,23,0,7
SPIWrite 04a8,37,0,7
SPIWrite 04a9,e0,0,7
SPIWrite 04aa,c5,0,7
SPIWrite 04ab,18,0,7
SPIWrite 04ac,4d,0,7
SPIWrite 04ad,19,0,7
SPIWrite 04ae,ed,0,7
SPIWrite 04af,7d,0,7
SPIWrite 04b0,09,0,7
SPIWrite 04b1,26,0,7
SPIWrite 04b2,19,0,7
SPIWrite 04b3,fb,0,7
SPIWrite 04b4,06,0,7
SPIWrite 04b5,f6,0,7
SPIWrite 04b6,77,0,7
SPIWrite 04b7,19,0,7
SPIWrite 04b8,c7,0,7
SPIWrite 04b9,19,0,7
SPIWrite 04ba,cf,0,7
SPIWrite 04bb,19,0,7
SPIWrite 04bc,97,0,7
SPIWrite 04bd,f9,0,7
SPIWrite 04be,22,0,7
SPIWrite 04bf,e0,0,7
SPIWrite 04c0,02,0,7
SPIWrite 04c1,eb,0,7
SPIWrite 04c2,c2,0,7
SPIWrite 04c3,0c,0,7
SPIWrite 04c4,ae,0,7
SPIWrite 04c5,19,0,7
SPIWrite 04c6,86,0,7
SPIWrite 04c7,19,0,7
```

```
SPIWrite 04c8,47,0,7
SPIWrite 04c9,19,0,7
SPIWrite 04ca,8e,0,7
SPIWrite 04cb,19,0,7
SPIWrite 04cc,67,0,7
SPIWrite 04cd,44,0,7
SPIWrite 04ce,cf,0,7
SPIWrite 04cf,19,0,7
SPIWrite 04d0,87,0,7
SPIWrite 04d1,f8,0,7
SPIWrite 04d2,22,0,7
SPIWrite 04d3,e0,0,7
SPIWrite 04d4,96,0,7
SPIWrite 04d5,f9,0,7
SPIWrite 04d6,58,0,7
SPIWrite 04d7,70,0,7
SPIWrite 04d8,46,0,7
SPIWrite 04d9,19,0,7
SPIWrite 04da,0b,0,7
SPIWrite 04db,fb,0,7
SPIWrite 04dc,04,0,7
SPIWrite 04dd,f0,0,7
SPIWrite 04de,0c,0,7
SPIWrite 04df,eb,0,7
SPIWrite 04e0,06,0,7
SPIWrite 04e1,05,0,7
SPIWrite 04e2,4e,0,7
SPIWrite 04e3,19,0,7
SPIWrite 04e4,0d,0,7
SPIWrite 04e5,18,0,7
SPIWrite 04e6,86,0,7
SPIWrite 04e7,f8,0,7
SPIWrite 04e8,58,0,7
SPIWrite 04e9,70,0,7
SPIWrite 04ea,ad,0,7
SPIWrite 04eb,7d,0,7
SPIWrite 04ec,5b,0,7
SPIWrite 04ed,1c,0,7
SPIWrite 04ee,db,0,7
SPIWrite 04ef,b2,0,7
SPIWrite 04f0,19,0,7
SPIWrite 04f1,e0,0,7
SPIWrite 04f2,03,0,7
SPIWrite 04f3,25,0,7
SPIWrite 04f4,19,0,7
SPIWrite 04f5,fb,0,7
SPIWrite 04f6,05,0,7
SPIWrite 04f7,35,0,7
SPIWrite 04f8,45,0,7
SPIWrite 04f9,19,0,7
SPIWrite 04fa,4d,0,7
SPIWrite 04fb,19,0,7
```

```
SPIWrite 04fc,95,0,7
SPIWrite 04fd,f8,0,7
SPIWrite 04fe,8e,0,7
SPIWrite 04ff,70,0,7
SPIWrite 0500,02,0,7
SPIWrite 0501,eb,0,7
SPIWrite 0502,42,0,7
SPIWrite 0503,06,0,7
SPIWrite 0504,9d,0,7
SPIWrite 0505,19,0,7
SPIWrite 0506,45,0,7
SPIWrite 0507,19,0,7
SPIWrite 0508,0a,0,7
SPIWrite 0509,fb,0,7
SPIWrite 050a,04,0,7
SPIWrite 050b,f0,0,7
SPIWrite 050c,4e,0,7
SPIWrite 050d,19,0,7
SPIWrite 050e,0d,0,7
SPIWrite 050f,18,0,7
SPIWrite 0510,86,0,7
SPIWrite 0511,f8,0,7
SPIWrite 0512,8e,0,7
SPIWrite 0513,70,0,7
SPIWrite 0514,2d,0,7
SPIWrite 0515,7c,0,7
SPIWrite 0516,5b,0,7
SPIWrite 0517,1c,0,7
SPIWrite 0518,db,0,7
SPIWrite 0519,b2,0,7
SPIWrite 051a,9d,0,7
SPIWrite 051b,42,0,7
SPIWrite 051c,e9,0,7
SPIWrite 051d,dc,0,7
SPIWrite 051e,0a,0,7
SPIWrite 051f,fb,0,7
SPIWrite 0520,04,0,7
SPIWrite 0521,13,0,7
SPIWrite 0522,9d,0,7
SPIWrite 0523,7d,0,7
SPIWrite 0524,00,0,7
SPIWrite 0525,23,0,7
SPIWrite 0526,9d,0,7
SPIWrite 0527,42,0,7
SPIWrite 0528,bf,0,7
SPIWrite 0529,dc,0,7
SPIWrite 052a,52,0,7
SPIWrite 052b,1c,0,7
SPIWrite 052c,06,0,7
SPIWrite 052d,2a,0,7
SPIWrite 052e,b6,0,7
SPIWrite 052f,db,0,7
```

```
SPIWrite 0530,06,0,7
SPIWrite 0531,22,0,7
SPIWrite 0532,88,0,7
SPIWrite 0533,f8,0,7
SPIWrite 0534,04,0,7
SPIWrite 0535,20,0,7
SPIWrite 0536,64,0,7
SPIWrite 0537,1c,0,7
SPIWrite 0538,aa,0,7
SPIWrite 0539,30,0,7
SPIWrite 053a,06,0,7
SPIWrite 053b,2c,0,7
SPIWrite 053c,9e,0,7
SPIWrite 053d,db,0,7
SPIWrite 053e,00,0,7
SPIWrite 053f,9a,0,7
SPIWrite 0540,08,0,7
SPIWrite 0541,46,0,7
SPIWrite 0542,11,0,7
SPIWrite 0543,46,0,7
SPIWrite 0544,e3,0,7
SPIWrite 0545,f7,0,7
SPIWrite 0546,3e,0,7
SPIWrite 0547,fd,0,7
SPIWrite 0548,bd,0,7
SPIWrite 0549,e8,0,7
SPIWrite 054a,f8,0,7
SPIWrite 054b,8f,0,7
SPIWrite 054c,10,0,7
SPIWrite 054d,b5,0,7
SPIWrite 054e,30,0,7
SPIWrite 054f,4a,0,7
SPIWrite 0550,2e,0,7
SPIWrite 0551,4c,0,7
SPIWrite 0552,13,0,7
SPIWrite 0553,78,0,7
SPIWrite 0554,54,0,7
SPIWrite 0555,f8,0,7
SPIWrite 0556,20,0,7
SPIWrite 0557,40,0,7
SPIWrite 0558,84,0,7
SPIWrite 0559,f8,0,7
SPIWrite 055a,58,0,7
SPIWrite 055b,3e,0,7
SPIWrite 055c,06,0,7
SPIWrite 055d,20,0,7
SPIWrite 055e,c0,0,7
SPIWrite 055f,f2,0,7
SPIWrite 0560,00,0,7
SPIWrite 0561,00,0,7
SPIWrite 0562,03,0,7
SPIWrite 0563,46,0,7
```

```
SPIWrite 0564,5b,0,7
SPIWrite 0565,1e,0,7
SPIWrite 0566,fd,0,7
SPIWrite 0567,d1,0,7
SPIWrite 0568,53,0,7
SPIWrite 0569,78,0,7
SPIWrite 056a,04,0,7
SPIWrite 056b,eb,0,7
SPIWrite 056c,83,0,7
SPIWrite 056d,03,0,7
SPIWrite 056e,c3,0,7
SPIWrite 056f,f8,0,7
SPIWrite 0570,c0,0,7
SPIWrite 0571,13,0,7
SPIWrite 0572,40,0,7
SPIWrite 0573,1e,0,7
SPIWrite 0574,fd,0,7
SPIWrite 0575,d1,0,7
SPIWrite 0576,50,0,7
SPIWrite 0577,78,0,7
SPIWrite 0578,84,0,7
SPIWrite 0579,f8,0,7
SPIWrite 057a,58,0,7
SPIWrite 057b,0e,0,7
SPIWrite 057c,10,0,7
SPIWrite 057d,bd,0,7
SPIWrite 057e,f8,0,7
SPIWrite 057f,b5,0,7
SPIWrite 0580,dd,0,7
SPIWrite 0581,f8,0,7
SPIWrite 0582,18,0,7
SPIWrite 0583,c0,0,7
SPIWrite 0584,07,0,7
SPIWrite 0585,46,0,7
SPIWrite 0586,14,0,7
SPIWrite 0587,46,0,7
SPIWrite 0588,1d,0,7
SPIWrite 0589,46,0,7
SPIWrite 058a,0e,0,7
SPIWrite 058b,46,0,7
SPIWrite 058c,cd,0,7
SPIWrite 058d,f8,0,7
SPIWrite 058e,00,0,7
SPIWrite 058f,c0,0,7
SPIWrite 0590,ea,0,7
SPIWrite 0591,f7,0,7
SPIWrite 0592,1e,0,7
SPIWrite 0593,fb,0,7
SPIWrite 0594,55,0,7
SPIWrite 0595,ea,0,7
SPIWrite 0596,04,0,7
SPIWrite 0597,00,0,7
```

```
SPIWrite 0598,37,0,7
SPIWrite 0599,d1,0,7
SPIWrite 059a,1e,0,7
SPIWrite 059b,4b,0,7
SPIWrite 059c,1e,0,7
SPIWrite 059d,4a,0,7
SPIWrite 059e,03,0,7
SPIWrite 059f,eb,0,7
SPIWrite 05a0,67,0,7
SPIWrite 05a1,01,0,7
SPIWrite 05a2,73,0,7
SPIWrite 05a3,31,0,7
SPIWrite 05a4,08,0,7
SPIWrite 05a5,78,0,7
SPIWrite 05a6,b3,0,7
SPIWrite 05a7,f8,0,7
SPIWrite 05a8,9e,0,7
SPIWrite 05a9,41,0,7
SPIWrite 05aa,12,0,7
SPIWrite 05ab,5c,0,7
SPIWrite 05ac,38,0,7
SPIWrite 05ad,46,0,7
SPIWrite 05ae,54,0,7
SPIWrite 05af,43,0,7
SPIWrite 05b0,47,0,7
SPIWrite 05b1,b1,0,7
SPIWrite 05b2,01,0,7
SPIWrite 05b3,2f,0,7
SPIWrite 05b4,08,0,7
SPIWrite 05b5,bf,0,7
SPIWrite 05b6,00,0,7
SPIWrite 05b7,25,0,7
SPIWrite 05b8,05,0,7
SPIWrite 05b9,d0,0,7
SPIWrite 05ba,02,0,7
SPIWrite 05bb,2f,0,7
SPIWrite 05bc,0c,0,7
SPIWrite 05bd,bf,0,7
SPIWrite 05be,03,0,7
SPIWrite 05bf,25,0,7
SPIWrite 05c0,02,0,7
SPIWrite 05c1,25,0,7
SPIWrite 05c2,00,0,7
SPIWrite 05c3,e0,0,7
SPIWrite 05c4,01,0,7
SPIWrite 05c5,25,0,7
SPIWrite 05c6,15,0,7
SPIWrite 05c7,4a,0,7
SPIWrite 05c8,d2,0,7
SPIWrite 05c9,5d,0,7
SPIWrite 05ca,01,0,7
SPIWrite 05cb,2a,0,7
```

```
SPIWrite 05cc,02,0,7
SPIWrite 05cd,d0,0,7
SPIWrite 05ce,91,0,7
SPIWrite 05cf,f8,0,7
SPIWrite 05d0,7e,0,7
SPIWrite 05d1,30,0,7
SPIWrite 05d2,23,0,7
SPIWrite 05d3,b1,0,7
SPIWrite 05d4,79,0,7
SPIWrite 05d5,08,0,7
SPIWrite 05d6,02,0,7
SPIWrite 05d7,d3,0,7
SPIWrite 05d8,28,0,7
SPIWrite 05d9,46,0,7
SPIWrite 05da,41,0,7
SPIWrite 05db,1c,0,7
SPIWrite 05dc,cd,0,7
SPIWrite 05dd,b2,0,7
SPIWrite 05de,d6,0,7
SPIWrite 05df,f8,0,7
SPIWrite 05e0,01,0,7
SPIWrite 05e1,10,0,7
SPIWrite 05e2,27,0,7
SPIWrite 05e3,09,0,7
SPIWrite 05e4,0a,0,7
SPIWrite 05e5,01,0,7
SPIWrite 05e6,b2,0,7
SPIWrite 05e7,fb,0,7
SPIWrite 05e8,f4,0,7
SPIWrite 05e9,f2,0,7
SPIWrite 05ea,07,0,7
SPIWrite 05eb,fb,0,7
SPIWrite 05ec,12,0,7
SPIWrite 05ed,11,0,7
SPIWrite 05ee,ff,0,7
SPIWrite 05ef,f7,0,7
SPIWrite 05f0,ad,0,7
SPIWrite 05f1,ff,0,7
SPIWrite 05f2,30,0,7
SPIWrite 05f3,78,0,7
SPIWrite 05f4,48,0,7
SPIWrite 05f5,b1,0,7
SPIWrite 05f6,d6,0,7
SPIWrite 05f7,f8,0,7
SPIWrite 05f8,06,0,7
SPIWrite 05f9,00,0,7
SPIWrite 05fa,01,0,7
SPIWrite 05fb,01,0,7
SPIWrite 05fc,b1,0,7
SPIWrite 05fd,fb,0,7
SPIWrite 05fe,f4,0,7
SPIWrite 05ff,f1,0,7
```

```
SPIWrite 0600,07,0,7
SPIWrite 0601,fb,0,7
SPIWrite 0602,11,0,7
SPIWrite 0603,01,0,7
SPIWrite 0604,28,0,7
SPIWrite 0605,46,0,7
SPIWrite 0606,ff,0,7
SPIWrite 0607,f7,0,7
SPIWrite 0608,a1,0,7
SPIWrite 0609,ff,0,7
SPIWrite 060a,f8,0,7
SPIWrite 060b,bd,0,7
SPIWrite 060c,bc,0,7
SPIWrite 060d,77,0,7
SPIWrite 060e,02,0,7
SPIWrite 060f,00,0,7
SPIWrite 0610,96,0,7
SPIWrite 0611,19,0,7
SPIWrite 0612,01,0,7
SPIWrite 0613,20,0,7
SPIWrite 0614,b4,0,7
SPIWrite 0615,01,0,7
SPIWrite 0616,01,0,7
SPIWrite 0617,20,0,7
SPIWrite 0618,3b,0,7
SPIWrite 0619,78,0,7
SPIWrite 061a,02,0,7
SPIWrite 061b,00,0,7
SPIWrite 061c,98,0,7
SPIWrite 061d,fe,0,7
SPIWrite 061e,00,0,7
SPIWrite 061f,20,0,7
SPIWrite 0620,1d,0,7
SPIWrite 0621,48,0,7
SPIWrite 0622,b0,0,7
SPIWrite 0623,b5,0,7
SPIWrite 0624,00,0,7
SPIWrite 0625,78,0,7
SPIWrite 0626,48,0,7
SPIWrite 0627,bb,0,7
SPIWrite 0628,1c,0,7
SPIWrite 0629,48,0,7
SPIWrite 062a,00,0,7
SPIWrite 062b,78,0,7
SPIWrite 062c,30,0,7
SPIWrite 062d,bb,0,7
SPIWrite 062e,1d,0,7
SPIWrite 062f,48,0,7
SPIWrite 0630,1b,0,7
SPIWrite 0631,4a,0,7
SPIWrite 0632,02,0,7
SPIWrite 0633,21,0,7
```

```
SPIWrite 0634,0c,0,7
SPIWrite 0635,38,0,7
SPIWrite 0636,50,0,7
SPIWrite 0637,f8,0,7
SPIWrite 0638,0c,0,7
SPIWrite 0639,3f,0,7
SPIWrite 063a,93,0,7
SPIWrite 063b,f8,0,7
SPIWrite 063c,40,0,7
SPIWrite 063d,47,0,7
SPIWrite 063e,93,0,7
SPIWrite 063f,f8,0,7
SPIWrite 0640,41,0,7
SPIWrite 0641,77,0,7
SPIWrite 0642,0f,0,7
SPIWrite 0643,b9,0,7
SPIWrite 0644,83,0,7
SPIWrite 0645,f8,0,7
SPIWrite 0646,70,0,7
SPIWrite 0647,47,0,7
SPIWrite 0648,52,0,7
SPIWrite 0649,f8,0,7
SPIWrite 064a,08,0,7
SPIWrite 064b,4b,0,7
SPIWrite 064c,94,0,7
SPIWrite 064d,f8,0,7
SPIWrite 064e,80,0,7
SPIWrite 064f,5b,0,7
SPIWrite 0650,d4,0,7
SPIWrite 0651,f8,0,7
SPIWrite 0652,80,0,7
SPIWrite 0653,3b,0,7
SPIWrite 0654,49,0,7
SPIWrite 0655,1e,0,7
SPIWrite 0656,65,0,7
SPIWrite 0657,f3,0,7
SPIWrite 0658,4d,0,7
SPIWrite 0659,33,0,7
SPIWrite 065a,c4,0,7
SPIWrite 065b,f8,0,7
SPIWrite 065c,80,0,7
SPIWrite 065d,3b,0,7
SPIWrite 065e,ea,0,7
SPIWrite 065f,d1,0,7
SPIWrite 0660,11,0,7
SPIWrite 0661,4c,0,7
SPIWrite 0662,04,0,7
SPIWrite 0663,20,0,7
SPIWrite 0664,54,0,7
SPIWrite 0665,f8,0,7
SPIWrite 0666,04,0,7
SPIWrite 0667,3b,0,7
```

```
SPIWrite 0668,93,0,7
SPIWrite 0669,f8,0,7
SPIWrite 066a,71,0,7
SPIWrite 066b,27,0,7
SPIWrite 066c,93,0,7
SPIWrite 066d,f8,0,7
SPIWrite 066e,72,0,7
SPIWrite 066f,17,0,7
SPIWrite 0670,40,0,7
SPIWrite 0671,1e,0,7
SPIWrite 0672,01,0,7
SPIWrite 0673,ea,0,7
SPIWrite 0674,02,0,7
SPIWrite 0675,01,0,7
SPIWrite 0676,83,0,7
SPIWrite 0677,f8,0,7
SPIWrite 0678,70,0,7
SPIWrite 0679,17,0,7
SPIWrite 067a,f3,0,7
SPIWrite 067b,d1,0,7
SPIWrite 067c,b0,0,7
SPIWrite 067d,bd,0,7
SPIWrite 067e,08,0,7
SPIWrite 067f,b5,0,7
SPIWrite 0680,d8,0,7
SPIWrite 0681,f7,0,7
SPIWrite 0682,e6,0,7
SPIWrite 0683,fe,0,7
SPIWrite 0684,ff,0,7
SPIWrite 0685,f7,0,7
SPIWrite 0686,cc,0,7
SPIWrite 0687,ff,0,7
SPIWrite 0688,08,0,7
SPIWrite 0689,bd,0,7
SPIWrite 068a,08,0,7
SPIWrite 068b,b5,0,7
SPIWrite 068c,d8,0,7
SPIWrite 068d,f7,0,7
SPIWrite 068e,94,0,7
SPIWrite 068f,ff,0,7
SPIWrite 0690,ff,0,7
SPIWrite 0691,f7,0,7
SPIWrite 0692,c6,0,7
SPIWrite 0693,ff,0,7
SPIWrite 0694,08,0,7
SPIWrite 0695,bd,0,7
SPIWrite 0696,c0,0,7
SPIWrite 0697,46,0,7
SPIWrite 0698,c2,0,7
SPIWrite 0699,19,0,7
SPIWrite 069a,01,0,7
SPIWrite 069b,20,0,7
```

```
SPIWrite 069c,f4,0,7
SPIWrite 069d,22,0,7
SPIWrite 069e,01,0,7
SPIWrite 069f,20,0,7
SPIWrite 06a0,bc,0,7
SPIWrite 06a1,77,0,7
SPIWrite 06a2,02,0,7
SPIWrite 06a3,00,0,7
SPIWrite 06a4,a8,0,7
SPIWrite 06a5,75,0,7
SPIWrite 06a6,02,0,7
SPIWrite 06a7,00,0,7
SPIWrite 06a8,9c,0,7
SPIWrite 06a9,77,0,7
SPIWrite 06aa,02,0,7
SPIWrite 06ab,00,0,7
SPIWrite 06ac,14,0,7
SPIWrite 06ad,49,0,7
SPIWrite 06ae,13,0,7
SPIWrite 06af,48,0,7
SPIWrite 06b0,09,0,7
SPIWrite 06b1,68,0,7
SPIWrite 06b2,00,0,7
SPIWrite 06b3,88,0,7
SPIWrite 06b4,00,0,7
SPIWrite 06b5,22,0,7
SPIWrite 06b6,48,0,7
SPIWrite 06b7,43,0,7
SPIWrite 06b8,c0,0,7
SPIWrite 06b9,f3,0,7
SPIWrite 06ba,40,0,7
SPIWrite 06bb,11,0,7
SPIWrite 06bc,01,0,7
SPIWrite 06bd,eb,0,7
SPIWrite 06be,90,0,7
SPIWrite 06bf,10,0,7
SPIWrite 06c0,06,0,7
SPIWrite 06c1,e0,0,7
SPIWrite 06c2,13,0,7
SPIWrite 06c3,21,0,7
SPIWrite 06c4,c0,0,7
SPIWrite 06c5,f2,0,7
SPIWrite 06c6,00,0,7
SPIWrite 06c7,01,0,7
SPIWrite 06c8,49,0,7
SPIWrite 06c9,1e,0,7
SPIWrite 06ca,fd,0,7
SPIWrite 06cb,d1,0,7
SPIWrite 06cc,00,0,7
SPIWrite 06cd,bf,0,7
SPIWrite 06ce,52,0,7
SPIWrite 06cf,1c,0,7
```

```
SPIWrite 06d0,90,0,7
SPIWrite 06d1,42,0,7
SPIWrite 06d2,f6,0,7
SPIWrite 06d3,d8,0,7
SPIWrite 06d4,70,0,7
SPIWrite 06d5,47,0,7
SPIWrite 06d6,f8,0,7
SPIWrite 06d7,b5,0,7
SPIWrite 06d8,0a,0,7
SPIWrite 06d9,4d,0,7
SPIWrite 06da,00,0,7
SPIWrite 06db,24,0,7
SPIWrite 06dc,0e,0,7
SPIWrite 06dd,46,0,7
SPIWrite 06de,07,0,7
SPIWrite 06df,46,0,7
SPIWrite 06e0,07,0,7
SPIWrite 06e1,e0,0,7
SPIWrite 06e2,38,0,7
SPIWrite 06e3,46,0,7
SPIWrite 06e4,31,0,7
SPIWrite 06e5,46,0,7
SPIWrite 06e6,e6,0,7
SPIWrite 06e7,f7,0,7
SPIWrite 06e8,a3,0,7
SPIWrite 06e9,f8,0,7
SPIWrite 06ea,ff,0,7
SPIWrite 06eb,f7,0,7
SPIWrite 06ec,df,0,7
SPIWrite 06ed,ff,0,7
SPIWrite 06ee,64,0,7
SPIWrite 06ef,1c,0,7
SPIWrite 06f0,e4,0,7
SPIWrite 06f1,b2,0,7
SPIWrite 06f2,28,0,7
SPIWrite 06f3,78,0,7
SPIWrite 06f4,a0,0,7
SPIWrite 06f5,42,0,7
SPIWrite 06f6,f4,0,7
SPIWrite 06f7,dc,0,7
SPIWrite 06f8,f8,0,7
SPIWrite 06f9,bd,0,7
SPIWrite 06fa,c0,0,7
SPIWrite 06fb,46,0,7
SPIWrite 06fc,f0,0,7
SPIWrite 06fd,22,0,7
SPIWrite 06fe,01,0,7
SPIWrite 06ff,20,0,7
SPIWrite 0700,68,0,7
SPIWrite 0701,03,0,7
SPIWrite 0702,01,0,7
SPIWrite 0703,20,0,7
```

```
SPIWrite 0704,f7,0,7
SPIWrite 0705,22,0,7
SPIWrite 0706,01,0,7
SPIWrite 0707,20,0,7
SPIWrite 0708,2d,0,7
SPIWrite 0709,e9,0,7
SPIWrite 070a,fe,0,7
SPIWrite 070b,4f,0,7
SPIWrite 070c,00,0,7
SPIWrite 070d,25,0,7
SPIWrite 070e,9b,0,7
SPIWrite 070f,46,0,7
SPIWrite 0710,91,0,7
SPIWrite 0711,46,0,7
SPIWrite 0712,80,0,7
SPIWrite 0713,46,0,7
SPIWrite 0714,0c,0,7
SPIWrite 0715,af,0,7
SPIWrite 0716,01,0,7
SPIWrite 0717,91,0,7
SPIWrite 0718,97,0,7
SPIWrite 0719,f8,0,7
SPIWrite 071a,00,0,7
SPIWrite 071b,a0,0,7
SPIWrite 071c,01,0,7
SPIWrite 071d,98,0,7
SPIWrite 071e,08,0,7
SPIWrite 071f,b9,0,7
SPIWrite 0720,5d,0,7
SPIWrite 0721,45,0,7
SPIWrite 0722,19,0,7
SPIWrite 0723,d1,0,7
SPIWrite 0724,05,0,7
SPIWrite 0725,eb,0,7
SPIWrite 0726,49,0,7
SPIWrite 0727,01,0,7
SPIWrite 0728,08,0,7
SPIWrite 0729,eb,0,7
SPIWrite 072a,c5,0,7
SPIWrite 072b,00,0,7
SPIWrite 072c,08,0,7
SPIWrite 072d,eb,0,7
SPIWrite 072e,c1,0,7
SPIWrite 072f,06,0,7
SPIWrite 0730,b0,0,7
SPIWrite 0731,f9,0,7
SPIWrite 0732,a4,0,7
SPIWrite 0733,7c,0,7
SPIWrite 0734,b6,0,7
SPIWrite 0735,f9,0,7
SPIWrite 0736,24,0,7
SPIWrite 0737,40,0,7
```

```
SPIWrite 0738,4a,0,7
SPIWrite 0739,46,0,7
SPIWrite 073a,2b,0,7
SPIWrite 073b,46,0,7
SPIWrite 073c,40,0,7
SPIWrite 073d,46,0,7
SPIWrite 073e,00,0,7
SPIWrite 073f,21,0,7
SPIWrite 0740,cd,0,7
SPIWrite 0741,f8,0,7
SPIWrite 0742,00,0,7
SPIWrite 0743,a0,0,7
SPIWrite 0744,d4,0,7
SPIWrite 0745,f7,0,7
SPIWrite 0746,f5,0,7
SPIWrite 0747,f9,0,7
SPIWrite 0748,e4,0,7
SPIWrite 0749,1b,0,7
SPIWrite 074a,6f,0,7
SPIWrite 074b,f3,0,7
SPIWrite 074c,df,0,7
SPIWrite 074d,34,0,7
SPIWrite 074e,84,0,7
SPIWrite 074f,f4,0,7
SPIWrite 0750,80,0,7
SPIWrite 0751,44,0,7
SPIWrite 0752,a4,0,7
SPIWrite 0753,f5,0,7
SPIWrite 0754,80,0,7
SPIWrite 0755,44,0,7
SPIWrite 0756,b4,0,7
SPIWrite 0757,84,0,7
SPIWrite 0758,6d,0,7
SPIWrite 0759,1c,0,7
SPIWrite 075a,02,0,7
SPIWrite 075b,2d,0,7
SPIWrite 075c,de,0,7
SPIWrite 075d,db,0,7
SPIWrite 075e,bd,0,7
SPIWrite 075f,e8,0,7
SPIWrite 0760,fe,0,7
SPIWrite 0761,8f,0,7
SPIWrite 0762,00,0,7
SPIWrite 0763,00,0,7
SPIWrite 0764,98,0,7
SPIWrite 0765,b5,0,7
SPIWrite 0766,e6,0,7
SPIWrite 0767,f7,0,7
SPIWrite 0768,89,0,7
SPIWrite 0769,fb,0,7
SPIWrite 076a,0c,0,7
SPIWrite 076b,48,0,7
```

```
SPIWrite 076c,0c,0,7
SPIWrite 076d,4a,0,7
SPIWrite 076e,00,0,7
SPIWrite 076f,27,0,7
SPIWrite 0770,4f,0,7
SPIWrite 0771,f6,0,7
SPIWrite 0772,df,0,7
SPIWrite 0773,73,0,7
SPIWrite 0774,40,0,7
SPIWrite 0775,1e,0,7
SPIWrite 0776,10,0,7
SPIWrite 0777,f8,0,7
SPIWrite 0778,01,0,7
SPIWrite 0779,1f,0,7
SPIWrite 077a,01,0,7
SPIWrite 077b,29,0,7
SPIWrite 077c,09,0,7
SPIWrite 077d,d1,0,7
SPIWrite 077e,00,0,7
SPIWrite 077f,2f,0,7
SPIWrite 0780,14,0,7
SPIWrite 0781,bf,0,7
SPIWrite 0782,02,0,7
SPIWrite 0783,f1,0,7
SPIWrite 0784,b8,0,7
SPIWrite 0785,04,0,7
SPIWrite 0786,14,0,7
SPIWrite 0787,1c,0,7
SPIWrite 0788,21,0,7
SPIWrite 0789,88,0,7
SPIWrite 078a,19,0,7
SPIWrite 078b,40,0,7
SPIWrite 078c,41,0,7
SPIWrite 078d,f4,0,7
SPIWrite 078e,00,0,7
SPIWrite 078f,51,0,7
SPIWrite 0790,21,0,7
SPIWrite 0791,80,0,7
SPIWrite 0792,7f,0,7
SPIWrite 0793,1c,0,7
SPIWrite 0794,02,0,7
SPIWrite 0795,2f,0,7
SPIWrite 0796,ee,0,7
SPIWrite 0797,db,0,7
SPIWrite 0798,98,0,7
SPIWrite 0799,bd,0,7
SPIWrite 079a,c0,0,7
SPIWrite 079b,46,0,7
SPIWrite 079c,9e,0,7
SPIWrite 079d,13,0,7
SPIWrite 079e,01,0,7
SPIWrite 079f,20,0,7
```

```
SPIWrite 07a0,06,0,7
SPIWrite 07a1,07,0,7
SPIWrite 07a2,06,0,7
SPIWrite 07a3,a8,0,7
SPIWrite 07a4,0b,0,7
SPIWrite 07a5,49,0,7
SPIWrite 07a6,0c,0,7
SPIWrite 07a7,4b,0,7
SPIWrite 07a8,0c,0,7
SPIWrite 07a9,22,0,7
SPIWrite 07aa,10,0,7
SPIWrite 07ab,b5,0,7
SPIWrite 07ac,09,0,7
SPIWrite 07ad,18,0,7
SPIWrite 07ae,10,0,7
SPIWrite 07af,fb,0,7
SPIWrite 07b0,02,0,7
SPIWrite 07b1,33,0,7
SPIWrite 07b2,91,0,7
SPIWrite 07b3,f8,0,7
SPIWrite 07b4,b8,0,7
SPIWrite 07b5,21,0,7
SPIWrite 07b6,5c,0,7
SPIWrite 07b7,68,0,7
SPIWrite 07b8,c2,0,7
SPIWrite 07b9,f1,0,7
SPIWrite 07ba,01,0,7
SPIWrite 07bb,02,0,7
SPIWrite 07bc,84,0,7
SPIWrite 07bd,f8,0,7
SPIWrite 07be,70,0,7
SPIWrite 07bf,27,0,7
SPIWrite 07c0,9a,0,7
SPIWrite 07c1,68,0,7
SPIWrite 07c2,91,0,7
SPIWrite 07c3,f8,0,7
SPIWrite 07c4,b8,0,7
SPIWrite 07c5,11,0,7
SPIWrite 07c6,c1,0,7
SPIWrite 07c7,f1,0,7
SPIWrite 07c8,01,0,7
SPIWrite 07c9,01,0,7
SPIWrite 07ca,82,0,7
SPIWrite 07cb,f8,0,7
SPIWrite 07cc,70,0,7
SPIWrite 07cd,17,0,7
SPIWrite 07ce,dd,0,7
SPIWrite 07cf,f7,0,7
SPIWrite 07d0,3a,0,7
SPIWrite 07d1,fa,0,7
SPIWrite 07d2,10,0,7
SPIWrite 07d3,bd,0,7
```

```
SPIWrite 07d4,b4,0,7
SPIWrite 07d5,01,0,7
SPIWrite 07d6,01,0,7
SPIWrite 07d7,20,0,7
SPIWrite 07d8,a8,0,7
SPIWrite 07d9,75,0,7
SPIWrite 07da,02,0,7
SPIWrite 07db,00,0,7
SPIWrite 07dc,08,0,7
SPIWrite 07dd,b5,0,7
SPIWrite 07de,eb,0,7
SPIWrite 07df,f7,0,7
SPIWrite 07e0,d7,0,7
SPIWrite 07e1,fa,0,7
SPIWrite 07e2,4f,0,7
SPIWrite 07e3,f4,0,7
SPIWrite 07e4,11,0,7
SPIWrite 07e5,60,0,7
SPIWrite 07e6,00,0,7
SPIWrite 07e7,78,0,7
SPIWrite 07e8,08,0,7
SPIWrite 07e9,bd,0,7
SPIWrite 07ea,38,0,7
SPIWrite 07eb,b5,0,7
SPIWrite 07ec,04,0,7
SPIWrite 07ed,4d,0,7
SPIWrite 07ee,05,0,7
SPIWrite 07ef,4c,0,7
SPIWrite 07f0,05,0,7
SPIWrite 07f1,4b,0,7
SPIWrite 07f2,2d,0,7
SPIWrite 07f3,78,0,7
SPIWrite 07f4,24,0,7
SPIWrite 07f5,78,0,7
SPIWrite 07f6,1b,0,7
SPIWrite 07f7,78,0,7
SPIWrite 07f8,eb,0,7
SPIWrite 07f9,f7,0,7
SPIWrite 07fa,12,0,7
SPIWrite 07fb,fb,0,7
SPIWrite 07fc,38,0,7
SPIWrite 07fd,bd,0,7
SPIWrite 07fe,c0,0,7
SPIWrite 07ff,46,0,7
SPIWrite 0800,20,0,7
SPIWrite 0801,00,0,7
SPIWrite 0802,00,0,7
SPIWrite 0803,64,0,7
SPIWrite 0804,20,0,7
SPIWrite 0805,00,0,7
SPIWrite 0806,00,0,7
SPIWrite 0807,54,0,7
```

```
SPIWrite 0808,20,0,7
SPIWrite 0809,00,0,7
SPIWrite 080a,00,0,7
SPIWrite 080b,74,0,7
SPIWrite 080c,38,0,7
SPIWrite 080d,b5,0,7
SPIWrite 080e,05,0,7
SPIWrite 080f,4d,0,7
SPIWrite 0810,00,0,7
SPIWrite 0811,24,0,7
SPIWrite 0812,28,0,7
SPIWrite 0813,68,0,7
SPIWrite 0814,01,0,7
SPIWrite 0815,46,0,7
SPIWrite 0816,20,0,7
SPIWrite 0817,46,0,7
SPIWrite 0818,88,0,7
SPIWrite 0819,47,0,7
SPIWrite 081a,64,0,7
SPIWrite 081b,1c,0,7
SPIWrite 081c,04,0,7
SPIWrite 081d,2c,0,7
SPIWrite 081e,f8,0,7
SPIWrite 081f,db,0,7
SPIWrite 0018,00,0,7  //Property_18h_0_0=0x0;
     Address(0x18[7:0])
SPIWrite 0018,20,0,7  //macro=0x1;    Address(0x18[7:5])
SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,08,0,7  //MACRO_OPERAND_REG0=0x8000000;
     Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00,0,7
SPIWrite 00a1,00,0,7
SPIWrite 00a0,00,0,7
SPIWrite 00a7,00,0,7  //MACRO_OPERAND_REG1=0x1800;
     Address(0xa4[7:0],0xa5[7:0],0xa6[7:0],0xa7[7:0],0xa8[7:0])
SPIWrite 00a6,00,0,7
SPIWrite 00a5,18,0,7
SPIWrite 00a4,00,0,7
SPIWrite 0193,78,0,7  //MACRO_OPCODE=0x78;
     Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])
```

```
SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
      Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
      Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIWrite 0144,00,0,7  //Property_124h_4_2=0x0;
      Address(0x144[7:2])
SPIWrite 0018,00,0,7  //macro=0x0;     Address(0x18[7:5])
SPIWrite 0018,01,0,7  //Property_18h_0_0=0x1;
      Address(0x18[7:0])
SPIWrite 0020,38,0,7
SPIWrite 0021,bd,0,7
SPIWrite 0022,c0,0,7
SPIWrite 0023,46,0,7
```

```
SPIWrite 0024,ec,0,7
SPIWrite 0025,de,0,7
SPIWrite 0026,00,0,7
SPIWrite 0027,20,0,7
SPIWrite 0028,70,0,7
SPIWrite 0029,47,0,7
SPIWrite 002a,03,0,7
SPIWrite 002b,48,0,7
SPIWrite 002c,00,0,7
SPIWrite 002d,78,0,7
SPIWrite 002e,08,0,7
SPIWrite 002f,b9,0,7
SPIWrite 0030,ee,0,7
SPIWrite 0031,f7,0,7
SPIWrite 0032,da,0,7
SPIWrite 0033,bf,0,7
SPIWrite 0034,70,0,7
SPIWrite 0035,47,0,7
SPIWrite 0036,c0,0,7
SPIWrite 0037,46,0,7
SPIWrite 0038,a1,0,7
SPIWrite 0039,13,0,7
SPIWrite 003a,01,0,7
SPIWrite 003b,20,0,7
SPIWrite 003c,03,0,7
SPIWrite 003d,48,0,7
SPIWrite 003e,08,0,7
SPIWrite 003f,21,0,7
SPIWrite 0040,41,0,7
SPIWrite 0041,76,0,7
SPIWrite 0042,09,0,7
SPIWrite 0043,21,0,7
SPIWrite 0044,c1,0,7
SPIWrite 0045,76,0,7
SPIWrite 0046,41,0,7
SPIWrite 0047,77,0,7
SPIWrite 0048,70,0,7
SPIWrite 0049,47,0,7
SPIWrite 004a,c0,0,7
SPIWrite 004b,46,0,7
SPIWrite 004c,88,0,7
SPIWrite 004d,18,0,7
SPIWrite 004e,01,0,7
SPIWrite 004f,20,0,7
SPIWrite 0050,00,0,7
SPIWrite 0051,04,0,7
SPIWrite 0052,07,0,7
SPIWrite 0053,07,0,7
SPIWrite 0054,00,0,7
SPIWrite 0055,00,0,7
SPIWrite 0056,03,0,7
SPIWrite 0057,07,0,7
```

```
SPIWrite 0058,00,0,7
SPIWrite 0059,00,0,7
SPIWrite 005a,00,0,7
SPIWrite 005b,07,0,7
SPIWrite 005c,00,0,7
SPIWrite 005d,05,0,7
SPIWrite 005e,05,0,7
SPIWrite 005f,07,0,7
SPIWrite 0060,07,0,7
SPIWrite 0061,00,0,7
SPIWrite 0062,0a,0,7
SPIWrite 0063,0c,0,7
SPIWrite 0064,0a,0,7
SPIWrite 0065,16,0,7
SPIWrite 0066,14,0,7
SPIWrite 0067,16,0,7
SPIWrite 0068,14,0,7
SPIWrite 0069,00,0,7
SPIWrite 006a,16,0,7
SPIWrite 006b,00,0,7
SPIWrite 006c,16,0,7
SPIWrite 006d,16,0,7
SPIWrite 006e,14,0,7
SPIWrite 006f,16,0,7
SPIWrite 0070,14,0,7
SPIWrite 0071,00,0,7
SPIWrite 0072,00,0,7
SPIWrite 0073,00,0,7
SPIWrite 0074,00,0,7
SPIWrite 0075,16,0,7
SPIWrite 0076,14,0,7
SPIWrite 0077,16,0,7
SPIWrite 0078,14,0,7
SPIWrite 0079,00,0,7
SPIWrite 007a,15,0,7
SPIWrite 007b,00,0,7
SPIWrite 007c,00,0,7
SPIWrite 007d,00,0,7
SPIWrite 007e,00,0,7
SPIWrite 007f,00,0,7
SPIWrite 0080,00,0,7
SPIWrite 0081,01,0,7
SPIWrite 0082,02,0,7
SPIWrite 0083,01,0,7
SPIWrite 0084,10,0,7
SPIWrite 0085,0a,0,7
SPIWrite 0086,10,0,7
SPIWrite 0087,00,0,7
SPIWrite 0088,00,0,7
SPIWrite 0089,00,0,7
SPIWrite 008a,00,0,7
SPIWrite 008b,00,0,7
```

```
SPIWrite 008c,00,0,7
SPIWrite 008d,00,0,7
SPIWrite 008e,00,0,7
SPIWrite 008f,06,0,7
SPIWrite 0090,02,0,7
SPIWrite 0091,01,0,7
SPIWrite 0092,10,0,7
SPIWrite 0093,0a,0,7
SPIWrite 0094,10,0,7
SPIWrite 0095,00,0,7
SPIWrite 0096,07,0,7
SPIWrite 0097,00,0,7
SPIWrite 0098,01,0,7
SPIWrite 0099,00,0,7
SPIWrite 009a,0a,0,7
SPIWrite 009b,00,0,7
SPIWrite 009c,00,0,7
SPIWrite 009d,16,0,7
SPIWrite 009e,00,0,7
SPIWrite 009f,00,0,7
SPIWrite 00a0,00,0,7
SPIWrite 00a1,0a,0,7
SPIWrite 00a2,00,0,7
SPIWrite 00a3,00,0,7
SPIWrite 00a4,01,0,7
SPIWrite 00a5,10,0,7
SPIWrite 00a6,01,0,7
SPIWrite 00a7,10,0,7
SPIWrite 00a8,0a,0,7
SPIWrite 00a9,00,0,7
SPIWrite 00aa,00,0,7
SPIWrite 00ab,07,0,7
SPIWrite 00ac,10,0,7
SPIWrite 00ad,01,0,7
SPIWrite 00ae,0f,0,7
SPIWrite 00af,0a,0,7
SPIWrite 00b0,00,0,7
SPIWrite 00b1,00,0,7
SPIWrite 00b2,00,0,7
SPIWrite 00b3,00,0,7
SPIWrite 00b4,08,0,7
SPIWrite 00b5,00,0,7
SPIWrite 00b6,00,0,7
SPIWrite 00b7,00,0,7
SPIWrite 00b8,00,0,7
SPIWrite 00b9,01,0,7
SPIWrite 00ba,10,0,7
SPIWrite 00bb,0a,0,7
SPIWrite 00bc,00,0,7
SPIWrite 00bd,00,0,7
SPIWrite 00be,00,0,7
SPIWrite 00bf,00,0,7
```

```
SPIWrite 00c0,00,0,7
SPIWrite 00c1,02,0,7
SPIWrite 00c2,00,0,7
SPIWrite 00c3,00,0,7
SPIWrite 00c4,00,0,7
SPIWrite 00c5,00,0,7
SPIWrite 00c6,00,0,7
SPIWrite 00c7,00,0,7
SPIWrite 00c8,00,0,7
SPIWrite 00c9,00,0,7
SPIWrite 00ca,00,0,7
SPIWrite 00cb,00,0,7
SPIWrite 00cc,00,0,7
SPIWrite 00cd,00,0,7
SPIWrite 00ce,00,0,7
SPIWrite 00cf,00,0,7
SPIWrite 00d0,00,0,7
SPIWrite 00d1,00,0,7
SPIWrite 00d2,00,0,7
SPIWrite 00d3,00,0,7
SPIWrite 00d4,00,0,7
SPIWrite 00d5,00,0,7
SPIWrite 00d6,11,0,7
SPIWrite 00d7,00,0,7
SPIWrite 00d8,00,0,7
SPIWrite 00d9,00,0,7
SPIWrite 00da,00,0,7
SPIWrite 00db,00,0,7
SPIWrite 00dc,01,0,7
SPIWrite 00dd,16,0,7
SPIWrite 00de,01,0,7
SPIWrite 00df,10,0,7
SPIWrite 00e0,0a,0,7
SPIWrite 00e1,10,0,7
SPIWrite 00e2,00,0,7
SPIWrite 00e3,01,0,7
SPIWrite 00e4,03,0,7
SPIWrite 00e5,01,0,7
SPIWrite 00e6,10,0,7
SPIWrite 00e7,0a,0,7
SPIWrite 00e8,10,0,7
SPIWrite 00e9,00,0,7
SPIWrite 00ea,00,0,7
SPIWrite 00eb,12,0,7
SPIWrite 00ec,01,0,7
SPIWrite 00ed,10,0,7
SPIWrite 00ee,0a,0,7
SPIWrite 00ef,00,0,7
SPIWrite 00f0,00,0,7
SPIWrite 00f1,00,0,7
SPIWrite 00f2,11,0,7
SPIWrite 00f3,01,0,7
```

```
SPIWrite 00f4,10,0,7
SPIWrite 00f5,0a,0,7
SPIWrite 00f6,00,0,7
SPIWrite 00f7,00,0,7
SPIWrite 00f8,01,0,7
SPIWrite 00f9,10,0,7
SPIWrite 00fa,01,0,7
SPIWrite 00fb,0e,0,7
SPIWrite 00fc,0a,0,7
SPIWrite 00fd,00,0,7
SPIWrite 00fe,00,0,7
SPIWrite 00ff,01,0,7
SPIWrite 0100,0f,0,7
SPIWrite 0101,0a,0,7
SPIWrite 0102,00,0,7
SPIWrite 0103,00,0,7
SPIWrite 0104,00,0,7
SPIWrite 0105,00,0,7
SPIWrite 0106,00,0,7
SPIWrite 0107,00,0,7
SPIWrite 0108,00,0,7
SPIWrite 0109,00,0,7
SPIWrite 010a,00,0,7
SPIWrite 010b,00,0,7
SPIWrite 010c,00,0,7
SPIWrite 010d,00,0,7
SPIWrite 010e,00,0,7
SPIWrite 010f,00,0,7
SPIWrite 0110,00,0,7
SPIWrite 0111,00,0,7
SPIWrite 0112,00,0,7
SPIWrite 0113,00,0,7
SPIWrite 0114,00,0,7
SPIWrite 0115,00,0,7
SPIWrite 0116,00,0,7
SPIWrite 0117,00,0,7
SPIWrite 0118,00,0,7
SPIWrite 0119,00,0,7
SPIWrite 011a,00,0,7
SPIWrite 011b,00,0,7
SPIWrite 011c,03,0,7
SPIWrite 011d,00,0,7
SPIWrite 011e,00,0,7
SPIWrite 011f,00,0,7
SPIWrite 0120,00,0,7
SPIWrite 0121,00,0,7
SPIWrite 0122,00,0,7
SPIWrite 0123,00,0,7
SPIWrite 0124,00,0,7
SPIWrite 0125,00,0,7
SPIWrite 0126,00,0,7
SPIWrite 0127,00,0,7
```

```
SPIWrite 0128,00,0,7
SPIWrite 0129,07,0,7
SPIWrite 012a,00,0,7
SPIWrite 012b,00,0,7
SPIWrite 012c,00,0,7
SPIWrite 012d,00,0,7
SPIWrite 012e,00,0,7
SPIWrite 012f,00,0,7
SPIWrite 0130,01,0,7
SPIWrite 0131,03,0,7
SPIWrite 0132,01,0,7
SPIWrite 0133,10,0,7
SPIWrite 0134,0a,0,7
SPIWrite 0135,10,0,7
SPIWrite 0136,00,0,7
SPIWrite 0137,09,0,7
SPIWrite 0138,02,0,7
SPIWrite 0139,01,0,7
SPIWrite 013a,10,0,7
SPIWrite 013b,0a,0,7
SPIWrite 013c,10,0,7
SPIWrite 013d,00,0,7
SPIWrite 013e,07,0,7
SPIWrite 013f,00,0,7
SPIWrite 0140,01,0,7
SPIWrite 0141,00,0,7
SPIWrite 0142,0a,0,7
SPIWrite 0143,00,0,7
SPIWrite 0144,00,0,7
SPIWrite 0145,01,0,7
SPIWrite 0146,10,0,7
SPIWrite 0147,0a,0,7
SPIWrite 0148,10,0,7
SPIWrite 0149,0a,0,7
SPIWrite 014a,00,0,7
SPIWrite 014b,00,0,7
SPIWrite 014c,00,0,7
SPIWrite 014d,00,0,7
SPIWrite 014e,00,0,7
SPIWrite 014f,00,0,7
SPIWrite 0150,00,0,7
SPIWrite 0151,02,0,7
SPIWrite 0152,00,0,7
SPIWrite 0153,02,0,7
SPIWrite 0154,06,0,7
SPIWrite 0155,00,0,7
SPIWrite 0156,00,0,7
SPIWrite 0157,00,0,7
SPIWrite 0158,00,0,7
SPIWrite 0159,00,0,7
SPIWrite 015a,00,0,7
SPIWrite 015b,00,0,7
```

```
SPIWrite 015c,00,0,7
SPIWrite 015d,02,0,7
SPIWrite 015e,06,0,7
SPIWrite 015f,00,0,7
SPIWrite 0160,00,0,7
SPIWrite 0161,00,0,7
SPIWrite 0162,00,0,7
SPIWrite 0163,00,0,7
SPIWrite 0164,00,0,7
SPIWrite 0165,00,0,7
SPIWrite 0166,00,0,7
SPIWrite 0167,00,0,7
SPIWrite 0168,06,0,7
SPIWrite 0169,00,0,7
SPIWrite 016a,00,0,7
SPIWrite 016b,00,0,7
SPIWrite 016c,7c,0,7
SPIWrite 016d,1c,0,7
SPIWrite 016e,01,0,7
SPIWrite 016f,20,0,7
SPIWrite 0170,d1,0,7
SPIWrite 0171,1e,0,7
SPIWrite 0172,01,0,7
SPIWrite 0173,20,0,7
SPIWrite 0174,84,0,7
SPIWrite 0175,1a,0,7
SPIWrite 0176,01,0,7
SPIWrite 0177,20,0,7
SPIWrite 0178,26,0,7
SPIWrite 0179,07,0,7
SPIWrite 017a,01,0,7
SPIWrite 017b,20,0,7
SPIWrite 017c,4a,0,7
SPIWrite 017d,0c,0,7
SPIWrite 017e,01,0,7
SPIWrite 017f,20,0,7
SPIWrite 0180,30,0,7
SPIWrite 0181,20,0,7
SPIWrite 0182,03,0,7
SPIWrite 0183,00,0,7
SPIWrite 0184,3c,0,7
SPIWrite 0185,20,0,7
SPIWrite 0186,03,0,7
SPIWrite 0187,00,0,7
SPIWrite 0188,41,0,7
SPIWrite 0189,20,0,7
SPIWrite 018a,03,0,7
SPIWrite 018b,00,0,7
SPIWrite 018c,59,0,7
SPIWrite 018d,20,0,7
SPIWrite 018e,03,0,7
SPIWrite 018f,00,0,7
```

```
SPIWrite 0190,fb,0,7
SPIWrite 0191,20,0,7
SPIWrite 0192,01,0,7
SPIWrite 0193,20,0,7
SPIWrite 0194,00,0,7
SPIWrite 0195,20,0,7
SPIWrite 0196,01,0,7
SPIWrite 0197,20,0,7
SPIWrite 0198,0c,0,7
SPIWrite 0199,20,0,7
SPIWrite 019a,01,0,7
SPIWrite 019b,20,0,7
SPIWrite 019c,11,0,7
SPIWrite 019d,20,0,7
SPIWrite 019e,01,0,7
SPIWrite 019f,20,0,7
SPIWrite 01a0,29,0,7
SPIWrite 01a1,20,0,7
SPIWrite 01a2,01,0,7
SPIWrite 01a3,20,0,7
SPIWrite 01a4,93,0,7
SPIWrite 01a5,21,0,7
SPIWrite 01a6,01,0,7
SPIWrite 01a7,20,0,7
SPIWrite 01a8,00,0,7
SPIWrite 0018,00,0,7  //Property_18h_0_0=0x0;
     Address(0x18[7:0])
SPIWrite 0018,20,0,7  //macro=0x1;    Address(0x18[7:5])
SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,01,0,7  //MACRO_OPERAND_REG0=0x1890000;
     Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,89,0,7
SPIWrite 00a1,00,0,7
SPIWrite 00a0,00,0,7
SPIWrite 00a7,00,0,7  //MACRO_OPERAND_REG1=0x2000;
     Address(0xa4[7:0],0xa5[7:0],0xa6[7:0],0xa7[7:0],0xa8[7:0])
SPIWrite 00a6,00,0,7
SPIWrite 00a5,20,0,7
SPIWrite 00a4,00,0,7
SPIWrite 0193,78,0,7  //MACRO_OPCODE=0x78;
     Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])
```

```
SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
      Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
      Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0x1;
```

```
     Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00,0,7
SPIWrite 00a1,00,0,7
SPIWrite 00a0,01,0,7
SPIWrite 0193,78,0,7  //MACRO_OPCODE=0x78;
     Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1; Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
     Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0; Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
     Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
     Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7
```

```
//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
     Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0x3;
     Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00,0,7
SPIWrite 00a1,00,0,7
SPIWrite 00a0,03,0,7
SPIWrite 0193,01,0,7  //MACRO_OPCODE=0x1;
     Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
     Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
     Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])
```

```
SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00fb,0,7
SPIRead 00fa,0,7
SPIRead 00f9,0,7
SPIRead 00f8,0,7

//Read     MACRO_RESULT_REG0=0x14071600;
      Address(0xf8[7:0],0xf9[7:0],0xfa[7:0],0xfb[7:0],0xfc[7:0])

SPIRead 00ff,0,7
SPIRead 00fe,0,7
SPIRead 00fd,0,7
SPIRead 00fc,0,7

//Read     MACRO_RESULT_REG1=0xa2;
      Address(0xfc[7:0],0xfd[7:0],0xfe[7:0],0xff[7:0],0x100[7:0])

SPIWrite 0018,00,0,7  //macro=0x0;     Address(0x18[7:5])

//STEP: pllEfuse/step0

//START: Enabling Temp Sense

SPIWrite 0015,02,0,7  //ana_4t4r=0x1;  Address(0x15[7:1])
SPIWrite 00c0,80,0,7  //Property_a0h_7_7=0x1;
      Address(0xc0[7:7])
SPIWrite 0015,00,0,7  //ana_4t4r=0x0;  Address(0x15[7:1])
SPIWrite 0015,40,0,7  //digtop=0x1;    Address(0x15[7:6])
SPIWrite 02a3,00,0,7  //Property_280h_31_0=0x7e;
      Address(0x2a0[7:0],0x2a1[7:0],0x2a2[7:0],0x2a3[7:0],0x2a4[7:
0])
SPIWrite 02a2,00,0,7
SPIWrite 02a1,00,0,7
SPIWrite 02a0,7e,0,7
SPIWrite 02a7,01,0,7  //Property_284h_31_0=0x1000000;
      Address(0x2a4[7:0],0x2a5[7:0],0x2a6[7:0],0x2a7[7:0],0x2a8[7:
0])
SPIWrite 02a6,00,0,7
SPIWrite 02a5,00,0,7
```

```
SPIWrite 02a4,00,0,7

//END: Enabling Temp Sense


//START: Loading PLL EFuse trims

SPIWrite 0015,00,0,7  //digtop=0x0;    Address(0x15[7:6])
SPIWrite 0018,20,0,7  //macro=0x1;     Address(0x18[7:5])
SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0x22f;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00,0,7
SPIWrite 00a1,02,0,7
SPIWrite 00a0,2f,0,7
SPIWrite 0193,33,0,7  //MACRO_OPCODE=0x33;
      Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
      Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
      Address(0xf0[7:5])

SPIRead 00f0,6,6
```

```
//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0x10f;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00,0,7
SPIWrite 00a1,01,0,7
SPIWrite 00a0,0f,0,7
SPIWrite 0193,34,0,7  //MACRO_OPCODE=0x34;
      Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
      Address(0xf1[7:0],0xf2[7:0])
```

```
SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0; Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
      Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0x1;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00,0,7
SPIWrite 00a1,00,0,7
SPIWrite 00a0,01,0,7
SPIWrite 0193,72,0,7  //MACRO_OPCODE=0x72;
      Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1; Address(0xf0[7:2])
```

```
SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
      Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
      Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0xe0100;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,0e,0,7
```

```
SPIWrite 00a1,01,0,7
SPIWrite 00a0,00,0,7
SPIWrite 0193,71,0,7  //MACRO_OPCODE=0x71;
     Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
     Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
     Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
     Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
     Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
```

```
//END: Done Loading PLL EFuse trims

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0x10101;
     Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,01,0,7
SPIWrite 00a1,01,0,7
SPIWrite 00a0,01,0,7
SPIWrite 0193,73,0,7  //MACRO_OPCODE=0x73;
     Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
     Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
     Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])
```

```
SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIWrite 0018,00,0,7  //macro=0x0;     Address(0x18[7:5])
SPIWrite 0012,01,0,7  //rxdig=0x1;     Address(0x12[7:0])
SPIWrite 0761,0a,0,7  //Property_740h_13_12=0x0;
      Address(0x761[7:4])
SPIWrite 0012,02,0,7  //rxdig=0x2;     Address(0x12[7:0])
SPIWrite 0761,0a,0,7  //Property_740h_13_12=0x0;
      Address(0x761[7:4])
SPIWrite 0012,04,0,7  //rxdig=0x4;     Address(0x12[7:0])
SPIWrite 0761,0a,0,7  //Property_740h_13_12=0x0;
      Address(0x761[7:4])
SPIWrite 0012,08,0,7  //rxdig=0x8;     Address(0x12[7:0])
SPIWrite 0761,0a,0,7  //Property_740h_13_12=0x0;
      Address(0x761[7:4])
SPIWrite 0012,00,0,7  //rxdig=0x0;     Address(0x12[7:0])

//STEP: pllConfig/step0

//START: Configuring PLL

SPIWrite 0015,08,0,7  //rx=0x2;  Address(0x15[7:2])
SPIWrite 0043,00,0,7  //Property_20h_31_0=0x0;
      Address(0x40[7:0],0x41[7:0],0x42[7:0],0x43[7:0],0x44[7:0])
SPIWrite 0042,00,0,7
SPIWrite 0041,00,0,7
SPIWrite 0040,00,0,7
SPIWrite 0015,00,0,7  //rx=0x0;  Address(0x15[7:2])
SPIWrite 0015,02,0,7  //ana_4t4r=0x1; Address(0x15[7:1])
SPIWrite 00c1,60,0,7  //Property_a0h_15_13=0x3;
      Address(0xc1[7:5])

//START: Requesting/releasing SPI Access to PLL Pages

SPIWrite 0015,00,0,7  //ana_4t4r=0x0; Address(0x15[7:1])
SPIWrite 0015,40,0,7  //digtop=0x1;   Address(0x15[7:6])
SPIWrite 0170,01,0,7  //pll_reg_spi_req_a=0x1;
      Address(0x170[7:0])
SPIWrite 0540,00,0,7  //Property_520h_0_0=0x0;
```

```
      Address(0x540[7:0])

SPIPoll 0171,0,0,01
SPIRead 0171,0,0

//Read     pll_reg_spi_a_ack=0x1(Meaning: );;
      Address(0x171[7:0])


//END: Requesting/releasing SPI Access to PLL Pages

SPIWrite 0015,00,0,7  //digtop=0x0;    Address(0x15[7:6])
SPIWrite 0015,01,0,7  //pll=0x1;       Address(0x15[7:0])
SPIWrite 003f,08,0,7  //Property_1ch_27_27=0x1;
      Address(0x3f[7:3])
SPIWrite 0028,01,0,7  //Property_8h_0_0=0x1;
      Address(0x28[7:0])
SPIWrite 0035,10,0,7  //Property_14h_12_12=0x1;
      Address(0x35[7:4])
SPIWrite 0036,40,0,7  //Property_14h_22_22=0x1;
      Address(0x36[7:6])
SPIWrite 0038,08,0,7  //Property_18h_3_3=0x1;
      Address(0x38[7:3])
SPIWrite 0039,20,0,7  //Property_18h_13_13=0x1;
      Address(0x39[7:5])
SPIWrite 003b,08,0,7  //Property_18h_27_27=0x1;
      Address(0x3b[7:3])
SPIWrite 0046,60,0,7  //Property_24h_21_21=0x1;
      Address(0x46[7:5])
SPIWrite 0046,60,0,7  //Property_24h_22_22=0x1;
      Address(0x46[7:6])
SPIWrite 0043,18,0,7  //Property_20h_28_28=0x1;
      Address(0x43[7:4])
SPIWrite 0043,18,0,7  //Property_20h_27_27=0x1;
      Address(0x43[7:3])
SPIWrite 004c,00,0,7  //Property_2ch_3_0=0x0;
      Address(0x4c[7:0])
SPIWrite 003c,e0,0,7  //Property_1ch_5_5=0x1;
      Address(0x3c[7:5])
SPIWrite 0015,00,0,7  //pll=0x0;       Address(0x15[7:0])
SPIWrite 0015,02,0,7  //ana_4t4r=0x1;  Address(0x15[7:1])
SPIWrite 010c,00,0,7  //EN_REFDIV_DMP=0x0;  Address(0x10c[7:0])
SPIWrite 0015,00,0,7  //ana_4t4r=0x0;  Address(0x15[7:1])
SPIWrite 0015,01,0,7  //pll=0x1;       Address(0x15[7:0])
SPIWrite 003c,60,0,7  //Property_1ch_7_7=0x0;
      Address(0x3c[7:7])
SPIWrite 003c,20,0,7  //Property_1ch_6_6=0x0;
      Address(0x3c[7:6])
SPIWrite 003d,00,0,7  //Property_1ch_8_8=0x0;
      Address(0x3d[7:0])
SPIWrite 0015,00,0,7  //pll=0x0;       Address(0x15[7:0])
SPIWrite 0015,02,0,7  //ana_4t4r=0x1;  Address(0x15[7:1])
```

```
SPIWrite 010d,01,0,7  //CTL_REFDIV_DIV=0x1;
     Address(0x10d[7:0])
SPIWrite 0015,00,0,7  //ana_4t4r=0x0; Address(0x15[7:1])
SPIWrite 0015,01,0,7  //pll=0x1;      Address(0x15[7:0])
SPIWrite 0056,43,0,7  //Property_34h_22_22=0x1;
     Address(0x56[7:6])
SPIWrite 0056,c3,0,7  //Property_34h_23_23=0x1;
     Address(0x56[7:7])
SPIWrite 0056,c3,0,7  //Property_34h_19_19=0x0;
     Address(0x56[7:3])
SPIWrite 0056,f3,0,7  //Property_34h_21_20=0x3;
     Address(0x56[7:4])
SPIWrite 0057,02,0,7  //Property_34h_25_25=0x1;
     Address(0x57[7:1])
SPIWrite 0015,00,0,7  //pll=0x0;      Address(0x15[7:0])
SPIWrite 0015,80,0,7  //timing_controller=0x1;
     Address(0x15[7:7])
SPIWrite 07f5,01,0,7  //Property_7d4h_15_0=0x17f;
     Address(0x7f4[7:0],0x7f5[7:0],0x7f6[7:0])
SPIWrite 07f4,7f,0,7
SPIWrite 0015,00,0,7  //timing_controller=0x0;
     Address(0x15[7:7])
SPIWrite 0015,01,0,7  //pll=0x1;      Address(0x15[7:0])
SPIWrite 006d,01,0,7  //LCMGEN_DIV=0x17f;
     Address(0x6c[7:0],0x6d[7:0],0x6e[7:0])
SPIWrite 006c,7f,0,7
SPIWrite 0062,00,0,7  //Property_40h_23_20=0x0;
     Address(0x62[7:4])
SPIWrite 0015,00,0,7  //pll=0x0;      Address(0x15[7:0])
SPIWrite 0015,02,0,7  //ana_4t4r=0x1; Address(0x15[7:1])
SPIWrite 010f,20,0,7  //CTL_FBDIV_DIV=0x20;
     Address(0x10f[7:0])
SPIWrite 010e,00,0,7  //CTL_FBDIV_DIVBY2=0x0;
     Address(0x10e[7:0])
SPIWrite 0015,00,0,7  //ana_4t4r=0x0; Address(0x15[7:1])
SPIWrite 0015,01,0,7  //pll=0x1;      Address(0x15[7:0])
SPIWrite 0050,fe,0,7  //Property_30h_2_1=0x3;
     Address(0x50[7:1])
SPIWrite 0050,fe,0,7  //Property_30h_4_3=0x3;
     Address(0x50[7:3])
SPIWrite 0050,fe,0,7  //Property_30h_6_5=0x3;
     Address(0x50[7:5])
SPIWrite 0015,00,0,7  //pll=0x0;      Address(0x15[7:0])
SPIWrite 0015,02,0,7  //ana_4t4r=0x1; Address(0x15[7:1])
SPIWrite 0110,01,0,7  //CTL_OUTDIV_MUX_TX=0x1;
     Address(0x110[7:0])
SPIWrite 0015,00,0,7  //ana_4t4r=0x0; Address(0x15[7:1])
SPIWrite 0015,01,0,7  //pll=0x1;      Address(0x15[7:0])
SPIWrite 0051,3f,0,7  //Property_30h_9_9=0x1;
     Address(0x51[7:1])
SPIWrite 0015,00,0,7  //pll=0x0;      Address(0x15[7:0])
SPIWrite 0015,02,0,7  //ana_4t4r=0x1; Address(0x15[7:1])
```

```
SPIWrite 0111,01,0,7  //CTL_OUTDIV_DIV_TX=0x1;
     Address(0x111[7:0])
SPIWrite 0015,00,0,7  //ana_4t4r=0x0; Address(0x15[7:1])
SPIWrite 0015,01,0,7  //pll=0x1;      Address(0x15[7:0])
SPIWrite 007f,00,0,7  //Property_5ch_30_30=0x0;
     Address(0x7f[7:6])
SPIWrite 0015,00,0,7  //pll=0x0;      Address(0x15[7:0])
SPIWrite 0015,02,0,7  //ana_4t4r=0x1; Address(0x15[7:1])
SPIWrite 0112,01,0,7  //CTL_OUTDIV_MUX_RX=0x1;
     Address(0x112[7:0])
SPIWrite 0015,00,0,7  //ana_4t4r=0x0; Address(0x15[7:1])
SPIWrite 0015,01,0,7  //pll=0x1;      Address(0x15[7:0])
SPIWrite 0051,3f,0,7  //Property_30h_10_10=0x1;
     Address(0x51[7:2])
SPIWrite 0015,00,0,7  //pll=0x0;      Address(0x15[7:0])
SPIWrite 0015,02,0,7  //ana_4t4r=0x1; Address(0x15[7:1])
SPIWrite 0113,03,0,7  //CTL_OUTDIV_DIV_RX=0x3;
     Address(0x113[7:0])
SPIWrite 0015,00,0,7  //ana_4t4r=0x0; Address(0x15[7:1])
SPIWrite 0015,01,0,7  //pll=0x1;      Address(0x15[7:0])
SPIWrite 007f,00,0,7  //Property_5ch_31_31=0x0;
     Address(0x7f[7:7])
SPIWrite 0015,00,0,7  //pll=0x0;      Address(0x15[7:0])
SPIWrite 0015,02,0,7  //ana_4t4r=0x1; Address(0x15[7:1])
SPIWrite 0114,01,0,7  //CTL_OUTDIV_MUX_FB=0x1;
     Address(0x114[7:0])
SPIWrite 0015,00,0,7  //ana_4t4r=0x0; Address(0x15[7:1])
SPIWrite 0015,01,0,7  //pll=0x1;      Address(0x15[7:0])
SPIWrite 0051,3f,0,7  //Property_30h_11_11=0x1;
     Address(0x51[7:3])
SPIWrite 0015,00,0,7  //pll=0x0;      Address(0x15[7:0])
SPIWrite 0015,02,0,7  //ana_4t4r=0x1; Address(0x15[7:1])
SPIWrite 0115,01,0,7  //CTL_OUTDIV_DIV_FB=0x1;
     Address(0x115[7:0])
SPIWrite 0015,00,0,7  //ana_4t4r=0x0; Address(0x15[7:1])
SPIWrite 0015,01,0,7  //pll=0x1;      Address(0x15[7:0])
SPIWrite 0051,2f,0,7  //Property_30h_12_12=0x0;
     Address(0x51[7:4])
SPIWrite 0063,01,0,7  //Property_40h_27_24=0x1;
     Address(0x63[7:0])
SPIWrite 0072,02,0,7  //Property_50h_23_16=0x2;
     Address(0x72[7:0],0x73[7:0])
SPIWrite 006f,05,0,7  //Property_4ch_31_24=0x5;
     Address(0x6f[7:0],0x70[7:0])
SPIWrite 0070,02,0,7  //Property_50h_7_0=0x2;
     Address(0x70[7:0],0x71[7:0])
SPIWrite 0071,02,0,7  //Property_50h_15_8=0x2;
     Address(0x71[7:0],0x72[7:0])
SPIWrite 006d,01,0,7  //LCMGEN_DIV=0x17f;
     Address(0x6c[7:0],0x6d[7:0],0x6e[7:0])
SPIWrite 006c,7f,0,7
SPIWrite 007c,04,0,7  //Property_5ch_6_0=0x4;
```

```
      Address(0x7c[7:0])
SPIWrite 0055,ff,0,7  //Property_34h_8_8=0x1;
      Address(0x55[7:0])
SPIWrite 0055,ff,0,7  //Property_34h_15_15=0x1;
      Address(0x55[7:7])
SPIWrite 0055,ff,0,7  //Property_34h_9_9=0x1;
      Address(0x55[7:1])
SPIWrite 0055,ff,0,7  //Property_34h_13_10=0xf;
      Address(0x55[7:2])
SPIWrite 0055,ff,0,7  //Property_34h_14_14=0x1;
      Address(0x55[7:6])
SPIWrite 0059,01,0,7  //Property_38h_8_8=0x1;
      Address(0x59[7:0])
SPIWrite 0058,00,0,7  //Property_38h_7_7=0x0;
      Address(0x58[7:7])
SPIWrite 0059,01,0,7  //Property_38h_10_10=0x0;
      Address(0x59[7:2])
SPIWrite 0059,01,0,7  //Property_38h_11_11=0x0;
      Address(0x59[7:3])
SPIWrite 005c,00,0,7  //Property_3ch_7_3=0x0;
      Address(0x5c[7:3])
SPIWrite 005d,04,0,7  //Property_3ch_10_9=0x2;
      Address(0x5d[7:1])
SPIWrite 005d,0c,0,7  //Property_3ch_11_11=0x1;
      Address(0x5d[7:3])
SPIWrite 003d,01,0,7  //Property_1ch_8_8=0x1;
      Address(0x3d[7:0])
SPIWrite 0053,03,0,7  //Property_30h_25_24=0x3;
      Address(0x53[7:0])
SPIWrite 003e,0c,0,7  //Property_1ch_19_18=0x3;
      Address(0x3e[7:2])
SPIWrite 0065,6a,0,7  //Property_44h_14_14=0x1;
      Address(0x65[7:6])
SPIWrite 004e,01,0,7  //Property_2ch_16_16=0x1;
      Address(0x4e[7:0])
SPIWrite 0052,00,0,7  //Property_30h_22_21=0x0;
      Address(0x52[7:5])
SPIWrite 0065,62,0,7  //Property_44h_11_10=0x0;
      Address(0x65[7:2])
SPIWrite 0052,00,0,7  //Property_30h_16_16=0x0;
      Address(0x52[7:0])
SPIWrite 0052,00,0,7  //Property_30h_20_20=0x0;
      Address(0x52[7:4])
SPIWrite 0053,03,0,7  //Property_30h_27_26=0x0;
      Address(0x53[7:2])
SPIWrite 005e,00,0,7  //Property_3ch_18_17=0x0;
      Address(0x5e[7:1])
SPIWrite 0052,00,0,7  //Property_30h_19_19=0x0;
      Address(0x52[7:3])
SPIWrite 0052,00,0,7  //Property_30h_23_23=0x0;
      Address(0x52[7:7])
SPIWrite 003e,0c,0,7  //Property_1ch_20_20_1ch_25_25=0x0;
```

```
      Address(0x3e[7:4],0x3f[7:1])
SPIWrite 003f,08,0,7
SPIWrite 0065,60,0,7  //Property_44h_9_8=0x0;
      Address(0x65[7:0])
SPIWrite 0087,00,0,7  //Property_64h_30_29=0x0;
      Address(0x87[7:5])
SPIWrite 005e,00,0,7  //Property_3ch_20_19=0x0;
      Address(0x5e[7:3])
SPIWrite 0087,00,0,7  //Property_64h_26_25=0x0;
      Address(0x87[7:1])
SPIWrite 0087,00,0,7  //Property_64h_28_27=0x0;
      Address(0x87[7:3])
SPIWrite 003e,0c,0,7  //Property_1ch_17_16=0x0;
      Address(0x3e[7:0])
SPIWrite 0051,2f,0,7  //Property_30h_15_14=0x0;
      Address(0x51[7:6])
SPIWrite 0052,00,0,7  //Property_30h_18_17=0x0;
      Address(0x52[7:1])
SPIWrite 0065,40,0,7  //Property_44h_13_12=0x0;
      Address(0x65[7:4])
SPIWrite 0084,10,0,7  //Property_64h_5_4=0x1;
      Address(0x84[7:4])
SPIWrite 0084,90,0,7  //Property_64h_7_6=0x2;
      Address(0x84[7:6])
SPIWrite 0069,47,0,7  //Property_48h_15_8=0x47;
      Address(0x69[7:0],0x6a[7:0])
SPIWrite 0045,20,0,7  //Property_24h_13_13=0x1;
      Address(0x45[7:5])
SPIWrite 0032,00,0,7  //Property_10h_19_18=0x0;
      Address(0x32[7:2])
SPIWrite 0049,38,0,7  //Property_28h_13_11=0x7;
      Address(0x49[7:3])
SPIWrite 0049,3d,0,7  //Property_28h_10_8=0x5;
      Address(0x49[7:0])
SPIWrite 004a,00,0,7  //Property_28h_21_19=0x0;
      Address(0x4a[7:3])
SPIWrite 004b,00,0,7  //Property_28h_30_28=0x0;
      Address(0x4b[7:4])
SPIWrite 004d,c0,0,7  //Property_2ch_9_8=0x0;
      Address(0x4d[7:0])
SPIWrite 004a,04,0,7  //Property_28h_18_16=0x4;
      Address(0x4a[7:0])
SPIWrite 004b,0f,0,7  //Property_28h_27_24=0xf;
      Address(0x4b[7:0])
SPIWrite 004b,3f,0,7  //Property_28h_30_28=0x3;
      Address(0x4b[7:4])
SPIWrite 0051,2f,0,7  //Property_30h_8_8=0x1;
      Address(0x51[7:0])
SPIWrite 0040,80,0,7  //Property_20h_7_5=0x4;
      Address(0x40[7:5])
SPIWrite 0041,00,0,7  //Property_20h_10_9=0x0;
      Address(0x41[7:1])
```

```
SPIWrite 0043,f8,0,7  //Property_20h_31_29=0x7;
     Address(0x43[7:5])
SPIWrite 0075,08,0,7  //Property_54h_12_11=0x1;
     Address(0x75[7:3])
SPIWrite 0075,0e,0,7  //Property_54h_10_8=0x6;
     Address(0x75[7:0])
SPIWrite 0045,24,0,7  //Property_24h_11_8=0x4;
     Address(0x45[7:0])
SPIWrite 0031,40,0,7  //Property_10h_15_14=0x1;
     Address(0x31[7:6])
SPIWrite 0046,63,0,7  //Property_24h_17_16=0x3;
     Address(0x46[7:0])
SPIWrite 0045,24,0,7  //Property_24h_15_14=0x0;
     Address(0x45[7:6])
SPIWrite 0064,07,0,7  //Property_44h_4_0=0x7;
     Address(0x64[7:0])
SPIWrite 0073,20,0,7  //Property_50h_29_29=0x1;
     Address(0x73[7:5])
SPIWrite 0056,f1,0,7  //Property_34h_17_17=0x0;
     Address(0x56[7:1])
SPIWrite 0058,00,0,7  //Property_38h_2_2=0x0;
     Address(0x58[7:2])
SPIWrite 0062,00,0,7  //Property_40h_23_20=0x0;
     Address(0x62[7:4])
SPIWrite 0066,00,0,7  //Property_44h_16_16=0x0;
     Address(0x66[7:0])
SPIWrite 0066,01,0,7  //Property_44h_16_16=0x1;
     Address(0x66[7:0])

WAIT 0.005
SPIWrite 0066,03,0,7  //Property_44h_17_17=0x1;
     Address(0x66[7:1])

WAIT 0.005
SPIWrite 0063,41,0,7  //CLR_FLAG_LOCK_LOST=0x1;
     Address(0x63[7:6])
SPIWrite 0063,01,0,7  //CLR_FLAG_LOCK_LOST=0x0;
     Address(0x63[7:6])

WAIT 0.005
SPIRead 0066,5,5

//Read     LOCK_OUT_STICKY=0x1;  Address(0x66[7:5])

SPIRead 0066,6,6

//Read     LOCK_LOST_STICKY=0x0;      Address(0x66[7:6])

SPIReadCheck 0066,4,4,10

//Read     LOCK=0x1;  Address(0x66[7:4])
```

```
SPIReadCheck 0066,6,6,00

//Read     LOCK_LOST_STICKY=0x0;       Address(0x66[7:6])

SPIWrite 0066,31,0,7  //Property_44h_17_17=0x0;
      Address(0x66[7:1])
SPIWrite 0063,81,0,7  //CLR_FLAG_LOCK_OUT=0x1;
      Address(0x63[7:7])
SPIWrite 0063,c1,0,7  //CLR_FLAG_LOCK_LOST=0x1;
      Address(0x63[7:6])
SPIWrite 0063,c2,0,7  //Property_40h_27_24=0x2;
      Address(0x63[7:0])

//START: Sending Sysref to device

SPIWrite 0015,00,0,7  //pll=0x0;       Address(0x15[7:0])
SPIWrite 0015,80,0,7  //timing_controller=0x1;
      Address(0x15[7:7])
SPIWrite 085b,00,0,7  //Property_838h_31_0=0x0;
      Address(0x858[7:0],0x859[7:0],0x85a[7:0],0x85b[7:0],0x85c[7:
0])
SPIWrite 085a,00,0,7
SPIWrite 0859,00,0,7
SPIWrite 0858,00,0,7
SPIWrite 085b,00,0,7  //Property_838h_31_0=0x101;
      Address(0x858[7:0],0x859[7:0],0x85a[7:0],0x85b[7:0],0x85c[7:
0])
SPIWrite 085a,00,0,7
SPIWrite 0859,01,0,7
SPIWrite 0858,01,0,7
SPIWrite 085b,00,0,7  //Property_838h_31_0=0x0;
      Address(0x858[7:0],0x859[7:0],0x85a[7:0],0x85b[7:0],0x85c[7:
0])
SPIWrite 085a,00,0,7
SPIWrite 0859,00,0,7
SPIWrite 0858,00,0,7
SPIWrite 0015,00,0,7  //timing_controller=0x0;
      Address(0x15[7:7])
SPIWrite 0015,01,0,7  //pll=0x1;       Address(0x15[7:0])
SPIWrite 006a,00,0,7  //Property_48h_17_17=0x0;
      Address(0x6a[7:1])
SPIWrite 006e,00,0,7  //LCMGEN_USE_SPI_SYSREF=0x0;
      Address(0x6e[7:0])
SPIWrite 006a,00,0,7  //Property_48h_17_17=0x0;
      Address(0x6a[7:1])
SPIWrite 006a,02,0,7  //Property_48h_17_17=0x1;
      Address(0x6a[7:1])
SPIWrite 0015,00,0,7  //pll=0x0;       Address(0x15[7:0])

//STEP: pllConfig/step1

//External-Action: Give Sysref Here.
```

```
WAIT 0.001

//END: Sending Sysref to device

SPIWrite 0015,01,0,7  //pll=0x1;       Address(0x15[7:0])
SPIWrite 0063,c0,0,7  //Property_40h_27_24=0x0;
      Address(0x63[7:0])
SPIWrite 0015,00,0,7  //pll=0x0;       Address(0x15[7:0])
SPIWrite 0015,02,0,7  //ana_4t4r=0x1;  Address(0x15[7:1])
SPIWrite 00c1,00,0,7  //Property_a0h_15_13=0x0;
      Address(0xc1[7:5])
SPIWrite 0015,00,0,7  //ana_4t4r=0x0;  Address(0x15[7:1])
SPIWrite 0015,01,0,7  //pll=0x1;       Address(0x15[7:0])
SPIWrite 0063,40,0,7  //CLR_FLAG_LOCK_OUT=0x0;
      Address(0x63[7:7])
SPIWrite 0063,00,0,7  //CLR_FLAG_LOCK_LOST=0x0;
      Address(0x63[7:6])
SPIWrite 0066,33,0,7  //Property_44h_17_17=0x1;
      Address(0x66[7:1])

//START: Requesting/releasing SPI Access to PLL Pages

SPIWrite 0015,00,0,7  //pll=0x0;       Address(0x15[7:0])
SPIWrite 0015,40,0,7  //digtop=0x1;    Address(0x15[7:6])
SPIWrite 0170,00,0,7  //pll_reg_spi_req_a=0x0;
      Address(0x170[7:0])
SPIWrite 0540,00,0,7  //Property_520h_0_0=0x0;
      Address(0x540[7:0])

WAIT 0.2

//END: Requesting/releasing SPI Access to PLL Pages

SPIWrite 0015,00,0,7  //digtop=0x0;    Address(0x15[7:6])
SPIWrite 0015,80,0,7  //timing_controller=0x1;
      Address(0x15[7:7])
SPIWrite 010d,03,0,7  //Property_ech_15_0=0x31f;
      Address(0x10c[7:0],0x10d[7:0],0x10e[7:0])
SPIWrite 010c,1f,0,7
SPIWrite 01ad,03,0,7  //Property_18ch_15_0=0x31f;
      Address(0x1ac[7:0],0x1ad[7:0],0x1ae[7:0])
SPIWrite 01ac,1f,0,7
SPIWrite 024d,03,0,7  //Property_22ch_15_0=0x31f;
      Address(0x24c[7:0],0x24d[7:0],0x24e[7:0])
SPIWrite 024c,1f,0,7
SPIWrite 02ed,03,0,7  //Property_2cch_15_0=0x31f;
      Address(0x2ec[7:0],0x2ed[7:0],0x2ee[7:0])
SPIWrite 02ec,1f,0,7
SPIWrite 0421,01,0,7  //Property_400h_15_0=0x190;
      Address(0x420[7:0],0x421[7:0],0x422[7:0])
```

```
SPIWrite 0420,90,0,7
SPIWrite 04d9,01,0,7  //Property_4b8h_15_0=0x190;
     Address(0x4d8[7:0],0x4d9[7:0],0x4da[7:0])
SPIWrite 04d8,90,0,7
SPIWrite 0591,01,0,7  //Property_570h_15_0=0x190;
     Address(0x590[7:0],0x591[7:0],0x592[7:0])
SPIWrite 0590,90,0,7
SPIWrite 0649,01,0,7  //Property_628h_15_0=0x190;
     Address(0x648[7:0],0x649[7:0],0x64a[7:0])
SPIWrite 0648,90,0,7
SPIWrite 0701,01,0,7  //Property_6e0h_15_0=0x190;
     Address(0x700[7:0],0x701[7:0],0x702[7:0])
SPIWrite 0700,90,0,7
SPIWrite 07b9,01,0,7  //Property_798h_15_0=0x190;
     Address(0x7b8[7:0],0x7b9[7:0],0x7ba[7:0])
SPIWrite 07b8,90,0,7

//END: Configuring PLL

SPIWrite 0015,00,0,7  //timing_controller=0x0;
     Address(0x15[7:7])

//STEP: pllConfig/step2
SPIWrite 0018,40,0,7  //Property_18h_6_6=0x1;
     Address(0x18[7:6])
SPIWrite 0086,01,0,7  //Property_64h_16_16=0x1;
     Address(0x86[7:0])
SPIWrite 0082,10,0,7  //Property_60h_21_16=0x10;
     Address(0x82[7:0])
SPIWrite 0083,01,0,7  //Property_60h_24_24=0x1;
     Address(0x83[7:0])
SPIWrite 0084,00,0,7  //Property_64h_0_0=0x0;
     Address(0x84[7:0])
SPIWrite 0084,01,0,7  //Property_64h_0_0=0x1;
     Address(0x84[7:0])
SPIWrite 0084,00,0,7  //Property_64h_0_0=0x0;
     Address(0x84[7:0])
SPIWrite 0018,00,0,7  //Property_18h_6_6=0x0;
     Address(0x18[7:6])
SPIWrite 0018,20,0,7  //macro=0x1;    Address(0x18[7:5])
SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 0193,12,0,7  //MACRO_OPCODE=0x12;
     Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2
```

```
//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
      Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
      Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIWrite 0018,00,0,7  //macro=0x0;     Address(0x18[7:5])

//STEP: serdesConfig/step0

//START: Enabling access to SERDES
```

```
SPIWrite 0016,10,0,7  //jesd_subchip=0x1;   Address(0x16[7:4])
SPIWrite 00c0,02,0,7  //apb_clk_disable=0x0;
      Address(0xc0[7:0])
SPIWrite 00c0,00,0,7  //apb_clk_dithered_mode_en=0x0;
      Address(0xc0[7:1])
SPIWrite 00c4,01,0,7  //apb_clk_from_MCU_clk_en=0x1;
      Address(0xc4[7:0])
SPIWrite 0020,12,0,7  //serdesab_apb_page_addr_index=0x2;
      Address(0x20[7:0])
SPIWrite 0021,12,0,7  //serdescd_apb_page_addr_index=0x2;
      Address(0x21[7:0])
SPIWrite 0020,12,0,7  //serdesab_apb_mode_16b=0x1;
      Address(0x20[7:4])
SPIWrite 0021,12,0,7  //serdescd_apb_mode_16b=0x1;
      Address(0x21[7:4])
SPIWrite 0020,12,0,7  //serdesab_apb_pin_intf_en=0x0;
      Address(0x20[7:2])
SPIWrite 0021,12,0,7  //serdescd_apb_pin_intf_en=0x0;
      Address(0x21[7:2])
SPIWrite 00c0,40,0,7  //apb_clk_sysref_sel=0x1;
      Address(0xc0[7:6])
SPIWrite 00c0,40,0,7  //apb_clk_sysref_val=0x0;
      Address(0xc0[7:7])
SPIWrite 00c0,c0,0,7  //apb_clk_sysref_val=0x1;
      Address(0xc0[7:7])
SPIWrite 00c0,40,0,7  //apb_clk_sysref_val=0x0;
      Address(0xc0[7:7])
SPIWrite 0016,00,0,7  //jesd_subchip=0x0;   Address(0x16[7:4])
SPIWrite 0016,20,0,7  //serdes_jesd=0x1;    Address(0x16[7:5])
SPIWrite 7007,00,0,7  //BUS_WIDTH_LANE3=0x0;
      Address(0x9803[7:3])
SPIWrite 7006,00,0,7
SPIWrite 7007,00,0,7  //BUS_WIDTH_LANE2=0x0;
      Address(0x9803[7:2])
SPIWrite 7006,00,0,7
SPIWrite 7007,00,0,7  //BUS_WIDTH_LANE1=0x0;
      Address(0x9803[7:1])
SPIWrite 7006,00,0,7
SPIWrite 7007,00,0,7  //BUS_WIDTH_LANE0=0x0;
      Address(0x9803[7:0])
SPIWrite 7006,00,0,7
SPIWrite 0016,40,0,7  //serdes_jesd=0x2;    Address(0x16[7:5])
SPIWrite 7007,00,0,7  //BUS_WIDTH_LANE3=0x0;
      Address(0x9803[7:3])
SPIWrite 7006,00,0,7
SPIWrite 7007,00,0,7  //BUS_WIDTH_LANE2=0x0;
      Address(0x9803[7:2])
SPIWrite 7006,00,0,7
SPIWrite 7007,00,0,7  //BUS_WIDTH_LANE1=0x0;
      Address(0x9803[7:1])
SPIWrite 7006,00,0,7
SPIWrite 7007,00,0,7  //BUS_WIDTH_LANE0=0x0;
```

```
     Address(0x9803[7:0])
SPIWrite 7006,00,0,7

//END: Done enabling access to SERDES


//START: Setting Serdes Reference Clock Divs

SPIWrite 0016,00,0,7  //serdes_jesd=0x0;    Address(0x16[7:5])
SPIWrite 0015,02,0,7  //ana_4t4r=0x1; Address(0x15[7:1])
SPIWrite 0107,00,0,7  //Property_e4h_31_0=0x101;
     Address(0x104[7:0],0x105[7:0],0x106[7:0],0x107[7:0],0x108[7:
0])
SPIWrite 0106,00,0,7
SPIWrite 0105,01,0,7
SPIWrite 0104,01,0,7

//END: Setting Serdes Reference Clock Divs

SPIWrite 0015,00,0,7  //ana_4t4r=0x0; Address(0x15[7:1])

//STEP: serdesConfig/step1

//START: Resetting Serdes

SPIWrite 0016,20,0,7  //serdes_jesd=0x1;    Address(0x16[7:5])
SPIWrite 701b,08,0,7  //DOMAIN_RESET=0x888;
     Address(0x980d[3:0],0x980e[7:0])
SPIWrite 701a,88,0,7
SPIWrite 701b,00,0,7  //DOMAIN_RESET=0x0;
     Address(0x980d[3:0],0x980e[7:0])
SPIWrite 701a,00,0,7

WAIT 0.1
SPIWrite 701b,07,0,7  //DOMAIN_RESET=0x777;
     Address(0x980d[3:0],0x980e[7:0])
SPIWrite 701a,77,0,7
SPIWrite 701b,00,0,7  //DOMAIN_RESET=0x0;
     Address(0x980d[3:0],0x980e[7:0])
SPIWrite 701a,00,0,7

WAIT 0.1

//END: Done resetting Serdes


//START: Resetting Serdes

SPIWrite 0016,40,0,7  //serdes_jesd=0x2;    Address(0x16[7:5])
SPIWrite 701b,08,0,7  //DOMAIN_RESET=0x888;
     Address(0x980d[3:0],0x980e[7:0])
SPIWrite 701a,88,0,7
```

```
SPIWrite 701b,00,0,7  //DOMAIN_RESET=0x0;
     Address(0x980d[3:0],0x980e[7:0])
SPIWrite 701a,00,0,7

WAIT 0.1
SPIWrite 701b,07,0,7  //DOMAIN_RESET=0x777;
     Address(0x980d[3:0],0x980e[7:0])
SPIWrite 701a,77,0,7
SPIWrite 701b,00,0,7  //DOMAIN_RESET=0x0;
     Address(0x980d[3:0],0x980e[7:0])
SPIWrite 701a,00,0,7

WAIT 0.1

//END: Done resetting Serdes

SPIWrite 0016,00,0,7  //serdes_jesd=0x0;    Address(0x16[7:5])

//STEP: serdesConfig/step2

//START: Configuring the SERDES

SPIWrite 0016,10,0,7  //jesd_subchip=0x1;   Address(0x16[7:4])
SPIWrite 00c1,02,0,7  //apb_clk_div_factor=0x2;
     Address(0xc1[7:0])
SPIWrite 00c0,40,0,7  //apb_clk_disable=0x0;
     Address(0xc0[7:0])
SPIWrite 0020,12,0,7  //serdesab_apb_page_addr_index=0x2;
     Address(0x20[7:0])
SPIWrite 0021,12,0,7  //serdescd_apb_page_addr_index=0x2;
     Address(0x21[7:0])
SPIWrite 0016,00,0,7  //jesd_subchip=0x0;   Address(0x16[7:4])
SPIWrite 0016,60,0,7  //serdes_jesd=0x3;    Address(0x16[7:5])
SPIWrite 7029,ff,0,7
SPIWrite 7028,f0,0,7
SPIWrite 701b,0a,0,7
SPIWrite 701a,aa,0,7
SPIWrite 701b,00,0,7
SPIWrite 701a,00,0,7
SPIWrite 7007,00,0,7
SPIWrite 7006,00,0,7
SPIWrite 0016,20,0,7  //serdes_jesd=0x1;    Address(0x16[7:5])
SPIWrite 49f1,92,0,7
SPIWrite 49f0,40,0,7
SPIWrite 49f3,ea,0,7
SPIWrite 49f2,80,0,7
SPIWrite 49e3,f0,0,7
SPIWrite 49e2,00,0,7
SPIWrite 49b5,47,0,7
SPIWrite 49b4,47,0,7
SPIWrite 49ff,fd,0,7
SPIWrite 49fe,b0,0,7
```

```
SPIWrite 49ed,1d,0,7
SPIWrite 49ec,c0,0,7
SPIWrite 49e7,52,0,7
SPIWrite 49e6,26,0,7
SPIWrite 49e5,6e,0,7
SPIWrite 49e4,b6,0,7
SPIWrite 49df,a8,0,7
SPIWrite 49de,28,0,7
SPIWrite 49eb,16,0,7
SPIWrite 49ea,90,0,7
SPIWrite 49e9,12,0,7
SPIWrite 49e8,44,0,7
SPIWrite 49fd,16,0,7
SPIWrite 49fc,90,0,7
SPIWrite 49fb,12,0,7
SPIWrite 49fa,48,0,7
SPIWrite 49f9,4a,0,7
SPIWrite 49f8,44,0,7
SPIWrite 49f7,79,0,7
SPIWrite 49f6,b6,0,7
SPIWrite 49d9,6c,0,7
SPIWrite 49d8,06,0,7
SPIWrite 4201,10,0,7
SPIWrite 4200,6b,0,7
SPIWrite 4203,64,0,7
SPIWrite 4202,80,0,7
SPIWrite 4205,62,0,7
SPIWrite 4204,00,0,7
SPIWrite 4207,7b,0,7
SPIWrite 4206,33,0,7
SPIWrite 4209,70,0,7
SPIWrite 4208,0a,0,7
SPIWrite 420b,bd,0,7
SPIWrite 420a,68,0,7
SPIWrite 420d,76,0,7
SPIWrite 420c,2d,0,7
SPIWrite 420f,66,0,7
SPIWrite 420e,ab,0,7
SPIWrite 4211,d0,0,7
SPIWrite 4210,08,0,7
SPIWrite 4213,00,0,7
SPIWrite 4212,18,0,7
SPIWrite 4215,66,0,7
SPIWrite 4214,2c,0,7
SPIWrite 4217,3d,0,7
SPIWrite 4216,15,0,7
SPIWrite 4219,00,0,7
SPIWrite 4218,80,0,7
SPIWrite 421b,00,0,7
SPIWrite 421a,02,0,7
SPIWrite 421d,34,0,7
SPIWrite 421c,00,0,7
```

```
SPIWrite 421f,00,0,7
SPIWrite 421e,00,0,7
SPIWrite 4221,10,0,7
SPIWrite 4220,1a,0,7
SPIWrite 4239,03,0,7
SPIWrite 4238,40,0,7
SPIWrite 423b,00,0,7
SPIWrite 423a,60,0,7
SPIWrite 423d,00,0,7
SPIWrite 423c,00,0,7
SPIWrite 423f,00,0,7
SPIWrite 423e,00,0,7
SPIWrite 4277,00,0,7
SPIWrite 4276,00,0,7
SPIWrite 4279,00,0,7
SPIWrite 4278,00,0,7
SPIWrite 427b,00,0,7
SPIWrite 427a,00,0,7
SPIWrite 427d,00,0,7
SPIWrite 427c,00,0,7
SPIWrite 4283,9f,0,7
SPIWrite 4282,df,0,7
SPIWrite 4285,b3,0,7
SPIWrite 4284,c0,0,7
SPIWrite 428f,24,0,7
SPIWrite 428e,a2,0,7
SPIWrite 4291,cc,0,7
SPIWrite 4290,34,0,7
SPIWrite 4293,e3,0,7
SPIWrite 4292,d7,0,7
SPIWrite 4295,76,0,7
SPIWrite 4294,60,0,7
SPIWrite 4297,06,0,7
SPIWrite 4296,db,0,7
SPIWrite 4341,03,0,7
SPIWrite 4340,41,0,7
SPIWrite 43e7,00,0,7
SPIWrite 43e6,80,0,7
SPIWrite 43e9,fc,0,7
SPIWrite 43e8,00,0,7
SPIWrite 43eb,9f,0,7
SPIWrite 43ea,fe,0,7
SPIWrite 43ed,00,0,7
SPIWrite 43ec,60,0,7
SPIWrite 43ef,10,0,7
SPIWrite 43ee,00,0,7
SPIWrite 43f1,68,0,7
SPIWrite 43f0,64,0,7
SPIWrite 43f3,92,0,7
SPIWrite 43f2,30,0,7
SPIWrite 43f5,00,0,7
SPIWrite 43f4,00,0,7
```

```
SPIWrite 43f7,6d,0,7
SPIWrite 43f6,83,0,7
SPIWrite 43f9,db,0,7
SPIWrite 43f8,6c,0,7
SPIWrite 43fb,42,0,7
SPIWrite 43fa,6e,0,7
SPIWrite 43fd,62,0,7
SPIWrite 43fc,78,0,7
SPIWrite 43ff,08,0,7
SPIWrite 43fe,c8,0,7
SPIWrite 4001,10,0,7
SPIWrite 4000,6b,0,7
SPIWrite 4003,64,0,7
SPIWrite 4002,80,0,7
SPIWrite 4005,62,0,7
SPIWrite 4004,00,0,7
SPIWrite 4007,7b,0,7
SPIWrite 4006,33,0,7
SPIWrite 4009,70,0,7
SPIWrite 4008,0a,0,7
SPIWrite 400b,bd,0,7
SPIWrite 400a,68,0,7
SPIWrite 400d,76,0,7
SPIWrite 400c,2d,0,7
SPIWrite 400f,66,0,7
SPIWrite 400e,ab,0,7
SPIWrite 4011,d0,0,7
SPIWrite 4010,08,0,7
SPIWrite 4013,00,0,7
SPIWrite 4012,18,0,7
SPIWrite 4015,66,0,7
SPIWrite 4014,2c,0,7
SPIWrite 4017,3d,0,7
SPIWrite 4016,15,0,7
SPIWrite 4019,00,0,7
SPIWrite 4018,80,0,7
SPIWrite 401b,00,0,7
SPIWrite 401a,02,0,7
SPIWrite 401d,34,0,7
SPIWrite 401c,00,0,7
SPIWrite 401f,00,0,7
SPIWrite 401e,00,0,7
SPIWrite 4021,10,0,7
SPIWrite 4020,1a,0,7
SPIWrite 4039,03,0,7
SPIWrite 4038,40,0,7
SPIWrite 403b,00,0,7
SPIWrite 403a,60,0,7
SPIWrite 403d,00,0,7
SPIWrite 403c,00,0,7
SPIWrite 403f,00,0,7
SPIWrite 403e,00,0,7
```

```
SPIWrite 4077,00,0,7
SPIWrite 4076,00,0,7
SPIWrite 4079,00,0,7
SPIWrite 4078,00,0,7
SPIWrite 407b,00,0,7
SPIWrite 407a,00,0,7
SPIWrite 407d,00,0,7
SPIWrite 407c,00,0,7
SPIWrite 4083,9f,0,7
SPIWrite 4082,df,0,7
SPIWrite 4085,b3,0,7
SPIWrite 4084,c0,0,7
SPIWrite 408f,24,0,7
SPIWrite 408e,a2,0,7
SPIWrite 4091,cc,0,7
SPIWrite 4090,34,0,7
SPIWrite 4093,e3,0,7
SPIWrite 4092,d7,0,7
SPIWrite 4095,76,0,7
SPIWrite 4094,60,0,7
SPIWrite 4097,06,0,7
SPIWrite 4096,db,0,7
SPIWrite 4141,03,0,7
SPIWrite 4140,41,0,7
SPIWrite 41e7,00,0,7
SPIWrite 41e6,80,0,7
SPIWrite 41e9,fc,0,7
SPIWrite 41e8,00,0,7
SPIWrite 41eb,9f,0,7
SPIWrite 41ea,fe,0,7
SPIWrite 41ed,00,0,7
SPIWrite 41ec,00,0,7
SPIWrite 41ef,10,0,7
SPIWrite 41ee,00,0,7
SPIWrite 41f1,68,0,7
SPIWrite 41f0,64,0,7
SPIWrite 41f3,92,0,7
SPIWrite 41f2,30,0,7
SPIWrite 41f5,00,0,7
SPIWrite 41f4,00,0,7
SPIWrite 41f7,6d,0,7
SPIWrite 41f6,87,0,7
SPIWrite 41f9,db,0,7
SPIWrite 41f8,6c,0,7
SPIWrite 41fb,42,0,7
SPIWrite 41fa,6e,0,7
SPIWrite 41fd,62,0,7
SPIWrite 41fc,7c,0,7
SPIWrite 41ff,88,0,7
SPIWrite 41fe,c8,0,7
SPIWrite 4401,10,0,7
SPIWrite 4400,6b,0,7
```

```
SPIWrite 4403,64,0,7
SPIWrite 4402,80,0,7
SPIWrite 4405,62,0,7
SPIWrite 4404,00,0,7
SPIWrite 4407,7b,0,7
SPIWrite 4406,33,0,7
SPIWrite 4409,70,0,7
SPIWrite 4408,0a,0,7
SPIWrite 440b,bd,0,7
SPIWrite 440a,68,0,7
SPIWrite 440d,76,0,7
SPIWrite 440c,2d,0,7
SPIWrite 440f,66,0,7
SPIWrite 440e,ab,0,7
SPIWrite 4411,d0,0,7
SPIWrite 4410,08,0,7
SPIWrite 4413,00,0,7
SPIWrite 4412,18,0,7
SPIWrite 4415,66,0,7
SPIWrite 4414,2c,0,7
SPIWrite 4417,3d,0,7
SPIWrite 4416,15,0,7
SPIWrite 4419,00,0,7
SPIWrite 4418,80,0,7
SPIWrite 441b,00,0,7
SPIWrite 441a,02,0,7
SPIWrite 441d,34,0,7
SPIWrite 441c,00,0,7
SPIWrite 441f,00,0,7
SPIWrite 441e,00,0,7
SPIWrite 4421,10,0,7
SPIWrite 4420,1a,0,7
SPIWrite 4439,03,0,7
SPIWrite 4438,40,0,7
SPIWrite 443b,00,0,7
SPIWrite 443a,60,0,7
SPIWrite 443d,00,0,7
SPIWrite 443c,00,0,7
SPIWrite 443f,00,0,7
SPIWrite 443e,00,0,7
SPIWrite 4477,00,0,7
SPIWrite 4476,00,0,7
SPIWrite 4479,00,0,7
SPIWrite 4478,00,0,7
SPIWrite 447b,00,0,7
SPIWrite 447a,00,0,7
SPIWrite 447d,00,0,7
SPIWrite 447c,00,0,7
SPIWrite 4483,9f,0,7
SPIWrite 4482,df,0,7
SPIWrite 4485,b3,0,7
SPIWrite 4484,c0,0,7
```

```
SPIWrite 448f,24,0,7
SPIWrite 448e,a2,0,7
SPIWrite 4491,cc,0,7
SPIWrite 4490,34,0,7
SPIWrite 4493,e3,0,7
SPIWrite 4492,d7,0,7
SPIWrite 4495,76,0,7
SPIWrite 4494,60,0,7
SPIWrite 4497,06,0,7
SPIWrite 4496,db,0,7
SPIWrite 4541,03,0,7
SPIWrite 4540,41,0,7
SPIWrite 45e7,00,0,7
SPIWrite 45e6,80,0,7
SPIWrite 45e9,fc,0,7
SPIWrite 45e8,00,0,7
SPIWrite 45eb,9f,0,7
SPIWrite 45ea,fe,0,7
SPIWrite 45ed,00,0,7
SPIWrite 45ec,00,0,7
SPIWrite 45ef,10,0,7
SPIWrite 45ee,00,0,7
SPIWrite 45f1,68,0,7
SPIWrite 45f0,64,0,7
SPIWrite 45f3,92,0,7
SPIWrite 45f2,30,0,7
SPIWrite 45f5,00,0,7
SPIWrite 45f4,00,0,7
SPIWrite 45f7,6d,0,7
SPIWrite 45f6,87,0,7
SPIWrite 45f9,db,0,7
SPIWrite 45f8,6c,0,7
SPIWrite 45fb,42,0,7
SPIWrite 45fa,6e,0,7
SPIWrite 45fd,62,0,7
SPIWrite 45fc,7c,0,7
SPIWrite 45ff,88,0,7
SPIWrite 45fe,c8,0,7
SPIWrite 4601,10,0,7
SPIWrite 4600,6b,0,7
SPIWrite 4603,64,0,7
SPIWrite 4602,80,0,7
SPIWrite 4605,62,0,7
SPIWrite 4604,00,0,7
SPIWrite 4607,7b,0,7
SPIWrite 4606,33,0,7
SPIWrite 4609,70,0,7
SPIWrite 4608,0a,0,7
SPIWrite 460b,bd,0,7
SPIWrite 460a,68,0,7
SPIWrite 460d,76,0,7
SPIWrite 460c,2d,0,7
```

```
SPIWrite 460f,66,0,7
SPIWrite 460e,ab,0,7
SPIWrite 4611,d0,0,7
SPIWrite 4610,08,0,7
SPIWrite 4613,00,0,7
SPIWrite 4612,18,0,7
SPIWrite 4615,66,0,7
SPIWrite 4614,2c,0,7
SPIWrite 4617,3d,0,7
SPIWrite 4616,15,0,7
SPIWrite 4619,00,0,7
SPIWrite 4618,80,0,7
SPIWrite 461b,00,0,7
SPIWrite 461a,02,0,7
SPIWrite 461d,34,0,7
SPIWrite 461c,00,0,7
SPIWrite 461f,00,0,7
SPIWrite 461e,00,0,7
SPIWrite 4621,10,0,7
SPIWrite 4620,1a,0,7
SPIWrite 4639,03,0,7
SPIWrite 4638,40,0,7
SPIWrite 463b,00,0,7
SPIWrite 463a,60,0,7
SPIWrite 463d,00,0,7
SPIWrite 463c,00,0,7
SPIWrite 463f,00,0,7
SPIWrite 463e,00,0,7
SPIWrite 4677,00,0,7
SPIWrite 4676,00,0,7
SPIWrite 4679,00,0,7
SPIWrite 4678,00,0,7
SPIWrite 467b,00,0,7
SPIWrite 467a,00,0,7
SPIWrite 467d,00,0,7
SPIWrite 467c,00,0,7
SPIWrite 4683,9f,0,7
SPIWrite 4682,df,0,7
SPIWrite 4685,b3,0,7
SPIWrite 4684,c0,0,7
SPIWrite 468f,24,0,7
SPIWrite 468e,a2,0,7
SPIWrite 4691,cc,0,7
SPIWrite 4690,34,0,7
SPIWrite 4693,e3,0,7
SPIWrite 4692,d7,0,7
SPIWrite 4695,76,0,7
SPIWrite 4694,60,0,7
SPIWrite 4697,06,0,7
SPIWrite 4696,db,0,7
SPIWrite 4741,03,0,7
SPIWrite 4740,41,0,7
```

```
SPIWrite 47e7,00,0,7
SPIWrite 47e6,80,0,7
SPIWrite 47e9,fc,0,7
SPIWrite 47e8,00,0,7
SPIWrite 47eb,9f,0,7
SPIWrite 47ea,fe,0,7
SPIWrite 47ed,00,0,7
SPIWrite 47ec,00,0,7
SPIWrite 47ef,10,0,7
SPIWrite 47ee,00,0,7
SPIWrite 47f1,68,0,7
SPIWrite 47f0,64,0,7
SPIWrite 47f3,92,0,7
SPIWrite 47f2,30,0,7
SPIWrite 47f5,00,0,7
SPIWrite 47f4,00,0,7
SPIWrite 47f7,6d,0,7
SPIWrite 47f6,87,0,7
SPIWrite 47f9,db,0,7
SPIWrite 47f8,6c,0,7
SPIWrite 47fb,42,0,7
SPIWrite 47fa,6e,0,7
SPIWrite 47fd,62,0,7
SPIWrite 47fc,7c,0,7
SPIWrite 47ff,88,0,7
SPIWrite 47fe,c8,0,7
SPIWrite 0016,40,0,7  //serdes_jesd=0x2;    Address(0x16[7:5])
SPIWrite 49f1,82,0,7
SPIWrite 49f0,40,0,7
SPIWrite 49f3,e2,0,7
SPIWrite 49f2,80,0,7
SPIWrite 49e3,b0,0,7
SPIWrite 49e2,00,0,7
SPIWrite 49b5,47,0,7
SPIWrite 49b4,47,0,7
SPIWrite 49ff,ed,0,7
SPIWrite 49fe,b0,0,7
SPIWrite 49ed,0d,0,7
SPIWrite 49ec,c0,0,7
SPIWrite 49e7,52,0,7
SPIWrite 49e6,26,0,7
SPIWrite 49e5,6e,0,7
SPIWrite 49e4,b6,0,7
SPIWrite 49df,a8,0,7
SPIWrite 49de,28,0,7
SPIWrite 49eb,16,0,7
SPIWrite 49ea,10,0,7
SPIWrite 49e9,12,0,7
SPIWrite 49e8,44,0,7
SPIWrite 49fd,16,0,7
SPIWrite 49fc,10,0,7
SPIWrite 49fb,12,0,7
```

```
SPIWrite 49fa,48,0,7
SPIWrite 49f9,4a,0,7
SPIWrite 49f8,44,0,7
SPIWrite 49f7,79,0,7
SPIWrite 49f6,b6,0,7
SPIWrite 49d9,6c,0,7
SPIWrite 49d8,06,0,7
SPIWrite 4601,10,0,7
SPIWrite 4600,6b,0,7
SPIWrite 4603,64,0,7
SPIWrite 4602,80,0,7
SPIWrite 4605,62,0,7
SPIWrite 4604,00,0,7
SPIWrite 4607,7b,0,7
SPIWrite 4606,33,0,7
SPIWrite 4609,70,0,7
SPIWrite 4608,0a,0,7
SPIWrite 460b,bd,0,7
SPIWrite 460a,68,0,7
SPIWrite 460d,76,0,7
SPIWrite 460c,2d,0,7
SPIWrite 460f,66,0,7
SPIWrite 460e,ab,0,7
SPIWrite 4611,d0,0,7
SPIWrite 4610,08,0,7
SPIWrite 4613,00,0,7
SPIWrite 4612,18,0,7
SPIWrite 4615,66,0,7
SPIWrite 4614,2c,0,7
SPIWrite 4617,3d,0,7
SPIWrite 4616,15,0,7
SPIWrite 4619,00,0,7
SPIWrite 4618,80,0,7
SPIWrite 461b,00,0,7
SPIWrite 461a,02,0,7
SPIWrite 461d,34,0,7
SPIWrite 461c,00,0,7
SPIWrite 461f,00,0,7
SPIWrite 461e,00,0,7
SPIWrite 4621,10,0,7
SPIWrite 4620,1a,0,7
SPIWrite 4639,03,0,7
SPIWrite 4638,40,0,7
SPIWrite 463b,00,0,7
SPIWrite 463a,60,0,7
SPIWrite 463d,00,0,7
SPIWrite 463c,00,0,7
SPIWrite 463f,00,0,7
SPIWrite 463e,00,0,7
SPIWrite 4677,00,0,7
SPIWrite 4676,00,0,7
SPIWrite 4679,00,0,7
```

```
SPIWrite 4678,00,0,7
SPIWrite 467b,00,0,7
SPIWrite 467a,00,0,7
SPIWrite 467d,00,0,7
SPIWrite 467c,00,0,7
SPIWrite 4683,9f,0,7
SPIWrite 4682,df,0,7
SPIWrite 4685,b3,0,7
SPIWrite 4684,c0,0,7
SPIWrite 468f,24,0,7
SPIWrite 468e,a2,0,7
SPIWrite 4691,cc,0,7
SPIWrite 4690,34,0,7
SPIWrite 4693,e3,0,7
SPIWrite 4692,d7,0,7
SPIWrite 4695,76,0,7
SPIWrite 4694,60,0,7
SPIWrite 4697,06,0,7
SPIWrite 4696,db,0,7
SPIWrite 4741,03,0,7
SPIWrite 4740,41,0,7
SPIWrite 47e7,00,0,7
SPIWrite 47e6,80,0,7
SPIWrite 47e9,fc,0,7
SPIWrite 47e8,00,0,7
SPIWrite 47eb,1f,0,7
SPIWrite 47ea,fe,0,7
SPIWrite 47ed,00,0,7
SPIWrite 47ec,00,0,7
SPIWrite 47ef,10,0,7
SPIWrite 47ee,00,0,7
SPIWrite 47f1,68,0,7
SPIWrite 47f0,64,0,7
SPIWrite 47f3,92,0,7
SPIWrite 47f2,30,0,7
SPIWrite 47f5,00,0,7
SPIWrite 47f4,00,0,7
SPIWrite 47f7,6d,0,7
SPIWrite 47f6,83,0,7
SPIWrite 47f9,db,0,7
SPIWrite 47f8,6c,0,7
SPIWrite 47fb,42,0,7
SPIWrite 47fa,6e,0,7
SPIWrite 47fd,62,0,7
SPIWrite 47fc,78,0,7
SPIWrite 47ff,08,0,7
SPIWrite 47fe,c8,0,7
SPIWrite 4401,10,0,7
SPIWrite 4400,6b,0,7
SPIWrite 4403,64,0,7
SPIWrite 4402,80,0,7
SPIWrite 4405,62,0,7
```

```
SPIWrite 4404,00,0,7
SPIWrite 4407,7b,0,7
SPIWrite 4406,33,0,7
SPIWrite 4409,70,0,7
SPIWrite 4408,0a,0,7
SPIWrite 440b,bd,0,7
SPIWrite 440a,68,0,7
SPIWrite 440d,76,0,7
SPIWrite 440c,2d,0,7
SPIWrite 440f,66,0,7
SPIWrite 440e,ab,0,7
SPIWrite 4411,d0,0,7
SPIWrite 4410,08,0,7
SPIWrite 4413,00,0,7
SPIWrite 4412,18,0,7
SPIWrite 4415,66,0,7
SPIWrite 4414,2c,0,7
SPIWrite 4417,3d,0,7
SPIWrite 4416,15,0,7
SPIWrite 4419,00,0,7
SPIWrite 4418,80,0,7
SPIWrite 441b,00,0,7
SPIWrite 441a,02,0,7
SPIWrite 441d,34,0,7
SPIWrite 441c,00,0,7
SPIWrite 441f,00,0,7
SPIWrite 441e,00,0,7
SPIWrite 4421,10,0,7
SPIWrite 4420,1a,0,7
SPIWrite 4439,03,0,7
SPIWrite 4438,40,0,7
SPIWrite 443b,00,0,7
SPIWrite 443a,60,0,7
SPIWrite 443d,00,0,7
SPIWrite 443c,00,0,7
SPIWrite 443f,00,0,7
SPIWrite 443e,00,0,7
SPIWrite 4477,00,0,7
SPIWrite 4476,00,0,7
SPIWrite 4479,00,0,7
SPIWrite 4478,00,0,7
SPIWrite 447b,00,0,7
SPIWrite 447a,00,0,7
SPIWrite 447d,00,0,7
SPIWrite 447c,00,0,7
SPIWrite 4483,9f,0,7
SPIWrite 4482,df,0,7
SPIWrite 4485,b3,0,7
SPIWrite 4484,c0,0,7
SPIWrite 448f,24,0,7
SPIWrite 448e,a2,0,7
SPIWrite 4491,cc,0,7
```

```
SPIWrite 4490,34,0,7
SPIWrite 4493,e3,0,7
SPIWrite 4492,d7,0,7
SPIWrite 4495,76,0,7
SPIWrite 4494,60,0,7
SPIWrite 4497,06,0,7
SPIWrite 4496,db,0,7
SPIWrite 4541,03,0,7
SPIWrite 4540,41,0,7
SPIWrite 45e7,00,0,7
SPIWrite 45e6,80,0,7
SPIWrite 45e9,fc,0,7
SPIWrite 45e8,00,0,7
SPIWrite 45eb,1f,0,7
SPIWrite 45ea,fe,0,7
SPIWrite 45ed,00,0,7
SPIWrite 45ec,00,0,7
SPIWrite 45ef,10,0,7
SPIWrite 45ee,00,0,7
SPIWrite 45f1,68,0,7
SPIWrite 45f0,64,0,7
SPIWrite 45f3,92,0,7
SPIWrite 45f2,30,0,7
SPIWrite 45f5,00,0,7
SPIWrite 45f4,00,0,7
SPIWrite 45f7,6d,0,7
SPIWrite 45f6,87,0,7
SPIWrite 45f9,db,0,7
SPIWrite 45f8,6c,0,7
SPIWrite 45fb,42,0,7
SPIWrite 45fa,6e,0,7
SPIWrite 45fd,62,0,7
SPIWrite 45fc,7c,0,7
SPIWrite 45ff,88,0,7
SPIWrite 45fe,c8,0,7
SPIWrite 4001,10,0,7
SPIWrite 4000,6b,0,7
SPIWrite 4003,64,0,7
SPIWrite 4002,80,0,7
SPIWrite 4005,62,0,7
SPIWrite 4004,00,0,7
SPIWrite 4007,7b,0,7
SPIWrite 4006,33,0,7
SPIWrite 4009,70,0,7
SPIWrite 4008,0a,0,7
SPIWrite 400b,bd,0,7
SPIWrite 400a,68,0,7
SPIWrite 400d,76,0,7
SPIWrite 400c,2d,0,7
SPIWrite 400f,66,0,7
SPIWrite 400e,ab,0,7
SPIWrite 4011,d0,0,7
```

```
SPIWrite 4010,08,0,7
SPIWrite 4013,00,0,7
SPIWrite 4012,18,0,7
SPIWrite 4015,66,0,7
SPIWrite 4014,2c,0,7
SPIWrite 4017,3d,0,7
SPIWrite 4016,15,0,7
SPIWrite 4019,00,0,7
SPIWrite 4018,80,0,7
SPIWrite 401b,00,0,7
SPIWrite 401a,02,0,7
SPIWrite 401d,34,0,7
SPIWrite 401c,00,0,7
SPIWrite 401f,00,0,7
SPIWrite 401e,00,0,7
SPIWrite 4021,10,0,7
SPIWrite 4020,1a,0,7
SPIWrite 4039,03,0,7
SPIWrite 4038,40,0,7
SPIWrite 403b,00,0,7
SPIWrite 403a,60,0,7
SPIWrite 403d,00,0,7
SPIWrite 403c,00,0,7
SPIWrite 403f,00,0,7
SPIWrite 403e,00,0,7
SPIWrite 4077,00,0,7
SPIWrite 4076,00,0,7
SPIWrite 4079,00,0,7
SPIWrite 4078,00,0,7
SPIWrite 407b,00,0,7
SPIWrite 407a,00,0,7
SPIWrite 407d,00,0,7
SPIWrite 407c,00,0,7
SPIWrite 4083,9f,0,7
SPIWrite 4082,df,0,7
SPIWrite 4085,b3,0,7
SPIWrite 4084,c0,0,7
SPIWrite 408f,24,0,7
SPIWrite 408e,a2,0,7
SPIWrite 4091,cc,0,7
SPIWrite 4090,34,0,7
SPIWrite 4093,e3,0,7
SPIWrite 4092,d7,0,7
SPIWrite 4095,76,0,7
SPIWrite 4094,60,0,7
SPIWrite 4097,06,0,7
SPIWrite 4096,db,0,7
SPIWrite 4141,03,0,7
SPIWrite 4140,41,0,7
SPIWrite 41e7,00,0,7
SPIWrite 41e6,80,0,7
SPIWrite 41e9,fc,0,7
```

```
SPIWrite 41e8,00,0,7
SPIWrite 41eb,1f,0,7
SPIWrite 41ea,fe,0,7
SPIWrite 41ed,00,0,7
SPIWrite 41ec,00,0,7
SPIWrite 41ef,10,0,7
SPIWrite 41ee,00,0,7
SPIWrite 41f1,68,0,7
SPIWrite 41f0,64,0,7
SPIWrite 41f3,92,0,7
SPIWrite 41f2,30,0,7
SPIWrite 41f5,00,0,7
SPIWrite 41f4,00,0,7
SPIWrite 41f7,6d,0,7
SPIWrite 41f6,83,0,7
SPIWrite 41f9,db,0,7
SPIWrite 41f8,6c,0,7
SPIWrite 41fb,42,0,7
SPIWrite 41fa,6e,0,7
SPIWrite 41fd,62,0,7
SPIWrite 41fc,78,0,7
SPIWrite 41ff,08,0,7
SPIWrite 41fe,c8,0,7
SPIWrite 4201,10,0,7
SPIWrite 4200,6b,0,7
SPIWrite 4203,64,0,7
SPIWrite 4202,80,0,7
SPIWrite 4205,62,0,7
SPIWrite 4204,00,0,7
SPIWrite 4207,7b,0,7
SPIWrite 4206,33,0,7
SPIWrite 4209,70,0,7
SPIWrite 4208,0a,0,7
SPIWrite 420b,bd,0,7
SPIWrite 420a,68,0,7
SPIWrite 420d,76,0,7
SPIWrite 420c,2d,0,7
SPIWrite 420f,66,0,7
SPIWrite 420e,ab,0,7
SPIWrite 4211,d0,0,7
SPIWrite 4210,08,0,7
SPIWrite 4213,00,0,7
SPIWrite 4212,18,0,7
SPIWrite 4215,66,0,7
SPIWrite 4214,2c,0,7
SPIWrite 4217,3d,0,7
SPIWrite 4216,15,0,7
SPIWrite 4219,00,0,7
SPIWrite 4218,80,0,7
SPIWrite 421b,00,0,7
SPIWrite 421a,02,0,7
SPIWrite 421d,34,0,7
```

```
SPIWrite 421c,00,0,7
SPIWrite 421f,00,0,7
SPIWrite 421e,00,0,7
SPIWrite 4221,10,0,7
SPIWrite 4220,1a,0,7
SPIWrite 4239,03,0,7
SPIWrite 4238,40,0,7
SPIWrite 423b,00,0,7
SPIWrite 423a,60,0,7
SPIWrite 423d,00,0,7
SPIWrite 423c,00,0,7
SPIWrite 423f,00,0,7
SPIWrite 423e,00,0,7
SPIWrite 4277,00,0,7
SPIWrite 4276,00,0,7
SPIWrite 4279,00,0,7
SPIWrite 4278,00,0,7
SPIWrite 427b,00,0,7
SPIWrite 427a,00,0,7
SPIWrite 427d,00,0,7
SPIWrite 427c,00,0,7
SPIWrite 4283,9f,0,7
SPIWrite 4282,df,0,7
SPIWrite 4285,b3,0,7
SPIWrite 4284,c0,0,7
SPIWrite 428f,24,0,7
SPIWrite 428e,a2,0,7
SPIWrite 4291,cc,0,7
SPIWrite 4290,34,0,7
SPIWrite 4293,e3,0,7
SPIWrite 4292,d7,0,7
SPIWrite 4295,76,0,7
SPIWrite 4294,60,0,7
SPIWrite 4297,06,0,7
SPIWrite 4296,db,0,7
SPIWrite 4341,03,0,7
SPIWrite 4340,41,0,7
SPIWrite 43e7,00,0,7
SPIWrite 43e6,80,0,7
SPIWrite 43e9,fc,0,7
SPIWrite 43e8,00,0,7
SPIWrite 43eb,1f,0,7
SPIWrite 43ea,fe,0,7
SPIWrite 43ed,00,0,7
SPIWrite 43ec,60,0,7
SPIWrite 43ef,10,0,7
SPIWrite 43ee,00,0,7
SPIWrite 43f1,68,0,7
SPIWrite 43f0,64,0,7
SPIWrite 43f3,92,0,7
SPIWrite 43f2,30,0,7
SPIWrite 43f5,00,0,7
```

```
SPIWrite 43f4,00,0,7
SPIWrite 43f7,6d,0,7
SPIWrite 43f6,83,0,7
SPIWrite 43f9,db,0,7
SPIWrite 43f8,6c,0,7
SPIWrite 43fb,42,0,7
SPIWrite 43fa,6e,0,7
SPIWrite 43fd,62,0,7
SPIWrite 43fc,78,0,7
SPIWrite 43ff,08,0,7
SPIWrite 43fe,c8,0,7
SPIWrite 0016,60,0,7  //serdes_jesd=0x3;    Address(0x16[7:5])
SPIWrite 7007,00,0,7  //BUS_WIDTH_LANE0=0x0;
     Address(0x9803[7:0])
SPIWrite 7006,00,0,7
SPIWrite 7007,00,0,7  //BUS_WIDTH_LANE1=0x0;
     Address(0x9803[7:1])
SPIWrite 7006,00,0,7
SPIWrite 7007,00,0,7  //BUS_WIDTH_LANE2=0x0;
     Address(0x9803[7:2])
SPIWrite 7006,00,0,7
SPIWrite 7007,00,0,7  //BUS_WIDTH_LANE3=0x0;
     Address(0x9803[7:3])
SPIWrite 7006,00,0,7
SPIWrite 0016,00,0,7  //serdes_jesd=0x0;    Address(0x16[7:5])

//END: Done configuring the SERDES


//STEP: serdesConfig/step3

//START: Loading Serdes Firmware.

SPIWrite 0018,20,5,5  //macro=0x1;     Address(0x18[7:5])
SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0x10300;
     Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,01,0,7
SPIWrite 00a1,03,0,7
SPIWrite 00a0,00,0,7
SPIWrite 0193,79,0,7  //MACRO_OPCODE=0x79;
     Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2
```

```
//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
      Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
      Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1
```

```
SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0x10301;
     Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,01,0,7
SPIWrite 00a1,03,0,7
SPIWrite 00a0,01,0,7
SPIWrite 0193,79,0,7  //MACRO_OPCODE=0x79;
     Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
     Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
     Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
     Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7
```

```
//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIWrite 0018,00,0,7  //macro=0x0;     Address(0x18[7:5])
SPIWrite 0016,60,0,7  //serdes_jesd=0x3;    Address(0x16[7:5])
SPIWrite 702d,00,0,7
SPIWrite 702c,05,0,7
SPIWrite 7025,00,0,7
SPIWrite 7024,08,0,7
SPIWrite 702b,e0,0,7
SPIWrite 702a,20,0,7

WAIT 0.01
SPIWrite 702d,00,0,7
SPIWrite 702c,02,0,7
SPIWrite 7025,00,0,7
SPIWrite 7024,50,0,7
SPIWrite 702b,e0,0,7
SPIWrite 702a,20,0,7

WAIT 0.01
SPIWrite 701b,07,0,7  //DOMAIN_RESET=0x777;
      Address(0x980d[3:0],0x980e[7:0])
SPIWrite 701a,77,0,7
SPIWrite 701b,00,0,7  //DOMAIN_RESET=0x0;
      Address(0x980d[3:0],0x980e[7:0])
SPIWrite 701a,00,0,7

WAIT 5
SPIWrite 0016,00,0,7  //serdes_jesd=0x0;    Address(0x16[7:5])

//END: Done loading Serdes Firmware.


//STEP: topConfig/step0

//START: Setting Top Control Modes

SPIWrite 0015,80,0,7  //timing_controller=0x1;
      Address(0x15[7:7])
SPIWrite 0081,00,0,7  //fdd_mode=0x0;  Address(0x81[7:0])
SPIWrite 0080,01,0,7  //mode_2t2r=0x1;      Address(0x80[7:0])
SPIWrite 008c,01,0,7  //use_per_ch_txab_tdd=0x1;
      Address(0x8c[7:0])
SPIWrite 008d,01,0,7  //use_per_ch_txcd_tdd=0x1;
      Address(0x8d[7:0])
SPIWrite 00a0,01,0,7  //use_per_ch_rxab_tdd=0x1;
      Address(0xa0[7:0])
SPIWrite 00a1,01,0,7  //use_per_ch_rxcd_tdd=0x1;
      Address(0xa1[7:0])
SPIWrite 0015,00,0,7  //timing_controller=0x0;
```

```
      Address(0x15[7:7])
SPIWrite 0015,02,0,7  //ana_4t4r=0x1; Address(0x15[7:1])
SPIWrite 0129,00,0,7  //Property_108h_11_8=0x0;
      Address(0x129[7:0])
SPIWrite 012a,00,0,7  //Property_108h_19_16=0x0;
      Address(0x12a[7:0])
SPIWrite 012b,00,0,7  //Property_108h_25_24=0x0;
      Address(0x12b[7:0])
SPIWrite 00dc,00,0,7  //Property_bch_1_0=0x0;
      Address(0xdc[7:0])
SPIWrite 00df,00,0,7  //Property_bch_25_24=0x0;
      Address(0xdf[7:0])
SPIWrite 00c4,00,0,7  //Property_a4h_1_0=0x0;
      Address(0xc4[7:0])
SPIWrite 00c7,00,0,7  //Property_a4h_25_24=0x0;
      Address(0xc7[7:0])
SPIWrite 00cc,00,0,7  //Property_ach_1_0=0x0;
      Address(0xcc[7:0])
SPIWrite 00cf,00,0,7  //Property_ach_25_24=0x0;
      Address(0xcf[7:0])
SPIWrite 0015,00,0,7  //ana_4t4r=0x0; Address(0x15[7:1])
SPIWrite 0015,80,0,7  //timing_controller=0x1;
      Address(0x15[7:7])
SPIWrite 0399,00,0,7  //Property_378h_15_0=0x0;
      Address(0x398[7:0],0x399[7:0],0x39a[7:0])
SPIWrite 0398,00,0,7
SPIWrite 039b,00,0,7  //Property_378h_31_16=0xe1;
      Address(0x39a[7:0],0x39b[7:0],0x39c[7:0])
SPIWrite 039a,e1,0,7
SPIWrite 0451,00,0,7  //Property_430h_15_0=0x0;
      Address(0x450[7:0],0x451[7:0],0x452[7:0])
SPIWrite 0450,00,0,7
SPIWrite 0453,00,0,7  //Property_430h_31_16=0xe1;
      Address(0x452[7:0],0x453[7:0],0x454[7:0])
SPIWrite 0452,e1,0,7
SPIWrite 0509,00,0,7  //Property_4e8h_15_0=0x0;
      Address(0x508[7:0],0x509[7:0],0x50a[7:0])
SPIWrite 0508,00,0,7
SPIWrite 050b,00,0,7  //Property_4e8h_31_16=0xe1;
      Address(0x50a[7:0],0x50b[7:0],0x50c[7:0])
SPIWrite 050a,e1,0,7
SPIWrite 05c1,00,0,7  //Property_5a0h_15_0=0x0;
      Address(0x5c0[7:0],0x5c1[7:0],0x5c2[7:0])
SPIWrite 05c0,00,0,7
SPIWrite 05c3,00,0,7  //Property_5a0h_31_16=0xe1;
      Address(0x5c2[7:0],0x5c3[7:0],0x5c4[7:0])
SPIWrite 05c2,e1,0,7
SPIWrite 0679,00,0,7  //Property_658h_15_0=0x0;
      Address(0x678[7:0],0x679[7:0],0x67a[7:0])
SPIWrite 0678,00,0,7
SPIWrite 067b,00,0,7  //Property_658h_31_16=0xe1;
      Address(0x67a[7:0],0x67b[7:0],0x67c[7:0])
```

```
SPIWrite 067a,e1,0,7
SPIWrite 0731,00,0,7  //Property_710h_15_0=0x0;
     Address(0x730[7:0],0x731[7:0],0x732[7:0])
SPIWrite 0730,00,0,7
SPIWrite 0733,00,0,7  //Property_710h_31_16=0xe1;
     Address(0x732[7:0],0x733[7:0],0x734[7:0])
SPIWrite 0732,e1,0,7

//END: Setting Top Control Modes

SPIWrite 0015,00,0,7  //timing_controller=0x0;
     Address(0x15[7:7])
SPIWrite 0015,40,0,7  //digtop=0x1;   Address(0x15[7:6])
SPIWrite 0180,00,0,7  //Property_160h_3_0=0x0;
     Address(0x180[7:0])
SPIWrite 0181,00,0,7  //Property_160h_11_8=0x0;
     Address(0x181[7:0])
SPIWrite 0015,00,0,7  //digtop=0x0;   Address(0x15[7:6])

//STEP: topConfig/step1
SPIWrite 0013,40,6,7  //dsa_page1=0x1;      Address(0x13[7:6])
SPIWrite 054e,00,0,0  //Property_52ch_16_16=0x0;
     Address(0x54e[7:0])
SPIWrite 0013,80,6,7  //dsa_page1=0x2;      Address(0x13[7:6])
SPIWrite 054e,00,0,0  //Property_52ch_16_16=0x0;
     Address(0x54e[7:0])
SPIWrite 0013,c0,0,7  //dsa_page1=0x3;      Address(0x13[7:6])
SPIWrite 0444,03,0,7
SPIWrite 0445,00,0,7
SPIWrite 0446,00,0,7
SPIWrite 0447,00,0,7
SPIWrite 0448,0b,0,7
SPIWrite 0449,84,0,7
SPIWrite 044a,00,0,7
SPIWrite 044b,00,0,7
SPIWrite 044c,1f,0,7
SPIWrite 044d,08,0,7
SPIWrite 044e,01,0,7
SPIWrite 044f,00,0,7
SPIWrite 0450,33,0,7
SPIWrite 0451,8c,0,7
SPIWrite 0452,01,0,7
SPIWrite 0453,00,0,7
SPIWrite 0454,47,0,7
SPIWrite 0455,90,0,7
SPIWrite 0456,02,0,7
SPIWrite 0457,00,0,7
SPIWrite 0458,5b,0,7
SPIWrite 0459,14,0,7
SPIWrite 045a,03,0,7
SPIWrite 045b,01,0,7
SPIWrite 045c,6f,0,7
```

```
SPIWrite 045d,18,0,7
SPIWrite 045e,04,0,7
SPIWrite 045f,01,0,7
SPIWrite 0460,83,0,7
SPIWrite 0461,9c,0,7
SPIWrite 0462,04,0,7
SPIWrite 0463,01,0,7
SPIWrite 0464,9b,0,7
SPIWrite 0465,a0,0,7
SPIWrite 0466,05,0,7
SPIWrite 0467,02,0,7
SPIWrite 0468,b3,0,7
SPIWrite 0469,a4,0,7
SPIWrite 046a,06,0,7
SPIWrite 046b,02,0,7
SPIWrite 046c,c7,0,7
SPIWrite 046d,a8,0,7
SPIWrite 046e,07,0,7
SPIWrite 046f,03,0,7
SPIWrite 0470,df,0,7
SPIWrite 0471,ac,0,7
SPIWrite 0472,08,0,7
SPIWrite 0473,03,0,7
SPIWrite 0474,f7,0,7
SPIWrite 0475,b0,0,7
SPIWrite 0476,09,0,7
SPIWrite 0477,04,0,7
SPIWrite 0478,17,0,7
SPIWrite 0479,b5,0,7
SPIWrite 047a,0a,0,7
SPIWrite 047b,04,0,7
SPIWrite 047c,37,0,7
SPIWrite 047d,b9,0,7
SPIWrite 047e,0b,0,7
SPIWrite 047f,04,0,7
SPIWrite 0480,4f,0,7
SPIWrite 0481,bd,0,7
SPIWrite 0482,0c,0,7
SPIWrite 0483,05,0,7
SPIWrite 0484,6b,0,7
SPIWrite 0485,c1,0,7
SPIWrite 0486,0d,0,7
SPIWrite 0487,07,0,7
SPIWrite 0488,87,0,7
SPIWrite 0489,c5,0,7
SPIWrite 048a,0e,0,7
SPIWrite 048b,07,0,7
SPIWrite 048c,9f,0,7
SPIWrite 048d,c9,0,7
SPIWrite 048e,0f,0,7
SPIWrite 048f,07,0,7
SPIWrite 0490,a7,0,7
```

```
SPIWrite 0491,49,0,7
SPIWrite 0492,10,0,7
SPIWrite 0493,07,0,7
SPIWrite 0494,bb,0,7
SPIWrite 0495,4d,0,7
SPIWrite 0496,11,0,7
SPIWrite 0497,08,0,7
SPIWrite 0498,d3,0,7
SPIWrite 0499,51,0,7
SPIWrite 049a,12,0,7
SPIWrite 049b,09,0,7
SPIWrite 049c,eb,0,7
SPIWrite 049d,55,0,7
SPIWrite 049e,13,0,7
SPIWrite 049f,0a,0,7
SPIWrite 04a0,0b,0,7
SPIWrite 04a1,da,0,7
SPIWrite 04a2,14,0,7
SPIWrite 04a3,0b,0,7
SPIWrite 04a4,23,0,7
SPIWrite 04a5,de,0,7
SPIWrite 04a6,15,0,7
SPIWrite 04a7,0c,0,7
SPIWrite 04a8,3b,0,7
SPIWrite 04a9,e2,0,7
SPIWrite 04aa,16,0,7
SPIWrite 04ab,0e,0,7
SPIWrite 04ac,4f,0,7
SPIWrite 04ad,66,0,7
SPIWrite 04ae,17,0,7
SPIWrite 04af,0e,0,7
SPIWrite 04b0,63,0,7
SPIWrite 04b1,ea,0,7
SPIWrite 04b2,17,0,7
SPIWrite 04b3,11,0,7
SPIWrite 04b4,77,0,7
SPIWrite 04b5,6e,0,7
SPIWrite 04b6,18,0,7
SPIWrite 04b7,11,0,7
SPIWrite 04b8,8b,0,7
SPIWrite 04b9,f2,0,7
SPIWrite 04ba,18,0,7
SPIWrite 04bb,13,0,7
SPIWrite 04bc,9f,0,7
SPIWrite 04bd,72,0,7
SPIWrite 04be,19,0,7
SPIWrite 04bf,15,0,7
SPIWrite 04c0,b3,0,7
SPIWrite 04c1,f6,0,7
SPIWrite 04c2,19,0,7
SPIWrite 04c3,16,0,7
SPIWrite 04c4,c3,0,7
```

```
SPIWrite 04c5,76,0,7
SPIWrite 04c6,1a,0,7
SPIWrite 04c7,18,0,7
SPIWrite 04c8,d7,0,7
SPIWrite 04c9,f6,0,7
SPIWrite 04ca,1a,0,7
SPIWrite 04cb,19,0,7
SPIWrite 04cc,eb,0,7
SPIWrite 04cd,76,0,7
SPIWrite 04ce,1b,0,7
SPIWrite 04cf,1b,0,7
SPIWrite 04d0,ff,0,7
SPIWrite 04d1,f6,0,7
SPIWrite 04d2,1b,0,7
SPIWrite 04d3,1d,0,7
SPIWrite 04d4,13,0,7
SPIWrite 04d5,77,0,7
SPIWrite 04d6,1c,0,7
SPIWrite 04d7,1f,0,7
SPIWrite 04d8,23,0,7
SPIWrite 04d9,f7,0,7
SPIWrite 04da,1c,0,7
SPIWrite 04db,1f,0,7
SPIWrite 04dc,33,0,7
SPIWrite 04dd,77,0,7
SPIWrite 04de,1d,0,7
SPIWrite 04df,1f,0,7
SPIWrite 04e0,3f,0,7
SPIWrite 04e1,f7,0,7
SPIWrite 04e2,1d,0,7
SPIWrite 04e3,1f,0,7
SPIWrite 04e4,4b,0,7
SPIWrite 04e5,77,0,7
SPIWrite 04e6,1e,0,7
SPIWrite 04e7,1f,0,7
SPIWrite 04e8,57,0,7
SPIWrite 04e9,f7,0,7
SPIWrite 04ea,1e,0,7
SPIWrite 04eb,1f,0,7
SPIWrite 04ec,5f,0,7
SPIWrite 04ed,77,0,7
SPIWrite 04ee,1f,0,7
SPIWrite 04ef,1f,0,7
SPIWrite 04f0,67,0,7
SPIWrite 04f1,f7,0,7
SPIWrite 04f2,1f,0,7
SPIWrite 04f3,1f,0,7
SPIWrite 04f4,73,0,7
SPIWrite 04f5,f7,0,7
SPIWrite 04f6,1f,0,7
SPIWrite 04f7,1f,0,7
SPIWrite 04f8,7b,0,7
```

```
SPIWrite 04f9,f7,0,7
SPIWrite 04fa,1f,0,7
SPIWrite 04fb,1f,0,7
SPIWrite 04fc,87,0,7
SPIWrite 04fd,f7,0,7
SPIWrite 04fe,1f,0,7
SPIWrite 04ff,1f,0,7
SPIWrite 0500,8f,0,7
SPIWrite 0501,f7,0,7
SPIWrite 0502,1f,0,7
SPIWrite 0503,1f,0,7
SPIWrite 0504,97,0,7
SPIWrite 0505,f7,0,7
SPIWrite 0506,1f,0,7
SPIWrite 0507,1f,0,7
SPIWrite 0508,9b,0,7
SPIWrite 0509,f7,0,7
SPIWrite 050a,1f,0,7
SPIWrite 050b,1f,0,7
SPIWrite 0744,03,0,7
SPIWrite 0745,00,0,7
SPIWrite 0746,00,0,7
SPIWrite 0747,00,0,7
SPIWrite 0748,0b,0,7
SPIWrite 0749,84,0,7
SPIWrite 074a,00,0,7
SPIWrite 074b,00,0,7
SPIWrite 074c,1f,0,7
SPIWrite 074d,08,0,7
SPIWrite 074e,01,0,7
SPIWrite 074f,00,0,7
SPIWrite 0750,33,0,7
SPIWrite 0751,8c,0,7
SPIWrite 0752,01,0,7
SPIWrite 0753,00,0,7
SPIWrite 0754,47,0,7
SPIWrite 0755,90,0,7
SPIWrite 0756,02,0,7
SPIWrite 0757,00,0,7
SPIWrite 0758,5b,0,7
SPIWrite 0759,14,0,7
SPIWrite 075a,03,0,7
SPIWrite 075b,01,0,7
SPIWrite 075c,6f,0,7
SPIWrite 075d,18,0,7
SPIWrite 075e,04,0,7
SPIWrite 075f,01,0,7
SPIWrite 0760,83,0,7
SPIWrite 0761,9c,0,7
SPIWrite 0762,04,0,7
SPIWrite 0763,01,0,7
SPIWrite 0764,9b,0,7
```

```
SPIWrite 0765,a0,0,7
SPIWrite 0766,05,0,7
SPIWrite 0767,02,0,7
SPIWrite 0768,b3,0,7
SPIWrite 0769,a4,0,7
SPIWrite 076a,06,0,7
SPIWrite 076b,02,0,7
SPIWrite 076c,c7,0,7
SPIWrite 076d,a8,0,7
SPIWrite 076e,07,0,7
SPIWrite 076f,03,0,7
SPIWrite 0770,df,0,7
SPIWrite 0771,ac,0,7
SPIWrite 0772,08,0,7
SPIWrite 0773,03,0,7
SPIWrite 0774,f7,0,7
SPIWrite 0775,b0,0,7
SPIWrite 0776,09,0,7
SPIWrite 0777,04,0,7
SPIWrite 0778,17,0,7
SPIWrite 0779,b5,0,7
SPIWrite 077a,0a,0,7
SPIWrite 077b,04,0,7
SPIWrite 077c,37,0,7
SPIWrite 077d,b9,0,7
SPIWrite 077e,0b,0,7
SPIWrite 077f,04,0,7
SPIWrite 0780,4f,0,7
SPIWrite 0781,bd,0,7
SPIWrite 0782,0c,0,7
SPIWrite 0783,05,0,7
SPIWrite 0784,6b,0,7
SPIWrite 0785,c1,0,7
SPIWrite 0786,0d,0,7
SPIWrite 0787,07,0,7
SPIWrite 0788,87,0,7
SPIWrite 0789,c5,0,7
SPIWrite 078a,0e,0,7
SPIWrite 078b,07,0,7
SPIWrite 078c,9f,0,7
SPIWrite 078d,c9,0,7
SPIWrite 078e,0f,0,7
SPIWrite 078f,07,0,7
SPIWrite 0790,a7,0,7
SPIWrite 0791,49,0,7
SPIWrite 0792,10,0,7
SPIWrite 0793,07,0,7
SPIWrite 0794,bb,0,7
SPIWrite 0795,4d,0,7
SPIWrite 0796,11,0,7
SPIWrite 0797,08,0,7
SPIWrite 0798,d3,0,7
```

```
SPIWrite 0799,51,0,7
SPIWrite 079a,12,0,7
SPIWrite 079b,09,0,7
SPIWrite 079c,eb,0,7
SPIWrite 079d,55,0,7
SPIWrite 079e,13,0,7
SPIWrite 079f,0a,0,7
SPIWrite 07a0,0b,0,7
SPIWrite 07a1,da,0,7
SPIWrite 07a2,14,0,7
SPIWrite 07a3,0b,0,7
SPIWrite 07a4,23,0,7
SPIWrite 07a5,de,0,7
SPIWrite 07a6,15,0,7
SPIWrite 07a7,0c,0,7
SPIWrite 07a8,3b,0,7
SPIWrite 07a9,e2,0,7
SPIWrite 07aa,16,0,7
SPIWrite 07ab,0e,0,7
SPIWrite 07ac,4f,0,7
SPIWrite 07ad,66,0,7
SPIWrite 07ae,17,0,7
SPIWrite 07af,0e,0,7
SPIWrite 07b0,63,0,7
SPIWrite 07b1,ea,0,7
SPIWrite 07b2,17,0,7
SPIWrite 07b3,11,0,7
SPIWrite 07b4,77,0,7
SPIWrite 07b5,6e,0,7
SPIWrite 07b6,18,0,7
SPIWrite 07b7,11,0,7
SPIWrite 07b8,8b,0,7
SPIWrite 07b9,f2,0,7
SPIWrite 07ba,18,0,7
SPIWrite 07bb,13,0,7
SPIWrite 07bc,9f,0,7
SPIWrite 07bd,72,0,7
SPIWrite 07be,19,0,7
SPIWrite 07bf,15,0,7
SPIWrite 07c0,b3,0,7
SPIWrite 07c1,f6,0,7
SPIWrite 07c2,19,0,7
SPIWrite 07c3,16,0,7
SPIWrite 07c4,c3,0,7
SPIWrite 07c5,76,0,7
SPIWrite 07c6,1a,0,7
SPIWrite 07c7,18,0,7
SPIWrite 07c8,d7,0,7
SPIWrite 07c9,f6,0,7
SPIWrite 07ca,1a,0,7
SPIWrite 07cb,19,0,7
SPIWrite 07cc,eb,0,7
```

```
SPIWrite 07cd,76,0,7
SPIWrite 07ce,1b,0,7
SPIWrite 07cf,1b,0,7
SPIWrite 07d0,ff,0,7
SPIWrite 07d1,f6,0,7
SPIWrite 07d2,1b,0,7
SPIWrite 07d3,1d,0,7
SPIWrite 07d4,13,0,7
SPIWrite 07d5,77,0,7
SPIWrite 07d6,1c,0,7
SPIWrite 07d7,1f,0,7
SPIWrite 07d8,23,0,7
SPIWrite 07d9,f7,0,7
SPIWrite 07da,1c,0,7
SPIWrite 07db,1f,0,7
SPIWrite 07dc,33,0,7
SPIWrite 07dd,77,0,7
SPIWrite 07de,1d,0,7
SPIWrite 07df,1f,0,7
SPIWrite 07e0,3f,0,7
SPIWrite 07e1,f7,0,7
SPIWrite 07e2,1d,0,7
SPIWrite 07e3,1f,0,7
SPIWrite 07e4,4b,0,7
SPIWrite 07e5,77,0,7
SPIWrite 07e6,1e,0,7
SPIWrite 07e7,1f,0,7
SPIWrite 07e8,57,0,7
SPIWrite 07e9,f7,0,7
SPIWrite 07ea,1e,0,7
SPIWrite 07eb,1f,0,7
SPIWrite 07ec,5f,0,7
SPIWrite 07ed,77,0,7
SPIWrite 07ee,1f,0,7
SPIWrite 07ef,1f,0,7
SPIWrite 07f0,67,0,7
SPIWrite 07f1,f7,0,7
SPIWrite 07f2,1f,0,7
SPIWrite 07f3,1f,0,7
SPIWrite 07f4,73,0,7
SPIWrite 07f5,f7,0,7
SPIWrite 07f6,1f,0,7
SPIWrite 07f7,1f,0,7
SPIWrite 07f8,7b,0,7
SPIWrite 07f9,f7,0,7
SPIWrite 07fa,1f,0,7
SPIWrite 07fb,1f,0,7
SPIWrite 07fc,87,0,7
SPIWrite 07fd,f7,0,7
SPIWrite 07fe,1f,0,7
SPIWrite 07ff,1f,0,7
SPIWrite 0800,8f,0,7
```

```
SPIWrite 0801,f7,0,7
SPIWrite 0802,1f,0,7
SPIWrite 0803,1f,0,7
SPIWrite 0804,97,0,7
SPIWrite 0805,f7,0,7
SPIWrite 0806,1f,0,7
SPIWrite 0807,1f,0,7
SPIWrite 0808,9b,0,7
SPIWrite 0809,f7,0,7
SPIWrite 080a,1f,0,7
SPIWrite 080b,1f,0,7
SPIWrite 0844,03,0,7
SPIWrite 0845,00,0,7
SPIWrite 0846,00,0,7
SPIWrite 0847,00,0,7
SPIWrite 0848,0b,0,7
SPIWrite 0849,84,0,7
SPIWrite 084a,00,0,7
SPIWrite 084b,00,0,7
SPIWrite 084c,1f,0,7
SPIWrite 084d,08,0,7
SPIWrite 084e,01,0,7
SPIWrite 084f,00,0,7
SPIWrite 0850,33,0,7
SPIWrite 0851,8c,0,7
SPIWrite 0852,01,0,7
SPIWrite 0853,00,0,7
SPIWrite 0854,47,0,7
SPIWrite 0855,90,0,7
SPIWrite 0856,02,0,7
SPIWrite 0857,00,0,7
SPIWrite 0858,5b,0,7
SPIWrite 0859,14,0,7
SPIWrite 085a,03,0,7
SPIWrite 085b,01,0,7
SPIWrite 085c,6f,0,7
SPIWrite 085d,18,0,7
SPIWrite 085e,04,0,7
SPIWrite 085f,01,0,7
SPIWrite 0860,83,0,7
SPIWrite 0861,9c,0,7
SPIWrite 0862,04,0,7
SPIWrite 0863,01,0,7
SPIWrite 0864,9b,0,7
SPIWrite 0865,a0,0,7
SPIWrite 0866,05,0,7
SPIWrite 0867,02,0,7
SPIWrite 0868,b3,0,7
SPIWrite 0869,a4,0,7
SPIWrite 086a,06,0,7
SPIWrite 086b,02,0,7
SPIWrite 086c,c7,0,7
```

```
SPIWrite 086d,a8,0,7
SPIWrite 086e,07,0,7
SPIWrite 086f,03,0,7
SPIWrite 0870,df,0,7
SPIWrite 0871,ac,0,7
SPIWrite 0872,08,0,7
SPIWrite 0873,03,0,7
SPIWrite 0874,f7,0,7
SPIWrite 0875,b0,0,7
SPIWrite 0876,09,0,7
SPIWrite 0877,04,0,7
SPIWrite 0878,17,0,7
SPIWrite 0879,b5,0,7
SPIWrite 087a,0a,0,7
SPIWrite 087b,04,0,7
SPIWrite 087c,37,0,7
SPIWrite 087d,b9,0,7
SPIWrite 087e,0b,0,7
SPIWrite 087f,04,0,7
SPIWrite 0880,4f,0,7
SPIWrite 0881,bd,0,7
SPIWrite 0882,0c,0,7
SPIWrite 0883,05,0,7
SPIWrite 0884,6b,0,7
SPIWrite 0885,c1,0,7
SPIWrite 0886,0d,0,7
SPIWrite 0887,07,0,7
SPIWrite 0888,87,0,7
SPIWrite 0889,c5,0,7
SPIWrite 088a,0e,0,7
SPIWrite 088b,07,0,7
SPIWrite 088c,9f,0,7
SPIWrite 088d,c9,0,7
SPIWrite 088e,0f,0,7
SPIWrite 088f,07,0,7
SPIWrite 0890,a7,0,7
SPIWrite 0891,49,0,7
SPIWrite 0892,10,0,7
SPIWrite 0893,07,0,7
SPIWrite 0894,bb,0,7
SPIWrite 0895,4d,0,7
SPIWrite 0896,11,0,7
SPIWrite 0897,08,0,7
SPIWrite 0898,d3,0,7
SPIWrite 0899,51,0,7
SPIWrite 089a,12,0,7
SPIWrite 089b,09,0,7
SPIWrite 089c,eb,0,7
SPIWrite 089d,55,0,7
SPIWrite 089e,13,0,7
SPIWrite 089f,0a,0,7
SPIWrite 08a0,0b,0,7
```

```
SPIWrite 08a1,da,0,7
SPIWrite 08a2,14,0,7
SPIWrite 08a3,0b,0,7
SPIWrite 08a4,23,0,7
SPIWrite 08a5,de,0,7
SPIWrite 08a6,15,0,7
SPIWrite 08a7,0c,0,7
SPIWrite 08a8,3b,0,7
SPIWrite 08a9,e2,0,7
SPIWrite 08aa,16,0,7
SPIWrite 08ab,0e,0,7
SPIWrite 08ac,4f,0,7
SPIWrite 08ad,66,0,7
SPIWrite 08ae,17,0,7
SPIWrite 08af,0e,0,7
SPIWrite 08b0,63,0,7
SPIWrite 08b1,ea,0,7
SPIWrite 08b2,17,0,7
SPIWrite 08b3,11,0,7
SPIWrite 08b4,77,0,7
SPIWrite 08b5,6e,0,7
SPIWrite 08b6,18,0,7
SPIWrite 08b7,11,0,7
SPIWrite 08b8,8b,0,7
SPIWrite 08b9,f2,0,7
SPIWrite 08ba,18,0,7
SPIWrite 08bb,13,0,7
SPIWrite 08bc,9f,0,7
SPIWrite 08bd,72,0,7
SPIWrite 08be,19,0,7
SPIWrite 08bf,15,0,7
SPIWrite 08c0,b3,0,7
SPIWrite 08c1,f6,0,7
SPIWrite 08c2,19,0,7
SPIWrite 08c3,16,0,7
SPIWrite 08c4,c3,0,7
SPIWrite 08c5,76,0,7
SPIWrite 08c6,1a,0,7
SPIWrite 08c7,18,0,7
SPIWrite 08c8,d7,0,7
SPIWrite 08c9,f6,0,7
SPIWrite 08ca,1a,0,7
SPIWrite 08cb,19,0,7
SPIWrite 08cc,eb,0,7
SPIWrite 08cd,76,0,7
SPIWrite 08ce,1b,0,7
SPIWrite 08cf,1b,0,7
SPIWrite 08d0,ff,0,7
SPIWrite 08d1,f6,0,7
SPIWrite 08d2,1b,0,7
SPIWrite 08d3,1d,0,7
SPIWrite 08d4,13,0,7
```

```
SPIWrite 08d5,77,0,7
SPIWrite 08d6,1c,0,7
SPIWrite 08d7,1f,0,7
SPIWrite 08d8,23,0,7
SPIWrite 08d9,f7,0,7
SPIWrite 08da,1c,0,7
SPIWrite 08db,1f,0,7
SPIWrite 08dc,33,0,7
SPIWrite 08dd,77,0,7
SPIWrite 08de,1d,0,7
SPIWrite 08df,1f,0,7
SPIWrite 08e0,3f,0,7
SPIWrite 08e1,f7,0,7
SPIWrite 08e2,1d,0,7
SPIWrite 08e3,1f,0,7
SPIWrite 08e4,4b,0,7
SPIWrite 08e5,77,0,7
SPIWrite 08e6,1e,0,7
SPIWrite 08e7,1f,0,7
SPIWrite 08e8,57,0,7
SPIWrite 08e9,f7,0,7
SPIWrite 08ea,1e,0,7
SPIWrite 08eb,1f,0,7
SPIWrite 08ec,5f,0,7
SPIWrite 08ed,77,0,7
SPIWrite 08ee,1f,0,7
SPIWrite 08ef,1f,0,7
SPIWrite 08f0,67,0,7
SPIWrite 08f1,f7,0,7
SPIWrite 08f2,1f,0,7
SPIWrite 08f3,1f,0,7
SPIWrite 08f4,73,0,7
SPIWrite 08f5,f7,0,7
SPIWrite 08f6,1f,0,7
SPIWrite 08f7,1f,0,7
SPIWrite 08f8,7b,0,7
SPIWrite 08f9,f7,0,7
SPIWrite 08fa,1f,0,7
SPIWrite 08fb,1f,0,7
SPIWrite 08fc,87,0,7
SPIWrite 08fd,f7,0,7
SPIWrite 08fe,1f,0,7
SPIWrite 08ff,1f,0,7
SPIWrite 0900,8f,0,7
SPIWrite 0901,f7,0,7
SPIWrite 0902,1f,0,7
SPIWrite 0903,1f,0,7
SPIWrite 0904,97,0,7
SPIWrite 0905,f7,0,7
SPIWrite 0906,1f,0,7
SPIWrite 0907,1f,0,7
SPIWrite 0908,9b,0,7
```

```
SPIWrite 0909,f7,0,7
SPIWrite 090a,1f,0,7
SPIWrite 090b,1f,0,7
SPIWrite 00d1,06,0,7  //dig_gain_range=0x6;
     Address(0xd1[7:0])
SPIWrite 0124,01,0,7  //spi_agc_dsa_A=0x1;  Address(0x124[7:0])
SPIWrite 0124,00,0,7  //spi_agc_dsa_A=0x0;  Address(0x124[7:0])
SPIWrite 0174,01,0,7  //spi_agc_dsa_B=0x1;  Address(0x174[7:0])
SPIWrite 0174,00,0,7  //spi_agc_dsa_B=0x0;  Address(0x174[7:0])
SPIWrite 0013,00,0,7  //dsa_page1=0x0;      Address(0x13[7:6])
SPIWrite 0013,10,0,7  //dsa_page0=0x1;      Address(0x13[7:4])
SPIWrite 006c,01,0,7  //spi_agc_dsa_fb=0x1;
     Address(0x6c[7:0])
SPIWrite 006c,00,0,7  //spi_agc_dsa_fb=0x0;
     Address(0x6c[7:0])
SPIWrite 0013,00,0,7  //dsa_page0=0x0;      Address(0x13[7:4])
SPIWrite 0013,80,0,7  //dsa_page1=0x2;      Address(0x13[7:6])
SPIWrite 00d1,06,0,7  //dig_gain_range=0x6;
     Address(0xd1[7:0])
SPIWrite 0124,01,0,7  //spi_agc_dsa_A=0x1;  Address(0x124[7:0])
SPIWrite 0124,00,0,7  //spi_agc_dsa_A=0x0;  Address(0x124[7:0])
SPIWrite 0174,01,0,7  //spi_agc_dsa_B=0x1;  Address(0x174[7:0])
SPIWrite 0174,00,0,7  //spi_agc_dsa_B=0x0;  Address(0x174[7:0])
SPIWrite 0013,00,0,7  //dsa_page1=0x0;      Address(0x13[7:6])
SPIWrite 0013,20,0,7  //dsa_page0=0x2;      Address(0x13[7:4])
SPIWrite 006c,01,0,7  //spi_agc_dsa_fb=0x1;
     Address(0x6c[7:0])
SPIWrite 006c,00,0,7  //spi_agc_dsa_fb=0x0;
     Address(0x6c[7:0])
SPIWrite 0013,00,0,7  //dsa_page0=0x0;      Address(0x13[7:4])
SPIWrite 0015,40,0,7  //digtop=0x1;   Address(0x15[7:6])
SPIWrite 0940,00,0,7  //Property_920h_2_0=0x0;
     Address(0x940[7:0])
SPIWrite 0941,00,0,7  //Property_920h_10_8=0x0;
     Address(0x941[7:0])
SPIWrite 0015,00,0,7  //digtop=0x0;   Address(0x15[7:6])
SPIWrite 0013,c0,0,7  //dsa_page1=0x3;      Address(0x13[7:6])
SPIWrite 0545,06,0,7  //Property_524h_13_8=0x6;
     Address(0x545[7:0])
SPIWrite 054a,06,0,7  //Property_528h_21_16=0x6;
     Address(0x54a[7:0])
SPIWrite 05a4,30,0,7  //Property_584h_5_0=0x30;
     Address(0x5a4[7:0])
SPIWrite 05a5,18,0,7  //Property_584h_13_8=0x18;
     Address(0x5a5[7:0])
SPIWrite 0544,18,0,7  //Property_524h_5_0=0x18;
     Address(0x544[7:0])
SPIWrite 056e,00,0,7  //Property_54ch_17_0=0x12;
     Address(0x56c[1:0],0x56d[1:0],0x56e[7:0])
SPIWrite 056d,00,0,7
SPIWrite 056c,12,0,7
SPIWrite 0572,00,0,7  //Property_550h_22_0=0x7;
```

```
     Address(0x570[6:0],0x571[6:0],0x572[7:0])
SPIWrite 0571,00,0,7
SPIWrite 0570,07,0,7
SPIWrite 0576,00,0,7  //Property_554h_17_0=0x0;
     Address(0x574[1:0],0x575[1:0],0x576[7:0])
SPIWrite 0575,00,0,7
SPIWrite 0574,00,0,7
SPIWrite 057e,00,0,7  //Property_55ch_21_0=0x5c;
     Address(0x57c[5:0],0x57d[5:0],0x57e[7:0])
SPIWrite 057d,00,0,7
SPIWrite 057c,5c,0,7
SPIWrite 057a,00,0,7  //Property_558h_22_0=0x1;
     Address(0x578[6:0],0x579[6:0],0x57a[7:0])
SPIWrite 0579,00,0,7
SPIWrite 0578,01,0,7
SPIWrite 0596,00,0,7  //Property_574h_22_0=0x7;
     Address(0x594[6:0],0x595[6:0],0x596[7:0])
SPIWrite 0595,00,0,7
SPIWrite 0594,07,0,7
SPIWrite 059a,00,0,7  //Property_578h_22_0=0x7;
     Address(0x598[6:0],0x599[6:0],0x59a[7:0])
SPIWrite 0599,00,0,7
SPIWrite 0598,07,0,7
SPIWrite 0556,00,0,7  //Property_534h_17_0=0x12;
     Address(0x554[1:0],0x555[1:0],0x556[7:0])
SPIWrite 0555,00,0,7
SPIWrite 0554,12,0,7
SPIWrite 055a,00,0,7  //Property_538h_22_0=0x7;
     Address(0x558[6:0],0x559[6:0],0x55a[7:0])
SPIWrite 0559,00,0,7
SPIWrite 0558,07,0,7
SPIWrite 055e,00,0,7  //Property_53ch_17_0=0x0;
     Address(0x55c[1:0],0x55d[1:0],0x55e[7:0])
SPIWrite 055d,00,0,7
SPIWrite 055c,00,0,7
SPIWrite 0566,00,0,7  //Property_544h_21_0=0x5c;
     Address(0x564[5:0],0x565[5:0],0x566[7:0])
SPIWrite 0565,00,0,7
SPIWrite 0564,5c,0,7
SPIWrite 0562,00,0,7  //Property_540h_22_0=0x1;
     Address(0x560[6:0],0x561[6:0],0x562[7:0])
SPIWrite 0561,00,0,7
SPIWrite 0560,01,0,7
SPIWrite 058e,00,0,7  //Property_56ch_22_0=0x7;
     Address(0x58c[6:0],0x58d[6:0],0x58e[7:0])
SPIWrite 058d,00,0,7
SPIWrite 058c,07,0,7
SPIWrite 0592,00,0,7  //Property_570h_22_0=0x7;
     Address(0x590[6:0],0x591[6:0],0x592[7:0])
SPIWrite 0591,00,0,7
SPIWrite 0590,07,0,7
SPIWrite 0577,01,0,7  //Property_554h_24_24=0x1;
```

```
      Address(0x577[7:0])
SPIWrite 056f,00,0,7  //Property_54ch_24_24=0x0;
      Address(0x56f[7:0])
SPIWrite 05a1,01,0,7  //Property_580h_8_8=0x1;
      Address(0x5a1[7:0])
SPIWrite 055f,01,0,7  //Property_53ch_24_24=0x1;
      Address(0x55f[7:0])
SPIWrite 0557,00,0,7  //Property_534h_24_24=0x0;
      Address(0x557[7:0])
SPIWrite 05a0,00,0,7  //Property_580h_0_0=0x0;
      Address(0x5a0[7:0])
SPIWrite 05a9,01,0,7  //Property_588h_8_8=0x1;
      Address(0x5a9[7:0])
SPIWrite 054a,06,0,7  //Property_528h_21_16=0x6;
      Address(0x54a[7:0])
SPIWrite 0013,00,0,7  //dsa_page1=0x0;      Address(0x13[7:6])

//STEP: topConfig/step2
SPIWrite 0013,10,0,7  //dsa_page0=0x1;      Address(0x13[7:4])
SPIWrite 00d0,18,0,7  //txa_dsa_dig0_gain=0x18;
      Address(0xd0[7:0],0xd1[7:0])
SPIWrite 00d4,18,0,7  //txb_dsa_dig0_gain=0x18;
      Address(0xd4[7:0],0xd5[7:0])
SPIWrite 0013,20,0,7  //dsa_page0=0x2;      Address(0x13[7:4])
SPIWrite 00d0,18,0,7  //txa_dsa_dig0_gain=0x18;
      Address(0xd0[7:0],0xd1[7:0])
SPIWrite 00d4,18,0,7  //txb_dsa_dig0_gain=0x18;
      Address(0xd4[7:0],0xd5[7:0])
SPIWrite 0013,00,0,7  //dsa_page0=0x0;      Address(0x13[7:4])
SPIWrite 0013,c0,0,7  //dsa_page1=0x3;      Address(0x13[7:6])
SPIWrite 0a37,40,0,7
SPIWrite 0a3f,40,0,7
SPIWrite 0a4f,40,0,7
SPIWrite 0a5f,40,0,7
SPIWrite 0a77,40,0,7
SPIWrite 0a7f,40,0,7
SPIWrite 0a97,40,0,7
SPIWrite 0a9f,40,0,7
SPIWrite 0aa7,40,0,7
SPIWrite 0aaf,40,0,7
SPIWrite 0c37,40,0,7
SPIWrite 0c3f,40,0,7
SPIWrite 0c4f,40,0,7
SPIWrite 0c5f,40,0,7
SPIWrite 0c77,40,0,7
SPIWrite 0c7f,40,0,7
SPIWrite 0c97,40,0,7
SPIWrite 0c9f,40,0,7
SPIWrite 0ca7,40,0,7
SPIWrite 0caf,40,0,7
SPIWrite 0013,00,0,7  //dsa_page1=0x0;      Address(0x13[7:6])
```

```
//STEP: sysConfig/step0

//START: Configuring RRF Mode to TOP MCU

SPIWrite 0018,20,0,7  //macro=0x1;    Address(0x18[7:5])
SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0x3;
     Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00,0,7
SPIWrite 00a1,00,0,7
SPIWrite 00a0,03,0,7
SPIWrite 0193,22,0,7  //MACRO_OPCODE=0x22;
     Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
     Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
     Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7
```

```
//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0xf020f;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,0f,0,7
SPIWrite 00a1,02,0,7
SPIWrite 00a0,0f,0,7
SPIWrite 0193,21,0,7  //MACRO_OPCODE=0x21;
      Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
      Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])
```

```
SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
      Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0x1;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00,0,7
SPIWrite 00a1,00,0,7
SPIWrite 00a0,01,0,7
SPIWrite 0193,2f,0,7  //MACRO_OPCODE=0x2f;
      Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00
```

```
//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
      Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0; Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
      Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])


//END: Configuring RRF Mode to TOP MCU

SPIWrite 0018,00,0,7  //macro=0x0;     Address(0x18[7:5])

//STEP: sysConfig/step1

//START: Configuring RX Chain Parameters to TOP MCU

SPIWrite 0018,20,0,7  //macro=0x1;     Address(0x18[7:5])
SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])
```

```
SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0x703;
     Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00,0,7
SPIWrite 00a1,07,0,7
SPIWrite 00a0,03,0,7
SPIWrite 0193,2c,0,7  //MACRO_OPCODE=0x2c;
     Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
     Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
     Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
     Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
```

```
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0x201;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00,0,7
SPIWrite 00a1,02,0,7
SPIWrite 00a0,01,0,7
SPIWrite 0193,29,0,7  //MACRO_OPCODE=0x29;
      Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
      Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
      Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])
```

```
SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0x101;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00,0,7
SPIWrite 00a1,01,0,7
SPIWrite 00a0,01,0,7
SPIWrite 0193,23,0,7  //MACRO_OPCODE=0x23;
      Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
      Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4
```

```
//Read     MACRO_ERROR_IN_OPCODE=0x0; Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
      Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,c7,0,7  //MACRO_OPERAND_REG0=0xc71c0301;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,1c,0,7
SPIWrite 00a1,03,0,7
SPIWrite 00a0,01,0,7
SPIWrite 00a7,c7,0,7  //MACRO_OPERAND_REG1=0xc71ca941;
      Address(0xa4[7:0],0xa5[7:0],0xa6[7:0],0xa7[7:0],0xa8[7:0])
SPIWrite 00a6,1c,0,7
SPIWrite 00a5,a9,0,7
SPIWrite 00a4,41,0,7
SPIWrite 00ab,00,0,7  //MACRO_OPERAND_REG2=0xe1b1;
      Address(0xa8[7:0],0xa9[7:0],0xaa[7:0],0xab[7:0],0xac[7:0])
SPIWrite 00aa,00,0,7
SPIWrite 00a9,e1,0,7
SPIWrite 00a8,b1,0,7
SPIWrite 00af,c7,0,7  //MACRO_OPERAND_REG3=0xc71cb9c0;
```

```
     Address(0xac[7:0],0xad[7:0],0xae[7:0],0xaf[7:0],0xb0[7:0])
SPIWrite 00ae,1c,0,7
SPIWrite 00ad,b9,0,7
SPIWrite 00ac,c0,0,7
SPIWrite 00b3,00,0,7  //MACRO_OPERAND_REG4=0xe1b1;
     Address(0xb0[7:0],0xb1[7:0],0xb2[7:0],0xb3[7:0],0xb4[7:0])
SPIWrite 00b2,00,0,7
SPIWrite 00b1,e1,0,7
SPIWrite 00b0,b1,0,7
SPIWrite 0193,31,0,7  //MACRO_OPCODE=0x31;
     Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
     Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
     Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
     Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
```

```
SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0x202;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00,0,7
SPIWrite 00a1,02,0,7
SPIWrite 00a0,02,0,7
SPIWrite 0193,29,0,7  //MACRO_OPCODE=0x29;
      Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
      Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
      Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])
```

```
SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0x102;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00,0,7
SPIWrite 00a1,01,0,7
SPIWrite 00a0,02,0,7
SPIWrite 0193,23,0,7  //MACRO_OPCODE=0x23;
      Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
      Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4
```

```
//Read     MACRO_ERROR_IN_OPCODE=0x0; Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
      Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,c7,0,7  //MACRO_OPERAND_REG0=0xc71c0302;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,1c,0,7
SPIWrite 00a1,03,0,7
SPIWrite 00a0,02,0,7
SPIWrite 00a7,c7,0,7  //MACRO_OPERAND_REG1=0xc71ca941;
      Address(0xa4[7:0],0xa5[7:0],0xa6[7:0],0xa7[7:0],0xa8[7:0])
SPIWrite 00a6,1c,0,7
SPIWrite 00a5,a9,0,7
SPIWrite 00a4,41,0,7
SPIWrite 00ab,00,0,7  //MACRO_OPERAND_REG2=0xe1b1;
      Address(0xa8[7:0],0xa9[7:0],0xaa[7:0],0xab[7:0],0xac[7:0])
SPIWrite 00aa,00,0,7
SPIWrite 00a9,e1,0,7
SPIWrite 00a8,b1,0,7
```

```
SPIWrite 00af,c7,0,7  //MACRO_OPERAND_REG3=0xc71cb9c0;
     Address(0xac[7:0],0xad[7:0],0xae[7:0],0xaf[7:0],0xb0[7:0])
SPIWrite 00ae,1c,0,7
SPIWrite 00ad,b9,0,7
SPIWrite 00ac,c0,0,7
SPIWrite 00b3,00,0,7  //MACRO_OPERAND_REG4=0xe1b1;
     Address(0xb0[7:0],0xb1[7:0],0xb2[7:0],0xb3[7:0],0xb4[7:0])
SPIWrite 00b2,00,0,7
SPIWrite 00b1,e1,0,7
SPIWrite 00b0,b1,0,7
SPIWrite 0193,31,0,7  //MACRO_OPCODE=0x31;
     Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1; Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
     Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0; Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
     Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
     Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
```

```
SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0x204;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00,0,7
SPIWrite 00a1,02,0,7
SPIWrite 00a0,04,0,7
SPIWrite 0193,29,0,7  //MACRO_OPCODE=0x29;
      Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
      Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
      Address(0xf0[7:5])

SPIRead 00f0,6,6
```

```
//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0x104;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00,0,7
SPIWrite 00a1,01,0,7
SPIWrite 00a0,04,0,7
SPIWrite 0193,23,0,7  //MACRO_OPCODE=0x23;
      Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
      Address(0xf1[7:0],0xf2[7:0])
```

```
SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0; Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
      Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,c7,0,7  //MACRO_OPERAND_REG0=0xc71c0304;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,1c,0,7
SPIWrite 00a1,03,0,7
SPIWrite 00a0,04,0,7
SPIWrite 00a7,c7,0,7  //MACRO_OPERAND_REG1=0xc71ca941;
      Address(0xa4[7:0],0xa5[7:0],0xa6[7:0],0xa7[7:0],0xa8[7:0])
SPIWrite 00a6,1c,0,7
SPIWrite 00a5,a9,0,7
SPIWrite 00a4,41,0,7
SPIWrite 00ab,00,0,7  //MACRO_OPERAND_REG2=0xe1b1;
      Address(0xa8[7:0],0xa9[7:0],0xaa[7:0],0xab[7:0],0xac[7:0])
SPIWrite 00aa,00,0,7
SPIWrite 00a9,e1,0,7
```

```
SPIWrite 00a8,b1,0,7
SPIWrite 00af,c7,0,7  //MACRO_OPERAND_REG3=0xc71cb9c0;
     Address(0xac[7:0],0xad[7:0],0xae[7:0],0xaf[7:0],0xb0[7:0])
SPIWrite 00ae,1c,0,7
SPIWrite 00ad,b9,0,7
SPIWrite 00ac,c0,0,7
SPIWrite 00b3,00,0,7  //MACRO_OPERAND_REG4=0xe1b1;
     Address(0xb0[7:0],0xb1[7:0],0xb2[7:0],0xb3[7:0],0xb4[7:0])
SPIWrite 00b2,00,0,7
SPIWrite 00b1,e1,0,7
SPIWrite 00b0,b1,0,7
SPIWrite 0193,31,0,7  //MACRO_OPCODE=0x31;
     Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1; Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
     Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0; Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
     Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
```

```
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0x208;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00,0,7
SPIWrite 00a1,02,0,7
SPIWrite 00a0,08,0,7
SPIWrite 0193,29,0,7  //MACRO_OPCODE=0x29;
      Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
      Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
      Address(0xf0[7:5])

SPIRead 00f0,6,6
```

```
//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0x108;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00,0,7
SPIWrite 00a1,01,0,7
SPIWrite 00a0,08,0,7
SPIWrite 0193,23,0,7  //MACRO_OPCODE=0x23;
      Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
      Address(0xf1[7:0],0xf2[7:0])
```

```
SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0; Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
      Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,c7,0,7  //MACRO_OPERAND_REG0=0xc71c0308;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,1c,0,7
SPIWrite 00a1,03,0,7
SPIWrite 00a0,08,0,7
SPIWrite 00a7,c7,0,7  //MACRO_OPERAND_REG1=0xc71ca941;
      Address(0xa4[7:0],0xa5[7:0],0xa6[7:0],0xa7[7:0],0xa8[7:0])
SPIWrite 00a6,1c,0,7
SPIWrite 00a5,a9,0,7
SPIWrite 00a4,41,0,7
SPIWrite 00ab,00,0,7  //MACRO_OPERAND_REG2=0xe1b1;
      Address(0xa8[7:0],0xa9[7:0],0xaa[7:0],0xab[7:0],0xac[7:0])
SPIWrite 00aa,00,0,7
```

```
SPIWrite 00a9,e1,0,7
SPIWrite 00a8,b1,0,7
SPIWrite 00af,c7,0,7  //MACRO_OPERAND_REG3=0xc71cb9c0;
     Address(0xac[7:0],0xad[7:0],0xae[7:0],0xaf[7:0],0xb0[7:0])
SPIWrite 00ae,1c,0,7
SPIWrite 00ad,b9,0,7
SPIWrite 00ac,c0,0,7
SPIWrite 00b3,00,0,7  //MACRO_OPERAND_REG4=0xe1b1;
     Address(0xb0[7:0],0xb1[7:0],0xb2[7:0],0xb3[7:0],0xb4[7:0])
SPIWrite 00b2,00,0,7
SPIWrite 00b1,e1,0,7
SPIWrite 00b0,b1,0,7
SPIWrite 0193,31,0,7  //MACRO_OPCODE=0x31;
     Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
     Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
     Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7
```

```
//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])


//END: Configuring RX Chain Parameters to TOP MCU

SPIWrite 0018,00,0,7  //macro=0x0;     Address(0x18[7:5])

//STEP: sysConfig/step2

//START: Configuring FB Chain Parameters to TOP MCU

SPIWrite 0018,20,0,7  //macro=0x1;     Address(0x18[7:5])
SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0x702;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00,0,7
SPIWrite 00a1,07,0,7
SPIWrite 00a0,02,0,7
SPIWrite 0193,2d,0,7  //MACRO_OPCODE=0x2d;
      Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
      Address(0xf1[7:0],0xf2[7:0])
```

```
SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0; Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
      Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0x401;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00,0,7
SPIWrite 00a1,04,0,7
SPIWrite 00a0,01,0,7
SPIWrite 0193,2a,0,7  //MACRO_OPCODE=0x2a;
      Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1; Address(0xf0[7:2])
```

```
SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
      Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
      Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0x301;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
```

```
SPIWrite 00a2,00,0,7
SPIWrite 00a1,03,0,7
SPIWrite 00a0,01,0,7
SPIWrite 00a7,00,0,7  //MACRO_OPERAND_REG1=0xb9c0;
     Address(0xa4[7:0],0xa5[7:0],0xa6[7:0],0xa7[7:0],0xa8[7:0])
SPIWrite 00a6,00,0,7
SPIWrite 00a5,b9,0,7
SPIWrite 00a4,c0,0,7
SPIWrite 00ab,00,0,7  //MACRO_OPERAND_REG2=0xb9c0;
     Address(0xa8[7:0],0xa9[7:0],0xaa[7:0],0xab[7:0],0xac[7:0])
SPIWrite 00aa,00,0,7
SPIWrite 00a9,b9,0,7
SPIWrite 00a8,c0,0,7
SPIWrite 00af,00,0,7  //MACRO_OPERAND_REG3=0xb9c0;
     Address(0xac[7:0],0xad[7:0],0xae[7:0],0xaf[7:0],0xb0[7:0])
SPIWrite 00ae,00,0,7
SPIWrite 00ad,b9,0,7
SPIWrite 00ac,c0,0,7
SPIWrite 00b3,00,0,7  //MACRO_OPERAND_REG4=0xb9c0;
     Address(0xb0[7:0],0xb1[7:0],0xb2[7:0],0xb3[7:0],0xb4[7:0])
SPIWrite 00b2,00,0,7
SPIWrite 00b1,b9,0,7
SPIWrite 00b0,c0,0,7
SPIWrite 0193,32,0,7  //MACRO_OPCODE=0x32;
     Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
     Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
     Address(0xf0[7:5])
```

```
SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0x402;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00,0,7
SPIWrite 00a1,04,0,7
SPIWrite 00a0,02,0,7
SPIWrite 0193,2a,0,7  //MACRO_OPCODE=0x2a;
      Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
```

```
      Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0; Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
      Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0x302;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00,0,7
SPIWrite 00a1,03,0,7
SPIWrite 00a0,02,0,7
SPIWrite 00a7,00,0,7  //MACRO_OPERAND_REG1=0xb9c0;
      Address(0xa4[7:0],0xa5[7:0],0xa6[7:0],0xa7[7:0],0xa8[7:0])
SPIWrite 00a6,00,0,7
SPIWrite 00a5,b9,0,7
SPIWrite 00a4,c0,0,7
SPIWrite 00ab,00,0,7  //MACRO_OPERAND_REG2=0xb9c0;
      Address(0xa8[7:0],0xa9[7:0],0xaa[7:0],0xab[7:0],0xac[7:0])
```

```
SPIWrite 00aa,00,0,7
SPIWrite 00a9,b9,0,7
SPIWrite 00a8,c0,0,7
SPIWrite 00af,00,0,7  //MACRO_OPERAND_REG3=0xb9c0;
     Address(0xac[7:0],0xad[7:0],0xae[7:0],0xaf[7:0],0xb0[7:0])
SPIWrite 00ae,00,0,7
SPIWrite 00ad,b9,0,7
SPIWrite 00ac,c0,0,7
SPIWrite 00b3,00,0,7  //MACRO_OPERAND_REG4=0xb9c0;
     Address(0xb0[7:0],0xb1[7:0],0xb2[7:0],0xb3[7:0],0xb4[7:0])
SPIWrite 00b2,00,0,7
SPIWrite 00b1,b9,0,7
SPIWrite 00b0,c0,0,7
SPIWrite 0193,32,0,7  //MACRO_OPCODE=0x32;
     Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
     Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
     Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7
```

```
//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
     Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
     Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])


//END: Configuring FB Chain Parameters to TOP MCU

SPIWrite 0018,00,0,7  //macro=0x0;     Address(0x18[7:5])

//STEP: sysConfig/step3

//START: Configuring TX Chain Parameters to TOP MCU

SPIWrite 0018,20,0,7  //macro=0x1;     Address(0x18[7:5])
SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0x0;
     Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00,0,7
SPIWrite 00a1,00,0,7
SPIWrite 00a0,00,0,7
SPIWrite 0193,8d,0,7  //MACRO_OPCODE=0x8d;
     Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
```

```
      Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0; Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
      Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0x0;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00,0,7
SPIWrite 00a1,00,0,7
SPIWrite 00a0,00,0,7
SPIWrite 0193,90,0,7  //MACRO_OPCODE=0x90;
      Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1; Address(0xf0[7:2])
```

```
SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
      Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0; Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
      Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIWrite 0144,04,0,7  //Property_124h_4_2=0x1;
      Address(0x144[7:2])
SPIWrite 0018,00,0,7  //macro=0x0;     Address(0x18[7:5])
SPIWrite 0018,08,0,7  //Property_18h_3_3=0x1;
      Address(0x18[7:3])
SPIWrite 7f54,00,0,7
SPIWrite 7f55,00,0,7
SPIWrite 7f56,00,0,7
```

```
SPIWrite 7f57,00,0,7
SPIWrite 0018,00,0,7  //Property_18h_3_3=0x0;
     Address(0x18[7:3])
SPIWrite 0018,20,0,7  //macro=0x1;    Address(0x18[7:5])
SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0x1;
     Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00,0,7
SPIWrite 00a1,00,0,7
SPIWrite 00a0,01,0,7
SPIWrite 0193,90,0,7  //MACRO_OPCODE=0x90;
     Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
     Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
     Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])
```

```
SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0xc03;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00,0,7
SPIWrite 00a1,0c,0,7
SPIWrite 00a0,03,0,7
SPIWrite 0193,2e,0,7  //MACRO_OPCODE=0x2e;
      Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
      Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0,5,5
```

```
//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
      Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0x40f;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00,0,7
SPIWrite 00a1,04,0,7
SPIWrite 00a0,0f,0,7
SPIWrite 0193,2b,0,7  //MACRO_OPCODE=0x2b;
      Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])
```

```
SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
      Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0; Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
      Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0x1f0;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00,0,7
SPIWrite 00a1,01,0,7
SPIWrite 00a0,f0,0,7
SPIWrite 0193,23,0,7  //MACRO_OPCODE=0x23;
      Address(0x193[7:0],0x194[7:0])
```

```
WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
      Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
      Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])
```

```
SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0x30f;
     Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00,0,7
SPIWrite 00a1,03,0,7
SPIWrite 00a0,0f,0,7
SPIWrite 00a7,e3,0,7  //MACRO_OPERAND_REG1=0xe38e5ce0;
     Address(0xa4[7:0],0xa5[7:0],0xa6[7:0],0xa7[7:0],0xa8[7:0])
SPIWrite 00a6,8e,0,7
SPIWrite 00a5,5c,0,7
SPIWrite 00a4,e0,0,7
SPIWrite 00ab,e3,0,7  //MACRO_OPERAND_REG2=0xe38e70d8;
     Address(0xa8[7:0],0xa9[7:0],0xaa[7:0],0xab[7:0],0xac[7:0])
SPIWrite 00aa,8e,0,7
SPIWrite 00a9,70,0,7
SPIWrite 00a8,d8,0,7
SPIWrite 00af,e3,0,7  //MACRO_OPERAND_REG3=0xe38e54a0;
     Address(0xac[7:0],0xad[7:0],0xae[7:0],0xaf[7:0],0xb0[7:0])
SPIWrite 00ae,8e,0,7
SPIWrite 00ad,54,0,7
SPIWrite 00ac,a0,0,7
SPIWrite 00b3,00,0,7  //MACRO_OPERAND_REG4=0x70d8;
     Address(0xb0[7:0],0xb1[7:0],0xb2[7:0],0xb3[7:0],0xb4[7:0])
SPIWrite 00b2,00,0,7
SPIWrite 00b1,70,0,7
SPIWrite 00b0,d8,0,7
SPIWrite 0193,30,0,7  //MACRO_OPCODE=0x30;
     Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
     Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])
```

```
SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
      Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])


//END: Configuring TX Chain Parameters to TOP MCU

SPIWrite 0018,00,0,7  //macro=0x0;     Address(0x18[7:5])

//STEP: configTune/step0

//START: Configuring Digital Chain

SPIWrite 0018,20,0,7  //macro=0x1;     Address(0x18[7:5])
SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0xf2f;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00,0,7
SPIWrite 00a1,0f,0,7
SPIWrite 00a0,2f,0,7
SPIWrite 0193,36,0,7  //MACRO_OPCODE=0x36;
      Address(0x193[7:0],0x194[7:0])
```

```
WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
      Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
      Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])


//END: Configuring Digital Chain

SPIWrite 0018,00,0,7  //macro=0x0;     Address(0x18[7:5])
```

```
//STEP: configTune/step1

//START: Setting FIFO Pointers

SPIWrite 0012,01,0,3  //rxdig=0x1;    Address(0x12[7:0])
SPIWrite 0060,46,0,3  //Property_40h_3_0=0x6;
     Address(0x60[7:0])
SPIWrite 0060,66,4,7  //Property_40h_7_4=0x6;
     Address(0x60[7:4])
SPIWrite 0061,46,0,3  //Property_40h_11_8=0x6;
     Address(0x61[7:0])
SPIWrite 0061,66,4,7  //Property_40h_15_12=0x6;
     Address(0x61[7:4])
SPIWrite 0012,02,0,3  //rxdig=0x2;    Address(0x12[7:0])
SPIWrite 0060,46,0,3  //Property_40h_3_0=0x6;
     Address(0x60[7:0])
SPIWrite 0060,66,4,7  //Property_40h_7_4=0x6;
     Address(0x60[7:4])
SPIWrite 0061,46,0,3  //Property_40h_11_8=0x6;
     Address(0x61[7:0])
SPIWrite 0061,66,4,7  //Property_40h_15_12=0x6;
     Address(0x61[7:4])
SPIWrite 0012,04,0,3  //rxdig=0x4;    Address(0x12[7:0])
SPIWrite 0060,46,0,3  //Property_40h_3_0=0x6;
     Address(0x60[7:0])
SPIWrite 0060,66,4,7  //Property_40h_7_4=0x6;
     Address(0x60[7:4])
SPIWrite 0061,46,0,3  //Property_40h_11_8=0x6;
     Address(0x61[7:0])
SPIWrite 0061,66,4,7  //Property_40h_15_12=0x6;
     Address(0x61[7:4])
SPIWrite 0012,08,0,3  //rxdig=0x8;    Address(0x12[7:0])
SPIWrite 0060,46,0,3  //Property_40h_3_0=0x6;
     Address(0x60[7:0])
SPIWrite 0060,66,4,7  //Property_40h_7_4=0x6;
     Address(0x60[7:4])
SPIWrite 0061,46,0,3  //Property_40h_11_8=0x6;
     Address(0x61[7:0])
SPIWrite 0061,66,4,7  //Property_40h_15_12=0x6;
     Address(0x61[7:4])
SPIWrite 0012,00,0,3  //rxdig=0x0;    Address(0x12[7:0])
SPIWrite 0012,10,4,5  //fbdig=0x1;    Address(0x12[7:4])
SPIWrite 0060,46,0,3  //Property_40h_3_0=0x6;
     Address(0x60[7:0])
SPIWrite 0060,66,4,7  //Property_40h_7_4=0x6;
     Address(0x60[7:4])
SPIWrite 0061,46,0,3  //Property_40h_11_8=0x6;
     Address(0x61[7:0])
SPIWrite 0061,66,4,7  //Property_40h_15_12=0x6;
     Address(0x61[7:4])
SPIWrite 0012,20,4,5  //fbdig=0x2;    Address(0x12[7:4])
```

```
SPIWrite 0060,46,0,3  //Property_40h_3_0=0x6;
      Address(0x60[7:0])
SPIWrite 0060,66,4,7  //Property_40h_7_4=0x6;
      Address(0x60[7:4])
SPIWrite 0061,46,0,3  //Property_40h_11_8=0x6;
      Address(0x61[7:0])
SPIWrite 0061,66,4,7  //Property_40h_15_12=0x6;
      Address(0x61[7:4])
SPIWrite 0012,00,4,5  //fbdig=0x0;     Address(0x12[7:4])
SPIWrite 0019,10,4,7  //txdig=0x1;     Address(0x19[7:4])
SPIWrite 0062,06,0,3  //Property_40h_19_16=0x6;
      Address(0x62[7:0])
SPIWrite 0019,20,4,7  //txdig=0x2;     Address(0x19[7:4])
SPIWrite 0062,06,0,3  //Property_40h_19_16=0x6;
      Address(0x62[7:0])
SPIWrite 0019,40,4,7  //txdig=0x4;     Address(0x19[7:4])
SPIWrite 0062,06,0,3  //Property_40h_19_16=0x6;
      Address(0x62[7:0])
SPIWrite 0019,80,4,7  //txdig=0x8;     Address(0x19[7:4])
SPIWrite 0062,06,0,3  //Property_40h_19_16=0x6;
      Address(0x62[7:0])
SPIWrite 0019,10,4,7  //txdig=0x1;     Address(0x19[7:4])
SPIWrite 0060,00,0,3  //Property_40h_3_0=0x0;
      Address(0x60[7:0])
SPIWrite 0019,20,4,7  //txdig=0x2;     Address(0x19[7:4])
SPIWrite 0060,00,0,3  //Property_40h_3_0=0x0;
      Address(0x60[7:0])
SPIWrite 0019,40,4,7  //txdig=0x4;     Address(0x19[7:4])
SPIWrite 0060,00,0,3  //Property_40h_3_0=0x0;
      Address(0x60[7:0])
SPIWrite 0019,80,4,7  //txdig=0x8;     Address(0x19[7:4])
SPIWrite 0060,00,0,3  //Property_40h_3_0=0x0;
      Address(0x60[7:0])
SPIWrite 0019,00,4,7  //txdig=0x0;     Address(0x19[7:4])
SPIWrite 0016,10,4,4  //jesd_subchip=0x1;   Address(0x16[7:4])
SPIWrite 0030,81,0,3  //rxa_afifo_offset=0x1;
      Address(0x30[7:0])
SPIWrite 0030,11,4,7  //rxb_afifo_offset=0x1;
      Address(0x30[7:4])
SPIWrite 0031,81,0,3  //rxc_afifo_offset=0x1;
      Address(0x31[7:0])
SPIWrite 0031,11,4,7  //rxd_afifo_offset=0x1;
      Address(0x31[7:4])
SPIWrite 0032,80,0,3  //fba_afifo_offset=0x0;
      Address(0x32[7:0])
SPIWrite 0032,00,4,7  //fbc_afifo_offset=0x0;
      Address(0x32[7:4])

//END: Setting FIFO Pointers

SPIWrite 0016,00,0,7  //jesd_subchip=0x0;   Address(0x16[7:4])
SPIWrite 0018,20,0,7  //macro=0x1;     Address(0x18[7:5])
```

```
SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 0193,3d,0,7  //MACRO_OPCODE=0x3d;
     Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
     Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
     Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
     Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
```

```
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIWrite 0018,00,0,7  //macro=0x0;     Address(0x18[7:5])

//STEP: analogWrites/step0
SPIWrite 0011,3f,0,7  //ec_ana=0x3f;   Address(0x11[7:0])
SPIWrite 0075,00,0,7  //Property_75h_7_7_76h_3_0=0x6;
      Address(0x75[7:7],0x76[7:0])
SPIWrite 0076,03,0,7
SPIWrite 0071,04,0,7  //Property_71h_2_1=0x2;
      Address(0x71[7:1])
SPIWrite 0071,14,0,7  //Property_71h_4_4=0x1;
      Address(0x71[7:4])
SPIWrite 0084,80,0,7  //Property_84h_7_6_85h_1_0=0xe;
      Address(0x84[7:6],0x85[7:0])
SPIWrite 0085,03,0,7
SPIWrite 0011,00,0,7  //ec_ana=0x0;    Address(0x11[7:0])
SPIWrite 0018,20,0,7  //macro=0x1;     Address(0x18[7:5])
SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0x124;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00,0,7
SPIWrite 00a1,01,0,7
SPIWrite 00a0,24,0,7
SPIWrite 0193,72,0,7  //MACRO_OPCODE=0x72;
      Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
```

```
      Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0; Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
      Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,01,0,7  //MACRO_OPERAND_REG0=0x1000600;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00,0,7
SPIWrite 00a1,06,0,7
SPIWrite 00a0,00,0,7
SPIWrite 00a7,05,0,7  //MACRO_OPERAND_REG1=0x5040302;
      Address(0xa4[7:0],0xa5[7:0],0xa6[7:0],0xa7[7:0],0xa8[7:0])
SPIWrite 00a6,04,0,7
SPIWrite 00a5,03,0,7
SPIWrite 00a4,02,0,7
SPIWrite 0193,71,0,7  //MACRO_OPCODE=0x71;
      Address(0x193[7:0],0x194[7:0])
```

```
WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
      Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
      Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIWrite 0018,00,0,7  //macro=0x0;     Address(0x18[7:5])
SPIWrite 0011,3f,0,7  //ec_ana=0x3f;   Address(0x11[7:0])
SPIWrite 0060,01,0,7  //Property_60h_0_0=0x1;
```

```
     Address(0x60[7:0])
SPIWrite 0060,00,0,7  //Property_60h_0_0=0x0;
     Address(0x60[7:0])
SPIWrite 0011,00,0,7  //ec_ana=0x0;    Address(0x11[7:0])

//STEP: analogWrites/step1

//START: Removing TDD Pin Overrides.

SPIWrite 0015,80,0,7  //timing_controller=0x1;
     Address(0x15[7:7])
SPIWrite 00ed,00,0,7  //Property_cch_11_8=0x0;
     Address(0xed[7:0])
SPIWrite 00f5,00,0,7  //Property_d4h_9_8=0x0;
     Address(0xf5[7:0])
SPIWrite 00e5,0f,0,7  //Property_c4h_11_8=0xf;
     Address(0xe5[7:0])

//END: Removing TDD Pin Overrides.


//START: DAC Analog Writes

SPIWrite 0015,00,0,7  //timing_controller=0x0;
     Address(0x15[7:7])
SPIWrite 0013,0f,0,7  //txdh=0xf;      Address(0x13[7:0])
SPIWrite 015a,20,0,7  //Property_138h_21_21=0x1;
     Address(0x15a[7:5])
SPIWrite 01bd,00,0,7  //Property_19ch_15_0=0x1;
     Address(0x1bc[7:0],0x1bd[7:0],0x1be[7:0])
SPIWrite 01bc,01,0,7
SPIWrite 015a,22,0,7  //Property_138h_17_17=0x1;
     Address(0x15a[7:1])
SPIWrite 0070,27,0,7  //Property_50h_5_0=0x27;
     Address(0x70[7:0])
SPIWrite 0071,27,0,7  //Property_50h_13_8=0x27;
     Address(0x71[7:0])
SPIWrite 0072,27,0,7  //Property_50h_21_16=0x27;
     Address(0x72[7:0])
SPIWrite 0074,27,0,7  //Property_54h_5_0=0x27;
     Address(0x74[7:0])
SPIWrite 0075,27,0,7  //Property_54h_13_8=0x27;
     Address(0x75[7:0])
SPIWrite 0076,27,0,7  //Property_54h_21_16=0x27;
     Address(0x76[7:0])
SPIWrite 0078,27,0,7  //Property_58h_5_0=0x27;
     Address(0x78[7:0])
SPIWrite 0079,27,0,7  //Property_58h_13_8=0x27;
     Address(0x79[7:0])
SPIWrite 007a,27,0,7  //Property_58h_21_16=0x27;
     Address(0x7a[7:0])
SPIWrite 015a,26,0,7  //Property_138h_18_18=0x1;
```

```
     Address(0x15a[7:2])
SPIWrite 015a,26,0,7  //Property_138h_18_18=0x1;
     Address(0x15a[7:2])
SPIWrite 0025,00,0,7  //Property_4h_8_8=0x0;
     Address(0x25[7:0])
SPIWrite 015a,27,0,7  //Property_138h_16_16=0x1;
     Address(0x15a[7:0])
SPIWrite 0168,01,0,7  //Property_148h_0_0=0x1;
     Address(0x168[7:0])
SPIWrite 017c,01,0,7  //Property_15ch_0_0=0x1;
     Address(0x17c[7:0])
SPIWrite 01b1,00,0,7  //Property_190h_15_0=0x10;
     Address(0x1b0[7:0],0x1b1[7:0],0x1b2[7:0])
SPIWrite 01b0,10,0,7
SPIWrite 0158,01,0,7  //Property_138h_0_0=0x1;
     Address(0x158[7:0])
SPIWrite 0159,01,0,7  //Property_138h_8_8=0x1;
     Address(0x159[7:0])
SPIWrite 0177,00,0,7  //Property_154h_31_0_158h_3_0=0x800000001;
     Address(0x174[7:0],0x175[7:0],0x176[7:0],0x177[7:0],0x178[7:
0],0x178[7:0])
SPIWrite 0176,00,0,7
SPIWrite 0175,00,0,7
SPIWrite 0174,01,0,7
SPIWrite 0178,08,0,7
SPIWrite 018b,00,0,7  //Property_168h_31_0_16ch_3_0=0x800000001;
     Address(0x188[7:0],0x189[7:0],0x18a[7:0],0x18b[7:0],0x18c[7:
0],0x18c[7:0])
SPIWrite 018a,00,0,7
SPIWrite 0189,00,0,7
SPIWrite 0188,01,0,7
SPIWrite 018c,08,0,7
SPIWrite 011a,00,0,7  //Property_f8h_20_0=0x0;
     Address(0x118[4:0],0x119[4:0],0x11a[7:0])
SPIWrite 0119,00,0,7
SPIWrite 0118,00,0,7
SPIWrite 0126,00,0,7  //Property_104h_20_0=0x0;
     Address(0x124[4:0],0x125[4:0],0x126[7:0])
SPIWrite 0125,00,0,7
SPIWrite 0124,00,0,7
SPIWrite 01c5,3d,0,7  //Property_1a4h_15_0=0x3de0;
     Address(0x1c4[7:0],0x1c5[7:0],0x1c6[7:0])
SPIWrite 01c4,e0,0,7
SPIWrite 0133,00,0,7  //Property_110h_31_0_114h_14_0=0x1fe0;
     Address(0x130[7:0],0x131[7:0],0x132[7:0],0x133[7:0],0x134[7:
0],0x134[6:0],0x135[7:0])
SPIWrite 0132,00,0,7
SPIWrite 0131,1f,0,7
SPIWrite 0130,e0,0,7
SPIWrite 0135,00,0,7
SPIWrite 0134,00,0,7
SPIWrite 0029,00,0,7  //Property_8h_8_8=0x0;
```

```
     Address(0x29[7:0])
SPIWrite 018e,01,0,7  //Property_16ch_16_16=0x1;
     Address(0x18e[7:0])
SPIWrite 0112,00,0,7  //Property_f0h_18_0=0x0;
     Address(0x110[2:0],0x111[2:0],0x112[7:0])
SPIWrite 0111,00,0,7
SPIWrite 0110,00,0,7
SPIWrite 0151,0e,0,7  //Property_130h_15_0=0xed3;
     Address(0x150[7:0],0x151[7:0],0x152[7:0])
SPIWrite 0150,d3,0,7
SPIWrite 01ad,00,0,7  //Property_18ch_15_0=0xff;
     Address(0x1ac[7:0],0x1ad[7:0],0x1ae[7:0])
SPIWrite 01ac,ff,0,7
SPIWrite 0162,00,0,7  //Property_140h_19_16=0x0;
     Address(0x162[7:0])
SPIWrite 0163,00,0,7  //Property_140h_27_24=0x0;
     Address(0x163[7:0])
SPIWrite 0013,00,0,7  //txdh=0x0;     Address(0x13[7:0])

//START: Requesting/releasing SPI Access to PLL Pages

SPIWrite 0015,40,0,7  //digtop=0x1;   Address(0x15[7:6])
SPIWrite 0170,01,0,7  //pll_reg_spi_req_a=0x1;
     Address(0x170[7:0])
SPIWrite 0540,00,0,7  //Property_520h_0_0=0x0;
     Address(0x540[7:0])

SPIPoll 0171,0,0,01
SPIRead 0171,0,0

//Read     pll_reg_spi_a_ack=0x1(Meaning: );;
     Address(0x171[7:0])


//END: Requesting/releasing SPI Access to PLL Pages

SPIWrite 0015,00,0,7  //digtop=0x0;   Address(0x15[7:6])
SPIWrite 0014,ff,0,7  //txcalib=0xff;
     Address(0x14[7:0],0x15[7:0])
SPIWrite 0119,00,0,7  //Property_f8h_15_0=0x1;
     Address(0x118[7:0],0x119[7:0],0x11a[7:0])
SPIWrite 0118,01,0,7

WAIT 0.1
SPIWrite 0119,00,0,7  //Property_f8h_15_0=0x0;
     Address(0x118[7:0],0x119[7:0],0x11a[7:0])
SPIWrite 0118,00,0,7

//START: Requesting/releasing SPI Access to PLL Pages

SPIWrite 0014,00,0,7  //txcalib=0x0;
     Address(0x14[7:0],0x15[7:0])
```

```
SPIWrite 0015,40,0,7  //digtop=0x1;    Address(0x15[7:6])
SPIWrite 0170,00,0,7  //pll_reg_spi_req_a=0x0;
     Address(0x170[7:0])
SPIWrite 0540,00,0,7  //Property_520h_0_0=0x0;
     Address(0x540[7:0])

WAIT 0.2

//END: Requesting/releasing SPI Access to PLL Pages

SPIWrite 0015,00,0,7  //digtop=0x0;    Address(0x15[7:6])
SPIWrite 0019,f0,0,7  //txdig=0xf;     Address(0x19[7:4])
SPIWrite 07d3,01,0,7  //EnDacDataRandomization=0x1;
     Address(0x7d3[7:0])
SPIWrite 0019,00,0,7  //txdig=0x0;     Address(0x19[7:4])
SPIWrite 0019,f0,0,7  //txdig=0xf;     Address(0x19[7:4])
SPIWrite 0320,00,0,7  //Property_300h_3_0=0x0;
     Address(0x320[7:0])
SPIWrite 0019,00,0,7  //txdig=0x0;     Address(0x19[7:4])
SPIWrite 0013,01,0,7  //txdh=0x1;      Address(0x13[7:0])
SPIWrite 0107,f0,0,7  //Property_e4h_31_0_e8h_19_0=0xf0000040;
     Address(0x104[7:0],0x105[7:0],0x106[7:0],0x107[7:0],0x108[7:
0],0x108[3:0],0x109[3:0],0x10a[7:0])
SPIWrite 0106,00,0,7
SPIWrite 0105,00,0,7
SPIWrite 0104,40,0,7
SPIWrite 010a,00,0,7
SPIWrite 0109,00,0,7
SPIWrite 0108,00,0,7
SPIWrite 0013,02,0,7  //txdh=0x2;      Address(0x13[7:0])
SPIWrite 0107,f0,0,7  //Property_e4h_31_0_e8h_19_0=0xf0000040;
     Address(0x104[7:0],0x105[7:0],0x106[7:0],0x107[7:0],0x108[7:
0],0x108[3:0],0x109[3:0],0x10a[7:0])
SPIWrite 0106,00,0,7
SPIWrite 0105,00,0,7
SPIWrite 0104,40,0,7
SPIWrite 010a,00,0,7
SPIWrite 0109,00,0,7
SPIWrite 0108,00,0,7
SPIWrite 0013,04,0,7  //txdh=0x4;      Address(0x13[7:0])
SPIWrite 0107,f0,0,7  //Property_e4h_31_0_e8h_19_0=0xf0000040;
     Address(0x104[7:0],0x105[7:0],0x106[7:0],0x107[7:0],0x108[7:
0],0x108[3:0],0x109[3:0],0x10a[7:0])
SPIWrite 0106,00,0,7
SPIWrite 0105,00,0,7
SPIWrite 0104,40,0,7
SPIWrite 010a,00,0,7
SPIWrite 0109,00,0,7
SPIWrite 0108,00,0,7
SPIWrite 0013,08,0,7  //txdh=0x8;      Address(0x13[7:0])
SPIWrite 0107,f0,0,7  //Property_e4h_31_0_e8h_19_0=0xf0000040;
     Address(0x104[7:0],0x105[7:0],0x106[7:0],0x107[7:0],0x108[7:
```

```
0],0x108[3:0],0x109[3:0],0x10a[7:0])
SPIWrite 0106,00,0,7
SPIWrite 0105,00,0,7
SPIWrite 0104,40,0,7
SPIWrite 010a,00,0,7
SPIWrite 0109,00,0,7
SPIWrite 0108,00,0,7
SPIWrite 0013,0f,0,7  //txdh=0xf;      Address(0x13[7:0])
SPIWrite 0024,00,0,7  //Property_4h_1_0=0x0;
     Address(0x24[7:0])
SPIWrite 0013,00,0,7  //txdh=0x0;      Address(0x13[7:0])
SPIWrite 0019,f0,0,7  //txdig=0xf;     Address(0x19[7:4])
SPIWrite 030c,01,0,7  //Property_2ech_0_0=0x1;
     Address(0x30c[7:0])
SPIWrite 0019,00,0,7  //txdig=0x0;     Address(0x19[7:4])
SPIWrite 0013,0f,0,7  //txdh=0xf;      Address(0x13[7:0])
SPIWrite 011a,00,0,7  //Property_f8h_20_0=0x2000;
     Address(0x118[4:0],0x119[4:0],0x11a[7:0])
SPIWrite 0119,20,0,7
SPIWrite 0118,00,0,7
SPIWrite 0126,00,0,7  //Property_104h_20_0=0x2000;
     Address(0x124[4:0],0x125[4:0],0x126[7:0])
SPIWrite 0125,20,0,7
SPIWrite 0124,00,0,7
SPIWrite 015a,25,0,7  //Property_138h_17_17=0x0;
     Address(0x15a[7:1])
SPIWrite 0013,00,0,7  //txdh=0x0;      Address(0x13[7:0])
SPIWrite 0015,80,0,7  //timing_controller=0x1;
     Address(0x15[7:7])
SPIWrite 00fd,01,0,7  //Property_dch_15_0=0x180;
     Address(0xfc[7:0],0xfd[7:0],0xfe[7:0])
SPIWrite 00fc,80,0,7
SPIWrite 0101,01,0,7  //Property_e0h_15_0=0x180;
     Address(0x100[7:0],0x101[7:0],0x102[7:0])
SPIWrite 0100,80,0,7
SPIWrite 019d,01,0,7  //Property_17ch_15_0=0x180;
     Address(0x19c[7:0],0x19d[7:0],0x19e[7:0])
SPIWrite 019c,80,0,7
SPIWrite 01a1,01,0,7  //Property_180h_15_0=0x180;
     Address(0x1a0[7:0],0x1a1[7:0],0x1a2[7:0])
SPIWrite 01a0,80,0,7
SPIWrite 023d,01,0,7  //Property_21ch_15_0=0x180;
     Address(0x23c[7:0],0x23d[7:0],0x23e[7:0])
SPIWrite 023c,80,0,7
SPIWrite 0241,01,0,7  //Property_220h_15_0=0x180;
     Address(0x240[7:0],0x241[7:0],0x242[7:0])
SPIWrite 0240,80,0,7
SPIWrite 02dd,01,0,7  //Property_2bch_15_0=0x180;
     Address(0x2dc[7:0],0x2dd[7:0],0x2de[7:0])
SPIWrite 02dc,80,0,7
SPIWrite 02e1,01,0,7  //Property_2c0h_15_0=0x180;
     Address(0x2e0[7:0],0x2e1[7:0],0x2e2[7:0])
```

```
SPIWrite 02e0,80,0,7
SPIWrite 0135,0c,0,7  //Property_114h_15_0=0xc00;
     Address(0x134[7:0],0x135[7:0],0x136[7:0])
SPIWrite 0134,00,0,7
SPIWrite 01d5,0c,0,7  //Property_1b4h_15_0=0xc00;
     Address(0x1d4[7:0],0x1d5[7:0],0x1d6[7:0])
SPIWrite 01d4,00,0,7
SPIWrite 0275,0c,0,7  //Property_254h_15_0=0xc00;
     Address(0x274[7:0],0x275[7:0],0x276[7:0])
SPIWrite 0274,00,0,7
SPIWrite 0315,0c,0,7  //Property_2f4h_15_0=0xc00;
     Address(0x314[7:0],0x315[7:0],0x316[7:0])
SPIWrite 0314,00,0,7
SPIWrite 0015,00,0,7  //timing_controller=0x0;
     Address(0x15[7:7])
SPIWrite 0013,0f,0,7  //txdh=0xf;      Address(0x13[7:0])
SPIWrite 0167,02,0,7  //Property_144h_27_0=0x2000000;
     Address(0x164[3:0],0x165[3:0],0x166[3:0],0x167[7:0])
SPIWrite 0166,00,0,7
SPIWrite 0165,00,0,7
SPIWrite 0164,00,0,7
SPIWrite 01b1,00,0,7  //Property_190h_15_0=0x30;
     Address(0x1b0[7:0],0x1b1[7:0],0x1b2[7:0])
SPIWrite 01b0,30,0,7
SPIWrite 0112,01,0,7  //Property_f0h_18_0=0x10000;
     Address(0x110[2:0],0x111[2:0],0x112[7:0])
SPIWrite 0111,00,0,7
SPIWrite 0110,00,0,7
SPIWrite 0013,00,0,7  //txdh=0x0;      Address(0x13[7:0])
SPIWrite 0019,f0,0,7  //txdig=0xf;     Address(0x19[7:4])
SPIWrite 07b2,00,0,7  //rf_droop_comp_bypass=0x0;
     Address(0x7b2[7:0])
SPIWrite 07b0,1c,0,7  //rf_headroom_band0=0x1c;
     Address(0x7b0[7:0])
SPIWrite 07b1,1c,0,7  //rf_headroom_band1=0x1c;
     Address(0x7b1[7:0])
SPIWrite 0019,00,0,7  //txdig=0x0;     Address(0x19[7:4])

//END: DAC Analog Writes

SPIWrite 0018,20,0,7  //macro=0x1;     Address(0x18[7:5])
SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,0a,0,7  //MACRO_OPERAND_REG0=0xa040414;
     Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,04,0,7
SPIWrite 00a1,04,0,7
```

```
SPIWrite 00a0,14,0,7
SPIWrite 00a7,1f,0,7  //MACRO_OPERAND_REG1=0x1f010100;
     Address(0xa4[7:0],0xa5[7:0],0xa6[7:0],0xa7[7:0],0xa8[7:0])
SPIWrite 00a6,01,0,7
SPIWrite 00a5,01,0,7
SPIWrite 00a4,00,0,7
SPIWrite 00ab,03,0,7  //MACRO_OPERAND_REG2=0x303041f;
     Address(0xa8[7:0],0xa9[7:0],0xaa[7:0],0xab[7:0],0xac[7:0])
SPIWrite 00aa,03,0,7
SPIWrite 00a9,04,0,7
SPIWrite 00a8,1f,0,7
SPIWrite 00af,00,0,7  //MACRO_OPERAND_REG3=0x101;
     Address(0xac[7:0],0xad[7:0],0xae[7:0],0xaf[7:0],0xb0[7:0])
SPIWrite 00ae,00,0,7
SPIWrite 00ad,01,0,7
SPIWrite 00ac,01,0,7
SPIWrite 0193,88,0,7  //MACRO_OPCODE=0x88;
     Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
     Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
     Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])
```

```
SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0x0;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00,0,7
SPIWrite 00a1,00,0,7
SPIWrite 00a0,00,0,7
SPIWrite 0193,90,0,7  //MACRO_OPCODE=0x90;
      Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
      Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0,5,5
```

```
//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
      Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIWrite 0144,08,0,7  //Property_124h_4_2=0x2;
      Address(0x144[7:2])
SPIWrite 0018,00,0,7  //macro=0x0;     Address(0x18[7:5])
SPIWrite 0018,08,0,7  //Property_18h_3_3=0x1;
      Address(0x18[7:3])
SPIWrite 1f96,00,0,7
SPIWrite 0018,00,0,7  //Property_18h_3_3=0x0;
      Address(0x18[7:3])
SPIWrite 0018,20,0,7  //macro=0x1;     Address(0x18[7:5])
SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0x1;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00,0,7
SPIWrite 00a1,00,0,7
SPIWrite 00a0,01,0,7
SPIWrite 0193,90,0,7  //MACRO_OPCODE=0x90;
      Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2
```

```
//Read     MACRO_DONE=0x1; Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
      Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0; Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
      Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])


//START: Configuring AUX ADC

SPIWrite 0018,00,0,7  //macro=0x0;     Address(0x18[7:5])
SPIWrite 0015,02,0,7  //ana_4t4r=0x1;  Address(0x15[7:1])
SPIWrite 00c0,c0,0,7  //Property_a0h_6_6=0x1;
```

```
     Address(0xc0[7:6])
SPIWrite 0015,00,0,7  //ana_4t4r=0x0; Address(0x15[7:1])
SPIWrite 0015,40,0,7  //digtop=0x1;   Address(0x15[7:6])
SPIWrite 0500,01,0,7  //Property_4e0h_0_0=0x1;
     Address(0x500[7:0])
SPIWrite 0500,01,0,7  //Property_4e0h_1_1=0x0;
     Address(0x500[7:1])
SPIWrite 0500,09,0,7  //Property_4e0h_3_3=0x1;
     Address(0x500[7:3])
SPIWrite 0506,01,0,7  //Property_4e4h_16_16=0x1;
     Address(0x506[7:0])
SPIWrite 0502,00,0,7  //Property_4e0h_23_21=0x0;
     Address(0x502[7:5])
SPIWrite 0502,00,0,7  //Property_4e0h_20_18=0x0;
     Address(0x502[7:2])
SPIWrite 0501,08,0,7  //Property_4e0h_12_11=0x1;
     Address(0x501[7:3])
SPIWrite 0501,0a,0,7  //Property_4e0h_10_8=0x2;
     Address(0x501[7:0])
SPIWrite 0508,00,0,7  //Property_4e8h_5_5=0x0;
     Address(0x508[7:5])
SPIWrite 0505,a0,0,7  //Property_4e4h_15_13=0x5;
     Address(0x505[7:5])
SPIWrite 0505,a1,0,7  //Property_4e4h_9_8=0x1;
     Address(0x505[7:0])
SPIWrite 0506,05,0,7  //Property_4e4h_18_17=0x2;
     Address(0x506[7:1])
SPIWrite 0506,15,0,7  //Property_4e4h_20_19=0x2;
     Address(0x506[7:3])
SPIWrite 0506,15,0,7  //Property_4e4h_23_21=0x0;
     Address(0x506[7:5])
SPIWrite 0505,a1,0,7  //Property_4e4h_12_10=0x0;
     Address(0x505[7:2])
SPIWrite 0508,00,0,7  //Property_4e8h_6_6=0x0;
     Address(0x508[7:6])
SPIWrite 0508,00,0,7  //Property_4e8h_4_4=0x0;
     Address(0x508[7:4])
SPIWrite 0503,00,0,7  //Property_4e0h_31_30=0x0;
     Address(0x503[7:6])
SPIWrite 0502,00,0,7  //Property_4e0h_17_16=0x0;
     Address(0x502[7:0])

WAIT 0.01
SPIWrite 0500,01,0,7  //Property_4e0h_3_3=0x0;
     Address(0x500[7:3])

WAIT 0.01
SPIWrite 0500,03,0,7  //Property_4e0h_1_1=0x1;
     Address(0x500[7:1])

//END: Configuring AUX ADC
```

```
SPIWrite 0015,00,0,7  //digtop=0x0;    Address(0x15[7:6])

//STEP: analogWrites/step2

//START: Removing TDD Pin Overrides.

SPIWrite 0015,80,0,7  //timing_controller=0x1;
      Address(0x15[7:7])
SPIWrite 00ed,0f,0,7  //Property_cch_11_8=0xf;
      Address(0xed[7:0])
SPIWrite 00f5,00,0,7  //Property_d4h_9_8=0x0;
      Address(0xf5[7:0])
SPIWrite 00e5,00,0,7  //Property_c4h_11_8=0x0;
      Address(0xe5[7:0])

//END: Removing TDD Pin Overrides.

SPIWrite 0015,00,0,7  //timing_controller=0x0;
      Address(0x15[7:7])
SPIWrite 0011,3f,0,7  //ec_ana=0x3f;   Address(0x11[7:0])
SPIWrite 0063,80,0,7  //Property_63h_7_7=0x1;
      Address(0x63[7:7])
SPIWrite 0067,10,0,7  //Property_67h_4_4=0x1;
      Address(0x67[7:4])
SPIWrite 0077,0c,0,7  //Property_77h_5_1=0x6;
      Address(0x77[7:1])
SPIWrite 0076,53,0,7  //Property_76h_6_4=0x5;
      Address(0x76[7:4])
SPIWrite 0082,80,0,7  //Property_82h_7_6=0x2;
      Address(0x82[7:6])
SPIWrite 0082,a0,0,7  //Property_82h_5_3=0x4;
      Address(0x82[7:3])
SPIWrite 0081,30,0,7  //Property_81h_5_4=0x3;
      Address(0x81[7:4])
SPIWrite 0086,c0,0,7  //Property_86h_7_5_87h_0_0=0xe;
      Address(0x86[7:5],0x87[7:0])
SPIWrite 0087,01,0,7
SPIWrite 0084,85,0,7  //Property_84h_2_0=0x5;
      Address(0x84[7:0])
SPIWrite 0087,05,0,7  //Property_87h_2_1=0x2;
      Address(0x87[7:1])
SPIWrite 00f9,00,0,7  //Property_f9h_7_7_fah_2_0=0xc;
      Address(0xf9[7:7],0xfa[7:0])
SPIWrite 00fa,06,0,7
SPIWrite 00e8,80,0,7  //Property_e8h_7_5=0x4;
      Address(0xe8[7:5])
SPIWrite 014e,01,0,7  //Property_14eh_2_0=0x1;
      Address(0x14e[7:0])
SPIWrite 014d,1c,0,7  //Property_14dh_4_2=0x7;
      Address(0x14d[7:2])
SPIWrite 014c,20,0,7  //Property_14ch_5_3=0x4;
      Address(0x14c[7:3])
```

```
SPIWrite 0138,18,0,7  //Property_138h_5_3=0x3;
      Address(0x138[7:3])
SPIWrite 013e,40,0,7  //Property_13eh_6_6=0x1;
      Address(0x13e[7:6])
SPIWrite 004a,60,0,7  //Property_4ah_6_4=0x6;
      Address(0x4a[7:4])
SPIWrite 0049,80,0,7  //Property_49h_7_6_4ah_0_0=0x6;
      Address(0x49[7:6],0x4a[7:0])
SPIWrite 004a,61,0,7
SPIWrite 00c2,c0,0,7  //Property_c2h_7_5=0x6;
      Address(0xc2[7:5])
SPIWrite 00c1,60,0,7  //Property_c1h_6_4=0x6;
      Address(0xc1[7:4])
SPIWrite 00b6,0c,0,7  //Property_b6h_3_2=0x3;
      Address(0xb6[7:2])
SPIWrite 004f,0c,0,7  //Property_4fh_3_2=0x3;
      Address(0x4f[7:2])
SPIWrite 012e,80,0,7  //Property_12eh_7_7_12fh_1_0=0x7;
      Address(0x12e[7:7],0x12f[7:0])
SPIWrite 012f,03,0,7
SPIWrite 012e,f0,0,7  //Property_12eh_6_4=0x7;
      Address(0x12e[7:4])
SPIWrite 012f,03,0,7  //Property_12fh_3_2=0x0;
      Address(0x12f[7:2])
SPIWrite 0011,00,0,7  //ec_ana=0x0;    Address(0x11[7:0])
SPIWrite 0010,3f,0,7  //ec_dig=0x3f;   Address(0x10[7:0])
SPIWrite 00c1,5a,0,7  //Property_c1h_6_0=0x5a;
      Address(0xc1[7:0])
SPIWrite 0078,60,0,7  //Property_78h_7_7=0x0;
      Address(0x78[7:7])
SPIWrite 00c0,17,0,7  //Property_c0h_3_3=0x0;
      Address(0xc0[7:3])
SPIWrite 00d5,00,0,7  //Property_d5h_1_0=0x0;
      Address(0xd5[7:0])
SPIWrite 00d5,08,0,7  //Property_d5h_3_2=0x2;
      Address(0xd5[7:2])
SPIWrite 0150,30,0,7  //Property_150h_3_3=0x0;
      Address(0x150[7:3])
SPIWrite 00f8,51,0,7  //Property_f8h_7_0_f9h_7_0_fah_7_0_fbh_7_0
_fch_7_0=0xa8c0c5051;
      Address(0xf8[7:0],0xf9[7:0],0xf9[7:0],0xfa[7:0],0xfa[7:0],0x
fb[7:0],0xfb[7:0],0xfc[7:0],0xfc[7:0],0xfd[7:0])
SPIWrite 00f9,50,0,7
SPIWrite 00fa,0c,0,7
SPIWrite 00fb,8c,0,7
SPIWrite 00fc,0a,0,7
SPIWrite 0168,02,0,7  //Property_168h_1_1=0x1;
      Address(0x168[7:1])
SPIWrite 00ef,08,0,7  //Property_efh_6_6=0x0;
      Address(0xef[7:6])
SPIWrite 0178,71,0,7  //Property_178h_4_4=0x1;
      Address(0x178[7:4])
```

```
SPIWrite 0075,b5,0,7  //Property_75h_4_4=0x1;
     Address(0x75[7:4])
SPIWrite 0168,06,0,7  //Property_168h_2_2=0x1;
     Address(0x168[7:2])
SPIWrite 0168,02,0,7  //Property_168h_2_2=0x0;
     Address(0x168[7:2])
SPIWrite 0169,bb,0,7  //Property_169h_3_0=0xb;
     Address(0x169[7:0])
SPIWrite 0074,7a,0,7  //Property_74h_7_7=0x0;
     Address(0x74[7:7])
SPIWrite 013c,fe,0,7  //Property_13ch_7_0_13dh_7_0_13eh_7_0=
0x6bfffe;
     Address(0x13c[7:0],0x13d[7:0],0x13d[7:0],0x13e[7:0],0x13e[7:
0],0x13f[7:0])
SPIWrite 013d,ff,0,7
SPIWrite 013e,6b,0,7
SPIWrite 0124,fe,0,7  //Property_124h_7_0_125h_7_0_126h_7_0=
0x6bfffe;
     Address(0x124[7:0],0x125[7:0],0x125[7:0],0x126[7:0],0x126[7:
0],0x127[7:0])
SPIWrite 0125,ff,0,7
SPIWrite 0126,6b,0,7
SPIWrite 0129,24,0,7  //Property_129h_2_0=0x4;
     Address(0x129[7:0])
SPIWrite 0130,76,0,7  //Property_130h_2_2=0x1;
     Address(0x130[7:2])
SPIWrite 0130,7e,0,7  //Property_130h_3_3=0x1;
     Address(0x130[7:3])
SPIWrite 0010,1f,0,7  //ec_dig=0x1f;  Address(0x10[7:0])
SPIWrite 0044,01,0,7  //Property_44h_0_0=0x1;
     Address(0x44[7:0])
SPIWrite 003c,01,0,7  //Property_3ch_0_0=0x1;
     Address(0x3c[7:0])

WAIT 0.001
SPIWrite 003c,00,0,7  //Property_3ch_0_0=0x0;
     Address(0x3c[7:0])
SPIWrite 0044,00,0,7  //Property_44h_0_0=0x0;
     Address(0x44[7:0])
SPIWrite 00e8,00,0,7  //Property_e8h_0_0=0x0;
     Address(0xe8[7:0])
SPIWrite 00e8,01,0,7  //Property_e8h_0_0=0x1;
     Address(0xe8[7:0])
SPIWrite 0010,00,0,7  //ec_dig=0x0;   Address(0x10[7:0])
SPIWrite 0015,04,0,7  //rx=0x1;  Address(0x15[7:2])
SPIWrite 0063,00,0,7  //Property_40h_31_0=0x40000;
     Address(0x60[7:0],0x61[7:0],0x62[7:0],0x63[7:0],0x64[7:0])
SPIWrite 0062,04,0,7
SPIWrite 0061,00,0,7
SPIWrite 0060,00,0,7
SPIWrite 0038,b0,0,7
SPIWrite 0028,04,0,7
```

```
SPIWrite 0015,08,0,7  //rx=0x2;  Address(0x15[7:2])
SPIWrite 0063,00,0,7  //Property_40h_31_0=0x40000;
     Address(0x60[7:0],0x61[7:0],0x62[7:0],0x63[7:0],0x64[7:0])
SPIWrite 0062,04,0,7
SPIWrite 0061,00,0,7
SPIWrite 0060,00,0,7
SPIWrite 0038,b0,0,7
SPIWrite 0028,04,0,7
SPIWrite 0015,00,0,7  //rx=0x0;  Address(0x15[7:2])
SPIWrite 0015,02,0,7  //ana_4t4r=0x1; Address(0x15[7:1])
SPIWrite 006b,00,0,7  //Property_48h_31_0=0x8;
     Address(0x68[7:0],0x69[7:0],0x6a[7:0],0x6b[7:0],0x6c[7:0])
SPIWrite 006a,00,0,7
SPIWrite 0069,00,0,7
SPIWrite 0068,08,0,7
SPIWrite 0067,00,0,7  //Property_44h_31_0=0x4000;
     Address(0x64[7:0],0x65[7:0],0x66[7:0],0x67[7:0],0x68[7:0])
SPIWrite 0066,00,0,7
SPIWrite 0065,40,0,7
SPIWrite 0064,00,0,7
SPIWrite 0015,00,0,7  //ana_4t4r=0x0; Address(0x15[7:1])
SPIWrite 0012,0f,0,7  //rxdig=0xf;    Address(0x12[7:0])
SPIWrite 20f4,32,0,7  //DSAGainRange0=0x32;
     Address(0x20f4[7:0])
SPIWrite 20f5,32,0,7  //DSAGainRange1=0x32;
     Address(0x20f5[7:0])
SPIWrite 20f6,32,0,7  //DSAGainRange2=0x32;
     Address(0x20f6[7:0])
SPIWrite 20f7,32,0,7  //DSAGainRange3=0x32;
     Address(0x20f7[7:0])
SPIWrite 20f8,32,0,7  //DSAGainRange4=0x32;
     Address(0x20f8[7:0])
SPIWrite 20f9,32,0,7  //DSAGainRange5=0x32;
     Address(0x20f9[7:0])
SPIWrite 0012,00,0,7  //rxdig=0x0;    Address(0x12[7:0])
SPIWrite 0012,30,0,7  //fbdig=0x3;    Address(0x12[7:4])
SPIWrite 20f4,32,0,7  //DSAGainRange0=0x32;
     Address(0x20f4[7:0])
SPIWrite 20f5,32,0,7  //DSAGainRange1=0x32;
     Address(0x20f5[7:0])
SPIWrite 20f6,32,0,7  //DSAGainRange2=0x32;
     Address(0x20f6[7:0])
SPIWrite 20f7,32,0,7  //DSAGainRange3=0x32;
     Address(0x20f7[7:0])
SPIWrite 20f8,32,0,7  //DSAGainRange4=0x32;
     Address(0x20f8[7:0])
SPIWrite 20f9,32,0,7  //DSAGainRange5=0x32;
     Address(0x20f9[7:0])
SPIWrite 0012,00,0,7  //fbdig=0x0;    Address(0x12[7:4])

//STEP: analogWrites/step3
```

```
//START: Removing TDD Pin Overrides.

SPIWrite 0015,80,0,7  //timing_controller=0x1;
     Address(0x15[7:7])
SPIWrite 00ed,00,0,7  //Property_cch_11_8=0x0;
     Address(0xed[7:0])
SPIWrite 00f5,03,0,7  //Property_d4h_9_8=0x3;
     Address(0xf5[7:0])
SPIWrite 00e5,00,0,7  //Property_c4h_11_8=0x0;
     Address(0xe5[7:0])

//END: Removing TDD Pin Overrides.

SPIWrite 0015,00,0,7  //timing_controller=0x0;
     Address(0x15[7:7])
SPIWrite 0010,20,0,7  //ec_dig=0x20;   Address(0x10[7:0])
SPIWrite 0044,01,0,7  //Property_44h_0_0=0x1;
     Address(0x44[7:0])
SPIWrite 003c,01,0,7  //Property_3ch_0_0=0x1;
     Address(0x3c[7:0])
SPIWrite 003c,00,0,7  //Property_3ch_0_0=0x0;
     Address(0x3c[7:0])
SPIWrite 0044,00,0,7  //Property_44h_0_0=0x0;
     Address(0x44[7:0])
SPIWrite 00e8,00,0,7  //Property_e8h_0_0=0x0;
     Address(0xe8[7:0])
SPIWrite 00e8,01,0,7  //Property_e8h_0_0=0x1;
     Address(0xe8[7:0])
SPIWrite 0010,00,0,7  //ec_dig=0x0;    Address(0x10[7:0])

//STEP: analogWrites/step4

//START: PLL Ana Trims


//START: Requesting/releasing SPI Access to PLL Pages

SPIWrite 0015,40,6,6  //digtop=0x1;    Address(0x15[7:6])
SPIWrite 0170,01,0,0  //pll_reg_spi_req_a=0x1;
     Address(0x170[7:0])
SPIWrite 0540,00,0,0  //Property_520h_0_0=0x0;
     Address(0x540[7:0])

SPIPoll 0171,0,0,01
SPIRead 0171,0,0

//Read     pll_reg_spi_a_ack=0x1(Meaning: );;
     Address(0x171[7:0])


//END: Requesting/releasing SPI Access to PLL Pages
```

```
SPIWrite 0015,00,6,6  //digtop=0x0;    Address(0x15[7:6])
SPIWrite 0015,01,0,0  //pll=0x1;       Address(0x15[7:0])
SPIWrite 005e,01,0,0  //Property_3ch_16_16=0x1;
     Address(0x5e[7:0])
SPIWrite 005d,ec,5,7  //Property_3ch_15_13=0x7;
     Address(0x5d[7:5])

//START: Requesting/releasing SPI Access to PLL Pages

SPIWrite 0015,00,0,0  //pll=0x0;       Address(0x15[7:0])
SPIWrite 0015,40,6,6  //digtop=0x1;    Address(0x15[7:6])
SPIWrite 0170,00,0,0  //pll_reg_spi_req_a=0x0;
     Address(0x170[7:0])
SPIWrite 0540,00,0,0  //Property_520h_0_0=0x0;
     Address(0x540[7:0])

WAIT 0.2

//END: Requesting/releasing SPI Access to PLL Pages

SPIWrite 050f,00,0,7  //Property_4ech_31_0=0xc0000;
     Address(0x50c[7:0],0x50d[7:0],0x50e[7:0],0x50f[7:0],0x510[7:
0])
SPIWrite 050e,0c,0,7
SPIWrite 050d,00,0,7
SPIWrite 050c,00,0,7
SPIWrite 0015,00,6,6  //digtop=0x0;    Address(0x15[7:6])
SPIWrite 0015,02,1,1  //ana_4t4r=0x1;  Address(0x15[7:1])
SPIWrite 00bb,00,0,7  //Property_98h_31_0=0x0;
     Address(0xb8[7:0],0xb9[7:0],0xba[7:0],0xbb[7:0],0xbc[7:0])
SPIWrite 00ba,00,0,7
SPIWrite 00b9,00,0,7
SPIWrite 00b8,00,0,7
SPIWrite 00bb,00,0,7  //Property_98h_31_0=0x8000;
     Address(0xb8[7:0],0xb9[7:0],0xba[7:0],0xbb[7:0],0xbc[7:0])
SPIWrite 00ba,00,0,7
SPIWrite 00b9,80,0,7
SPIWrite 00b8,00,0,7
SPIWrite 00bb,00,0,7  //Property_98h_31_0=0x0;
     Address(0xb8[7:0],0xb9[7:0],0xba[7:0],0xbb[7:0],0xbc[7:0])
SPIWrite 00ba,00,0,7
SPIWrite 00b9,00,0,7
SPIWrite 00b8,00,0,7

WAIT 0.1

//END: PLL Ana Trims

SPIWrite 0015,00,0,7  //ana_4t4r=0x0;  Address(0x15[7:1])

//STEP: jesdConfig/step0
```

```
//START: Configuring JESD Muxes and Pointers


//START: Configuring JESD TX Lane Mux

SPIWrite 0016,10,0,7  //jesd_subchip=0x1;   Address(0x16[7:4])
SPIWrite 0048,13,0,7  //txoctetpath0_sel=0x3;
      Address(0x48[7:0])
SPIWrite 0048,13,0,7  //txoctetpath1_sel=0x1;
      Address(0x48[7:4])
SPIWrite 0049,32,0,7  //txoctetpath2_sel=0x2;
      Address(0x49[7:0])
SPIWrite 0049,02,0,7  //txoctetpath3_sel=0x0;
      Address(0x49[7:4])
SPIWrite 004a,54,0,7  //txoctetpath4_sel=0x4;
      Address(0x4a[7:0])
SPIWrite 004a,54,0,7  //txoctetpath5_sel=0x5;
      Address(0x4a[7:4])
SPIWrite 004b,76,0,7  //txoctetpath6_sel=0x6;
      Address(0x4b[7:0])
SPIWrite 004b,76,0,7  //txoctetpath7_sel=0x7;
      Address(0x4b[7:4])
SPIWrite 004c,13,0,7  //txoctetpath0_clk_sel=0x3;
      Address(0x4c[7:0])
SPIWrite 004c,13,0,7  //txoctetpath1_clk_sel=0x1;
      Address(0x4c[7:4])
SPIWrite 004d,32,0,7  //txoctetpath2_clk_sel=0x2;
      Address(0x4d[7:0])
SPIWrite 004d,02,0,7  //txoctetpath3_clk_sel=0x0;
      Address(0x4d[7:4])
SPIWrite 004e,54,0,7  //txoctetpath4_clk_sel=0x4;
      Address(0x4e[7:0])
SPIWrite 004e,54,0,7  //txoctetpath5_clk_sel=0x5;
      Address(0x4e[7:4])
SPIWrite 004f,76,0,7  //txoctetpath6_clk_sel=0x6;
      Address(0x4f[7:0])
SPIWrite 004f,76,0,7  //txoctetpath7_clk_sel=0x7;
      Address(0x4f[7:4])

//END: Configuring JESD TX Lane Mux


//START: Configuring JESD RX Lane Mux

SPIWrite 0068,12,0,7  //rxoctetpath0_sel=0x2;
      Address(0x68[7:0])
SPIWrite 0068,12,0,7  //rxoctetpath1_sel=0x1;
      Address(0x68[7:4])
SPIWrite 0069,30,0,7  //rxoctetpath2_sel=0x0;
      Address(0x69[7:0])
SPIWrite 0069,40,0,7  //rxoctetpath3_sel=0x4;
      Address(0x69[7:4])
```

```
SPIWrite 006a,53,0,7  //rxoctetpath4_sel=0x3;
      Address(0x6a[7:0])
SPIWrite 006a,53,0,7  //rxoctetpath5_sel=0x5;
      Address(0x6a[7:4])
SPIWrite 006b,76,0,7  //rxoctetpath6_sel=0x6;
      Address(0x6b[7:0])
SPIWrite 006b,76,0,7  //rxoctetpath7_sel=0x7;
      Address(0x6b[7:4])
SPIWrite 006c,12,0,7  //rxoctetpath0_clk_sel=0x2;
      Address(0x6c[7:0])
SPIWrite 006c,12,0,7  //rxoctetpath1_clk_sel=0x1;
      Address(0x6c[7:4])
SPIWrite 006d,30,0,7  //rxoctetpath2_clk_sel=0x0;
      Address(0x6d[7:0])
SPIWrite 006d,40,0,7  //rxoctetpath3_clk_sel=0x4;
      Address(0x6d[7:4])
SPIWrite 006e,53,0,7  //rxoctetpath4_clk_sel=0x3;
      Address(0x6e[7:0])
SPIWrite 006e,53,0,7  //rxoctetpath5_clk_sel=0x5;
      Address(0x6e[7:4])
SPIWrite 006f,76,0,7  //rxoctetpath6_clk_sel=0x6;
      Address(0x6f[7:0])
SPIWrite 006f,76,0,7  //rxoctetpath7_clk_sel=0x7;
      Address(0x6f[7:4])

//END: Configuring JESD RX Lane Mux


//START: Configuring the DDC-JESD Data Muxes

SPIWrite 0034,00,0,7  //mux_sel_rxa_b1_i_for_2r1f_ab=0x0;
      Address(0x34[7:0])
SPIWrite 0034,00,0,7  //mux_sel_rxa_b1_q_for_2r1f_ab=0x0;
      Address(0x34[7:4])
SPIWrite 0035,22,0,7  //mux_sel_rxa_b2_i_for_2r1f_ab=0x2;
      Address(0x35[7:0])
SPIWrite 0035,22,0,7  //mux_sel_rxa_b2_q_for_2r1f_ab=0x2;
      Address(0x35[7:4])
SPIWrite 0036,44,0,7  //mux_sel_rxb_b1_i_for_2r1f_ab=0x4;
      Address(0x36[7:0])
SPIWrite 0036,44,0,7  //mux_sel_rxb_b1_q_for_2r1f_ab=0x4;
      Address(0x36[7:4])
SPIWrite 0037,66,0,7  //mux_sel_rxb_b2_i_for_2r1f_ab=0x6;
      Address(0x37[7:0])
SPIWrite 0037,66,0,7  //mux_sel_rxb_b2_q_for_2r1f_ab=0x6;
      Address(0x37[7:4])
SPIWrite 0038,40,0,7  //mux_sel_rxc_b1_i_for_2r1f_ab=0x0;
      Address(0x38[7:0])
SPIWrite 0038,00,0,7  //mux_sel_rxc_b1_q_for_2r1f_ab=0x0;
      Address(0x38[7:4])
SPIWrite 0039,52,0,7  //mux_sel_rxc_b2_i_for_2r1f_ab=0x2;
      Address(0x39[7:0])
```

```
SPIWrite 0039,22,0,7  //mux_sel_rxc_b2_q_for_2r1f_ab=0x2;
     Address(0x39[7:4])
SPIWrite 003a,64,0,7  //mux_sel_rxd_b1_i_for_2r1f_ab=0x4;
     Address(0x3a[7:0])
SPIWrite 003a,44,0,7  //mux_sel_rxd_b1_q_for_2r1f_ab=0x4;
     Address(0x3a[7:4])
SPIWrite 003b,76,0,7  //mux_sel_rxd_b2_i_for_2r1f_ab=0x6;
     Address(0x3b[7:0])
SPIWrite 003b,66,0,7  //mux_sel_rxd_b2_q_for_2r1f_ab=0x6;
     Address(0x3b[7:4])
SPIWrite 0040,00,0,7  //mux_sel_rxc_b1_i_for_2r1f_cd=0x0;
     Address(0x40[7:0])
SPIWrite 0040,00,0,7  //mux_sel_rxc_b1_q_for_2r1f_cd=0x0;
     Address(0x40[7:4])
SPIWrite 0041,22,0,7  //mux_sel_rxc_b2_i_for_2r1f_cd=0x2;
     Address(0x41[7:0])
SPIWrite 0041,22,0,7  //mux_sel_rxc_b2_q_for_2r1f_cd=0x2;
     Address(0x41[7:4])
SPIWrite 0042,24,0,7  //mux_sel_rxd_b1_i_for_2r1f_cd=0x4;
     Address(0x42[7:0])
SPIWrite 0042,44,0,7  //mux_sel_rxd_b1_q_for_2r1f_cd=0x4;
     Address(0x42[7:4])
SPIWrite 0043,36,0,7  //mux_sel_rxd_b2_i_for_2r1f_cd=0x6;
     Address(0x43[7:0])
SPIWrite 0043,66,0,7  //mux_sel_rxd_b2_q_for_2r1f_cd=0x6;
     Address(0x43[7:4])
SPIWrite 0044,50,0,7  //mux_sel_fba_i0_for_2r1f_ab=0x0;
     Address(0x44[7:0])
SPIWrite 0044,50,0,7  //mux_sel_fba_q0_for_2r1f_ab=0x0;
     Address(0x44[7:2])
SPIWrite 0044,50,0,7  //mux_sel_fba_i1_for_2r1f_ab=0x1;
     Address(0x44[7:4])
SPIWrite 0044,50,0,7  //mux_sel_fba_q1_for_2r1f_ab=0x1;
     Address(0x44[7:6])
SPIWrite 0045,fa,0,7  //mux_sel_fbc_i0_for_2r1f_ab=0x2;
     Address(0x45[7:0])
SPIWrite 0045,fa,0,7  //mux_sel_fbc_q0_for_2r1f_ab=0x2;
     Address(0x45[7:2])
SPIWrite 0045,fa,0,7  //mux_sel_fbc_i1_for_2r1f_ab=0x3;
     Address(0x45[7:4])
SPIWrite 0045,fa,0,7  //mux_sel_fbc_q1_for_2r1f_ab=0x3;
     Address(0x45[7:6])
SPIWrite 0046,fa,0,7  //mux_sel_fba_i0_for_2r1f_cd=0x2;
     Address(0x46[7:0])
SPIWrite 0046,fa,0,7  //mux_sel_fba_q0_for_2r1f_cd=0x2;
     Address(0x46[7:2])
SPIWrite 0046,fa,0,7  //mux_sel_fba_i1_for_2r1f_cd=0x3;
     Address(0x46[7:4])
SPIWrite 0046,fa,0,7  //mux_sel_fba_q1_for_2r1f_cd=0x3;
     Address(0x46[7:6])
SPIWrite 0047,50,0,7  //mux_sel_fbc_i0_for_2r1f_cd=0x0;
     Address(0x47[7:0])
```

```
SPIWrite 0047,50,0,7  //mux_sel_fbc_q0_for_2r1f_cd=0x0;
     Address(0x47[7:2])
SPIWrite 0047,50,0,7  //mux_sel_fbc_i1_for_2r1f_cd=0x1;
     Address(0x47[7:4])
SPIWrite 0047,50,0,7  //mux_sel_fbc_q1_for_2r1f_cd=0x1;
     Address(0x47[7:6])

//END: Configuring the DDC-JESD Data Muxes


//START: Configuring the JESD-DUC Data Muxes

SPIWrite 00cc,00,0,7  //mux_sel_for_txa_b0_i=0x0;
     Address(0xcc[7:0])
SPIWrite 00cc,00,0,7  //mux_sel_for_txa_b0_q=0x0;
     Address(0xcc[7:4])
SPIWrite 00cd,11,0,7  //mux_sel_for_txa_b1_i=0x1;
     Address(0xcd[7:0])
SPIWrite 00cd,11,0,7  //mux_sel_for_txa_b1_q=0x1;
     Address(0xcd[7:4])
SPIWrite 00ce,22,0,7  //mux_sel_for_txb_b0_i=0x2;
     Address(0xce[7:0])
SPIWrite 00ce,22,0,7  //mux_sel_for_txb_b0_q=0x2;
     Address(0xce[7:4])
SPIWrite 00cf,33,0,7  //mux_sel_for_txb_b1_i=0x3;
     Address(0xcf[7:0])
SPIWrite 00cf,33,0,7  //mux_sel_for_txb_b1_q=0x3;
     Address(0xcf[7:4])
SPIWrite 00d0,48,0,7  //mux_sel_for_txc_b0_i=0x8;
     Address(0xd0[7:0])
SPIWrite 00d0,88,0,7  //mux_sel_for_txc_b0_q=0x8;
     Address(0xd0[7:4])
SPIWrite 00d1,59,0,7  //mux_sel_for_txc_b1_i=0x9;
     Address(0xd1[7:0])
SPIWrite 00d1,99,0,7  //mux_sel_for_txc_b1_q=0x9;
     Address(0xd1[7:4])
SPIWrite 00d2,6a,0,7  //mux_sel_for_txd_b0_i=0xa;
     Address(0xd2[7:0])
SPIWrite 00d2,aa,0,7  //mux_sel_for_txd_b0_q=0xa;
     Address(0xd2[7:4])
SPIWrite 00d3,7b,0,7  //mux_sel_for_txd_b1_i=0xb;
     Address(0xd3[7:0])
SPIWrite 00d3,bb,0,7  //mux_sel_for_txd_b1_q=0xb;
     Address(0xd3[7:4])
SPIWrite 0060,10,0,7  //mux_sel_for_txa_ctrl=0x0;
     Address(0x60[7:0])
SPIWrite 0060,10,0,7  //mux_sel_for_txb_ctrl=0x1;
     Address(0x60[7:4])
SPIWrite 0061,34,0,7  //mux_sel_for_txc_ctrl=0x4;
     Address(0x61[7:0])
SPIWrite 0061,54,0,7  //mux_sel_for_txd_ctrl=0x5;
     Address(0x61[7:4])
```

```
//END: Configuring the JESD-DUC Data Muxes


//START: Configuring JESD TX Sync Mux

SPIWrite 0054,00,0,7  //adc_jesd_sync_n0_mux_sel=0x0;
     Address(0x54[7:0])
SPIWrite 0054,00,0,7  //adc_jesd_sync_n1_mux_sel=0x0;
     Address(0x54[7:4])
SPIWrite 0055,30,0,7  //adc_jesd_sync_n2_mux_sel=0x0;
     Address(0x55[7:0])
SPIWrite 0055,00,0,7  //adc_jesd_sync_n3_mux_sel=0x0;
     Address(0x55[7:4])
SPIWrite 0056,50,0,7  //adc_jesd_sync_n4_mux_sel=0x0;
     Address(0x56[7:0])
SPIWrite 0056,00,0,7  //adc_jesd_sync_n5_mux_sel=0x0;
     Address(0x56[7:4])

//END: Configuring JESD TX Sync Mux


//START: Configuring JESD RX Sync Mux

SPIWrite 00ca,e4,0,7  //dac_jesd_sync_n0_mux_sel=0x0;
     Address(0xca[7:0])
SPIWrite 00ca,e0,0,7  //dac_jesd_sync_n1_mux_sel=0x0;
     Address(0xca[7:2])
SPIWrite 00ca,c0,0,7  //dac_jesd_sync_n2_mux_sel=0x0;
     Address(0xca[7:4])
SPIWrite 00ca,00,0,7  //dac_jesd_sync_n3_mux_sel=0x0;
     Address(0xca[7:6])

//END: Configuring JESD RX Sync Mux

SPIWrite 009c,03,0,7  //rx_clk_dithered_mode_en=0x1;
     Address(0x9c[7:1])
SPIWrite 009e,03,0,7  //fb_clk_dithered_mode_en=0x1;
     Address(0x9e[7:1])
SPIWrite 009c,03,0,7  //rx_clk_disable=0x1;
     Address(0x9c[7:0])
SPIWrite 00a0,02,0,7  //tx_clk_disable=0x0;
     Address(0xa0[7:0])
SPIWrite 00a0,00,0,7  //tx_clk_dithered_mode_en=0x0;
     Address(0xa0[7:1])

//END: Configuring JESD Muxes and Pointers


//START: Setting JESD SyncB Pin Mode
```

```
//END: Setting JESD SyncB Pin Mode

SPIWrite 0016,00,0,7  //jesd_subchip=0x0;   Address(0x16[7:4])

//STEP: jesdConfig/step1

//START: Configuring ADC JESD TX

SPIWrite 0016,01,0,7  //adc_jesd=0x1; Address(0x16[7:0])
SPIWrite 006d,07,0,7  //link0_init_state=0x1;
      Address(0x6d[7:0])
SPIWrite 006d,07,0,7  //link1_init_state=0x1;
      Address(0x6d[7:1])
SPIWrite 006d,07,0,7  //link2_init_state=0x1;
      Address(0x6d[7:2])
SPIWrite 006f,02,0,7  //init_state_gearbox_spi_ovr=0x1;
      Address(0x6f[7:1])
SPIWrite 006c,0f,0,7  //lane0_gearbox_init_state=0x1;
      Address(0x6c[7:0])
SPIWrite 006c,0f,0,7  //lane1_gearbox_init_state=0x1;
      Address(0x6c[7:1])
SPIWrite 006c,0f,0,7  //lane2_gearbox_init_state=0x1;
      Address(0x6c[7:2])
SPIWrite 006c,0f,0,7  //lane3_gearbox_init_state=0x1;
      Address(0x6c[7:3])
SPIWrite 006c,0e,0,7  //lane0_gearbox_init_state=0x0;
      Address(0x6c[7:0])
SPIWrite 006c,0c,0,7  //lane1_gearbox_init_state=0x0;
      Address(0x6c[7:1])
SPIWrite 006c,08,0,7  //lane2_gearbox_init_state=0x0;
      Address(0x6c[7:2])
SPIWrite 006c,00,0,7  //lane3_gearbox_init_state=0x0;
      Address(0x6c[7:3])
SPIWrite 006e,0f,0,7  //lane0_serdes_fifo_init_state=0x1;
      Address(0x6e[7:0])
SPIWrite 006e,0f,0,7  //lane1_serdes_fifo_init_state=0x1;
      Address(0x6e[7:1])
SPIWrite 006e,0f,0,7  //lane2_serdes_fifo_init_state=0x1;
      Address(0x6e[7:2])
SPIWrite 006e,0f,0,7  //lane3_serdes_fifo_init_state=0x1;
      Address(0x6e[7:3])
SPIWrite 005c,1f,0,7  //rx_root_clk_dither_en=0x1;
      Address(0x5c[7:0])
SPIWrite 005c,1f,0,7  //fb_root_clk_dither_en=0x1;
      Address(0x5c[7:1])
SPIWrite 005c,1b,0,7  //ddc_rd_clk_dither_en=0x0;
      Address(0x5c[7:2])
SPIWrite 005c,13,0,7  //jesd_clk_dither_en=0x0;
      Address(0x5c[7:3])
SPIWrite 005c,03,0,7  //jesd_clk_div2_dither_en=0x0;
      Address(0x5c[7:4])
SPIWrite 0021,01,0,7  //jesd_system_mode=0x1;
```

```
      Address(0x21[7:0])
SPIWrite 005d,01,0,7  //rx_adc_clk_sysref_mux=0x1;
      Address(0x5d[7:0])
SPIWrite 005d,01,0,7  //fb_adc_clk_sysref_mux=0x0;
      Address(0x5d[7:1])
SPIWrite 0024,0f,0,7  //jesd_clear_data=0xf;
      Address(0x24[7:0])
SPIWrite 0069,8c,0,7  //serdes_fifo_read_dly_lane0=0xc;
      Address(0x69[7:0])
SPIWrite 0069,cc,0,7  //serdes_fifo_read_dly_lane1=0xc;
      Address(0x69[7:4])
SPIWrite 006a,8c,0,7  //serdes_fifo_read_dly_lane2=0xc;
      Address(0x6a[7:0])
SPIWrite 006a,cc,0,7  //serdes_fifo_read_dly_lane3=0xc;
      Address(0x6a[7:4])
SPIWrite 0040,01,0,7  //rx1_root_clk_div_m=0x1;
      Address(0x40[7:0])
SPIWrite 0041,00,0,7  //rx1_root_clk_div_n_m1=0x0;
      Address(0x41[7:0])
SPIWrite 0046,01,0,7  //ddc_rd_clk_rx1_div_m=0x1;
      Address(0x46[7:0])
SPIWrite 0047,05,0,7  //ddc_rd_clk_rx1_div_n_m1=0x5;
      Address(0x47[7:0])
SPIWrite 004c,02,0,7  //jesd_clk_rx1_div_m=0x2;
      Address(0x4c[7:0])
SPIWrite 004d,02,0,7  //jesd_clk_rx1_div_n_m1=0x2;
      Address(0x4d[7:0])
SPIWrite 0034,14,0,7  //rx1_jesd_mode=0x14;
      Address(0x34[7:0])
SPIWrite 0084,00,0,7  //link0_k_m1=0x0;
      Address(0x84[7:0],0x85[7:0])
SPIWrite 0079,00,0,7  //link0_ila_k_m1=0x0;
      Address(0x79[7:0],0x7a[7:0])
SPIWrite 0042,01,0,7  //rx2_root_clk_div_m=0x1;
      Address(0x42[7:0])
SPIWrite 0043,00,0,7  //rx2_root_clk_div_n_m1=0x0;
      Address(0x43[7:0])
SPIWrite 0048,01,0,7  //ddc_rd_clk_rx2_div_m=0x1;
      Address(0x48[7:0])
SPIWrite 0049,05,0,7  //ddc_rd_clk_rx2_div_n_m1=0x5;
      Address(0x49[7:0])
SPIWrite 004e,02,0,7  //jesd_clk_rx2_div_m=0x2;
      Address(0x4e[7:0])
SPIWrite 004f,02,0,7  //jesd_clk_rx2_div_n_m1=0x2;
      Address(0x4f[7:0])
SPIWrite 0035,14,0,7  //rx2_jesd_mode=0x14;
      Address(0x35[7:0])
SPIWrite 009c,00,0,7  //link1_k_m1=0x0;
      Address(0x9c[7:0],0x9d[7:0])
SPIWrite 0091,00,0,7  //link1_ila_k_m1=0x0;
      Address(0x91[7:0],0x92[7:0])
SPIWrite 0044,02,0,7  //fb_root_clk_div_m=0x2;
```

```
     Address(0x44[7:0])
SPIWrite 0045,02,0,7  //fb_root_clk_div_n_m1=0x2;
     Address(0x45[7:0])
SPIWrite 004a,01,0,7  //ddc_rd_clk_fb_div_m=0x1;
     Address(0x4a[7:0])
SPIWrite 004b,03,0,7  //ddc_rd_clk_fb_div_n_m1=0x3;
     Address(0x4b[7:0])
SPIWrite 0050,01,0,7  //jesd_clk_fb_div_m=0x1;
     Address(0x50[7:0])
SPIWrite 0051,00,0,7  //jesd_clk_fb_div_n_m1=0x0;
     Address(0x51[7:0])
SPIWrite 0036,0b,0,7  //fb_jesd_mode=0xb;   Address(0x36[7:0])
SPIWrite 00b4,00,0,7  //link2_k_m1=0x0;
     Address(0xb4[7:0],0xb5[7:0])
SPIWrite 00a9,00,0,7  //link2_ila_k_m1=0x0;
     Address(0xa9[7:0],0xaa[7:0])
SPIWrite 0020,02,0,7  //jesd_std_sel=0x2;   Address(0x20[7:0])
SPIWrite 0077,01,0,7  //link0_scr=0x0;      Address(0x77[7:7])
SPIWrite 008f,01,0,7  //link1_scr=0x0;      Address(0x8f[7:7])
SPIWrite 00a7,01,0,7  //link2_scr=0x0;      Address(0xa7[7:7])
SPIWrite 0023,05,0,7  //lane_ena=0x5; Address(0x23[7:0])
SPIWrite 003c,02,0,7  //sel_rx1_jesd_mode_1s_2s_ovr=0x1;
     Address(0x3c[7:1])
SPIWrite 003c,02,0,7  //sel_rx1_jesd_mode_1s_2s_val=0x0;
     Address(0x3c[7:0])
SPIWrite 003c,0a,0,7  //sel_rx2_jesd_mode_1s_2s_ovr=0x1;
     Address(0x3c[7:3])
SPIWrite 003c,0a,0,7  //sel_rx2_jesd_mode_1s_2s_val=0x0;
     Address(0x3c[7:2])
SPIWrite 003c,2a,0,7  //sel_fb_jesd_mode_1s_2s_ovr=0x1;
     Address(0x3c[7:5])
SPIWrite 003c,3a,0,7  //sel_fb_jesd_mode_1s_2s_val=0x1;
     Address(0x3c[7:4])
SPIWrite 0083,01,0,7  //link0_jesd_ila_config_override=0x1;
     Address(0x83[7:0])
SPIWrite 009b,01,0,7  //link1_jesd_ila_config_override=0x1;
     Address(0x9b[7:0])
SPIWrite 0078,0f,0,7  //link0_ila_f_m1=0xf;
     Address(0x78[7:0],0x79[7:0])
SPIWrite 0090,0f,0,7  //link1_ila_f_m1=0xf;
     Address(0x90[7:0],0x91[7:0])
SPIWrite 00a8,07,0,7  //link2_ila_f_m1=0x7;
     Address(0xa8[7:0],0xa9[7:0])
SPIWrite 007a,07,0,7  //link0_ila_m_m1=0x7;
     Address(0x7a[7:0],0x7b[7:0])
SPIWrite 0092,07,0,7  //link1_ila_m_m1=0x7;
     Address(0x92[7:0],0x93[7:0])
SPIWrite 00aa,01,0,7  //link2_ila_m_m1=0x1;
     Address(0xaa[7:0],0xab[7:0])
SPIWrite 0077,03,0,7  //link0_ila_l_m1=0x3;
     Address(0x77[7:0])
SPIWrite 008f,03,0,7  //link1_ila_l_m1=0x3;
```

```
     Address(0x8f[7:0])
SPIWrite 00a7,01,0,7  //link2_ila_l_m1=0x1;
     Address(0xa7[7:0])
SPIWrite 007b,0f,0,7  //link0_ila_n_m1=0xf;
     Address(0x7b[7:0])
SPIWrite 0093,0f,0,7  //link1_ila_n_m1=0xf;
     Address(0x93[7:0])
SPIWrite 00ab,0f,0,7  //link2_ila_n_m1=0xf;
     Address(0xab[7:0])
SPIWrite 00bc,00,0,7  //lid0=0x0;      Address(0xbc[7:0])
SPIWrite 00bd,01,0,7  //lid1=0x1;      Address(0xbd[7:0])
SPIWrite 00be,02,0,7  //lid2=0x2;      Address(0xbe[7:0])
SPIWrite 00bf,03,0,7  //lid3=0x3;      Address(0xbf[7:0])
SPIWrite 00e4,42,0,7  //msf_rx1_offset_default_mode0=0x2;
     Address(0xe4[7:0])
SPIWrite 00e4,22,0,7  //msf_rx1_offset_default_mode1=0x2;
     Address(0xe4[7:4])
SPIWrite 00e5,83,0,7  //msf_rx1_offset_default_mode2=0x3;
     Address(0xe5[7:0])
SPIWrite 00e5,43,0,7  //msf_rx1_offset_default_mode3=0x4;
     Address(0xe5[7:4])
SPIWrite 00e6,42,0,7  //msf_rx2_offset_default_mode0=0x2;
     Address(0xe6[7:0])
SPIWrite 00e6,22,0,7  //msf_rx2_offset_default_mode1=0x2;
     Address(0xe6[7:4])
SPIWrite 00e7,83,0,7  //msf_rx2_offset_default_mode2=0x3;
     Address(0xe7[7:0])
SPIWrite 00e7,43,0,7  //msf_rx2_offset_default_mode3=0x4;
     Address(0xe7[7:4])
SPIWrite 00e8,42,0,7  //msf_fb_offset_default_mode0=0x2;
     Address(0xe8[7:0])
SPIWrite 00e8,22,0,7  //msf_fb_offset_default_mode1=0x2;
     Address(0xe8[7:4])
SPIWrite 00e9,83,0,7  //msf_fb_offset_default_mode2=0x3;
     Address(0xe9[7:0])
SPIWrite 00e9,43,0,7  //msf_fb_offset_default_mode3=0x4;
     Address(0xe9[7:4])
SPIWrite 0037,06,0,7  //rx1_ctrlmode_12b_trunc_en=0x0;
     Address(0x37[7:0])
SPIWrite 0037,04,0,7  //rx2_ctrlmode_12b_trunc_en=0x0;
     Address(0x37[7:1])
SPIWrite 0037,00,0,7  //fb_ctrlmode_12b_trunc_en=0x0;
     Address(0x37[7:2])
SPIWrite 0122,02,0,7  //ctrl_tdd_rx1_mapper_sig_invalid=0x2;
     Address(0x122[7:0])
SPIWrite 0122,0a,0,7  //ctrl_tdd_rx2_mapper_sig_invalid=0x2;
     Address(0x122[7:2])
SPIWrite 0122,2a,0,7  //ctrl_tdd_fb_mapper_sig_invalid=0x2;
     Address(0x122[7:4])
SPIWrite 011c,03,0,7  //ctrl_rx1_mapper_clk_gating=0x3;
     Address(0x11c[7:0])
SPIWrite 011d,03,0,7  //ctrl_rx3_rx4_clk_gating=0x3;
```

```
      Address(0x11d[7:0])
SPIWrite 011c,33,0,7  //ctrl_fb_mapper_clk_gating=0x3;
      Address(0x11c[7:4])

//END: Done Configuring ADC JESD TX


//START: Configuring ADC JESD TX

SPIWrite 0016,02,0,7  //adc_jesd=0x2; Address(0x16[7:0])
SPIWrite 006d,07,0,7  //link0_init_state=0x1;
      Address(0x6d[7:0])
SPIWrite 006d,07,0,7  //link1_init_state=0x1;
      Address(0x6d[7:1])
SPIWrite 006d,07,0,7  //link2_init_state=0x1;
      Address(0x6d[7:2])
SPIWrite 006f,02,0,7  //init_state_gearbox_spi_ovr=0x1;
      Address(0x6f[7:1])
SPIWrite 006c,0f,0,7  //lane0_gearbox_init_state=0x1;
      Address(0x6c[7:0])
SPIWrite 006c,0f,0,7  //lane1_gearbox_init_state=0x1;
      Address(0x6c[7:1])
SPIWrite 006c,0f,0,7  //lane2_gearbox_init_state=0x1;
      Address(0x6c[7:2])
SPIWrite 006c,0f,0,7  //lane3_gearbox_init_state=0x1;
      Address(0x6c[7:3])
SPIWrite 006c,0e,0,7  //lane0_gearbox_init_state=0x0;
      Address(0x6c[7:0])
SPIWrite 006c,0c,0,7  //lane1_gearbox_init_state=0x0;
      Address(0x6c[7:1])
SPIWrite 006c,08,0,7  //lane2_gearbox_init_state=0x0;
      Address(0x6c[7:2])
SPIWrite 006c,00,0,7  //lane3_gearbox_init_state=0x0;
      Address(0x6c[7:3])
SPIWrite 006e,0f,0,7  //lane0_serdes_fifo_init_state=0x1;
      Address(0x6e[7:0])
SPIWrite 006e,0f,0,7  //lane1_serdes_fifo_init_state=0x1;
      Address(0x6e[7:1])
SPIWrite 006e,0f,0,7  //lane2_serdes_fifo_init_state=0x1;
      Address(0x6e[7:2])
SPIWrite 006e,0f,0,7  //lane3_serdes_fifo_init_state=0x1;
      Address(0x6e[7:3])
SPIWrite 005c,1f,0,7  //rx_root_clk_dither_en=0x1;
      Address(0x5c[7:0])
SPIWrite 005c,1f,0,7  //fb_root_clk_dither_en=0x1;
      Address(0x5c[7:1])
SPIWrite 005c,1b,0,7  //ddc_rd_clk_dither_en=0x0;
      Address(0x5c[7:2])
SPIWrite 005c,13,0,7  //jesd_clk_dither_en=0x0;
      Address(0x5c[7:3])
SPIWrite 005c,03,0,7  //jesd_clk_div2_dither_en=0x0;
      Address(0x5c[7:4])
```

```
SPIWrite 0021,01,0,7  //jesd_system_mode=0x1;
     Address(0x21[7:0])
SPIWrite 005d,01,0,7  //rx_adc_clk_sysref_mux=0x1;
     Address(0x5d[7:0])
SPIWrite 005d,01,0,7  //fb_adc_clk_sysref_mux=0x0;
     Address(0x5d[7:1])
SPIWrite 0024,0f,0,7  //jesd_clear_data=0xf;
     Address(0x24[7:0])
SPIWrite 0069,8c,0,7  //serdes_fifo_read_dly_lane0=0xc;
     Address(0x69[7:0])
SPIWrite 0069,cc,0,7  //serdes_fifo_read_dly_lane1=0xc;
     Address(0x69[7:4])
SPIWrite 006a,8c,0,7  //serdes_fifo_read_dly_lane2=0xc;
     Address(0x6a[7:0])
SPIWrite 006a,cc,0,7  //serdes_fifo_read_dly_lane3=0xc;
     Address(0x6a[7:4])
SPIWrite 0040,01,0,7  //rx1_root_clk_div_m=0x1;
     Address(0x40[7:0])
SPIWrite 0041,00,0,7  //rx1_root_clk_div_n_m1=0x0;
     Address(0x41[7:0])
SPIWrite 0046,01,0,7  //ddc_rd_clk_rx1_div_m=0x1;
     Address(0x46[7:0])
SPIWrite 0047,05,0,7  //ddc_rd_clk_rx1_div_n_m1=0x5;
     Address(0x47[7:0])
SPIWrite 004c,02,0,7  //jesd_clk_rx1_div_m=0x2;
     Address(0x4c[7:0])
SPIWrite 004d,02,0,7  //jesd_clk_rx1_div_n_m1=0x2;
     Address(0x4d[7:0])
SPIWrite 0034,14,0,7  //rx1_jesd_mode=0x14;
     Address(0x34[7:0])
SPIWrite 0084,00,0,7  //link0_k_m1=0x0;
     Address(0x84[7:0],0x85[7:0])
SPIWrite 0079,00,0,7  //link0_ila_k_m1=0x0;
     Address(0x79[7:0],0x7a[7:0])
SPIWrite 0042,01,0,7  //rx2_root_clk_div_m=0x1;
     Address(0x42[7:0])
SPIWrite 0043,00,0,7  //rx2_root_clk_div_n_m1=0x0;
     Address(0x43[7:0])
SPIWrite 0048,01,0,7  //ddc_rd_clk_rx2_div_m=0x1;
     Address(0x48[7:0])
SPIWrite 0049,05,0,7  //ddc_rd_clk_rx2_div_n_m1=0x5;
     Address(0x49[7:0])
SPIWrite 004e,02,0,7  //jesd_clk_rx2_div_m=0x2;
     Address(0x4e[7:0])
SPIWrite 004f,02,0,7  //jesd_clk_rx2_div_n_m1=0x2;
     Address(0x4f[7:0])
SPIWrite 0035,14,0,7  //rx2_jesd_mode=0x14;
     Address(0x35[7:0])
SPIWrite 009c,00,0,7  //link1_k_m1=0x0;
     Address(0x9c[7:0],0x9d[7:0])
SPIWrite 0091,00,0,7  //link1_ila_k_m1=0x0;
     Address(0x91[7:0],0x92[7:0])
```

```
SPIWrite 0044,02,0,7  //fb_root_clk_div_m=0x2;
     Address(0x44[7:0])
SPIWrite 0045,02,0,7  //fb_root_clk_div_n_m1=0x2;
     Address(0x45[7:0])
SPIWrite 004a,01,0,7  //ddc_rd_clk_fb_div_m=0x1;
     Address(0x4a[7:0])
SPIWrite 004b,03,0,7  //ddc_rd_clk_fb_div_n_m1=0x3;
     Address(0x4b[7:0])
SPIWrite 0050,01,0,7  //jesd_clk_fb_div_m=0x1;
     Address(0x50[7:0])
SPIWrite 0051,00,0,7  //jesd_clk_fb_div_n_m1=0x0;
     Address(0x51[7:0])
SPIWrite 0036,0b,0,7  //fb_jesd_mode=0xb;   Address(0x36[7:0])
SPIWrite 00b4,00,0,7  //link2_k_m1=0x0;
     Address(0xb4[7:0],0xb5[7:0])
SPIWrite 00a9,00,0,7  //link2_ila_k_m1=0x0;
     Address(0xa9[7:0],0xaa[7:0])
SPIWrite 0020,02,0,7  //jesd_std_sel=0x2;   Address(0x20[7:0])
SPIWrite 0077,01,0,7  //link0_scr=0x0;      Address(0x77[7:7])
SPIWrite 008f,01,0,7  //link1_scr=0x0;      Address(0x8f[7:7])
SPIWrite 00a7,01,0,7  //link2_scr=0x0;      Address(0xa7[7:7])
SPIWrite 0023,00,0,7  //lane_ena=0x0; Address(0x23[7:0])
SPIWrite 003c,02,0,7  //sel_rx1_jesd_mode_1s_2s_ovr=0x1;
     Address(0x3c[7:1])
SPIWrite 003c,02,0,7  //sel_rx1_jesd_mode_1s_2s_val=0x0;
     Address(0x3c[7:0])
SPIWrite 003c,0a,0,7  //sel_rx2_jesd_mode_1s_2s_ovr=0x1;
     Address(0x3c[7:3])
SPIWrite 003c,0a,0,7  //sel_rx2_jesd_mode_1s_2s_val=0x0;
     Address(0x3c[7:2])
SPIWrite 003c,2a,0,7  //sel_fb_jesd_mode_1s_2s_ovr=0x1;
     Address(0x3c[7:5])
SPIWrite 003c,3a,0,7  //sel_fb_jesd_mode_1s_2s_val=0x1;
     Address(0x3c[7:4])
SPIWrite 0083,01,0,7  //link0_jesd_ila_config_override=0x1;
     Address(0x83[7:0])
SPIWrite 009b,01,0,7  //link1_jesd_ila_config_override=0x1;
     Address(0x9b[7:0])
SPIWrite 0078,0f,0,7  //link0_ila_f_m1=0xf;
     Address(0x78[7:0],0x79[7:0])
SPIWrite 0090,0f,0,7  //link1_ila_f_m1=0xf;
     Address(0x90[7:0],0x91[7:0])
SPIWrite 00a8,07,0,7  //link2_ila_f_m1=0x7;
     Address(0xa8[7:0],0xa9[7:0])
SPIWrite 007a,07,0,7  //link0_ila_m_m1=0x7;
     Address(0x7a[7:0],0x7b[7:0])
SPIWrite 0092,07,0,7  //link1_ila_m_m1=0x7;
     Address(0x92[7:0],0x93[7:0])
SPIWrite 00aa,01,0,7  //link2_ila_m_m1=0x1;
     Address(0xaa[7:0],0xab[7:0])
SPIWrite 0077,03,0,7  //link0_ila_l_m1=0x3;
     Address(0x77[7:0])
```

```
SPIWrite 008f,03,0,7  //link1_ila_l_m1=0x3;
     Address(0x8f[7:0])
SPIWrite 00a7,01,0,7  //link2_ila_l_m1=0x1;
     Address(0xa7[7:0])
SPIWrite 007b,0f,0,7  //link0_ila_n_m1=0xf;
     Address(0x7b[7:0])
SPIWrite 0093,0f,0,7  //link1_ila_n_m1=0xf;
     Address(0x93[7:0])
SPIWrite 00ab,0f,0,7  //link2_ila_n_m1=0xf;
     Address(0xab[7:0])
SPIWrite 00bc,04,0,7  //lid0=0x4;     Address(0xbc[7:0])
SPIWrite 00bd,05,0,7  //lid1=0x5;     Address(0xbd[7:0])
SPIWrite 00be,06,0,7  //lid2=0x6;     Address(0xbe[7:0])
SPIWrite 00bf,07,0,7  //lid3=0x7;     Address(0xbf[7:0])
SPIWrite 00e4,42,0,7  //msf_rx1_offset_default_mode0=0x2;
     Address(0xe4[7:0])
SPIWrite 00e4,22,0,7  //msf_rx1_offset_default_mode1=0x2;
     Address(0xe4[7:4])
SPIWrite 00e5,83,0,7  //msf_rx1_offset_default_mode2=0x3;
     Address(0xe5[7:0])
SPIWrite 00e5,43,0,7  //msf_rx1_offset_default_mode3=0x4;
     Address(0xe5[7:4])
SPIWrite 00e6,42,0,7  //msf_rx2_offset_default_mode0=0x2;
     Address(0xe6[7:0])
SPIWrite 00e6,22,0,7  //msf_rx2_offset_default_mode1=0x2;
     Address(0xe6[7:4])
SPIWrite 00e7,83,0,7  //msf_rx2_offset_default_mode2=0x3;
     Address(0xe7[7:0])
SPIWrite 00e7,43,0,7  //msf_rx2_offset_default_mode3=0x4;
     Address(0xe7[7:4])
SPIWrite 00e8,42,0,7  //msf_fb_offset_default_mode0=0x2;
     Address(0xe8[7:0])
SPIWrite 00e8,22,0,7  //msf_fb_offset_default_mode1=0x2;
     Address(0xe8[7:4])
SPIWrite 00e9,83,0,7  //msf_fb_offset_default_mode2=0x3;
     Address(0xe9[7:0])
SPIWrite 00e9,43,0,7  //msf_fb_offset_default_mode3=0x4;
     Address(0xe9[7:4])
SPIWrite 0037,06,0,7  //rx1_ctrlmode_12b_trunc_en=0x0;
     Address(0x37[7:0])
SPIWrite 0037,04,0,7  //rx2_ctrlmode_12b_trunc_en=0x0;
     Address(0x37[7:1])
SPIWrite 0037,00,0,7  //fb_ctrlmode_12b_trunc_en=0x0;
     Address(0x37[7:2])
SPIWrite 0122,02,0,7  //ctrl_tdd_rx1_mapper_sig_invalid=0x2;
     Address(0x122[7:0])
SPIWrite 0122,0a,0,7  //ctrl_tdd_rx2_mapper_sig_invalid=0x2;
     Address(0x122[7:2])
SPIWrite 0122,2a,0,7  //ctrl_tdd_fb_mapper_sig_invalid=0x2;
     Address(0x122[7:4])
SPIWrite 011c,03,0,7  //ctrl_rx1_mapper_clk_gating=0x3;
     Address(0x11c[7:0])
```

```
SPIWrite 011d,03,0,7  //ctrl_rx3_rx4_clk_gating=0x3;
     Address(0x11d[7:0])
SPIWrite 011c,33,0,7  //ctrl_fb_mapper_clk_gating=0x3;
     Address(0x11c[7:4])

//END: Done Configuring ADC JESD TX

SPIWrite 0016,00,0,7  //adc_jesd=0x0; Address(0x16[7:0])

//STEP: jesdConfig/step2

//START: Configuring DAC JESD RX

SPIWrite 0016,04,0,7  //dac_jesd=0x1; Address(0x16[7:2])
SPIWrite 006c,00,0,7  //link0_k_m1=0x0;
     Address(0x6c[7:0],0x6d[7:0])
SPIWrite 006d,00,0,7  //link1_k_m1=0x0;
     Address(0x6d[7:0],0x6e[7:0])
SPIWrite 0057,00,0,7  //link1_ila_k_m1=0x0;
     Address(0x57[7:0],0x58[7:0])
SPIWrite 0049,00,0,7  //link0_ila_k_m1=0x0;
     Address(0x49[7:0],0x4a[7:0])
SPIWrite 0069,00,0,7  //link0_rbd_m1=0x3;
     Address(0x68[7:0],0x69[7:0],0x6a[7:0])
SPIWrite 0068,03,0,7
SPIWrite 006b,00,0,7  //link1_rbd_m1=0x3;
     Address(0x6a[7:0],0x6b[7:0],0x6c[7:0])
SPIWrite 006a,03,0,7
SPIWrite 0024,5e,0,7  //gearbox_init_state_ovr=0x1;
     Address(0x24[7:6])
SPIWrite 0025,ff,0,7  //gearbox_init_state_lane0_val=0x1;
     Address(0x25[7:0])
SPIWrite 0025,ff,0,7  //gearbox_init_state_lane1_val=0x1;
     Address(0x25[7:1])
SPIWrite 0025,ff,0,7  //gearbox_init_state_lane2_val=0x1;
     Address(0x25[7:2])
SPIWrite 0025,ff,0,7  //gearbox_init_state_lane3_val=0x1;
     Address(0x25[7:3])
SPIWrite 0025,fe,0,7  //gearbox_init_state_lane0_val=0x0;
     Address(0x25[7:0])
SPIWrite 0025,fc,0,7  //gearbox_init_state_lane1_val=0x0;
     Address(0x25[7:1])
SPIWrite 0025,f8,0,7  //gearbox_init_state_lane2_val=0x0;
     Address(0x25[7:2])
SPIWrite 0025,f0,0,7  //gearbox_init_state_lane3_val=0x0;
     Address(0x25[7:3])
SPIWrite 0020,03,0,7  //link0_init_state=0x1;
     Address(0x20[7:0])
SPIWrite 0020,03,0,7  //link1_init_state=0x1;
     Address(0x20[7:1])
SPIWrite 0064,ff,0,7  //jesd_clear_data=0xf;
     Address(0x64[7:4])
```

```
SPIWrite 0040,04,0,7  //link0_comma_align_lock_reset_disable=0x1;
     Address(0x40[7:2])
SPIWrite 0040,0c,0,7  //link1_comma_align_lock_reset_disable=0x1;
     Address(0x40[7:3])
SPIWrite 00ac,04,0,7  //link0_emb_align_lock_reset_disable=0x1;
     Address(0xac[7:2])
SPIWrite 00ac,0c,0,7  //link1_emb_align_lock_reset_disable=0x1;
     Address(0xac[7:3])
SPIWrite 002c,01,0,7  //root_clk_tx1_div_m=0x1;
     Address(0x2c[7:0])
SPIWrite 002d,00,0,7  //root_clk_tx1_div_n_m1=0x0;
     Address(0x2d[7:0])
SPIWrite 002e,01,0,7  //root_clk_tx2_div_m=0x1;
     Address(0x2e[7:0])
SPIWrite 002f,00,0,7  //root_clk_tx2_div_n_m1=0x0;
     Address(0x2f[7:0])
SPIWrite 0030,01,0,7  //duc_clk_tx1_div_m=0x1;
     Address(0x30[7:0])
SPIWrite 0031,02,0,7  //duc_clk_tx1_div_n_m1=0x2;
     Address(0x31[7:0])
SPIWrite 0032,01,0,7  //duc_clk_tx2_div_m=0x1;
     Address(0x32[7:0])
SPIWrite 0033,02,0,7  //duc_clk_tx2_div_n_m1=0x2;
     Address(0x33[7:0])
SPIWrite 0034,02,0,7  //jesd_clk_tx1_div_m=0x2;
     Address(0x34[7:0])
SPIWrite 0035,02,0,7  //jesd_clk_tx1_div_n_m1=0x2;
     Address(0x35[7:0])
SPIWrite 0036,02,0,7  //jesd_clk_tx2_div_m=0x2;
     Address(0x36[7:0])
SPIWrite 0037,02,0,7  //jesd_clk_tx2_div_n_m1=0x2;
     Address(0x37[7:0])
SPIWrite 0022,41,0,7  //link0_jesd_mode=0x1;
     Address(0x22[7:0])
SPIWrite 0023,41,0,7  //link1_jesd_mode=0x1;
     Address(0x23[7:0])
SPIWrite 0022,41,0,7  //link0_jesd_sample_mode=0x1;
     Address(0x22[7:6])
SPIWrite 0023,41,0,7  //link1_jesd_sample_mode=0x1;
     Address(0x23[7:6])
SPIWrite 0038,1f,0,7  //tx_root_clk_div_dither_en=0x1;
     Address(0x38[7:0])
SPIWrite 0038,1d,0,7  //duc_clk_io_div_dither_en=0x0;
     Address(0x38[7:1])
SPIWrite 0038,19,0,7  //duc_clk_div_dither_en=0x0;
     Address(0x38[7:2])
SPIWrite 0038,11,0,7  //jesd_clk_div_dither_en=0x0;
     Address(0x38[7:3])
SPIWrite 0038,01,0,7  //jesd_clk_div2_div_dither_en=0x0;
     Address(0x38[7:4])
SPIWrite 0026,00,0,7  //num_links=0x0;      Address(0x26[7:2])
SPIWrite 0042,7f,0,7  //comma_align_valid_thresh=0x7f;
```

```
      Address(0x42[7:0])
SPIWrite 00ad,86,0,7  //emb_align_valid_thresh=0x6;
      Address(0xad[7:0])
SPIWrite 0078,00,0,7  //link0_sync_request_ena=0x0;
      Address(0x78[7:0],0x79[7:0])
SPIWrite 0079,00,0,7  //link1_sync_request_ena=0x0;
      Address(0x79[7:0],0x7a[7:0])
SPIWrite 007a,00,0,7  //link0_error_ena=0x0;
      Address(0x7a[7:0],0x7b[7:0])
SPIWrite 007b,00,0,7  //link1_error_ena=0x0;
      Address(0x7b[7:0],0x7c[7:0])
SPIWrite 0103,00,0,7  //alarms_clear=0xbf;
      Address(0x100[7:0],0x101[7:0],0x102[7:0],0x103[7:0],0x104[7:
0],0x104[7:0],0x105[7:0],0x106[7:0],0x107[7:0],0x108[7:0])
SPIWrite 0102,00,0,7
SPIWrite 0101,00,0,7
SPIWrite 0100,bf,0,7
SPIWrite 0107,00,0,7
SPIWrite 0106,00,0,7
SPIWrite 0105,00,0,7
SPIWrite 0104,00,0,7
SPIWrite 00fb,00,0,7  //alarms_mask=0xbf;
      Address(0xf8[7:0],0xf9[7:0],0xfa[7:0],0xfb[7:0],0xfc[7:0],0x
fc[7:0],0xfd[7:0],0xfe[7:0],0xff[7:0],0x100[7:0])
SPIWrite 00fa,00,0,7
SPIWrite 00f9,00,0,7
SPIWrite 00f8,bf,0,7
SPIWrite 00ff,00,0,7
SPIWrite 00fe,00,0,7
SPIWrite 00fd,00,0,7
SPIWrite 00fc,00,0,7
SPIWrite 0113,00,0,7  //alarms_to_pap_clear=0xbf;
      Address(0x110[7:0],0x111[7:0],0x112[7:0],0x113[7:0],0x114[7:
0],0x114[7:0],0x115[7:0],0x116[7:0],0x117[7:0],0x118[7:0])
SPIWrite 0112,00,0,7
SPIWrite 0111,00,0,7
SPIWrite 0110,bf,0,7
SPIWrite 0117,00,0,7
SPIWrite 0116,00,0,7
SPIWrite 0115,00,0,7
SPIWrite 0114,00,0,7
SPIWrite 010b,00,0,7  //alarms_to_pap_mask=0xbf;
      Address(0x108[7:0],0x109[7:0],0x10a[7:0],0x10b[7:0],0x10c[7:
0],0x10c[7:0],0x10d[7:0],0x10e[7:0],0x10f[7:0],0x110[7:0])
SPIWrite 010a,00,0,7
SPIWrite 0109,00,0,7
SPIWrite 0108,bf,0,7
SPIWrite 010f,00,0,7
SPIWrite 010e,00,0,7
SPIWrite 010d,00,0,7
SPIWrite 010c,00,0,7
SPIWrite 0024,5c,0,7  //alarm_zeros_jesd_data_ena=0x0;
```

```
     Address(0x24[7:1])
SPIWrite 003c,82,0,7  //serdes_fifo_offset_lane0=0x2;
     Address(0x3c[7:0])
SPIWrite 003c,22,0,7  //serdes_fifo_offset_lane1=0x2;
     Address(0x3c[7:4])
SPIWrite 003d,82,0,7  //serdes_fifo_offset_lane2=0x2;
     Address(0x3d[7:0])
SPIWrite 003d,22,0,7  //serdes_fifo_offset_lane3=0x2;
     Address(0x3d[7:4])
SPIWrite 0026,02,0,7  //jesd_std_sel=0x2;   Address(0x26[7:0])
SPIWrite 0047,01,0,7  //link0_scr=0x0;      Address(0x47[7:7])
SPIWrite 0055,01,0,7  //link1_scr=0x0;      Address(0x55[7:7])
SPIWrite 0064,f1,0,7  //lane_ena=0x1; Address(0x64[7:0])
SPIWrite 0081,f1,0,7  //rbd_buf_overflow_err_cnt_thresh=0xf;
     Address(0x81[7:4])
SPIWrite 0083,1f,0,7  //dec_8b10b_code_err_cnt_thresh=0xf;
     Address(0x83[7:0])
SPIWrite 0083,ff,0,7  //dec_8b10b_disp_err_cnt_thresh=0xf;
     Address(0x83[7:4])
SPIWrite 0081,ff,0,7  //link_config_err_cnt_thresh=0xf;
     Address(0x81[7:0])
SPIWrite 0080,1f,0,7  //multiframe_align_err_cnt_thresh=0xf;
     Address(0x80[7:0])
SPIWrite 0080,ff,0,7  //frame_align_err_cnt_thresh=0xf;
     Address(0x80[7:4])
SPIWrite 00a8,02,0,7  //Property_88h_1_1=0x1;
     Address(0xa8[7:1])
SPIWrite 0024,58,0,7  //zero_invalid_data=0x0;
     Address(0x24[7:2])
SPIWrite 0024,50,0,7  //fifo_error_zeros_data_ena=0x0;
     Address(0x24[7:3])

//END: Done Configuring DAC JESD RX


//START: Configuring DAC JESD RX

SPIWrite 0016,08,0,7  //dac_jesd=0x2; Address(0x16[7:2])
SPIWrite 006c,00,0,7  //link0_k_m1=0x0;
     Address(0x6c[7:0],0x6d[7:0])
SPIWrite 006d,00,0,7  //link1_k_m1=0x0;
     Address(0x6d[7:0],0x6e[7:0])
SPIWrite 0057,00,0,7  //link1_ila_k_m1=0x0;
     Address(0x57[7:0],0x58[7:0])
SPIWrite 0049,00,0,7  //link0_ila_k_m1=0x0;
     Address(0x49[7:0],0x4a[7:0])
SPIWrite 0069,00,0,7  //link0_rbd_m1=0x3;
     Address(0x68[7:0],0x69[7:0],0x6a[7:0])
SPIWrite 0068,03,0,7
SPIWrite 006b,00,0,7  //link1_rbd_m1=0x3;
     Address(0x6a[7:0],0x6b[7:0],0x6c[7:0])
SPIWrite 006a,03,0,7
```

```
SPIWrite 0024,5e,0,7  //gearbox_init_state_ovr=0x1;
     Address(0x24[7:6])
SPIWrite 0025,ff,0,7  //gearbox_init_state_lane0_val=0x1;
     Address(0x25[7:0])
SPIWrite 0025,ff,0,7  //gearbox_init_state_lane1_val=0x1;
     Address(0x25[7:1])
SPIWrite 0025,ff,0,7  //gearbox_init_state_lane2_val=0x1;
     Address(0x25[7:2])
SPIWrite 0025,ff,0,7  //gearbox_init_state_lane3_val=0x1;
     Address(0x25[7:3])
SPIWrite 0025,fe,0,7  //gearbox_init_state_lane0_val=0x0;
     Address(0x25[7:0])
SPIWrite 0025,fc,0,7  //gearbox_init_state_lane1_val=0x0;
     Address(0x25[7:1])
SPIWrite 0025,f8,0,7  //gearbox_init_state_lane2_val=0x0;
     Address(0x25[7:2])
SPIWrite 0025,f0,0,7  //gearbox_init_state_lane3_val=0x0;
     Address(0x25[7:3])
SPIWrite 0020,03,0,7  //link0_init_state=0x1;
     Address(0x20[7:0])
SPIWrite 0020,03,0,7  //link1_init_state=0x1;
     Address(0x20[7:1])
SPIWrite 0064,ff,0,7  //jesd_clear_data=0xf;
     Address(0x64[7:4])
SPIWrite 0040,04,0,7  //link0_comma_align_lock_reset_disable=0x1;
     Address(0x40[7:2])
SPIWrite 0040,0c,0,7  //link1_comma_align_lock_reset_disable=0x1;
     Address(0x40[7:3])
SPIWrite 00ac,04,0,7  //link0_emb_align_lock_reset_disable=0x1;
     Address(0xac[7:2])
SPIWrite 00ac,0c,0,7  //link1_emb_align_lock_reset_disable=0x1;
     Address(0xac[7:3])
SPIWrite 002c,01,0,7  //root_clk_tx1_div_m=0x1;
     Address(0x2c[7:0])
SPIWrite 002d,00,0,7  //root_clk_tx1_div_n_m1=0x0;
     Address(0x2d[7:0])
SPIWrite 002e,01,0,7  //root_clk_tx2_div_m=0x1;
     Address(0x2e[7:0])
SPIWrite 002f,00,0,7  //root_clk_tx2_div_n_m1=0x0;
     Address(0x2f[7:0])
SPIWrite 0030,01,0,7  //duc_clk_tx1_div_m=0x1;
     Address(0x30[7:0])
SPIWrite 0031,02,0,7  //duc_clk_tx1_div_n_m1=0x2;
     Address(0x31[7:0])
SPIWrite 0032,01,0,7  //duc_clk_tx2_div_m=0x1;
     Address(0x32[7:0])
SPIWrite 0033,02,0,7  //duc_clk_tx2_div_n_m1=0x2;
     Address(0x33[7:0])
SPIWrite 0034,02,0,7  //jesd_clk_tx1_div_m=0x2;
     Address(0x34[7:0])
SPIWrite 0035,02,0,7  //jesd_clk_tx1_div_n_m1=0x2;
     Address(0x35[7:0])
```

```
SPIWrite 0036,02,0,7  //jesd_clk_tx2_div_m=0x2;
     Address(0x36[7:0])
SPIWrite 0037,02,0,7  //jesd_clk_tx2_div_n_m1=0x2;
     Address(0x37[7:0])
SPIWrite 0022,41,0,7  //link0_jesd_mode=0x1;
     Address(0x22[7:0])
SPIWrite 0023,41,0,7  //link1_jesd_mode=0x1;
     Address(0x23[7:0])
SPIWrite 0022,41,0,7  //link0_jesd_sample_mode=0x1;
     Address(0x22[7:6])
SPIWrite 0023,41,0,7  //link1_jesd_sample_mode=0x1;
     Address(0x23[7:6])
SPIWrite 0038,1f,0,7  //tx_root_clk_div_dither_en=0x1;
     Address(0x38[7:0])
SPIWrite 0038,1d,0,7  //duc_clk_io_div_dither_en=0x0;
     Address(0x38[7:1])
SPIWrite 0038,19,0,7  //duc_clk_div_dither_en=0x0;
     Address(0x38[7:2])
SPIWrite 0038,11,0,7  //jesd_clk_div_dither_en=0x0;
     Address(0x38[7:3])
SPIWrite 0038,01,0,7  //jesd_clk_div2_div_dither_en=0x0;
     Address(0x38[7:4])
SPIWrite 0026,00,0,7  //num_links=0x0;      Address(0x26[7:2])
SPIWrite 0042,7f,0,7  //comma_align_valid_thresh=0x7f;
     Address(0x42[7:0])
SPIWrite 00ad,86,0,7  //emb_align_valid_thresh=0x6;
     Address(0xad[7:0])
SPIWrite 0078,00,0,7  //link0_sync_request_ena=0x0;
     Address(0x78[7:0],0x79[7:0])
SPIWrite 0079,00,0,7  //link1_sync_request_ena=0x0;
     Address(0x79[7:0],0x7a[7:0])
SPIWrite 007a,00,0,7  //link0_error_ena=0x0;
     Address(0x7a[7:0],0x7b[7:0])
SPIWrite 007b,00,0,7  //link1_error_ena=0x0;
     Address(0x7b[7:0],0x7c[7:0])
SPIWrite 0103,00,0,7  //alarms_clear=0xbf;
     Address(0x100[7:0],0x101[7:0],0x102[7:0],0x103[7:0],0x104[7:
0],0x104[7:0],0x105[7:0],0x106[7:0],0x107[7:0],0x108[7:0])
SPIWrite 0102,00,0,7
SPIWrite 0101,00,0,7
SPIWrite 0100,bf,0,7
SPIWrite 0107,00,0,7
SPIWrite 0106,00,0,7
SPIWrite 0105,00,0,7
SPIWrite 0104,00,0,7
SPIWrite 00fb,00,0,7  //alarms_mask=0xbf;
     Address(0xf8[7:0],0xf9[7:0],0xfa[7:0],0xfb[7:0],0xfc[7:0],0x
fc[7:0],0xfd[7:0],0xfe[7:0],0xff[7:0],0x100[7:0])
SPIWrite 00fa,00,0,7
SPIWrite 00f9,00,0,7
SPIWrite 00f8,bf,0,7
SPIWrite 00ff,00,0,7
```

```
SPIWrite 00fe,00,0,7
SPIWrite 00fd,00,0,7
SPIWrite 00fc,00,0,7
SPIWrite 0113,00,0,7  //alarms_to_pap_clear=0xbf;
     Address(0x110[7:0],0x111[7:0],0x112[7:0],0x113[7:0],0x114[7:
0],0x114[7:0],0x115[7:0],0x116[7:0],0x117[7:0],0x118[7:0])
SPIWrite 0112,00,0,7
SPIWrite 0111,00,0,7
SPIWrite 0110,bf,0,7
SPIWrite 0117,00,0,7
SPIWrite 0116,00,0,7
SPIWrite 0115,00,0,7
SPIWrite 0114,00,0,7
SPIWrite 010b,00,0,7  //alarms_to_pap_mask=0xbf;
     Address(0x108[7:0],0x109[7:0],0x10a[7:0],0x10b[7:0],0x10c[7:
0],0x10c[7:0],0x10d[7:0],0x10e[7:0],0x10f[7:0],0x110[7:0])
SPIWrite 010a,00,0,7
SPIWrite 0109,00,0,7
SPIWrite 0108,bf,0,7
SPIWrite 010f,00,0,7
SPIWrite 010e,00,0,7
SPIWrite 010d,00,0,7
SPIWrite 010c,00,0,7
SPIWrite 0024,5c,0,7  //alarm_zeros_jesd_data_ena=0x0;
     Address(0x24[7:1])
SPIWrite 003c,82,0,7  //serdes_fifo_offset_lane0=0x2;
     Address(0x3c[7:0])
SPIWrite 003c,22,0,7  //serdes_fifo_offset_lane1=0x2;
     Address(0x3c[7:4])
SPIWrite 003d,82,0,7  //serdes_fifo_offset_lane2=0x2;
     Address(0x3d[7:0])
SPIWrite 003d,22,0,7  //serdes_fifo_offset_lane3=0x2;
     Address(0x3d[7:4])
SPIWrite 0026,02,0,7  //jesd_std_sel=0x2;   Address(0x26[7:0])
SPIWrite 0047,01,0,7  //link0_scr=0x0;      Address(0x47[7:7])
SPIWrite 0055,01,0,7  //link1_scr=0x0;      Address(0x55[7:7])
SPIWrite 0064,f1,0,7  //lane_ena=0x1; Address(0x64[7:0])
SPIWrite 0081,f1,0,7  //rbd_buf_overflow_err_cnt_thresh=0xf;
     Address(0x81[7:4])
SPIWrite 0083,1f,0,7  //dec_8b10b_code_err_cnt_thresh=0xf;
     Address(0x83[7:0])
SPIWrite 0083,ff,0,7  //dec_8b10b_disp_err_cnt_thresh=0xf;
     Address(0x83[7:4])
SPIWrite 0081,ff,0,7  //link_config_err_cnt_thresh=0xf;
     Address(0x81[7:0])
SPIWrite 0080,1f,0,7  //multiframe_align_err_cnt_thresh=0xf;
     Address(0x80[7:0])
SPIWrite 0080,ff,0,7  //frame_align_err_cnt_thresh=0xf;
     Address(0x80[7:4])
SPIWrite 00a8,02,0,7  //Property_88h_1_1=0x1;
     Address(0xa8[7:1])
SPIWrite 0024,58,0,7  //zero_invalid_data=0x0;
```

```
     Address(0x24[7:2])
SPIWrite 0024,50,0,7  //fifo_error_zeros_data_ena=0x0;
     Address(0x24[7:3])

//END: Done Configuring DAC JESD RX

SPIWrite 0016,00,0,7  //dac_jesd=0x0; Address(0x16[7:2])

//STEP: jesdConfig/step3
SPIWrite 0016,01,0,7  //adc_jesd=0x1; Address(0x16[7:0])
SPIWrite 0120,02,0,7  //ctrl_rx1_msf_sig_invalid=0x2;
     Address(0x120[7:0])
SPIWrite 0120,0a,0,7  //ctrl_rx2_msf_sig_invalid=0x2;
     Address(0x120[7:2])
SPIWrite 0120,2a,0,7  //ctrl_rx3_rx4_msf_sig_invalid=0x2;
     Address(0x120[7:4])
SPIWrite 0121,02,0,7  //ctrl_fb1_msf_sig_invalid=0x2;
     Address(0x121[7:0])
SPIWrite 0121,0a,0,7  //ctrl_fb2_msf_sig_invalid=0x2;
     Address(0x121[7:2])
SPIWrite 0016,00,0,7  //adc_jesd=0x0; Address(0x16[7:0])
SPIWrite 0016,10,0,7  //jesd_subchip=0x1;   Address(0x16[7:4])
SPIWrite 0029,02,0,7  //dual_2t2r1f_mode_ab=0x0;
     Address(0x29[7:0])
SPIWrite 0029,00,0,7  //dual_2t2r1f_mode_cd=0x0;
     Address(0x29[7:1])
SPIWrite 0016,00,0,7  //jesd_subchip=0x0;   Address(0x16[7:4])
SPIWrite 0016,02,0,7  //adc_jesd=0x2; Address(0x16[7:0])
SPIWrite 0120,02,0,7  //ctrl_rx1_msf_sig_invalid=0x2;
     Address(0x120[7:0])
SPIWrite 0120,0a,0,7  //ctrl_rx2_msf_sig_invalid=0x2;
     Address(0x120[7:2])
SPIWrite 0120,2a,0,7  //ctrl_rx3_rx4_msf_sig_invalid=0x2;
     Address(0x120[7:4])
SPIWrite 0121,02,0,7  //ctrl_fb1_msf_sig_invalid=0x2;
     Address(0x121[7:0])
SPIWrite 0121,0a,0,7  //ctrl_fb2_msf_sig_invalid=0x2;
     Address(0x121[7:2])
SPIWrite 0016,00,0,7  //adc_jesd=0x0; Address(0x16[7:0])
SPIWrite 0016,10,0,7  //jesd_subchip=0x1;   Address(0x16[7:4])
SPIWrite 0029,00,0,7  //dual_2t2r1f_mode_ab=0x0;
     Address(0x29[7:0])
SPIWrite 0029,00,0,7  //dual_2t2r1f_mode_cd=0x0;
     Address(0x29[7:1])
SPIWrite 0016,00,0,7  //jesd_subchip=0x0;   Address(0x16[7:4])

//STEP: agcConfig/step0
SPIWrite 0013,40,0,7  //dsa_page1=0x1;      Address(0x13[7:6])
SPIWrite 00d0,02,0,7  //gain_ctrl=0x2;      Address(0xd0[7:0])
SPIWrite 0013,80,0,7  //dsa_page1=0x2;      Address(0x13[7:6])
SPIWrite 00d0,02,0,7  //gain_ctrl=0x2;      Address(0xd0[7:0])
SPIWrite 0013,00,0,7  //dsa_page1=0x0;      Address(0x13[7:6])
```

```
SPIWrite 0012,01,0,7  //rxdig=0x1;     Address(0x12[7:0])
SPIWrite 0773,00,0,7  //Property_750h_24_24=0x0;
     Address(0x773[7:0])
SPIWrite 0012,00,0,7  //rxdig=0x0;     Address(0x12[7:0])
SPIWrite 0018,20,0,7  //macro=0x1;     Address(0x18[7:5])
SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,06,0,7  //MACRO_OPERAND_REG0=0x6020601;
     Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,02,0,7
SPIWrite 00a1,06,0,7
SPIWrite 00a0,01,0,7
SPIWrite 00a7,00,0,7  //MACRO_OPERAND_REG1=0x2;
     Address(0xa4[7:0],0xa5[7:0],0xa6[7:0],0xa7[7:0],0xa8[7:0])
SPIWrite 00a6,00,0,7
SPIWrite 00a5,00,0,7
SPIWrite 00a4,02,0,7
SPIWrite 0193,67,0,7  //MACRO_OPCODE=0x67;
     Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
     Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
     Address(0xf0[7:5])

SPIRead 00f0,6,6
```

```
//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,0c,0,7  //MACRO_OPERAND_REG0=0xc040a01;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,04,0,7
SPIWrite 00a1,0a,0,7
SPIWrite 00a0,01,0,7
SPIWrite 00a7,50,0,7  //MACRO_OPERAND_REG1=0x50381230;
      Address(0xa4[7:0],0xa5[7:0],0xa6[7:0],0xa7[7:0],0xa8[7:0])
SPIWrite 00a6,38,0,7
SPIWrite 00a5,12,0,7
SPIWrite 00a4,30,0,7
SPIWrite 0193,58,0,7  //MACRO_OPCODE=0x58;
      Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])
```

```
SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
      Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0; Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
      Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0x1101;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00,0,7
SPIWrite 00a1,11,0,7
SPIWrite 00a0,01,0,7
SPIWrite 00a7,22,0,7  //MACRO_OPERAND_REG1=0x22000011;
      Address(0xa4[7:0],0xa5[7:0],0xa6[7:0],0xa7[7:0],0xa8[7:0])
SPIWrite 00a6,00,0,7
```

```
SPIWrite 00a5,00,0,7
SPIWrite 00a4,11,0,7
SPIWrite 00ab,00,0,7  //MACRO_OPERAND_REG2=0x22;
      Address(0xa8[7:0],0xa9[7:0],0xaa[7:0],0xab[7:0],0xac[7:0])
SPIWrite 00aa,00,0,7
SPIWrite 00a9,00,0,7
SPIWrite 00a8,22,0,7
SPIWrite 0193,59,0,7  //MACRO_OPCODE=0x59;
      Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
      Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
      Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
```

```
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0x801;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00,0,7
SPIWrite 00a1,08,0,7
SPIWrite 00a0,01,0,7
SPIWrite 00a7,08,0,7  //MACRO_OPERAND_REG1=0x8000008;
      Address(0xa4[7:0],0xa5[7:0],0xa6[7:0],0xa7[7:0],0xa8[7:0])
SPIWrite 00a6,00,0,7
SPIWrite 00a5,00,0,7
SPIWrite 00a4,08,0,7
SPIWrite 00ab,00,0,7  //MACRO_OPERAND_REG2=0x80000;
      Address(0xa8[7:0],0xa9[7:0],0xaa[7:0],0xab[7:0],0xac[7:0])
SPIWrite 00aa,08,0,7
SPIWrite 00a9,00,0,7
SPIWrite 00a8,00,0,7
SPIWrite 00af,00,0,7  //MACRO_OPERAND_REG3=0x0;
      Address(0xac[7:0],0xad[7:0],0xae[7:0],0xaf[7:0],0xb0[7:0])
SPIWrite 00ae,00,0,7
SPIWrite 00ad,00,0,7
SPIWrite 00ac,00,0,7
SPIWrite 0193,5b,0,7  //MACRO_OPCODE=0x5b;
      Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
      Address(0xf1[7:0],0xf2[7:0])
```

```
SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0; Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
      Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0x1e0001;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,1e,0,7
SPIWrite 00a1,00,0,7
SPIWrite 00a0,01,0,7
SPIWrite 0193,5f,0,7  //MACRO_OPCODE=0x5f;
      Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1; Address(0xf0[7:2])
```

```
SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
      Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
      Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0x40301;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
```

```
SPIWrite 00a2,04,0,7
SPIWrite 00a1,03,0,7
SPIWrite 00a0,01,0,7
SPIWrite 00a7,00,0,7  //MACRO_OPERAND_REG1=0x10000;
     Address(0xa4[7:0],0xa5[7:0],0xa6[7:0],0xa7[7:0],0xa8[7:0])
SPIWrite 00a6,01,0,7
SPIWrite 00a5,00,0,7
SPIWrite 00a4,00,0,7
SPIWrite 0193,6b,0,7  //MACRO_OPCODE=0x6b;
     Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
     Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
     Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
     Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
```

```
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,03,0,7  //MACRO_OPERAND_REG0=0x3003201;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00,0,7
SPIWrite 00a1,32,0,7
SPIWrite 00a0,01,0,7
SPIWrite 0193,69,0,7  //MACRO_OPCODE=0x69;
      Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
      Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
      Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])
```

```
SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,02,0,7  //MACRO_OPERAND_REG0=0x2580101;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,58,0,7
SPIWrite 00a1,01,0,7
SPIWrite 00a0,01,0,7
SPIWrite 00a7,00,0,7  //MACRO_OPERAND_REG1=0x100;
      Address(0xa4[7:0],0xa5[7:0],0xa6[7:0],0xa7[7:0],0xa8[7:0])
SPIWrite 00a6,00,0,7
SPIWrite 00a5,01,0,7
SPIWrite 00a4,00,0,7
SPIWrite 0193,5e,0,7  //MACRO_OPCODE=0x5e;
      Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7
```

```
//Read     MACRO_ERROR_OPCODE=0x0;
      Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0; Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
      Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0xd0001;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,0d,0,7
SPIWrite 00a1,00,0,7
SPIWrite 00a0,01,0,7
SPIWrite 00a7,00,0,7  //MACRO_OPERAND_REG1=0x0;
      Address(0xa4[7:0],0xa5[7:0],0xa6[7:0],0xa7[7:0],0xa8[7:0])
SPIWrite 00a6,00,0,7
SPIWrite 00a5,00,0,7
SPIWrite 00a4,00,0,7
SPIWrite 0193,61,0,7  //MACRO_OPCODE=0x61;
```

```
      Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;       Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
      Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
      Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;       Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0
```

```
//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,01,0,7  //MACRO_OPERAND_REG0=0x1000001;
     Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00,0,7
SPIWrite 00a1,00,0,7
SPIWrite 00a0,01,0,7
SPIWrite 00a7,01,0,7  //MACRO_OPERAND_REG1=0x1800000;
     Address(0xa4[7:0],0xa5[7:0],0xa6[7:0],0xa7[7:0],0xa8[7:0])
SPIWrite 00a6,80,0,7
SPIWrite 00a5,00,0,7
SPIWrite 00a4,00,0,7
SPIWrite 00ab,00,0,7  //MACRO_OPERAND_REG2=0x0;
     Address(0xa8[7:0],0xa9[7:0],0xaa[7:0],0xab[7:0],0xac[7:0])
SPIWrite 00aa,00,0,7
SPIWrite 00a9,00,0,7
SPIWrite 00a8,00,0,7
SPIWrite 0193,66,0,7  //MACRO_OPCODE=0x66;
     Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
     Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
     Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])
```

```
SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0x1;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00,0,7
SPIWrite 00a1,00,0,7
SPIWrite 00a0,01,0,7
SPIWrite 0193,8e,0,7  //MACRO_OPCODE=0x8e;
      Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
      Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4
```

```
//Read     MACRO_ERROR_IN_OPCODE=0x0; Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
      Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0x1101;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00,0,7
SPIWrite 00a1,11,0,7
SPIWrite 00a0,01,0,7
SPIWrite 0193,8f,0,7  //MACRO_OPCODE=0x8f;
      Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1; Address(0xf0[7:2])


SPIPoll 00f0,2,2,4
```

```
SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
      Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
      Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0x1101;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00,0,7
SPIWrite 00a1,11,0,7
```

```
SPIWrite 00a0,01,0,7
SPIWrite 0193,68,0,7  //MACRO_OPCODE=0x68;
     Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
     Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
     Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
     Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
     Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
```

```
SPIWrite 0018,00,0,7  //macro=0x0;     Address(0x18[7:5])
SPIWrite 0012,01,0,7  //rxdig=0x1;     Address(0x12[7:0])
SPIWrite 0773,00,0,7  //Property_750h_24_24=0x0;
     Address(0x773[7:0])
SPIWrite 0012,00,0,7  //rxdig=0x0;     Address(0x12[7:0])
SPIWrite 0018,20,0,7  //macro=0x1;     Address(0x18[7:5])
SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,06,0,7  //MACRO_OPERAND_REG0=0x6020602;
     Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,02,0,7
SPIWrite 00a1,06,0,7
SPIWrite 00a0,02,0,7
SPIWrite 00a7,00,0,7  //MACRO_OPERAND_REG1=0x2;
     Address(0xa4[7:0],0xa5[7:0],0xa6[7:0],0xa7[7:0],0xa8[7:0])
SPIWrite 00a6,00,0,7
SPIWrite 00a5,00,0,7
SPIWrite 00a4,02,0,7
SPIWrite 0193,67,0,7  //MACRO_OPCODE=0x67;
     Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
     Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
     Address(0xf0[7:5])
```

```
SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,0c,0,7  //MACRO_OPERAND_REG0=0xc040a02;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,04,0,7
SPIWrite 00a1,0a,0,7
SPIWrite 00a0,02,0,7
SPIWrite 00a7,50,0,7  //MACRO_OPERAND_REG1=0x50381230;
      Address(0xa4[7:0],0xa5[7:0],0xa6[7:0],0xa7[7:0],0xa8[7:0])
SPIWrite 00a6,38,0,7
SPIWrite 00a5,12,0,7
SPIWrite 00a4,30,0,7
SPIWrite 0193,58,0,7  //MACRO_OPCODE=0x58;
      Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00
```

```
//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
      Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0; Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
      Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0x1102;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00,0,7
SPIWrite 00a1,11,0,7
SPIWrite 00a0,02,0,7
SPIWrite 00a7,22,0,7  //MACRO_OPERAND_REG1=0x22000011;
      Address(0xa4[7:0],0xa5[7:0],0xa6[7:0],0xa7[7:0],0xa8[7:0])
```

```
SPIWrite 00a6,00,0,7
SPIWrite 00a5,00,0,7
SPIWrite 00a4,11,0,7
SPIWrite 00ab,00,0,7  //MACRO_OPERAND_REG2=0x22;
     Address(0xa8[7:0],0xa9[7:0],0xaa[7:0],0xab[7:0],0xac[7:0])
SPIWrite 00aa,00,0,7
SPIWrite 00a9,00,0,7
SPIWrite 00a8,22,0,7
SPIWrite 0193,59,0,7  //MACRO_OPCODE=0x59;
     Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
     Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
     Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
     Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
```

```
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0x802;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00,0,7
SPIWrite 00a1,08,0,7
SPIWrite 00a0,02,0,7
SPIWrite 00a7,08,0,7  //MACRO_OPERAND_REG1=0x8000008;
      Address(0xa4[7:0],0xa5[7:0],0xa6[7:0],0xa7[7:0],0xa8[7:0])
SPIWrite 00a6,00,0,7
SPIWrite 00a5,00,0,7
SPIWrite 00a4,08,0,7
SPIWrite 00ab,00,0,7  //MACRO_OPERAND_REG2=0x80000;
      Address(0xa8[7:0],0xa9[7:0],0xaa[7:0],0xab[7:0],0xac[7:0])
SPIWrite 00aa,08,0,7
SPIWrite 00a9,00,0,7
SPIWrite 00a8,00,0,7
SPIWrite 00af,00,0,7  //MACRO_OPERAND_REG3=0x0;
      Address(0xac[7:0],0xad[7:0],0xae[7:0],0xaf[7:0],0xb0[7:0])
SPIWrite 00ae,00,0,7
SPIWrite 00ad,00,0,7
SPIWrite 00ac,00,0,7
SPIWrite 0193,5b,0,7  //MACRO_OPCODE=0x5b;
      Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
```

```
      Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0; Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
      Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0x1e0002;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,1e,0,7
SPIWrite 00a1,00,0,7
SPIWrite 00a0,02,0,7
SPIWrite 0193,5f,0,7  //MACRO_OPCODE=0x5f;
      Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])
```

```
SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
      Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
      Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0x40302;
```

```
     Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,04,0,7
SPIWrite 00a1,03,0,7
SPIWrite 00a0,02,0,7
SPIWrite 00a7,00,0,7  //MACRO_OPERAND_REG1=0x10000;
     Address(0xa4[7:0],0xa5[7:0],0xa6[7:0],0xa7[7:0],0xa8[7:0])
SPIWrite 00a6,01,0,7
SPIWrite 00a5,00,0,7
SPIWrite 00a4,00,0,7
SPIWrite 0193,6b,0,7  //MACRO_OPCODE=0x6b;
     Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1; Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
     Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0; Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
     Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
     Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
```

```
SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,03,0,7  //MACRO_OPERAND_REG0=0x3003202;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00,0,7
SPIWrite 00a1,32,0,7
SPIWrite 00a0,02,0,7
SPIWrite 0193,69,0,7  //MACRO_OPCODE=0x69;
      Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
      Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
      Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])
```

```
SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,02,0,7  //MACRO_OPERAND_REG0=0x2580102;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,58,0,7
SPIWrite 00a1,01,0,7
SPIWrite 00a0,02,0,7
SPIWrite 00a7,00,0,7  //MACRO_OPERAND_REG1=0x100;
      Address(0xa4[7:0],0xa5[7:0],0xa6[7:0],0xa7[7:0],0xa8[7:0])
SPIWrite 00a6,00,0,7
SPIWrite 00a5,01,0,7
SPIWrite 00a4,00,0,7
SPIWrite 0193,5e,0,7  //MACRO_OPCODE=0x5e;
      Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7
```

```
//Read     MACRO_ERROR_OPCODE=0x0;
      Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
      Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0xd0002;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,0d,0,7
SPIWrite 00a1,00,0,7
SPIWrite 00a0,02,0,7
SPIWrite 00a7,00,0,7  //MACRO_OPERAND_REG1=0x0;
      Address(0xa4[7:0],0xa5[7:0],0xa6[7:0],0xa7[7:0],0xa8[7:0])
SPIWrite 00a6,00,0,7
SPIWrite 00a5,00,0,7
SPIWrite 00a4,00,0,7
```

```
SPIWrite 0193,61,0,7  //MACRO_OPCODE=0x61;
     Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
     Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
     Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
     Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
     Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0
```

```
//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,01,0,7  //MACRO_OPERAND_REG0=0x1000002;
     Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00,0,7
SPIWrite 00a1,00,0,7
SPIWrite 00a0,02,0,7
SPIWrite 00a7,01,0,7  //MACRO_OPERAND_REG1=0x1800000;
     Address(0xa4[7:0],0xa5[7:0],0xa6[7:0],0xa7[7:0],0xa8[7:0])
SPIWrite 00a6,80,0,7
SPIWrite 00a5,00,0,7
SPIWrite 00a4,00,0,7
SPIWrite 00ab,00,0,7  //MACRO_OPERAND_REG2=0x0;
     Address(0xa8[7:0],0xa9[7:0],0xaa[7:0],0xab[7:0],0xac[7:0])
SPIWrite 00aa,00,0,7
SPIWrite 00a9,00,0,7
SPIWrite 00a8,00,0,7
SPIWrite 0193,66,0,7  //MACRO_OPCODE=0x66;
     Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
     Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
     Address(0xf0[7:5])

SPIRead 00f0,6,6
```

```
//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0x1;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00,0,7
SPIWrite 00a1,00,0,7
SPIWrite 00a0,01,0,7
SPIWrite 0193,8e,0,7  //MACRO_OPCODE=0x8e;
      Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
      Address(0xf1[7:0],0xf2[7:0])
```

```
SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0; Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
      Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0x1102;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00,0,7
SPIWrite 00a1,11,0,7
SPIWrite 00a0,02,0,7
SPIWrite 0193,8f,0,7  //MACRO_OPCODE=0x8f;
      Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1; Address(0xf0[7:2])
```

```
SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
      Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
      Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0x1102;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00,0,7
```

```
SPIWrite 00a1,11,0,7
SPIWrite 00a0,02,0,7
SPIWrite 0193,68,0,7  //MACRO_OPCODE=0x68;
     Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
     Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
     Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
     Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
     Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
```

```
SPIWrite 0018,00,0,7  //macro=0x0;     Address(0x18[7:5])
SPIWrite 0012,08,0,7  //rxdig=0x8;     Address(0x12[7:0])
SPIWrite 0773,00,0,7  //Property_750h_24_24=0x0;
     Address(0x773[7:0])
SPIWrite 0012,00,0,7  //rxdig=0x0;     Address(0x12[7:0])
SPIWrite 0018,20,0,7  //macro=0x1;     Address(0x18[7:5])
SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,06,0,7  //MACRO_OPERAND_REG0=0x6020604;
     Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,02,0,7
SPIWrite 00a1,06,0,7
SPIWrite 00a0,04,0,7
SPIWrite 00a7,00,0,7  //MACRO_OPERAND_REG1=0x2;
     Address(0xa4[7:0],0xa5[7:0],0xa6[7:0],0xa7[7:0],0xa8[7:0])
SPIWrite 00a6,00,0,7
SPIWrite 00a5,00,0,7
SPIWrite 00a4,02,0,7
SPIWrite 0193,67,0,7  //MACRO_OPCODE=0x67;
     Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
     Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
     Address(0xf0[7:5])
```

```
SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,0c,0,7  //MACRO_OPERAND_REG0=0xc040a04;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,04,0,7
SPIWrite 00a1,0a,0,7
SPIWrite 00a0,04,0,7
SPIWrite 00a7,50,0,7  //MACRO_OPERAND_REG1=0x50381230;
      Address(0xa4[7:0],0xa5[7:0],0xa6[7:0],0xa7[7:0],0xa8[7:0])
SPIWrite 00a6,38,0,7
SPIWrite 00a5,12,0,7
SPIWrite 00a4,30,0,7
SPIWrite 0193,58,0,7  //MACRO_OPCODE=0x58;
      Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00
```

```
//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
      Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
      Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0x1104;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00,0,7
SPIWrite 00a1,11,0,7
SPIWrite 00a0,04,0,7
SPIWrite 00a7,22,0,7  //MACRO_OPERAND_REG1=0x22000011;
```

```
     Address(0xa4[7:0],0xa5[7:0],0xa6[7:0],0xa7[7:0],0xa8[7:0])
SPIWrite 00a6,00,0,7
SPIWrite 00a5,00,0,7
SPIWrite 00a4,11,0,7
SPIWrite 00ab,00,0,7  //MACRO_OPERAND_REG2=0x22;
     Address(0xa8[7:0],0xa9[7:0],0xaa[7:0],0xab[7:0],0xac[7:0])
SPIWrite 00aa,00,0,7
SPIWrite 00a9,00,0,7
SPIWrite 00a8,22,0,7
SPIWrite 0193,59,0,7  //MACRO_OPCODE=0x59;
     Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1; Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
     Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0; Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
     Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
     Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
```

```
SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0x804;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00,0,7
SPIWrite 00a1,08,0,7
SPIWrite 00a0,04,0,7
SPIWrite 00a7,08,0,7  //MACRO_OPERAND_REG1=0x8000008;
      Address(0xa4[7:0],0xa5[7:0],0xa6[7:0],0xa7[7:0],0xa8[7:0])
SPIWrite 00a6,00,0,7
SPIWrite 00a5,00,0,7
SPIWrite 00a4,08,0,7
SPIWrite 00ab,00,0,7  //MACRO_OPERAND_REG2=0x80000;
      Address(0xa8[7:0],0xa9[7:0],0xaa[7:0],0xab[7:0],0xac[7:0])
SPIWrite 00aa,08,0,7
SPIWrite 00a9,00,0,7
SPIWrite 00a8,00,0,7
SPIWrite 00af,00,0,7  //MACRO_OPERAND_REG3=0x0;
      Address(0xac[7:0],0xad[7:0],0xae[7:0],0xaf[7:0],0xb0[7:0])
SPIWrite 00ae,00,0,7
SPIWrite 00ad,00,0,7
SPIWrite 00ac,00,0,7
SPIWrite 0193,5b,0,7  //MACRO_OPCODE=0x5b;
      Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7
```

```
//Read     MACRO_ERROR_OPCODE=0x0;
      Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0; Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
      Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0x1e0004;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,1e,0,7
SPIWrite 00a1,00,0,7
SPIWrite 00a0,04,0,7
SPIWrite 0193,5f,0,7  //MACRO_OPCODE=0x5f;
      Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2
```

```
//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
      Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
      Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1
```

```
SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0x40304;
     Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,04,0,7
SPIWrite 00a1,03,0,7
SPIWrite 00a0,04,0,7
SPIWrite 00a7,00,0,7  //MACRO_OPERAND_REG1=0x10000;
     Address(0xa4[7:0],0xa5[7:0],0xa6[7:0],0xa7[7:0],0xa8[7:0])
SPIWrite 00a6,01,0,7
SPIWrite 00a5,00,0,7
SPIWrite 00a4,00,0,7
SPIWrite 0193,6b,0,7  //MACRO_OPCODE=0x6b;
     Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1; Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
     Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0; Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
     Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
     Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
```

```
SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,03,0,7  //MACRO_OPERAND_REG0=0x3003204;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00,0,7
SPIWrite 00a1,32,0,7
SPIWrite 00a0,04,0,7
SPIWrite 0193,69,0,7  //MACRO_OPCODE=0x69;
      Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
      Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
      Address(0xf0[7:5])

SPIRead 00f0,6,6
```

```
//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,02,0,7  //MACRO_OPERAND_REG0=0x2580104;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,58,0,7
SPIWrite 00a1,01,0,7
SPIWrite 00a0,04,0,7
SPIWrite 00a7,00,0,7  //MACRO_OPERAND_REG1=0x100;
      Address(0xa4[7:0],0xa5[7:0],0xa6[7:0],0xa7[7:0],0xa8[7:0])
SPIWrite 00a6,00,0,7
SPIWrite 00a5,01,0,7
SPIWrite 00a4,00,0,7
SPIWrite 0193,5e,0,7  //MACRO_OPCODE=0x5e;
      Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])
```

```
SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
      Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
      Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0xd0004;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,0d,0,7
SPIWrite 00a1,00,0,7
SPIWrite 00a0,04,0,7
SPIWrite 00a7,00,0,7  //MACRO_OPERAND_REG1=0x0;
      Address(0xa4[7:0],0xa5[7:0],0xa6[7:0],0xa7[7:0],0xa8[7:0])
SPIWrite 00a6,00,0,7
SPIWrite 00a5,00,0,7
```

```
SPIWrite 00a4,00,0,7
SPIWrite 0193,61,0,7  //MACRO_OPCODE=0x61;
      Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
      Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
      Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
```

```
SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,01,0,7  //MACRO_OPERAND_REG0=0x1000004;
     Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00,0,7
SPIWrite 00a1,00,0,7
SPIWrite 00a0,04,0,7
SPIWrite 00a7,01,0,7  //MACRO_OPERAND_REG1=0x1800000;
     Address(0xa4[7:0],0xa5[7:0],0xa6[7:0],0xa7[7:0],0xa8[7:0])
SPIWrite 00a6,80,0,7
SPIWrite 00a5,00,0,7
SPIWrite 00a4,00,0,7
SPIWrite 00ab,00,0,7  //MACRO_OPERAND_REG2=0x0;
     Address(0xa8[7:0],0xa9[7:0],0xaa[7:0],0xab[7:0],0xac[7:0])
SPIWrite 00aa,00,0,7
SPIWrite 00a9,00,0,7
SPIWrite 00a8,00,0,7
SPIWrite 0193,66,0,7  //MACRO_OPCODE=0x66;
     Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
     Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
     Address(0xf0[7:5])

SPIRead 00f0,6,6
```

```
//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0x1;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00,0,7
SPIWrite 00a1,00,0,7
SPIWrite 00a0,01,0,7
SPIWrite 0193,8e,0,7  //MACRO_OPCODE=0x8e;
      Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
      Address(0xf1[7:0],0xf2[7:0])
```

```
SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0; Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
      Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0x1104;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00,0,7
SPIWrite 00a1,11,0,7
SPIWrite 00a0,04,0,7
SPIWrite 0193,8f,0,7  //MACRO_OPCODE=0x8f;
      Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1; Address(0xf0[7:2])
```

```
SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
      Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
      Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0x1104;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
```

```
SPIWrite 00a2,00,0,7
SPIWrite 00a1,11,0,7
SPIWrite 00a0,04,0,7
SPIWrite 0193,68,0,7  //MACRO_OPCODE=0x68;
     Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
     Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
     Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
     Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
```

```
     Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIWrite 0018,00,0,7  //macro=0x0;     Address(0x18[7:5])
SPIWrite 0012,08,0,7  //rxdig=0x8;     Address(0x12[7:0])
SPIWrite 0773,00,0,7  //Property_750h_24_24=0x0;
     Address(0x773[7:0])
SPIWrite 0012,00,0,7  //rxdig=0x0;     Address(0x12[7:0])
SPIWrite 0018,20,0,7  //macro=0x1;     Address(0x18[7:5])
SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,06,0,7  //MACRO_OPERAND_REG0=0x6020608;
     Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,02,0,7
SPIWrite 00a1,06,0,7
SPIWrite 00a0,08,0,7
SPIWrite 00a7,00,0,7  //MACRO_OPERAND_REG1=0x2;
     Address(0xa4[7:0],0xa5[7:0],0xa6[7:0],0xa7[7:0],0xa8[7:0])
SPIWrite 00a6,00,0,7
SPIWrite 00a5,00,0,7
SPIWrite 00a4,02,0,7
SPIWrite 0193,67,0,7  //MACRO_OPCODE=0x67;
     Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
     Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
```

```
      Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,0c,0,7  //MACRO_OPERAND_REG0=0xc040a08;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,04,0,7
SPIWrite 00a1,0a,0,7
SPIWrite 00a0,08,0,7
SPIWrite 00a7,50,0,7  //MACRO_OPERAND_REG1=0x50381230;
      Address(0xa4[7:0],0xa5[7:0],0xa6[7:0],0xa7[7:0],0xa8[7:0])
SPIWrite 00a6,38,0,7
SPIWrite 00a5,12,0,7
SPIWrite 00a4,30,0,7
SPIWrite 0193,58,0,7  //MACRO_OPCODE=0x58;
      Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4
```

```
SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
      Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0; Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
      Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0x1108;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00,0,7
SPIWrite 00a1,11,0,7
SPIWrite 00a0,08,0,7
```

```
SPIWrite 00a7,22,0,7  //MACRO_OPERAND_REG1=0x22000011;
     Address(0xa4[7:0],0xa5[7:0],0xa6[7:0],0xa7[7:0],0xa8[7:0])
SPIWrite 00a6,00,0,7
SPIWrite 00a5,00,0,7
SPIWrite 00a4,11,0,7
SPIWrite 00ab,00,0,7  //MACRO_OPERAND_REG2=0x22;
     Address(0xa8[7:0],0xa9[7:0],0xaa[7:0],0xab[7:0],0xac[7:0])
SPIWrite 00aa,00,0,7
SPIWrite 00a9,00,0,7
SPIWrite 00a8,22,0,7
SPIWrite 0193,59,0,7  //MACRO_OPCODE=0x59;
     Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1; Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
     Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0; Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
     Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
     Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])
```

```
SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0x808;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00,0,7
SPIWrite 00a1,08,0,7
SPIWrite 00a0,08,0,7
SPIWrite 00a7,08,0,7  //MACRO_OPERAND_REG1=0x8000008;
      Address(0xa4[7:0],0xa5[7:0],0xa6[7:0],0xa7[7:0],0xa8[7:0])
SPIWrite 00a6,00,0,7
SPIWrite 00a5,00,0,7
SPIWrite 00a4,08,0,7
SPIWrite 00ab,00,0,7  //MACRO_OPERAND_REG2=0x80000;
      Address(0xa8[7:0],0xa9[7:0],0xaa[7:0],0xab[7:0],0xac[7:0])
SPIWrite 00aa,08,0,7
SPIWrite 00a9,00,0,7
SPIWrite 00a8,00,0,7
SPIWrite 00af,00,0,7  //MACRO_OPERAND_REG3=0x0;
      Address(0xac[7:0],0xad[7:0],0xae[7:0],0xaf[7:0],0xb0[7:0])
SPIWrite 00ae,00,0,7
SPIWrite 00ad,00,0,7
SPIWrite 00ac,00,0,7
SPIWrite 0193,5b,0,7  //MACRO_OPCODE=0x5b;
      Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7
```

```
//Read     MACRO_ERROR_OPCODE=0x0;
      Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
      Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0x1e0008;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,1e,0,7
SPIWrite 00a1,00,0,7
SPIWrite 00a0,08,0,7
SPIWrite 0193,5f,0,7  //MACRO_OPCODE=0x5f;
      Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2
```

```
//Read     MACRO_DONE=0x1; Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
      Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0; Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
      Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1
```

```
SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0x40308;
     Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,04,0,7
SPIWrite 00a1,03,0,7
SPIWrite 00a0,08,0,7
SPIWrite 00a7,00,0,7  //MACRO_OPERAND_REG1=0x10000;
     Address(0xa4[7:0],0xa5[7:0],0xa6[7:0],0xa7[7:0],0xa8[7:0])
SPIWrite 00a6,01,0,7
SPIWrite 00a5,00,0,7
SPIWrite 00a4,00,0,7
SPIWrite 0193,6b,0,7  //MACRO_OPCODE=0x6b;
     Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1; Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
     Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0; Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
     Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
```

```
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,03,0,7  //MACRO_OPERAND_REG0=0x3003208;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00,0,7
SPIWrite 00a1,32,0,7
SPIWrite 00a0,08,0,7
SPIWrite 0193,69,0,7  //MACRO_OPCODE=0x69;
      Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
      Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
      Address(0xf0[7:5])

SPIRead 00f0,6,6
```

```
//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,02,0,7  //MACRO_OPERAND_REG0=0x2580108;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,58,0,7
SPIWrite 00a1,01,0,7
SPIWrite 00a0,08,0,7
SPIWrite 00a7,00,0,7  //MACRO_OPERAND_REG1=0x100;
      Address(0xa4[7:0],0xa5[7:0],0xa6[7:0],0xa7[7:0],0xa8[7:0])
SPIWrite 00a6,00,0,7
SPIWrite 00a5,01,0,7
SPIWrite 00a4,00,0,7
SPIWrite 0193,5e,0,7  //MACRO_OPCODE=0x5e;
      Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])
```

```
SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
      Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0; Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
      Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0xd0008;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,0d,0,7
SPIWrite 00a1,00,0,7
SPIWrite 00a0,08,0,7
SPIWrite 00a7,00,0,7  //MACRO_OPERAND_REG1=0x0;
      Address(0xa4[7:0],0xa5[7:0],0xa6[7:0],0xa7[7:0],0xa8[7:0])
SPIWrite 00a6,00,0,7
```

```
SPIWrite 00a5,00,0,7
SPIWrite 00a4,00,0,7
SPIWrite 0193,61,0,7  //MACRO_OPCODE=0x61;
     Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
     Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
     Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
     Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
     Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
```

```
SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,01,0,7  //MACRO_OPERAND_REG0=0x1000008;
     Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00,0,7
SPIWrite 00a1,00,0,7
SPIWrite 00a0,08,0,7
SPIWrite 00a7,01,0,7  //MACRO_OPERAND_REG1=0x1800000;
     Address(0xa4[7:0],0xa5[7:0],0xa6[7:0],0xa7[7:0],0xa8[7:0])
SPIWrite 00a6,80,0,7
SPIWrite 00a5,00,0,7
SPIWrite 00a4,00,0,7
SPIWrite 00ab,00,0,7  //MACRO_OPERAND_REG2=0x0;
     Address(0xa8[7:0],0xa9[7:0],0xaa[7:0],0xab[7:0],0xac[7:0])
SPIWrite 00aa,00,0,7
SPIWrite 00a9,00,0,7
SPIWrite 00a8,00,0,7
SPIWrite 0193,66,0,7  //MACRO_OPCODE=0x66;
     Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
     Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
     Address(0xf0[7:5])
```

```
SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0x1;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00,0,7
SPIWrite 00a1,00,0,7
SPIWrite 00a0,01,0,7
SPIWrite 0193,8e,0,7  //MACRO_OPCODE=0x8e;
      Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
```

```
      Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0; Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
      Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0x1108;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00,0,7
SPIWrite 00a1,11,0,7
SPIWrite 00a0,08,0,7
SPIWrite 0193,8f,0,7  //MACRO_OPCODE=0x8f;
      Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1; Address(0xf0[7:2])
```

```
SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
      Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
      Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0x1108;
```

```
     Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00,0,7
SPIWrite 00a1,11,0,7
SPIWrite 00a0,08,0,7
SPIWrite 0193,68,0,7  //MACRO_OPCODE=0x68;
     Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1; Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
     Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0; Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
     Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
     Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7
```

```
//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIWrite 0018,00,0,7  //macro=0x0;     Address(0x18[7:5])

//STEP: miscConfig/step0
SPIWrite 0015,80,0,7  //timing_controller=0x1;
      Address(0x15[7:7])
SPIWrite 00b8,00,0,7  //broadcast_fbncosel=0x0;
      Address(0xb8[7:0])
SPIWrite 00bc,03,0,7  //enable_fbncosel_ab=0x3;
      Address(0xbc[7:0])
SPIWrite 00bd,03,0,7  //enable_fbncosel_cd=0x3;
      Address(0xbd[7:0])

//START: Setting RX NCO Sel Mode

SPIWrite 00ac,01,0,7  //broadcast_rxncosel=0x1;
      Address(0xac[7:0])
SPIWrite 00ad,01,0,7  //rxncosel_mode_ab=0x1;
      Address(0xad[7:0])
SPIWrite 00ae,01,0,7  //rxncosel_mode_cd=0x1;
      Address(0xae[7:0])
SPIWrite 00b0,03,0,7  //enable_rxncosel_a=0x3;
      Address(0xb0[7:0])
SPIWrite 00b1,03,0,7  //enable_rxncosel_b=0x3;
      Address(0xb1[7:0])
SPIWrite 00b2,03,0,7  //enable_rxncosel_c=0x3;
      Address(0xb2[7:0])
SPIWrite 00b3,03,0,7  //enable_rxncosel_d=0x3;
      Address(0xb3[7:0])

//END: Setting RX NCO Sel Mode


//START: Setting TX NCO Sel Mode

SPIWrite 0098,00,0,7  //broadcast_txncosel=0x0;
      Address(0x98[7:0])

//END: Setting TX NCO Sel Mode


//START: Configuring Interrupt Pins

SPIWrite 0015,00,0,7  //timing_controller=0x0;
      Address(0x15[7:7])
SPIWrite 0015,40,0,7  //digtop=0x1;    Address(0x15[7:6])
SPIWrite 0101,02,0,7  //alarm_mask_lsb_for_alarm0=0x21f;
      Address(0x100[7:0],0x101[7:0],0x102[7:0])
SPIWrite 0100,1f,0,7
SPIWrite 0103,00,0,7  //alarm_mask_msb_for_alarm0=0x0;
```

```
      Address(0x102[7:0],0x103[7:0],0x104[7:0])
SPIWrite 0102,00,0,7
SPIWrite 0105,00,0,7  //alarm_mask_lsb_for_alarm1=0x20;
      Address(0x104[7:0],0x105[7:0],0x106[7:0])
SPIWrite 0104,20,0,7
SPIWrite 0107,00,0,7  //alarm_mask_msb_for_alarm1=0x0;
      Address(0x106[7:0],0x107[7:0],0x108[7:0])
SPIWrite 0106,00,0,7

//END: Done configuring Interrupt Pins


//START: Power Saving Options

SPIWrite 0931,01,0,7  //Property_910h_8_8=0x1;
      Address(0x931[7:0])
SPIWrite 0015,00,0,7  //digtop=0x0;    Address(0x15[7:6])
SPIWrite 0011,3f,0,7  //ec_ana=0x3f;   Address(0x11[7:0])
SPIWrite 00ce,20,0,7  //Property_ceh_5_5=0x1;
      Address(0xce[7:5])
SPIWrite 00cb,04,0,7  //Property_cbh_2_2=0x1;
      Address(0xcb[7:2])
SPIWrite 00ca,20,0,7  //Property_cah_5_5=0x1;
      Address(0xca[7:5])
SPIWrite 00ce,30,0,7  //Property_ceh_4_4=0x1;
      Address(0xce[7:4])
SPIWrite 00c3,40,0,7  //Property_c3h_6_6=0x1;
      Address(0xc3[7:6])
SPIWrite 00c0,01,0,7  //Property_c0h_0_0=0x1;
      Address(0xc0[7:0])
SPIWrite 00b9,40,0,7  //Property_b9h_6_6=0x1;
      Address(0xb9[7:6])
SPIWrite 00b9,50,0,7  //Property_b9h_4_4=0x1;
      Address(0xb9[7:4])
SPIWrite 00b9,70,0,7  //Property_b9h_5_5=0x1;
      Address(0xb9[7:5])
SPIWrite 00b9,78,0,7  //Property_b9h_3_3=0x1;
      Address(0xb9[7:3])
SPIWrite 0011,00,0,7  //ec_ana=0x0;    Address(0x11[7:0])
SPIWrite 0010,3f,0,7  //ec_dig=0x3f;   Address(0x10[7:0])
SPIWrite 00b0,30,0,7  //Property_b0h_5_5=0x1;
      Address(0xb0[7:5])
SPIWrite 00b4,30,0,7  //Property_b4h_5_5=0x1;
      Address(0xb4[7:5])
SPIWrite 0010,00,0,7  //ec_dig=0x0;    Address(0x10[7:0])
SPIWrite 0019,01,0,7  //Property_19h_0_0=0x1;
      Address(0x19[7:0])
SPIWrite 039c,01,0,7  //Property_37ch_0_0=0x1;
      Address(0x39c[7:0])
SPIWrite 039d,01,0,7  //Property_37ch_8_8=0x1;
      Address(0x39d[7:0])
SPIWrite 039e,01,0,7  //Property_37ch_16_16=0x1;
```

```
     Address(0x39e[7:0])
SPIWrite 039f,01,0,7  //Property_37ch_24_24=0x1;
     Address(0x39f[7:0])
SPIWrite 03a0,01,0,7  //Property_380h_0_0=0x1;
     Address(0x3a0[7:0])
SPIWrite 03a1,01,0,7  //Property_380h_8_8=0x1;
     Address(0x3a1[7:0])

//END: Power Saving Options

SPIWrite 0019,00,0,7  //Property_19h_0_0=0x0;
     Address(0x19[7:0])

//STEP: miscConfig/step1
SPIWrite 0013,40,0,7  //dsa_page1=0x1;      Address(0x13[7:6])
SPIWrite 0124,00,0,7  //spi_agc_dsa_A=0x0;  Address(0x124[7:0])
SPIWrite 0174,00,0,7  //spi_agc_dsa_B=0x0;  Address(0x174[7:0])
SPIWrite 0013,80,0,7  //dsa_page1=0x2;      Address(0x13[7:6])
SPIWrite 0124,00,0,7  //spi_agc_dsa_A=0x0;  Address(0x124[7:0])
SPIWrite 0174,00,0,7  //spi_agc_dsa_B=0x0;  Address(0x174[7:0])
SPIWrite 0013,00,0,7  //dsa_page1=0x0;      Address(0x13[7:6])
SPIWrite 0013,10,0,7  //dsa_page0=0x1;      Address(0x13[7:4])
SPIWrite 00c8,00,0,7  //txa_dsa_index=0x0;  Address(0xc8[7:0])
SPIWrite 00cc,00,0,7  //txb_dsa_index=0x0;  Address(0xcc[7:0])
SPIWrite 0013,20,0,7  //dsa_page0=0x2;      Address(0x13[7:4])
SPIWrite 00c8,00,0,7  //txa_dsa_index=0x0;  Address(0xc8[7:0])
SPIWrite 00cc,00,0,7  //txb_dsa_index=0x0;  Address(0xcc[7:0])
SPIWrite 0013,10,0,7  //dsa_page0=0x1;      Address(0x13[7:4])
SPIWrite 006c,18,0,7  //spi_agc_dsa_fb=0x18;
     Address(0x6c[7:0])
SPIWrite 0013,20,0,7  //dsa_page0=0x2;      Address(0x13[7:4])
SPIWrite 006c,18,0,7  //spi_agc_dsa_fb=0x18;
     Address(0x6c[7:0])
SPIWrite 0013,00,0,7  //dsa_page0=0x0;      Address(0x13[7:4])

//STEP: gpioConfig/step0
SPIWrite 0015,10,0,7  //io_wrap=0x1;   Address(0x15[7:4])
SPIWrite 0420,01,0,7  //preferred_input_sel_gpio_8=0x0;
     Address(0x420[7:2])
SPIWrite 0420,01,0,7  //buf_dir_ctrl_gpio_8=0x1;
     Address(0x420[7:0])
SPIWrite 08c9,00,0,7  //ovr_sel_intpi_tdd_en_fbab=0x0;
     Address(0x8c9[7:1])
SPIWrite 08ca,09,0,7  //crossbar_sel_intpi_tdd_en_fbab=0x9;
     Address(0x8ca[7:0],0x8cb[7:0])
SPIWrite 0420,01,0,7  //preferred_input_sel_gpio_8=0x0;
     Address(0x420[7:2])
SPIWrite 0420,01,0,7  //buf_dir_ctrl_gpio_8=0x1;
     Address(0x420[7:0])
SPIWrite 08cd,00,0,7  //ovr_sel_intpi_tdd_en_fbcd=0x0;
     Address(0x8cd[7:1])
SPIWrite 08ce,09,0,7  //crossbar_sel_intpi_tdd_en_fbcd=0x9;
```

```
      Address(0x8ce[7:0],0x8cf[7:0])
SPIWrite 0454,05,0,7  //preferred_input_sel_gpio_21=0x1;
      Address(0x454[7:2])
SPIWrite 0454,05,0,7  //buf_dir_ctrl_gpio_21=0x1;
      Address(0x454[7:0])
SPIWrite 0905,00,0,7  //ovr_sel_intpi_global_pdn=0x0;
      Address(0x905[7:1])
SPIWrite 04cc,01,0,7  //preferred_input_sel_gpio_51=0x0;
      Address(0x4cc[7:2])
SPIWrite 04cc,01,0,7  //buf_dir_ctrl_gpio_51=0x1;
      Address(0x4cc[7:0])
SPIWrite 09d5,00,0,7  //ovr_sel_intpi_tdd_en_rxa=0x0;
      Address(0x9d5[7:1])
SPIWrite 09d6,2d,0,7  //crossbar_sel_intpi_tdd_en_rxa=0x2d;
      Address(0x9d6[7:0],0x9d7[7:0])
SPIWrite 04cc,01,0,7  //preferred_input_sel_gpio_51=0x0;
      Address(0x4cc[7:2])
SPIWrite 04cc,01,0,7  //buf_dir_ctrl_gpio_51=0x1;
      Address(0x4cc[7:0])
SPIWrite 09d9,00,0,7  //ovr_sel_intpi_tdd_en_rxb=0x0;
      Address(0x9d9[7:1])
SPIWrite 09da,2d,0,7  //crossbar_sel_intpi_tdd_en_rxb=0x2d;
      Address(0x9da[7:0],0x9db[7:0])
SPIWrite 04cc,01,0,7  //preferred_input_sel_gpio_51=0x0;
      Address(0x4cc[7:2])
SPIWrite 04cc,01,0,7  //buf_dir_ctrl_gpio_51=0x1;
      Address(0x4cc[7:0])
SPIWrite 09dd,00,0,7  //ovr_sel_intpi_tdd_en_rxc=0x0;
      Address(0x9dd[7:1])
SPIWrite 09de,2d,0,7  //crossbar_sel_intpi_tdd_en_rxc=0x2d;
      Address(0x9de[7:0],0x9df[7:0])
SPIWrite 04cc,01,0,7  //preferred_input_sel_gpio_51=0x0;
      Address(0x4cc[7:2])
SPIWrite 04cc,01,0,7  //buf_dir_ctrl_gpio_51=0x1;
      Address(0x4cc[7:0])
SPIWrite 09e1,00,0,7  //ovr_sel_intpi_tdd_en_rxd=0x0;
      Address(0x9e1[7:1])
SPIWrite 09e2,2d,0,7  //crossbar_sel_intpi_tdd_en_rxd=0x2d;
      Address(0x9e2[7:0],0x9e3[7:0])
SPIWrite 04a0,01,0,7  //preferred_input_sel_gpio_40=0x0;
      Address(0x4a0[7:2])
SPIWrite 04a0,01,0,7  //buf_dir_ctrl_gpio_40=0x1;
      Address(0x4a0[7:0])
SPIWrite 0a25,00,0,7  //ovr_sel_intpi_fb_ncosel_2=0x0;
      Address(0xa25[7:1])
SPIWrite 0a26,22,0,7  //crossbar_sel_intpi_fb_ncosel_2=0x22;
      Address(0xa26[7:0],0xa27[7:0])
SPIWrite 0530,21,0,7  //preferred_output_sel_gpio_76=0x1;
      Address(0x530[7:5])
SPIWrite 0530,22,0,7  //buf_dir_ctrl_gpio_76=0x2;
      Address(0x530[7:0])
SPIWrite 10b5,00,0,7  //ovr_sel_intpo_rxc_ext_lnabypass_0=0x0;
```

```
      Address(0x10b5[7:1])
SPIWrite 0430,05,0,7  //preferred_input_sel_gpio_12=0x1;
      Address(0x430[7:2])
SPIWrite 0430,05,0,7  //buf_dir_ctrl_gpio_12=0x1;
      Address(0x430[7:0])
SPIWrite 0701,00,0,7  //ovr_sel_intbipi_spib1_sdi=0x0;
      Address(0x701[7:1])
SPIWrite 0404,01,0,7  //preferred_input_sel_gpio_1=0x0;
      Address(0x404[7:2])
SPIWrite 0404,01,0,7  //buf_dir_ctrl_gpio_1=0x1;
      Address(0x404[7:0])
SPIWrite 0a0d,00,0,7  //ovr_sel_intpi_tx_gain_sw_0=0x0;
      Address(0xa0d[7:1])
SPIWrite 0a0e,02,0,7  //crossbar_sel_intpi_tx_gain_sw_0=0x2;
      Address(0xa0e[7:0],0xa0f[7:0])
SPIWrite 0404,01,0,7  //preferred_input_sel_gpio_1=0x0;
      Address(0x404[7:2])
SPIWrite 0404,01,0,7  //buf_dir_ctrl_gpio_1=0x1;
      Address(0x404[7:0])
SPIWrite 0a11,00,0,7  //ovr_sel_intpi_tx_gain_sw_1=0x0;
      Address(0xa11[7:1])
SPIWrite 0a12,02,0,7  //crossbar_sel_intpi_tx_gain_sw_1=0x2;
      Address(0xa12[7:0],0xa13[7:0])
SPIWrite 0404,01,0,7  //preferred_input_sel_gpio_1=0x0;
      Address(0x404[7:2])
SPIWrite 0404,01,0,7  //buf_dir_ctrl_gpio_1=0x1;
      Address(0x404[7:0])
SPIWrite 0a15,00,0,7  //ovr_sel_intpi_tx_gain_sw_2=0x0;
      Address(0xa15[7:1])
SPIWrite 0a16,02,0,7  //crossbar_sel_intpi_tx_gain_sw_2=0x2;
      Address(0xa16[7:0],0xa17[7:0])
SPIWrite 0404,01,0,7  //preferred_input_sel_gpio_1=0x0;
      Address(0x404[7:2])
SPIWrite 0404,01,0,7  //buf_dir_ctrl_gpio_1=0x1;
      Address(0x404[7:0])
SPIWrite 0a19,00,0,7  //ovr_sel_intpi_tx_gain_sw_3=0x0;
      Address(0xa19[7:1])
SPIWrite 0a1a,02,0,7  //crossbar_sel_intpi_tx_gain_sw_3=0x2;
      Address(0xa1a[7:0],0xa1b[7:0])
SPIWrite 0404,01,0,7  //preferred_input_sel_gpio_1=0x0;
      Address(0x404[7:2])
SPIWrite 0404,01,0,7  //buf_dir_ctrl_gpio_1=0x1;
      Address(0x404[7:0])
SPIWrite 0a3d,00,0,7  //ovr_sel_intpi_tx_ncosel_0=0x0;
      Address(0xa3d[7:1])
SPIWrite 0a3e,02,0,7  //crossbar_sel_intpi_tx_ncosel_0=0x2;
      Address(0xa3e[7:0],0xa3f[7:0])
SPIWrite 0500,21,0,7  //preferred_output_sel_gpio_64=0x1;
      Address(0x500[7:5])
SPIWrite 0500,22,0,7  //buf_dir_ctrl_gpio_64=0x2;
      Address(0x500[7:0])
SPIWrite 10b9,00,0,7  //ovr_sel_intpo_rxd_ext_lnabypass_0=0x0;
```

```
      Address(0x10b9[7:1])
SPIWrite 040c,01,0,7  //preferred_input_sel_gpio_3=0x0;
      Address(0x40c[7:2])
SPIWrite 040c,01,0,7  //buf_dir_ctrl_gpio_3=0x1;
      Address(0x40c[7:0])
SPIWrite 08b9,00,0,7  //ovr_sel_intpi_tdd_en_txa=0x0;
      Address(0x8b9[7:1])
SPIWrite 08ba,04,0,7  //crossbar_sel_intpi_tdd_en_txa=0x4;
      Address(0x8ba[7:0],0x8bb[7:0])
SPIWrite 040c,01,0,7  //preferred_input_sel_gpio_3=0x0;
      Address(0x40c[7:2])
SPIWrite 040c,01,0,7  //buf_dir_ctrl_gpio_3=0x1;
      Address(0x40c[7:0])
SPIWrite 08bd,00,0,7  //ovr_sel_intpi_tdd_en_txb=0x0;
      Address(0x8bd[7:1])
SPIWrite 08be,04,0,7  //crossbar_sel_intpi_tdd_en_txb=0x4;
      Address(0x8be[7:0],0x8bf[7:0])
SPIWrite 040c,01,0,7  //preferred_input_sel_gpio_3=0x0;
      Address(0x40c[7:2])
SPIWrite 040c,01,0,7  //buf_dir_ctrl_gpio_3=0x1;
      Address(0x40c[7:0])
SPIWrite 08c1,00,0,7  //ovr_sel_intpi_tdd_en_txc=0x0;
      Address(0x8c1[7:1])
SPIWrite 08c2,04,0,7  //crossbar_sel_intpi_tdd_en_txc=0x4;
      Address(0x8c2[7:0],0x8c3[7:0])
SPIWrite 040c,01,0,7  //preferred_input_sel_gpio_3=0x0;
      Address(0x40c[7:2])
SPIWrite 040c,01,0,7  //buf_dir_ctrl_gpio_3=0x1;
      Address(0x40c[7:0])
SPIWrite 08c5,00,0,7  //ovr_sel_intpi_tdd_en_txd=0x0;
      Address(0x8c5[7:1])
SPIWrite 08c6,04,0,7  //crossbar_sel_intpi_tdd_en_txd=0x4;
      Address(0x8c6[7:0],0x8c7[7:0])
SPIWrite 0438,05,0,7  //preferred_input_sel_gpio_14=0x1;
      Address(0x438[7:2])
SPIWrite 0438,05,0,7  //buf_dir_ctrl_gpio_14=0x1;
      Address(0x438[7:0])
SPIWrite 0899,00,0,7  //ovr_sel_intpi_spib1_cs_n=0x0;
      Address(0x899[7:1])
SPIWrite 0444,05,0,7  //preferred_input_sel_gpio_17=0x1;
      Address(0x444[7:2])
SPIWrite 0444,05,0,7  //buf_dir_ctrl_gpio_17=0x1;
      Address(0x444[7:0])
SPIWrite 089d,00,0,7  //ovr_sel_intpi_spib1_clk=0x0;
      Address(0x89d[7:1])
SPIWrite 0400,01,0,7  //preferred_input_sel_gpio_0=0x0;
      Address(0x400[7:2])
SPIWrite 0400,01,0,7  //buf_dir_ctrl_gpio_0=0x1;
      Address(0x400[7:0])
SPIWrite 09e5,00,0,7  //ovr_sel_intpi_rx_gain_sw_0=0x0;
      Address(0x9e5[7:1])
SPIWrite 09e6,01,0,7  //crossbar_sel_intpi_rx_gain_sw_0=0x1;
```

```
      Address(0x9e6[7:0],0x9e7[7:0])
SPIWrite 0400,01,0,7  //preferred_input_sel_gpio_0=0x0;
      Address(0x400[7:2])
SPIWrite 0400,01,0,7  //buf_dir_ctrl_gpio_0=0x1;
      Address(0x400[7:0])
SPIWrite 0a2d,00,0,7  //ovr_sel_intpi_rx_ncosel_0=0x0;
      Address(0xa2d[7:1])
SPIWrite 0a2e,01,0,7  //crossbar_sel_intpi_rx_ncosel_0=0x1;
      Address(0xa2e[7:0],0xa2f[7:0])
SPIWrite 042c,21,0,7  //preferred_output_sel_gpio_11=0x1;
      Address(0x42c[7:5])
SPIWrite 042c,22,0,7  //buf_dir_ctrl_gpio_11=0x2;
      Address(0x42c[7:0])
SPIWrite 1005,00,0,7  //ovr_sel_intpo_spib1_sdo=0x0;
      Address(0x1005[7:1])
SPIWrite 04b8,21,0,7  //preferred_output_sel_gpio_46=0x1;
      Address(0x4b8[7:5])
SPIWrite 04b8,22,0,7  //buf_dir_ctrl_gpio_46=0x2;
      Address(0x4b8[7:0])
SPIWrite 10b1,00,0,7  //ovr_sel_intpo_rxb_ext_lnabypass_0=0x0;
      Address(0x10b1[7:1])
SPIWrite 0450,01,0,7  //preferred_input_sel_gpio_20=0x0;
      Address(0x450[7:2])
SPIWrite 0450,01,0,7  //buf_dir_ctrl_gpio_20=0x1;
      Address(0x450[7:0])
SPIWrite 09e9,00,0,7  //ovr_sel_intpi_rx_gain_sw_1=0x0;
      Address(0x9e9[7:1])
SPIWrite 09ea,14,0,7  //crossbar_sel_intpi_rx_gain_sw_1=0x14;
      Address(0x9ea[7:0],0x9eb[7:0])
SPIWrite 04c0,05,0,7  //preferred_input_sel_gpio_48=0x1;
      Address(0x4c0[7:2])
SPIWrite 04c0,05,0,7  //buf_dir_ctrl_gpio_48=0x1;
      Address(0x4c0[7:0])
SPIWrite 08a1,00,0,7  //ovr_sel_intpi_adc_sync_n_ab_0=0x0;
      Address(0x8a1[7:1])
SPIWrite 04bc,21,0,7  //preferred_output_sel_gpio_47=0x1;
      Address(0x4bc[7:5])
SPIWrite 04bc,22,0,7  //buf_dir_ctrl_gpio_47=0x2;
      Address(0x4bc[7:0])
SPIWrite 10c5,00,0,7  //ovr_sel_intpo_dac_sync_n_ab_0=0x0;
      Address(0x10c5[7:1])
SPIWrite 046c,21,0,7  //preferred_output_sel_gpio_27=0x1;
      Address(0x46c[7:5])
SPIWrite 046c,22,0,7  //buf_dir_ctrl_gpio_27=0x2;
      Address(0x46c[7:0])
SPIWrite 10bd,00,0,7  //ovr_sel_intpo_alarm_1=0x0;
      Address(0x10bd[7:1])
SPIWrite 04a4,01,0,7  //preferred_input_sel_gpio_41=0x0;
      Address(0x4a4[7:2])
SPIWrite 04a4,01,0,7  //buf_dir_ctrl_gpio_41=0x1;
      Address(0x4a4[7:0])
SPIWrite 0a29,00,0,7  //ovr_sel_intpi_fb_ncosel_3=0x0;
```

```
     Address(0xa29[7:1])
SPIWrite 0a2a,23,0,7  //crossbar_sel_intpi_fb_ncosel_3=0x23;
     Address(0xa2a[7:0],0xa2b[7:0])
SPIWrite 0458,21,0,7  //preferred_output_sel_gpio_22=0x1;
     Address(0x458[7:5])
SPIWrite 0458,22,0,7  //buf_dir_ctrl_gpio_22=0x2;
     Address(0x458[7:0])
SPIWrite 10c1,00,0,7  //ovr_sel_intpo_alarm_2=0x0;
     Address(0x10c1[7:1])
SPIWrite 04a8,21,0,7  //preferred_output_sel_gpio_42=0x1;
     Address(0x4a8[7:5])
SPIWrite 04a8,22,0,7  //buf_dir_ctrl_gpio_42=0x2;
     Address(0x4a8[7:0])
SPIWrite 10ad,00,0,7  //ovr_sel_intpo_rxa_ext_lnabypass_0=0x0;
     Address(0x10ad[7:1])

//START: Leaking Sysref To Dig


//START: Requesting/releasing SPI Access to PLL Pages

SPIWrite 0015,00,0,7  //io_wrap=0x0;   Address(0x15[7:4])
SPIWrite 0015,40,0,7  //digtop=0x1;    Address(0x15[7:6])
SPIWrite 0170,01,0,7  //pll_reg_spi_req_a=0x1;
     Address(0x170[7:0])
SPIWrite 0540,00,0,7  //Property_520h_0_0=0x0;
     Address(0x540[7:0])

SPIPoll 0171,0,0,01
SPIRead 0171,0,0

//Read     pll_reg_spi_a_ack=0x1(Meaning: );;
     Address(0x171[7:0])


//END: Requesting/releasing SPI Access to PLL Pages

SPIWrite 0015,00,0,7  //digtop=0x0;    Address(0x15[7:6])
SPIWrite 0015,01,0,7  //pll=0x1;       Address(0x15[7:0])
SPIWrite 0077,08,0,7  //Property_54h_27_27=0x1;
     Address(0x77[7:3])
SPIWrite 0082,0c,0,7  //Property_60h_21_18=0x3;
     Address(0x82[7:2])
SPIWrite 0077,0b,0,7  //Property_54h_25_16=0x3ff;
     Address(0x76[1:0],0x77[7:0])
SPIWrite 0076,ff,0,7
SPIWrite 0077,0b,0,7  //Property_54h_26_26=0x0;
     Address(0x77[7:2])
SPIWrite 0077,0f,0,7  //Property_54h_26_26=0x1;
     Address(0x77[7:2])
SPIWrite 0077,07,0,7  //Property_54h_27_27=0x0;
     Address(0x77[7:3])
```

```
SPIWrite 0082,00,0,7  //Property_60h_21_18=0x0;
     Address(0x82[7:2])
SPIWrite 0077,04,0,7  //Property_54h_25_16=0x0;
     Address(0x76[1:0],0x77[7:0])
SPIWrite 0076,00,0,7

//START: Requesting/releasing SPI Access to PLL Pages

SPIWrite 0015,00,0,7  //pll=0x0;      Address(0x15[7:0])
SPIWrite 0015,40,0,7  //digtop=0x1;   Address(0x15[7:6])
SPIWrite 0170,00,0,7  //pll_reg_spi_req_a=0x0;
     Address(0x170[7:0])
SPIWrite 0540,00,0,7  //Property_520h_0_0=0x0;
     Address(0x540[7:0])

WAIT 0.2

//END: Requesting/releasing SPI Access to PLL Pages


//END: Leaking Sysref To Dig

SPIWrite 0015,00,0,7  //digtop=0x0;   Address(0x15[7:6])

//STEP: postLinkUp/step0

//START: Removing TDD Pin Overrides.

SPIWrite 0015,80,0,7  //timing_controller=0x1;
     Address(0x15[7:7])
SPIWrite 00ed,00,0,7  //Property_cch_11_8=0x0;
     Address(0xed[7:0])
SPIWrite 00f5,00,0,7  //Property_d4h_9_8=0x0;
     Address(0xf5[7:0])
SPIWrite 00e5,0f,0,7  //Property_c4h_11_8=0xf;
     Address(0xe5[7:0])

//END: Removing TDD Pin Overrides.

SPIWrite 0015,00,0,7  //timing_controller=0x0;
     Address(0x15[7:7])
SPIWrite 0018,20,0,7  //macro=0x1;    Address(0x18[7:5])
SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0x10f;
     Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00,0,7
```

```
SPIWrite 00a1,01,0,7
SPIWrite 00a0,0f,0,7
SPIWrite 00a7,00,0,7  //MACRO_OPERAND_REG1=0x1;
     Address(0xa4[7:0],0xa5[7:0],0xa6[7:0],0xa7[7:0],0xa8[7:0])
SPIWrite 00a6,00,0,7
SPIWrite 00a5,00,0,7
SPIWrite 00a4,01,0,7
SPIWrite 0193,52,0,7  //MACRO_OPCODE=0x52;
     Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
     Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
     Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
     Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
```

```
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0x30f;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00,0,7
SPIWrite 00a1,03,0,7
SPIWrite 00a0,0f,0,7
SPIWrite 0193,53,0,7  //MACRO_OPCODE=0x53;
      Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
      Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
      Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7
```

```
//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0x0;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00,0,7
SPIWrite 00a1,00,0,7
SPIWrite 00a0,00,0,7
SPIWrite 0193,90,0,7  //MACRO_OPCODE=0x90;
      Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
      Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])
```

```
SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
      Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIWrite 0144,08,0,7  //Property_124h_4_2=0x2;
      Address(0x144[7:2])
SPIWrite 0018,00,0,7  //macro=0x0;     Address(0x18[7:5])
SPIWrite 0018,08,0,7  //Property_18h_3_3=0x1;
      Address(0x18[7:3])
SPIWrite 1f8f,64,0,7
SPIWrite 0018,00,0,7  //Property_18h_3_3=0x0;
      Address(0x18[7:3])
SPIWrite 0018,20,0,7  //macro=0x1;     Address(0x18[7:5])
SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0x1;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00,0,7
SPIWrite 00a1,00,0,7
SPIWrite 00a0,01,0,7
SPIWrite 0193,90,0,7  //MACRO_OPCODE=0x90;
      Address(0x193[7:0],0x194[7:0])
```

```
WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
      Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
      Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])
```

```
SPIPoll 00f0,0,0,1

SPIWrite 00a3,01,0,7  //MACRO_OPERAND_REG0=0x101020f;
     Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,01,0,7
SPIWrite 00a1,02,0,7
SPIWrite 00a0,0f,0,7
SPIWrite 0193,9f,0,7  //MACRO_OPCODE=0x9f;
     Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
     Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
     Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
     Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
```

```
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0xb020f;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,0b,0,7
SPIWrite 00a1,02,0,7
SPIWrite 00a0,0f,0,7
SPIWrite 0193,49,0,7  //MACRO_OPCODE=0x49;
      Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
      Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
      Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])
```

```
SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0x10200;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,01,0,7
SPIWrite 00a1,02,0,7
SPIWrite 00a0,00,0,7
SPIWrite 0193,4b,0,7  //MACRO_OPCODE=0x4b;
      Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
      Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4
```

```
//Read     MACRO_ERROR_IN_OPCODE=0x0; Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
      Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,01,0,7  //MACRO_OPERAND_REG0=0x10100ff;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,01,0,7
SPIWrite 00a1,00,0,7
SPIWrite 00a0,ff,0,7
SPIWrite 00a7,00,0,7  //MACRO_OPERAND_REG1=0x0;
      Address(0xa4[7:0],0xa5[7:0],0xa6[7:0],0xa7[7:0],0xa8[7:0])
SPIWrite 00a6,00,0,7
SPIWrite 00a5,00,0,7
SPIWrite 00a4,00,0,7
SPIWrite 0193,13,0,7  //MACRO_OPCODE=0x13;
      Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2
```

```
//Read      MACRO_DONE=0x0; Address(0xf0[7:2])
SPIRead 00f0,2,2
//Read      MACRO_DONE=0x0; Address(0xf0[7:2])
SPIRead 00f0,2,2
//Read      MACRO_DONE=0x0; Address(0xf0[7:2])
SPIRead 00f0,2,2
//Read      MACRO_DONE=0x0; Address(0xf0[7:2])
SPIRead 00f0,2,2
//Read      MACRO_DONE=0x0; Address(0xf0[7:2])
SPIRead 00f0,2,2
//Read      MACRO_DONE=0x0; Address(0xf0[7:2])
SPIRead 00f0,2,2
//Read      MACRO_DONE=0x0; Address(0xf0[7:2])
SPIRead 00f0,2,2
//Read      MACRO_DONE=0x0; Address(0xf0[7:2])
SPIRead 00f0,2,2
//Read      MACRO_DONE=0x0; Address(0xf0[7:2])
SPIRead 00f0,2,2
//Read      MACRO_DONE=0x0; Address(0xf0[7:2])
SPIRead 00f0,2,2
//Read      MACRO_DONE=0x0; Address(0xf0[7:2])
SPIRead 00f0,2,2
//Read      MACRO_DONE=0x0; Address(0xf0[7:2])
SPIRead 00f0,2,2
//Read      MACRO_DONE=0x0; Address(0xf0[7:2])
SPIRead 00f0,2,2
```

```
//Read     MACRO_DONE=0x0;  Address(0xf0[7:2])

SPIRead 00f0,2,2

//Read     MACRO_DONE=0x0;  Address(0xf0[7:2])

SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;       Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
      Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
      Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;       Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;     Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])
```

```
SPIWrite 0018,00,5,5  //macro=0x0;     Address(0x18[7:5])
SPIWrite 0012,01,0,3  //rxdig=0x1;     Address(0x12[7:0])
SPIWrite 14c4,00,0,0  //dc_corr_fw_pause=0x0;
      Address(0x14c4[7:0])
SPIWrite 0012,02,0,3  //rxdig=0x2;     Address(0x12[7:0])
SPIWrite 14c4,00,0,0  //dc_corr_fw_pause=0x0;
      Address(0x14c4[7:0])
SPIWrite 0012,04,0,3  //rxdig=0x4;     Address(0x12[7:0])
SPIWrite 14c4,00,0,0  //dc_corr_fw_pause=0x0;
      Address(0x14c4[7:0])
SPIWrite 0012,08,0,3  //rxdig=0x8;     Address(0x12[7:0])
SPIWrite 14c4,00,0,0  //dc_corr_fw_pause=0x0;
      Address(0x14c4[7:0])
SPIWrite 0012,00,0,3  //rxdig=0x0;     Address(0x12[7:0])
SPIWrite 0012,10,4,5  //fbdig=0x1;     Address(0x12[7:4])
SPIWrite 14c4,00,0,0  //dc_corr_fw_pause=0x0;
      Address(0x14c4[7:0])
SPIWrite 0012,20,4,5  //fbdig=0x2;     Address(0x12[7:4])
SPIWrite 14c4,00,0,0  //dc_corr_fw_pause=0x0;
      Address(0x14c4[7:0])

//START: Removing TDD Pin Overrides.

SPIWrite 0012,00,0,7  //fbdig=0x0;     Address(0x12[7:4])
SPIWrite 0015,80,0,7  //timing_controller=0x1;
      Address(0x15[7:7])
SPIWrite 00ed,00,0,7  //Property_cch_11_8=0x0;
      Address(0xed[7:0])
SPIWrite 00f5,03,0,7  //Property_d4h_9_8=0x3;
      Address(0xf5[7:0])
SPIWrite 00e5,00,0,7  //Property_c4h_11_8=0x0;
      Address(0xe5[7:0])

//END: Removing TDD Pin Overrides.


//START: Removing TDD Pin Overrides.

SPIWrite 00ed,0f,0,7  //Property_cch_11_8=0xf;
      Address(0xed[7:0])
SPIWrite 00f5,00,0,7  //Property_d4h_9_8=0x0;
      Address(0xf5[7:0])
SPIWrite 00e5,00,0,7  //Property_c4h_11_8=0x0;
      Address(0xe5[7:0])

//END: Removing TDD Pin Overrides.


//START: Removing TDD Pin Overrides.

SPIWrite 00ec,00,0,7  //Property_cch_0_0=0x0;
```

```
     Address(0xec[7:0])
SPIWrite 00f4,00,0,7  //Property_d4h_0_0=0x0;
     Address(0xf4[7:0])
SPIWrite 00e4,00,0,7  //Property_c4h_0_0=0x0;
     Address(0xe4[7:0])

//END: Removing TDD Pin Overrides.

SPIWrite 0015,00,0,7  //timing_controller=0x0;
     Address(0x15[7:7])
SPIWrite 0018,20,0,7  //macro=0x1;    Address(0x18[7:5])
SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0x0;
     Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00,0,7
SPIWrite 00a1,00,0,7
SPIWrite 00a0,00,0,7
SPIWrite 0193,15,0,7  //MACRO_OPCODE=0x15;
     Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1; Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
     Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0; Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
     Address(0xf0[7:5])
```

```
SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIWrite 0018,00,0,7  //macro=0x0;     Address(0x18[7:5])

//STEP: postLinkUp/step1
SPIWrite 0016,03,0,7  //adc_jesd=0x3; Address(0x16[7:0])
SPIWrite 0024,00,0,7  //jesd_clear_data=0x0;
      Address(0x24[7:0])
SPIWrite 00f0,0f,0,7  //alarms_serdes_fifo_errors_clear=0xf;
      Address(0xf0[7:0])
SPIWrite 00f0,00,0,7  //alarms_serdes_fifo_errors_clear=0x0;
      Address(0xf0[7:0])
SPIWrite 0016,00,0,7  //adc_jesd=0x0; Address(0x16[7:0])
SPIWrite 0016,0c,0,7  //dac_jesd=0x3; Address(0x16[7:2])
SPIWrite 0064,01,0,7  //jesd_clear_data=0x0;
      Address(0x64[7:4])
SPIWrite 0128,01,0,7  //clear_all_alarms=0x1;
      Address(0x128[7:0])
SPIWrite 0128,00,0,7  //clear_all_alarms=0x0;
      Address(0x128[7:0])
SPIWrite 0128,04,0,7  //clear_all_alarms_to_pap=0x1;
      Address(0x128[7:2])
SPIWrite 0128,00,0,7  //clear_all_alarms_to_pap=0x0;
      Address(0x128[7:2])
SPIWrite 0016,00,0,7  //dac_jesd=0x0; Address(0x16[7:2])
SPIWrite 0019,30,0,7  //txdig=0x3;     Address(0x19[7:4])
SPIWrite 0a40,0f,0,7  //HBF59OvrClr=0xf;    Address(0xa40[7:0])
SPIWrite 0a41,0f,0,7  //HBF23HROvrClr=0xf;  Address(0xa41[7:0])
SPIWrite 0a44,0f,0,7  //mixerOvrClr=0xf;    Address(0xa44[7:0])
SPIWrite 0a45,0f,0,7  //isincOvrClr=0xf;    Address(0xa45[7:0])
SPIWrite 0a46,0f,0,7  //dacDitherOvrClr=0xf;
      Address(0xa46[7:0])
```

```
SPIWrite 0a40,00,0,7  //HBF59OvrClr=0x0;    Address(0xa40[7:0])
SPIWrite 0a41,00,0,7  //HBF23HROvrClr=0x0;  Address(0xa41[7:0])
SPIWrite 0a44,00,0,7  //mixerOvrClr=0x0;    Address(0xa44[7:0])
SPIWrite 0a45,00,0,7  //isincOvrClr=0x0;    Address(0xa45[7:0])
SPIWrite 0a46,00,0,7  //dacDitherOvrClr=0x0;
      Address(0xa46[7:0])
SPIWrite 054d,07,0,7  //Property_52ch_10_0=0x7ff;
      Address(0x54c[2:0],0x54d[7:0])
SPIWrite 054c,ff,0,7
SPIWrite 0580,07,0,7  //Property_560h_2_0=0x7;
      Address(0x580[7:0])
SPIWrite 0589,07,0,7  //Property_568h_10_8=0x7;
      Address(0x589[7:0])
SPIWrite 06b4,01,0,7  //pap_hw_alarm_act_alc_clr=0x1;
      Address(0x6b4[7:0])
SPIWrite 06b4,03,0,7  //pap_hw_alarm_act_lmt_clr=0x1;
      Address(0x6b4[7:1])
SPIWrite 054d,00,0,7  //Property_52ch_10_0=0x0;
      Address(0x54c[2:0],0x54d[7:0])
SPIWrite 054c,00,0,7
SPIWrite 0580,00,0,7  //Property_560h_2_0=0x0;
      Address(0x580[7:0])
SPIWrite 0589,00,0,7  //Property_568h_10_8=0x0;
      Address(0x589[7:0])
SPIWrite 06b4,02,0,7  //pap_hw_alarm_act_alc_clr=0x0;
      Address(0x6b4[7:0])
SPIWrite 06b4,00,0,7  //pap_hw_alarm_act_lmt_clr=0x0;
      Address(0x6b4[7:1])
SPIWrite 052c,1f,0,7  //Property_50ch_4_0=0x1f;
      Address(0x52c[7:0])
SPIWrite 052c,00,0,7  //Property_50ch_4_0=0x0;
      Address(0x52c[7:0])
SPIWrite 0019,00,0,7  //txdig=0x0;    Address(0x19[7:4])

//END: Device Config Complete

SPIWrite 0015,80,0,7  //timing_controller=0x1;
      Address(0x15[7:7])
SPIWrite 00a2,00,0,7  //rxgswap_mode_ab=0x0;
      Address(0xa2[7:0])
SPIWrite 00a3,00,0,7  //rxgswap_mode_cd=0x0;
      Address(0xa3[7:0])
SPIWrite 00a4,01,0,7  //enable_rx_gain_swap_a=0x1;
      Address(0xa4[7:0])
SPIWrite 00a5,00,0,7  //enable_rx_gain_swap_b=0x0;
      Address(0xa5[7:0])
SPIWrite 00a6,00,0,7  //enable_rx_gain_swap_c=0x0;
      Address(0xa6[7:0])
SPIWrite 00a7,00,0,7  //enable_rx_gain_swap_d=0x0;
      Address(0xa7[7:0])
SPIWrite 00a8,01,0,7  //broadcast_swap_rx=0x1;
      Address(0xa8[7:0])
```

```
SPIWrite 00b5,02,0,7  //enable_fb_gain_swap_ab=0x2;
     Address(0xb5[7:0])
SPIWrite 00b6,02,0,7  //enable_fb_gain_swap_cd=0x2;
     Address(0xb6[7:0])
SPIWrite 0090,00,0,7  //enable_tx_gain_swap_a=0x0;
     Address(0x90[7:0])
SPIWrite 0091,01,0,7  //enable_tx_gain_swap_b=0x1;
     Address(0x91[7:0])
SPIWrite 0092,00,0,7  //enable_tx_gain_swap_c=0x0;
     Address(0x92[7:0])
SPIWrite 0093,00,0,7  //enable_tx_gain_swap_d=0x0;
     Address(0x93[7:0])
SPIWrite 0094,00,0,7  //broadcast_swap_tx=0x0;
     Address(0x94[7:0])
SPIWrite 009c,00,0,7  //enable_txncosel_a=0x0;
     Address(0x9c[7:0])
SPIWrite 009e,00,0,7  //enable_txncosel_c=0x0;
     Address(0x9e[7:0])
SPIWrite 009f,00,0,7  //enable_txncosel_d=0x0;
     Address(0x9f[7:0])
SPIWrite 00b1,00,0,7  //enable_rxncosel_b=0x0;
     Address(0xb1[7:0])
SPIWrite 00b2,00,0,7  //enable_rxncosel_c=0x0;
     Address(0xb2[7:0])
SPIWrite 00b3,00,0,7  //enable_rxncosel_d=0x0;
     Address(0xb3[7:0])
SPIWrite 0015,00,0,7  //timing_controller=0x0;
     Address(0x15[7:7])
SPIWrite 0016,40,0,7  //serdes_jesd=0x2;    Address(0x16[7:5])
SPIWrite 47eb,0d,0,7  //PU_TX_LANE=0x0;     Address(0x80f6[7:7])
SPIWrite 47ea,b0,0,7
SPIWrite 45eb,0d,0,7  //PU_TX_LANE=0x0;     Address(0x80f6[7:7])
SPIWrite 45ea,b0,0,7
SPIWrite 41eb,0d,0,7  //PU_TX_LANE=0x0;     Address(0x80f6[7:7])
SPIWrite 41ea,b0,0,7
SPIWrite 43eb,0d,0,7  //PU_TX_LANE=0x0;     Address(0x80f6[7:7])
SPIWrite 43ea,b0,0,7
SPIWrite 0016,20,0,7  //serdes_jesd=0x1;    Address(0x16[7:5])
SPIWrite 43eb,0d,0,7  //PU_TX_LANE=0x0;     Address(0x80f6[7:7])
SPIWrite 43ea,b0,0,7
SPIWrite 41eb,0d,0,7  //PU_TX_LANE=0x0;     Address(0x80f6[7:7])
SPIWrite 41ea,b0,0,7
SPIWrite 0016,40,0,7  //serdes_jesd=0x2;    Address(0x16[7:5])
SPIWrite 47f7,6f,0,7  //PU_RX_ADC_LANE=0x0;
     Address(0x80fb[7:2])
SPIWrite 47f6,00,0,7
SPIWrite 47fd,23,0,7  //PU_RX_INTP_LANE=0x0;
     Address(0x80fe[7:2])
SPIWrite 47fc,00,0,7
SPIWrite 47ff,00,0,7  //PU_RX_AGC_LANE=0x0;
     Address(0x8100[7:7])
SPIWrite 47fe,b6,0,7
```

```
SPIWrite 49f1,12,0,7  //PU_RX_INTP_LANE0=0x0;
     Address(0x84f9[7:7])
SPIWrite 49f0,40,0,7
SPIWrite 49f3,8a,0,7  //PU_RX_ADC_LANE0=0x0;
     Address(0x84fa[7:5])
SPIWrite 49f2,80,0,7
SPIWrite 45f7,6f,0,7  //PU_RX_ADC_LANE=0x0;
     Address(0x80fb[7:2])
SPIWrite 45f6,00,0,7
SPIWrite 45fd,23,0,7  //PU_RX_INTP_LANE=0x0;
     Address(0x80fe[7:2])
SPIWrite 45fc,00,0,7
SPIWrite 45ff,00,0,7  //PU_RX_AGC_LANE=0x0;
     Address(0x8100[7:7])
SPIWrite 45fe,b6,0,7
SPIWrite 49f1,02,0,7  //PU_RX_INTP_LANE1=0x0;
     Address(0x84f9[7:4])
SPIWrite 49f0,40,0,7
SPIWrite 49f3,82,0,7  //PU_RX_ADC_LANE1=0x0;
     Address(0x84fa[7:3])
SPIWrite 49f2,80,0,7
SPIWrite 41f7,6f,0,7  //PU_RX_ADC_LANE=0x0;
     Address(0x80fb[7:2])
SPIWrite 41f6,00,0,7
SPIWrite 41fd,23,0,7  //PU_RX_INTP_LANE=0x0;
     Address(0x80fe[7:2])
SPIWrite 41fc,00,0,7
SPIWrite 41ff,00,0,7  //PU_RX_AGC_LANE=0x0;
     Address(0x8100[7:7])
SPIWrite 41fe,b6,0,7
SPIWrite 49f1,00,0,7  //PU_RX_INTP_LANE2=0x0;
     Address(0x84f9[7:1])
SPIWrite 49f0,40,0,7
SPIWrite 49f3,80,0,7  //PU_RX_ADC_LANE2=0x0;
     Address(0x84fa[7:1])
SPIWrite 49f2,80,0,7
SPIWrite 43f7,6f,0,7  //PU_RX_ADC_LANE=0x0;
     Address(0x80fb[7:2])
SPIWrite 43f6,00,0,7
SPIWrite 43fd,23,0,7  //PU_RX_INTP_LANE=0x0;
     Address(0x80fe[7:2])
SPIWrite 43fc,00,0,7
SPIWrite 43ff,00,0,7  //PU_RX_AGC_LANE=0x0;
     Address(0x8100[7:7])
SPIWrite 43fe,b6,0,7
SPIWrite 49f1,00,0,7  //PU_RX_INTP_LANE3=0x0;
     Address(0x84f8[7:6])
SPIWrite 49f0,00,0,7
SPIWrite 49f3,80,0,7  //PU_RX_ADC_LANE3=0x0;
     Address(0x84f9[7:7])
SPIWrite 49f2,00,0,7
SPIWrite 0016,20,0,7  //serdes_jesd=0x1;    Address(0x16[7:5])
```

```
SPIWrite 43f7,6f,0,7  //PU_RX_ADC_LANE=0x0;
     Address(0x80fb[7:2])
SPIWrite 43f6,00,0,7
SPIWrite 43fd,23,0,7  //PU_RX_INTP_LANE=0x0;
     Address(0x80fe[7:2])
SPIWrite 43fc,00,0,7
SPIWrite 43ff,00,0,7  //PU_RX_AGC_LANE=0x0;
     Address(0x8100[7:7])
SPIWrite 43fe,b6,0,7
SPIWrite 41f7,6f,0,7  //PU_RX_ADC_LANE=0x0;
     Address(0x80fb[7:2])
SPIWrite 41f6,00,0,7
SPIWrite 41fd,23,0,7  //PU_RX_INTP_LANE=0x0;
     Address(0x80fe[7:2])
SPIWrite 41fc,00,0,7
SPIWrite 41ff,00,0,7  //PU_RX_AGC_LANE=0x0;
     Address(0x8100[7:7])
SPIWrite 41fe,b6,0,7
SPIWrite 0016,00,0,7  //serdes_jesd=0x0;    Address(0x16[7:5])
SPIWrite 0015,40,0,7  //digtop=0x1;    Address(0x15[7:6])
SPIWrite 0180,00,0,7  //Property_160h_3_0=0x0;
     Address(0x180[7:0])
SPIWrite 0181,0a,0,7  //Property_160h_11_8=0xa;
     Address(0x181[7:0])
SPIWrite 0015,00,0,7  //digtop=0x0;    Address(0x15[7:6])
```