User's Guide
High Speed Data Converter Pro GUI

TEXAS INSTRUMENTS

ABSTRACT

This document outlines the High-Speed Data Converter Pro Graphical User Interface (HSDC Pro GUI). Instructions for software start up and the user interface are included. Operating procedures for ADC data capture software and TSW14xxx pattern generation are also provided along with functional descriptions of the TSW1400, TSW1405, TSW1450, and TSW14J5x capture cards.

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1 Introduction

The HSDC Pro GUI supports testing of all TI high-speed data converter EVMs when used with a TSW14xxx EVM. When used with an ADC EVM, high-speed data (either CMOS, LVDS, JESD204B serial, or JESD204C serial) is captured and then stored into a memory bank or directly inside the FPGA, depending on which TSW14xxx platform is being used. To acquire data on a host PC, the FPGA reads the data from memory and transmits it on Serial Peripheral Interface (SPI). An onboard high-speed USB-to-SPI converter bridges the FPGA SPI interface to the host PC and GUI.

In Pattern Generator Mode, HSDC Pro can generate the desired test patterns or load existing patterns for DAC EVMs under test. These patterns are sent from the host PC over the USB interface to the TSW14xxx. The FPGA stores the data received internally or into board memory, depending on the platform used. The data is then read by the FPGA and transmitted to a DAC EVM across the mating connector.

HSDC Pro GUI utilizes a DLL and a set of API's to communicate from the GUI to the TSW14J5x via a Cypress FX3 USB 3.0 device. This next-generation USB 3.0 controller provides a programmable parallel interface which connects directly to the FPGA to provide high speed data transfers. The interface is compatible with both USB 2.0 and 3.0 systems. The theoretical limit for data transfer via USB 3.0 is 5Gbps and USB 2.0 is 480 Mbps. But with packet overhead and handshaking latency the effective throughput via the Cypress FX3 device is 2Gbps for USB 3.0 systems and 320Mbps for USB 2.0 systems. The samples that are transferred to PC will undergo post processing and will be stored as a binary file, due to which the effective data transfer rate is again reduced. With a 3.0 system, the user can capture 1GBytes ≈ 20 seconds (400Mbps). With a 2.0 system, around 45 seconds (177Mbps). This controller is also used to configure the onboard FPGA using parallel programming mode, which allows for configuration in less than three seconds.

For the TSW1400/05/06 EVMs, the GUI communicates via a FTDI FT4232H device. The FT4232H is a USB 2.0 Hi-Speed to UART IC. It has the capability of being configured in a variety of industry standards, such as serial or parallel interfaces. The FT4232H features 4 UARTs. Two of these have an option to independently configure an MPSSE engine, this allows the FT4232H to operate as two UART/Bit-Bang ports plus two MPSSE engines used to emulate JTAG, SPI, I2C, Bit-bang or other synchronous serial modes.

Key features of the HSDC Pro Software:

- Single- or multiple-tone frequency tests
- Continuous data captures
- Channel power measurement
- External trigger capability
- Master and slave operation
- Pattern generator
- Load custom patterns
- Save and export captured data
- Frequency and Time analysis
- One GUI supports all TSW14xxx platforms

The TSW14xxx family consists of the following EVM's:
- TSW1400 – The TSW1400 EVM supports all high-speed ADC and DAC EVM's that use an LVDS or CMOS interface for the data path.
- TSW1405 – Low cost, limited memory data capture card to be used with all high-speed ADC EVM's with LVDS interface.
- TSW1406 – Low cost, limited memory pattern generator card to be used with all high-speed DAC EVM's with LVDS interface.
- TSW14J10 - The TSW14J10 EVM allows users to evaluate TI JESD204B high-speed data converters using existing FPGA vendor development platforms.
- TSW14J50 – The TSW14J50 EVM supports all high-speed ADC and DAC EVMs using a JESD204B interface for the data path.
- TSW14J56 – The TSW14J56 EVM supports all high-speed ADC and DAC EVMs using a JESD204B interface for the data path.

- TSW14J57 – The TSW14J57 EVM supports up to 16 lanes for all high-speed ADC and DAC EVMs using a JESD204B interface for the data path.
- TSW14J58 - The TSW14J58 EVM supports up to 16 lanes for all high-speed ADC and DAC EVMs using a JESD204C interface for the data path.
- TSW14DL3200 - The TSW14DL3200 EVM supports up to 48 pairs of high-speed LVDS signals or to provide up to 48 pairs of LVDS data.

Consult the TSW140x High Speed Data Capture/Pattern Generator Card User's Guide (SLWU079) for more information regarding the hardware aspect of the TSW1400, TSW1405 and TSW1406 EVMs.

Consult the TSW14J5x JESD204B/C High Speed Data Capture and Pattern Generator Card User's Guide for more information regarding the hardware aspect of these four EVMs.

Consult the TSW14DL3200EVM High Speed LVDS Data Capture/Pattern Generator Card User's Guide for more information regarding the hardware aspect of this EVM.

Additionally, the user has the option of using Xilinx FPGA development kits to interface with TI's JESD204B based high-speed data converter EVMs.

2 Software Start up

2.1 Installation Instructions

- Download the latest version of the HSDC Pro GUI to a local location on a host PC. This can be found on the TI website by entering "HIGH SPEED DATA CONVERTER PRO GUI INSTALLER" or "TSW1400EVM" in the search parameter window at www.ti.com.
- Unzipping the software package will generate a folder called "High Speed Data Converter Pro - Installer vx.xx.exe", where x.xx is the version number. Run this program to start the installation.
- Make sure to disconnect all USB cables from any TSW14xxx boards before installing the software.
- Follow the on-screen instructions during installation.
- Click on the "Install" button. A new window opens. Click the "Next" button.
- Accept the License Agreement. Click on the "Next" button to start the installation. After the installer has finished, click the "Next" button one last time.
- The installation is now complete. The GUI executable and associated files will reside in the following directory:
  C:\Program Files (x86)\Texas Instruments\High Speed Data Converter Pro.
- Power up the TSW14xxx under test.
- To start the GUI, click on the file called "High Speed Data Converter Pro.exe", located under
  C:\Program Files (x86)\Texas Instruments\High Speed Data Converter Pro.

Note

If an older version of the GUI has already been installed, make sure to uninstall it before loading a newer version. If the GUI detects that a newer version of the GUI is available online (http://www.ti.com/tool/tsw1400evm), it will assist the user with downloading the latest version from the TI website. The GUI automatically interrogates the product website for latest version every seven days but the latest version check can also be manually invoked through use of the pull-down menu Help->Check for updates.

Note

When new TI HSDC EVMs become available that are not supported with the current GUI software release, the HSDCProv_xpxx_Patch_setup executable, available on the TI website (www.ti.com), will allow the user to add these EVMs to the GUI device list. Doing a search for TSW1400 will direct the user to this location. The user should download this patch . Start the application and follow the on screen instructions. The patch will display the files that will be either added or replaced and have tabs for viewing what files will be deleted and release notes. After running the patch, the user will then be able to start the High Speed Data Converter Pro GUI and notice new parts added to the ADC and DAC device drop down selection box. The patch is always specific to a core GUI version so the patch application would not work for any GUI version that the patch was not explicitly created for.

2.2 USB Interface and Drivers

The HSDC Pro GUI will first attempt to connect to the EVM USB interface. If the GUI identifies a valid board serial number, a pop-up will open displaying this value, as shown in Figure 2-1. The serial number also has an EVM type number attached to it. This indicates to the GUI which TSW14xxx board is presently connected to the host PC. It is possible to connect several TSW14xxx EVM's to one host PC but the GUI can only connect to one at a time. If multiple boards are connected to the PC, the pop-up displays all of the serial numbers found. It is then up to the user to select which board the GUI will be associated with.
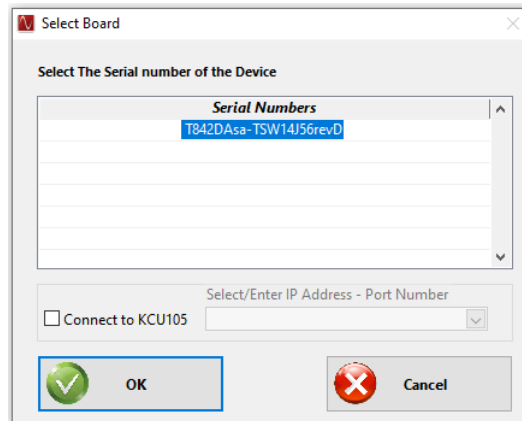
Figure 2-1. TSW14xxx EVM Serial Number

Click on "OK" to connect the GUI to the board. If the FPGA firmware version read by the GUI does not match the firmware to be used as determined by the device selected (see section 3.4 for more info on device selection), the following message appears as shown in Figure 2-2. This message also appears after power up as the FPGA is not programmed.
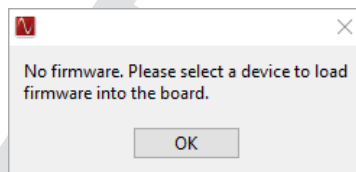
Figure 2-2. Firmware Does Not Match the Device Selected

Click on "OK". The Top level GUI now opens and appears as shown in Figure 2-3.
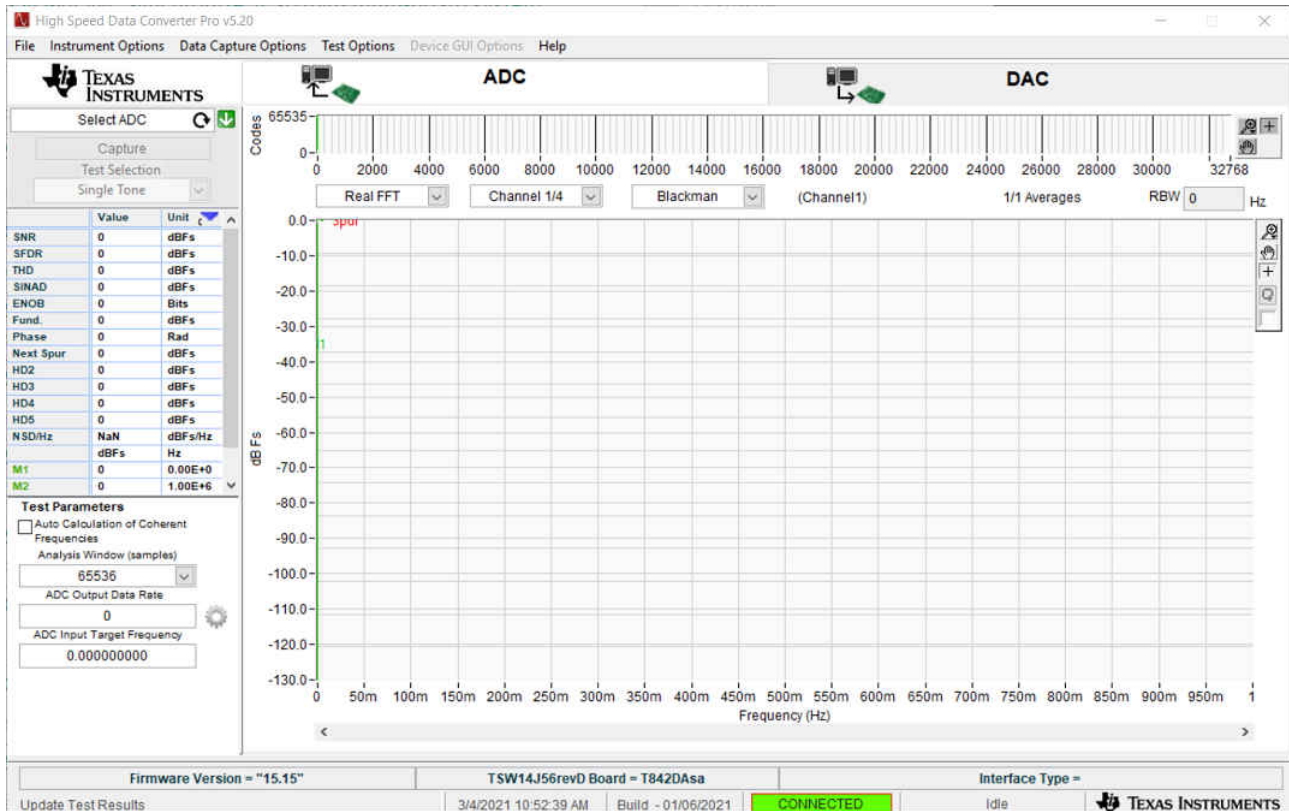
Figure 2-3. TSW14xxx EVM GUI Top Level

After the software has established a connection, if the message "No Board Connected" opens, double check the USB cable connections and that power is present. If the cable connections appear fine, try establishing a connection by clicking on the "Instrument Options" tab at the top left of the GUI and select "Connect to the Board" (see Figure 2-4). If this does not help, disconnect the USB cable from the board then reconnect it, click on the "Instrument Options" tab, then select "Connect to the Board". If this still does not correct the issue, check the status of the host USB port.
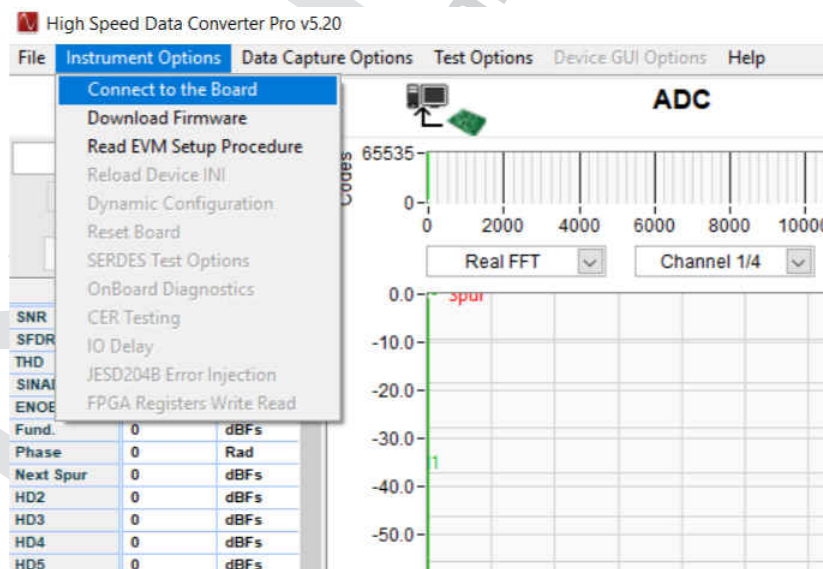
Figure 2-4. Connecting GUI to EVM

When the software has been installed and the USB cable has been connected to a TSW1400/05/06 EVM and the PC, the USB serial converter should be located in the Hardware Device Manager under the Universal Serial Bus controllers as shown in Figure 2-5. This is a quad device which is why there is an A, B, C, and D USB Serial Converter shown. When the USB cable is removed, these four will no longer be visible in the Device Manager. If the drivers are present in the Device Manager window and the software still does not connect, cycle power to the board and repeat the steps above.

If the GUI starts up but freezes before it brings up the "Connected to Board" dialog, or takes an unusually long time for other actions to occur, it is possible the USB being used from the host PC is operating at USB 1.0 speeds. A common indication of this is when the status bar on the bottom left of the screen keeps reading "Disable all Controls" upon loading the software without ever going to the "Connect Board Dialog". The GUI is designed to run at USB 3.0 speeds and some computers have USB 1.0 ports on the front panel and 2.0 or 3.0 on the back panel. Using the 3.0 ports on the back of the PC if at all possible is recommended.

The .exe file installs the FTDI drivers during software installation. If after connecting the USB cable and Windows lists the board as an "unknown device", this could be caused by corrupted FTDI drivers being installed on the computer. This happens in cases where the same computer has been used to interface with previous products that used FTDI drivers. In this case, users are advised to download and install a utility from FTDI at http://www.ftdichip.com/Support/Utilities/CDMUninstaller_v1.4.zip.

The help file for using this utility can be found at: http:/www.ftdichip.com/Support/Utilities/CDM_Uninst_GUI_Readme.html

Users will need to use the following hex values to uninstall previous versions of the ftdi drivers:

Vendor ID (VID): 0403

Product ID (PID): 6010

After removing the drivers for this PID and VID, users are advised to re-connect the TSW14xxx USB cable and check if the TSW14xxx ports get listed properly in Device Manager.

For the TSW14J5x, the .exe file installs the Cypress USB 3.0 drivers during software installation. The USB 3.0 driver, called "Cypress FX3 USB StreamerExample Device", should be located in the Hardware Device Manager under the Universal Serial Bus controllers as shown in Figure 2-6.

If after connecting the USB cable and Windows lists the board as an "unknown device", this could be caused by the Cypress USB 3.0 not booting properly from the flash device. Press the USB reset switch SW11 (SW5 on J57) and try to reconnect the GUI. If this does not work cycle the board power.
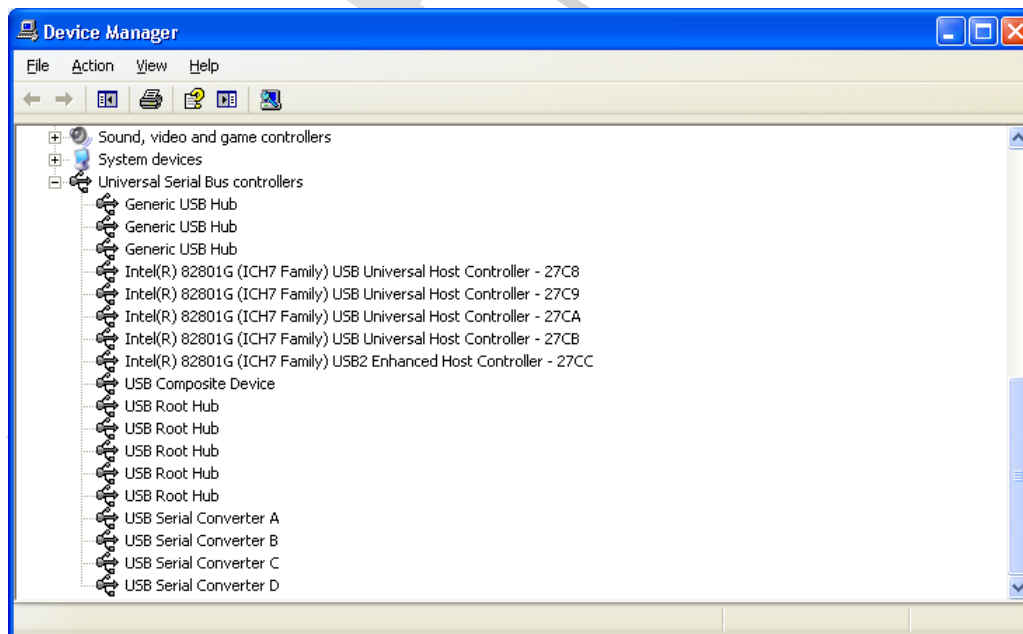
Figure 2-5. Hardware Device Manager
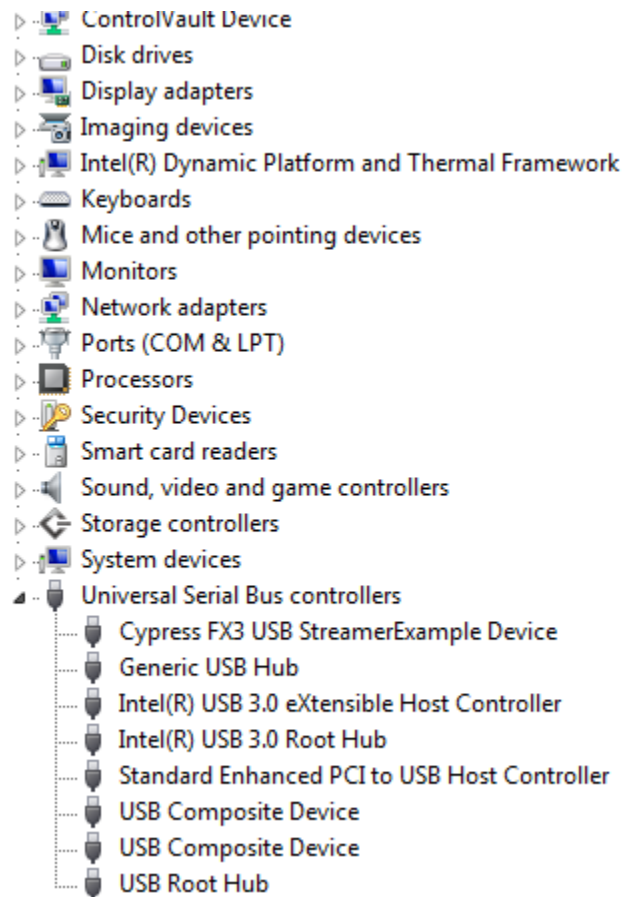
Figure 2-6. Cypress FX3 USB Streamer Example Device in USB Controllers

2.3 Device ini Files

Included in the installation for the HSDC Pro GUI software is a subdirectory of ini files for each category of ADC and DAC that is supported by the TSW14xxx EVMs. TI strongly recommends that these files are not edited except at the factory. These files contain necessary information for the GUI software to properly configure the TSW14xxx EVM FPGA registers for proper operation with the desired ADC or DAC EVM. Some of the entries within the ini file are obvious, such as defining the bit resolution for a device as 11, 12, 14, or 16 bits. Other entries in the ini file define for the FPGA which LVDS pairs within the Samtec connector comprise the data bus, and correct operation may not be possible if these entries are edited. The use of ini files allows for new device types to be supported by the TSW14xxx EVM as they become available without having to modify, re-release, or re-install the HSDC Pro GUI software. New device types may be supported at a later date simply by adding a new ini file to the proper subdirectory.

3 User Interface

When the HSDC Pro GUI software is started, the initial setup screen of Figure 2-3 appears. The TSW14xxx EVM serial number is reported in the lower center of the GUI. After the FPGA is loaded with the selected firmware, the GUI will report the firmware version in the lower left and the interface type will be reported in the lower right. The connection status should read "Connected" and be highlighted in green (lower center of the GUI). The status panel, located in the lower right, will report "IDLE". Many of the TSW14xxx software controls are available from the main screen, such as "ADC or DAC" mode, "Select device", "Capture and Test Selection" (ADC mode only), and "Load External Pattern File" (DAC mode only).

3.1 Toolbar

The toolbar contains options and settings that are independent of the device selected for test or the test to be performed, such as configuration options and save/recall operations. The operations available under the toolbar are grouped in categories as follows: File, Instrument Options, Data Capture Options, Test Options and Help.

3.1.1 File Options

The file tab contains all of the options for saving or importing test results. Placing the mouse indicator over the File tab will open a window with the available options as shown in Figure 3-1.
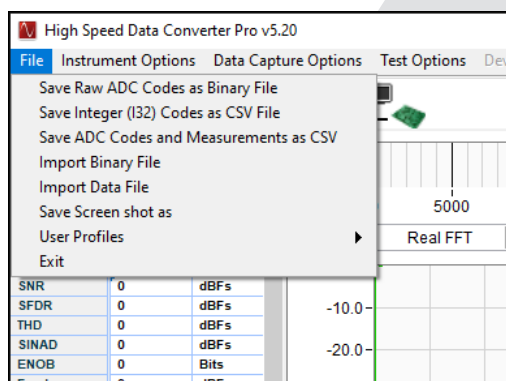
Figure 3-1. File Tab Options

There are options for saving the ADC captured data as 32 bit singed integer (I32) CSV or Binary format in a directory specified by the user for export or archival purposes. The "Save I32 Codes as CSV File" options will save the captured ADC data as 32 bit singed integers with each channel's data across columns in a CSV file. The CSV data can range from $- 2^{(Number\ of\ Bits\ -1)}$ to $2^{(Number\ of\ Bits\ -1)} – 1$. The "Save ADC Codes and Measurements as CSV" option will save the captured ADC data as 32 bit singed integers along with the measurements data as CSV file. The "Save Raw ADC Codes as Binary File" option will save the raw data captured from the ADC as a binary file. The "Save Screen shot as" option, when selected, will open a window that will allow the user to save the current GUI screen shot as either a bmp, jpeg, or png file in the directory specified by the user.

Note: Number of Bits = Sample resolution.

The GUI provides an option to allow the user to replay files captured from an ADC by the GUI itself. To use this feature, import a test file by either selecting "Import Binary File" or "Import Data File" in the drop down. A new navigator window will open. Select the desired file to be loaded. If a binary file is to be used select "Import Binary File" menu option, after the file is selected (.bin file), a new window will open asking for number of channels and number of bits. Provide this information then click "OK". The format of the binary sample is big-endian and the size of the samples should be either 2 Bytes (for sample resolutions less than or equal to 16) or 4 Bytes (for sample resolutions greater than 16 and less than or equal to 32). For multiple channel test cases, the test file must have channel data interleaved. For example, if there are 4 channels, the samples should be arranged as Channel1Sample1, Channel2Sample1, Channel3Sample1, Channel4Sample1, Channel1Sample2, Channel2Sample2, Channel3Sample2, Channel4Sample2,……, Channel1SampleN, Channel2SampleN, Channel3SampleN, Channel4SampleN.

For the "Import Data File" option, the user can use several different types of files. After the file is selected, the GUI will ask for number of channels and number of bits. The user must know this information for proper data to be displayed. The data test file must be in text format having integer values from – 2^ (Number of Bits -1) to 2^ (Number of Bits -1) – 1. For two channel test cases, channel 1 is the data in the first column and channel 2 is the data in the second column. The different file types that can be used include .gcin (space), .ssv (space), .csv (comma), .txt (tab), and .tsw. The GUI expects such files to be delimited by the delimiters shown in the parentheses. Adjacent columns are separated by the delimiter. The .tsw files are proprietary encoded files created by Texas Instruments.

3.1.1.1 User Profiles

This option can be used to save the user interface settings to a file and load it while launching the GUI (by default) or whenever needed. The list of UI settings that are being saved are *Test Selection*, *Graph Type*, *FFT Window*, and *Filter Parameters* available in *Notch Frequency* bins of the GUI. Clicking on 'User Profiles' under 'File' menu will list down the submenu as shown in Figure 3-2.
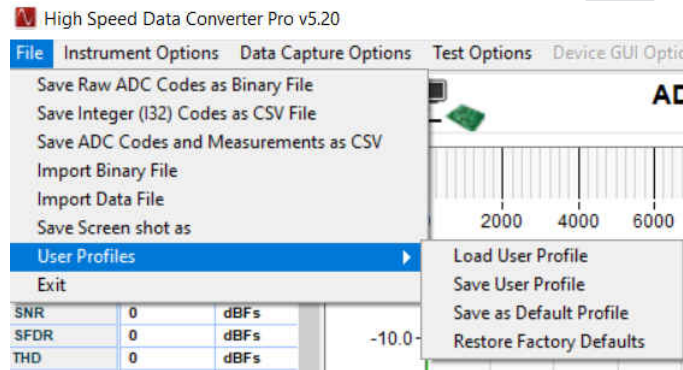
Figure 3-2. User Profiles

Load User Profile – Clicking on this option opens the 'Open' dialog box where user-saved file, default file, or factory settings file can be loaded.

Save User Profile – This option saves the current UI settings to a file and prompts the user to specify the name of the file in the 'Save As' dialog box.

Save as Default Profile - This option will replace the default profile file with the current settings in the GUI. Whenever the GUI is launched, the default profile will be loaded.

Restore Factory Defaults – This option will restore the default settings that came along with the installer and also replace the default profile file with these values.

3.1.2 Instrument Options

The Instrument Options menu tab contains 4 generic options: Connect or Disconnect from the board, Download Firmware, Read EVM Setup Procedure, and Reload INI. The Dynamic Configuration, Reset Board and SERDES Test Options, Onboard Diagnostics, CER Testing, IO Delay, JESD204B Error Injection and FPGA Registers Write Read options are specific to some TSW14xxx boards and selected device INIs. These options are listed when selecting the Instrument Options menu as shown in Figure 3-3.
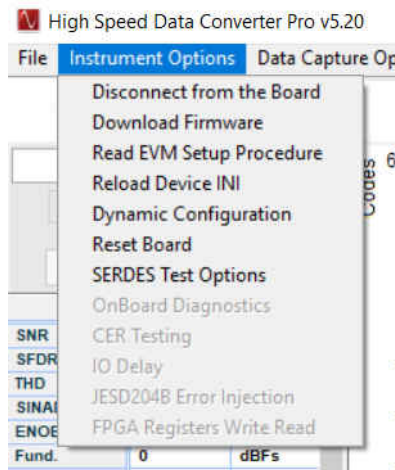
Figure 3-3. Instrument Options

The Connect to the Board command will cause the GUI to read the serial number inside the USB controller on the TSW14xxx and display the value found or report that no board is connected. This can be used when a user removes power from the TSW14xxx board, then re-applies power while leaving the GUI active. Disconnect from the Board will release the GUI from the USB interface and allow the GUI to now be connected to another board. This is useful when operating multiple TSW14xxx EVMs with one computer.

The Download Firmware command allows the user to select a file that will be used to program the FPGA. These files need to be .rbf or .bin files for this to work. The files used by the GUI currently reside in the directory called "Firmware", under the TSW14xxx directory. This option would be used if the GUI cannot identify the firmware file called out in the ini file, or if an advanced user has a new file they would like to try.

The Read EVM Setup Procedure command causes the HSDC Pro software to read a comment string from the ini file for the device that is currently selected and then display that comment string in the status pane. This comment string generally contains necessary setup information pertaining to the EVM under test, such as possibly requiring a non-default data format or required jumper setting for the EVM to communicate properly with the TSW14xxx. Some ini files may not support this feature though.

Reload Device INI causes HSDC Pro software to reload INI files for the selected ADC or DAC device. For more information on INI files, refer to Section 2.3.

The Dynamic Configuration command is used by the TSW14J5x JESD204B serial interface EVMs only. This command allows the user to change certain JESD204B parameters such as number of lanes, number of converters, number of octets per frame, and so forth. See Section 10 for more information regarding this command.

The Reset Board command is currently only used with the TSW14J5x EVMs. The firmware for this EVM has a reset register that will initialize the firmware without reloading the firmware.

The SERDES Test Options tab provides the ability to analyze the device by measuring the eye opening. The EyeQ Scan feature is discussed in further detail in the section below.

IO Delay, JESD204B Error Injection, and FPGA Registers Write Read is discussed in the sections below.

3.1.2.1 TSW14J56 and High Speed Data Converter (HSDC) Pro Eye Quality Analysis

The TSW14J56EVM utilizes an Intel PSG® Arria® V GZ FPGA device for the receive and transmit functions for the JESD204B link. One of the features of the Arria® V GZ device is the On-Chip Signal Quality Monitoring Circuitry (EyeQ). The EyeQ feature is a debug and diagnosis tool that analyzes the received data by measuring the horizontal and vertical eye opening.

The following section provides a quick start-up example that highlights the software features of the EyeQ Scan analysis.
1. Verify that the ADC EVM provides an FFT capture on HSDC Pro.
2. Under the "Instrument Options" tab, click on "SERDES Test Options".

3. A new window should appear with the following features:
   - Lane – Selects one of the available lanes for the selected interface mode
   - Time per iteration – Selects how long data is accumulated before generation of the Eye diagram. Increasing this value also increases the Test Time proportionally
   - EQ DC Gain – Adjusts DC gain of FPGA receive hardware block
   - EQ AC Gain – Adjusts AC gain of FPGA receive hardware block
   - Display Standard Eye – Overlays one of the JESD204B receive eye-mask templates onto the Eye diagram
4. After configuring the parameters, click on "START". The scan may take a few seconds to a few minutes depending on the parameters chosen.

Figure 3-4 shows an eye diagram of the ADC34J45EVM in 442 mode, sampling at 140 MHz and a lane rate of 2.8 GHz.
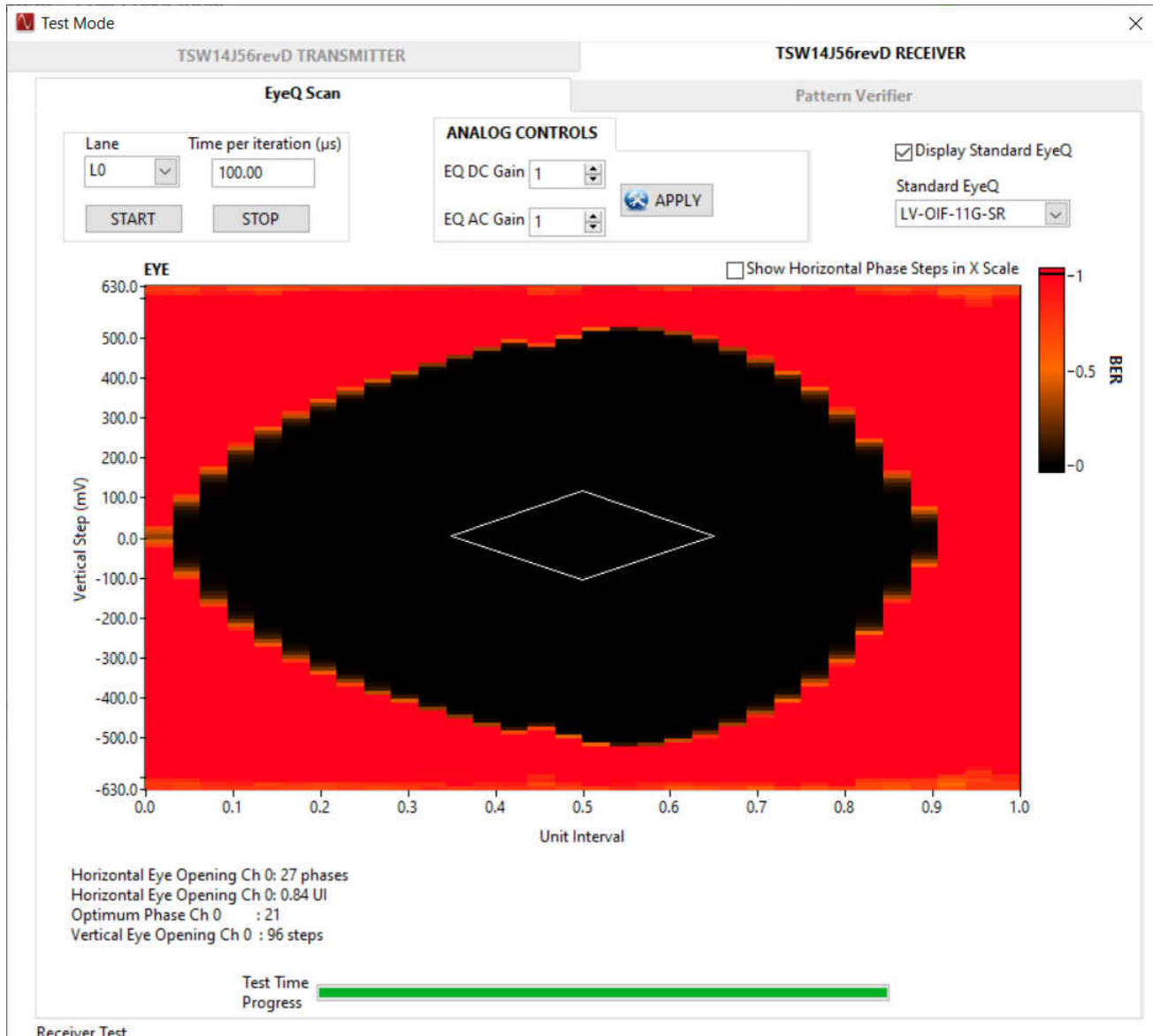
Figure 3-4. Example Eye Diagram Plot

3.1.2.2 IO Delay

The "IO Delay" Calibration process will sweep the IO Delay tap values across a lane and get the tap values where there are no bit errors. Selecting the IO Delay opens the window shown in Figure 3-5 below, using this one can calibrate the lane wise delay adjustments.
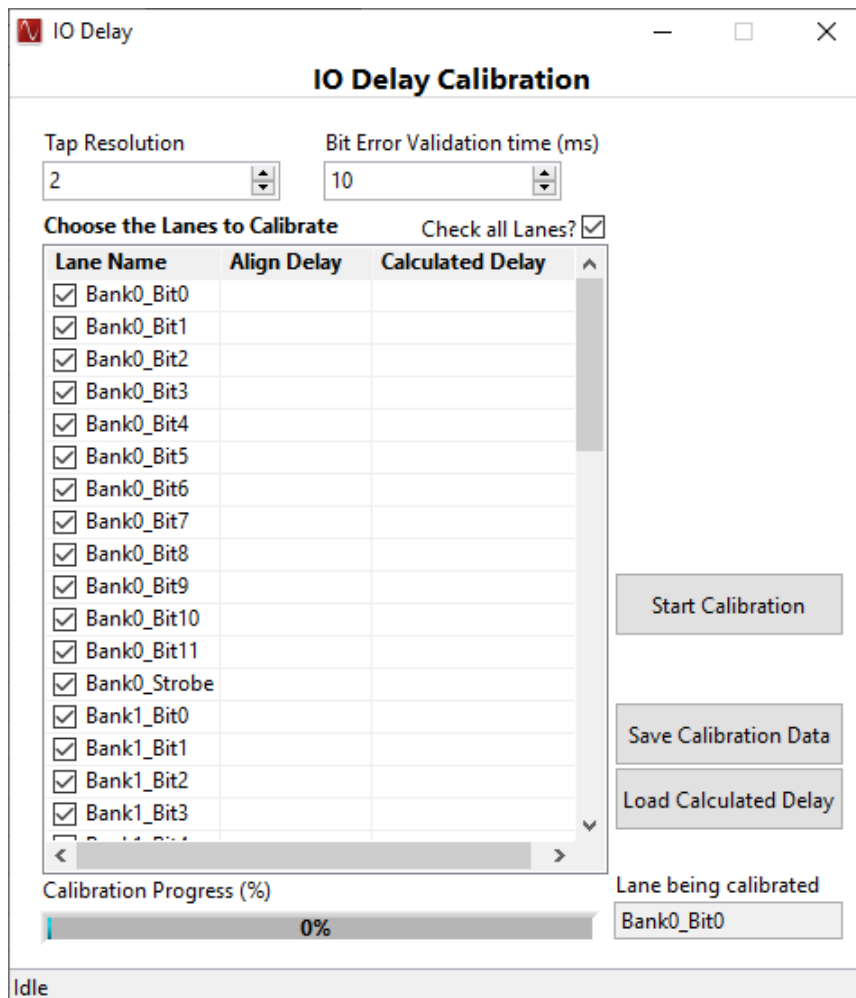
Figure 3-5. IO Delay Calibration

Calibration is done sequentially for the selected lanes, one after the other. The "Tap Resolution" denotes the minimum step size with which the tap values should be swept across IO Delay tap values. "Bit Error Validation time (ms)" specifies the time delay to wait before checking if the Error Bit is true/false while sweeping across the IO Delay tap vales. "Check all Lanes?" can be used to check/uncheck all the lanes. After selecting the required lanes to calibrate, click on the "Start Calibration Data" button, this will run the calibration on the selected lanes one after the other. Once calibration has been started ("Start Calibration" will then turn into "Stop Calibration"), it can be stopped anytime using "Stop Calibration" button. After the calibration completes, the calibrated data can be saved by clicking on "Save Calibration Data" and entering the target file location. Click on "Load Calculated Delay" and load the previously saved file with Calibration data, this action will derive the "Calculated Delay" for all the selected/calibrated lanes and the same calculated delay gets loaded to the FW. This completes the IO Delay Calibration. After the IO Delay Calibration steps are done, data capture can be done from HSDC Pro as usual.

Note: Currently the IO Delay option is supported only in the TSW14DL3200 EVM board. Do not close the IO Delay window when the calibration is running. If closed when the calibration is running, restart HSDC Pro. Before doing the calibration, ensure that the FW has been downloaded and no capture/calibration has been done after the FW download.

3.1.2.3 JESD204B Error Injection

The JESD204B Error Injection option (shown in Figure 3-6) is a debug feature that enables the user to inject errors like LOS events, disparity error and Not In Table error in the TX SERDES Lanes of the FPGA and verifying the same at the DAC devices.

User can turn off/on the TX SERDES Lanes Individually by unchecking/checking the "FPGA STX Lane # to (Device SRX Lane #)" check boxes. Whenever a TX lane powers down, a pulse (rising edge) of configurable width will be sent out of FPGA on SMA pin (TRIG OUTA). The width of the pulse can be configured with the "Trigger Pulse Width (ns)" input control.

Note: When a specific TX lane is powered down, in addition to LOS Event, the disparity error and Not In Table Error are set in that particular lane and the same can be observed in the DAC devices. This feature is currently available only in the DAC Mode of TSW14J57revE board.
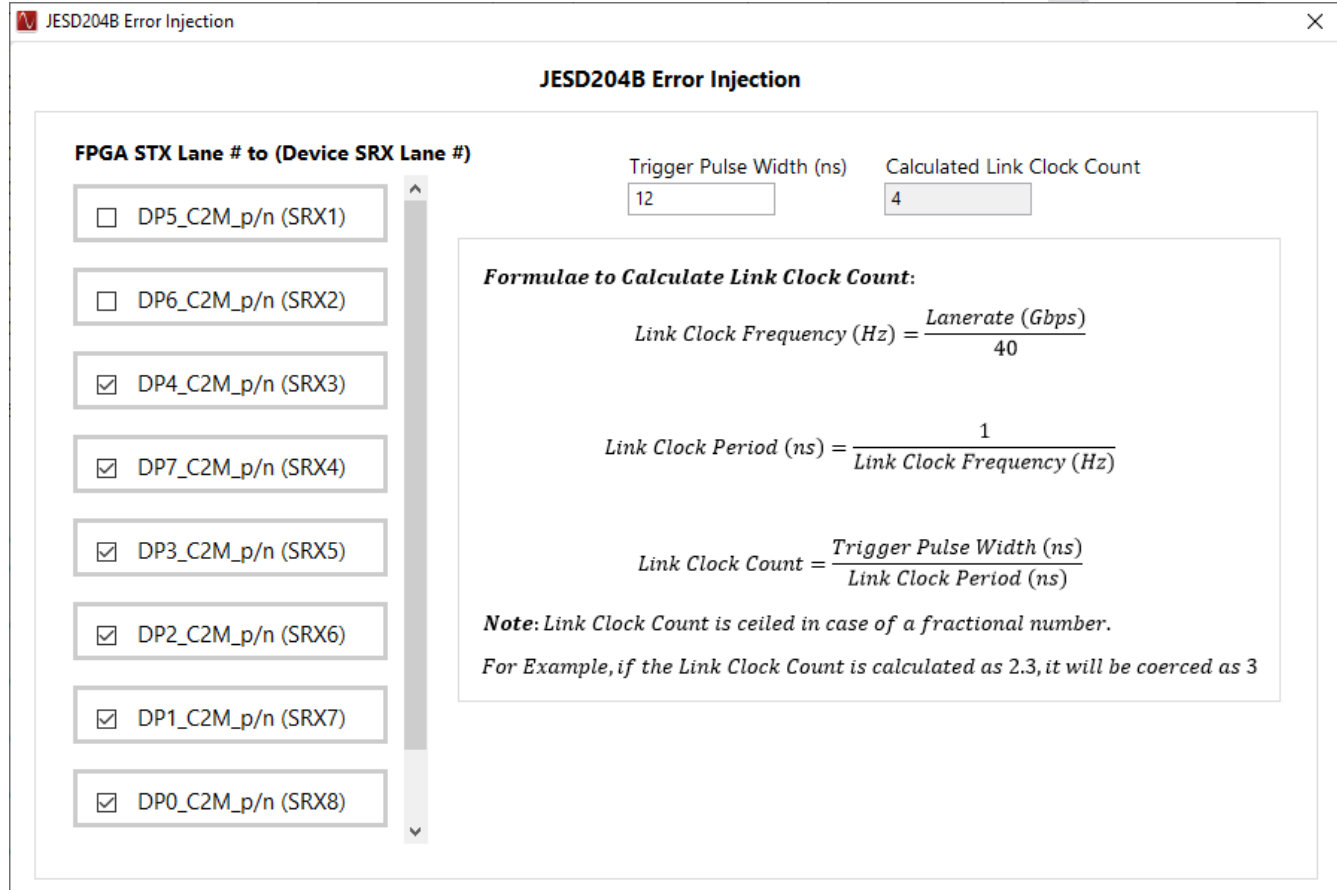
Figure 3-6. JESD204B Error Injection Window

3.1.2.4 FPGA Registers Write Read

The FPGA Registers Write Read menu option (shown in Figure 3-7) allows the user to write/read the registers of the FPGA Firmware. The firmware register map of the TSW14xxx board will be loaded and the Register Name, Register Address, R/W Mode, Register Values and Register Description will be shown. The register write operation can be done by selecting the required register element from the tree or by specifying the required register address in the "Address" input control and providing a value to be written at "Write Data" input control and then clicking on the "Write Register" button. Similarly, the register read operation can be done by clicking on the "Read Register" button after specifying the required register address and the read register value will be updated both in the register tree and "Read Data" output indicator. The current register configuration listed in the register map can be exported as ".cfg" file by using the "Save Config" button and the same can be loaded by using the "Load Config" button. The "Load Config" operation will overwrite the existing data in registers with the value specified in the loaded configuration file.
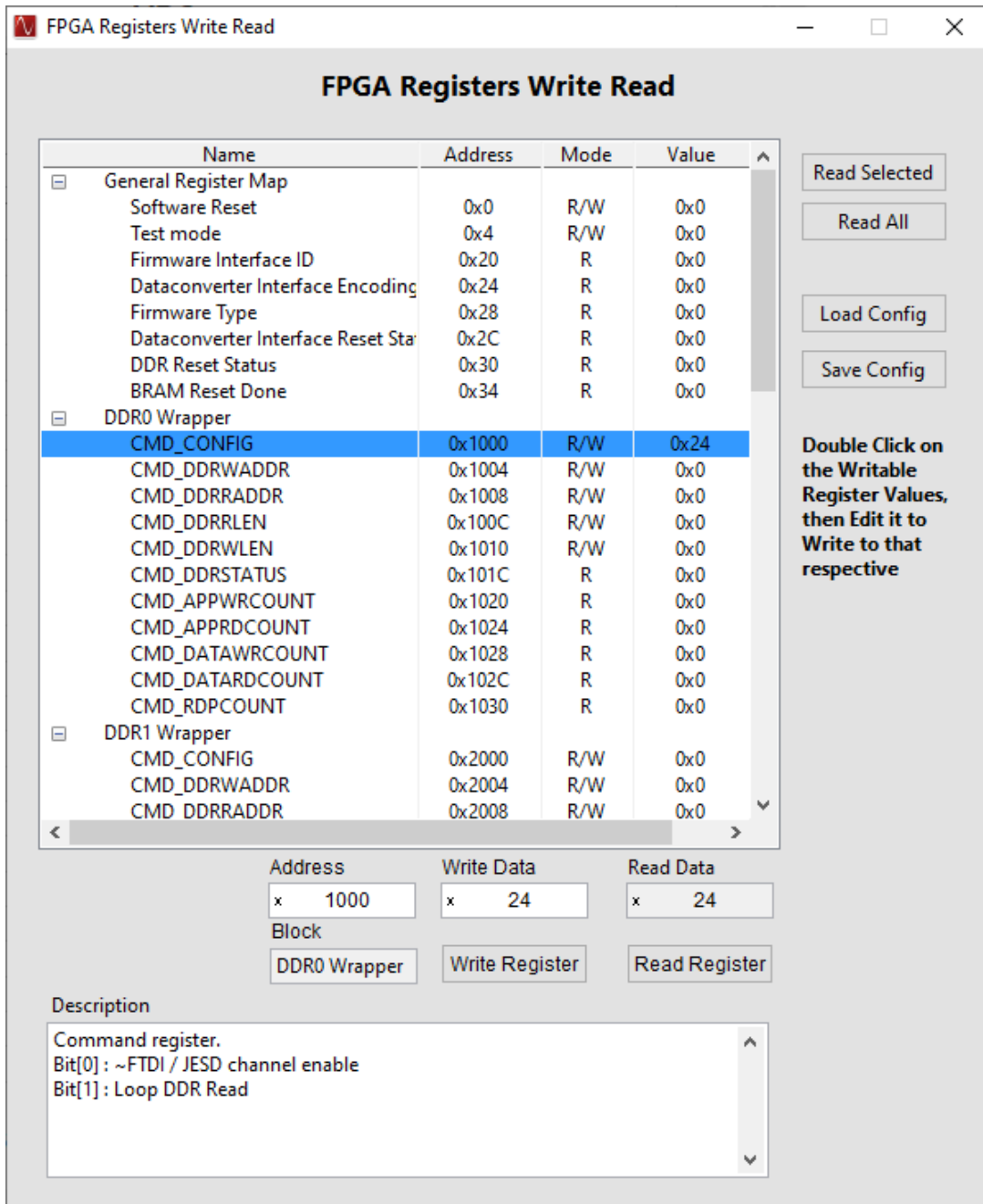
Figure 3-7. FPGA Registers Write Read Window

Note: This feature is currently implemented only for the TSW14J58EVM.

3.1.3 Data Capture Option

The *Data Capture Options* drop-down menu (ADC mode only) has three choices: (1) *Capture Option* (2) *Number of Channels* and (3) *Trigger Option*.

3.1.3.1 Capture Option

Selecting the *Capture Option* opens the window shown in Figure 3-8. From this menu, one can capture continuously by checking the appropriate box – allowing the monitoring of continuous captures over time.
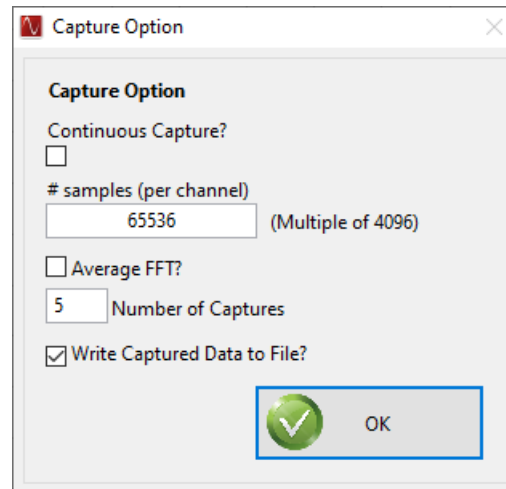
Figure 3-8. Capture Option

The *Capture Option* allows the flexibility to set the *# samples (per channel)* to be captured. This value is limited by the memory available on the TSW EVM. For example, if using the TSW1400, which has 1GB of RAM, with a 4-channel ADC, the value that would utilize all memory, and, therefore, the maximum value, would be:

(1048576 Mbytes) × (1 sample / 2 bytes) × (1/4 ADC channels) = 131072 Msamples / channel

The TSW14J56 has 1GB (8Gb) of RAM which allows up to 536,870,912 16-bit samples divided by the number of channels. Similarly, the TSW14J57 has 2GB (16Gb) of RAM which allows up to 1,073,741,824 16-bit samples divided by the number of channels. The sample amounts for the TSW14J56 and TSW14J57 are calculated under the assumption that no tail bits are present in the data frames.

The GUI default value for both boards is 65,536.

The GUI automatically rounds down to the nearest multiple of the displayed value on the right of the "# samples (per channel)" control field and updates the entered value. This value determines the number of samples that will be captured and saved to binary or CSV file. This value does not affect the record length used to generate the FFT plot. The record length used by the FFT plot is determined by the value of *Analysis Window (samples)* in the fixed left front panel of HSDCpro and can be set from 4096 to 524,288 samples when using the TSW14xxx.

The processed FFT data can be averaged over N captures by checking the box *Average FFT?* and setting the value N into the *Number of Captures* box. The average FFT uses the root mean square method so as to minimize PC memory usage. This value is limited to 1024 averages. If *Average FFT?* is enabled at the same time that *Continuous Capture?* is enabled, then the displayed FFT is a rolling average of the last N captures.

When the "Write captured data to a file" option is checked:

- For TSW14J5x data capture boards, data for each channel is stored in a separate file at the location: C:\Users\Public\Documents\Texas Instruments\High Speed Data Converter Pro\HSDCPro Data

- For TSW14xx data capture boards, all of the channel data is stored in a single file using an interleaved format at the location: C:\Users\Public\Documents\Texas Instruments\High Speed Data Converter Pro\ADC Temp.bin

3.1.3.2 Number of Channels

The *Number of Channels* option allows the user to specify the number of channels to be captured regardless of the number of channels the DUT has. This allows user to utilize the full memory capacity for a single channel if desired. This feature is presently only supported on the TSW1405 capture card where memory is 128KB (KBytes).
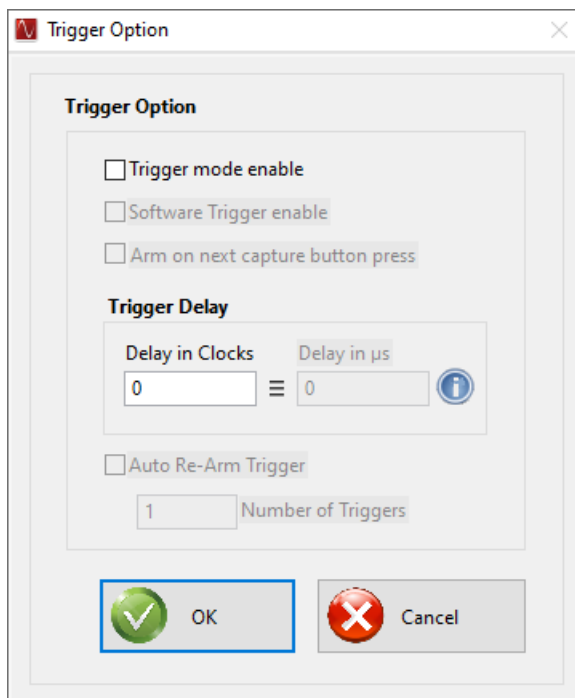
3.1.3.3 Trigger Option

Clicking on the Trigger Option will open a new panel as shown in Figure 3-9. This option is not available for the TSW1405/06. The GUI provides four options of capturing data using a trigger function. Selecting *Trigger mode enable* will arm the TSW14xxx to accept an external trigger.

Figure 3-9. Trigger Option

With both enables selected, the capture button on the main panel of the GUI will now change from "Capture" to "Generate Trigger". When the user clicks on this button, the GUI will send a CMOS logic level (1.8 VDC) active high pulse to the four SMA connectors labeled SYNC1, SYNC2, SYNC3, and SYNC4 on the TSW1400. On the TSW14J5x, these are labeled as TRIG_OUT_A, TRIG_OUT_B, and TRIG_OUT_C. This signal can be used to trigger other TSW14xxx EVMs or the same TSW14xxx. To use this rising edge to trigger the same TSW14xxx, the user must connect a cable from the SMA labeled as "EXT_TRG_INPUT" SMA (J11) on the TSW1400 ("TRIG_IN", SMA J13 on the TSW14J5x) to one of the SYNC (TRG_OUT) SMA's. Without this connection, the GUI will never detect a trigger and will report "No trigger occurred" a short time after the user has clicked on the "Generate Trigger" button. Once a trigger is detected, the GUI will do a capture.

Another trigger option is to use an external trigger source. To use this mode, only select "Trigger mode enable". When this mode is selected, the status button located at the bottom of the main GUI screen will display "TRIGGER ARMED" in yellow and the capture button will display "Read DDR Memory". The software is now waiting for a CMOS logic low to high transition to occur on the "EXT_TRG_INPUT" (TRG_IN) input SMA. Once this occurs, a data capture will occur. The user will now click on the "Read DDR Memory" button to display the captured data. If the user clicks on this button before a trigger occurred, a short time later a "No trigger occurred" message appears. If the external trigger is a continuous event, the GUI will not do a new capture until the user clicks on "Read DDR Memory". This causes the software to display the results from the first trigger event and reload the memory with new data on the next rising edge of the external trigger input.
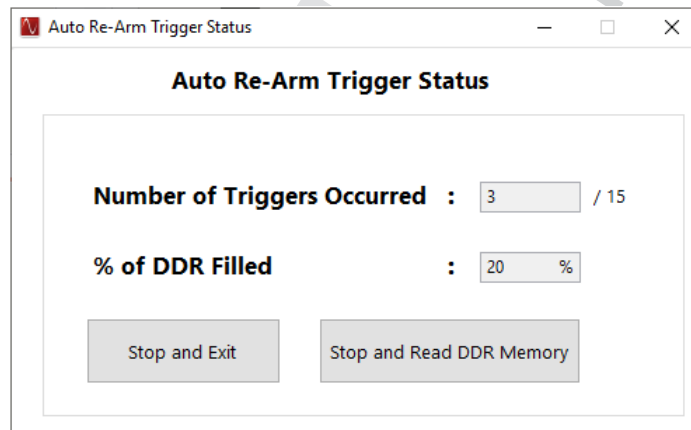
Another trigger option invloves selecting both "Trigger mode enable" and "Arm on next capture button press". With these two selected, the software will do a capture on the next rising edge detected on EXT_TRG_INPUT/

TRIG_IN connectors only after the user clicks on the "capture" button. This mode comes in handy if there are multiple trigger pulses arriving but the user does not want to trigger until a certain time later. If a trigger is not detected within about 12 seconds after clicking on capture, the software will time out and report no trigger detected.

When using the trigger capture mode, the user has an option to capture data a fixed amount of samples after the capture has actually started. This is useful for devices that have a "High Resolution Burst mode", where it takes several clock cycles to occur before valid samples are available. This delay is determined by the value entered in the "Trigger CLK Delays" box. The default value is "0". The user can enter a value from 0–7 with the corresponding sample delay shown in Table 3-1. Note that the delay is also based on the number of channels captured. For example, if a user selects a Trigger Delay of "2" and is capturing data from 2 Channels, after a trigger is detected by the GUI, the data capture starts. With this delay setting though, the first data sample used by the GUI will be the 81th sample from the ADC after the trigger occurred.

Another trigger option involves selecting both "Trigger mode enable" and "Auto Re-Arm Trigger". With these two selected the TSW14xxx EVM will capture the configured amount of samples ("# of samples per channel", from the Capture Option) for every trigger pulse (CMOS logic low to high transition that occurs on the "EXT_TRG_INPUT" (TRIG_IN, TSW14J5x) SMA.) and accumulate the captured samples in the DDR memory until the defined numbers of "Number of Triggers" gets completed.

When using this capture mode, the status button located at the bottom of the main GUI screen will display "TRIGGER ARMED" in yellow and the capture button will display "Show Trigger Status". Clicking on the "Show Trigger Status" button will open up a popup window displaying the status of the trigger operations with "Number of Triggers Occurred" and "% of DDR Filled". Clicking on the "Stop and Exit" button will stop the current capture operations without reading the captured sample. Clicking on the "Stop and Read the DDR Memory" button will stop the current capture operations and read the captured samples from the DDR. After the configured Number of Triggers occurs and required amount of DDR gets filled, the "Stop and Read the DDR Memory" button will display "Read DDR Memory" and clicking on the same will read the captured samples from the DDR.

Figure 3-10. Auto Re-Arm Trigger Status Window

For DAC mode, with both enables selected, the send button on the main panel of the GUI now changes from "Send" to "Generate Trigger". When this button is clicked, the GUI sends a CMOS logic high level (3 VDC) to the four SYNC SMA's on the TSW1400 and the three TRIG_OUT SMA's on the TSW14J5x. This signal can trigger other TSW14xxx EVMs or the same TSW14xxx. A cable must be connected from the "EXT_TRG_INPUT" (TRIG_IN, TSW14J5x) SMA to one of the SYNC (TRIG_OUT, TSW14J5x) SMA's to use this rising edge to trigger the same TSW14xxx. Without this connection, the GUI will never send the data from the memory.

Table 3-1. Trigger Delay Options

Trigger Delay	Number of Samples Skipped Per Channel			
	1 Channel	2 Channel	4 Channel	8 Channel
1	80	40	20	10
2	160	80	40	20
3	240	120	60	30

Table 3-1. Trigger Delay Options (continued)

Trigger Delay	Number of Samples Skipped Per Channel			
	1 Channel	2 Channel	4 Channel	8 Channel
4	320	160	80	40
5	400	200	100	50
6	480	240	120	60
7	560	280	140	70

Another trigger option involves selecting both "Trigger mode enable" and "Auto Re-Arm Trigger". With these two selected the TSW14xxx EVM will capture the configured amount of samples ("# of samples per channel", from the Capture Option) for every trigger pulse (CMOS logic low to high transition that occurs on the "EXT_TRG_INPUT" (TRIG_IN, TSW14J5x) SMA.) and accumulate the captured samples in the DDR memory until the defined numbers of "Number of Triggers" gets completed.

When using this capture mode, the status button located at the bottom of the main GUI screen will display "TRIGGER ARMED" in yellow and the capture button will display "Show Trigger Status". Clicking on the "Show Trigger Status" button will open up a popup window displaying the status of the trigger operations with "Number of Triggers Occurred" and "% of DDR Filled". Clicking on the "Stop and Exit" button will stop the current capture operations without reading the captured sample. Clicking on the "Stop and Read the DDR Memory" button will stop the current capture operations and read the captured samples from the DDR. After the configured Number of Triggers occurs and required amount of DDR gets filled, the "Stop and Read the DDR Memory" button will display "Read DDR Memory" and clicking on the same will read the captured samples from the DDR.

For DAC Auto Re-Arm Trigger mode, whenever the board receives a trigger signal at "EXT_TRG_INPUT" (TRIG_IN, TSW14J5x) SMA, the samples from the start index will be sent out to the DAC from the FPGA.

3.1.3.4 Using Multiple TSW14xxx and ADC EVM's for Simultaneous Capture using Trigger Option

Multiple TSW14xxx EVMs can connect to a single PC. To access up to four individual TSW14xxx EVMs with the HSDC Pro software, use the disconnect and connect function of the HSDC Pro GUI.
- To disconnect: go to "Instrument Options > Disconnect from the Board"
- To connect: go to "Instrument Options > connect to the Board"

Before setting the trigger option, determine which EVM is the master and which is the slave. In the example shown in Figure 3-11, one board has serial number "T8051Dcu and the other is T80529Un. Use this info and the cabling setup for selecting which be is the slave board and which is the master board.
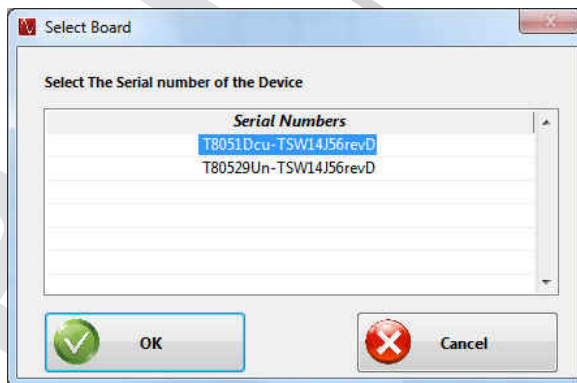
Figure 3-11. Two TSW14J56 EVM's Connected to one PC

3.1.3.4.1 Hardware Setup

- Connect a cable from the Master TSW14xxx SYNC/TRIG_OUT SMA to the Master TSW14xxx EXT_TRIG_INPUT/TRIG_IN SMA. This allows the Master TSW14xxx to register its own trigger output.
- Connect another cable from an unused SYNC/TRIG_OUT SMA on the Master to the SLAVE EXT_TRIG_INPUT SMA. This allows the slave TSW14xxx to receive the trigger signal from the Master.

Note

All SYNC/TRIG_OUT SMA's contain the same signal. The order does not matter. The cables of each trigger signal should have equal length to ensure the trigger signal arrives at the same time for all boards.

3.1.3.4.2 Setting up the Slave Board

With the HSDCPro GUI, establish connection to the slave TSW14xxx. Select the device, sample rate, and set up the slave TSW14xxx to accept a trigger signal, go to "Data Capture Options > Trigger Option".

Setup the trigger option as shown in Figure 3-12. This step arms the TSW14xxx slave board to detect trigger signal.
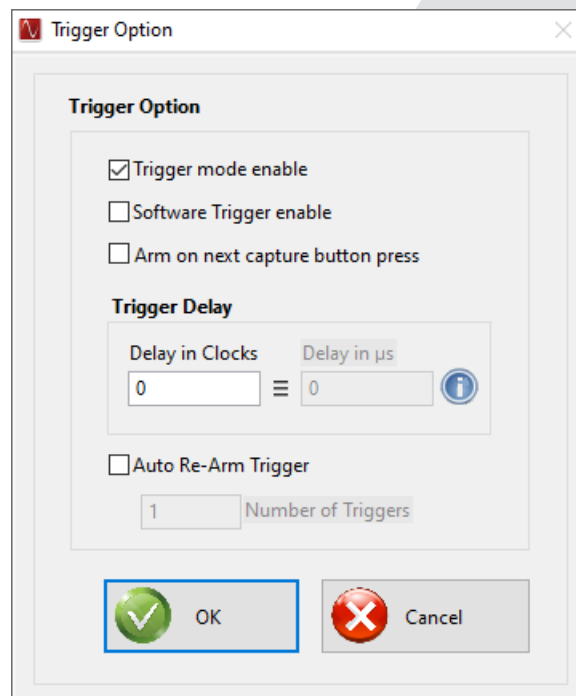
Figure 3-12. Slave Trigger Setup

The capture button will now change to "Read DDR Memory" and the message "Trigger Armed" will appear in the bottom of the GUI display. Disconnect the TSW14xxx slave board from the HSDC Pro GUI. To disconnect, go to "Instrument Options > Disconnect from the Board".

3.1.3.4.3 Setting up the Master Board

Connect the GUI to the master TSW14xxx board. Select the device, set the sample rate, then go to "data capture options > trigger option".

Set up the trigger option as shown in Figure 3-13. The software trigger sends out a trigger signal upon a software GUI button press. This also arms the TSW14xxx master board to register its own trigger signal. To capture data using the "Software Trigger enable" option, click on the "Generate Trigger" button on the main panel of the GUI. This will send out a pulse on the SYNC/TRIG_OUT outputs. This signal, which is now connected to the EXT_TRG_INPUT/TRIG_IN of both boards, starts a capture once detected by the FPGA of each board.
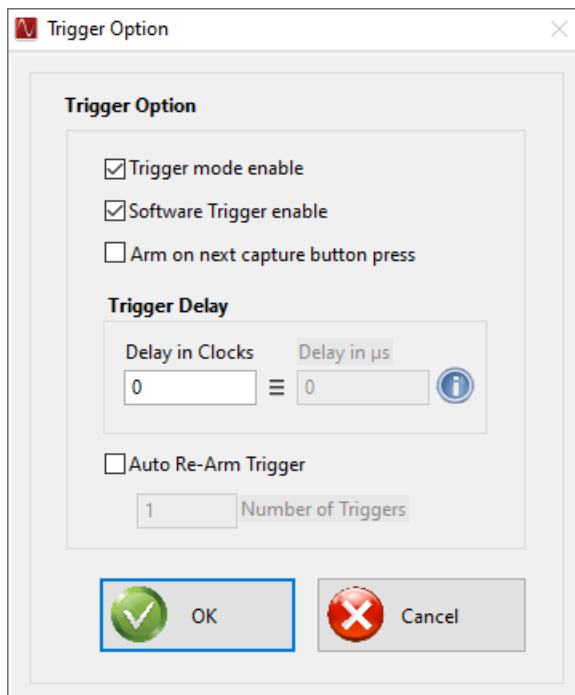
Figure 3-13. Master Trigger Setup

3.1.3.4.4 Read Captured Memory from the Slave Board

Disconnect the HSDC Pro from master board, and connect the software to slave. The user must select the device under test on the slave board again as the GUI does not keep track when using multiple boards.

Once the device is selected from the drag down menu, the message in Figure 3-14 will occur. Click OK to continue.
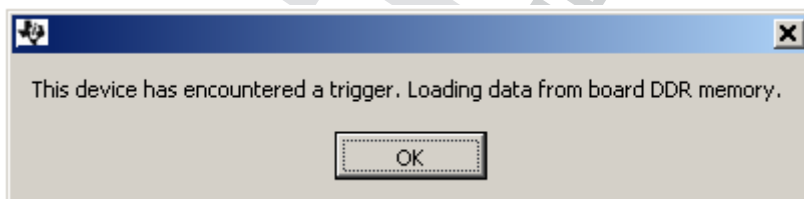
Figure 3-14. Trigger Confirmation Window

In the GUI main panel, enter the sampling rate to ensure correct FFT processing. Once this value is entered, the captured data from the trigger event is displayed.

For the TSW14J5x, there is an advanced option available for Master/Slave triggering that is synchronized with the SYSREF signal used by the JESD204B interface. This mode enables a Master/Slave triggering synchronized with SYSREF rising edges. In master mode, a hardware output trigger is generated on the TRIG_OUT_A/B/C SMA's at the first rising edge of SYSREF that occurs after the user presses the 'Capture' button. The data will then be captured at the next rising edge of SYSREF.

In the case of slave triggering mode, the capture occurs at the first SYSREF rising edge following the trigger input rising edge on the TRIG_IN SMA input. This way both Master and Slave will start capturing data at the same SYSREF edge in a Synchronized manner.

Software Changes Required: (The following steps are applicable for both ADC and DAC)

To put the TSW14J5x boards in Sysref-Based Master Slave Triggering mode, add the following INI parameter just below the [Version 1.0] entry in the corresponding master and slave device INI files, as shown in Figure 3-15.

• Sysref Based Master Slave Trigger = 1

```
DLL Version=1.0
Read EVM Setup Procedure="EVM Setup Procedure not available"
\\use <> as delimiter for newline


[Version 1.0]

Sysref Based Master Slave Trigger = 1

JESD IP Core_CS=0
JESD IP Core_F=2
JESD IP Core_HD=0
JESD IP Core_K=16
JESD IP Core_L=8
JESD IP Core_M=2
JESD IP Core_N=16
JESD IP Core_NTotal=16
JESD IP Core_S=4
JESD IP Core_SCR=0
JESD IP Core_Tailbits=2
JESD IP Core_LaneSync=1
JESD IP Core_Subclass=1
```

Figure 3-15. Sysref-Based Master Slave Triggering INI Setting

In the HSDC Pro GUI, select the **Trigger Option** menu under Data Capture Options.

For the master board, select **Trigger mode enable** and **Arm on next capture button press**.

For the slave board, select **Trigger mode enable** in the Trigger Option window.

HSDC Pro GUI is now configured for SYSREF-Based Master Slave Triggering. Go back to the master board and the software will do a capture on the next rising edge detected on EXT_TRG_INPUT/TRIG_IN connectors after the user clicks on the "capture" button.

3.1.4 Test Options

The Test Options menu tab allows for setting the parameter options for the different frequency and time domain tests. These options include Notch frequency bins, Cursor Lock, 2 channel display, Analysis Window Markers, X-Scale in time, Y-Scale in Voltage, Other Frequency Options, NSD Marker, Phase Plot, Phase in Degree, and Histogram as shown in Figure 3-16.

Test Options | Device GUI Options
- Notch frequency bins
- Cursor Lock
- 2 Channel Display
- Analysis Window Markers
- X-Scale in time
- Y-Scale in Voltage
- Other Frequency Options
- ✓ NSD Marker
- Phase Plot
- Phase in Degree
- Histogram
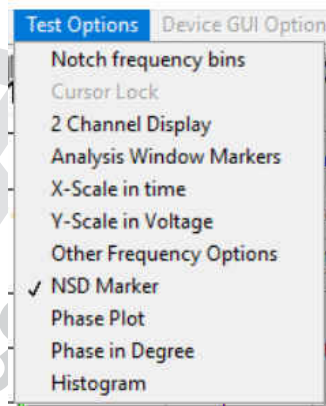
Figure 3-16. Test Options

3.1.4.1 Notch Frequency Bins

The Notch Frequency Bins option allows the user to remove a number of bins from the SNR calculation of the input frequency around the fundamental, DC and a predetermined number of harmonics. The default values for these settings when capturing data using Blackman window mode is 25, 0, 25, and 5, as shown in Figure 3-17. When the capture mode is set to Rectangular mode, the default values are 0, 0, 1, 5.

Figure 3-17. Notch Frequency Bin Removal

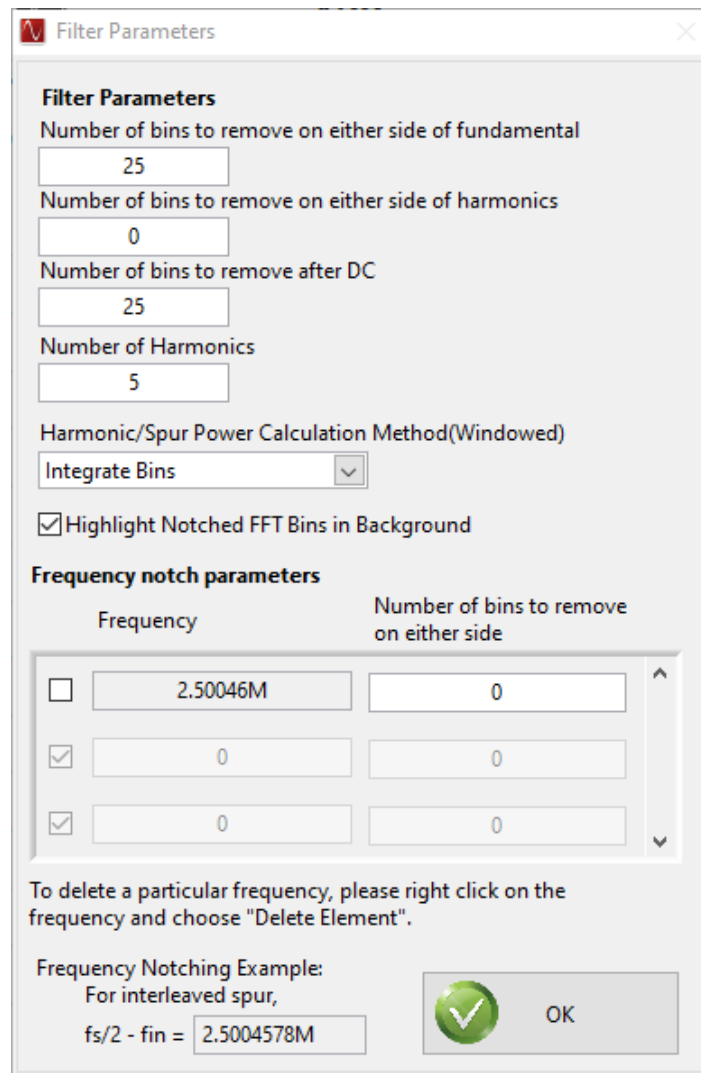By default, the noise calculations for SNR and SINAD are based on the FFT of the captured data with the Notch Filter parameters applied. The first FFT bin at DC is not used because the first bin contains DC offset and thus does not effect AC parameters or AC performance. The rest of the FFT bins out to the Nyquist frequency are included in the calculation of the total noise.

The Harmonic/Spur Power Calculation Method(Windowed) button allows the user to either Integrate the Bins or Don't Integrate the bins. When "Integrate Bins" is selected, the neighboring bins are also included in the harmonic and spur calculations. Apart from the harmonic frequency bin, its neighboring bins will also be used for harmonic power calculation.

When "Don't Integrate" is selected, the neighboring bins are not included in the harmonic and spur calculations. Only the single harmonic frequency bin will be used for the harmonic power calculation.

This option will also affect the FFT filtering. In "Integrate" mode, neighboring bins of the harmonics will not be notched.

There is also an option to notch out bins around a user defined frequency. The default sets the number of bins to 0. If the clock input is mixing with the input signal, there may be a spur at fs/2 - fin, where fs is the ADC sample frequency and fin is the input frequency. This option could be used to notch this spur from the results if desired. Select the top entry to enable notching for this frequency. Select the other boxes below this one to notch out bins around user defined frequencies. If the user enters a "1" for number of bins to be removed, 1 bin will be removed at the frequency entered and one bin will be removed from each side of this frequency. If the user enters a "2", the bin at the frequency will be removed along with 2 bins on each side of the frequency, and so on. The GUI

calculates the fs/2-fin frequency for informational use only in the equation box. The default value is "0" since the default value of both fs/2 and fin is "0". This value is updated when the user enters the ADC sample rate and ADC Input target frequency in the main GUI panel.

The "Highlight Notched FFT Bins in Background" option is used to highlight the area of notched frequency bins in the FFT display window.

3.1.4.2 2 Channel Display and Cursor Lock

If the 2 channel display option is selected, a second data capture display window will open (Figure 3-18). The user can now use this window to display the same channel but a different parameter, or a different channel if a multi-channel ADC is under test. To remove the second channel display and go back to a single channel display, click on this option again to remove the selected check mark.
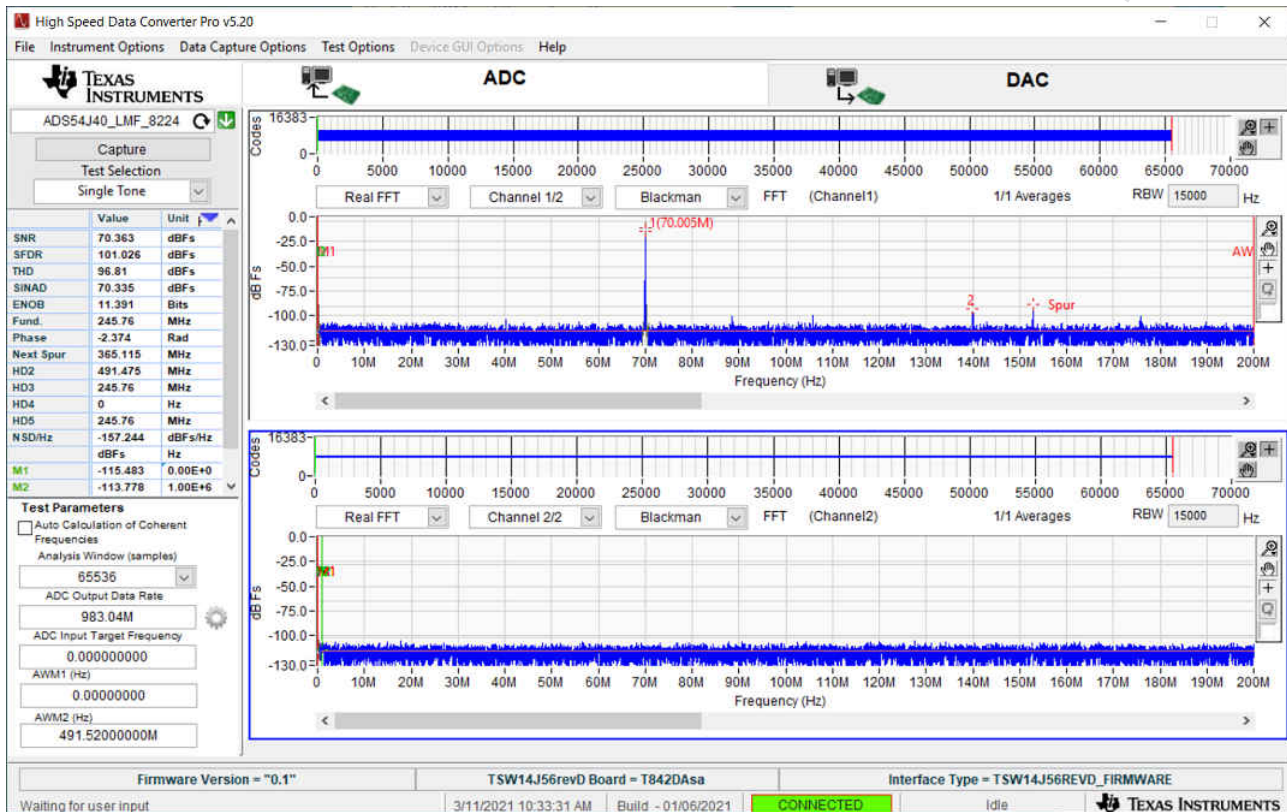

Figure 3-18. Two Channel Display

When 2 channels are displayed, if Cursor lock is enabled, the cursors in the lower display is locked to the ones in the upper display.
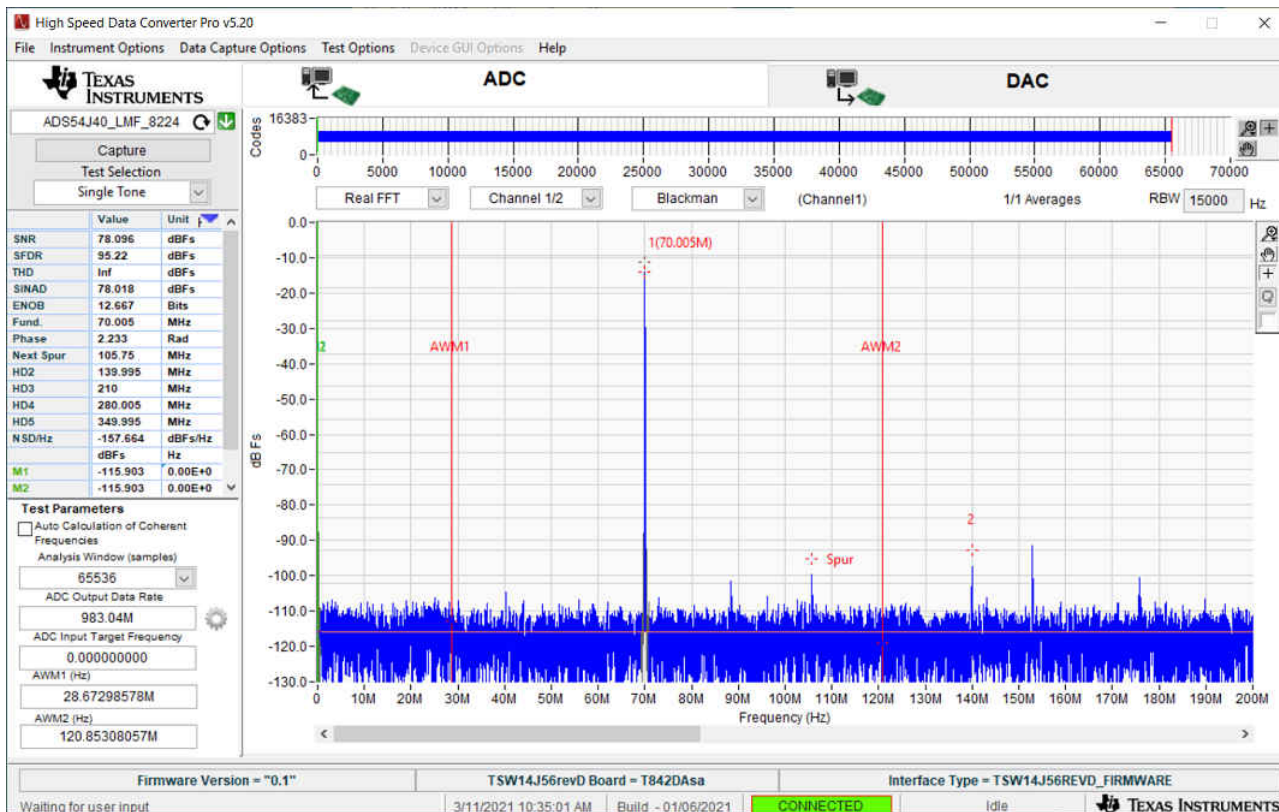
3.1.4.3 Analysis Window Markers

Figure 3-19. Analysis Window Marker Example

When this option is selected, two new markers labeled AWM1 and AWM2 will appear on the FFT plot when using the GUI in Single Tone mode only. All of the calculated AC performance statistics in the left column will only use the captured values between these window markers for the calculations. The default location of marker AWM1 is at 0 MHz and marker AWM2 is at ½ the ADC sample rate (Nyquist). The location of these markers can be set either by entering a frequency value (in Hertz) in the AWM1 and AWM2 location boxes located in the bottom left corner of the GUI or by clicking on the markers directly and dragging them with the computer mouse. The AC parameters update immediately after the markers have been moved. Figure 3-19 shows an example of the Analysis Window Markers being used to display AC parameters inside a 90-MHz analysis window centered around a 70-MHz tone inside the FFT.

3.1.4.4 X-Scale in Time

When using the Time Domain option, the user can change the X-scale of the display from samples to time (μs).

3.1.4.5 Y-Scale in Voltage

When using the Time Domain option (Test Selection in 'Time Domain'), the user can change the Y-scale of the top graphical display of the GUI from Codes to Voltage. The default setting is Codes.

3.1.4.6 Other Frequency Options

The *Other Frequency Options* menu has 3 features - *Peak Analysis*, *Disable Fundamental Frequency Search*, and *Disable Harmonic Frequency Search*, as shown in Figure 3-20.
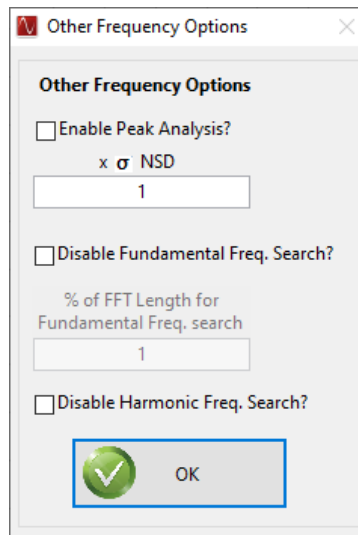
Figure 3-20. Other Frequency Options Menu

Peak Analysis

When Peak Analysis is enabled, it finds the other peaks above the average noise floor (those other than fundamental, harmonics, and next spur) and marks them from "A" to "Z", based on the amplitude of the peaks. The threshold is set as n number of standard deviations above the noise floor and will be shown as a horizontal line in the graph when enabled.

Disable Fundamental Frequency Search

When Disable Fundamental Frequency Search is enabled, the GUI takes the user-provided *Input Target Frequency* as the location of the fundamental (and will not search the entire FFT for the fundamental). This option is typically used if there is a spur or harmonic frequency whose amplitude is greater than the actual signal frequency's amplitude. By default, this selection is inactive, and the software searches the spectrum for the largest signal as the fundamental frequency.

Disable Harmonic Frequency Search

When Disable Harmonic Frequency Search is enabled, the GUI will no longer search the entire FFT for harmonics. By default, this selection is inactive, and the software searches the spectrum to find four harmonics (HD2 - HD5).

3.1.4.7 NSD Marker

When this option is selected, a horizontal marker (in red) representing the *Noise Spectral Density* will appear on the FFT plot when using the GUI in Single Tone mode only. Refer to Appendix A.8 for additional details.

3.1.4.8 Phase Plot

When this option is selected, the GUI will plot phase of the captured signal (in radian) on the FFT window.

3.1.4.9 Phase in Degree

Enabling this option will display phase in degrees. Disabling this option will revert phase display to radians.

3.1.4.10 Histogram

Clicking on this feature will open a new window that displays a histogram of codes from the data in HSDC Pro, as shown in Figure 3-21.
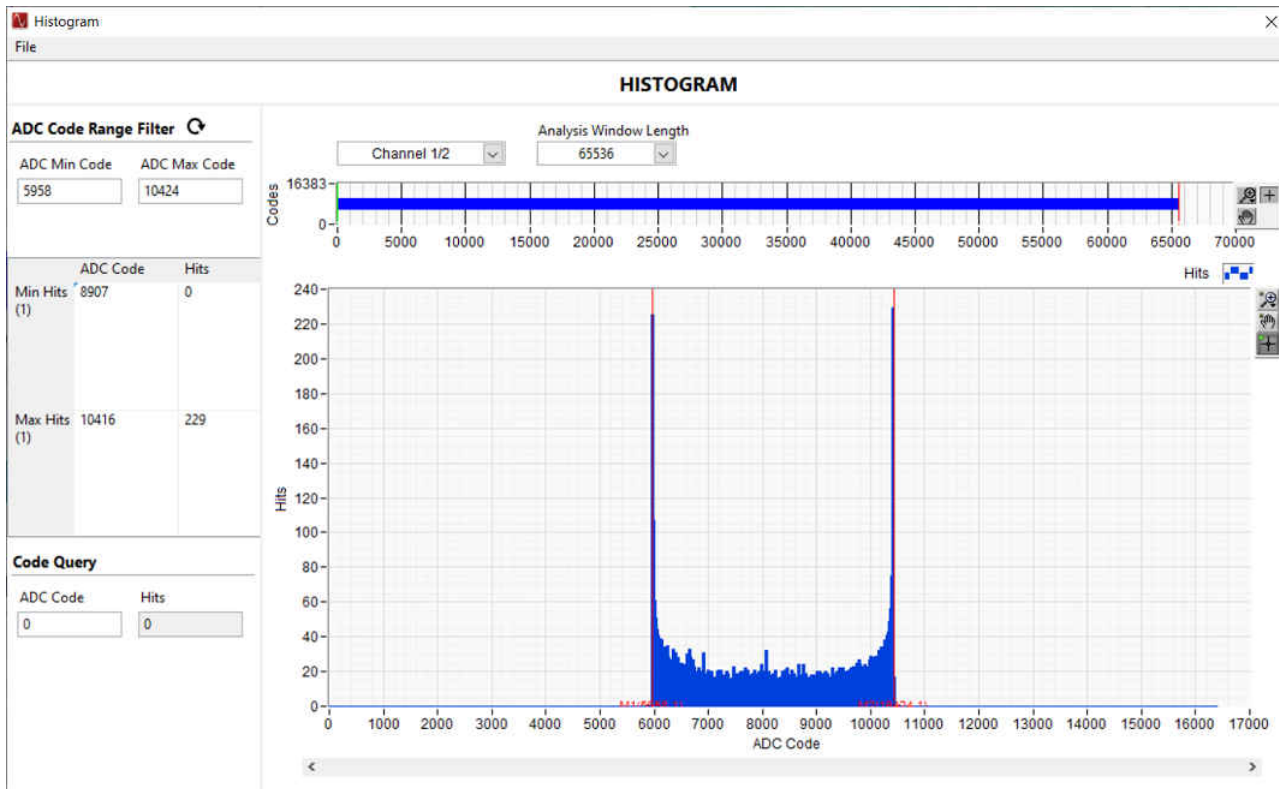
Figure 3-21. Code Histogram

The analysis window length should match the number of samples from the data capture, in order to get a histogram analysis for full capture data. In order to analyze the ADC Codes over a particular section of capture length, set the required "Analysis Window Length" appropriately and move the green cursor over the length of the context plot graph to include the desired section of ADC capture data to be considered for Histogram analysis.

3.1.5 Help

Clicking on the help tab opens a window with five options. The first option, labeled "About", opens a status window displaying the current version of the GUI, the software DLL, the loaded firmware, and patch version.

The second option labeled "Debug Support", enables a debug email option. With this option enabled, if a GUI error occurs, the software prompts the user that it is emailing a debug log to a TI support team. For every subsequent error until the user disables this feature, the GUI will silently send the log file. The third option, labeled "Check for Updates", will verify if the user's GUI is the latest version available on the TI website.

The fourth option, labeled "EVM GUI Help", opens a window displaying the contents of the User's Guide, allowing the user to search for topics regarding the operation of the GUI.

The fifth option, labeled "Version History", opens a window showing the revision history of the HSDC Pro GUI.

3.2 Status Windows

The HSDC Pro GUI reports system status such as downloading, capturing, warnings, errors, and informational output in several locations. In the lower right portion of the screen, when the GUI is loading the FPGA, loading data to memory, or performing a data capture, a rolling bar will appear in place of the IDLE message. A new window will also open in the middle of the screen describing what the GUI is currently doing. An example showing the status windows during a firmware load is shown in Figure 3-22.
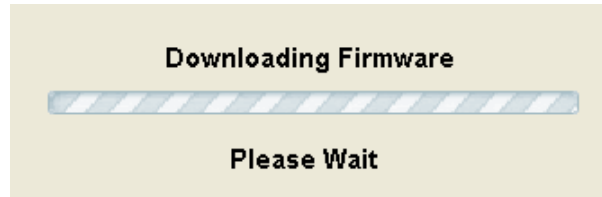
Figure 3-22. Status Window

During operation of the HSDC Pro GUI software, warnings may appear in the center status window if selections made from the drop-down menus of the interface are incompatible with the hardware selections or settings. For example, if a sample rate is entered that is faster than that supported by a particular ADC data sheet, a warning appears as shown in Figure 3-23.
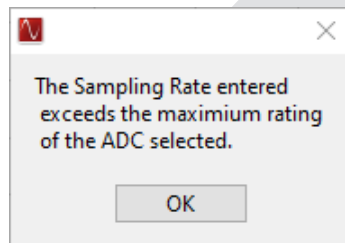
Figure 3-23. Center Status Window

3.3 Mode Selection

The first selection a user needs to make is to select the type of EVM that is to be tested with the TSW14xxx EVM. The user will click on either the "ADC" or "DAC" button located at the top of the GUI as shown in Figure 3-24.

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Figure 3-24. TSW1400 and TSW14J5x Modes

The mode selected will determine the main screen format. When ADC is selected, the GUI will be setup for displaying ADC data capture results. If DAC is selected, the GUI will setup controls to load a test pattern, create a test pattern, and display the graphical representation of the test pattern to be sent to a DAC EVM once the file has been read by the GUI.

3.4 Device Selection

After the board mode has been set, the user needs to select the device to be tested from the device selection drop-down menu. If the GUI is in ADC mode, clicking on the drop down arrow will display the ADC options available, as shown in Figure 3-25. If in DAC mode, the list will display available DAC's.
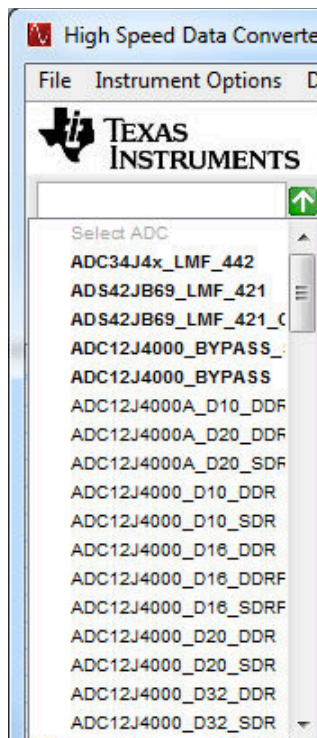
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Figure 3-25. ADC Device Selection Window

Each device that has an ini file installed in the proper directory automatically has an entry in the device selection drop-down menu.

3.5 Capture Button (ADC Mode Only)

The Capture button initiates a data capture once all other selections are made. The data capture can be a single capture and display, or a continuous repeating capture (Capture option under Data Capture Option tab in Tool Bar). When continuous capture is enabled, this button display will change from "Capture" to "Stop". Clicking on this button when in this mode will stop the continuous capture. After a captured has been issued, the GUI will store the setups currently used. If the GUI is closed and then re-opened, most of the settings will be restored if the original firmware is still present in the FPGA.

3.6 Test Selection (ADC Mode only)

The Test Selection drop-down has options for displaying data as a Time Domain, Single Tone, Two Tone, or Channel Power, as shown in Figure 3-26. The Single Tone FFT displays the power spectrum of the captured data with calculated AC performance statistics. Time Domain displays the raw captured data in the format of a logic analyzer display and output level over time. Two tone mode sets up cursors and displays results normally used with this type of testing. Channel Power will place cursors around the channels selected by the user (up to 5) and report the power of each.
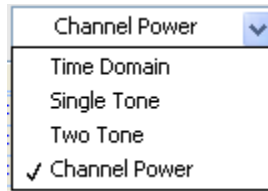
Figure 3-26. Test Selection Drop-Down Options

3.6.1 Single Tone FFT

The Single Tone FFT screen is shown in Figure 3-27. The larger central pane displays the FFT power spectrum, whereas the calculated statistics are grouped into categories on the left side of the screen. Settings and inputs relevant to the test are entered in drop-down menus or text input boxes on the bottom left portion of the window. .

The red horizontal line shown is the RMS line. This line indicates the RMS average of the noise floor of the FFT plot. The RMS average is computed over all of the FFT bins except the bin containing the input frequency. More precisely, the RMS line = SINAD + FFT Record Length Process Gain where FFT Record Process Gain = 10log(number of points/2).
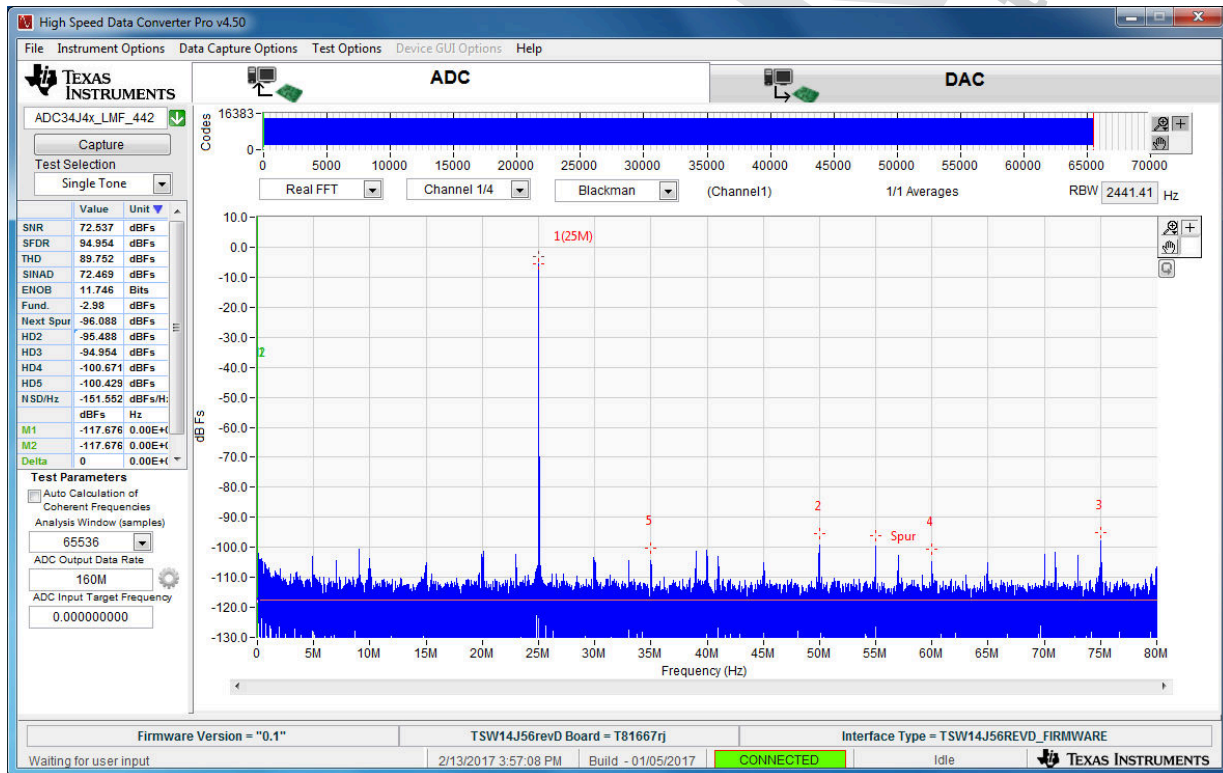
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Figure 3-27. Single Tone FFT Display

3.6.1.1 Parameter Controls

The output data rate is entered in the ADC Output Data Rate text box. In most cases this value will be the same as the sample rate of the ADC. For parts that support decimation, this value is usually lower. For example, this number is usually 2x lower if the part decimates by 2 and 4x lower if it decimates by 4. The number is entered in Hertz (Hz), although the letter M may be appended to represent the sampling rate in MHz. For example, 125M = 125 MHz or 125,000,000 Hz.

The expected input frequency is entered in the ADC Input Target Frequency text box. If the Auto Calculation of Coherent Input Frequency mode is enabled, then this input frequency is adjusted up or down slightly away from the input frequency automatically. If coherent input frequency is required, the signal generator used to source

the input frequency must be set to this exact calculated coherent frequency. The coherent frequency calculation takes the ADC sampling rate, the input frequency as entered by the user in Hertz, and the FFT record length and adjusts the input frequency so that the captured data starts and ends on the same place of the sine wave of the input frequency. This avoids an artifact of the FFT calculation from presenting a smeared power spectrum due to the fact that the FFT presumes the sample of the input is part of a continuous input signal. If the input and sampling frequency is not coherent, and the sampled data is appended end to end to form a continuous input signal, then there is an apparent phase discontinuity at the beginning and the end of the sampled data. Making the sampling and input frequencies coherent avoids this apparent discontinuity. If the input frequency cannot be made coherent, then the windowing functions other than Rectangular can be used to process out this effect to some degree.

The FFT record length can be set in the Analysis Window (samples) text box. The TSW1400 and TSW14J5x EVMs support FFT analysis lengths of as much as 524,288 samples, or as little as 1024 samples. In order to analyze the ADC Samples over a particular section of capture length, set the required "Analysis Window (samples)" appropriately and move the green cursor over the length of the context plot graph to include the desired section of ADC capture data to be considered for analysis. The red vertical line shown in the codes graph represents where the last sample is used from the captured data for analysis. The GUI will only allow record lengths that are the same size or smaller than the number of captured samples, which is set by the value in the capture option under the Data Capture Options tab (See Section 3.1.3.1). The default value is 65,536.
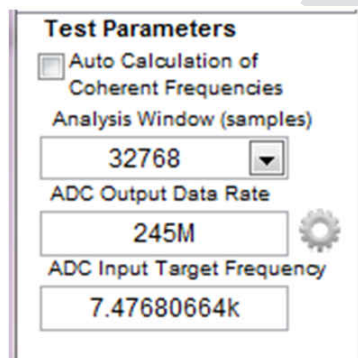

Figure 3-28. Test Parameters

Clicking on the *Settings* button (a gear) near the 'ADC Output Data Rate' will open a window as shown in Figure 3-29, which allows the user to specify the additional device parameters. Check "Enable" to enable this option.
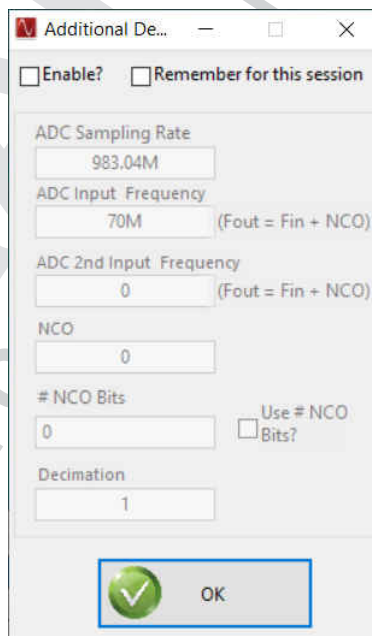

Figure 3-29. Additional Device Parameters

This additional setting is used to calculate the exact location of the spurs in the captured tone based on the following device parameters:

ADC Sampling Rate – Actual ADC sampling rate from the device. The ADC Output Data Rate value displayed in Figure 3-28 will be (Actual ADC Sampling Rate / Decimation).

ADC Input Target Frequency – Actual signal frequency on the device input.

ADC 2nd Input Target Frequency – Actual signal frequency on the second device input.

NCO – NCO frequency configured in the device that goes to the mixer. The NCO frequency provides a frequency shift of specified frequency value to the input tone. The spur search algorithm in HSDC Pro will account for this and identify the spurs properly.

# of NCO Bits – Number of NCO accuracy bits used in adjusting the user specified NCO frequency. To include the same amount in the calculation of NCO frequency, check on the "Use # NCO Bits?" The formula used to modify the User Specified NCO Frequency, based on the number NCO accuracy bits is given below. In order to use the # of NCO Bits, the "Auto Calc of Coherent Frequencies" should be enabled.

$$Calculated\ NCO\ Frequency = \textbf{ROUND}\left[2^{\#\ NCO\ Bits} * \left(\frac{User\ Specified\ NCO\ Frequency - \left(ADC\ Output\ Data\ Rate * \textbf{INT}\left(\frac{User\ Specified\ NCO\ Frequency}{ADC\ Output\ Data\ Rate}\right)\right)}{ADC\ Output\ Data\ Rate}\right)\right] * \left(\frac{ADC\ Output\ Data\ Rate}{2^{\#\ NCO\ Bits}}\right)$$

Decimation – Specifies the Decimation mode configured in the device.

Remember for this session – This will save the test parameter settings in case the board is disconnected or switched.

3.6.1.2 ADC Captured Data Display Pane

The ADC captured data is displayed in the major center portion of the GUI. The data display panel has four display control drop-downs. The data type drop-down allows the user to display the results as Codes, Bits, Real FFT or Complex FFT as shown in Figure 3-30.
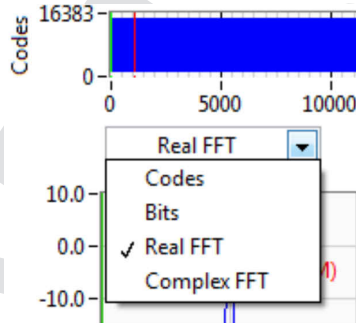
Figure 3-30. Data Display Options

The Codes option will display the data as actual digital codes. The Bit option will show the values of the individual ADC output bits and displayed as if it were captured by a logic analyzer.

The Channel drop-down selects which channel of a multi-channel ADC is to be displayed as shown in Figure 3-31.
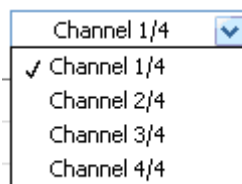
Figure 3-31. Channel Selection Window

When in the frequency domain mode, the GUI provides a windowing function to be applied to ADC captured data in the Window Display drop-down menu (Figure 3-32), Rectangular Window applies a unity gain to all data points of the captured data. A Hanning Window, Hamming Window, or Blackman-Harris Window function can be applied to the captured data for situations where the ADC output data rate and the input frequency are not or cannot be set precisely to capture an integer number of cycles of the input frequency (Coherent frequency).
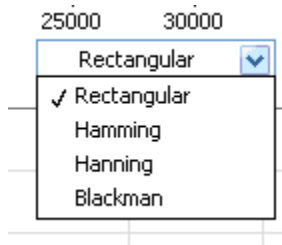

Figure 3-32. Data Windowing Options

3.6.1.3 FFT Power Spectrum

The FFT power spectrum of the captured data is displayed in the major center portion of the window. The HSDC Pro GUI software automatically scales the horizontal axis from DC through the Nyquist frequency, although the scale of the horizontal axis can be changed simply by highlighting the text and typing in a new value. For example, the display in Figure 3-27 can be used to zoom in on the input frequency by highlighting the 0 MHz at the end of the spectrum and typing 25M, and then highlighting a value at the other end and typing in 35M. This causes the portion of the power spectrum from 25 MHz through 35 MHz to fill the power spectrum display.

The vertical scale of the power spectrum is automatically scaled to display the noise floor of the FFT result up through 0 dBFS. The vertical scale can also be manually adjusted by highlighting the limits of the vertical scale and typing in new limits. By default, the first few harmonics of the input frequency are marked in the display, as well as 2 additional marker, M1 and M2, that can be placed by dragging the marker to any place in the power spectrum, such as a noise spur that is not already marked as a harmonic.

Display properties can be edited by using the mouse to right-click in the power spectrum display. Visible properties such as the graph palette or plot legend can be edited, and auto-scale of the vertical and horizontal axis's can be enabled or not. The data can also be exported to Excel or a clipboard for coping or processing.

3.6.1.4 Overlay Unwrap Waveform

When in the time domain mode, the Overlay Unwrap Waveform check box, located near the top left section of the captured display, allows a calculated normalized waveform to be overlaid (in orange) onto the sample data waveform (in blue). If the sample and input frequencies are coherent, the sampled data is normalized into a calculated representation of a single period of a sine wave. Errors in the sampled data for any reason become immediately apparent as spikes on the unwrapped waveform.

3.6.1.5 Single Tone FFT Statistics

For the Single FFT test, a number of calculated statistics and AC performance measurements are displayed to the left of the power spectrum display.

SNR - Signal-to-Noise Ratio is the ratio of the power of the fundamental (PS) or input frequency to the noise floor power (PN), excluding the power at DC and the first five harmonics. SNR is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

$$SNR = 10Log10(Ps/Pn) \tag{2}$$

SFDR - Spurious-Free Dynamic Range is ratio of the power of the fundamental to the highest other spectral component (either spur or harmonic). SFDR is typically given in units of dBc (dB to carrier).

THD - Total Harmonic Distortion is the ratio of the power of the fundamental (PS) to the power in the first five harmonics (PD). THD is typically given in data sheets in units of dBc (dB to carrier).

SINAD - Signal-to-Noise and Distortion is the ratio of the power of the fundamental (PS) to the power of all the other spectral components including noise (PN) and distortion (PD), but excluding DC.

SINAD = 10Log10(Ps/(Pn+Pd))   (3)

ENOB - Effective Number of Bits is a measure of a converter's performance as compared to the theoretical limit based on quantization noise.

ENOB = (SINAD+Fundamental Power-1.76)/6.02   (4)

Fund. – This parameter displays the power level of the fundamental.

Next Spur. - This parameter displays the power level of the next largest spur that is not an HD spur.
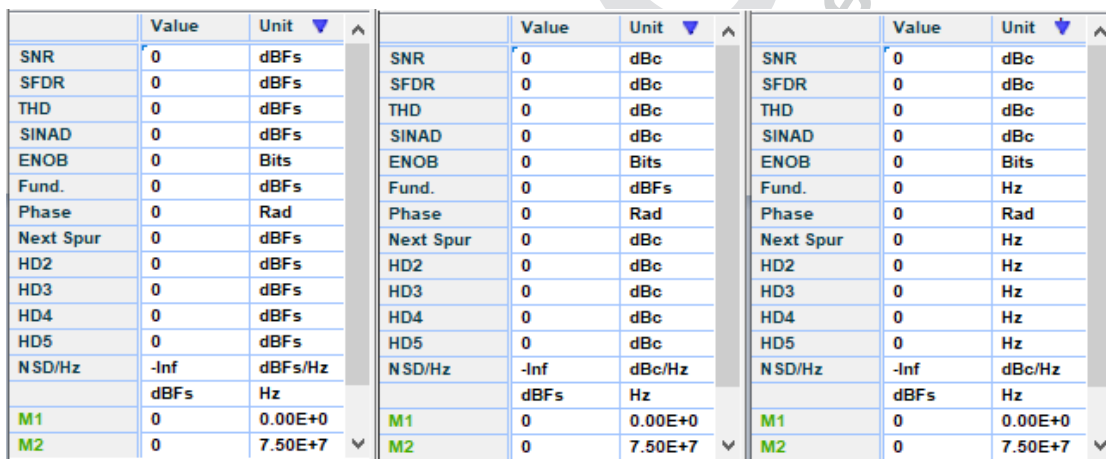
HD2-6 – Display the power values of the second through sixth harmonics of the input frequency in dBc.

NSD/Hz – The parameter displays the Noise Spectral Distortion in full scale/Hertz of bandwidth or dBFs/Hz.

M1, M2, Delta – Displays the power level of the location of markers M1 and M2. These markers can be moved around on the spectrum with the mouse. The Delta parameter displays the power difference between M2 and M1.

3.6.2 Unit Selection

By clicking the Unit sign in the statistics section, a selection can be made to change the units of the various FFT statistics. SNR, SFDR, THD, SINAD, Fundamental, Phase, Next Spur and HD2-5 can be displayed in dBFs, dBc, or Hz. When Hz is selected, only the Fund, Next Spur, and HD2-5 will be seen in Hertz, other values will be in dBc as seen below in Figure 3-33.

	Value	Unit ▼			Value	Unit ▼			Value	Unit ▼
SNR	0	dBFs		SNR	0	dBc		SNR	0	dBc
SFDR	0	dBFs		SFDR	0	dBc		SFDR	0	dBc
THD	0	dBFs		THD	0	dBc		THD	0	dBc
SINAD	0	dBFs		SINAD	0	dBc		SINAD	0	dBc
ENOB	0	Bits		ENOB	0	Bits		ENOB	0	Bits
Fund.	0	dBFs		Fund.	0	dBFs		Fund.	0	Hz
Phase	0	Rad		Phase	0	Rad		Phase	0	Rad
Next Spur	0	dBFs		Next Spur	0	dBc		Next Spur	0	Hz
HD2	0	dBFs		HD2	0	dBc		HD2	0	Hz
HD3	0	dBFs		HD3	0	dBc		HD3	0	Hz
HD4	0	dBFs		HD4	0	dBc		HD4	0	Hz
HD5	0	dBFs		HD5	0	dBc		HD5	0	Hz
NSD/Hz	-Inf	dBFs/Hz		NSD/Hz	-Inf	dBc/Hz		NSD/Hz	-Inf	dBc/Hz
	dBFs	Hz			dBFs	Hz			dBFs	Hz
M1	0	0.00E+0		M1	0	0.00E+0		M1	0	0.00E+0
M2	0	7.50E+7		M2	0	7.50E+7		M2	0	7.50E+7

Figure 3-33. Unit Selection

3.6.3 Time Domain

The Time Domain option, when selected, will display the ADC captured data as digital codes in the time domain. The statistics of the codes reported on the left side of the GUI are minimum value (Min), maximum value (Max), Standard deviation (St. Dev), Mean, Median, RMS, Peak-to-Peak and PAR.

M1, M2, Delta – Displays the code value of the location of markers M1 and M2. These markers can be moved around on the display with the mouse. The Delta parameter displays the code value difference between M2 and M1.

Furthermore, the time domain RMS value is calculated with the DC power of the signal. The Standard deviation value does not include the DC power.

Below is an explanation of how HSDC Pro calculates the RMS and Standard Deviation values.

1. **Standard Deviation:** Square root of (Sum of (square of(All elements of the Time Domain Channel data array - Mean))/(Time Domain Channel data array size - 1))

The VI calculates the standard deviation value using the following equation:

$$\Psi_x = \sqrt{\frac{1}{n}\sum_{i=0}^{n-1}|x_i - \mu|^2}$$

where Ψ_x is the standard deviation value and n is the number of elements in X and the mean value is represented by μ.

2. **RMS:** Square root of (Sum of (square of(All elements of the Time Domain Channel data array))/(Time Domain Channel data array size - 1))

The VI calculates rms value using the following equation:

$$\Psi_x = \sqrt{\frac{1}{n}\sum_{i=0}^{n-1}|x_i|^2}$$

where Ψ_x is rms value and n is the number of elements in X.

3.6.4 Two Tone

The Two Tone option, when selected, will display a two tone ADC captured with markers placed at the locations specified by the user. The statistics of the captured data reported on the left side of the GUI are as follows:

F1 - This parameter displays the power level of the first fundamental.

F2 - This parameter displays the power level of the second fundamental.

2F1+F2 - This parameter displays the power level at the frequency that is equal to twice the first fundamental plus the second fundamental.

2F2+F1 - This parameter displays the power level at the frequency that is equal to twice the second fundamental plus the first fundamental. The other parameters follow this format.

A new window opens on the bottom left of the GUI for entering the second ADC input frequency, Figure 3-34.

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Figure 3-34. ADC 2nd Input Frequency Box

3.6.5 Channel Power

The Channel Power option, when selected, will display the calculated power of the channels selected in the parameter column on the left side of the GUI. This option will have three new setting windows displayed in the bottom left of the GUI for the user to select the number of channels (up to 5), the signal width, and channel separation of the captured data to be used for channel power measurements. Each channel that is selected for a power measurement will have two cursors, one labeled CxL and the other CxU. The "x" value will indicate the actual channel number. Figure 3-35 shows an example of a 3 channel power measurement while using the simulated ADC input function. The input test pattern is called "WCDMA_TM1_complexIF30MHZ_Fdata245.76MHZ_1000.tsw", which is located in the test files directory.
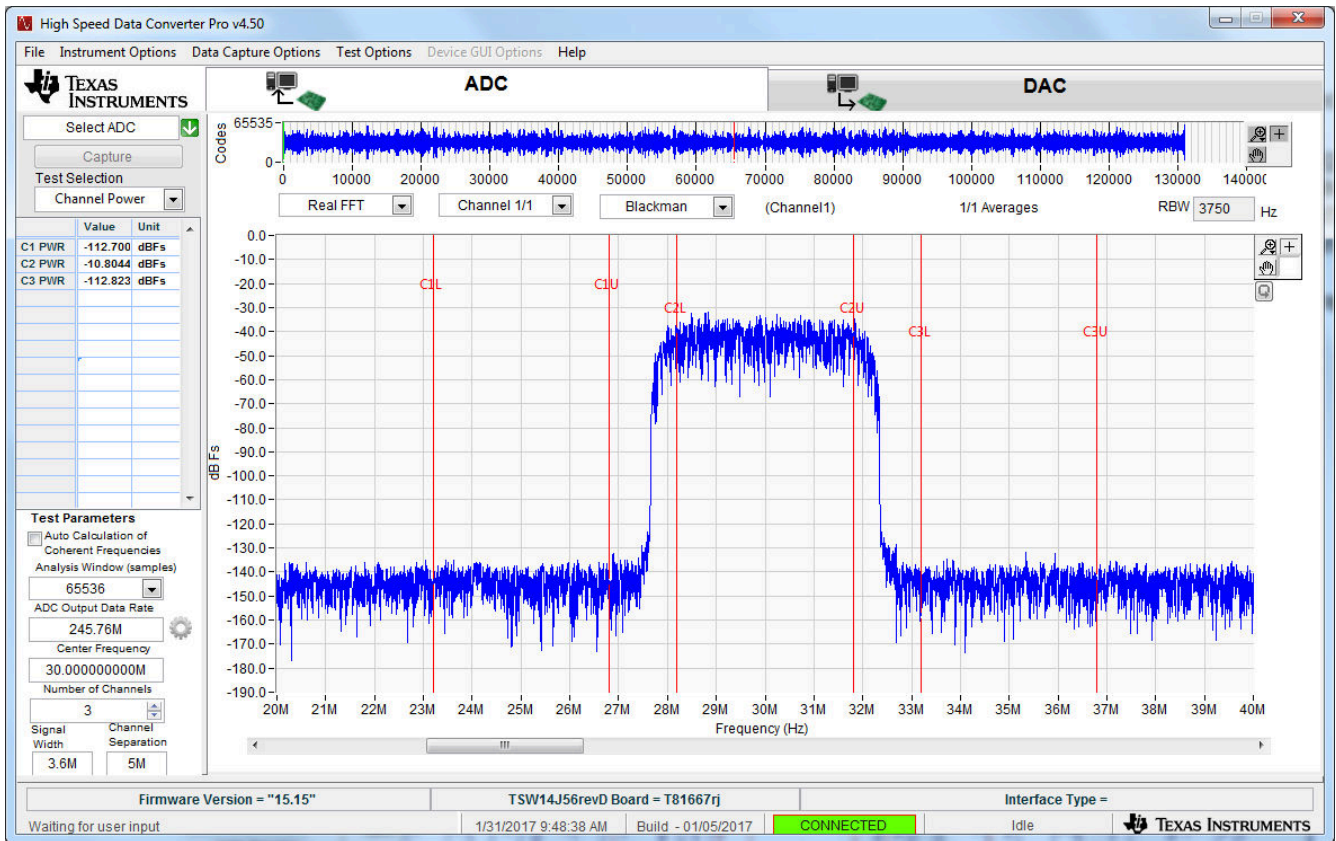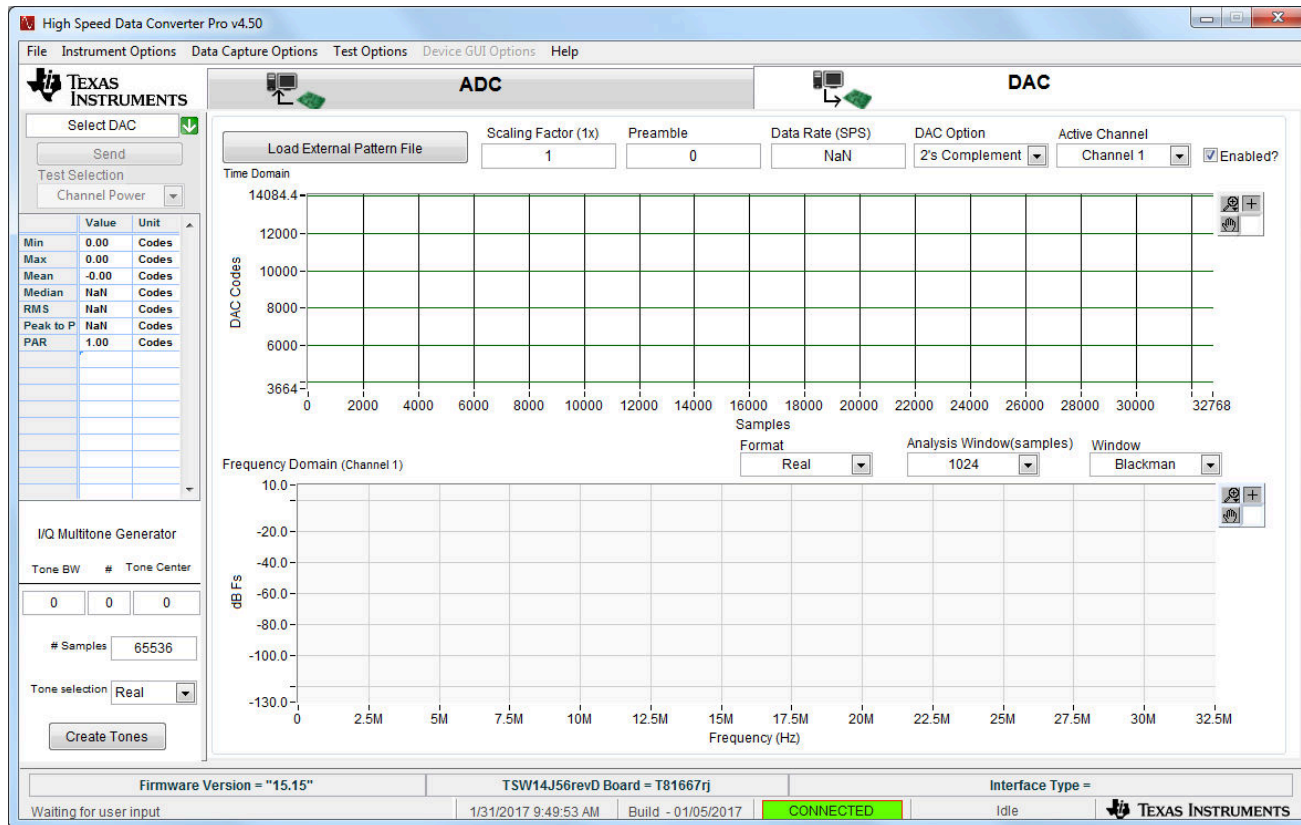
Figure 3-35. Three Channel Power Measurement Example

3.7 DAC Display Panel (DAC Mode only)

Selecting the "DAC" button at the top right of the GUI main panel will change the panel display mode for DAC operation as shown in Figure 3-36.

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Figure 3-36. DAC Display Mode

3.7.1 Send Button (DAC Mode Only)

This button, located in the upper left side of the GUI, causes the GUI to download data to the TSW14xxx on-board memory, followed by the TSW14xxx sending data from the memory module to the DAC EVM under test. This button is only active after valid data has been loaded into the PC memory by the GUI. Clicking on the "Reset Board" option under the Instruments Option tab will cause the GUI to stop sending the test pattern.

3.7.2 Load File to Transfer into TSW14xxx Button

The button labeled "Load External Pattern File" is used to select the test pattern file to be loaded into the board memory. Clicking on this button opens a navigator which the user will use to select the desired test file. The format of the test file can be either .csv or .tsw. Once selected, the file will be loaded into the PC memory used by the GUI.

The imported file must be text format integer value from – 2^ (Number of Bits -1) to 2^ (Number of Bits -1) – 1 in a single column format if testing a single DAC. For dual DAC's, the file must be in 2 columns. For quad DAC's, 4 columns. The length can be from 4096 to 512M (single column) in increments of 32 for the TSW1400 and TSW14J5x. For the TSW1406, the maximum is 16K. The GUI comes with several example test files that can be found under the following directory: C:\Program Files (x86)\Texas Instruments\High Speed Data Converter Pro\Test files.

Note: Number of Bits = Sample Resolution.

3.7.3 Parameter Controls

The five parameters used with the data file to generate the Time and Frequency domain plots are:

Scaling Factor (1x) – Scales the data based on the value (default is 1). This is applied for data loaded from files, and for the tone generated data. The scale data is sent to the DAC.

Preamble – The number of samples before the loop starting point (default is 0). This value must be in increments of 32.

Data Rate – Sample rate of I/Q samples of the test file. This is only used by the GUI FFT frequency display graph. The number is entered in Hertz (Hz), although the letter M may be appended to represent the sampling rate in MHz.

DAC Option – Determines if the test pattern file is either 2's compliment or Offset Binary.

Active Channel – Selects the channel in the test pattern file that is displayed (1, 2, 3, or 4) when the Enabled box is selected.

After a file has been loaded and the parameters updated, the GUI panel will present a graphical representation of the data. An example of an Offset Binary, 25.1-MHz tone with a data rate of 250 MHz is shown in Figure 3-37.
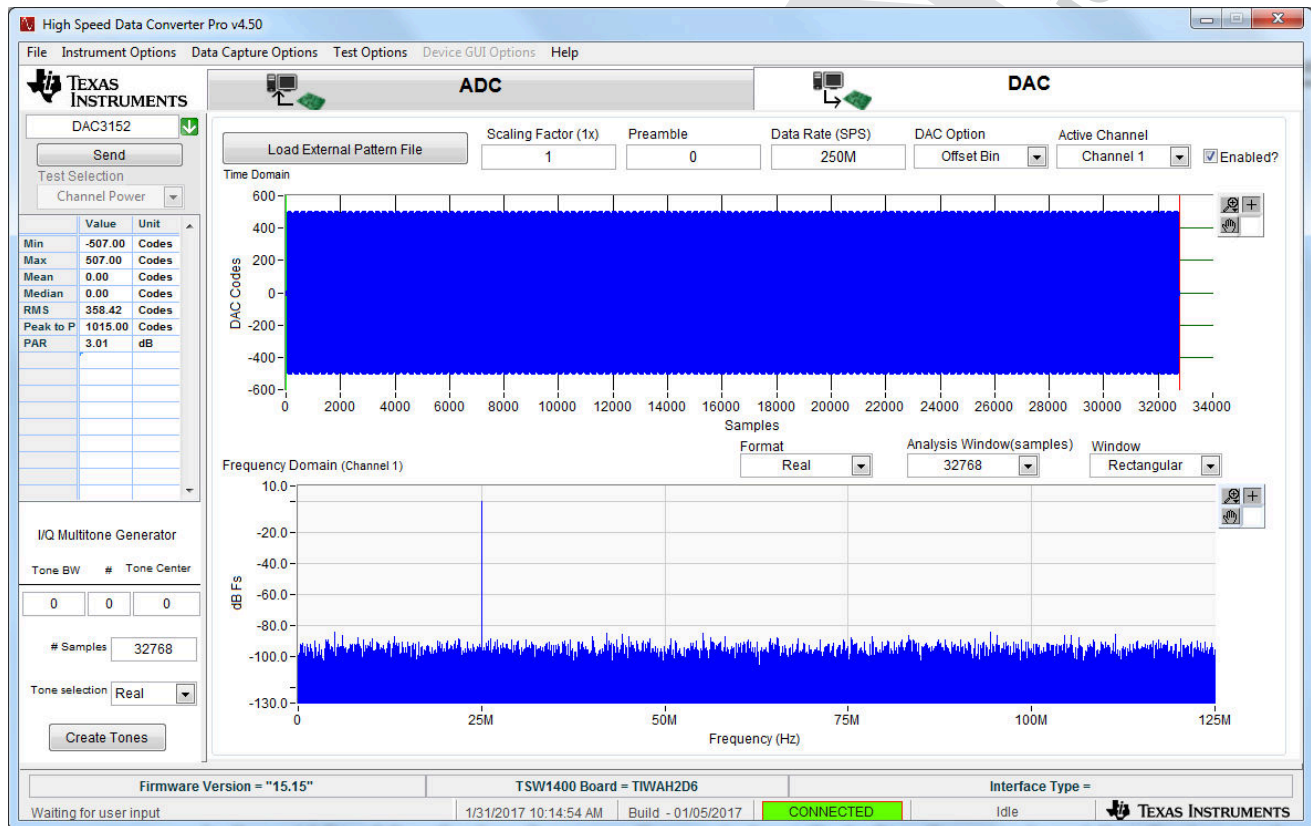
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Figure 3-37. DAC Test Pattern Display

The "Send" button will now become active. Clicking on this button starts the transfer of data from the TSW14xxx to a DAC EVM under test. This pattern is a looping test pattern that constantly runs until the send button is clicked on again.

On the TSW1400 EVM, every time the pattern starts over, a sync pulse will be generated on the SMA labeled "SYNC4". This active high pulse width will be 8 sample clock cycles wide. The SMA labeled "SYNC3" will have a clock that is the sample rate divided by 16. These signals can be used to trigger external test equipment such as a spectrum analyzer.
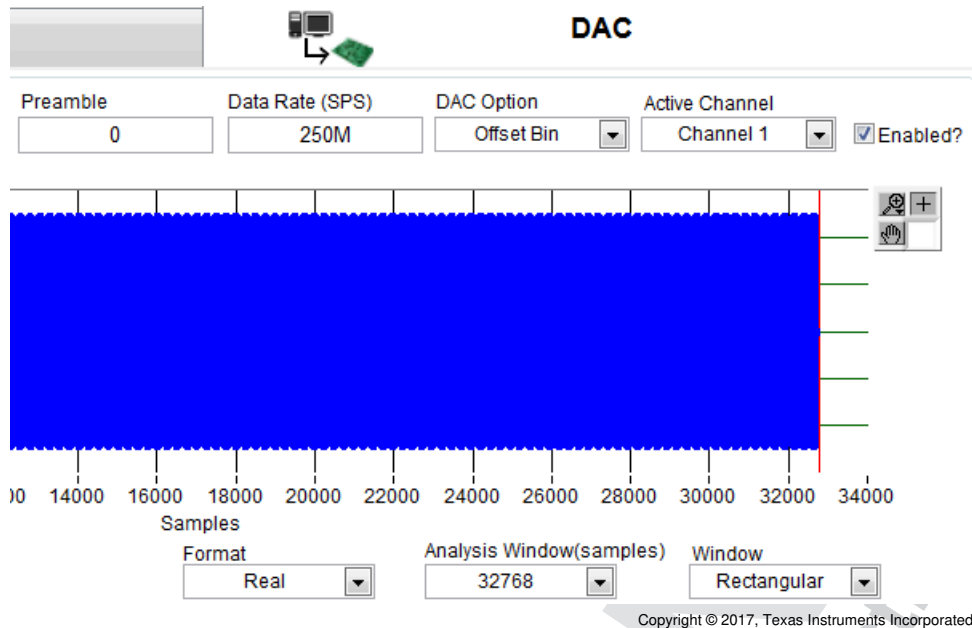
Figure 3-38. Display Mode Options

In the middle of the display, there are three windows that allow the user to set the display mode of the test pattern to be sent, as shown in Figure 3-38. The data can be displayed as complex or real, the number of data points to display (from 1024 up to 524,288 depending on the TSW14xxx under test) and different windowing options.

3.8 I/Q Multi-Tone Generator

Located in the lower left corner of the GUI is an I/Q Multi-tone Generator tool that allows the user to generate test patterns that can be used with the HSDC Pro GUI. The following parameters are used with this tool:

Tone BW – Tone bandwidth in Hertz. For Megahertz, enter a "M" after the number.

– Number of tones. If set to 1, Tone BW will be ignored.

Tone Center – Center frequency of tones in Hertz.

# of Samples – Number of test samples. 4096 to 2M, in increments of 32.

Tone Selection – Real or I/Q.

To generate a pattern, enter the desired parameters then click on the button labeled "Create Tones". Click on "Send" will send the data to the TSW14xxx memory then to the DAC EVM under test. An option exist to allow the user to save this file as well.

4 ADC Data Capture Software Operation

4.1 Testing a TSW1400 EVM with an ADS5281 EVM

This section describes the operation when testing with an ADS5281 EVM that has a LVDS output interface.

- Power down the TSW1400 if an ADC EVM is not installed.
- Connect J8 of the ADS5281 EVM to connector J3 of the TSW1400.
- Provide unpowered +5 VDC connections to J1 and return to J2 of the ADS5281 EVM.
- Provide a 1.5 V*PP* 40-MHz sine-wave clock to J26 of the ADS5281 EVM.
- Provide a filter 10 MHz analog input to CH1.
- Power up the TSW1400 followed by the ADC EVM.
- Start up the HSDC Pro GUI as described in the Software Start Up section.
- The TSW1400 EVM connected to an ADS5281 EVM is shown in Figure 4-1
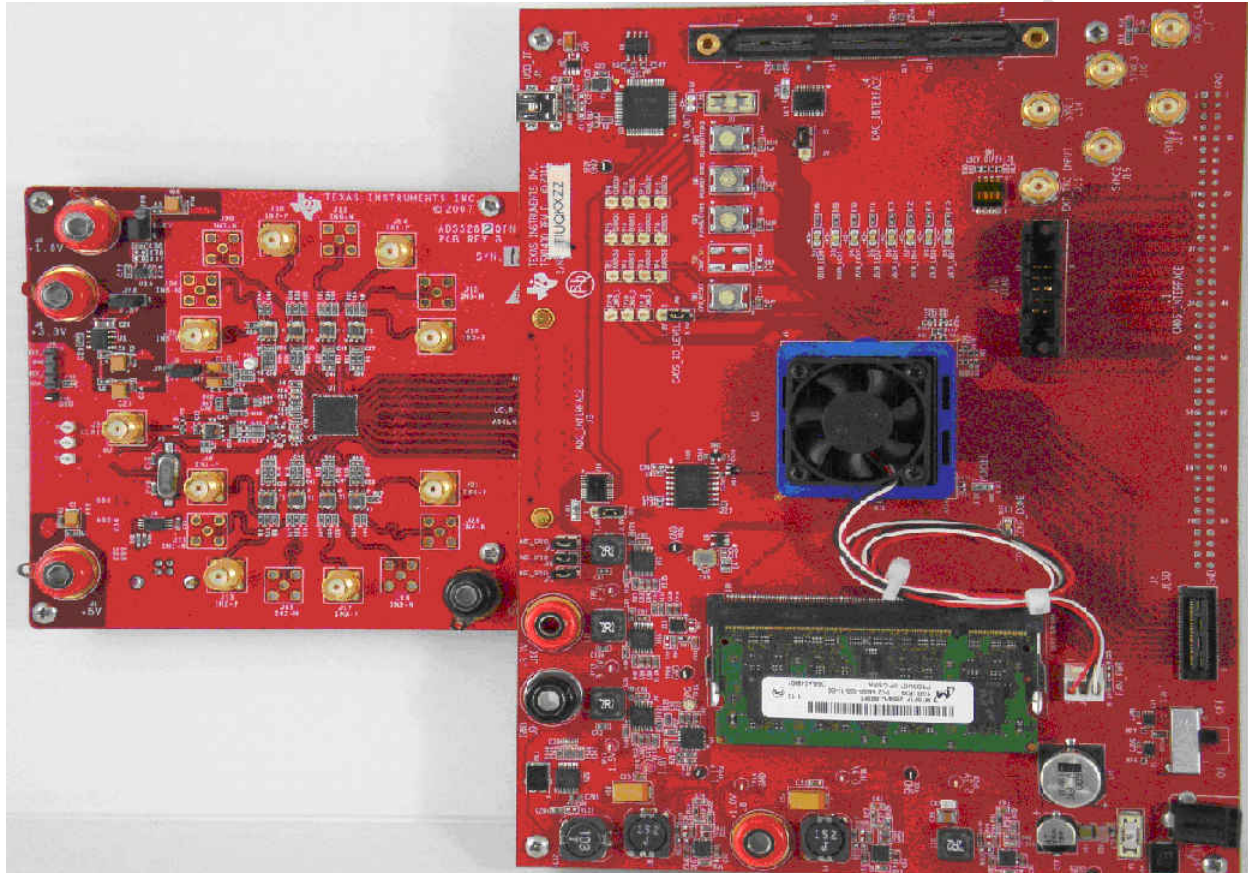
**Figure 4-1. TSW1400EVM interfacing to an ADS5281 EVM**

To setup the GUI to run in the data capture mode, click on the "ADC" tab in the top left side of the GUI. Navigate to the device selection button located in the upper left side of the GUI, click on the drop down arrow, then select "ADS5281". After clicking on this file, a pop-up will open asking "Do you want to update the Firmware for ADC". Click on "Yes". The firmware will now start loading and take ≈ 20 seconds to complete. After the ADS5281 firmware load has completed, the FPGA_CONF_DONE LED will turn on after the FPGA configured. The LED's labeled USER_LED (0–7) will also be on except for USER_LED4.

Note

If the TSW1400 is not receiving a valid clock from the ADC EVM, USER_LED3 will be off.

- Use the "Test Selection" button to change the capture display to Single Tone.
- Set the active channel setting to Channel 1/8.
- Use the default Record Length value of 65,536.

- Set the ADC Sampling Rate to 40 MHz.
- Click on the Auto Calculation of Coherent Frequency function and Rectangular capture mode if using a coherent input frequency. Otherwise, do not set this and use "Blackman" windowing mode.
- Set the input frequency source to the new value in ADC Input Target Frequency that is generated by the Auto Calculation of Coherent Frequency function.
- Make sure the display mode is set to "Frequency".
- Click on the "Capture" button to perform a data capture. The results should like similar to those shown in Figure 4-2.
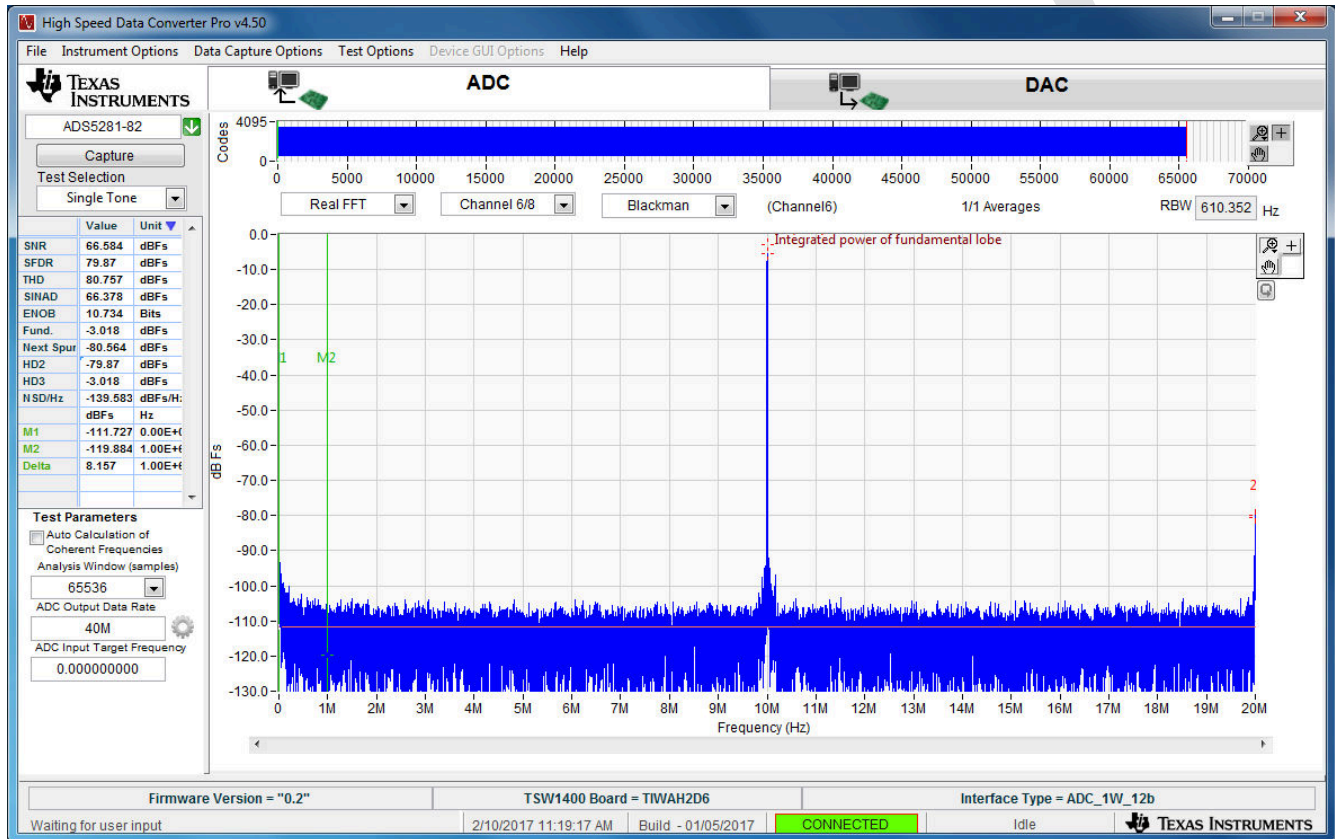
Figure 4-2. ADC5281 Single Tone FFT Capture Results

The user can now change other parameters and do another capture to observe the ADC outputs with different frequencies, amplitudes, and in other formats such as codes, or bits.

After the firmware is loaded, if the user clicks the drop down arrow in the device selection window, the GUI will indicate which ADC EVM's can be used with this firmware load by adding a black diamond in front of the device name, as shown in Figure 4-3. If the user does not power down the TSW1400, any one of the devices with a black diamond can be tested without doing another firmware load. The devices supported with the current firmware are marked with a black diamond.
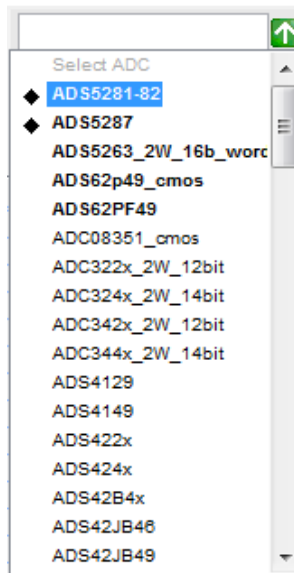
Figure 4-3. Devices Supported with Current Firmware Loaded

## 4.2 Testing a TSW1400EVM with an ADS62P49EVM (CMOS Interface)

This section describes the operation when testing with an ADS62P49 EVM that is configured for CMOS output interface.

- Power down the TSW1400 if an ADC EVM is not installed.
- Connect J1 and J2 of the ADS62P49 EVM to connector J1 of the TSW1400 EVM.

Note

Pin 1 of the TSW1400 connector plugs into pin 39 of J1 on the ADS62P49 EVM.

- Provide unpowered +5 VDC connections to J10 and return to J12 of the ADS62P49 EVM.
- Provide a 1.5 V_{PP} 40-MHz sine-wave clock to J19 of the ADS62P49 EVM. Make sure this clock is within the frequency limits specified in the data sheet when operating in CMOS mode.
- Provide a filtered 10-MHz analog input to CH1 (J6).
- Power up the TSW1400 followed by the ADC EVM.
- Setup the ADS62P49 EVM to operate in parallel mode, offset binary parallel CMOS output, and internal reference.
- Start up the HSDC Pro GUI as described in the Software Start Up section.
- The TSW1400 EVM connected to the CMOS connectors of the ADS62P49 EVM is shown in
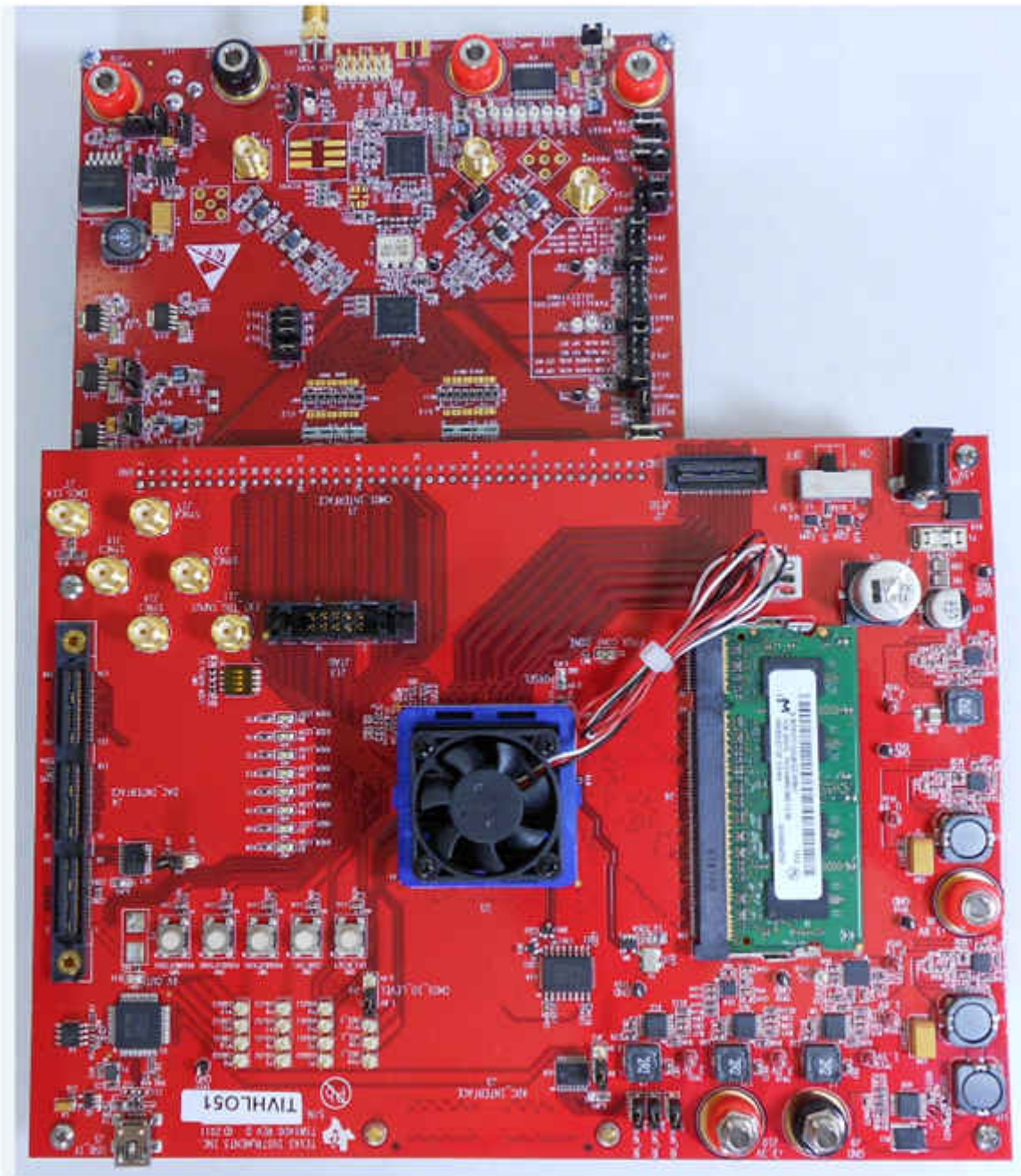
**Figure 4-4. TSW1400EVM interfacing to the CMOS connectors of an ADS62P49EVM**

To setup the GUI to run in the data capture mode, click on the "ADC" tab in the top left side of the GUI. Navigate to the device selection button located in the upper left side of the GUI, click on the drop down arrow, then select "ADS62p49_cmos". After clicking on this file, a pop-up will open asking "Do you want to update the Firmware for ADC". Click on "Yes". The firmware starts loading which takes approximately 20 seconds to complete. After the firmware load has completed, the FPGA_CONF_DONE LED turns on after the FPGA is configured. The LED's labeled USER_LED (0–7) should now all be on.

Note

If the TSW1400 is not receiving a valid clock from the ADC EVM, USER_LED3 and USER_LED4 will be off.

• Use the "Test Selection" button to change the capture display to Single Tone.

- Set the active channel setting to Channel 1/2.
- Use the default Record Length value of 65,536.
- Set the ADC Sampling Rate to 40 MHz.
- Click on the Auto Calculation of Coherent Frequency function and Rectangular capture mode if using a coherent input frequency. Otherwise, do not set this and use "Blackman" windowing mode.
- Set the input frequency source to the new value in ADC Input Target Frequency that is generated by the Auto Calculation of Coherent Frequency function.
- Make sure the display mode is set to "Frequency".
- Click on the "Capture" button to perform a data capture. The results should like similar to those shown in Figure 4-5.
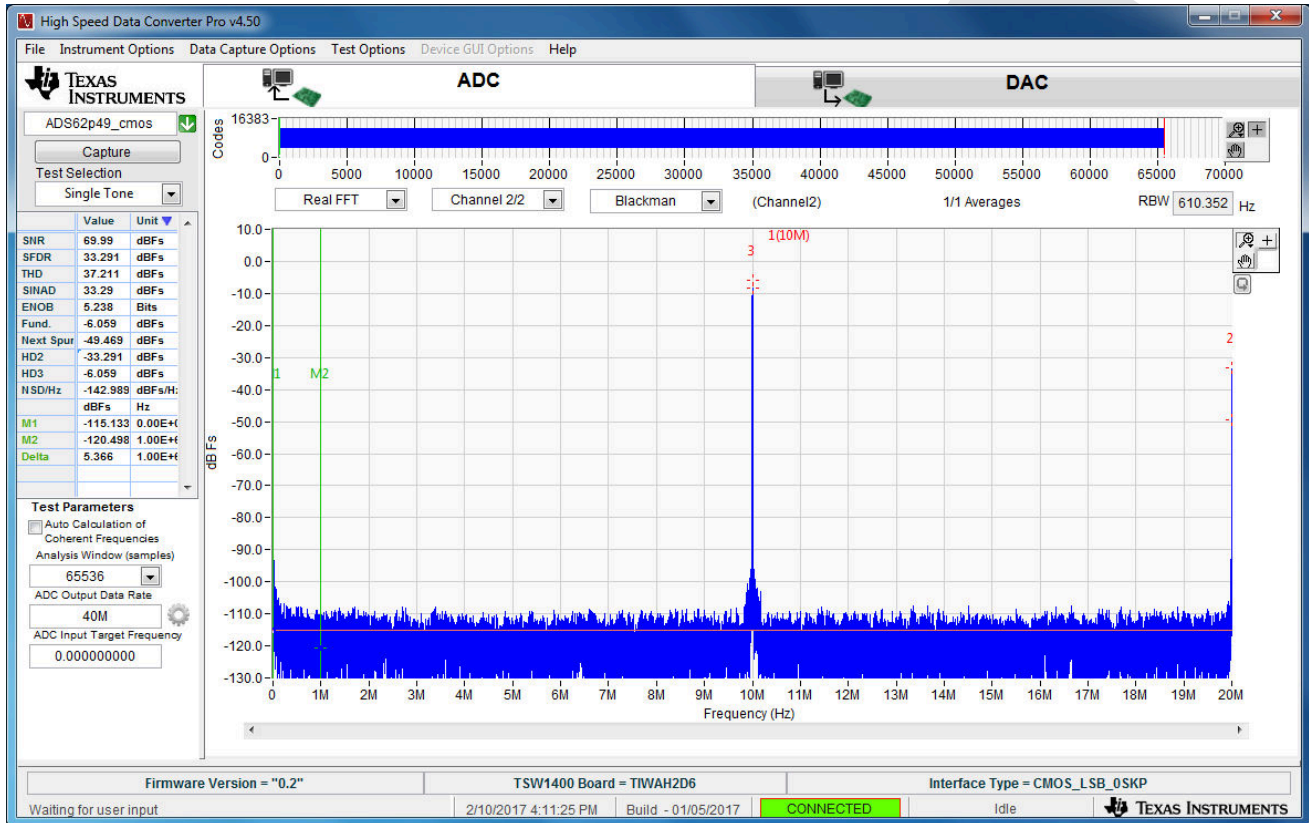
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Figure 4-5. TSW1400EVM Captured Results from ADS62P49EVM

5 TSW1400 Pattern Generator Operation

5.1 Testing a TSW1400 EVM with a DAC3152 EVM

This section describes the pattern generator operation when testing with a DAC3152 EVM that has a LVDS input interface.

- Power down the TSW1400.
- Connect J5 of the DAC3152 to connector J4 of the TSW1400.
- Provide +5 VDC to J12 and return to J13 of the DAC3152 EVM.
- Provide a 0.5-Vrms 250-MHz clock to J9 of the DAC3152 EVM.
- Power up the TSW1400 EVM
- Start up the HSDC Pro GUI as described in the Software Start Up.
- A TSW1400 EVM connected to a DAC3152 EVM is shown in Figure 5-1.
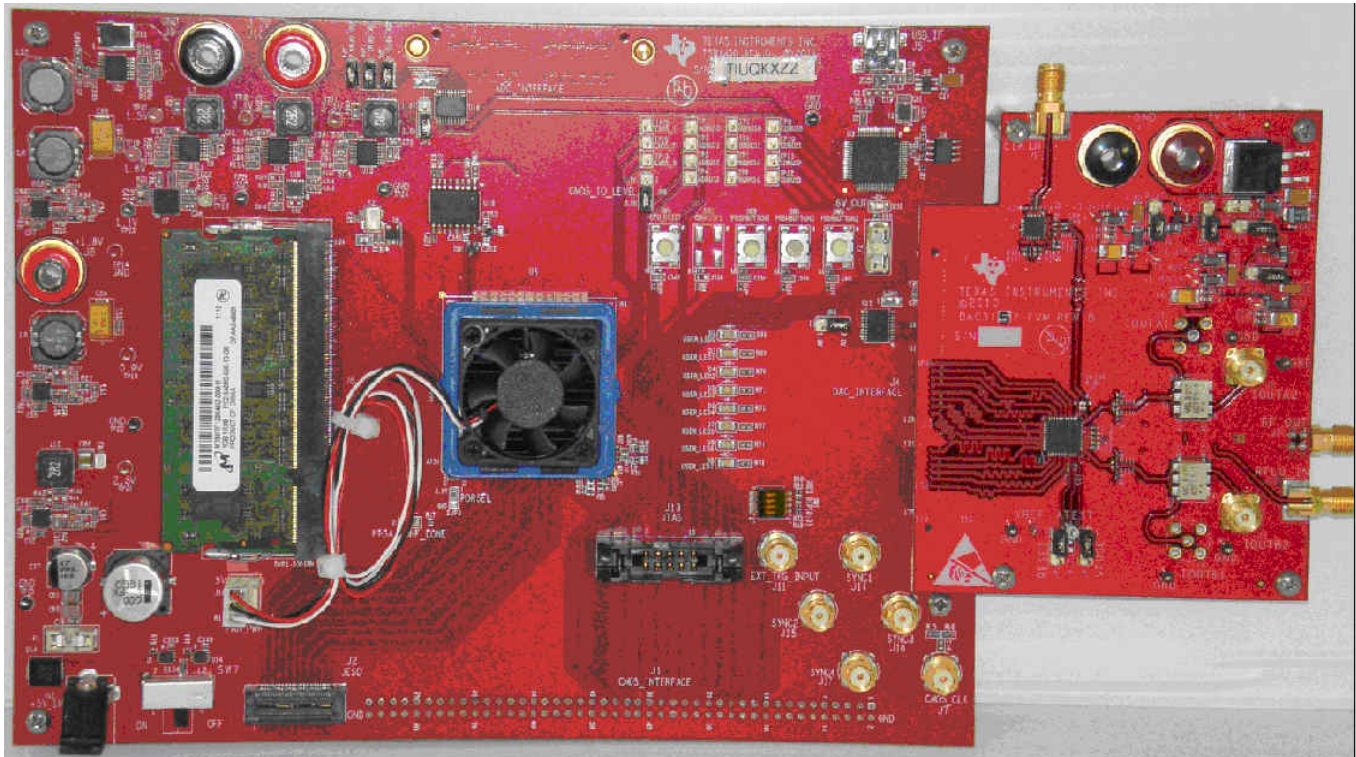
Figure 5-1. TSW1400 EVM Interfacing to a DAC EVM

Note

The FPGA clocks from DAC EVM's to the TSW1400 EVM have to be LVDS level. Exceeding LVDS levels may damage the TSW1400 FPGA.

5.2 Loading DAC Firmware

If opening the GUI for the first time, when setting up for pattern generator mode, make sure "DAC" in the top right side of the GUI is selected. After clicking on "DAC", the top level GUI shall look as shown in Figure 5-2.
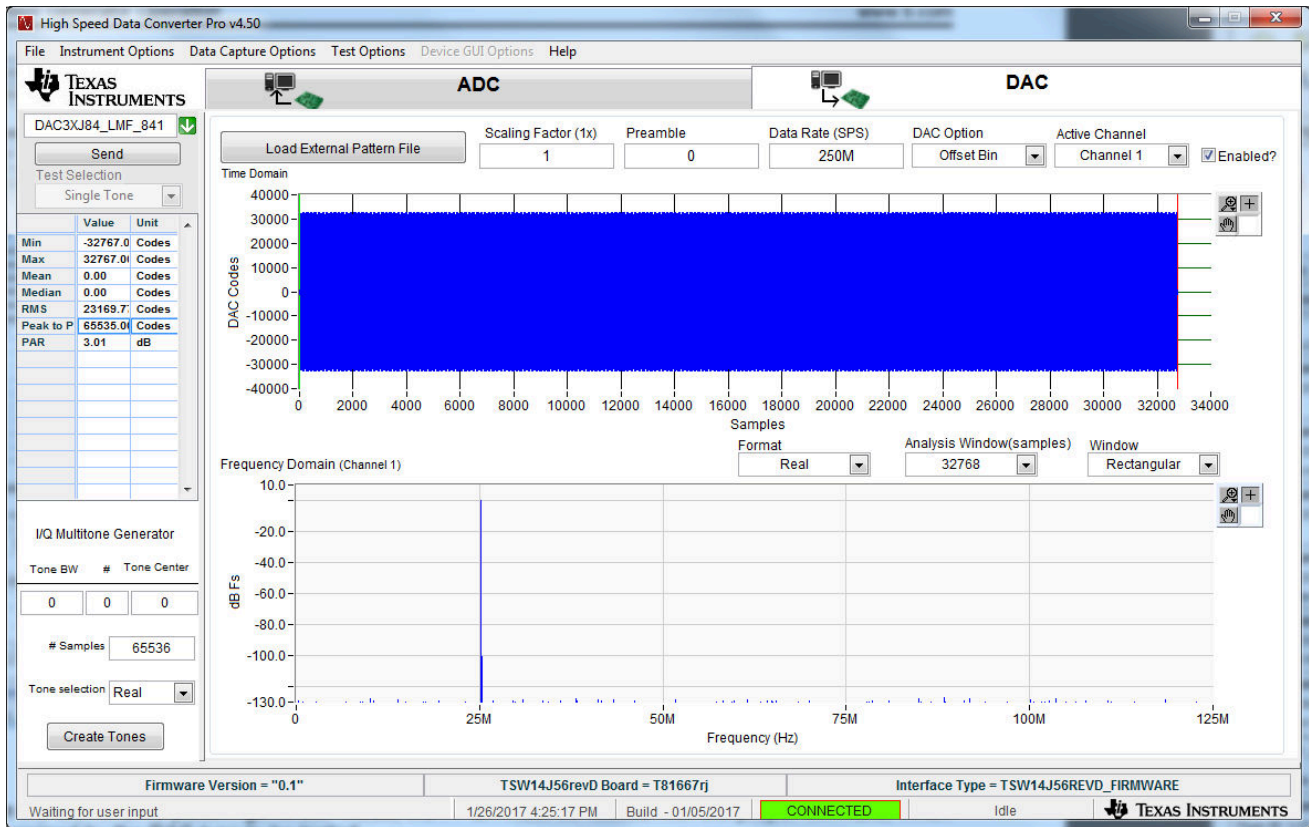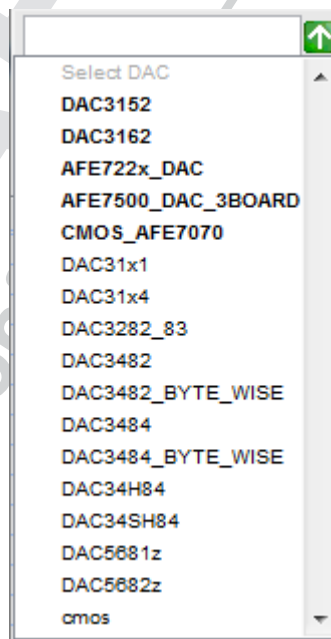
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Figure 5-2. TSW14xxxEVM GUI DAC Mode Top Level

To run the GUI in DAC pattern generator mode, the FPGA must be loaded with the proper firmware, which is determined by the DAC type to be tested.

In the "Select DAC" button of the GUI, click on the drop down arrow and select the DAC3152 (Figure 5-3). This will be the targeted EVM for this test example.

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Figure 5-3. DAC Selection

Click on "Yes" when asked "Do you want to update the firmware for DAC". The firmware for this setup will now be loaded during this process, which will take approximately 20 seconds. After the firmware load has completed, the LED's labeled USER_LED (0–7) will now turn on except for USER_LED 3 and 5. USER_LED 3 is used to indicate the status of a second PLL, which is not used with this firmware build, and USER_LED 5 indicates if there is a FIFO overflow (error) of the transmit data.

Note

If the TSW1400 is not receiving a valid clock from the DAC EVM, USER_LED3 and USER_LED4 will be off.

## 5.3 Configuring TSW1400 for Pattern Generation

For this test, at the top of the GUI, set the following parameters:
- Preamble to 0
- Data Rate – 250 MSPS
- DAC Option – Offset Binary
- Active Channel – Channel 1
- FFT Length – 32,768
- Window - Rectangular
- Scaling Factor to 1

The pattern generation data file should match one of the Record Length's to us the Rectangular window mode. If it does not, switch the window mode to another setting such as "Hanning".
- Click on the button labeled "Load External Pattern File".
- Select "single_tone_cmplx_32768_250MSPS_BW_25.1MHZ.csv".
- Click on "Send".

The display panel of the GUI will be updated, showing the test data that will be transmitted to the DAC EVM in both codes and frequency domain as shown in Figure 5-4.
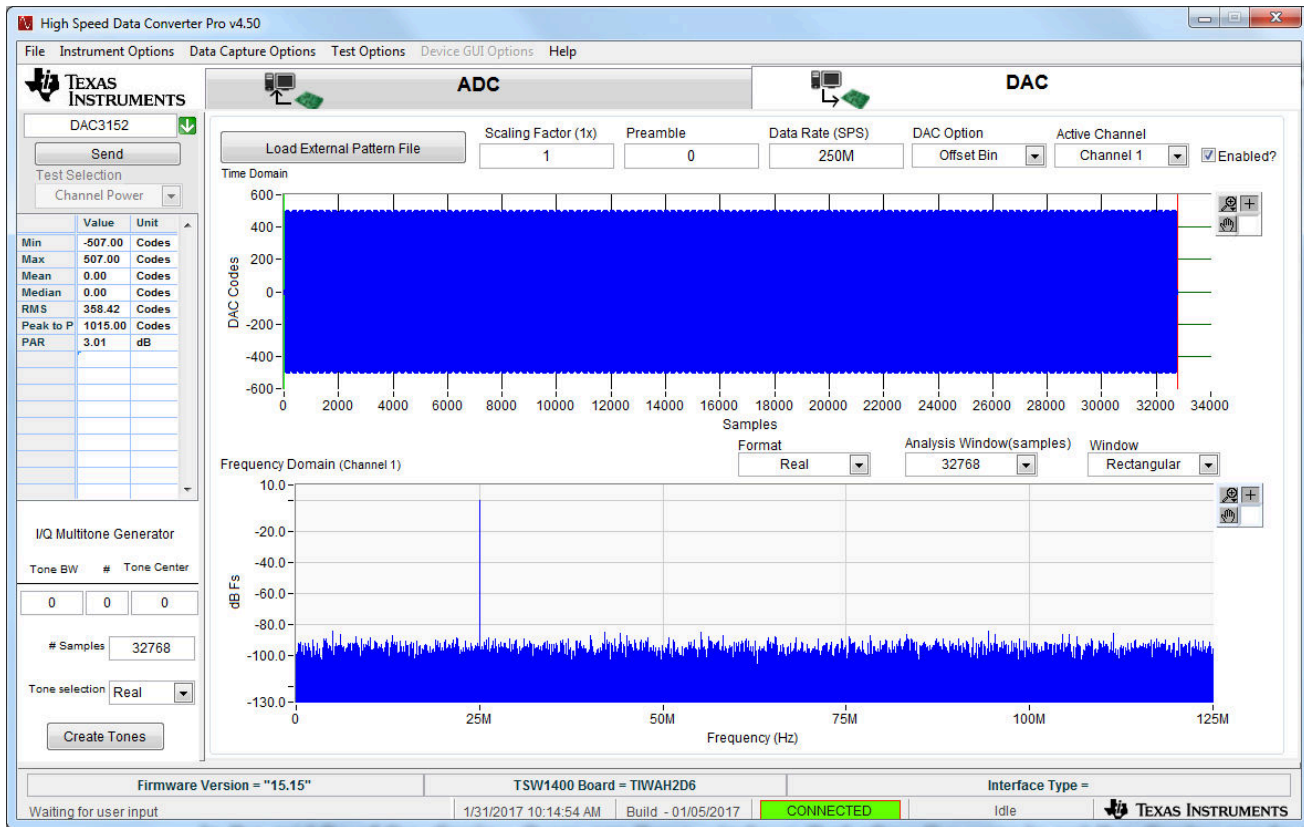
Figure 5-4. TSW1400 Output Data to DAC EVM

Using a spectrum analyzer, verify that there is now a 25.1-MHz tone present on both SMA J2 (IOUTA2) and J3 (IOUTB2) of the DAC3152 EVM.

To shut down the GUI, click on the "File" tab in the upper right corner of the GUI and select "Exit" in the pop up window that opens. This will specify that the USB ports are released by the software.

## 5.4 Testing a TSW1400 EVM with a DAC5688EVM (CMOS Interface)

This section describes the operation when testing with a DAC5688 EVM that has a CMOS input interface.

- Power down the TSW1400 if the DAC5688 EVM is not installed.

Note

J1 pin 1 of the TSW1400 connector plugs into J2 pin 1 on the DAC5688 EVM

- Provide unpowered +3.3 VDC connections to J15 and return to J16 of the DAC5688 EVM.
- Provide unpowered +1.8 VDC connections to J13 and return to J14 of the DAC5688 EVM.
- Provide a USB cable between the DAC5688 EVM and a host PC.
- Provide an external sinewave source at 491.52 MHz with a 1-Vrms, 0-V offset to SMA J20 (EXT_VCXO) of the DAC5688 EVM.
- Connect a SMA cable from OUTCLK3 connector (J17) of the DAC5688 EVM to CMOS_CLK (J7) of the TSW1400 EVM.
- Power up the TSW1400 followed by the DAC EVM.
- Load and start up the DAC5688 EVM GUI as described in the DAC5688EVM User's Guide. The software and User's Guide can be found at http://www.ti.com/tool/dac5688evm.

- Start up the HSDC Pro GUI as described in the Software Start Up section.
- The TSW1400 EVM connected to the CMOS connectors of the DAC5688 EVM is shown in Figure 5-5.
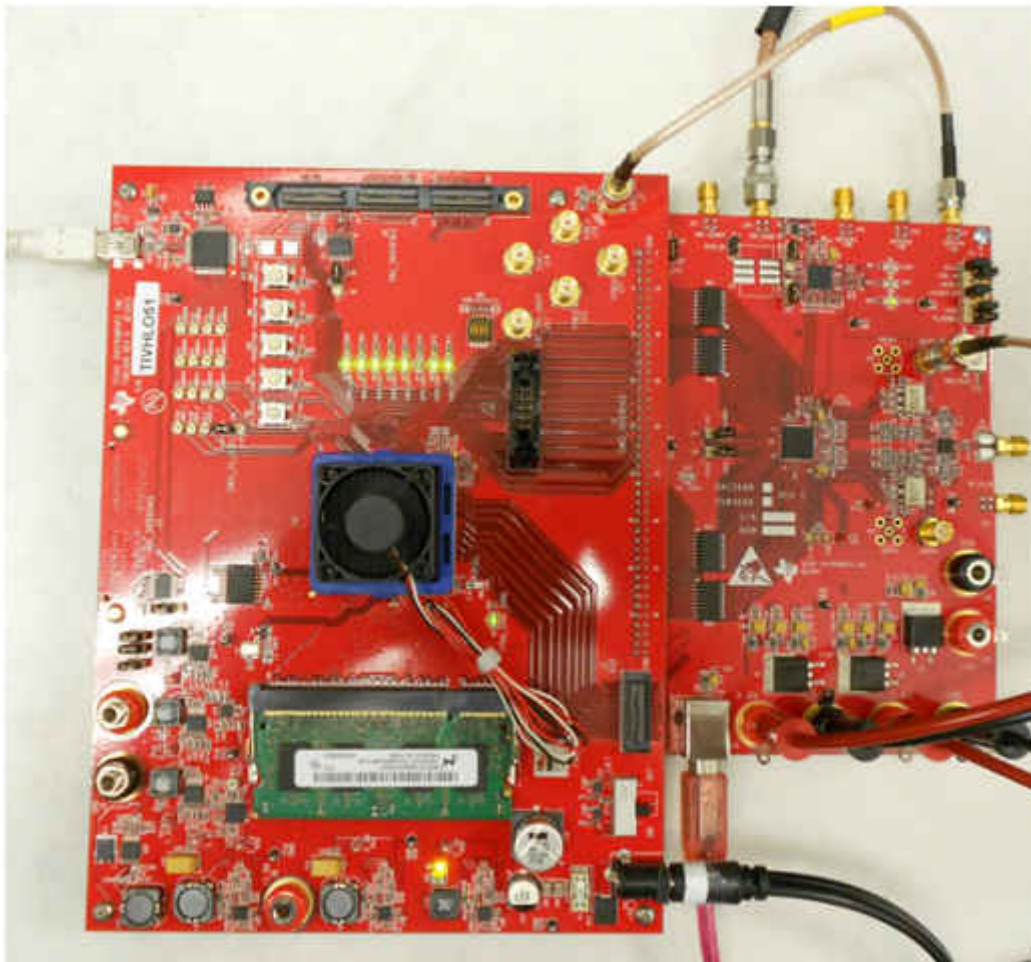
Figure 5-5. TSW1400EVM Interfacing to the CMOS Connectors of a DAC5688EVM

Using the DAC5688 EVM GUI, load the EVM with the test file called "example". This can be found at C:\Program Files (x86)\Texas Instruments\DAC5688\DAC5688 Configuration Files. This sets up the DAC5688 to receive a WCDMA test pattern from the TSW1400 with a data rate of 122.88 MHz. CLK2 of DAC5688 operates at 491.52 MHz and the DAC interpolation is set to 4x, requiring the input data rate to be at 122.88 MHz.

In the DAC5688 GUI, go to the CDCM7005 tab and set the Y3 Output (OUTCLK3) to divide by 4, LVCMOS, and inverting per Figure 5-6.
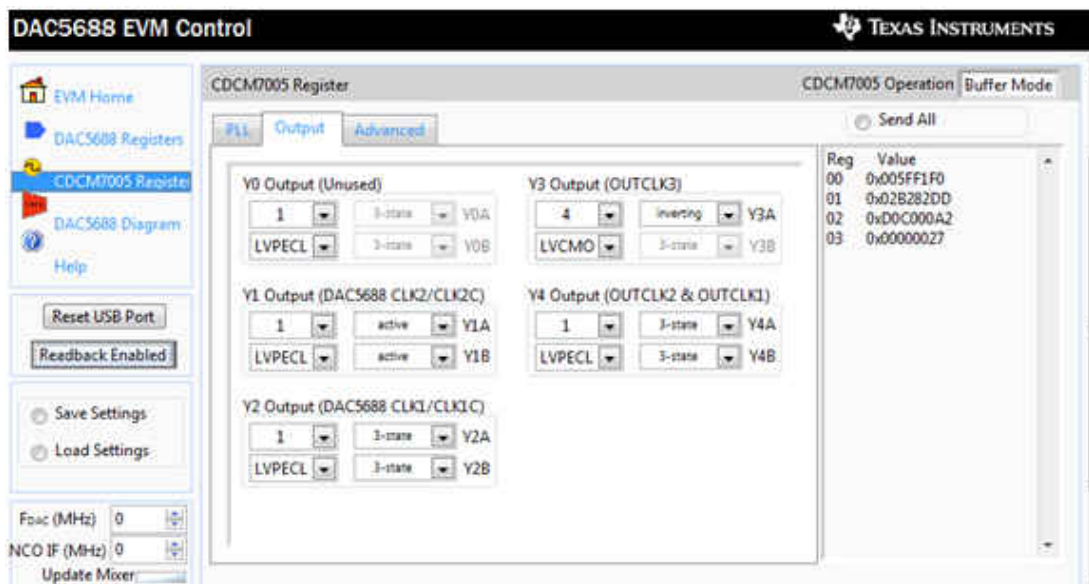
Figure 5-6. CDCM7005 Tab on DAC5688 GUI

This generates an inverted 122.88-MHz clock used by the TSW1400 to generate the CMOS test pattern.

Note

The CMOS data rate for the TSW1400 EVM should never exceed 250 MHz. This rate is set by the CMOS_CLOCK input provide to J7. When operating at frequencies near this limit, the user may need to adjust the delay of this signal to meet the timing specs of the DAC under test.

On the DAC5688 EVM, there is an option to use a spare output of the CDCM7005 clock generator as a clock source. In this example, the OUTCLK3 of the CDCM7005 is inverted for optimized setup and hold time. Another way to adjust the delay is to use different cable lengths for this clock source.

If opening the HSDC Pro GUI for the first time, when setting up for pattern generator mode, make sure "DAC" in the top right side of the GUI is selected. This targets the EVM for this test example. In the "Select DAC" button of the GUI, click on the drop down arrow and select "cmos". This firmware is used by most High Speed CMOS DAC EVM's.

Click on "Yes" when asked "Do you want to update the firmware for DAC". The firmware setup is loaded during this process, which takes approximately 20 seconds. After the firmware load has completed, the LED's labeled USER_LED (0–7) will now turn on except for USER_LED 5. USER_LED 3 is used to indicate the status of a second PLL, and USER_LED 5 indicates if there is a FIFO overflow (error) of the transmit data.


Note

If the TSW1400 is not receiving a valid clock from the DAC EVM, USER_LED3 and USER_LED4 are off.

For this test, at the top of the GUI, set the following parameters:

- Scaling factor to 1
- Preamble to 0
- Data Rate – 122.88M (MSPS)
- DAC Option – 2's Complement
- Active Channel – Channel 1
- Click on the button labeled "Load External Pattern File".
- Select "WCDMA_TM1_complexIF30MHz_Fdata122.88MHz_1000.csv".
- Click on "Send".

The display panel of the GUI is updated, showing the test data that is transmitted to the DAC EVM in both codes and frequency domain as shown in Figure 5-7.
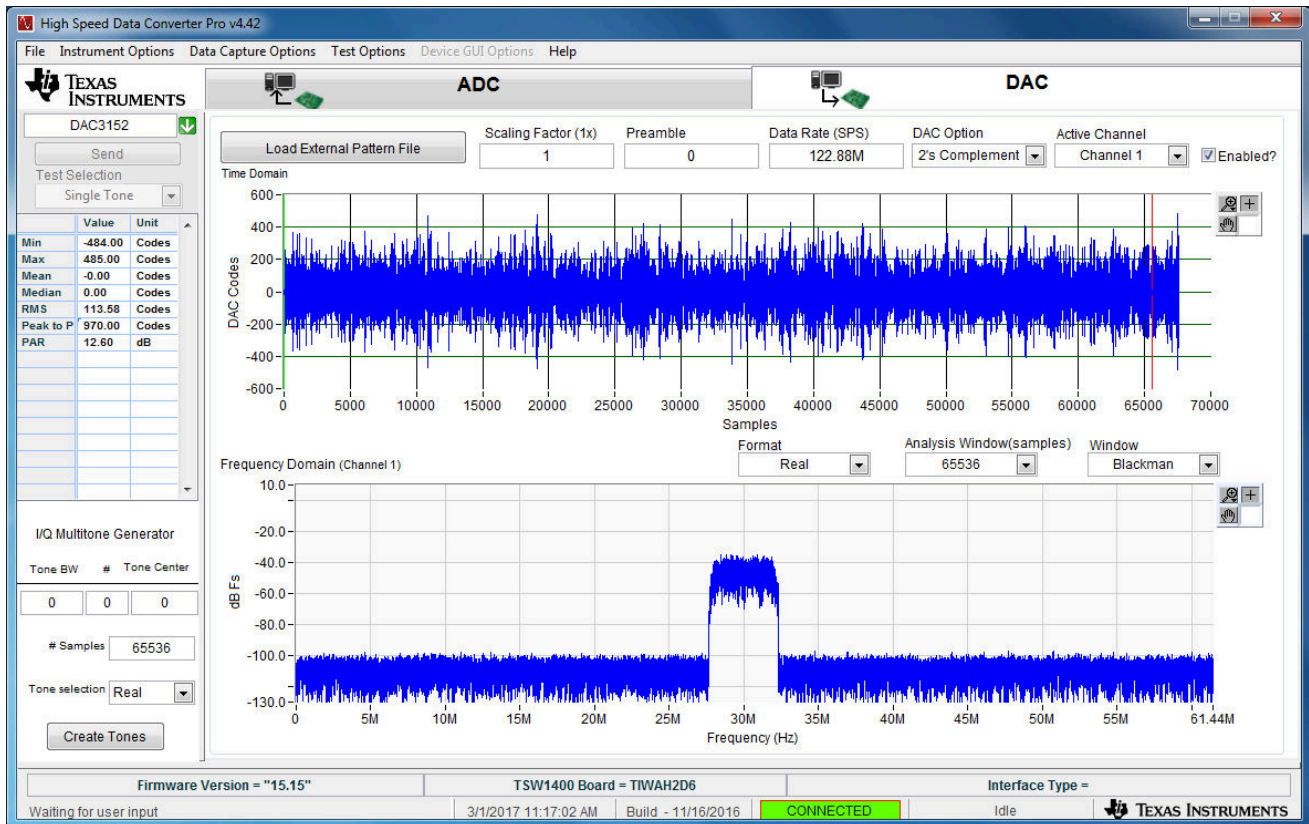
Figure 5-7. GUI After Test File Loaded

If the DAC5688 EVM is configured for IF output, connect a spectrum analyzer to either SMA J4 (IOUTB2) or J9 (IOUTA2) of the EVM. The DAC example file has a NCO setting of 61.44 MHz and the test pattern IF is centered at 30 MHz. The signal should be a single carrier centered around 91.44 MHz, as shown in Figure 5-8.

Note

The DAC5688 EVM has the default setup as RF output. The modulator output location will be at the LO frequency plus 91.44 MHz. For details about IF and RF output configuration settings, see section 4.7 of the DAC5688 EVM User's Guide (SLAU241).
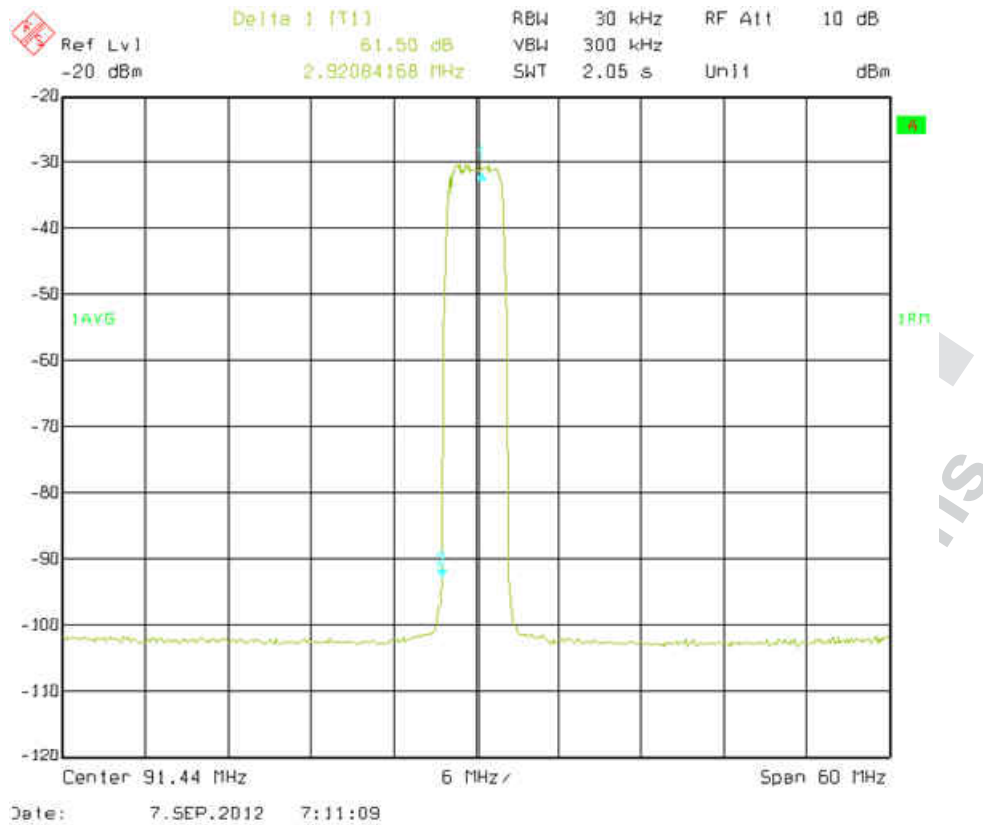

Figure 5-8. DAC5688 IF Output

6 TSW1405 Functional Description

HSDC Pro GUI operates with the TSW1405 Capture Card. This is a low cost capture card with reduced memory capacity for storing samples captured from TI High Speed ADC EVMs. The TSW1405 has a Samtec connector to directly connect to the LVDS data bus from the EVM. The TSW1405 does not have connections for CMOS ADC EVMs.

The TSW1405 does not have an EEPROM resident on the board to hold an FPGA bit file, but rather will get the bit file downloaded from the software GUI running on a PC at runtime. In this manner the TSW1405 will not need to be reprogrammed when new ADC EVMs or additional capture features become available. The planned FPGA firmware upgrades consists of new files to be downloaded to the software GUI. The TSW1405 does have a footprint for a firmware EEPROM to be installed, if desired. An illustration of the TSW1405 EVM connected to the DAC input of the AFE7225 EVM is shown in Figure 6-1.
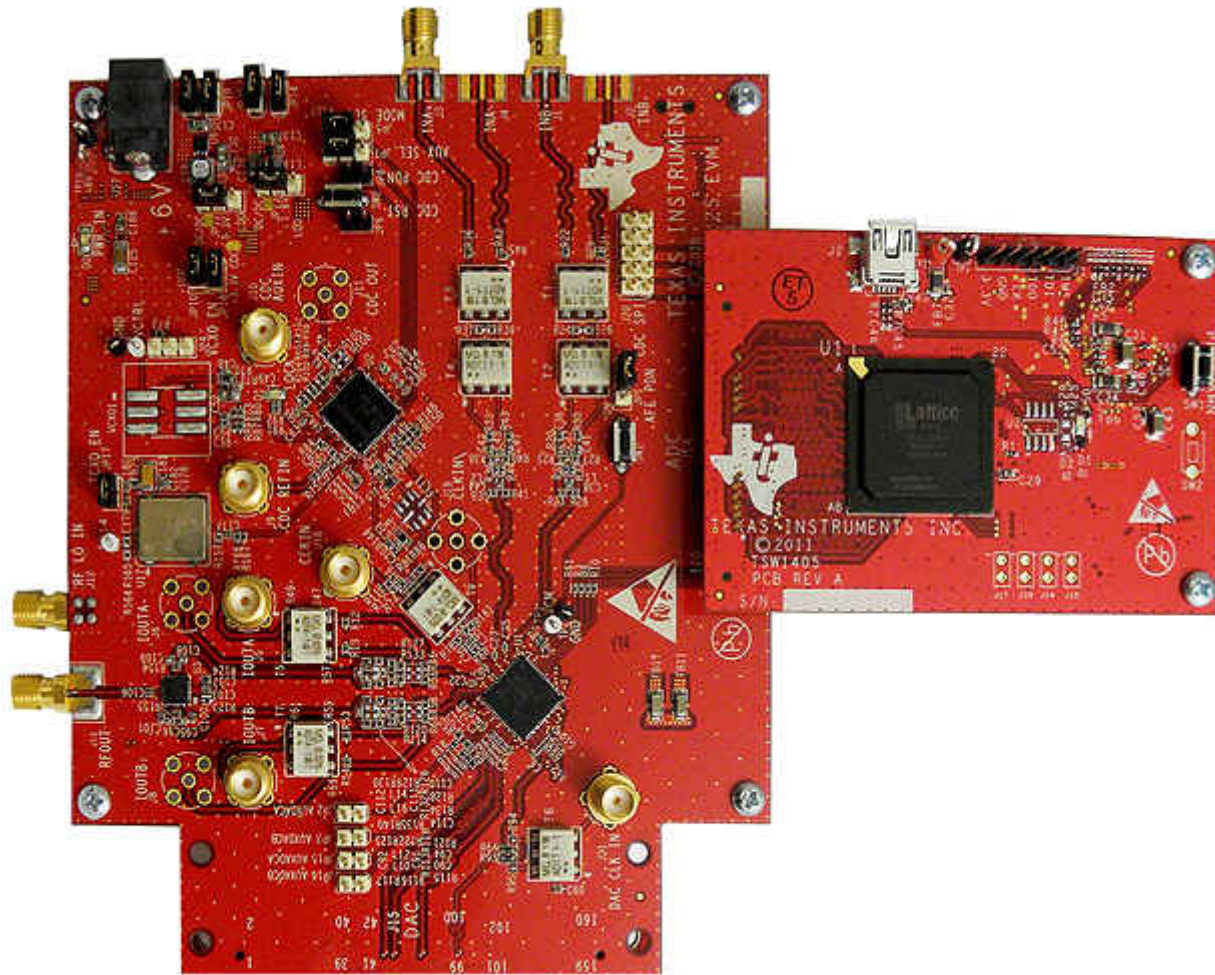
Figure 6-1. TSW1405 EVM Connected to the ADC Output of the AFE7225 EVM

6.1 Software Operation

The TSW1405 uses the HSDC Pro GUI which provides for a consistent and familiar experience for the user of the TI Capture Cards. When the GUI is launched on the PC, the GUI will detect the TSW1405 capture card and connect it to the PC USB port, and allow the user to select which to connect to if more than one EVM is connected.

6.1.1 Channel Selection

Because the TSW1405 has limited memory for sample capture, the GUI makes provision for selecting the number of channels from which to capture samples. This is a feature in the GUI that is not needed for the TSW1400 or TSW14J5x, so there is a GUI popup dialog box only used by the TSW1405, as shown in Figure 6-2.

If a device is selected in the GUI that has more than one channel available, the Channel Selection Dialog window will let the user select one or more channels to be used for capture. If two, four or eight channels are selected, then samples from those channels are captured into the capture memory simultaneously.
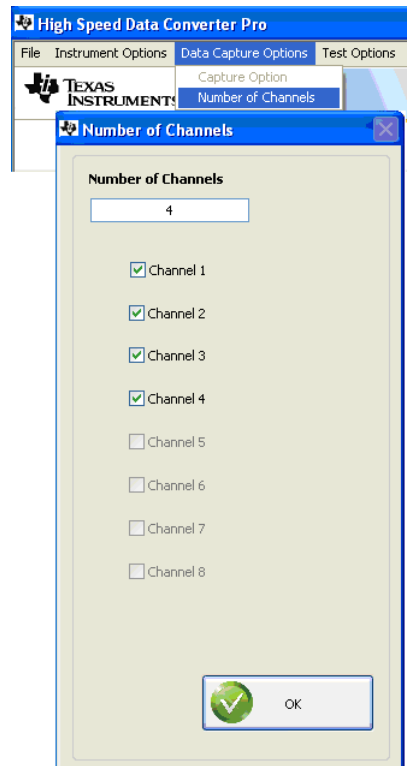

Figure 6-2. Number of Channels Selection

The TSW1405 has enough internal memory in the FPGA to capture as many as 65,536 samples of 16bit data. The 65,536 samples will be automatically allocated to one, two, four or eight channels depending on the channel selections set in the GUI. If one channel is selected for capture, then the record length for that channel will be 65,536 samples. If two channels are selected for capture, then each channel will get a record length of 32,768 samples. Four channels will cause a record length of 16,384 samples to be captured for each channel, and eight channels will capture 8,192 samples for each channel.

7 TSW1406 Functional Description

HSDC Pro GUI operates with the TSW1406 Pattern Generator Card, a low cost pattern generator card with reduced memory capacity for providing test patterns to TI High Speed DAC EVMs. The TSW1406 has a High Speed Samtec connector that directly connects to the LVDS input data bus of DAC EVM. The TSW1406 does not have connections for CMOS DAC EVMs.

The TSW1406 does not have an EEPROM resident on the board to hold an FPGA bit file, but rather will get the bit file downloaded from the software GUI running on a PC at runtime. In this manner the TSW1406 will not need to be reprogrammed when new DAC EVMs or additional capture features become available. The planned FPGA firmware upgrades consists of new files to be downloaded to the software GUI. The TSW1406 does have a footprint for a firmware EEPROM to be installed, if desired. An illustration of the TSW1406 EVM connected to the DAC input of the AFE7225 EVM is shown in Figure 7-1.
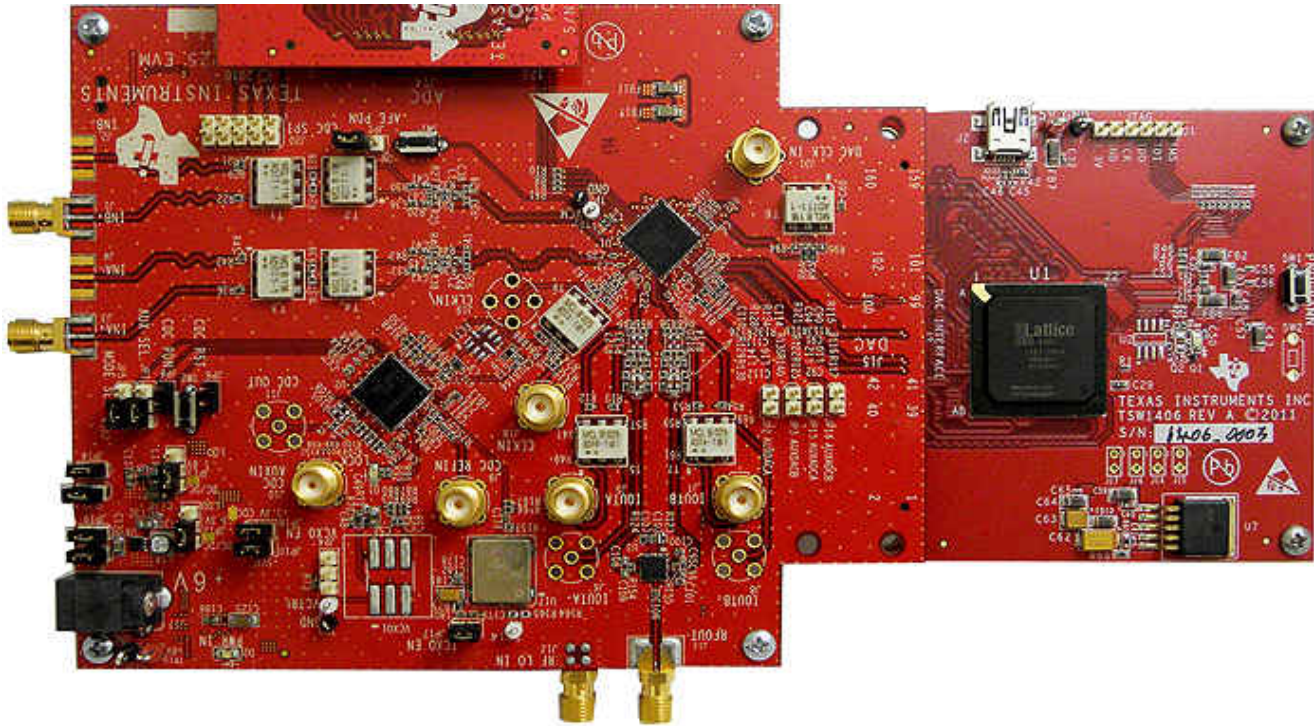
Figure 7-1. TSW1406 EVM Connected to the DAC input of the AFE7225 EVM

7.1 Software Operation

The TSW1405 uses the HSDC Pro GUI which provides for a consistent and familiar experience for the user of the TI Pattern Generator Cards. When the GUI is launched on the PC, the GUI will detect the TSW1406 capture card and connect it to the PC USB port, and allow the user to select which to connect to if more than one EVM is connected.

8 TSW14J58 Functional Description

The TSW14J58 EVM is a pattern generator and data capture card with a JESD204B/C serial interface. The TSW14J58 has a single industry standard FMC+ connector that interfaces directly with TI JESD204B ADC, DAC, and AFE EVMs. (see Figure 8-1). For an ADC, the high speed serial data is captured, de-serialized, and formatted by a Xilinx® Kintex® UltraScale® + FPGA. The data is then stored into an external DDR4 memory bank, enabling the TSW14J58 to store up to 1.536G, 16-bit data samples. It also supports lane speeds from 1.6 Gbps to 24.5 Gbps, from 1 to 16 lanes. Together with the accompanying HSDC Pro GUI, it is a complete system that captures and evaluates data samples from ADC EVMs, generates and sends desired test patterns to DAC EVMs, and perform both tasks simultaneously with AFE EVMs (transciever mode).

To acquire data on a host PC, the FPGA reads the data from memory and transmits it on a high-speed 16-bit parallel interface. An onboard high-speed USB 3.0 to parallel converter bridges the FPGA interface to the host PC and GUI.

In pattern generator mode, the TSW14J58 generates the desired test patterns for DAC EVMs under test. These patterns are sent from the host PC over the USB interface to the TSW14J58. The FPGA stores the data received into the board DDR4 memory module. The data from memory is then read by the FPGA and transmitted to a DAC EVM across the FMC+ interface connector.
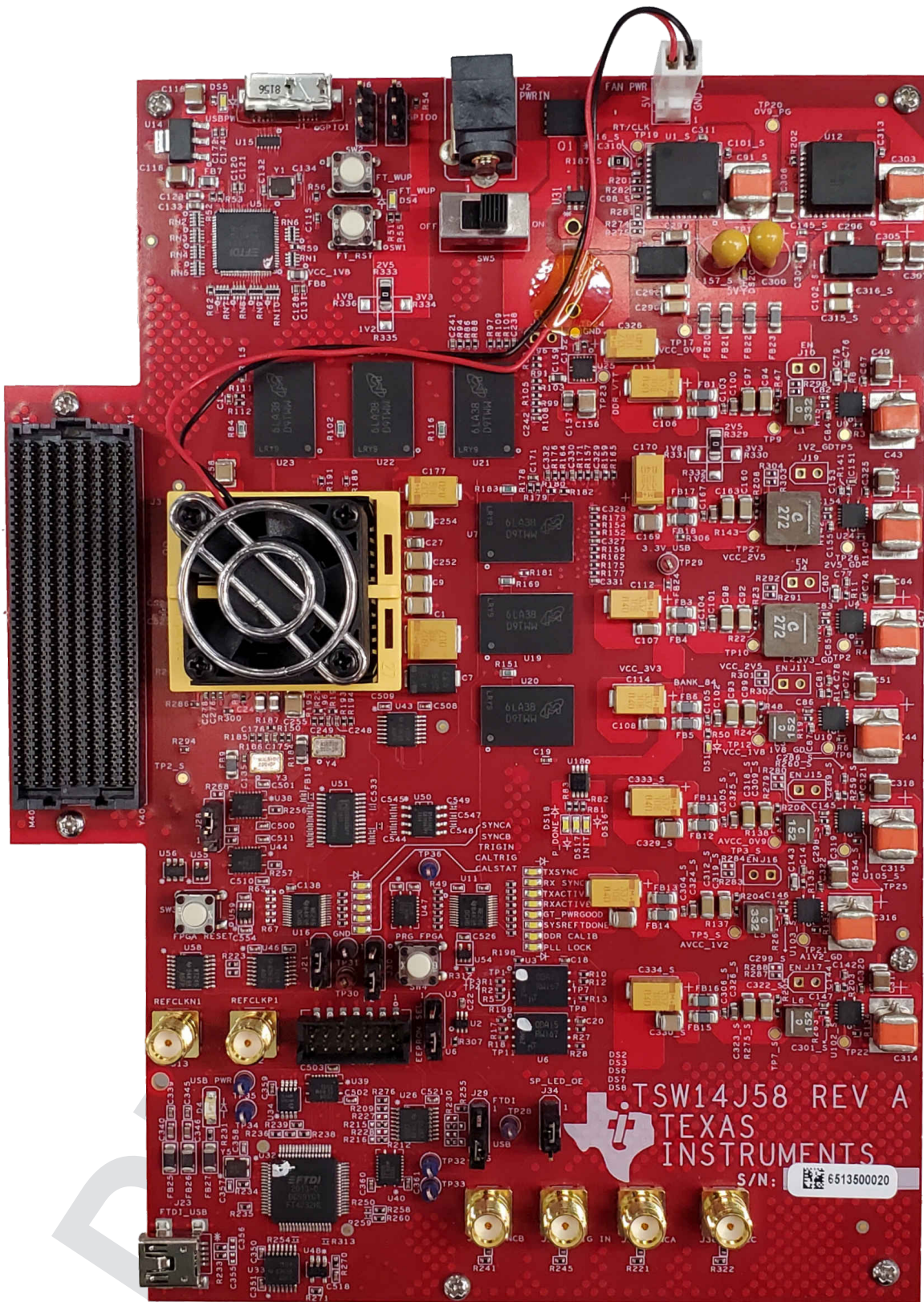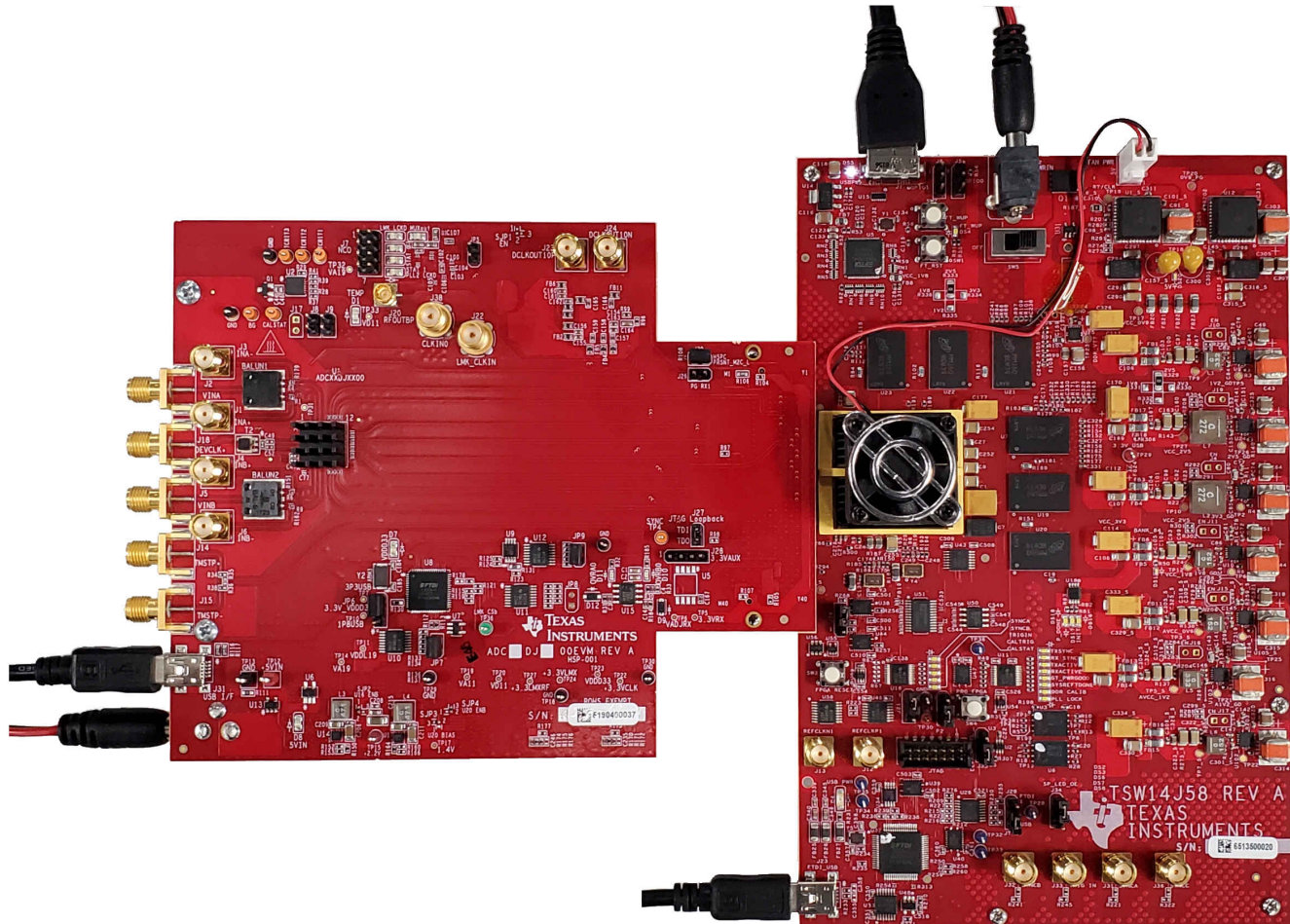
Figure 8-1. TSW14J58 EVM

8.1 Testing the TSW14J58 EVM with an ADC12DJ3200 EVM

This section describes the operation when testing with an ADC12DJ3200 EVM that has a JESD204B output interface.

- Power down the TSW14J58 EVM if an ADC EVM is not installed.
- Connect the ADC12DJ3200 EVM to the TSW14J58 EVM using the FMC connector.
- Provide +6 V_{DC} connection to J2 of the TSW14J58 EVM and +5 V_{DC} connection to J37 of the ADC12DJ3200 EVM.
- Connect a Micro-USB 3.0 cable to J1 and a Mini-USB 2.0 cable to J23 of the TSW14J58 EVM.
- Connect a Mini-USB 2.0 cable to J31 of the ADC12DJ3200 EVM.
- Power up the TSW14J58 and ADC12DJ3200 EVMs.
- The TSW14J58 EVM connected to an ADC12DJ3200 EVM is shown in Figure 8-2.

Figure 8-2. TSW14J58 EVM connected to an ADC12DJ3200 EVM

Single Tone FFT Test

1. The evaluation of the ADC12DJ3200 EVM requires programming the ADC, LMK04828, and LMX2582 devices. This process is easy using the ADC12DJxx00EVM GUI.
    - Open the ADC12DJ3200 GUI and connect to the ADC.
    - Select the onboard clock as the clocking source and choose a sampling rate from the drop down menu. This example uses a 3Gsps sampling rate.
    - Choose JMODE3 as the *Decimation and Serial Data Mode* (Dual channel, 16 JESD204B lanes).
    - Press the *Program Clocks and ADC* button and wait for programming to complete.
2. Start the HSDC Pro GUI program. When the program starts, first connect to the TSW14J58 EVM board and then select the device *ADC12DJ3200_JMODE3_2G_3G* under the the *Select ADC* drop-down menu, as seen in Figure 8-3.
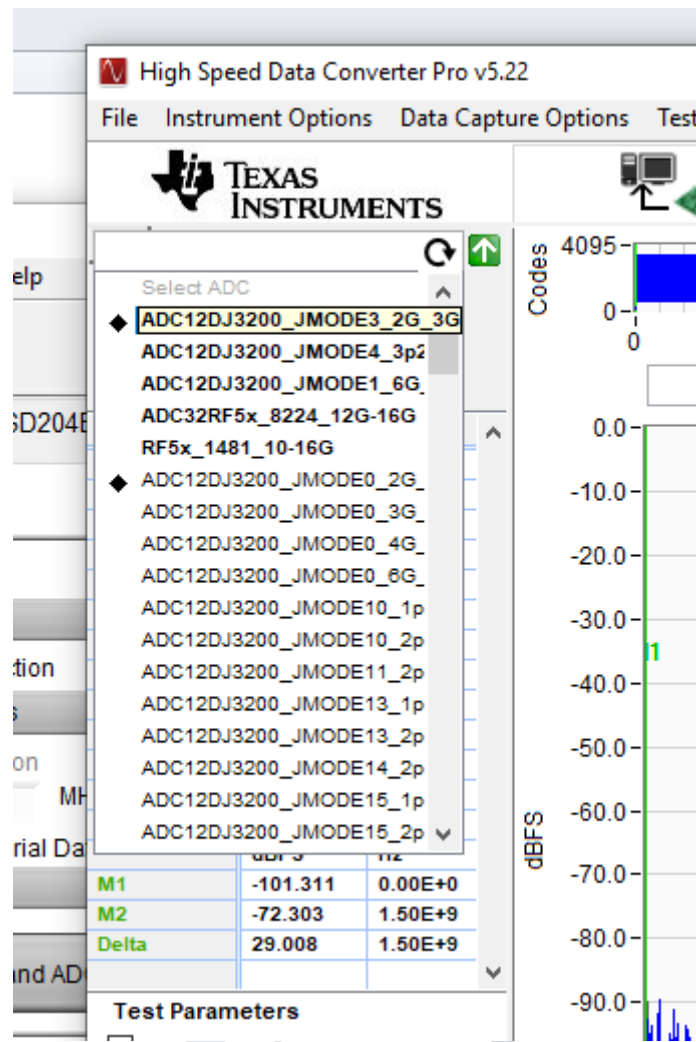
Figure 8-3. Select *ADC12DJ3200_JMODE3_2G_3G* in the HSDC Pro GUI Program

3. When prompted by *Load ADC Firmware?*, select YES
4. Select Single Tone FFT Test under Test Selection.
5. Select the number of sample points (and resulting number of FFT bins) to be used. The example shown in Figure 8-4 has 65536 samples.
6. Enter the ADC12DJ3200 sampling rate. The example shown in Figure 8-4 has the sample rate set at 3 Gsps.
7. Enter the input frequency desired. The example shown in Figure 8-4 has the filtered input frequency set at 347 MHz and -3 dBFs on the HSDC Pro FFT plot.
8. Select the channel the signal generator is connected to (channel B shown).
9. Press the *Capture* button on the HSDC Pro GUI.
10. Observe an FFT result similar to that of Figure 8-4.
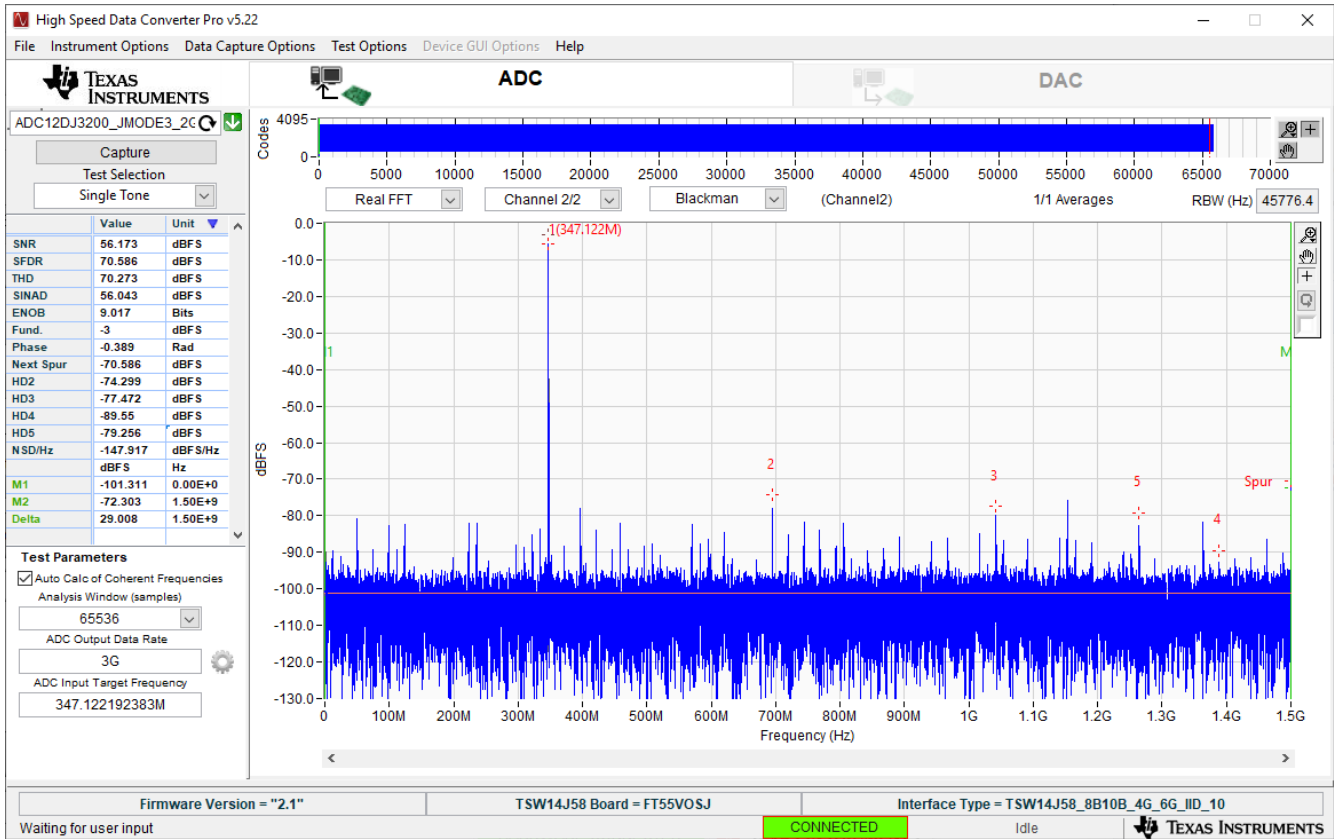
Figure 8-4. ADC12DJ3200 Operating in JMODE3 at 3 Gsps with 347-MHz Input Signal

9 TSW14J57 Functional Description

The TI TSW14J57 EVM is a pattern generator and data capture card with a JESD204B serial interface. The TSW14J57 has an FMC+ connector that can be used to evaluate the performance of the TI JESD204B device family ADCs and DACs (see Figure 9-1). For an ADC, the high speed serial data is captured and de-serialized and formatted by an Intel PSG® Arria® 10 FPGA, then stored in an onboard DDR4 SDRAM, allowing the TSW14J57 to store up to 1G of 16-bit samples. It also supports lane speeds from 2 Gbps to 15 Gbps, from 1 to 16 lanes with one firmware build. Together with the accompanying HSDC Pro GUI, it is a complete system that captures and evaluates data samples from ADC EVMs and generates and sends desired test patterns to DAC EVMs.

To acquire data on a host PC, the FPGA reads the data from memory and transmits it on SPI. An onboard high-speed USB-to-SPI converter bridges the FPGA SPI interface to the host PC and GUI.

In Pattern Generator Mode, the TSW14J57 generates desired test patterns for DAC EVMs under test. These patterns are sent from the host PC over the USB interface to the TSW14J57. The FPGA stores the data received into the board DDR4 memory module. The data from the memory is then read by the FPGA and transmitted to a DAC EVM across the JESD204B interface connector.

In the Instrument Options tab of the GUI, the option called "Dynamic Configuration" allows the user to change certain JESD204B parameters without loading new firmware into the FPGA. The ini files load default values for these parameters based on what ADC or DAC is selected and what mode of operation is chosen. For the most part, users should not have to change these values in this tab. If any values are changed, the default values of the ini file will be overwritten. Any changes will effect the operation of the JESD204B interface and will have to be made at both the receiver and transmit side of the interface.
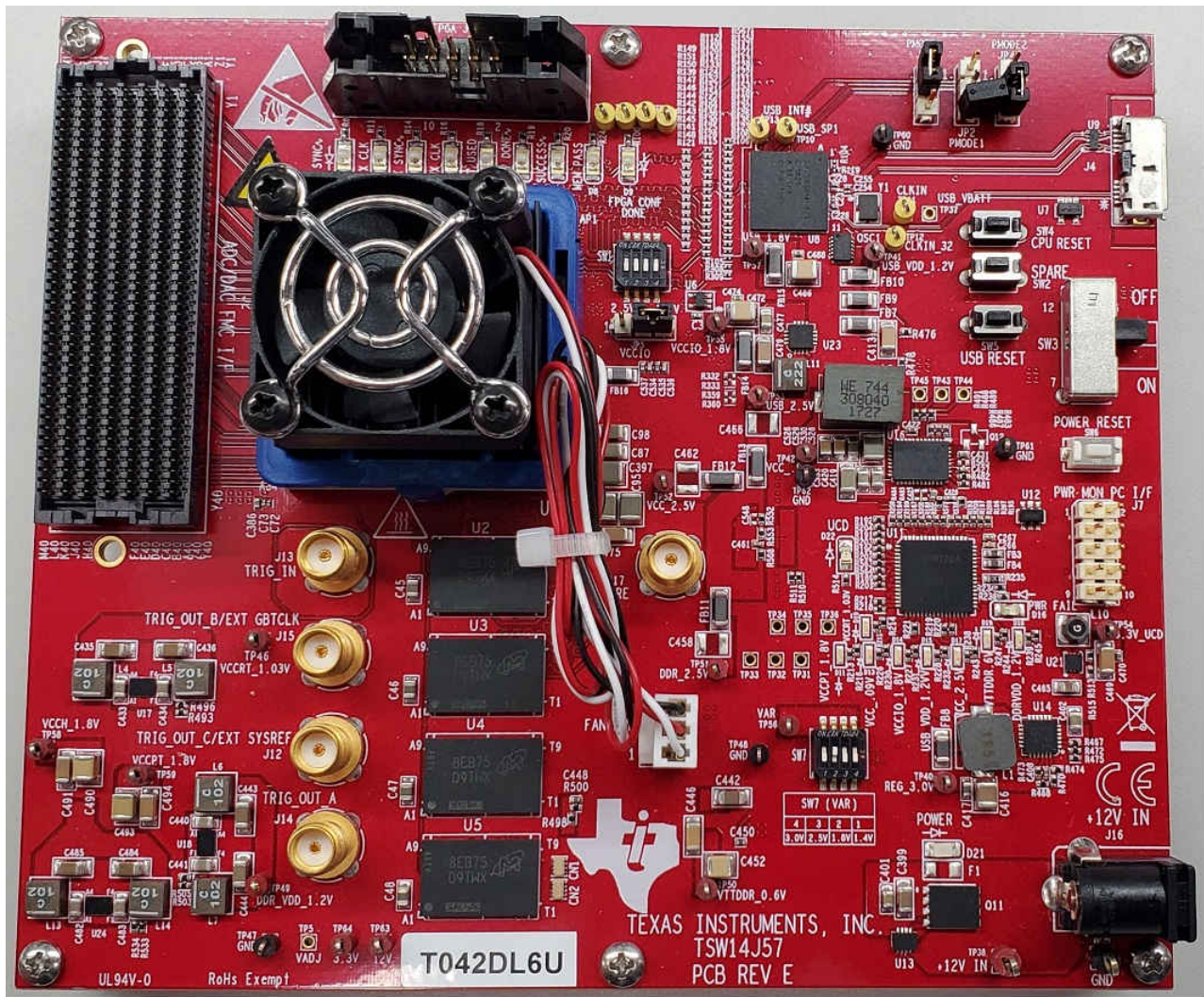
Figure 9-1. TSW14J57 EVM

9.1 Testing the TSW14J57 EVM with an ADC34J45 EVM

This section describes the operation when testing with an ADC34J45 EVM that has a JESD204B output interface.

- Power down the TSW14J57 if an ADC EVM is not installed.
- Connect J17 of the ADC34J45 EVM to connector J2 of the TSW14J57.
- Provide +5 VDC connection to J20 of the ADC34J45 EVM and +12 VDC connection to J16 of the TSW14J57 EVM.
- Connect a USB 3.0 cable to J4 of the TSW14J57 EVM and a USB 2.0 cable to J18 of the ADC34J45 EVM.
- Power up the TSW14J57 followed by the ADC EVM.
- The TSW14J57 EVM connected to an ADC34J45 EVM is shown in Figure 9-2
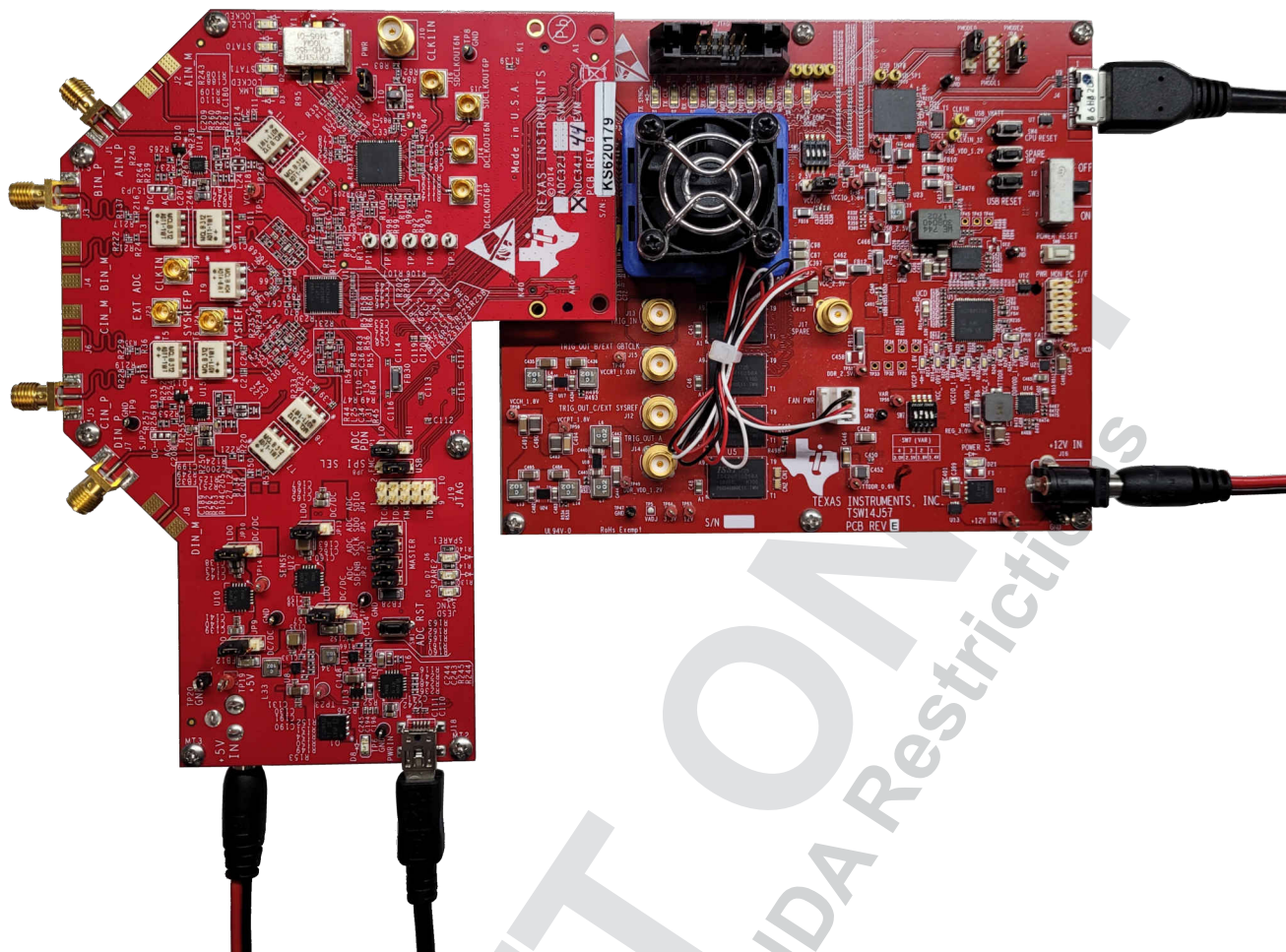
Figure 9-2. TSW14J57 EVM connected to an ADC34J45 EVM

Single Tone FFT Test

1. The evaluation of the ADC34J45 EVM requires programming the LMK04828 clock source with the correct PLL settings to provide a 160 Msps clock.
   - Open the ADC3000 GUI, and connect to the ADC34J45 EVM
   - Go to the Low Level tab and click **Load Config**
   - Browse and find the *ADC3xJxx_160MSPS_Operation_LMK_Setting.cfg*
   - Check that the PLL2 LED D4 is lit on the ADC34J45 EVM – this indicates that the PLL is programmed properly and the correct clocks are being generated
2. Start the HSDC Pro GUI program. When the program starts, select the ADC tab and then select *ADC34J4x_LMF_442* device in the *Select ADC* drop-down menu as seen in Figure 9-3.

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Figure 9-3. Select ADC34Jxx in the HSDC Pro GUI Program

3. When prompted by *Load ADC Firmware?*, select YES
4. Select Single Tone FFT Test under Test Selection
5. Select the number of sample points (and resulting number of FFT bins) to be used. The example shown in Figure 9-4 has 65536 samples.
6. Enter the ADC34J45 sampling rate. The example shown in Figure 9-4 has the sample rate set at 160 Msps
7. Enter the input frequency desired. The example shown in Figure 9-4 has the filtered input frequency set at 25 MHz and approximately –1 dBFs on the HSDC Pro FFT plot
8. Select channel 1, 2, 3, 4 depending on the channel to which the signal generator is connected
9. Press the Capture button on the HSDC Pro GUI
10. Observe an FFT result similar to that of Figure 9-4
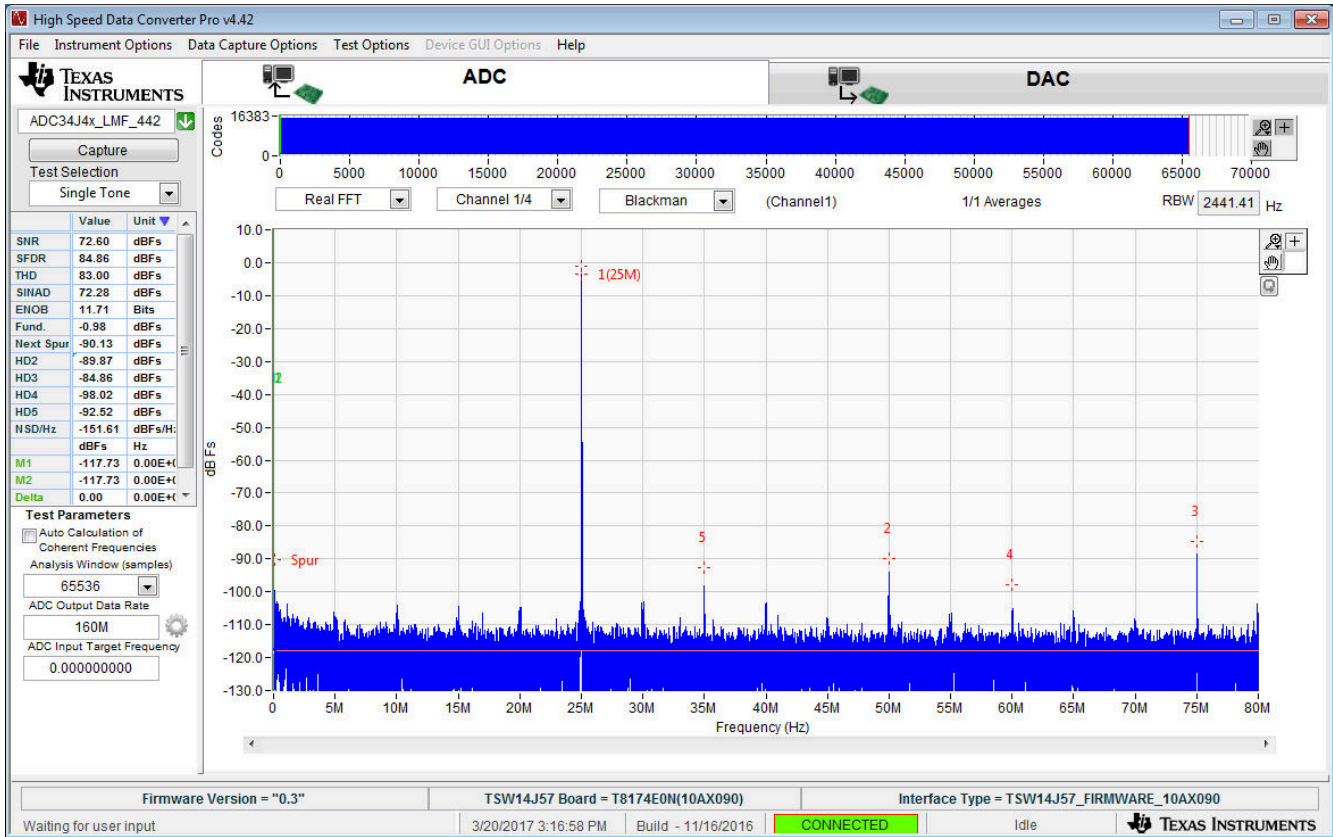
Figure 9-4. ADC34J45 Operating in 14-Bit Mode at 160 Msps with 25-MHz Input Signal

If the basic capture at this point is correct, then the front panel options of the ADC3000 SPI GUI and the front panel options of the High Speed Data Converter Pro GUI may be varied as desired to test out different device SPI options
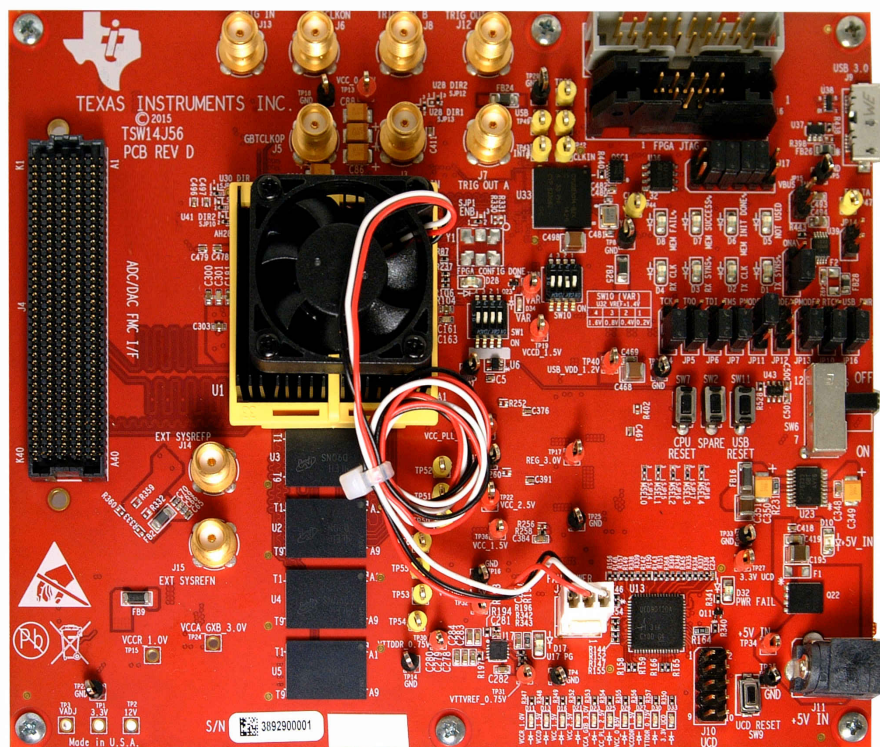
10 TSW14J56 Functional Description

HSDC Pro GUI operates with the TSW14J56 EVM, a JESD204B serial interface data capture/pattern generator platform. This EVM has a single industry standard FMC connector that interfaces directly with all TI JESD204B ADC and DAC EVMs (see Figure 10-1). When used with an ADC EVM, high speed serial data is captured and de-serialized and formatted by an Intel PSG® Arria® V GZ FPGA, then stored into an external DDR3 memory bank, enabling the TSW14J56 to store up to 512MB, 16-bit data samples. To acquire data on a host PC, the FPGA reads the data from memory and transmits it on SPI. An onboard high-speed USB-to-SPI converter bridges the FPGA SPI interface to the host PC and GUI.

In Pattern Generator Mode, the TSW14J56 generates desired test patterns for DAC EVMs under test. These patterns are sent from the host PC over the USB interface to the TSW14J56. The FPGA stores the data received into the board DDR3 memory module. The data from the memory is then read by the FPGA and transmitted to a DAC EVM across the JESD204B interface connector.

In the Instrument Options tab of the GUI, the option called "Dynamic Configuration" allows the user to change certain JESD204B parameters without loading new firmware into the FPGA. The ini files load default values for these parameters based on what ADC or DAC is selected and what mode of operation is chosen. For the most part, users should not have to change these values in this tab. If any values are changed, the default values of the ini file will be overwritten. Any changes will effect the operation of the JESD204B interface and will have to be made at both the receiver and transmit side of the interface.

Figure 10-1. TSW14J56 EVM

10.1 Testing the TSW14J56 EVM with an ADC34J45 EVM

This section describes the operation when testing with an ADC34J45 EVM that has a JESD204B output interface.

- Power down the TSW14J56 if an ADC EVM is not installed.
- Connect J17 of the ADC34J45 EVM to connector J4 of the TSW14J56.

- Provide +5 VDC connection to J20 of the ADC34J45 EVM and J11 of the TSW14J56 EVM.
- Connect a USB 3.0 cable to J9 of the TSW14J56 EVM and a USB 2.0 cable to J18 of the ADC34J45 EVM.
- Power up the TSW14J56 followed by the ADC EVM.
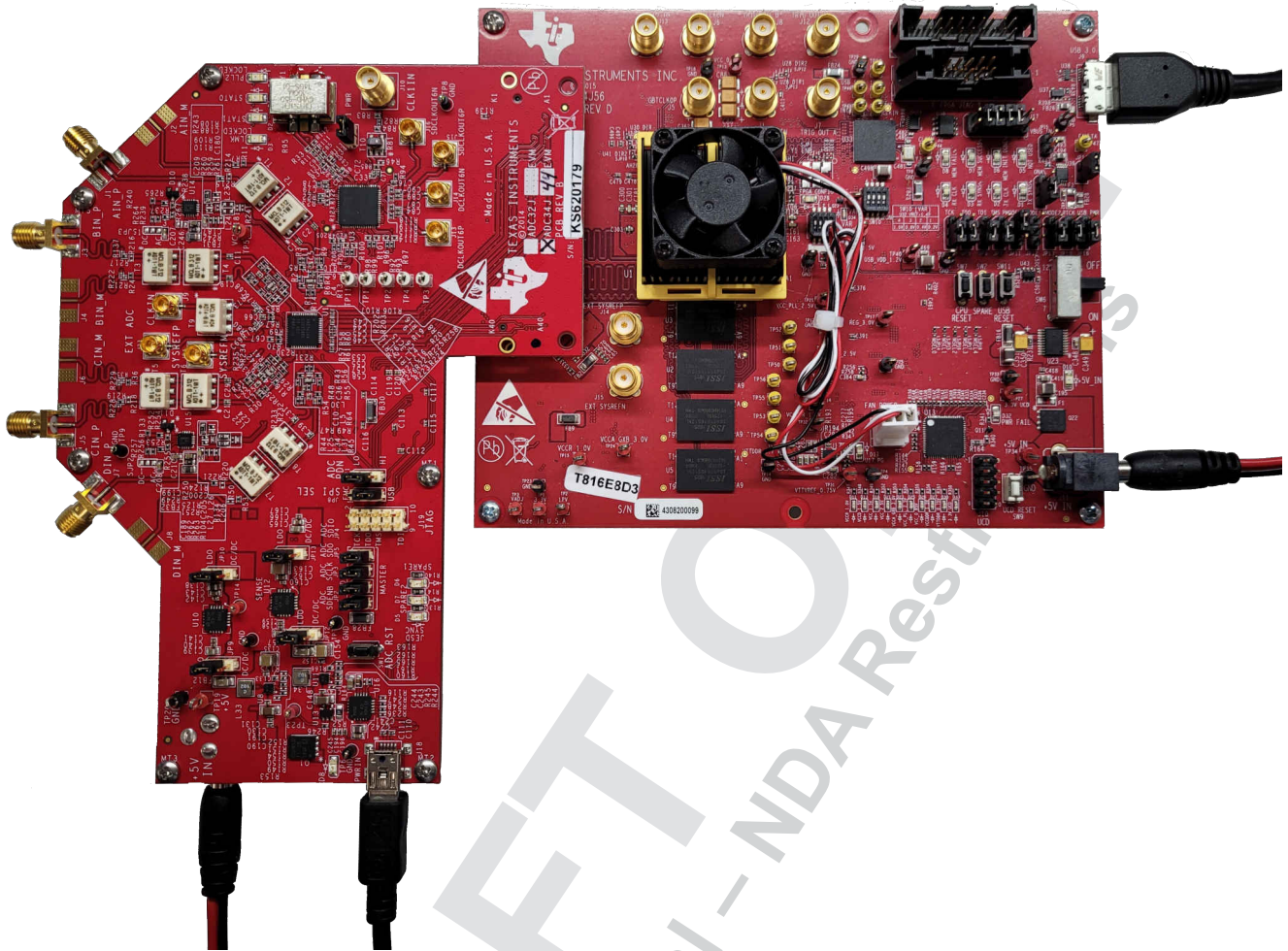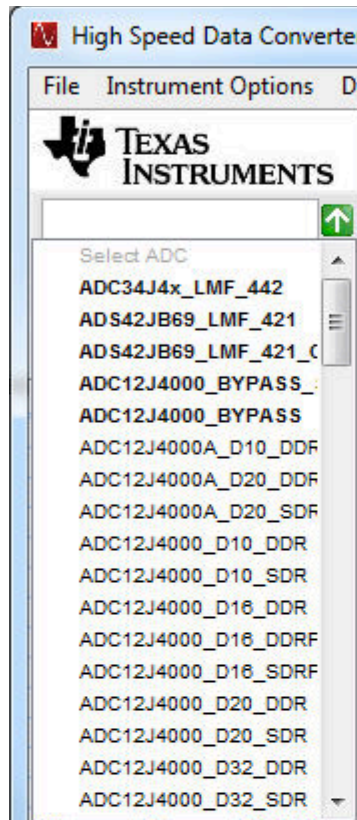- The TSW14J56 EVM connected to an ADC34J45 EVM is shown in Figure 10-2

Figure 10-2. TSW14J56 EVM connected to an ADC34J45 EVM

Single Tone FFT Test

1. The evaluation of the ADC34J45 EVM requires programming the LMK04828 clock source with the correct PLL settings to provide a 160 Msps clock.
   - Open the ADC3000 GUI, and connect to the ADC34J45 EVM
   - Go to the Low Level tab and click **Load Config**
   - Browse and find the *ADC3xJxx_160MSPS_Operation_LMK_Setting.cfg*
   - Check that the PLL2 LED D4 is lit on the ADC34J45 EVM – this indicates that the PLL is programmed properly and the correct clocks are being generated
2. Start the HSDC Pro GUI program. When the program starts, select the ADC tab and then select *ADC34J4x_LMF_442* device in the *Select ADC* drop-down menu as seen in Figure 10-3.

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Figure 10-3. Select ADC34Jxx in the HSDC Pro GUI Program

3. When prompted by *Load ADC Firmware?*, select YES
4. Select Single Tone FFT Test under Test Selection
5. Select the number of sample points (and resulting number of FFT bins) to be used. The example shown in Figure 10-4 has 65536 samples.
6. Enter the ADC34J45 sampling rate. The example shown in Figure 10-4 has the sample rate set at 160 Msps
7. Enter the input frequency desired. The example shown in Figure 10-4 has the filtered input frequency set at 10 MHz and −1 dBFs on the HSDC Pro FFT plot
8. Select channel 1, 2, 3, 4 depending on the channel to which the signal generator is connected
9. Press the Capture button on the HSDC Pro GUI
10. Observe an FFT result similar to that of Figure 10-4
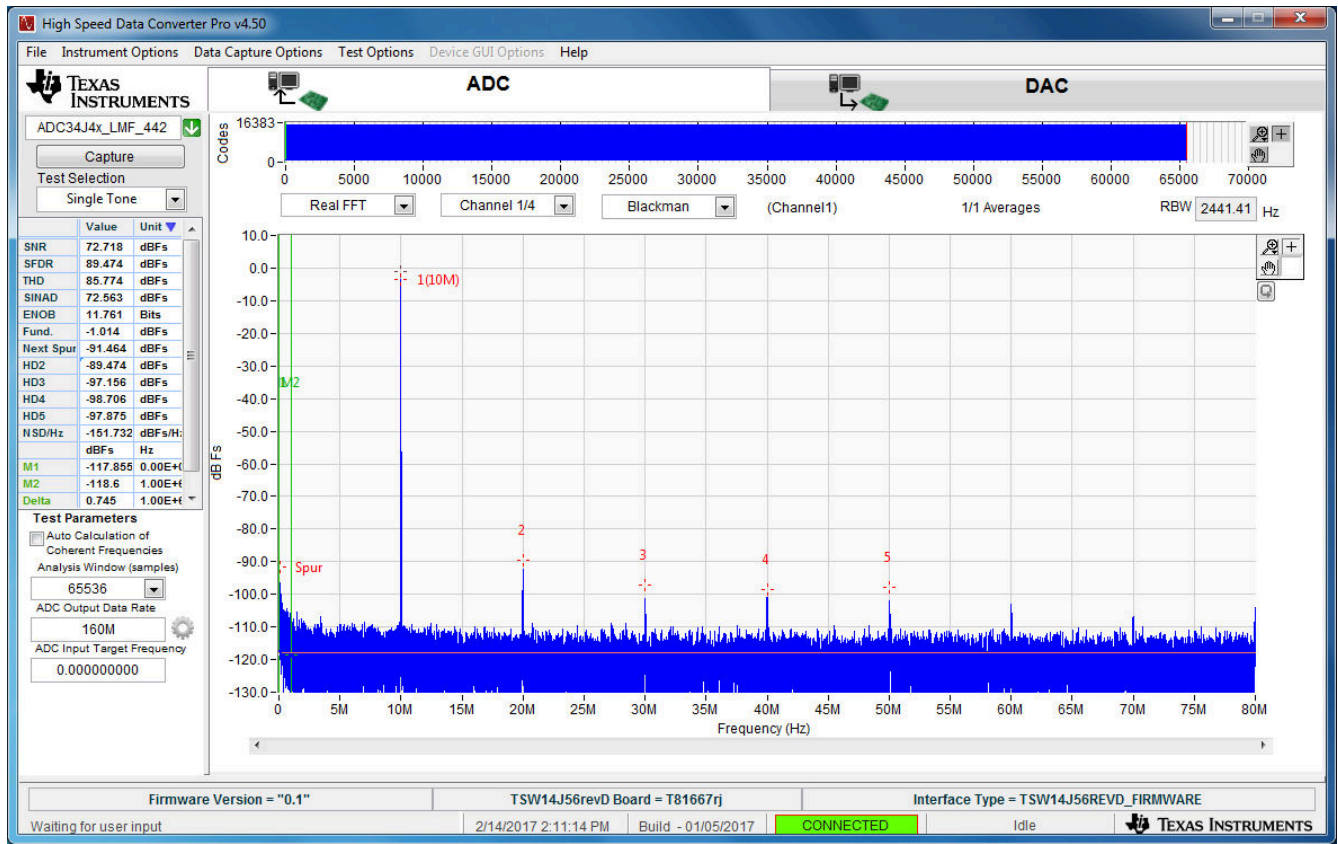
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Figure 10-4. ADC34J45 Operating in 14-Bit Mode at 160 Msps with 10-MHz Input Signal

If the basic capture at this point is correct, then the front panel options of the ADC3000 SPI GUI and the front panel options of the High Speed Data Converter Pro GUI may be varied as desired to test out different device SPI options

11 TSW14J50 Functional Description

HSDC Pro GUI operates with the TSW14J50 EVM, a JESD204B serial interface data capture/pattern generator platform. This EVM has a single industry standard FMC connector that interfaces directly with all TI JESD204B ADC and DAC EVMs (see Figure 11-1). When used with an ADC EVM, high speed serial data is captured and de-serialized and formatted by an Intel PSG Arria V GX FPGA, then stored into an external DDR3 memory bank, enabling the TSW14J50 to store up to 256MB, 16-bit data samples. To acquire data on a host PC, the FPGA reads the data from memory and transmits it on SPI. An onboard high-speed USB-to-SPI converter bridges the FPGA SPI interface to the host PC and GUI.

In Pattern Generator Mode, the TSW14J50 generates desired test patterns for DAC EVMs under test. These patterns are sent from the host PC over the USB interface to the TSW14J50. The FPGA stores the data received into the board DDR3 memory module. The data from the memory is then read by the FPGA and transmitted to a DAC EVM across the JESD204B interface connector.

In the Instrument Options tab of the GUI, the option called "Dynamic Configuration" allows the user to change certain JESD204B parameters without loading new firmware into the FPGA. The ini files load default values for these parameters based on what ADC or DAC is selected and what mode of operation is chosen. For the most part, users should not have to change these values in this tab. If any values are changed, the default values of the ini file will be overwritten. Any changes will affect the operation of the JESD204B interface and will have to be made at both the receiver and transmit side of the interface.
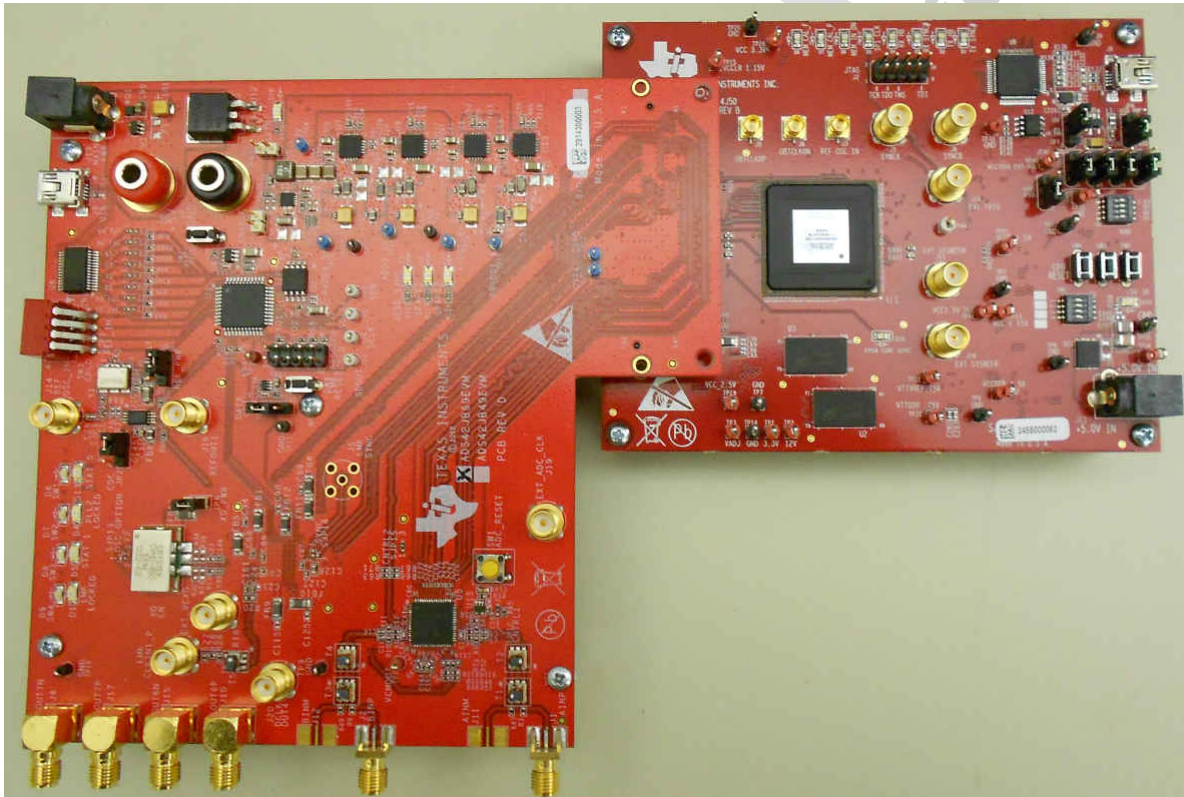

Figure 11-1. TSW14J50 EVM Connected to an ADS42JB69 EVM

11.1 Device Selection

After the board mode has been set, select the device to be tested from the device selection drop-down menu. If the GUI is in ADC mode, clicking on the drop down arrow will display the ADC options available, as shown in Figure 3-25. If in DAC mode, the list will display available DACs. The TSW14J50 device list provides a description of the JESD204B interface in the name itself. For example, if "ADS42JB69_LMF_421" is selected (see Figure 11-2), the interface parameters loaded in the FPGA will set the number of lanes to 4, the number of converters to 2, and the number of octets per frame to 1.
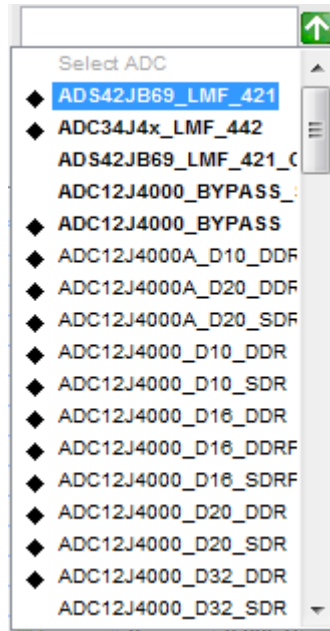
Figure 11-2. ADS42JB69_LMF_421

12 TSW14J10 Functional Description

TI's TSW14J10 Evaluation Module (EVM) allows operation of the High Speed Data Converter Pro Graphic User Interface (HSDC Pro GUI) software on certain Xilinx® and Intel PSG development kits that incorporate the FMC connector. This FMC-FMC adapter has a four-bus FTDI USB-to-GPIO device, that when connected to a PC, provides an interface to the FPGA on the development platform allowing the HSDC Pro GUI to operate as if it were connected to a TI development board. The TSW14J10 is compatible with all TI ADC and DAC JESD204B-based EVMs. Currently the software supports a limited number of ADC and DAC EVMs connected to either a Kintex® KC705 or Virtex® VC707 development card with a TSW14J10.
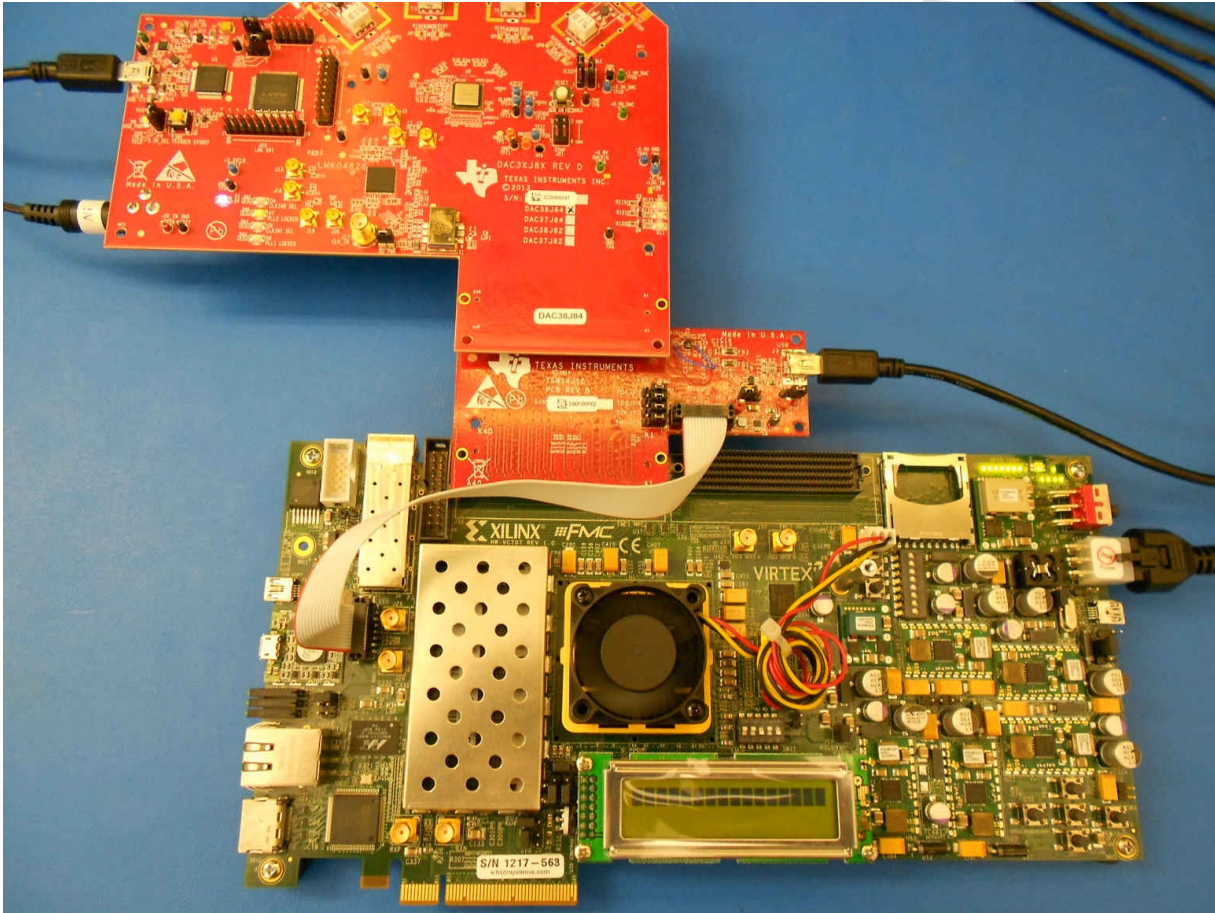
Figure 12-1. TSW14J10EVM, DAC38J84EVM, and Virtex VC707 Development Card

12.1 DAC and ADC GUI Configuration File Changes When Using a Xilinx Development Platform

The configuration files that come with the TI ADC and DAC EVM GUIs are setup to operate with the Intel-based TSW14J5xEVM. These files will work with the TSW14J10EVM when using a Xilinx platform but need a couple of changes to the settings of the LMK04828 registers. The firmware for the Xilinx Development Platforms use a separate clock input for REFCLK and Core clock. These can be the same clock under certain circumstances (when both are greater than 80 MHz and less than 165 MHz) but the firmware uses both clocks, by default, to give the maximum flexibility and support all line rates in a single design.

The REFCLK and Core clock are determined by the following lane rate conditions:

REFCLK = Lane rate / 10, and Core clock = Lane rate / 10 when Lane rate is between 1G and 3.2G

REFCLK = Lane rate / 20 and Core clock = Lane rate / 40 when Lane rate is between 3.2G and 10.3G

The ADC and DAC GUIs do not always use the same LMK04828 outputs for these two clocks. The output from the LMK04828 connected to FMC connector pins D4 and D5 will be the REFCLK. The output from the LMK04828 connected to FMC connector pins G6 and G7 will be the Core clock. Consult the EVM schematic to verify the outputs.

12.2 DAC38J84EVM GUI Setup Example

The following example shows what must be modified in the DAC3XJ8X GUI for a setup using 4 lanes, 1x interpolation, and a DAC sample rate of 368.64M.

After opening the DAC GUI, enter the parameters as shown in Figure 12-2.
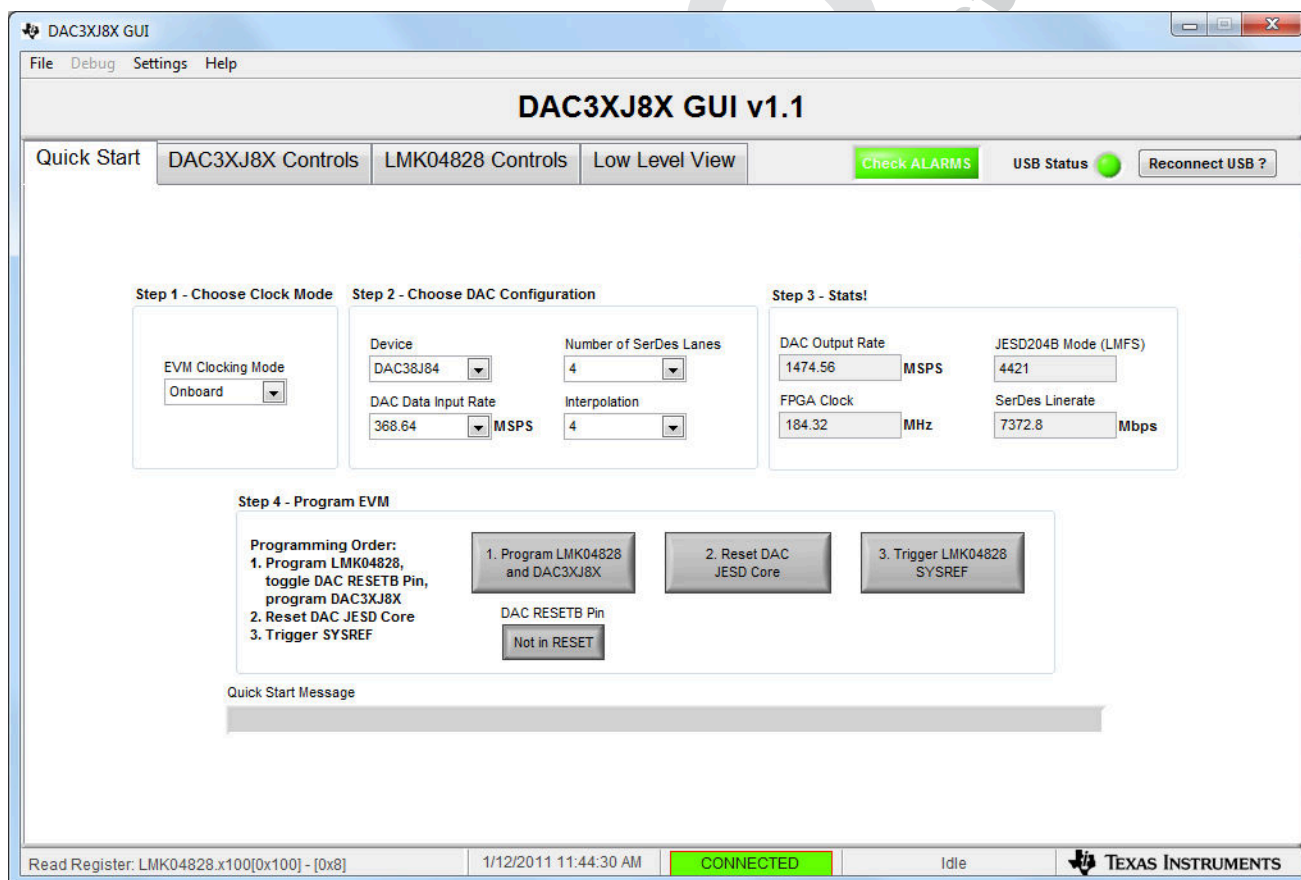
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Figure 12-2. Quick Start Menu

The GUI calculates the lane rate and displays it in the box called *SerDes Linerate*. For this example, the lane rate is 7372.8Mbps. Using the lane rate conditions in Section 12.1, REFCLK = 368.64 MHz and Core clock = 184.32 MHz.

Click on the *Program LMK04828 and DAC3XJ8X* button. After the programming has completed, click on the *LMK04828 Controls* tab. Next click on the *Clock Outputs* tab.

For the DAC3XJ8X GUI, the REFCLK is provided by *CLKout 0* and the Core clock is provided by *CLKout 12*. Notice that the default setting for *CLKout 12* is *Group Powerdown*, as shown in Figure 12-3.
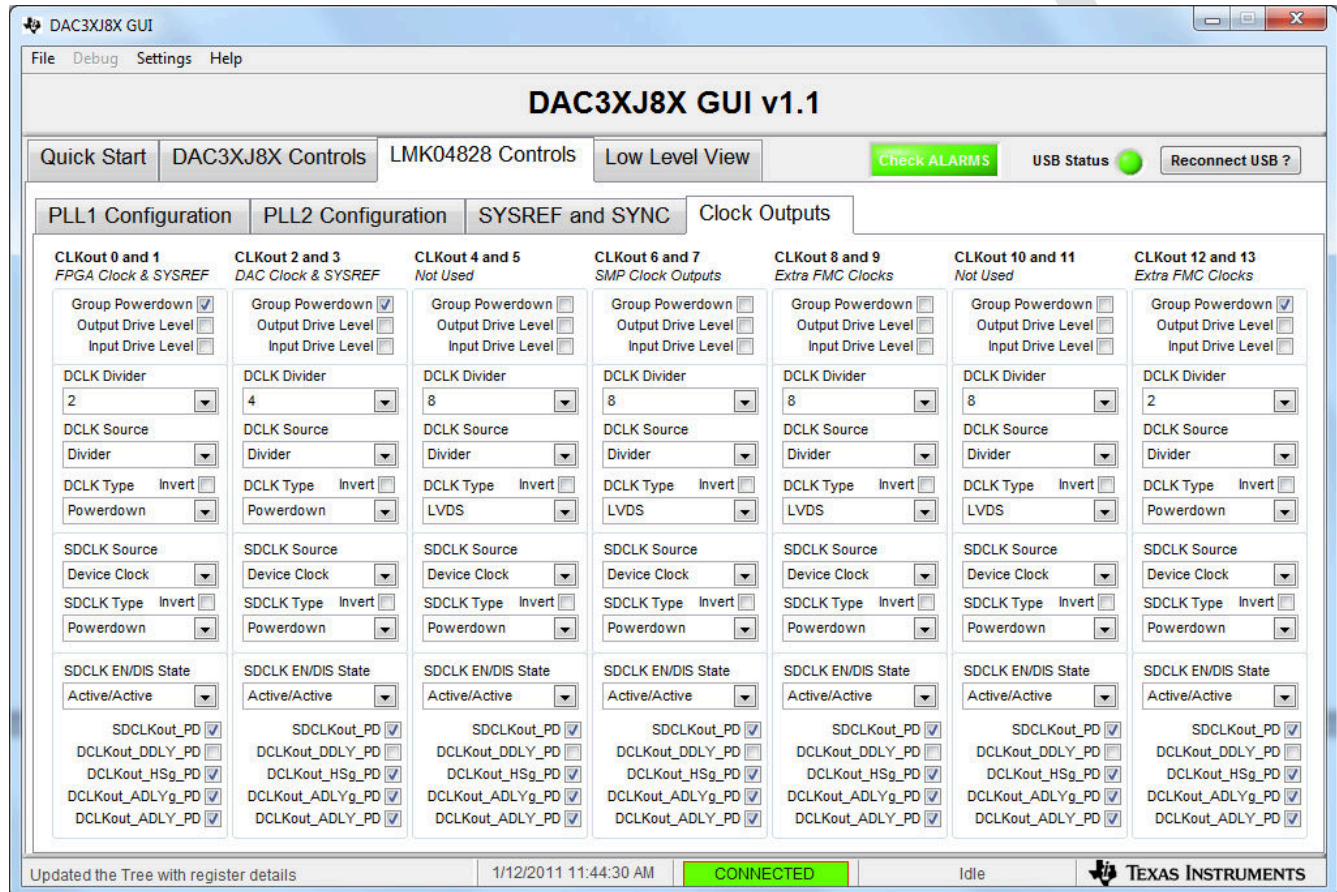
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Figure 12-3. LMK04828 Clock Outputs Menu

Since the DAC Clock is 368.64 MHz, to provide a REFCLK of 368.64 MHz, change the *DCLK Divider* for *CLKout 0* to "8".

To generate a Core clock of 184.32 MHz, set the *DCLK Divider* for *CLKout 12* to "16". Also, remove the checkmark from the *Group Powerdown* box to enable this output. The *Clock Outputs* menu is now as seen in Figure 12-4.
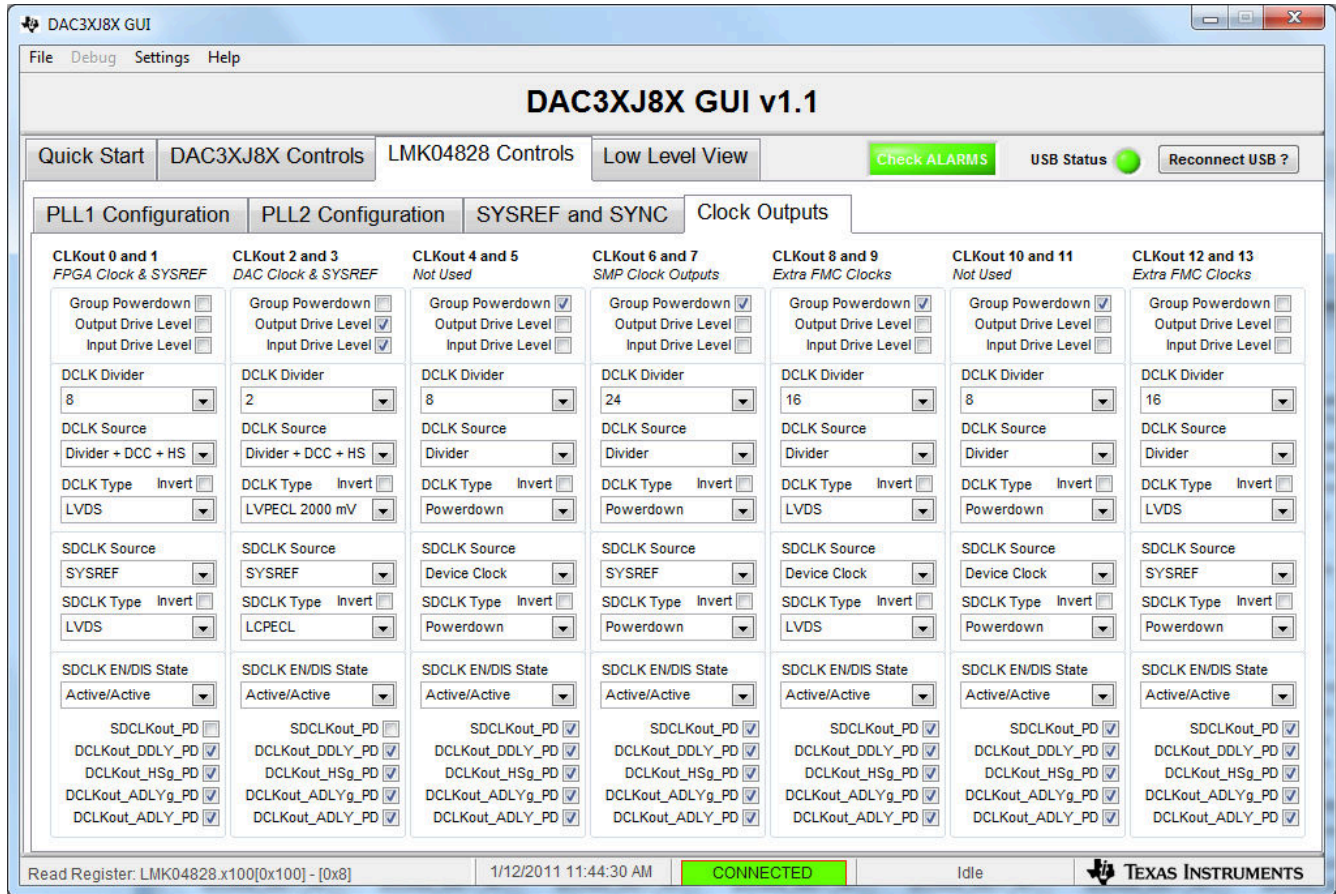
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Figure 12-4. LMK04828 Clock Outputs Menu

Open HSDC Pro GUI, select the *DAC* tab, then select *DAC3XJ84_LMF_442* in the device button. After the firmware is loaded, enter 368.64M in the *Data Rate (SPS)* window, select 2's Complement in the *DAC Option* window and generate a 10-MHz test tone using the *IQ Multitone Generator* located in the lower left of the GUI. Click on the *Create Tones* button. The display looks as shown in Figure 12-5.
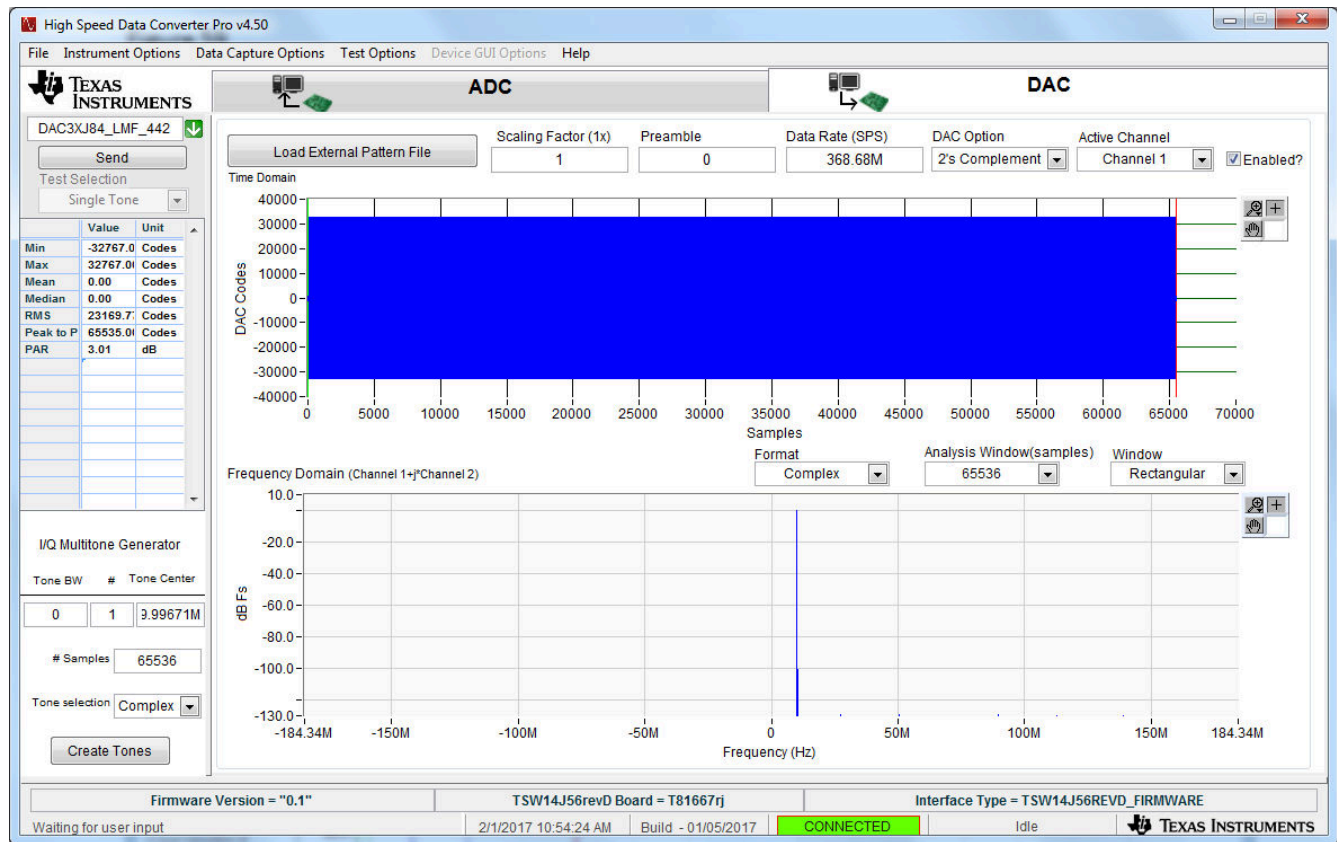
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Figure 12-5. HSDC Pro GUI

Click the *Send* button. A new window opens showing the lane rate of the interface and the required frequency of REFCLK, as shown in Figure 12-6.
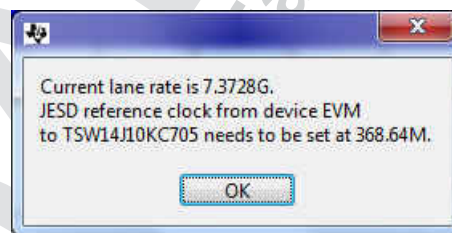

Figure 12-6. HSDC Pro GUI: Lane Rate and REFCLK Settings

Go back to the DAC GUI *Quick Start* tab and click on *Reset DAC JESD Core*. Click on *Trigger LMK04828 SYSREF*. There should now be a 10-MHz tone present at all four DAC EVM outputs.

A Signal Processing in High Speed Data Converter Pro

A.1 Introduction

The signal processing calculations in High Speed Data Converter Pro, from v2.20 are explained in the following sections.

A.2 FFT Calculation from Time Domain Data

While calculating the Real FFT, the time domain data of the current channel, along with the FFT windowing technique (Hamming, Hanning, Blackman, and Rectangular) is provided to the Intel® Signal Processing DLL, which calculates the FFT.

While calculating Complex FFT, channels are grouped into pairs of two, sequentially. Considering the channel number starting from 1, the time domain data of the odd channel is provided as the real channel data, while the time domain data of the even channel is provided for the imaginary part to calculate the Complex FFT using the Intel Signal Processing DLL.

A.2.1 FFT Window Correction Factor

Depending on the FFT windowing technique, a correction factor is applied to the entire FFT as follows:

1. Hamming – 4.01 dB
2. Hanning – 4.26 dB
3. Blackman – 5.17 dB
4. Rectangular – 0 dB

A.3 FFT Filtering

The frequency which has the maximum power is taken as the fundamental frequency. To determine the position and power of the harmonics, the maximum power value is searched around the approximate harmonic frequency, on either side of $(2 \times n + 1)$, where "n" is the number of harmonics.

Filtering is applied to the FFT based on the following user-specified values in the HSDC Pro menu option – *Notch frequency bins*.

1. Number of bins to remove on either side of fundamental
2. Number of bins to remove on either side of harmonics
3. Number of bins to remove after DC
4. Number of harmonics
5. Harmonic/Spur Power Calculation method (Integrate/Don't Integrate)
6. Custom Notch Frequencies

Depending on the FFT windowing technique, some neighboring bins on either side of the fundamental bin are excluded from notching.

The number of neighboring bins on either side of the fundamental bin excluded based on FFT windowing technique are as follows:

1. Hamming – 2
2. Hanning – 2
3. Blackman – 4
4. Rectangular – 0

When the *Harmonic/Spur Power Calculation method* is provided as *Integrate*, the above neighboring bins are also applied to the either side of harmonic frequencies, and are excluded from notching. This also controls whether to exclude these neighboring bins around harmonics in calculation of RMS noise.

The RMS noise is calculated from the FFT, excluding the fundamental and its neighboring bins (based on the FFT window), harmonics and its neighboring bins (based on GUI menu option and FFT window), and the custom notch frequencies.

RMS Noise = Square Root (Average of, Sum of Squares of each FFT value excluding the notching)

A.4 Single Tone Parameters

A.4.1 Number of Neighboring Bins for each FFT Window

The number of neighboring bins on either side of a frequency depends on the FFT windowing technique as follows:

1. Hamming – 2
2. Hanning – 2
3. Blackman – 4
4. Rectangular – 0

These neighboring bins are always included for the fundamental.

For harmonics and spurs, it is user configurable in the HSDC Pro menu option – *Notch frequency bins*. If *Harmonic/Spur Power Calculation method* is *Integrate*, the neighboring bins are included for the harmonics and spur.

If *Harmonic/Spur Power Calculation method* is *Don't Integrate*, the neighboring bins are excluded for the harmonics and spur.

A.5 Fundamental Power

The frequency which has the maximum power is taken as the fundamental frequency. The fundamental power is calculated as: the sum of the powers at the fundamental bin and its neighboring bins.

The FFT window correction factor, applied while calculating the FFT from time domain data, is subtracted from the fundamental power.

A.5.1 Harmonic Distortions

From the fundamental frequency, the approximate locations of the harmonic distortions are determined. The maximum power value is searched on either side of the approximate harmonic frequency, in the range (2 × n + 1), where "n" is the number of harmonics, for determining the position and power of the individual harmonics.

When the *Harmonic/Spur Power Calculation method* is provided as *Integrate*, the neighboring bins around the individual harmonics are included in the harmonic power calculation.

When the *Harmonic/Spur Power Calculation method* is provided as *Don't Integrate*, the neighboring bins around the individual harmonics are not included in the harmonic power calculation.

A.5.2 SNR

SNR is calculated as the difference between integrated fundamental power (fundamental power, including its neighboring bins) and the noise power.

The noise power is calculated, excluding the fundamental and its neighboring bins, harmonics, and custom notch frequencies. The neighboring bins of the harmonics are excluded if the GUI menu option - *Notch frequency bins - Harmonic/Spur Power Calculation method* is *Integrate*.

A.5.3 SFDR

SFDR is calculated from the maximum power value, excluding the fundamental, and including the harmonics.

When the *Harmonic/Spur Power Calculation method* is provided as *Integrate*, it is calculated with respect to the integrated fundamental power (i.e including the neighboring bins of the fundamental).

When the *Harmonic/Spur Power Calculation method* is provided as *Don't Integrate*, it is calculated with respect to the power of the single fundamental bin.

A.5.4 THD

Total harmonic distortions is calculated as the ratio between the fundamental power, and the square root of, sum of squares of the harmonic powers.

When the *Harmonic/Spur Power Calculation method* is provided as *Integrate*, the neighboring bins are included for both fundamental and harmonics power calculations.

When the *Harmonic/Spur Power Calculation method* is provided as *Don't Integrate*, the neighboring bins are not included for fundamental and harmonics, in the calculation of THD.

A.5.5 SINAD

SINAD is calculated from the filtered FFT data, as the ratio between the integrated fundamental power (that is, including the neighboring bins around the fundamental) to the square root of, sum of squares of the filtered FFT data.

A.5.6 ENOB

ENOB is calculated from the dBFs value of SINAD as, (SINAD – 1.76) / 6.02.

A.5.7 Next Spur

Next Spur is calculated from the maximum power value excluding the fundamental and the harmonics.

When the *Harmonic/Spur Power Calculation method* is provided as *Integrate*, Next Spur is calculated as the sum of powers of the spur and its neighboring bins, with respect to the integrated fundamental power (that is, including the neighboring bins of the fundamental).

When the *Harmonic/Spur Power Calculation method* is provided as *Don't Integrate*, Next Spur is calculated for the single bin with respect to the power of the single fundamental bin.

A.6 Two Tone Parameters

For Two Tone parameters, user-provided Input Target Frequency-1 and Input Target Frequency-2, are used for searching the frequencies F1 and F2 (50 bins on either side of the expected frequency).

The resultant frequencies are used for calculating the two tone parameters, by searching one bin before and two bins after the expected resultant frequencies.

A.7 Average FFT Calculation

From HSDC Pro v2.20, average FFT is calculated as "Power Average" (Root Mean Square method). It is calculated by taking square root, over the average of sum of squares of FFT arrays. (Each FFT array representing a single capture)

In previous versions, average FFT was calculated by normal average method (Arithmetic average of "n" FFT data arrays).

A.8 NSD Calculation

The Noise Spectral Density is calculated from the FFT, excluding the fundamental and its neighboring bins (based on the FFT window), harmonics and its neighboring bins (based on GUI menu option and FFT window), and the custom notch frequencies.

NSD = Square Root (Average of, Sum of Squares of each FFT value excluding the notching).

B Revision History

HSDC Pro GUI User's Guide (November 2013)

Created a new "High Speed Data Converter Pro GUI" User's Guide document (SLWU087) that will replace the software and operational sections of the "TSW140x High Speed Data Capture/Pattern Generator Card" User's Guide (SLWU079B).

HSDC Pro GUI Software Version 5.22 (since Version 3.1)

1. Added the ability to reload device INI files through Instrument Options menu.
2. Added IO Delay / calibration feature for adjusting delay on individual lanes for the TSW14DL3200EVM.
3. Added JESD204B Error Injection debugging feature.
4. Added the option for writing and reading to FPGA firmware registers using the FPGA Registers Write/Read option.
5. New feature for writing captured data to binary file.
6. Added feature for automatic re-arming of trigger.
7. Added phase plot for viewing phase in radian (or degree) on FFT window.
8. Added 2nd input target frequency for compatible devices under the additional device parameters menu.
9. Added # NCO Bits field for user defined NCO accuracy.
10. New histogram feature allows users to view maximum and minimum codes recorded and number of hits for any code for a capture.
11. Added the feature to highlight notched FFT bins in window.

HSDC Pro GUI Software Version 3.1 (since Version 3.0)

1. Added the feature to communicate with the Device GUI EXE from HSDC Pro EXE through back channel communication (Device GUI EXE needs to be updated with the necessary changes).
2. Implemented the new Spur Search algorithm that uses NCO and Decimation along with Fs and Fin values.
3. Updated 14J50 ADC INIs, Firmware, and DLL to support Megacore IP. TSW14J50 DLL works at 3MHz SPI baud rate for now (future version will have it increased to 30MHz).
4. Added Unit selection option to the measurement table to switch between dBF, dBc and Hz.
5. Added an option to display Time domain Y Scale in Voltage. By default the voltage range will be from -2V to 2V. The value can be specified in the Device INI by adding the parameter "Y Scale Voltage Range= -2V to 2V"
6. Added a right click shortcut option to the Real FFT graphs to display X scale in log scale.
7. Time domain graph X axis has been updated to display only integers even while zooming (earlier it was displaying floating numbers).
8. Added the option to load maximum of 512K data in the display in DAC page. (Earlier it was 64K).
9. NSD parameter in the measurement table has been updated to be displayed in dBFs/Hz (earlier it was dBFs/bin).
10. Menu option to enable or disable the NSD Marker has been added.
11. TSW14J56 DLL and Firmware has been updated to support Sysref based Trigger (for testing).
12. Added AFE5801, AFE5803, AFE5804, AFE5805, AFE5807, AFE5808, AFE5809, AFE5851_12X, ADS52J90 device and mode support to TSW1400.
13. Added ADS54J54, ADS58J8x, ADC14X250, ADC31JB68, ADC32RF45, ADS42B4, ADC12J4000_D10_SDR, ADC12J4000_D20_DDR, ADC12J4000_D32_DDR and RFDAC device and mode support to TSW14J56.
14. Removed 14J01 folder from the installer.
15. Removed TSW1400 and TSW1405 API document from the installer.
16. Removed Auto scaling for the X axis in the graph while switching between Channels or Graph types.
17. Updated the Peak to peak calculation in the measurement table using "Peak to Peak = (max code – min code) + 1" in both ADC and DAC Time domain.
18. Bug fix in handling the parameters exported from the Device GUI through Back Channel communication.
19. Bug fix in updating the Codes page with the correct data when the cursor in the context plot is moved, with the X scale in Time.
20. Bug fix in displaying the markers M1 and M2 in DAC page when the cursor is moved.

21. Bug fix in displaying the Test Parameters (Two Tone and Channel Power) when we switch between ADC and DAC tabs.
22. Bug fix in Sync pattern search in TSW1400.
23. Bug fix in applying the Bit packing pattern in DLL - TSW14J56, KC705, VC707 platforms.
24. Bug fix in handling the Parameters exported from the Plugin GUI.
25. Bug fix in updating the current values of JESD parameters in the Dynamic Configuration popup.

HSDC Pro GUI Software Version 3.0 (since Version 2.70)

1. Updated TSW14J56 firmware, DLL and INI files to support Megacore IP.
2. Added support for TSW14J10 to interface with Xilinx Virtex VC707 Board.
3. FFT Display changes (a) showing –fs/2 and fs/2 components in complex FFT (b) fs/2 and DC are not summed in Real FFT.
4. Automation functions for Import Data File, Import Binary File and DAC Scaling Factor added.
5. Export functions for the parameter GUI Channels to Disable, Channel Display Strings, and Device GUI Tab Name are added.
6. Fixed issue with the Average FFT memory buildup for large number of captures.
7. Fixed Trigger modes when the Number of Samples to capture is changed, it was not getting updated in the next immediate capture.
8. Added the feature to save the Screenshots of all channels for ADC.
9. Added support for DAC Bit masking in all the boards.
10. Retaining the DAC Scaling Factor value while Creating Tones (Earlier it was reset to 1).
11. Retaining the Last Selected ADC and DAC device name while switching between ADC and DAC tabs based on the firmware present in the board.
12. Fixed displaying the Time domain X axis scale in Time when the Channel pattern is unequal.
13. Support for skipping of Sync Pattern in TSW1400 v1.0 DLL.
14. Added HSDC Pro Manifest File – SRAS approved HTML format.

HSDC Pro GUI Software Version 2.70 (since Version 2.40)

1. Added support for TSW14J10 to interface to Xilinx KC705 Board.
2. Fix for "JTAG Broken Chain Issue" when connected to USB3 Port PC.
3. Added FFT Peak Analysis feature, which can be enabled from the menu - Test Options -> Other Frequency Options. When enabled, the dotted line present represents the threshold for peak frequency analysis.
4. HSDC Pro UI has been resized to fit 768 resolution PCs.
5. Added disabling of fundamental frequency search feature. This disables the fundamental frequency search, and allows the user to set the Fundamental frequency using the Input Target Frequency. This option is available under the menu - Test Options -> Other Frequency Options.
6. Two Tone FFT calculation has been updated to support two closely spaced tones. The integration of the nearby bins for frequency power calculation is also now applied for the Two Tone frequency parameters, based on the menu setting.
7. Fixed error in Complex FFT calculation, whose FFT result which was having an offset.
8. Added Automation function for FFT Peak Analysis and for exporting the Time Domain Parameters.
9. The fundamental frequency pointer in the FFT plot has been replaced with a single marker, which represents the integrated fundamental frequency.
10. Made changes in the TSW14J56 DLL to fix the random FTDI errors in continuous capture mode. Reduced the capture time taken by TSW14J56 board.
11. Input target frequencies now support negative frequency inputs.
12. Fixed the issue with the updating of the FFT Plot in Two channel display mode.
13. Modified the short cut menu option for exporting the FFT data from plot(right clicking on the FFT plot -> Export -> Export Data to Excel), to have the X-axis frequency values in floating point (previously they were in SI notation which was difficult for post processing using other software.
14. Modified the TSW14J56 reference clock pop up to appear when ADC Data Rate changes (instead of when pressing Capture button).

HSDC Pro GUI Software Version 2.40 (since Version 2.30)

1. Modified DAC scaling factor, which is now applied to both the data files and to the tone generated data. The scaling factor that was present near the DAC tone generation has been removed.

2. Implemented device search for ADC and DAC devices. Supports partial search – for a given input string, GUI will list all devices which has this string in any part of the device name. While searching, pressing enter/return key, will automatically select the first listed device under the search.
3. Implemented Software and Hardware Triggering in TSW1400 DAC.
4. Added automation functions - To read the ADC time domain data as a binary file, set the ADC 2nd input target frequency and functions for DAC Hardware and Software Triggering.
5. Modified the automation function architecture to execute each case and the cases they call, before starting to execute the next automation DLL command in queue.
6. Plugin GUI unloading will now happen only when the next device (ADC/DAC) is selected. When no valid device is selected, the plugin GUI tab will be hidden.
7. Added support for decoding bit packed data (no padded zeroes) in TSW14J56 ADC.
8. Support for 0s, and sample re-ordering in TSW14J56 DAC.
9. GUI Support for 16 channels devices in TSW1405.
10. Fixed issue with the updating of context plot in TSW1405, which happened when some of the channels were disabled.

HSDC Pro GUI Software Version 2.3 (since Version 2.2, November 2013)

Added support for TSW14J56 Board.

The default value for notching around harmonics has been changed to 0 for all FFT windows.

Updated Single Tone Parameters table to display the configured number of harmonic values.

When markers M1 and M2 are moved, their corresponding frequency values will be displayed.

Added automatic checking and installing of .NET 2.0 in the HSDC Pro Installer.

Fixed issue with the latest FTDI driver, which caused GUI to hang after downloading firmware in TSW1405 and TSW1406 EVM's.

Added board dynamic configuration menu item for TSW14J56, to change the device ini parameter values on the fly. User message with reference clock value has been added for TSW14J56, which will be displayed when the lane rate changes, when capture/send button is pressed.

Updated ini/firmware files of TSW14J56. TSW14J56 DAC now uses MPSSE mode.

Updated TSW14J56 Channel pattern to accept 0's (which will discard the data).

Updated the board dynamic configuration with option for "Reset", which will reload the values from the device ini file.

Added user message with reference clock value for TSW14J56, which will be displayed when the lane rate changes, when capture/send button is pressed.

Added feature of selecting the channel number to where the channel data will be displayed in GUI for TSW14J56. For example, if the DDR contains only 2 channels data, but the data needs to be displayed in channels 1, 3, then the channel pattern will be set using 1 and 3, and number of channels will be set as 4. Data read from DDR will be displayed in channels 1 and 3, and channels 2 and 4 will not have any data.

Modified lane rate calculation based on "Number of Channels" instead of JESD parameter M.

Fixed DSPLib error issue which was reported in one Windows XP PC.

Displaying the configured harmonics in the Single Tone Parameters table, with a scroll bar.

Added Automation function for setting the starting sample for the ADC Analysis window.

Fixed bug in the FFT plot, when switching to a channel with a lesser number of samples, compared to the Analysis Window length (FBRX mode).

HSDC Pro GUI Software Version 2.2 and Earlier

Version 2.2

Average FFT is now calculated by Root Mean Square method.

GUI has been optimized for faster capture time.

Added Automation functions for ADC FFT Averaging, Setting Bandwidth Integration Markers, and Channel Power Settings.

Patch 2.10.01

1. Added DAC31x1 and DAC31x4 ini files for TSW1400,TSW1406 and ADS5401-09 ini file for TSW1405.

2. Added Read/Write Register Automation functions for Plugin GUI.

Version 2.10

Added Complex FFT for ADC.

Added HSDC Pro Automation DLL, which can be used to communicate with HSDC Pro GUI from another application at \High Speed Data Converter Pro\HSDCPro Automation DLL.

Added LabVIEW, C and Matlab examples for the Automation DLL at \High Speed Data Converter Pro\HSDCPro Automation DLL.

Removed negative tone frequencies in DAC tone generation.

Renamed ADC Sampling Rate to ADC Output Data Rate.

The exact frequency values can be viewed by hovering the mouse over the respective control.

C Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (July 2015) to Revision D (March 2017)   **Page**

Changes from Revision D (March 2017) to Revision E (April 2021)   **Page**

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