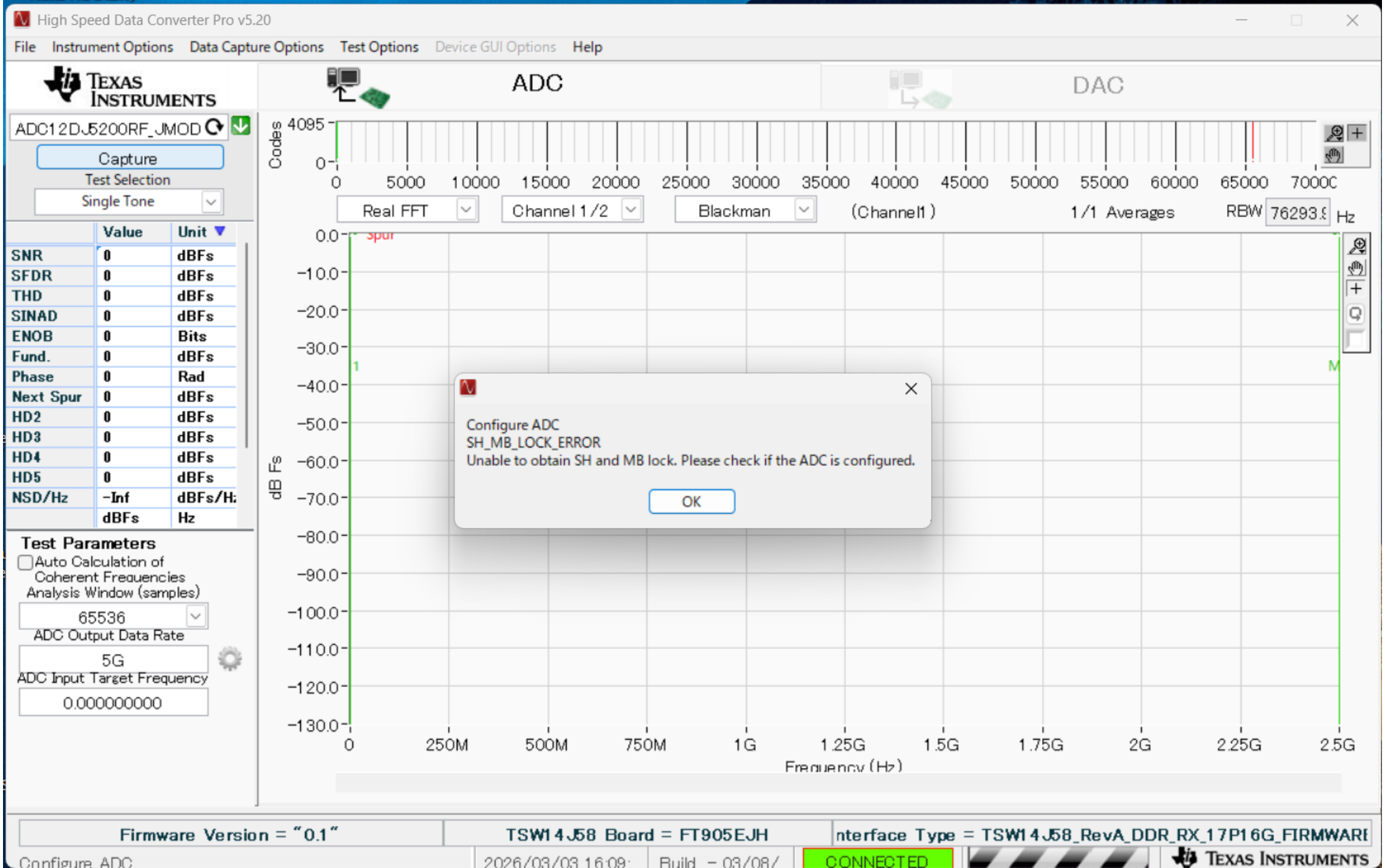
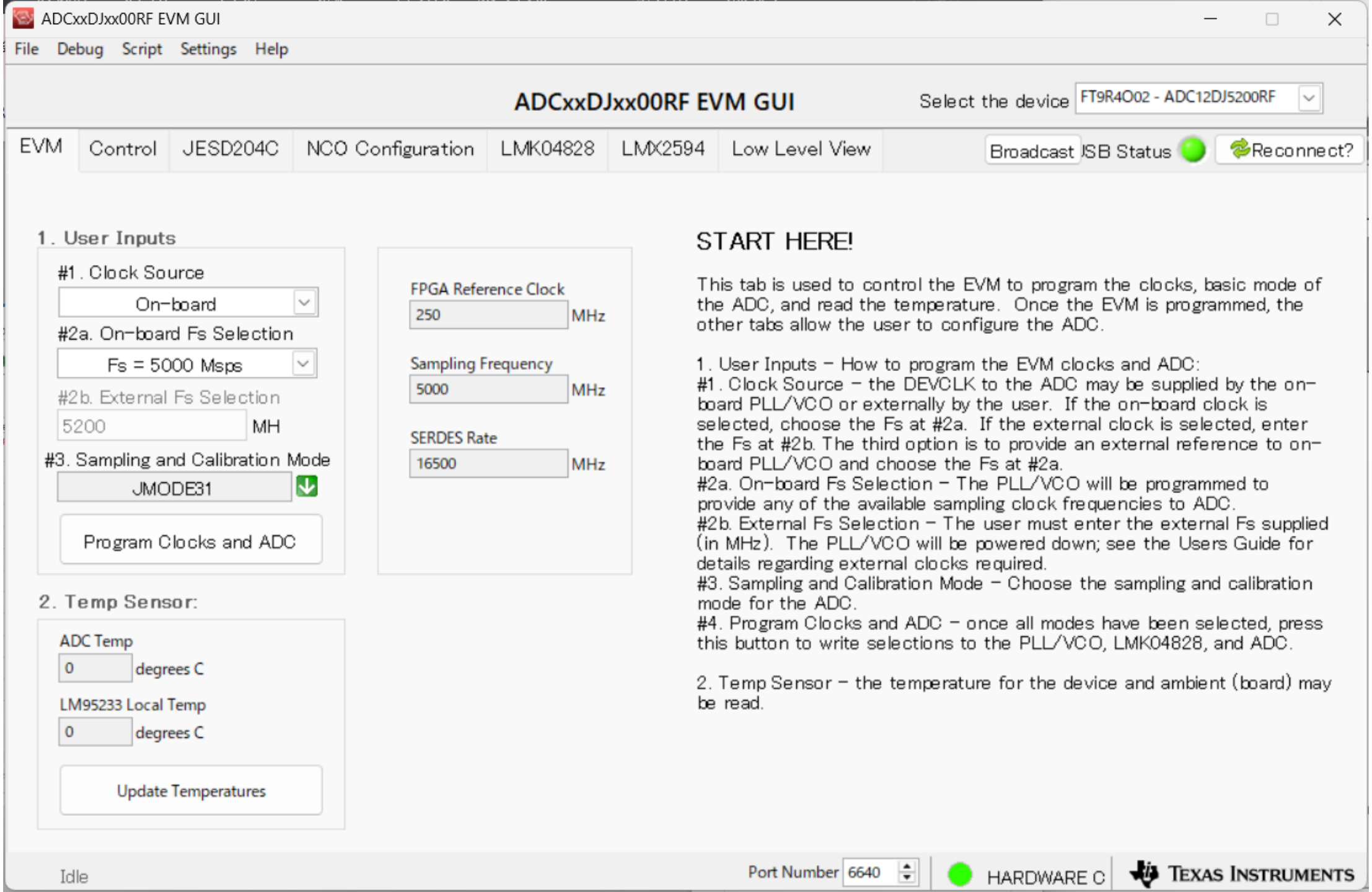
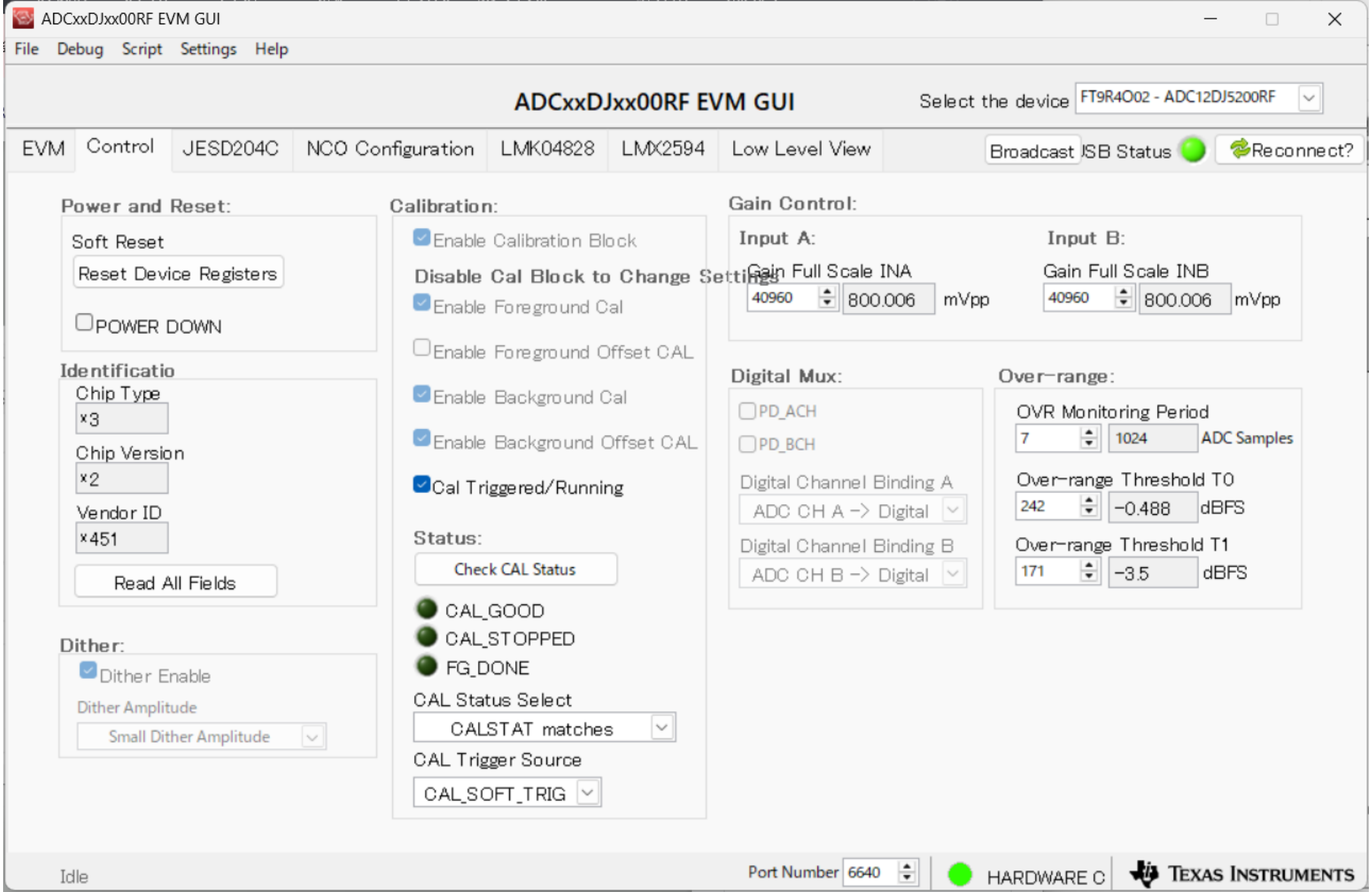
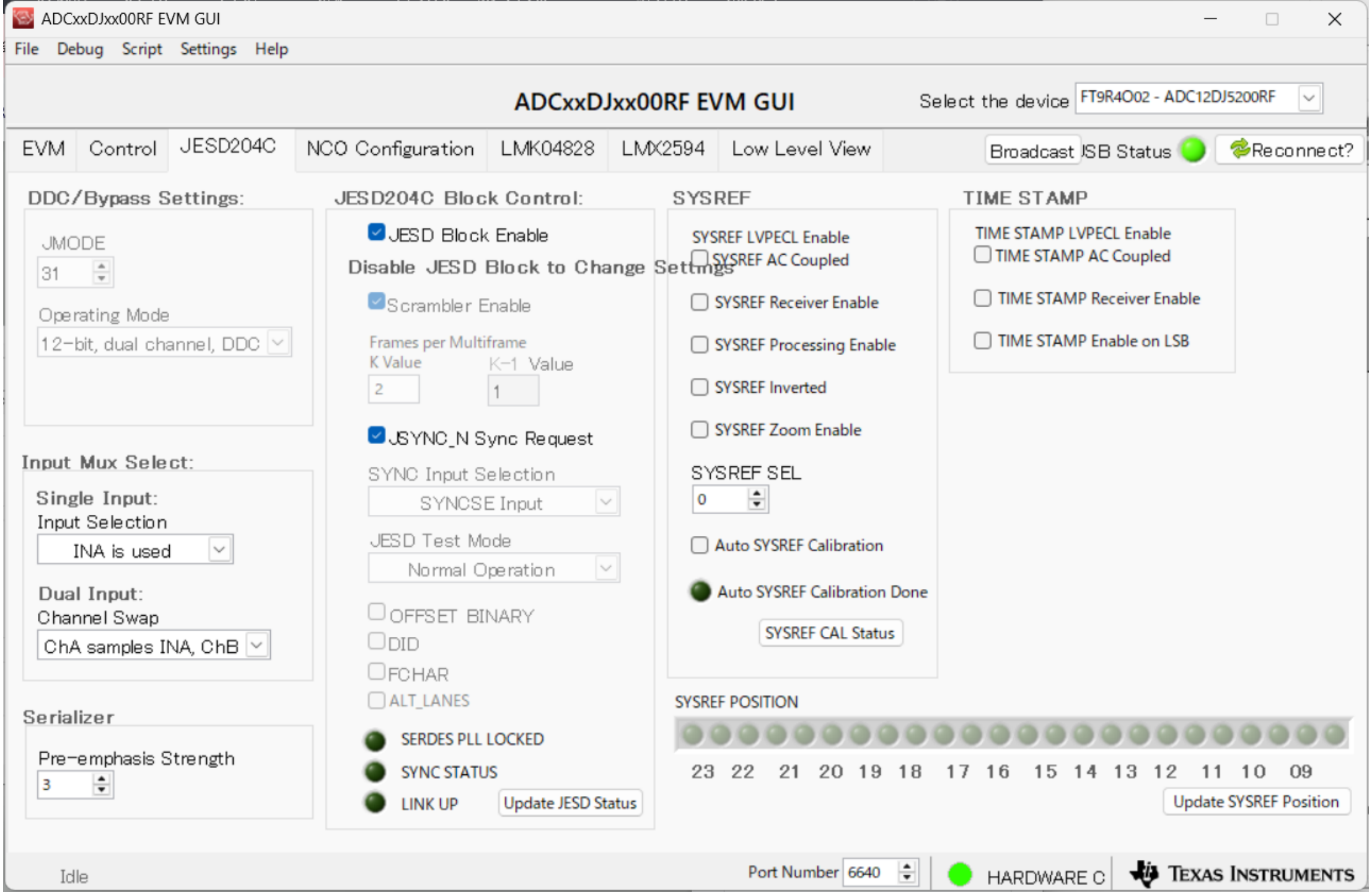

High Speed Data Converter Pro v5.20
File
Instrument Options
Data Capture Options
Test Options
Device GUI Options
Help
Texas Instruments
ADC
DAC
ADC12DJ5200RF_JMOD
Capture
Test Selection
Single Tone
Value
Unit
SNR 0 dBFs
SFDR 0 dBFs
THD 0 dBFs
SINAD 0 dBFs
ENOB 0 Bits
Fund. 0 dBFs
Phase 0 Rad
Next Spur 0 dBFs
HD2 0 dBFs
HD3 0 dBFs
HD4 0 dBFs
HD5 0 dBFs
NSD/Hz -Inf dBFs/Hz
dBFs Hz
Test Parameters
Auto Calculation of Coherent Frequencies
Analysis Window (samples)
65536
ADC Output Data Rate
5G
ADC Input Target Frequency
0.000000000
Codes
4095
0
0 5000 10000 15000 20000 25000 30000 35000 40000 45000 50000 55000 60000 65000 70000
Real FFT
Channel 1/2
Blackman
(Channel1)
1/1 Averages
RBW 76293.8 Hz
Spur
dB Fs
0.0 -10.0 -20.0 -30.0 -40.0 -50.0 -60.0 -70.0 -80.0 -90.0 -100.0 -110.0 -120.0 -130.0
0 250M 500M 750M 1G 1.25G 1.5G 1.75G 2G 2.25G 2.5G
Frequency (Hz)
Configure ADC
SH_MB_LOCK_ERROR
Unable to obtain SH and MB lock. Please check if the ADC is configured.
OK
Firmware Version = "0.1"
TSW14J58 Board = FT905EJH
nterface Type = TSW14J58_RevA_DDR_RX_17P16G_FIRMWARE
Configure ADC
2026/03/03 16:09:
Build - 03/08/
CONNECTED
Texas Instruments


ADCxxDJxx00RF EVM GUI
File Debug Script Settings Help
ADCxxDJxx00RF EVM GUI
Select the device FT9R4O02 - ADC12DJ5200RF
EVM Control JESD204C NCO Configuration LMK04828 LMX2594 Low Level View
Broadcast
SB Status
Reconnect?
1. User Inputs
#1. Clock Source
On-board
#2a. On-board Fs Selection
Fs = 5000 Msps
#2b. External Fs Selection
5200
MH
#3. Sampling and Calibration Mode
JMODE31
Program Clocks and ADC
FPGA Reference Clock
250
MHz
Sampling Frequency
5000
MHz
SERDES Rate
16500
MHz
START HERE!
This tab is used to control the EVM to program the clocks, basic mode of the ADC, and read the temperature. Once the EVM is programmed, the other tabs allow the user to configure the ADC.
1. User Inputs – How to program the EVM clocks and ADC:
#1. Clock Source – the DEVCLK to the ADC may be supplied by the on-board PLL/VCO or externally by the user. If the on-board clock is selected, choose the Fs at #2a. If the external clock is selected, enter the Fs at #2b. The third option is to provide an external reference to on-board PLL/VCO and choose the Fs at #2a.
#2a. On-board Fs Selection – The PLL/VCO will be programmed to provide any of the available sampling clock frequencies to ADC.
#2b. External Fs Selection – The user must enter the external Fs supplied (in MHz). The PLL/VCO will be powered down; see the Users Guide for details regarding external clocks required.
#3. Sampling and Calibration Mode – Choose the sampling and calibration mode for the ADC.
#4. Program Clocks and ADC – once all modes have been selected, press this button to write selections to the PLL/VCO, LMK04828, and ADC.
2. Temp Sensor – the temperature for the device and ambient (board) may be read.
2. Temp Sensor:
ADC Temp
0
degrees C
LM95233 Local Temp
0
degrees C
Update Temperatures
Idle
Port Number 6640
HARDWARE C
Texas Instruments


ADCxxDJxx00RF EVM GUI
File Debug Script Settings Help
ADCxxDJxx00RF EVM GUI
Select the device FT9R4O02 - ADC12DJ5200RF
EVM Control JESD204C NCO Configuration LMK04828 LMX2594 Low Level View
Broadcast
SB Status
Reconnect?
Power and Reset:
Soft Reset
Reset Device Registers
POWER DOWN
Identificatio
Chip Type
x3
Chip Version
x2
Vendor ID
x451
Read All Fields
Dither:
Dither Enable
Dither Amplitude
Small Dither Amplitude
Calibration:
Enable Calibration Block
Disable Cal Block to Change Settings
Enable Foreground Cal
Enable Foreground Offset CAL
Enable Background Cal
Enable Background Offset CAL
Cal Triggered/Running
Status:
Check CAL Status
CAL_GOOD
CAL_STOPPED
FG_DONE
CAL Status Select
CALSTAT matches
CAL Trigger Source
CAL_SOFT_TRIG
Gain Control:
Input A:
Gain Full Scale INA
40960
800.006
mVpp
Input B:
Gain Full Scale INB
40960
800.006
mVpp
Digital Mux:
PD_ACH
PD_BCH
Digital Channel Binding A
ADC CH A -> Digital
Digital Channel Binding B
ADC CH B -> Digital
Over-range:
OVR Monitoring Period
7
1024
ADC Samples
Over-range Threshold T0
242
-0.488
dBFS
Over-range Threshold T1
171
-3.5
dBFS
Idle
Port Number 6640
HARDWARE C
Texas Instruments


ADCxxDJxx00RF EVM GUI
File Debug Script Settings Help
ADCxxDJxx00RF EVM GUI
Select the device
FT9R4O02 - ADC12DJ5200RF
EVM Control JESD204C NCO Configuration LMK04828 LMX2594 Low Level View
Broadcast
JSB Status
Reconnect?
DDC/Bypass Settings:
JMODE
31
Operating Mode
12-bit, dual channel, DDC
Input Mux Select:
Single Input:
Input Selection
INA is used
Dual Input:
Channel Swap
ChA samples INA, ChB
Serializer
Pre-emphasis Strength
3
JESD204C Block Control:
JESD Block Enable
Disable JESD Block to Change Settings
Scrambler Enable
Frames per Multiframe
K Value
K-1 Value
2
1
JSYNC_N Sync Request
SYNC Input Selection
SYNCSE Input
JESD Test Mode
Normal Operation
OFFSET BINARY
DID
FCHAR
ALT_LANES
SERDES PLL LOCKED
SYNC STATUS
LINK UP
Update JESD Status
SYSREF
SYSREF LVPECL Enable
SYSREF AC Coupled
SYSREF Receiver Enable
SYSREF Processing Enable
SYSREF Inverted
SYSREF Zoom Enable
SYSREF SEL
0
Auto SYSREF Calibration
Auto SYSREF Calibration Done
SYSREF CAL Status
TIME STAMP
TIME STAMP LVPECL Enable
TIME STAMP AC Coupled
TIME STAMP Receiver Enable
TIME STAMP Enable on LSB
SYSREF POSITION
23 22 21 20 19 18 17 16 15 14 13 12 11 10 09
Update SYSREF Position
Idle
Port Number
6640
HARDWARE C
Texas Instruments