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### Introduction

A hardware demonstration design, targeting the UltraScale Kintex KCU105 or Zynq UltraScale+ MPSoC ZCU102 Rev 1.0 or later evaluation platforms, can be generated and exercised using the scripts, source and GUI provided in this download.

This is a complete FPGA design, incorporating transmit and receive JESD204B cores and a JESD204 PHY core containing GTH transceivers. The transceivers are setup for PMA or cable loopback to allow the operation of the JESD204B cores to be explored. The JESD204 PHY core can be dynamically configured to line rates between 1G and 12.5G.

Using Xilinx Vivado Design Suite 2017.3. This design can be implemented and can be downloaded to the KCU105 or ZCU102 evaluation board. The data output from the RX core can be monitored using Xilinx Vivado Hardware Manager.

This design is controlled using an included GUI that connects to the KCU105 or ZCU102 using Ethernet. The GUI allows the line rate, link parameters and test patterns to be dynamically changed. The GUI also supports running eyescan (KCU105 only) on the transceivers and provides a simple 2D heat map of BER results.

### **Demo Package contents**

The JESD204\_uhwd.zip file contains the following folders:

- *script* This folder contains the scripts used to generate the UltraScale Hardware Demo for the KCU105 platform.
- *hdl* This folder contains all the required source code for design blocks not sourced from the Vivado IP catalog.
- *constraints* This folder contains the design constraints required for the design.
- **sw\_src** This folder contains the source code and a pre-generated ELF files for the software running on the Microblaze processor that is included in the design.
- **GUI** This folder contains the GUI used to control this hardware demo.
- **bitstream** This folder contains pre built bitstreams for the KCU105. These bitstreams were built using the source and scripts from this demo.

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**Overview of the KCU105 Hardware Demonstration Design** 



Figure 1 UltraScale Hardware Demonstration Design

Figure 1 illustrates the KCU105 UltraScale hardware demonstration design which consists of the following:

- JESD204 Subsystem
  - Transmit JESD204B core.
  - Receive JESD204B core.
  - JESD204B PHY core. This allows the transceivers to be shared between the transmit and receive JESD204B cores.
  - Data Interface. This custom IP enables playback and capture of data through the JESD204B cores.
  - o AXI DMA. This provides DMA access to DDR4 memory for playback and capture of data.
  - Monitor Block. This custom IP is used to de-map the received data into sample data which can then be monitored using an ILA in the Vivado Hardware manager.

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- IO Block. This custom IP is used to provide IO buffers and is also used to generate CORECLK and SYSREF from the externally supplied REFCLK.
- Microblaze Subsystem
  - Microblaze Processor.
  - AXI Lite Peripheral Interconnect structure.
  - AXI IIC. This is used to control the SI570 programmable oscillator on the KCU105. This oscillator is used to supply REFCLK to the JESD204B Subsystem.
  - $\circ$   $\;$  AXI UART. This can be used for development / Debug.
  - $\circ~$  AXI Timer. This timer is required by the TCP protocol implementation of the LwIP software stack.
  - AXI SPI. Unused in this demo design.
- Ethernet Subsystem
  - AXI 1G/2.5G Ethernet Subsystem. This IP is configured for 1G and uses SGMII to communicate with the Ethernet Phy on the KCU105.
  - $\circ$  AXI DMA. This provides DMA access to memory for the AXI Ethernet Subsystem.
- Memory Subsystem
  - MIG. This block provides the DDR4 Memory interface. The local bus is 512bits wide and runs at 300MHz which equates to a memory clock of 1.2GHz for the DDR4 memory. The MIG core is also used to generate the 142MHz clock used to drive the MicroBlaze processor and the AXI peripherals as well as a 25Mhz clock for the DRP interface on the transceivers.
  - AXI interconnect. This is a multi-layered structure to separate and optimise the routing and resources used by the two data bus structures (512bit 300MHz and 32bit 150Mhz).
  - Block Rams for processor memory and buffer descriptor memory for the JESD204 block AXI DMA.

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Figure 2 UltraScale Hardware Demonstration Design

Figure 2 illustrates the ZCU102 UltraScale+ MPSoC hardware demonstration design which consists of the following:

- JESD204 Subsystem
  - Transmit JESD204B core.
  - Receive JESD204B core.
  - JESD204B PHY core. This allows the transceivers to be shared between the transmit and receive JESD204B cores.
  - Data Interface. This custom IP enables playback and capture of data through the JESD204B cores.
  - AXI DMA. This provides DMA access to DDR4 memory for playback and capture of data.
  - Monitor Block. This custom IP is used to de-map the received data into sample data which can then be monitored using an ILA in the Vivado Hardware manager.
  - IO Block. This custom IP is used to provide IO buffers and is also used to generate CORECLK and SYSREF from the externally supplied REFCLK.
- ZYNQ UltraScale+ MPSoC
  - ARM R5 Processor.

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- $\circ$   $\;$  AXI UART. This can be used for development / Debug.
- $\circ~$  AXI Timer. This timer is required by the TCP protocol implementation of the LwIP software stack.
- o Ethernet
- $\circ~$  Block Rams for processor memory and buffer descriptor memory for the JESD204 block AXI DMA.
- Sample BRAM Subsystem
  - AXI interconnect. This is a multi-layered structure to separate and optimise the routing and resources used by the two data bus structures (512bit 300MHz and 32bit 150Mhz).

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## **Generating the Hardware Demonstration Design**

All the files required to create the hardware demonstration design are located in the download. The following steps must be carried out to successfully generate the hardware demo project.

- 1) Unzip and open the hardware demo folder.
- 2) Open Vivado and confirm the version is 2017.3
- 3) Change the Vivado working directory to the root of the unzipped folder. Changing directory in Vivado is achieved by simply typing "cd <directory>" at the tcl console.
- 4) Choose to build for either KCU105 or ZCU102 by typing either of the following in the vivado tcl console:

```
set BOARD "KCU105"
```

Or

set BOARD "ZCU102"

5) Type the following in the tcl console "source ./script/build\_it.tcl" This will run the main script that builds the design.

The build\_it.tcl script does the following:

- a) Creates a new Vivado project for the design.
- b) Creates projects for the included hdl blocks and packages them as IP for use in the IPI block diagram of main design.
- c) Builds the design in IPI.
- d) Synthesizes the design.
- e) Implements the design.
- f) Generates bitstream's for the designs.

For the KCU105 two bitstream are generated:

"KCU105\_XLOOP\_STATIC.bit" which has the Ethernet interface set to use a static IP address.

**"KCU105\_XLOOP\_DHCP.bit"** which has the Ethernet interface set to accept an IP address from a DHCP server. See <u>Setup Ethernet Interface</u> later in this document for detailed instructions.

For the ZCU102 a single bitstream "**mySystem\_wrapper.bit**" is generated. The choice between static and dynamic IP address is made when you choose which software to download and run on the ARM processor in the design.

After running the build\_it.tcl script two new folders will have been created.

local\_IP\_<BOARD>\_XLOOP

This folder contains:

- The projects that were created to package the RTL blocks from the hdl directory into IP for use in IP Integrator.
- A repository containing all the packaged IP blocks.
- prj\_<BOARD>\_XLOOP

This folder contains the Vivado project for the BOARD that has been built.

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## **Running the Hardware Design Using Vivado**

### **Prerequisites for Running the Demonstration**

- KCU105 or ZCU102 Evaluation Platform
- Vivado 2017.3 toolset
- Micro-USB cable for USB JTAG connection
- Micro-USB cable for USB UART connection
- Ethernet Cable

### **Setup Ethernet Interface**

A choice must be made on how to run the demo based on your local network and any relevant security policies. The choices are detailed as follows:

- Static IP address. With static IP address the design running on the BOARD is configured to
  use an IP address of 192.168.1.10 and a subnet mask of 255.255.255.0. In this setup, it is
  expected that the BOARD is directly connected to your PC and not to local network
  connection. See <u>Setup for Static IP address</u>. Note: If a network is available and it contains a
  DHCP server then it is recommended to use Dynamic IP Address over Static IP address.
- Dynamic IP Address. With Dynamic IP address, the design running on the BOARD is configured to communicate with a DHCP server to request an IP address and subnet mask. See <u>Setup for Dynamic IP Address</u>.



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#### **Setup for Static IP address**

- Connect an Ethernet cable between the Ethernet port on the host PC and the RJ45 Ethernet port on the BOARD.
- Set the host PC to use the wired Ethernet port and configure an IP address of 192.168.1.1

This can be achieved as follows:

Open the "Networks and Sharing Center" from "Control Panel"

😋 😔 🗢 😫 🕨 Control Panel 🕨	All Control Panel Items      Network and Sharing Center	l 🔎
Control Panel Home Manage wireless networks Change adapter settings Change advanced sharing settings	View your basic network information and set up connections           Image: Imag	ect .
	Vinx.xuinx.com     Access type:     Internet       Domain network     Connections: <ul> <li>Connections:</li> <li>Local Area Connection 3</li> </ul> <ul> <li>Vinidentified network</li> <li>Public network</li> <li>Access type:</li> <li>No network access</li> <li>VirtualBox Host-Only Network</li> </ul>	k
	Change your networking settings	int.
See also HomeGroup Internet Options Windows Firewall	Choose homegroup and sharing options Access files and printers located on other network computers, or change sharing settings. Troubleshoot problems Diagnose and repair network problems, or get troubleshooting information.	

Figure 3 Network and Sharing Center

Click on "Change adapter settings" Highlighted yellow in Figure 3



Figure 4 Network Connection Right click on your "Local Area Connection" icon and choose properties



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🕌 Local Area Connection 3 Properties 🛛 🔯	Internet Protocol Version 4 (TCP/IPv4) Properties
Networking Sharing	General
Connect using:	You can get IP settings assigned automatically if your network supports this capability. Otherwise, you need to ask your network administrator for the appropriate IP settings.
Configure This connection uses the following items:	Obtain an IP address automatically     O     Use the following IP address:
<ul> <li>✓ Intervention Microsoft Networks</li> <li>✓ Intervention Bridged Networking Driver</li> </ul>	IP address: 192.168.1.1
<ul> <li>✓ □ QoS Packet Scheduler</li> <li>✓ □ □ File and Printer Sharing for Microsoft Networks</li> </ul>	Subnet mask: 255 . 255 . 0
	Obtain DNS server address automatically
Link-Layer Topology Discovery Responder	Use the following DNS server addresses:
Install Uninstall Properties	Preferred DNS server:
Description Transmission Control Protocol/Internet Protocol. The default	Alternate DNS server:
wide area network protocol that provides communication across diverse interconnected networks.	Validate settings upon exit
OK Cancel	OK Cancel

Figure 5 TCP/IPv4 properties

Then edit the Properties for "Internet Protocol Version 4 (TCP/IPv4)" as shown in Figure 5.

OK all the changes.

Notes:

- You may need to temporarily disable any wireless networking interfaces.
- You may need to temporarily disable any firewall that may be used on your PC network interface.

#### **Setup for Dynamic IP Address**

• Connect an Ethernet cable between the Ethernet port on your local network and the RJ45 Ethernet port on the BOARD.

Notes:

- Do not connect directly your PC.
- The BOARD, the DHCP server and your PC must all be on the same network.
- You may need to temporarily disable any firewall that may be used on your PC network interface.

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### **Configuring the FPGA KCU105**

- Connect a USB port on the host PC to the USB-JTAG port on the evaluation board.
- Connect a USB port on the host PC to the USB UART port on the evaluation board. See the KCU105 User guide for details about the Silicon Labs CP2105GM dual USB-to-UART Bridge interface on the KCU105. You must ensure the Silicon Labs drivers are installed.
- Configure a terminal application (Tera Term, Hyperterm, PuTTY etc) to communicate with the COM port assigned to the Silicon Labs CP210x standard interface as shown in Figure 6.



#### Figure 6 Status console UART Setup

- Power up the evaluation board.
- Open the Vivado Hardware Manager from the Flow Navigator in the project that was built.
- Open a new hardware target
- Select the targeted FPGA, and click on next. Leave all other options on the default values.
- Right click on the device that should have appeared in the GUI and select '*program device*' from drop down menu.
- Locate the bitstream file. Two bitstream files will have been generated. You must choose the correct file based on your chosen network configuration (Static IP or DHCP assigned).
  - 1. ./prj\_MyKcu105\_XLOOP/prj\_MyKcu105\_XLOOP.runs/impl\_1/KCU105\_XLOOP\_STATIC.bit
  - $2. \ ./prj_MyKcu105\_XLOOP/prj_MyKcu105\_XLOOP.runs/impl\_1/KCU105\_XLOOP\_DHCP.bit$
- Click ok. This action will program the device.
- After programming completes. The on board firmware will negotiate the Ethernet link speed and initialise the platform.
- Take note of the BOARD IP address output from the UART to the status console (see Figure 7). This IP address must be used when connecting with the GUI.



Figure 7 Board IP Address

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### **Configuring the FPGA ZCU102**

- Connect a USB port on the host PC to the USB-JTAG port on the evaluation board.
- Connect a USB port on the host PC to the USB UART port on the evaluation board. See the ZCU105 User guide for details about the Silicon Labs CP2108 Quad USB-to-UART Bridge interface on the ZCU102. You must ensure the Silicon Labs drivers are installed.
- Configure a terminal application (Tera Term, Hyperterm, PuTTY etc) to communicate with the COM port assigned to the Silicon Labs CP210x Uart Bridge interface 0 as shown in Figure 8.

	Reconfiguration		
	Category:		
	Session	Options controlli	ng local serial lines
	Logging	Configure the serial line	
	Keyboard	Speed (baud)	115200
	Bell	Data bits	8
	- Features	Charle	1
	Appearance	Stop bits	
	- Behaviour - Translation	Parity	None
File Action View Help	Selection	Flow control	XON/XOFF -
	- Colours		
Intel/(2) Ethernat Connection (2) 1210 I.M.	Serial		
▲ TP Ports (COM & LPT)			
Communications Port (COM1)			
ECP Printer Port (LPT1)			
Intel(R) Active Management Technology - SOL (COM3)			
Silicon Labs Quad CP210X USB to UART Bridge: Interface 0 (COM27)			
- TSilicon Labs Quad CP210x USB to UART Bridge: Interface 2 (COM26)			
Silicon Labs Quad CP210x USB to UART Bridge: Interface 3 (COM28)			
Processors			Apply Cancel
			Calicer

Figure 8 Status console UART Setup

- Power up the evaluation board.
- Open the Vivado Hardware Manager from the Flow Navigator in the project that was built.
- Open a new hardware target
- Select the targeted FPGA, and click on next. Leave all other options on the default values.
- Right click on the device that should have appeared in the GUI and select 'program device' from drop down menu.
- Locate the bitstream file. A single bitstream file will have been generated.
- Click ok. This action will program the device.
- After programming completes. Procede to downloading the SW to the ARM processor using the SDK.

### **Download software to ZCU102 using SDK**

- Ensure the FPGA has been programmed successfully using the instructions for configuring the FGPA ZCU102 in this document.
- Launce the SDK from the file menu in Vivado.

•

- Once the SDK is open you should see two prebuild app projects with associated bsp projects
  - 1. "uhwd\_static" Containing the ARM software built with a static IP address
  - 2. "uhwd\_dhcp" Containing the ARM software built to obtain an IP address from a DHCP server.
- Select one or other of the app projects and chose "Run Configurations" from the "Run" menu.

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- When the run configurations dialog appears choose "Run or Debug program using system debugger"
- When the system debugger pane opens ensure to select "Reset RPU" and "PL Powerup" as shown in Figure 9

		Run Configurations			×
Create, manage, and run configuration Run or Debug a program using System De	<b>15</b> ebugger.				
Image: Type filter text         Image: Type filter text	Name: System Debug Target Setup Debug Type: Stande Connection: Local Hardware Platform: Bitstream File: Initialization File: FPGA Device: PS Device:	ger using Debug_uhwd_dhcp.elf on Local application @ Arguments Environment & Symbol Files & signal files & sig	Source & Path Search Search Select Select	Map Commo	Generate
C m >	Reset entire syste     Reset APU     Reset RPU     Enable RPU Split     Program FPGA     Run psu_init     PL Powerup	Summary of operations to be performed Following operations will be performed before launchi 1. Resets and clears RPU reset. 2. Enables RPU split mode (Default mode is lock-step). 3. Runs psu_init to initialize PS. 4. Request trigger for PL powerup and reset. Required 5. The following processors will be reset and suspende 1) psu_cortexr5_0 6. All processors in the system will be suspended, and. following processors as specified in the Applications ta 1) psu_cortexr5_0 (/Sandbox/hughw/IP3_hughw.grou uhwd_2017_3/pri_ZCU102_XLOOP/pri_ZCU102_XLOOP.	ng the debugge after programn d. Applications wi b. sdk/uhwd_stati	er. ning FPGA. II be downloader (wired/jesd204_j (/Debug/uhwd_s	d to the platforms/ static.elf)
2				Close	Run

#### Figure 9 Run Configurations

- Hit Apply then Run.
- Take note of the BOARD IP address output from the UART to the status console (see Figure 10). This IP address must be used when connecting with the GUI.

	🛃 COM27 - PuTTY		ľ
	UltraScale Hardware Demo for JESD204B	*	
	SW Version 3.0.000		
	For Vivado 2017.3		
	Start PHY autonegotiation	=	l
1	Waiting for PHY to complete autonegotiation.		
1	autonegotiation complete		
)	link speed for phy address 12: 1000		
	Board IP: 149.199.131.159		
3	Netmask : 255.255.255.0		
ļ	Gateway : 149.199.131.254		
1	UHWD Jesd IP server started @ port 80		
1		Ŧ	

Figure 10 Run Configurations

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### Monitoring the Device in the Vivado Hardware Manager

Once the device has been configured three entries will appear in the Vivado GUI under the device (SysMon, hw\_ila\_1, MIG\_1(KCU105 only)).

On the KCU105. The MIG\_1 Tab will be open by default. This should show successful calibration of the DDR4 memory. Double click on the SysMon entry and select all the check boxes in the New Dashboard dialog box that appears as, shown in Figure 11. This will create a dashboard that contains the FPGA System Monitor and the hw\_ila\_1 signals. The Run Trigger button can be pressed at any time to observe the data that is coming from the JESD204B receive core. There should also be a SysMon entry showing the temperature of the FPGA.

r	New Dashboard 🛛 🗙
Specify dashbo	the name and contents for a new 🛛 🗼
<u>N</u> ame: Content	dashboard_1
¢-	xcku040_0 w_iia_1 (ILA) Status Settings Capture Setup Waveform SysMon (System Monitor)
-	OK Cancel
	Source 11 Deckhoord Coture

Figure 11 Dashboard Setup

On the ZCU102 the hw\_ila\_1 window will be open by default.

Analog waveforms may be observed in the dashboard by selecting the RX Monitor channel data and setting the waveform style to Analog, shown in Figure 12.

	rance		900	1,000
• 📲 mySystem_i/JesdSubSys/Jesd_data_if/inst/rx_mon_i/ch0_0[15:0	] 8fb8	1////	ΛΛΛΛ	MM
	Cu <u>t</u>	Ctrl+X	VVVV	
a line of stars interaction of stars in the stars of the stars of the stars of	⊆opy	Ctrl+C	(NNNN)	NNN
mysystem_typesdsdbsys/jesd_data_ir/inst/rx_mon_t/cno_1(15.0	<u>P</u> aste	Ctrl+V	<b>N N N N N</b>	
	<u>D</u> elete	Delete	A A A A A	
•	<u>F</u> ind	Ctrl+F	$\Lambda \Lambda \Lambda \Lambda$	//////
	Select <u>A</u> ll	Ctrl+A	<u> </u>	/ / / /
	Expand		KNNN	A N N N
mySystem_i/JesdSubSys/jesd_data_if/inst/rx_mon_i/ch1_1[15:0]	<u>C</u> ollapse		JAIAIAA	AIAIAN
	<u>U</u> ngroup		*****	
•	R <u>e</u> name	F2	ИЛЛЛ	ЛЛЛ
	Name	+	<u> </u>	
	Waveform Styl	e ▶	🗆 <u>D</u> igital	
mySystem_i/JesdSubSys/jesd_data_if/inst/rx_mon_i/ch2_1[15:0]	Radix	•	🗹 Analog	
	Signal Color	•	Analog Se	ttings
m Sustam i (lacdSubSuc (lacd data if (inst (m man i (ch2 0[15:0	Divider Color	- L	7/7/7/7/	
inysystem_tyjesusussysyjesu_uata_ityinstytx_mon_tyths_o[15.0	Brinder Color	dor	/	VVVV
		uer	<b>NAN</b>	A A A A
•	📜 New Gr <u>o</u> up		MAIAIA	JANAN
	New D <u>i</u> vider		NNNN	
	≈ New <u>V</u> irtual B	1S	$\Lambda \Lambda \Lambda \Lambda I$	
mySystem_i/JesdSubSys/jesd_data_if/inst/rx_mon_i/ch4_0[15:0	9764	VVVV	//////	VVVV
•	67.0	MMM	$\Lambda \Lambda \Lambda \Lambda$	NNN/

Figure 12 Analog waveform setup

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### **Setting Up the Control GUI**

To launch the JESD204 UltraScale Hardware Demo GUI navigate to GUI directory and double click on uhwd\_gui.exe. A window will appear asking for the device's IP address, Figure 13. The IP address you enter here must be the address you noted at step 6 of <u>Configuring the FPGA</u>. After entering the appropriate IP address and click Accept.

P Address					
Current IP Address:	192	. 168	•	1	10
			_		

Figure 13 IP Address Input

If the BOARD is connected correctly to the PC and the IP address is correct, the GUI will launch. If not, an error message will appear stating that the BOARD could not be found (after clicking OK on the error message the GUI will open).

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**Operating the Hardware Demonstration** 

Once the GUI has been launched it will open in its default state which can be seen in Figure 14.

e					
	IESD204 Lilter	Soalo Hardwara	omo		
	JESD204 0108		emo		
ALC THOUSANIMADEL					
onfiguration Eyescan					
ESD204 Configuration	120 Section 120 Section 1	Line	Rate	Data R	ate
Ine Rate (GHz) F K	Subclass Scrambling	Equalization Mode	ALCONT D	The second se	
			6 /	8	
			A CONTRACTOR	10 4	
7 6 5 4 3 2	1 0			12	40 50 60 70
Active Lanes: 🔽 🗹 🗹 🔽 🗸			0.000 GI	bps	0.00 Gbps 8
	Py Coro			-10	9
Data			21	12 12	191
Sine Wave	Read Error	rkeg	20	100 M	
Ramos	Force Sync I	nactive			
PSK Pattern					
RPAT Pattern					
JSPAT Pattern					
		Mea	sure Latency		
		Displ	av Result Units		
		0.Cr	re Clk Cycles _ ns		
Update Configuration	n 🔘 🔘	Update Required			
		Result:	0		
latus					
	RX PLL LOCK:	JESD204 PHY STATUS:	0x0000003	HARDWARE ID:	0x01010088
TX PLL LOCK:			0-000000-		142
TX PLL LOCK:	BY SYNC.			HARDWARE VERSION:	1.4.2
TX PLL LOCK: 🥌 TX SYNC: 🌑	RX SYNC: 🔘	SYSTEM STATUS:	0,0000000		
TX PLL LOCK: TX SYNC: TX RESET DONE:	RX SYNC: 🥥	SYSTEM STATUS:	0x0000000	SOFTWARE VERSION:	2.1.0

Figure 14 GUI Default State

The GUI under the Configuration Tab is split up into three major sections:

- JESD204 Configurations: from here, various JESD204 configurations can be set
  - $\circ$   $\:$  Line Rate: Set Line rate of transceiver. Valid values from 1.0GHz to 12.5GHz
  - o F: Octets per frame, any value from 1-256 can be selected
  - o K: Frames per multiframe, any value from 1-32 can be selected
  - Subclass: JESD204 Subclass selection
  - o Scrambling. A toggle button to enable or disable scrambling in the JESD204 core
  - Equalization Mode: Select between LPM and DFE
  - o Active Lanes. Each check-box represents a lane, when selected that lane is active
  - Cable Loopback: When selected an external SMA cable loopback can be performed on lane 8. If no cables are present and this option is enabled the cores will not achieve SYNC
  - Under the Tx Core section, five different data patterns are available, a Sine Wave, a Ramp Pattern and a Phase Shift Keying modulation Pattern. The last two options, RPAT and JSPAT are Link test patterns and when enabled, the JESD204 cores will not achieve SYNC. These patterns can be used to run Eyescan(KCU105 only).
  - Under the Rx Core section, the '*Read Error Reg*' when pressed displays any errors that have occurred over the Link and the '*Force Sync Inactive*' toggle button forces the Tx JESD204 SYNC

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input low. Both of these buttons can be pressed at any time and do not require the '*Update Configuration*' to be pressed.

- The 'Update Configuration' when pressed updates the JESD204 configuration with the values selected in the GUI. Note, that until this button is pressed, any changes made to the configuration values in the GUI will not be passed into the cores. If a core setting has been modified, the LED located on the right of the button will turn RED, indicating that an update of the configuration is required.
- The right side of the GUI contains controls and displays for various features of the Hardware Demo:
  - The left speedometer displays the configured line rate of the Transceivers while the one on the right displays the aggregate data rate.
  - The 'Measure Latency' toggle button enables a deterministic latency test witch counts the number of core clock cycles (or ns depending on GUI selection) required from the data entering the transmit JESD204 core to it exiting the receive JESD204 core. This test is available only when all 8 lanes are enabled. To run, enable the test and toggle the 'Force Sync Inactive' button. The result should remain the same (Subclass 1 and 2 only) between resynchronizations.
- The bottom part of the GUI displays various Status indicators based on the state of the hardware demo.

Once the 'Update Configuration' is pressed the Tx and Rx SYNC LEDs should turn green and the GUI should match Figure 15.

JESD204 UltraScale Hardware Dem	0	3.	the	The second second second	
	JESD204 Ult	raScale Hardw	vare Demo		
Configuration Eyescan JESD204 Configuration Line Rate (GHz) F K 6.250 + 4 + 8	Subclass Scrambling	g Equalization Mode	Line Rate	Data R	late
7 6 5 4 3 Active Lanes: ♥ ♥ ♥ ♥ Cable Loopback: □ Tx Core Data	2 1 0 V V Rx Core	Tor Page	3 6.25 1	Gbps 12 13	40 50 60 70 50.00 3bps 80 90 100
Sine Wave     Ramps     PSK Pattern     RPAT Pattern     SPAT Pattern	Force Syn	c Inactive			
Update Configura	tion	Running	Measure Latency Display Result Units Core Clk Cycles n	5	
Status TX PLL LOCK: ●	RX PLL LOCK:	JESD204 PHY	Result: 0 STATUS: 0x00000003	HARDWARE ID:	0x01010088
TX SYNC: 🤍	RX SYNC: 🥥	SYSTEM	STATUS: 0x0000003c	HARDWARE VERSION:	1.4.2

Figure 15 GUI After Configuration

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### Running Eyescan (KCU105 only)

In the second tab of the GUI (which is only displayed if connected to a KCU105), Figure 6, Eyescan can be run on any enabled lane. To start the data sampling required to display the BER heat map, select the correct lane tab depending on the lane wanting to run Eyescan and then click on Start Eyescan. Once clicked the button will grey out until the process is complete. Note that while Eyescan is running, changing the configuration of the JESD204 cores is disabled (Figure 17). Eyescan can be run in parallel on multiple lanes. The time required to complete the Eyescan depends on the line rate and equalization mode selected in the Configuration tab.



Figure 16 Eyescan Result

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ile						
EXILINX ALL PROGRAMMABLE.	JESD204 Ultr	raScale Hard	ware <mark>D</mark> ei	mo		
onfiguration Eyescan						
JESD204 Configuration			-Line Pa		Data	lata
Line Rate (GHz) F K 12.500 A 4 8 4	Subclass Scrambling	Equalization Mode	Line Ka	Station for the	8 9 9 10 C	
7 6 5 4 3 2 J Active Lanes: V V V V V K Cable Loopback:	10		Sum S	3 12.500 Gb	ps 12 10 20	40 <sup>50</sup> 60 70 100.00 Gbps 80
Tx Core	Rx Core				13 🦻 🌮	
Data	Read Erro	or Reg		0		
Data © Sine Wave	Read Erro	or Reg		0		
Data © Sine Wave © Ramps	Read Erro Force Sync	or Reg		0		
Data Osine Wave Ramps PSK Pattern	Read Erro Force Sync	or Reg		0		
Data Osine Wave Ramps PSK Pattern RPAT Pattern	Read Erro Force Sync	or Reg		0		
Data Sine Wave Ramps PSK Pattern RPAT Pattern JSPAT Pattern	Read Erro Force Sync	or Reg	Measure	e latency		
Data Sine Wave Ramps PSK Pattern RPAT Pattern SPSAT Pattern	Read Err	or Reg	Measure	e Latency		
Data Sine Wave Ramps PSK Pattern RPAT Pattern SISPAT Pattern	Read Err	or Reg	Measure	e Latency Result Units		
Data Sine Wave Ramps PSK Pattern RPAT Pattern SJSPAT Pattern Update Configuration	Read Err	Inactive	Measuri Display © Core	e Latency Result Units Clk Cycles © ns		
Data Osine Wave Ramps PSK Pattern RPAT Pattern Osphare Space Update Configuration	Read Err	Inactive	Measure Display @ Core Result: 0	e Latency Result Units Clk Cycles © ns		
Data © Sine Wave Ramps PSK Pattern PSK Pattern Ø JSPAT Pattern Update Configuration Status	Read Err	Inactive	Measuri Display @ Core Result: 0	e Latency Result Units Clk Cycles © ns		
Data Sine Wave Ramps PSK Pattern RPAT Pattern JSPAT Pattern Update Configuration	Read Err	Inactive	Measuri Display @ Core Result: 0	e Latency Result Units Clk Cycles © ns		
Data Sine Wave Ramps PSK Pattern RPAT Pattern JSPAT Pattern Update Configuration Update Configuration TX PLL LOCK:	Read Err Force Sync	Inactive Inactive Running Eyescan JESD204 PH	Measure Display @ Core Result: 0	e Latency Result Units Clk Cycles © ns 0x0000003	HARDWARE ID:	0×01010088
Data Sine Wave Ramps PSK Pattern PSK Pattern PSK Pattern Update Configuration Update Configuration TX PLL LOCK: TX SYNC:	Read Err Force Sync	or Reg Inactive Running Eyescan JESD204 PH SYSTER	Measurn Display © Core Result: 0 HY STATUS: M STATUS:	e Latency Result Units Clk Cycles ns 0x00000003 0x0000000c	HARDWARE ID: HARDWARE VERSION:	0x01010088 1.4.2

Figure 17 Configuration Tab When Running Eyescan

#### **Status LEDs**

The user GPIO LEDs on the evaluation boards are used to provide additional visual status indications. The LEDS are assigned as shown in Table 1. The flashing LED's are used to indicate the status of individual clocks and are actually divided versions of the clock.

GPIO LED	Function	Description
0	Rx SYNC	ON = SYNCB deasserted by Rx core
1	Tx SYNC	ON = SYNCB deasserted at Tx core
2	RX Reset done	ON = RX reset complete.
3	DRP CLK	Flashing = CLK Active.
4	AXI CLK	Flashing = CLK Active.
5	TX/RX CORECLK	Flashing = CLK Active.
6	GT REFCLK	Flashing = CLK Active.
7	TX EMPTY	ON = There is no data available for the TX core from
		the AXI DMA.

**Table 1 Status LEDs**