

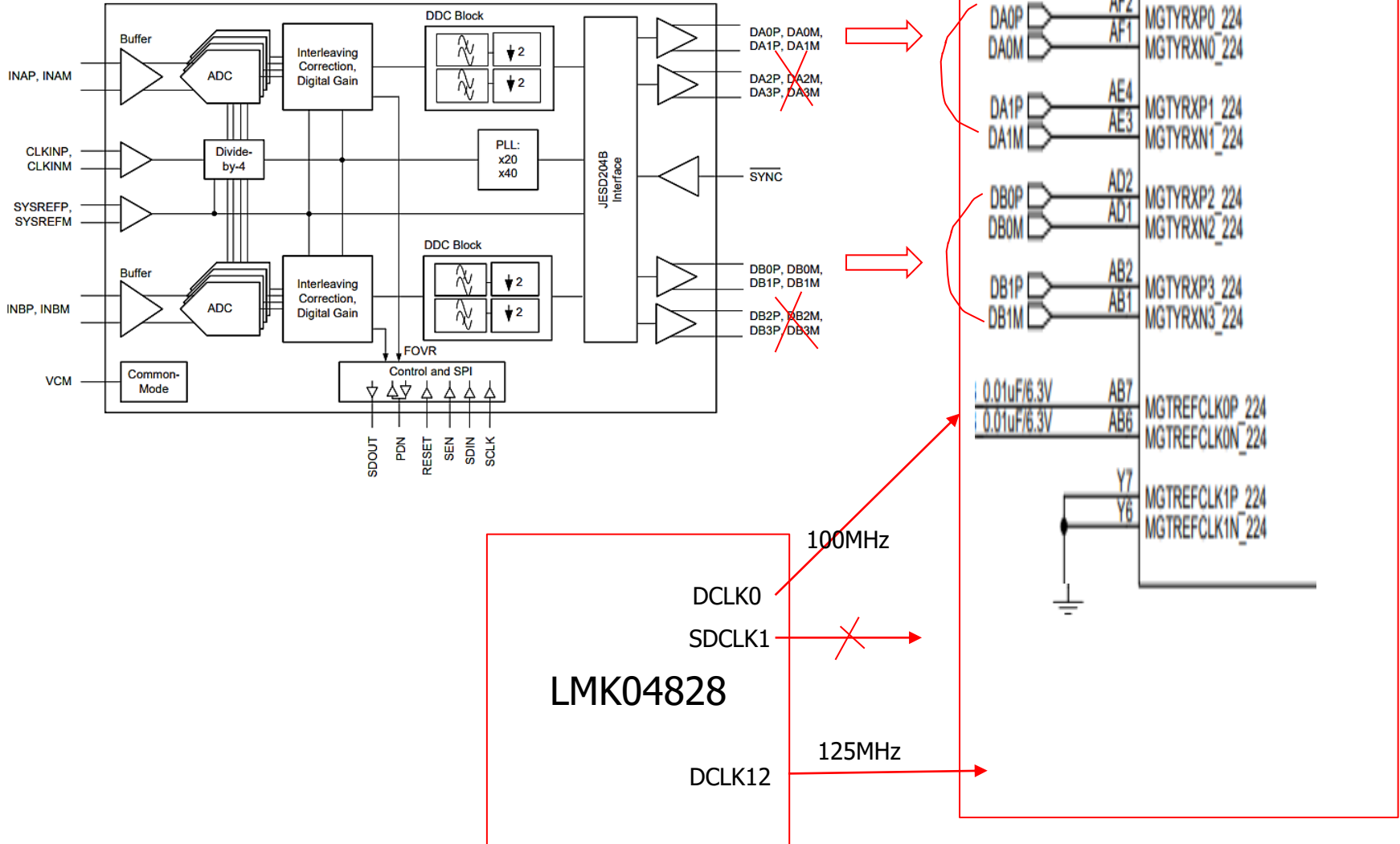


JESD Pattern Test

2023-06-22
dkkim

4. JESD

1. Configuration Interconnect



4. JESD

2. Test Mode Setting

ADS54JxxLMK04828Low Level ViewUSB Status ● Reconnect FTDI ?

Transfer Read to Write

Register Map

Block / Register Name	Address	Default	Mode	Size	Value
x16D	0x16D	0x00	R/W	8	0x00
x16E	0x16E	0x16	R/W	8	0x13
x17C	0x17C	0x15	R/W	8	0x15
x17D	0x17D	0x0F	R/W	8	0x0F
[-] ADS54Jxx_ANALOG					
0x00	0x00	0x00	R/W	8	0x81
MASTER 0x20	0x8020	0x00	R/W	8	0x00
MASTER 0x21	0x8021	0x00	R/W	8	0x00
MASTER 0x22	0x8022	0x00	R/W	8	0x00
MASTER 0x26	0x8026	0x00	R/W	8	0x00
MASTER 0x53	0x8053	0x00	R/W	8	0x00
MASTER 0x55	0x8055	0x00	R/W	8	0x00
[-] ADS54Jxx_DIGITAL					
MAIN DIGITAL 0x00	0x680000	0x00	W	8	0x00
JESD DIGITAL 0x00	0x690000	0x00	R/W	8	0x90
JESD DIGITAL 0x01	0x690001	0x00	R/W	8	0x31
JESD DIGITAL 0x02	0x690002	0x00	R/W	8	0x00
JESD DIGITAL 0x03	0x690003	0x00	R/W	8	0x00
JESD DIGITAL 0x05	0x690005	0x00	R/W	8	0x00
JESD DIGITAL 0x06	0x690006	0x00	R/W	8	0x0F
JESD DIGITAL 0x07	0x690007	0x00	R/W	8	0x00
JESD DIGITAL 0x16	0x690016	0x00	R/W	8	0x00

Write Data

Read Data

Current Address

Note: Load Config will Overwrite all Registers.

Register Data

	R	W
0	<input type="checkbox"/>	<input type="checkbox"/>
1	<input type="checkbox"/>	<input type="checkbox"/>
2	<input type="checkbox"/>	<input type="checkbox"/>
3	<input type="checkbox"/>	<input type="checkbox"/>
4	<input type="checkbox"/>	<input checked="" type="checkbox"/>
5	<input type="checkbox"/>	<input type="checkbox"/>
6	<input type="checkbox"/>	<input type="checkbox"/>
7	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>

Register Description

CTRL_K[7:7]
Enable bit for number of frames per multiframe - if cleared K = 5, if set K is set in register
0x6906

TESTMODE_EN[4:4]
Generates long transport layer test pattern

Block: ADS54Jxx_DIGITAL

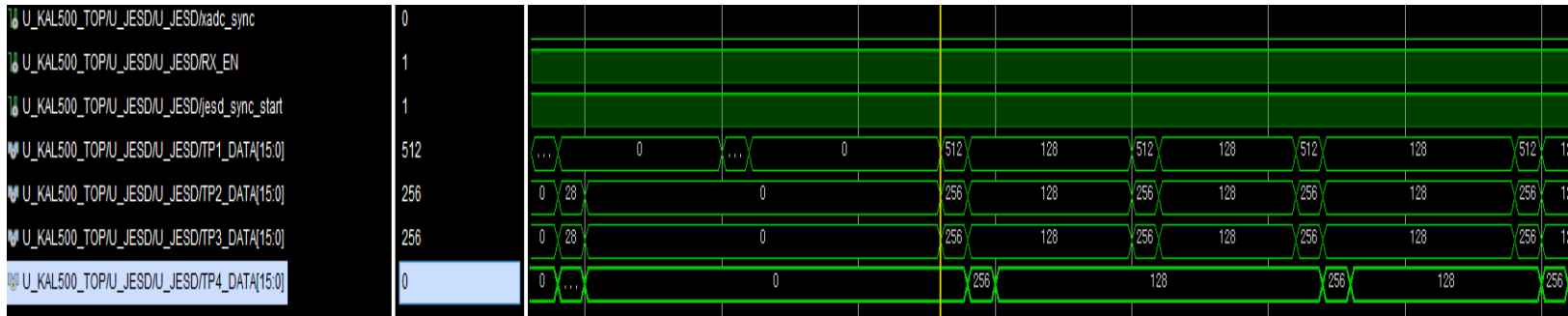
Address: x 690000

Write Data: x 90

Read Data_Generic: x 80

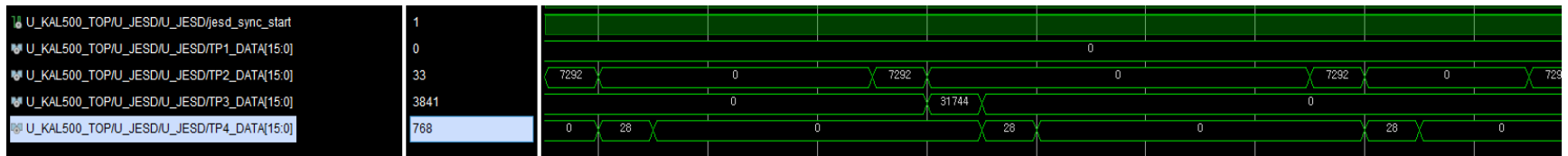
4. JESD

3. JESD204B PAI Output(unsigned Decimal 16bit , 4 Sample at 125MHz)



(0 0 0 0)
(0 256 256 512)
(256 128 128 128)
(128 128 128 128)
(128 128 128 128)
(128 128 128 128)
(128 128 128 128)
(128 128 128 128)
(128 128 128 128)
(128 256 256 512)

ADDR 69002 : 60h,



Q & A

Thank You!