

Address	Register Name	CD5a_Pixmclk	SH1a_default	SH2a_pixel_mclk_default	SH2b_default	SH3_default	Test_pattern_line_ramp
0x00	ANLG_CONFIG	2F	2E	2E	2E	2E	2C
0x01	INTF_CONFIG	0C	6C	6C	6C	6C	04
0x02	CLP_CONFIG, Sample Timing Control	1E	1E	FC	FD	9C	9D
0x03	CDSG_CONFIG, CDS / SH Gain Enable, FDAC Range Select	38	00	00	80	00	07
0x04	Main Configuration 4	83	82	83	82	80	83
0x05	Main Configuration 5	77	77	77	F7	77	F7
0x06	SRESET	00	00	00	00	00	00
0x07	Device Revision	A0	A0	A0	A0	09	A0
0x08	GA_R1	B1	00	00	00	00	F8
0x09	C_OFFSET_R1	12	10	14	1F	10	11
0x0A	F_OFFSET_R1	6A	80	A8	80	80	6E
0x0B	F_OFFSET_R1 LSB	20	00	80	00	00	A0
0x0C	GA_R2	AB	00	00	00	00	FF
0x0D	C_OFFSET_R2	12	10	1F	07	10	11
0x0E	F_OFFSET_R2	85	80	80	80	80	77
0x0F	F_OFFSET_R2 LSB	60	00	00	00	00	E0
0x10	GA_G1	00	00	00	00	00	00
0x11	C_OFFSET_G1	13	10	14	1A	10	11
0x12	F_OFFSET_G1	8D	80	A8	80	80	6F
0x13	F_OFFSET_G1 LSB	60	00	E0	00	00	00
0x14	GA_G2	00	00	00	00	00	FC
0x15	C_OFFSET_G2	13	10	14	05	10	11
0x16	F_OFFSET_G2	83	80	9F	80	80	83
0x17	F_OFFSET_G2 LSB	40	00	20	00	00	00
0x18	GA_B1	00	00	00	00	00	FF
0x19	C_OFFSET_B1	13	10	14	1C	10	10
0x1A	F_OFFSET_B1	7D	80	9F	7E	80	95
0x1B	F_OFFSET_B1 LSB	20	00	C0	60	00	20
0x1C	GA_B2	00	00	00	00	00	F8
0x1D	C_OFFSET_B2	13	10	14	04	10	11
0x1E	F_OFFSET_B2	89	80	A7	80	80	7A
0x1F	F_OFFSET_B2 LSB	40	00	40	C0	00	E0
0x20	TARG_BLK_R	20	40	40	40	40	20
0x21	TARG_BLK_G	20	40	40	40	40	20
0x22	TARG_BLK_B	20	40	40	40	40	20
0x23	BLKCLP_CTL0	00	00	04	04	00	0C
0x24	BLKCLP_CTRL1	84	34	8C	0C	0C	84
0x25	CDAC_THLD_MSB	50	64	64	64	64	50
0x26	CDAC_THLD_LSB	40	00	00	00	00	40
0x27	High Speed Mode	88	88	88	88	88	88
0x28	AGC_CONFIG	10	50	50	50	50	41
0x29	PK_AVE	00	04	04	04	04	04
0x2A	REG_PK_DET_ST_MSB	00	00	00	00	00	0
0x2B	REG_PK_DET_ST_LSB	32	64	64	64	64	0A
0x2C	PK_DET_WID_MSB	1D	07	07	07	07	09
0x2D	PK_DET_WID_LSB	4C	6C	6C	6C	6C	4C
0x2E	AGCDuration	00	FF	FF	FF	FF	10
0x2F	AGCTargetMSB	00	90	90	90	90	E0
0x30	AGCTargetLSB	00	00	00	00	00	00
0x31	AGCTolerance	00	14	14	14	14	28
0x32	AGC_BLKINT	00	00	00	00	00	00
0x33	AGC STATUS	00	00	00	00	3F	00
0x34	Reserved						
0x35	Reserved						
0x36	DLL Sample Position	00	1F	0C	13	00	1F
0x37	DLL Sample Width	02	00	63	63	00	60
0x38	TEST_PAT_CTL	20	00	00	00	00	A0
0x39	TESTPLVL_MSB	00	FF	FF	00	FF	02
0x3A	TESTPLVL_LSB	00	C0	C0	00	C0	80
0x3B	PATW	01	00	00	00	00	0C
0x3C	PATS	01	00	00	00	00	0F
0x3D	LINE_INTVL	00	00	00	00	00	06
0x3E	Reserved						
0x3F	PAGE_SEL for Page Control						