Hi,

We are using the LM98640W-MPR Dual channel, 14bit 40MSPS AFE and we are unable to get it to operate as expected. Our end goal is to use the LM98640QML-P for a space application with a CCD imager.

Regardless of the mode (S/H, CDS, or Test Pattern Output) the output data signals TXOUT1 and TXOUT2 are fixed. They send out a value approximating full scale (0x3FFF) almost always. In some rare cases the output was instead fixed at half scale (0x1fff). I am not sure what was different in the setups of those two cases yet.

Can examples of complete register setups, with the order that the registers must be written, and the expected results be provided for the Test pattern output, S/H and CDS modes?

The register setups we used for each case is provided below.

After powering the device we first program all of the non-reserved registers with the baseline values per the datasheet. We do not program base values to reserved registers per some TI support forum recommendations. Some TI support entries discuss programming some of the reserved registers but this is not clearly documented. One support entry says to write value 0x34 to reserved address 0x24. Other support entries say to not write any reserved registers.

We are running INCLK at 5MHz. We are in dual channel mode. The S/H and CDS buffer gain is 2x, PGA gain is 1x.

We have tried S/H, CDS, and test modes and find that the data out of TXOUT1 and TXOUT2 does not change from one mode to another and regardless of input stimulus.

The output signal TXOUT1 outputs values in the range of 0x3f67 to 0x3f87. Only bits 7:4 change. All other bits are static.

The output signal TXOUT2 outputs values in the range of 0x3df7 to 0x3e27. Only bits 9:4 change. All other bits are static.

While in S/H and also CDS modes the output stayed the same regardless of the following stimulus being applied to the OS- and OS+ inputs for each channel:

OS- OS+

0V 0V

0V 0.9Vdc

0.1Vpk-pk ac 0V

0V 0.9Vpk-pkac

We also tried setting the PGA gain to 8.

We did observe that the width of TXFRM behaves as expected when going between S/H and CDS modes. We did observe the DTM0 and DTM1 timing monitor signals once enabled. The LVDS outputs did respond to LVDS Output Mode register settings. We do not know of any other signals to look at for feedback on how the part is working.

We have looked through the Data Converters Forum on the TI website. Can you suggest any other sources for setup and application information?

Can you suggest what we are not doing correctly? We would welcome a call to discuss. Is there any other information that we can provide?

We welcome any ideas to help us get this device to operate as expected.

Also, the ADC code gain formula is not specified and there are 3 reference voltages present (2V, 1V, 1.2V). Can We assume that the ADC reference voltage is 2V?

Please see below table with register setups. Yellow highlighting shows programming performed after setting baseline values for that mode. 4 register setups are shown: baseline, test mode, S/H, and CDS.

Reg setup table is below:



Please see image below of waveform from internal logic analyzer in FPGA. Shown is the txfrm, txout1, txout2 signals. The complete 14 bit data is shown as txout1\_data\_d1 and txout2\_data\_d1.

Logic analyzer images showing output signals is below:







Lastly I show a register access to test pattern control reg. The register accesses seem to be working fine.

One Write, then 3 reads. Data of 0xe0 is written to address 0x34 followed by reads of same data.



Zoom of the first write and first read



Zoom of 3rd and last read



Thank you,

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