7.3.9 LVDS Output Mode

7.3.9.1 LVDS Output Format

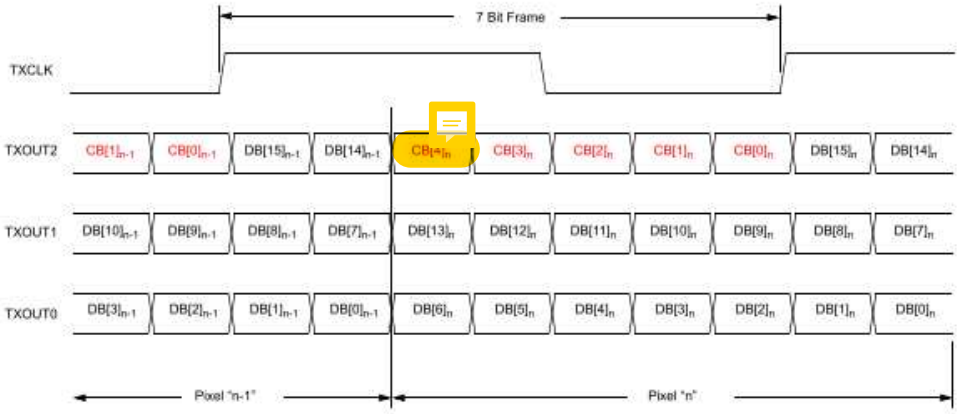

Figure 43. LVDS Output Bit Alignment and Data Format

LM98714 output format

7.4.15.5 LVDS Output Format - LM98714 Mode

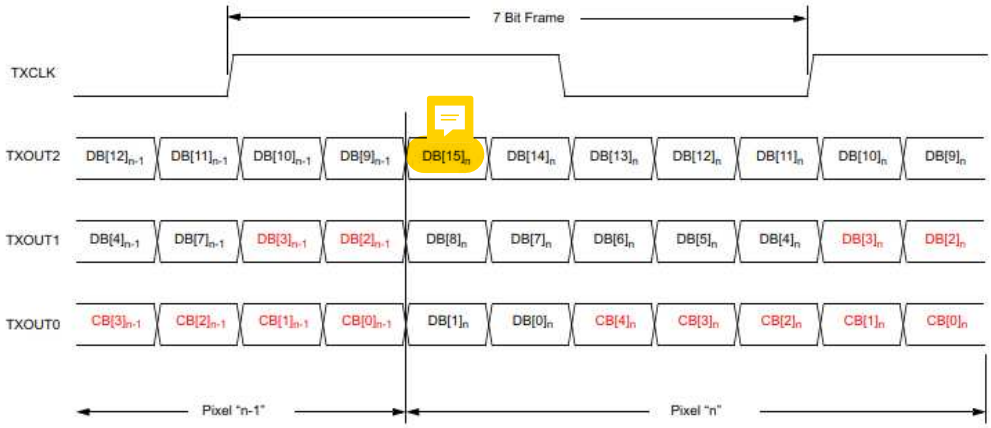

Figure 45. LVDS Output Bit Alignment and Data Format

98722 相容 98714 Mode 的 Format 與正常的 LM98714 不同

LVDS Output Format - LM98714 Mode

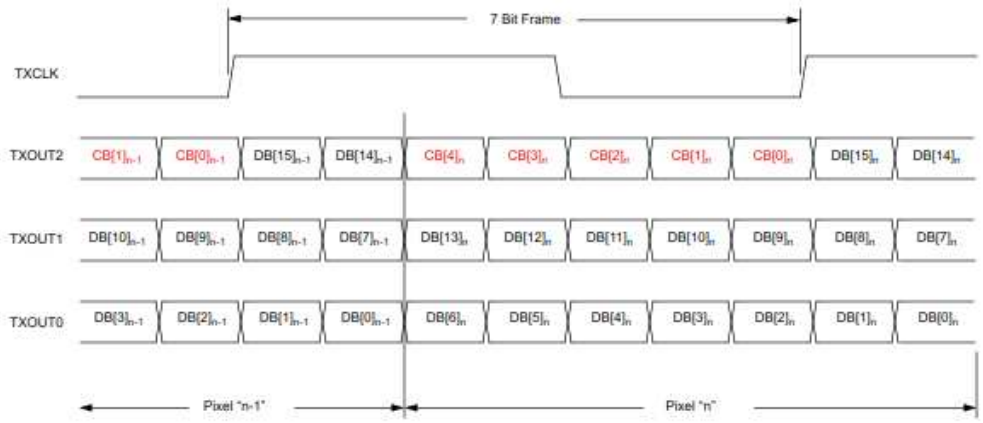

Figure 42: LVDS Output Bit Alignment and Data Format

LVDS Control Bit Coding - LM98714 Mode

The 5 control bits included in the LVDS data stream are coded as follows:

The "active" and "black" pixel tags are programmable tags that the LM9872X provides in order to identify how many pixels have been processed since the falling edge of SH.

Which pixels are given "Active" and "Black" CB tags is controlled by Page 2, Registers 0x02, 0x08-0x0C, and 0x0F. (# Black Pixels Averaged, Black Pixels Start, Active/White Pixels Start, Active/White Pixels End, and Line Length Multiplier).

The LM9872X counts the number of pixel periods after the SH Interval: If the number of pixel periods after the SH Interval is greater than (Black Pixels Start) and less than (Black Pixels Start + # Black Pixels Averaged) the CB bits will indicate that the pixel is a Black pixel. If the number of pixel periods after the falling edge of SH is between Active/White Pixels Start and Active/White Pixels End, the CB bits will indicate that the pixel is an Active pixel.

Latency Compensation of CB Bits

By default, the CB bits will be compensated for the latency through the AFE signal chain. This compensation can be turned off by setting Page 8, Register 0x08, Bit 2 = 1.

LM9872x Porgramming and Operation Manual 內的 Format 也與 LM98722 不同?