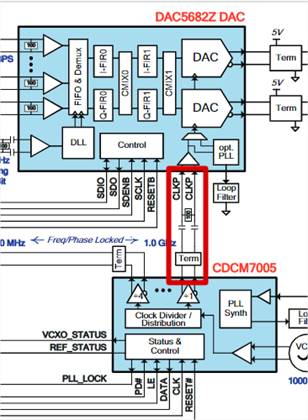
Hi Team,

In my design I use the LMK04828 as a clock source to the DAC5682Z.

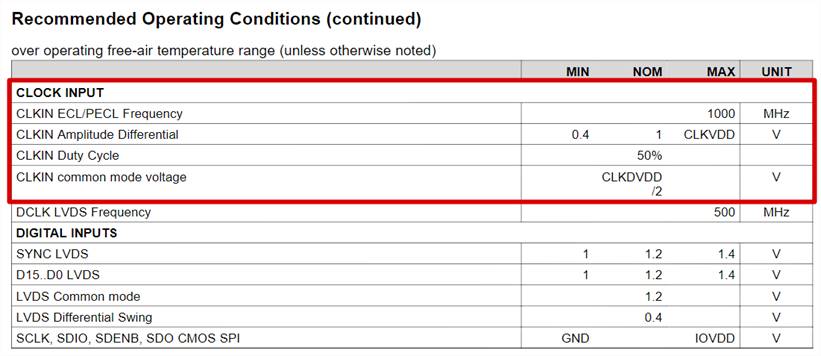
The LMK04828 generate a 1GHz clock to the DAC5682Z.

As describe in the next picture:

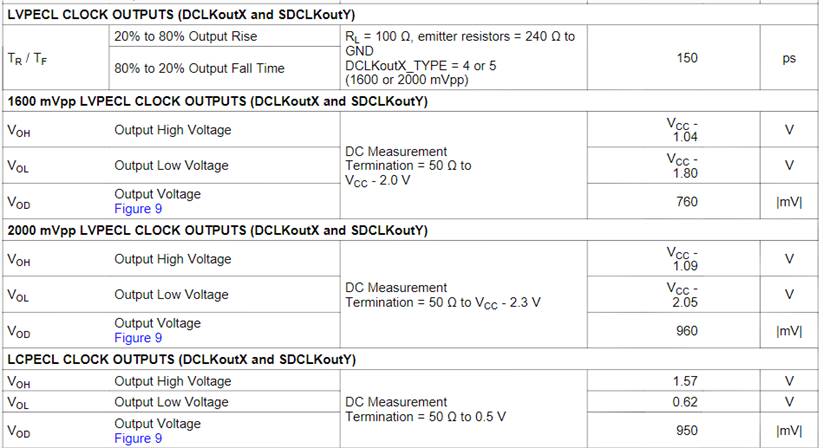


The LMK04828 is replacing the CDCM7005.

According to the DAC5682Z data sheet, DAC5682Z expect in CLKin to:



The next table is from the LMK04828 data sheet. The table describes the voltage level of the LMK04828 Output:



The LMK04828 configured to LVPECL 200mV, LVPECL 1600mV and LCPECL .

The Emitter resistor is 240 ohm.

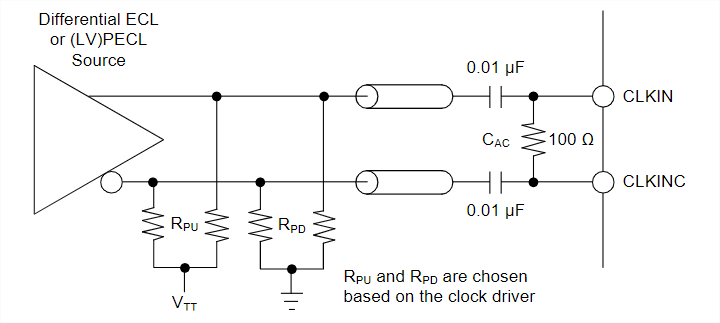
The connection between the LMK04828 outputs and the DAC5682Z CLKin is AC coupled.

The DAC5682Z can play a clean sine wave only with LCPECL clock.

Some time it work and other time it doesn’t. I didn’t get an answer why LVPCEL doesn’t work.

I try to do a simulation in Hyperlynx. I use the Ibis model of the DAC5682Z and the LMK04828 .

I build my simulation as describe in the next picture:



According the LMK04828 EVM I need to use RPD = 240 hom. Only in the EVM Document I have this information. In the LMK04828 data sheet I don’t have the information.

When I use the sires capacitors, the clock in the DAC5682Z looks a sine wave. When I don’t use the capacitors the result looks good. In reality I need this capacitor.

I suspect the Ibis model of the DAC5682Z  made the problem. When I run the simulation to see the results are good.

To summer up:

We have several problems:

1. The results in the simulation don’t have  a correlation  with  the board.
2. Only one configuration in the LMK04828 results with clean sine wave at the output of the DAC. The other configuration doesn’t make the some results. I try use HSDS 10mA the sine wave at the DAC output still bad.
3. The LMK04828 output start at different time. I expect the output to be aligned.

Thanks,

Shlomi