LMK04828 configuration modes

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# Clock Distribution Mode

The clock distribution mode is the easiest way to operate the LMK04828 device. A user simply passes a reference frequency into the CLKin1 input and sets the VCO to “External VCO”. This will pass the reference clock provided to CLKin1 directly to the delay and output divider stages (div/1 through div/32).



# Single PLL

In single PLL mode, the input reference is passed into PLL2 of the LMK04828 and the user can generate frequencies within the different VCO ranges for this device. VCO0 covers frequencies between 2370MHz and 2630MHz while VCO1 covers 2920MHz through 3080MHz. The user then can select the available integer (div/1 through div/32) output divider values to generate the frequencies of interest on each clock output. SYSREF generation works using the same principal.



# Dual PLL

In dual PLL mode the first PLL acts as a jitter cleaner. A reference clock is passed into the device via the CLKin0, CLKin1, CLKin2 input(s) and used in combination with a low noise crystal acting as feedback for PLL1 (and also a reference for PLL2) in a narrow PLL loop bandwidth. This will achieve a jitter cleaning affect as the close-in phase noise is improved due to the crystal while the further offset freq remain the higher performance input. Then the jitter cleaned reference is proided into PLL2 as shown above in single PLL mode.

For instance, the upper side band (USB) of the input would look similar to this:

Input reference

Crystal

Jitter cleaned output

