

[illegible]

GATE BIAS CONTROLLER SECTION

The schematic diagram illustrates the Gate Bias Controller Section. It features a central LMP92066PWP (U19) gate driver IC. The circuit is powered by +3.3V and +5V rails. Key components include:

- Resistors:** RS1 (4.7k, 0.063W), RS2 (4.7k, 0.063W), RS3 (4.7k, 0.063W), RS4 (4.7k, 0.063W), RS5 (4.7k, 0.063W), R48 (4.7k, 0.063W), R49 (4.7k, 0.063W), R46 (4.7k, 0.063W), R40 (360 ohm), R39 (360 ohm), R41 (25.2 ohm, 0.1W).
- Capacitors:** C86 (2.2uF, 16V), C87 (2.2uF, 16V), C88 (7uF, 5.3mm x 6.1mm, 16V), C89 (0.1uF), C90 (0.1uF), C91 (0.1uF), C92 (6pF, 50V).
- Transistors:** C84 (MOSFET), C89 (MOSFET).
- Other Components:** TP11 (test point), U19 (LMP92066PWP).

The circuit is designed to provide a precise gate bias voltage to the MOSFETs, ensuring optimal switching performance. The +3.3V rail is used for the control logic, while the +5V rail is used for the gate driver and the MOSFETs. The gate driver IC (U19) is configured to drive the MOSFETs (C84, C89) through the gate bias network.

+3.3V LDO Section

Note: Place the input capacitor & Output Capacitor as close to the Input & Output of the device as possible respectively.

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DC TO DC CONVERTER SECTION			
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