```
SPIWrite 0015,80,7,7  //timing_controller=0x1;
     Address(0x15[7:7])
SPIWrite 00ec,01,0,0  //use_reg_for_rxtdd=0x1;
     Address(0xec[7:0])
SPIWrite 00f4,01,0,0  //use_reg_for_fbtdd=0x1;
     Address(0xf4[7:0])
SPIWrite 00e4,01,0,0  //use_reg_for_txtdd=0x1;
     Address(0xe4[7:0])
SPIWrite 00ed,0f,0,3  //reg_for_rxtdd=0xf;  Address(0xed[7:0])
SPIWrite 00f5,00,0,1  //reg_for_fbtdd=0x0;  Address(0xf5[7:0])
SPIWrite 00e5,0f,0,3  //reg_for_txtdd=0xf;  Address(0xe5[7:0])

//END: Setting TDD Pin in override state and setting override
values.

SPIWrite 0015,00,7,7  //timing_controller=0x0;
     Address(0x15[7:7])

SPIWrite 0018,20,0,7  //macro=0x1;    Address(0x18[7:5])
SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0x0;
     Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00,0,7
SPIWrite 00a1,00,0,7
SPIWrite 00a0,00,0,7
SPIWrite 0193,90,0,7  //MACRO_OPCODE=0x90;
     Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
     Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4
```

```
//Read     MACRO_ERROR_IN_OPCODE=0x0; Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
      Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIWrite 0018,00,0,7  //macro=0x0;     Address(0x18[7:5])
SPIWrite 0018,40,0,7  //cm4_internal=0x1;   Address(0x18[7:6])
SPIWrite 0274,02,0,7  //NLE_WFI_DIS=0x1;    Address(0x274[7:1])
SPIWrite 0018,00,0,7  //cm4_internal=0x0;   Address(0x18[7:6])
SPIWrite 0018,20,0,7  //macro=0x1;     Address(0x18[7:5])
SPIWrite 0144,08,0,7  //all_addr_high=0x2;  Address(0x144[7:2])
SPIWrite 0018,00,0,7  //macro=0x0;     Address(0x18[7:5])
SPIWrite 0018,08,0,7  //cm4top_dram=0x1;    Address(0x18[7:3])
SPIWrite 1408,10,0,7
SPIWrite 1409,01,0,7
SPIWrite 1402,3f,0,7
SPIWrite 1403,00,0,7
SPIWrite 1443,05,0,7
SPIWrite 1442,f5,0,7
SPIWrite 1441,e1,0,7
SPIWrite 1440,00,0,7
SPIWrite 140b,27,0,7
SPIWrite 140c,27,0,7
SPIWrite 140d,27,0,7
SPIWrite 140e,27,0,7
SPIWrite 140f,27,0,7
SPIWrite 1410,27,0,7
```

```
SPIWrite 0018,00,0,7  //cm4top_dram=0x0;    Address(0x18[7:3])
SPIWrite 0018,20,0,7  //macro=0x1;     Address(0x18[7:5])
SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0x7;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00,0,7
SPIWrite 00a1,00,0,7
SPIWrite 00a0,07,0,7
SPIWrite 0193,a4,0,7  //MACRO_OPCODE=0xa4;
      Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
      Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
      Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
```

```
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0x8;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00,0,7
SPIWrite 00a1,00,0,7
SPIWrite 00a0,08,0,7
SPIWrite 0193,a4,0,7  //MACRO_OPCODE=0xa4;
      Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
      Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
```

```
      Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0x100;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00,0,7
SPIWrite 00a1,01,0,7
SPIWrite 00a0,00,0,7
SPIWrite 0193,72,0,7  //MACRO_OPCODE=0x72;
      Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7
```

```
//Read     MACRO_ERROR_OPCODE=0x0;
      Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
      Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIWrite 0018,00,0,7  //macro=0x0;     Address(0x18[7:5])
SPIWrite 0015,40,0,7  //digtop=0x1;    Address(0x15[7:6])
SPIWrite 0b01,00,0,7  //addr_high_nlcm4=0x0;
      Address(0xb01[7:0])
SPIWrite 0015,00,0,7  //digtop=0x0;    Address(0x15[7:6])
SPIWrite 0019,04,0,7  //NL_dram=0x1;   Address(0x19[7:2])
SPIWrite 027b,02,0,7
SPIWrite 0264,ff,0,7
SPIWrite 0265,ff,0,7
SPIWrite 0274,ff,0,7
SPIWrite 0275,ff,0,7
SPIWrite 0019,00,0,7  //NL_dram=0x0;   Address(0x19[7:2])
SPIWrite 0015,40,0,7  //digtop=0x1;    Address(0x15[7:6])
SPIWrite 0b01,00,0,7  //addr_high_nlcm4=0x0;
      Address(0xb01[7:0])
SPIWrite 0015,00,0,7  //digtop=0x0;    Address(0x15[7:6])
SPIWrite 0019,04,0,7  //NL_dram=0x1;   Address(0x19[7:2])
```

```
SPIWrite 0097,00,0,7  //qHwAggrTimeus=0x3e8;
     Address(0x94[7:0],0x95[7:0],0x96[7:0],0x97[7:0],0x98[7:0])
SPIWrite 0096,00,0,7
SPIWrite 0095,03,0,7
SPIWrite 0094,e8,0,7
SPIWrite 0019,00,0,7  //NL_dram=0x0;   Address(0x19[7:2])
SPIWrite 0018,20,0,7  //macro=0x1;     Address(0x18[7:5])
SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0x8f0001;
     Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,8f,0,7
SPIWrite 00a1,00,0,7
SPIWrite 00a0,01,0,7
SPIWrite 0193,89,0,7  //MACRO_OPCODE=0x89;
     Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
     Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
     Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])
```

```
SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0x7;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00,0,7
SPIWrite 00a1,00,0,7
SPIWrite 00a0,07,0,7
SPIWrite 0193,a3,0,7  //MACRO_OPCODE=0xa3;
      Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
      Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4
```

```
//Read     MACRO_ERROR_IN_OPCODE=0x0; Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
      Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0x78;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00,0,7
SPIWrite 00a1,00,0,7
SPIWrite 00a0,78,0,7
SPIWrite 0193,a3,0,7  //MACRO_OPCODE=0xa3;
      Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1; Address(0xf0[7:2])


SPIPoll 00f0,2,2,4
```

```
SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
      Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0; Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
      Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0x0;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00,0,7
SPIWrite 00a1,00,0,7
SPIWrite 00a0,00,0,7
```

```
SPIWrite 0193,90,0,7  //MACRO_OPCODE=0x90;
     Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
     Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
     Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
     Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
     Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIWrite 0018,00,0,7  //macro=0x0;     Address(0x18[7:5])
```

```
SPIWrite 0018,40,0,7  //cm4_internal=0x1;   Address(0x18[7:6])
SPIWrite 0274,02,0,7  //NLE_WFI_DIS=0x1;    Address(0x274[7:1])
SPIWrite 0018,00,0,7  //cm4_internal=0x0;   Address(0x18[7:6])

SPIWrite 0018,20,0,7  //macro=0x1;     Address(0x18[7:5])
SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0xf00;
     Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,00,0,7
SPIWrite 00a1,0f,0,7
SPIWrite 00a0,00,0,7
SPIWrite 0193,a3,0,7  //MACRO_OPCODE=0xa3;
     Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
     Address(0xf1[7:0],0xf2[7:0])

SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0;  Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
     Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7
```

```
//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIRead 00f0,0,0

//Read     MACRO_READY=0x1;      Address(0xf0[7:0])


SPIPoll 00f0,0,0,1

SPIWrite 00a3,00,0,7  //MACRO_OPERAND_REG0=0x10002;
      Address(0xa0[7:0],0xa1[7:0],0xa2[7:0],0xa3[7:0],0xa4[7:0])
SPIWrite 00a2,01,0,7
SPIWrite 00a1,00,0,7
SPIWrite 00a0,02,0,7
SPIWrite 00a7,00,0,7  //MACRO_OPERAND_REG1=0x13f;
      Address(0xa4[7:0],0xa5[7:0],0xa6[7:0],0xa7[7:0],0xa8[7:0])
SPIWrite 00a6,00,0,7
SPIWrite 00a5,01,0,7
SPIWrite 00a4,3f,0,7
SPIWrite 0193,a0,0,7  //MACRO_OPCODE=0xa0;
      Address(0x193[7:0],0x194[7:0])

WAIT 0.001
SPIRead 00f0,2,2

//Read     MACRO_DONE=0x1;  Address(0xf0[7:2])


SPIPoll 00f0,2,2,4

SPIReadCheck 00f0,3,3,00

//Read     MACRO_ERROR=0x0;      Address(0xf0[7:3])

SPIRead 00f1,0,7

//Read     MACRO_ERROR_OPCODE=0x0;
      Address(0xf1[7:0],0xf2[7:0])
```

```
SPIRead 00f0,4,4

//Read     MACRO_ERROR_IN_OPCODE=0x0; Address(0xf0[7:4])

SPIRead 00f0,5,5

//Read     MACRO_ERROR_OPCODE_NOT_ALLOWED=0x0;
      Address(0xf0[7:5])

SPIRead 00f0,6,6

//Read     MACRO_ERROR_IN_OPERAND=0x0;      Address(0xf0[7:6])

SPIRead 00f0,7,7

//Read     MACRO_ERROR_IN_EXECUTION=0x0;    Address(0xf0[7:7])

SPIRead 00f3,0,7
SPIRead 00f2,0,7

//Read     MACRO_ERROR_EXTENDED_CODE=0x0;
      Address(0xf2[7:0],0xf3[7:0],0xf4[7:0])

SPIRead 00f7,0,7
SPIRead 00f6,0,7
SPIRead 00f5,0,7
SPIRead 00f4,0,7

//Read     MACRO_ERROR_EXTENDED_CODE_2=0x0;
      Address(0xf4[7:0],0xf5[7:0],0xf6[7:0],0xf7[7:0],0xf8[7:0])

SPIWrite 0018,00,0,7  //macro=0x0;     Address(0x18[7:5])
```