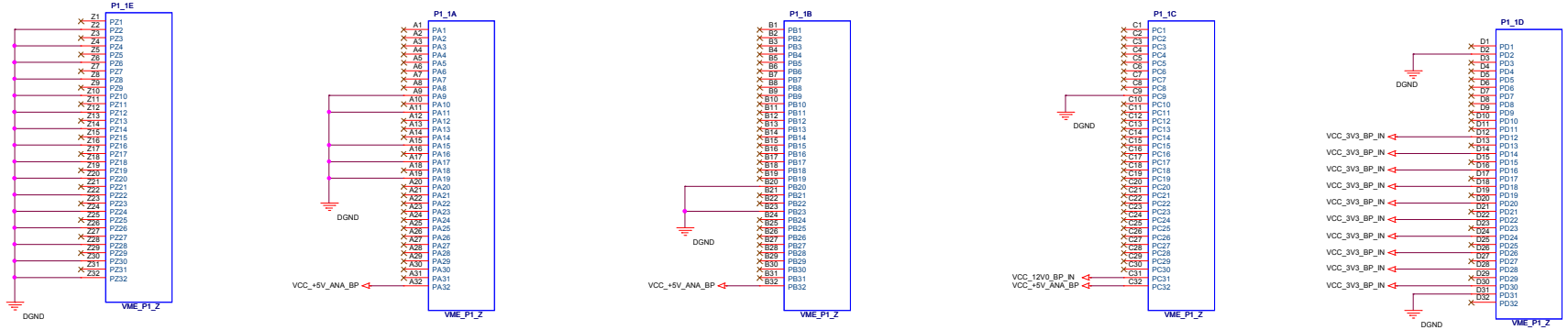
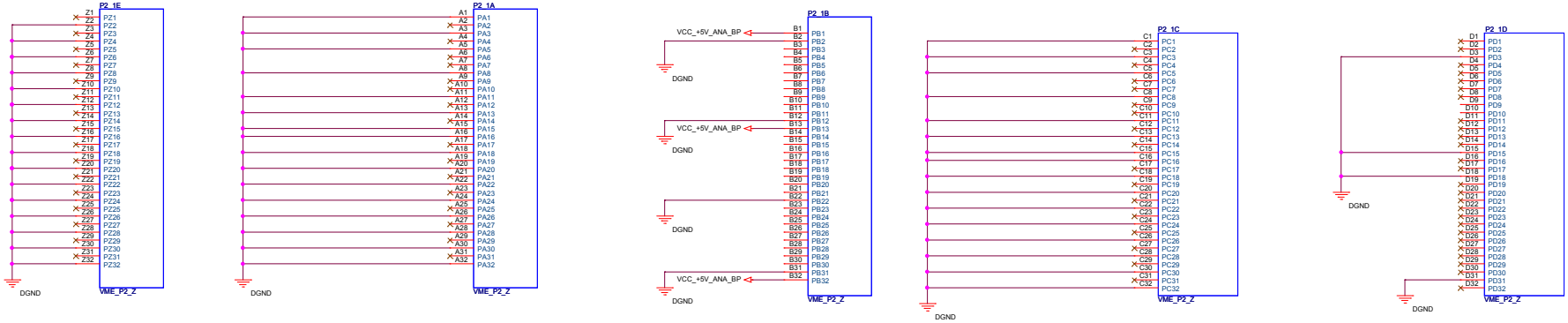
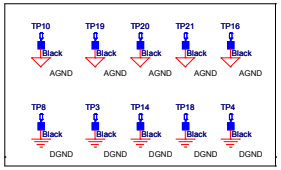
P1 CONNECTOR

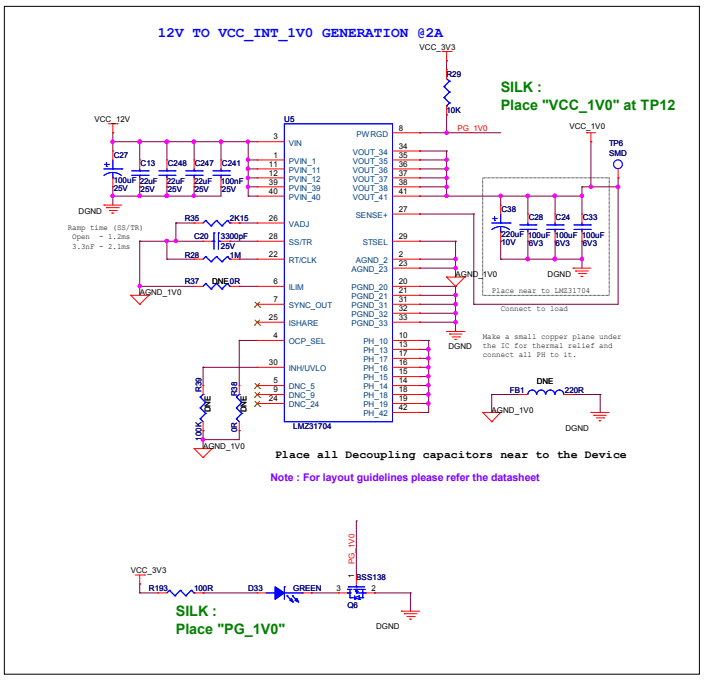


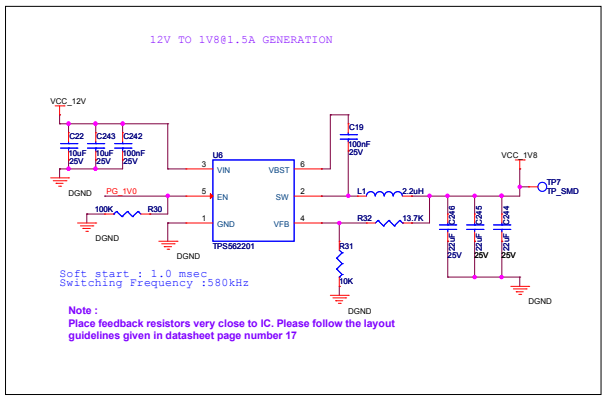
P2 connector

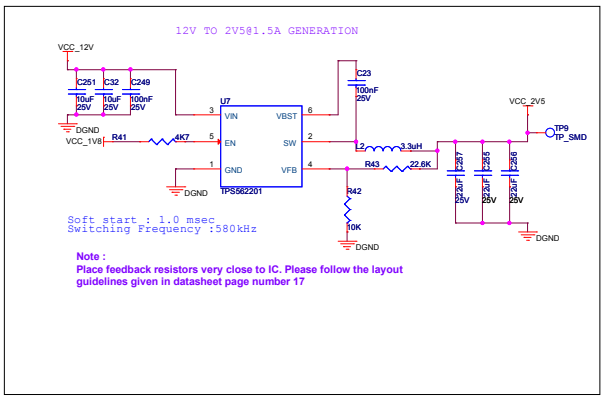


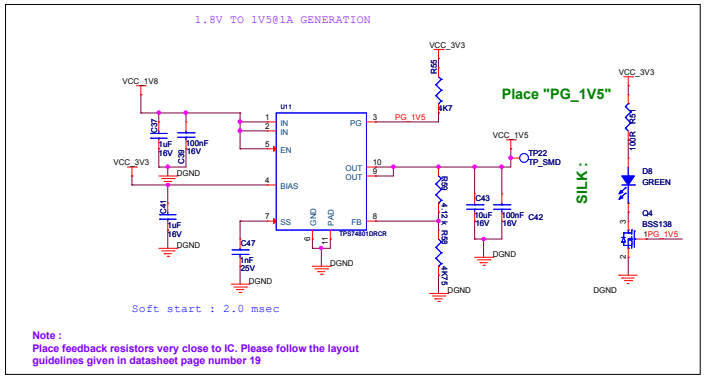


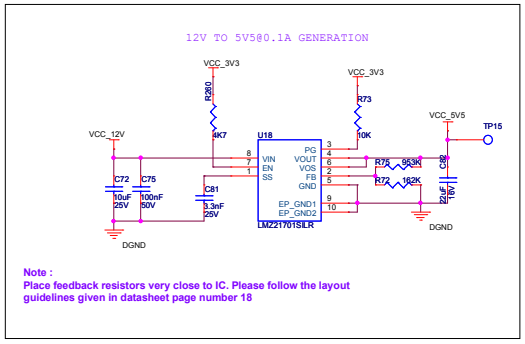
distribute test points evenly throughout

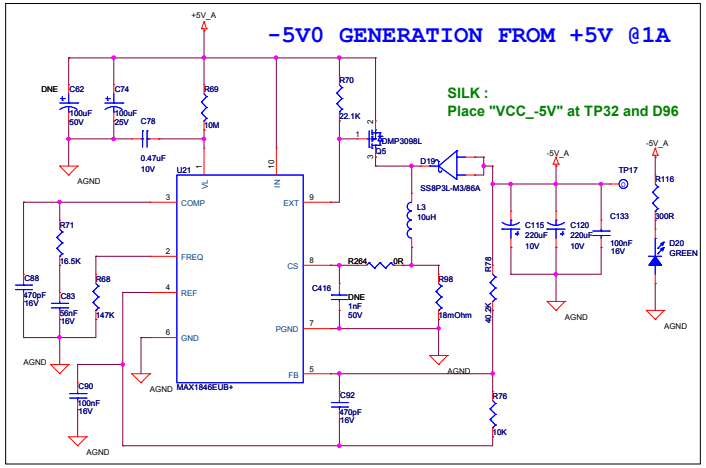

12V TO VCC_INT_1V0 GENERATION @2A
SILK :
Place "VCC_1V0" at TP12
SILK :
Place "PG_1V0"
Place all Decoupling capacitors near to the Device
Note : For layout guidelines please refer the datasheet

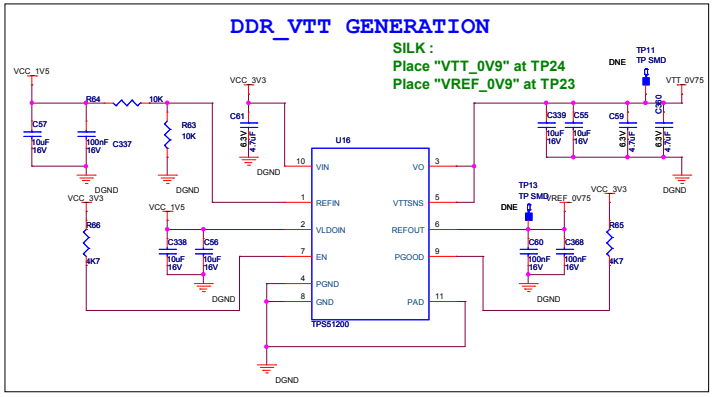

12V TO 1V8@1.5A GENERATION
Soft start : 1.0 msec
Switching Frequency :580kHz
Note :
Place feedback resistors very close to IC. Please follow the layout guidelines given in datasheet page number 17


12V TO 2V5@1.5A GENERATION
Soft start : 1.0 msec
Switching Frequency :580kHz
Note :
Place feedback resistors very close to IC. Please follow the layout guidelines given in datasheet page number 17

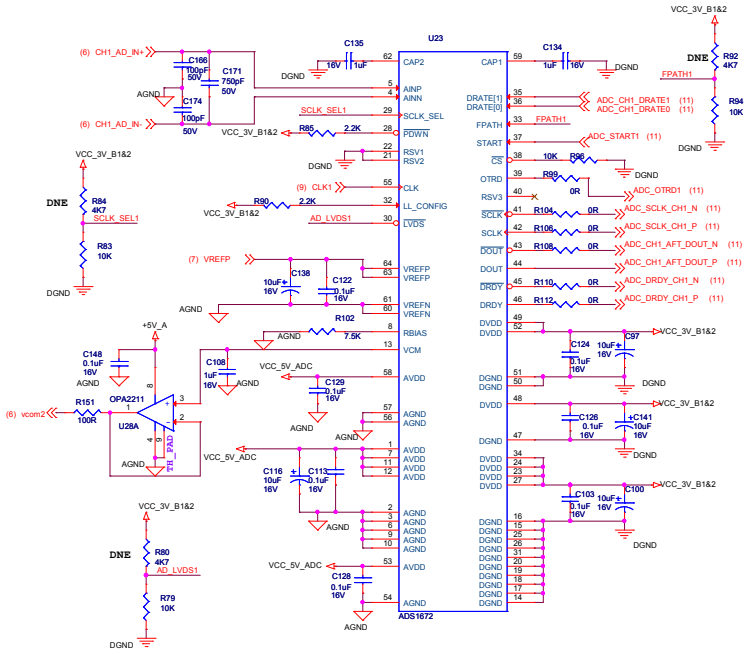

1.8V TO 1V5@1A GENERATION
Place "PG_1V5"
SILK :
Soft start : 2.0 msec
Note :
Place feedback resistors very close to IC. Please follow the layout guidelines given in datasheet page number 19


12V TO 5V5@0.1A GENERATION
Note :
Place feedback resistors very close to IC. Please follow the layout guidelines given in datasheet page number 18

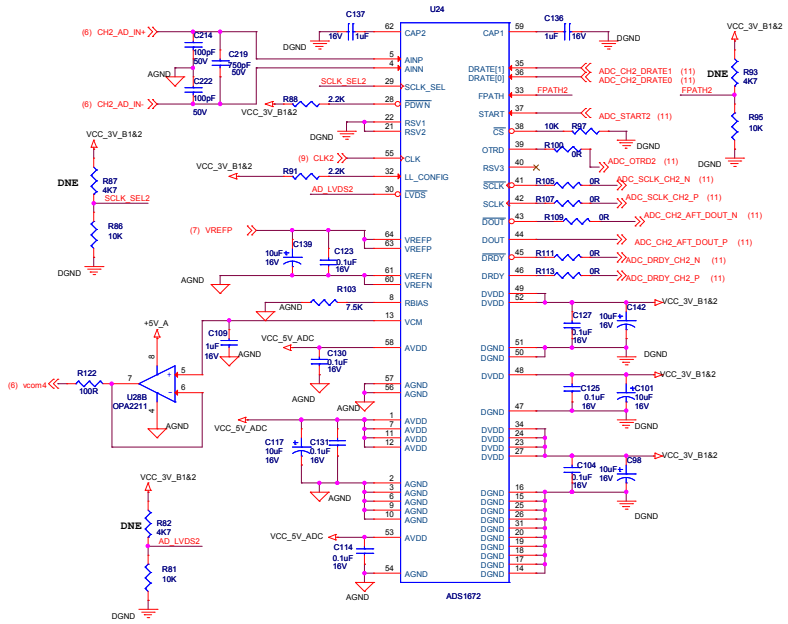

-5V0 GENERATION FROM +5V @1A
SILK :
Place "VCC_-5V" at TP32 and D96


DDR_VTT GENERATION
SILK :
Place "VTT_0V9" at TP24
Place "VREF_0V9" at TP23

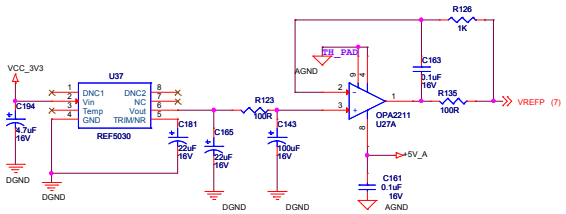
(Channel 1)



(Channel 2)

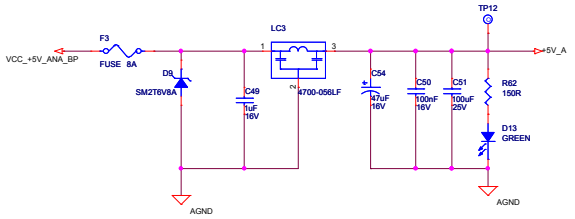


Reference voltage for ADCs

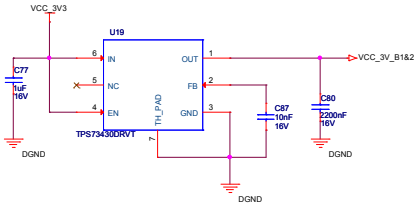


EMI FILTERS

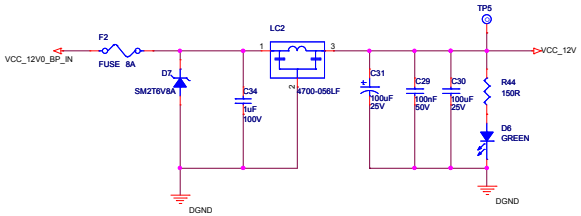
EMI FILTER +5V(A)



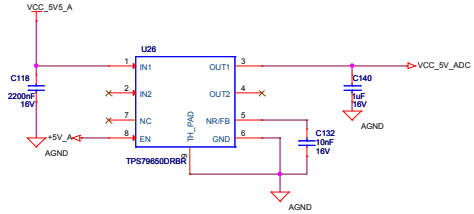
SILK :
Place "VCC_5VA" at TP29 and D61

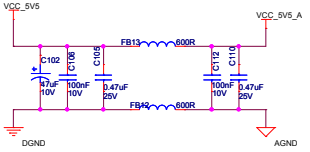


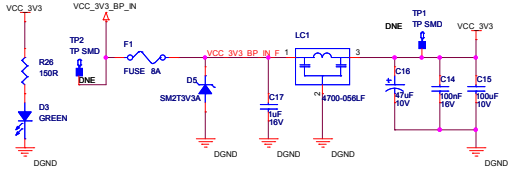
EMI FILTER +5V(A)



SILK :
Place "VCC_12V" at TP30 and D62







SILK :
Place "VCC_3V3" at TP27 and D85